POWER9 Monza Single-Chip Module Datasheet

OpenPOWER

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Revision Log

Each release of this document supersedes all previously released versions. The revision log lists all significant changes made to the document since its initial release. In the rest of the document, change bars in the margin indicate that the adjacent text was modified from the previous release of this document.

Revision Date	Description
16 August 2022	Version 1.5. • Added the PVR for DD 2.3 to *Table 1-1 POWER9 Processor Version Register* on page 16. • Revised *Section 1.11 Related Documents* on page 16. • Updated the frequency range to *Table 2-1 POWER9 SCM Technology* on page 19. • Revised the table notes in *Table 5-5 AVS Signals* on page 38. • Removed the note “Values in this table are pending hardware validation and are subject to change” from the following tables: *Table 6-1 POWER9 Frequency Domains* on page 61, *Table 6-2 POWER9 Processor V_{DD} (Core) Voltage Requirements* on page 63, *Table 6-3 POWER9 Processor V_{CS} (Cache) Voltage Requirements* on page 64, *Table 6-4 POWER9 Processor V_{DN} Voltage Requirements* on page 64, *Table 6-5 POWER9 Processor V_{IO} Voltage Requirements* on page 65, *Table 6-6 POWER9 Processor AV_{DD}/DV_{DD} Voltage Requirements* on page 65, *Table 6-7 POWER9 DDR4 Voltage Requirements* on page 66, *Table 6-8 1.1 V_{SB}: Standby/Auxiliary* on page 66, *Table 6-9 3.3 V_{SB}: Standby/Auxiliary* on page 66, *Table 6-10 Power, Frequencies, and Junction Temperature[1]* on page 68, *Table 6-12 Differential Reference Clock DC and AC Specification* on page 70, *Table 6-13 DC and AC Specifications* on page 73, *Table 6-16 SPI AC Specification* on page 76, *Table 6-18 AVS AC Specification* on page 77. • Revised *Table 6-1 POWER9 Frequency Domains* on page 61. • Revised the DC voltage parameter and the table notes in *Table 6-2 POWER9 Processor V_{DD} (Core) Voltage Requirements* on page 63. • Revised the DC voltage paramter, the load line parameter, and the table notes in *Table 6-3 POWER9 Processor V_{CS} (Cache) Voltage Requirements* on page 64. • Revised the DC voltage parameter, the maximum current load parameter, and the table notes in *Table 6-4 POWER9 Processor V_{DN} Voltage Requirements* on page 64. • Revised the DC voltage parameter, the regulation set-point tolerance parameter, and the maximum current load parameter in *Table 6-5 POWER9 Processor V_{IO} Voltage Requirements* on page 65. • Added DD2.3 part numbers in *Table 6-10 Power, Frequencies, and Junction Temperature[1]* on page 68. • Revised *Section 6.3.1 Clock AC Specifications* on page 68. • Revised the receiver V_{IL} and receiver V_{IH} parameters in *Table 6-14 FSI Electrical Specification* on page 75. • Revised the receiver V_{IL} and receiver V_{IH} parameters in *Table 6-18 AVS AC Specification* on page 77. • Revised the pull-down and pull-up internal values in *Table 6-19 Default AVS Settings* on page 77. • Revised the passing level paramters in *Table 7-2 ESD Stress Qualification* on page 80. • Revised the *Glossary* on page 115.
9 March 2018	Version 1.4. • Added 190 W frequency to *Table 2-1 POWER9 SCM Technology* on page 19. • Revised *Table 6-4 POWER9 Processor V_{DN} Voltage Requirements* on page 64. • Revised *Table 6-10 Power, Frequencies, and Junction Temperature[1]* on page 68. • Added 190 W frequency to *Table 7-1 SCM Features* on page 79. • Revised the *Glossary* on page 115.

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6 February 2018	Version 1.3. • Revised *Table 2-1 POWER9 SCM Technology* on page 19. • Revised *Table 3-5 Chip P0* on page 25. • Revised *Section 4.1 Power Gating and On-Chip, Per-Core Voltage Regulation* on page 31. • Revised *Section 4.2 Efficient Power Supply Oversubscription Capability* on page 31. • Revised *Table 4-2 System Main Power Sequence* on page 34. • Revised *Section 4.4 System Power Sequencing* on page 34. • Revised *Table 6-2 POWER9 Processor V_{DD} (Core) Voltage Requirements* on page 63. • Revised *Table 6-3 POWER9 Processor V_{CS} (Cache) Voltage Requirements* on page 64. • Revised *Table 6-4 POWER9 Processor V_{DN} Voltage Requirements* on page 64. • Revised *Section 6.2.2 Power and Frequencies* on page 66. • Revised *Table 7-1 SCM Features* on page 79.
15 June 2017	Version 1.2. • Updated a URL hyperlink to the IBM Portal for OpenPOWER throughout the document. • Revised *Section 1 Introduction* on page 13. • Revised *Section 1.1 Processor Feature Summary* on page 13. • Revised *Section 1.2 Supported Technologies* on page 14. • Revised *Section 1.3 Interfaces* on page 14. • Revised *Section 1.4 Power Management Support* on page 14 • Revised *Table 1-1 POWER9 Processor Version Register* on page 16. • Revised *Table 2-1 POWER9 SCM Technology* on page 19. • Revised *Section 3.3.1 Specification Compliance* on page 24. • Revised *Table 3-5 Chip P0* on page 25. • Revised *Section 3.4 DDR4 Interface* on page 27. • Revised *Section 3.5 Inter-Node SMP X Bus* on page 28. • Revised *Section 4 Power Management* on page 31. • Revised *Table 4-1 System Standby/Auxiliary Power Sequence* on page 34. • Revised *Table 4-2 System Main Power Sequence* on page 34. • Revised *Section 4.4 System Power Sequencing* on page 34. • Revised *Table 5-4 APSS Signals* on page 38. • Revised *Table 5-5 AVS Signals* on page 38. • Revised *Table 5-6 FSI Signals* on page 39. • Revised *Table 5-14 Miscellaneous Signals* on page 53. • Revised *Table 6-2 POWER9 Frequency Domains* on page 62. • Revised *Table 6-2 POWER9 Processor V_{DD} (Core) Voltage Requirements* on page 63. • Revised *Table 6-10 Frequencies and TDP for DD1 Part Numbers1* on page 67. • Added *Table 6-11 Frequencies and TDP for DD2 Part Numbers1* on page 67. • Updated *Section 7.2 Electrostatic Discharge Considerations* on page 79. • Revised the *Glossary* on page 115.
20 March 2017	Version 1.11. • Revised *Table 6-10 Frequencies and TDP for DD1 Part Numbers1* on page 67.

Revision Date	Description
16 January 2017	Version 1.1. • Changed BlueLink to 25G where appropriate in the document. • Revised *Section 1 Introduction* on page 13. • Revised *Section 1.1 Processor Feature Summary* on page 13. • Revised *Section 1.6 Signals* on page 15. • Revised *Section 1.7 Electrical* on page 15. • Revised *Section 1.8 Package Support* on page 15. • Revised *Section 1.12.2 Bit Significance* on page 17. • Revised *Table 2-1 POWER9 SCM Technology* on page 19. • Revised *Table 3-2 Inter-Node SMP X-Bus Highlights* on page 22. • Revised *Section 3.3.4 PCIe Bus* on page 25. • Revised *Table 3-5 Chip P0* on page 25. • Revised *Section 3.5 Inter-Node SMP X Bus* on page 28. • Added *Table 3-7 25G Link GPU Connectivity* on page 29. • Added *Table 3-8 25G Link OpenCAPI Connectivity* on page 30. • Revised *Section 3.7 CAPI* on page 30. • Revised *Section 5.1 Pin Naming Convention* on page 36. • Revised *Section 5.2.2 APSS Signals* on page 38. • Revised *Table 5-3 Voltage and Ground Signals* on page 37. • Added a note to *Table 5-4 APSS Signals* on page 38. • Revised *Table 5-5 AVS Signals* on page 38. • Revised *Table 5-6 FSI Signals* on page 39. • Added a note to *Table 5-7 Clock System Signals* on page 39. • Revised *Table 5-8 I^2C Signals* on page 40. • Revised *Section 5.2.7 X-Bus Signals* on page 41. • Revised *Table 5-9 X-Bus Signals* on page 41. • Revised *Table 5-10 PCIe Controller and Clock Bus Signals* on page 42. • Revised *Table 5-11 LPC Bus Signals* on page 44. • Revised *Table 5-12 Memory Signals* on page 44. • Revised *Table 5-13 JTAG Signals* on page 52 • Revised *Table 5-14 Miscellaneous Signals* on page 53. • Revised *Table 5-15 Test Signals* on page 55. • Revised a note in *Table 5-19 BEOL Sense Signals* on page 58. • Revised *Table 5-20 25G Link Signals* on page 59. • Revised *Table 6-2 POWER9 Processor V_{DD} (Core) Voltage Requirements* on page 63. • Revised *Table 6-3 POWER9 Processor V_{CS} (Cache) Voltage Requirements* on page 64. • Revised *Table 6-4 POWER9 Processor V_{DN} Voltage Requirements* on page 64. • Revised *Table 6-5 POWER9 Processor V_{IO} Voltage Requirements* on page 65. • Revised *Table 6-6 POWER9 Processor AV_{DD}/DV_{DD} Voltage Requirements* on page 65. • Revised *Table 6-7 POWER9 DDR4 Voltage Requirements* on page 66. • Revised *Section 6.2.3 Miscellaneous Signals* on page 68. • Revised *Section 6.3.1 Clock AC Specifications* on page 68. • Removed tables previously known as *Table 6-8 DIMM V_{TT} Voltage Requirements* and *Table 6-9 DIMM V_{PP} Voltage Requirements*. • Revised *Table 6-8 1.1 V_{SB}: Standby/Auxiliary* on page 66. • Revised *Table 6-9 3.3 V_{SB}: Standby/Auxiliary* on page 66. • Revised *Table 6-17 Default SPI Settings* on page 76. • Revised *Section 6.3.5 AVS AC Specifications* on page 77. • Revised note in *Table 6-18 AVS AC Specification* on page 77. • Removed the Pull-Up column in *Table 6-19 Default AVS Settings* on page 77. • Revised *Section 6.3.5.1 Recommended AVSBus Topology* on page 78. • Revised *Table 7-1 SCM Features* on page 79. • Revised the *Glossary* on page 115.
26 August 2016	Version 1.0 (initial version).

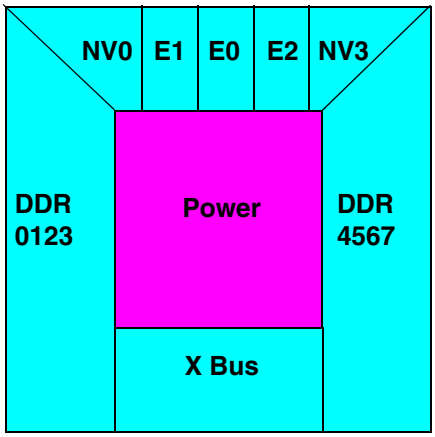
1. Introduction

This datasheet describes the IBM® POWER9™ processor in the Monza single-chip module (SCM). The POWER9 processor is a superscalar symmetric multiprocessor designed for use in servers and large-cluster systems. It uses CMOS 14 nm technology with 17 metal layers.

The POWER9 processor can have up to 24 cores enabled on a single chip. It supports direct-attach memory, a maximum symmetric multiprocessing (SMP) size of two sockets, and is targeted for scale-out workloads. Each POWER9 core supports up to four threads using simultaneous multithreading (SMT). The SMT can be dynamically tuned so that each core has one, two, or four threads.

Figure 1-1 illustrates the POWER9 pinout diagram.

Figure 1-1. POWER9 Pinout Map



1.1 Processor Feature Summary

The POWER9 processor consists of the following main components:

- Twenty-four POWER9 cores with shared L2 and L3 caches and a noncacheable unit (NCU)
- On-chip accelerators.
  - CAPI allows an FPGA or ASIC to connect coherently to the POWER9 processor SMP interconnect via the PCIe bus.
  - On-chip: compression, encryption, data move initiated by the hypervisor, GZIP engine, or nest MMU to enable user access to all accelerators.
  - In-core: user invocation encryption (AES, SHA).
- Two memory controllers that support direct-attached DDR4 memory.
  - Supports eight direct-attach memory buses.
  - Supports ×4 and ×8, 4 - 16 Gb DRAMs and 3D stacked DRAMs.
  - Supports RDIMMs and LRDIMMs.

- Processor SMP interconnect.
  - Supports one inter-node SMP X-bus link.
  - Maximum two-socket SMP.
- Six 25G Link bricks with support for OpenCAPI 3.0 and NVIDIA® NVLink™ 2.0 interconnect.
- Three PCIe controllers (PEC) with 34 lanes of PCI Express Gen4 I/O.
  - PEC0: one ×16 lanes.
  - PEC1: two ×1 lanes (bifurcation).
  - PEC2: one ×16 lane mode, two ×8 lanes (bifurcation), or one ×8 lane and two ×4 lanes (trifurcation).
  - PEC0 and PEC2 support CAPI 2.0.
- Power management.
- Pervasive interface.

1.2 Supported Technologies

The POWER9 processor supports the following technologies:

- Power ISA Book I, II, and III (version 3.0)
- Linux on Power Architecture Platform Reference
- IEEE P754-2008 for binary and decimal floating-point compliant
- Big-endian, little-endian, strong-ordering support extension
- 51-bit real address, 68-bit virtual address

1.3 Interfaces

The primary service interface to the POWER9 processor is the field replaceable unit (FRU) service interface (FSI) that runs at 166 MHz. See *Section 3.1 Service Interfaces* on page 21 for more information.

1.4 Power Management Support

Key features of the POWER9 processor are as follows:

- Hypervisor-directed power change requests using the Pstate mechanism
  - Core/L2/L3 instant on and off
  - Halt state support
  - Controlled by 17 on-chip programmable PPE engines
  - Dynamic lane width reduction (SMP interconnect fabric, PCI)
- Sensors
  - Digital thermal sensor (DTS2) ±5°C
  - Off-chip analog thermal diode ±1 - 2°C

  - Voltage drop monitor
  - Dedicated performance, microarchitecture, and event counters
- Accelerators
  - On-chip IBM PowerPC® 405 embedded processor core for thermal management control
  - On-chiplet hardware assist (automated core chiplet management)
  - On-chip power management controls
    - Automated communications to the voltage regulation modules (VRMs)
    - Voltage and frequency sequencers for automated Pstate and idle state support
- Actuators
  - Per quad chiplet frequency control through the DPLL
  - Architected idle states: nap, sleep, and winkle; each with increasing power savings capability (and latency)
  - SPR power management control registers (PMCR, PMICR, and PMSR) for hypervisor support
- Memory and DIMM throttling for memory subsystem power and thermal management

1.5 Thermal Specification

Thermal junction temperature (T_J) is measured by digital thermal sensors located on the chip. There are four sensors per core, which are averaged. The specified T_J is the worst case of these averages or the hottest core average. The maximum T_J is not allowed to exceed 85°C. The average T_J, at which the reliability is calculated, is 70°C. Margin does not need to be applied when measuring against the worst-case specification because the chip is sorted using the same thermal sensors. The digital thermal sensor has an absolute accuracy of ±5% and can be read out in Celsius (°C).

1.6 Signals

Section 5 Signals on page 35 describes the POWER9 Monza SCM signals.

1.7 Electrical

Section 6 Electrical Characteristics on page 61 discusses the DC and AC electrical characteristics of the POWER9 Monza SCM.

1.8 Package Support

Section 7 Mechanical Specifications on page 79 describes the POWER9 Monza SCM features and provides a pin list.

1.9 Processor Version Register

The POWER9 processor has the following Processor Version Register (PVR) values for the respective design revision levels.

Table 1-1. POWER9 Processor Version Register

POWER9 Design Revision Level	POWER9 PVR
DD 2.1	x'004E1201'
DD 2.2	x'004E1202'
DD 2.3	x'004E1203'

1.10 Marking Specification

The POWER9 Monza single-chip module (SCM) marking drawing FC PLGA can be found in the IBM Portal for OpenPOWER. See the *POWER9 Thermal and Mechanical Reference Guide for the Monza SCM* document.

1.11 Related Documents

The following documents can be helpful when reading this specification. Contact your IBM representative to obtain any documents that are not available through the IBM Portal for OpenPOWER, an online IBM technical library or the OpenPOWER Foundation web site.

POWER9 Processor DD 2.1 Use Restrictions Application Note

POWER9 Processor SCM Hardware Errata Notice DD 2.2

For the Development of an Electrostatic Discharge Control Program for – Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices) (ANSI/ESD S20.20-2007)

For the Protection of Electrostatic Discharge Susceptible Items - Packaging Materials for ESD Sensitive Items (ANSI/ESD S541-2008)

I²C Bus Specification (Version 2.1)

PMBus Specification v1.3.1

PCI Express Base Specification, Revision 4.0

1.12 Conventions

This section explains the number, bit field, instruction, and signal conventions that are used in this document.

1.12.1 Representation of Numbers

Numbers are generally shown in decimal format, unless designated as follows:

- Hexadecimal values are preceded by an “x” and enclosed in single quotation marks.
  For example: x‘0A00’.
- Binary values in sentences are shown in single quotation marks.
  For example: ‘1010’.

Note: A bit value that is immaterial, which is called a “don't care” bit, is represented by an “x.”

1.12.2 Bit Significance

In the POWER9 documentation, big-endian notation is usually used. That is, the smallest bit number represents the most significant bit of a field, and the largest bit number represents the least significant bit of a field.

1.12.3 Typographical Conventions

Convention	Description
Footnote reference.[1] 1. Descriptive footnote text.	A footnote is an explanatory note or reference inserted at the foot of the page or under a table that explains or expands upon a point within the text or indicates the source of a citation or peripheral information.
Hyperlink	Web-based URLs are displayed in blue text to denote a virtual link to an external document. For example: http://www.ibm.com
Italic typeface	The italic typeface denotes user-specified components when describing command usage and functionality.
`Monospaced` typeface	The monospaced typeface is used for code examples and for commands in general descriptions.
Note: This is note text.	The note block denotes information that emphasizes a concept or provides critical information.
Underline	An underline indicates that the definition of an acronym is displayed when the user hovers the cursor over the term.

2. Technologies

This section provides a high-level overview of the technologies implemented in the POWER9 processor.

2.1 General Parameters

Table 2-1 lists general parameters for the POWER9 processor.

Table 2-1. POWER9 SCM Technology

Feature	Description
Technology	CMOS 14 nm technology with 17 metal layers
Die Size	695 mm^2
Chip Package (SCM)	See *Table 7-1 SCM Features* on page 79 for details.
Signal I/O	3899
Frequency Range	2.46 - 3.8 GHz
Power	190 W and 250 W

3. Interfaces

This section describes the interfaces supported on the POWER9 processor.

3.1 Service Interfaces

The POWER9 processor has multiple service interfaces that are used for initialization during boot. The service interfaces are also accessible by using the debug box. The primary entry point to the POWER9 processor service interface is the FRU service interface (FSI), a serial interface that runs at 166 MHz.

The POWER9 SCM provides the following FSIs:

- One FSI slave for connecting to the debug box or multichip SMP.
- One FSI master for communication to a second POWER9 chip in the system. One POWER9 chip is defined as the master and is responsible for initializing the other POWER9 chip over this FSI.

The POWER9 SCM provides the following additional service interfaces:

- Two adaptive voltage scaling (AVS) buses for controlling processor-related voltage regulators.
- One SPI master for on-chip controller (OCC) management.
- One LPC bus for connecting to the BMC.
- Six I^2C masters for controlling LEDs, PCIe cards, DDR, and so on. The I^2C masters can be manipulated from the OCC or hostboot code.

3.2 Supported Processor Interfaces

This section gives an overview of the physical layer and on-chip initialization provided by the POWER9 processor.

The POWER9 processor supports the following types of drivers and receivers:

- X-bus interface: high-speed differential at 16 Gbps for chip-to-chip interconnect
- DDR4 PHY memory interface
- 25G Link interface

Table 3-1 lists the requirements relative to the operational mode definitions.

Table 3-1. Interface Operational Mode Definitions

Mode Name	Definition
Initialization	The act of aligning and locking the data eye and bit lanes plus additional deltas relative to re-alignment and re-locking.
Functional	Passing workload data and maintaining signal integrity post-initialization.
Power Saving	All related capabilities for minimizing unused and idle lane power consumption.
Test	Capabilities related to hardware manufacturability.
Diagnostic	Bringup lab characterization of interface performance capabilities.

3.2.1 Inter-Node SMP Bus Highlights

Table 3-2 highlights the inter-node SMP X bus. See the *POWER9 Processor User's Manual* for additional information.

Table 3-2. Inter-Node SMP X-Bus Highlights

Feature	Inter-Node SMP X Bus
Frequency	16 Gbps
Initialization Mode Requirement	16 Gbps, 9.6 Gbps
Spare Lane Detect	Data failover Two signals total per bus/port
Functional Mode Specification	16, 9.6 Gbps
Power-Saving Mode Requirement	Power-saving mode supports light power down with fast wakeup
Test Mode Requirement	16 Gbps, 9.6 Gbps[1]
Driver Features	• 16 Gbps with 8:1 serializer. • 9.6 Gbps in 4:1 serializer mode. • Full-rate SST driver. • Selectable 8:1 or 4:1 serializer with pre-cursor FFE. • R_{PRE} up to 1.30. • Selectable AC boost: analog post-cursor FFE. • Set and forget impedance calibrator. • Drive amplitude reduction (margining) up to 50%. For characterization only, not mission mode. • BIST error detector for at-speed loopback testing. • Shared test pin mode. Differential driver output only. • Time domain reflectometer (TDR).
Receiver Features	• RX clock macro with PLL – Same I/O specifications as the POWER8 processor: 2.0 - 2.4 GHz bus clock range – Programmable feedback divider for POWER8 memory buffer backward compatibility • RX data macro – Each data bit with a single data path (single bank) using shadow-lane protocol for calibration – Long-tail equalizer (LTE) for improved eye margins on lossiest channels – Continuous time linear equalizer (CTLE) with 12 dB of peaking range, 6 dB of gain range – CTLE applies common mode (differential zero) for DAC calibrations – 12-tap DFE with current integrating summer. Modes: no-DFE, DFE1, DFE12) – 16 Gbps with 1:8 deserialization mode – 9.6 Gbps with 1:4 deserialization mode – Cross-coupled PRBS streams for RX BIST testing

1. Subject to PLL range limitations and a test frequency of 200 MHz.

3.2.2 25G Link Interface

Table 3-3 highlights the 25G Link interface, which supports the following drivers and receivers: OpenCAPI 3.0 and NVLink 2.0 interconnect. See the *POWER9 Processor User's Manual* for additional information.

Table 3-3. 25G Link Interface Highlights

Feature	25G Link Bus
Frequency	25.78125 Gbps, 19.2 Gbps
Initialization Mode Requirement	25.78125 Gbps, 19.2 Gbps
Spare Lane Detect	–
Functional Mode Specification	25.78125 Gbps, 19.2 Gbps
Power-Saving Mode Requirement	No power-saving mode support
Test Mode Requirement	25.78125 Gbps, 19.2 Gbps
Driver Features	• 16:1 serializer. • Half-rate SST with precursor FFE, amplitude margin function, and impedance calibration. • Selectable AC boost: precursor FFE. • Set and forget impedance calibrator. • Drive amplitude reduction (margining) up to 50%. For characterization only, not mission mode. • Full TX power-down mode when port is not required. • Individual TX lane power-down mode when lanes are not required. • BIST error detector for at-speed loopback testing. • Shared test pin mode. Differential driver output only. • Time domain reflectometer.
Receiver Features	• CTLE peaking. • Gain calibration. • 1-tap speculative DFE. • Local offset calibration compatible with floating body devices. • Common mode calibration. • Recovered clock. • SCOM support. • JTAG wire test support. • Eye metrics available on spare lanes with full vertical and horizontal eye scan capability. • Full RX power-down mode when group is not required. • Individual RX lane power-down mode when lanes are not required. • CDR must run continuously. • Other parameters are calibrated every 50 ms.

3.3 PCI Express Controller

The PCI Express controller (PEC) bridges between the internal processor bus and the high-speed serial (HSS) links that drive the PCI Express I/O. The PEC acts as a processor bus master on behalf of the PCI Express port, converting inbound memory read and write packets into processor bus DMA traffic. The PEC also acts as a processor bus slave, transferring processor load and store commands to the PCI Express devices attached to the port.

3.3.1 Specification Compliance

The PEC is compliant with the following IBM and industry standards:

- *Linux on Power Architecture Platform Reference*
- *I/O Design Architecture v2 (IODA2) Specification, Version 2.4+*
- *PCI Express Base Specification Revision 4.0*

3.3.2 PEC Feature Summary

- PCI Express Gen4 root complex (RC)
  - Backwards compatible with generation 1, generation 2, and generation 3
  - 2.5, 5, 8, and 16 GTps signalling rate
- Thirty-four PCIe I/O lanes configurable to six independent root complexes
- Each root complex has 256 partitionable endpoints (PE) for LPAR support
- TCE-based address translation for DMA requests
  - 51-bit address support
  - Translation validation table based on PCI routing ID
- 2048 MSI interrupts per RC
- Eight LSI interrupts per RC
- IBM enhanced error handling (EEH) support
- Processor bus cache-inhibited space segmented by PEC
  - PCI 32-bit memory space segmented into 256 domains by the memory domain table
  - PCI 64-bit memory space segmented by 16 M64 BARs with 16 segments each
- Support for ECRC
- Support for lane wrapping
- Support for PCIe atomic operations and TLP hints

3.3.3 Supported Configuration

The 34 lanes of HSS I/O can be configured to support six independent PCIe buses. *Table 3-4* describes the maximum lane allocation. In addition to supporting PCI operations, the HSS I/O can be allocated for use by the processor bus SMP interface.

Table 3-4. Supported I/O Configurations

PECx	PHB0	PHB1	PHB2	PHB3	PHB4	PHB5
PEC0	´16					
PEC1		´1	´1			
PEC2				´16		
				´8	´8	
				´8	´4	´4

3.3.4 PCIe Bus

The POWER9 Monza SCM has a total of 34 PCIe Gen4 lanes. There are three PCIe controllers per processor. The number of PHBs per PEC is variable.

- PEC0 has a single PHB that is non-bifurcatible, ×16 lanes, and CAPI capable.
- PEC 1 has two PHBs that are each ´1 lane. PEC1 does not support CAPI.
- PEC2 contains up to three PHBs. PEC2 can be run as a single ×16 interface, two ×8 lanes, or a single ×8 lane plus two ×4 lanes. PEC2 is CAPI enabled only as a ×16 interface or the first ×8 lane.

Note: The lanes can be reversed for easier routing if required. The polarity can also be reversed on a lane-by-lane basis.

Table 3-5. Chip P0 (Sheet 1 of 2)

Chip	Interface	Mode	Pins		Notes
P0	E0	×16	Data Lanes	Receive: PE_E0_PIN_P_P0_DAT_[00:15]_P/N Transmit: PE_E0_P0_P_PIN_DAT_[00:15]_P/N	
			Clocks	PV_E0_P0_P_PIN_SLOT_CLK_P/N	1, 2
			Reset	$\overline{\text{PV\_E0\_P0\_P\_PIN\_PERST\_B}}$	3, 4
			Present	$\overline{\text{PV\_E0A\_PIN\_P\_P0\_PRSNT\_B}}$	4, 5
				$\overline{\text{PV\_E0B\_PIN\_P\_P0\_PRSNT\_B}}$	5

1. This bus is ×16 mode only (non-bifurcatible). Thus, there is only one slot clock.
2. A 49.9 Ω pull-down to GND is required on each of the nets of a clock pair whether the bus is used or unused.
3. If this bus is used, include a 3.3 KΩ pull-down resistor to GND. If the bus is not used, this pin should be tied-off with a 3.3 KΩ pull-up resistor to 3.3 V_{AUX}.
4. PERST and PRSNT are 3.3 V tolerant. Pull-ups should be to the same rail as used to power the VSB_V3P3.
5. For PRSNT signals, if the bus goes to a PCIe slot, use a 3.3 KΩ pull-up to 3.3 V_{AUX}. If the bus is wired to a device that is always present, use a 49.9 Ω pull-down resistor to GND. Unused PRSNT signals (such as, PV_E0B_PIN_P_P0_PRSNT_B) are tied-off with a 3.3 KΩ pull-up to 3.3 V_{AUX}.
6. This bus can be bifurcated into the following modes: ×16, ×8 + ×8, or ×8 + ×4 + ×4.

Table 3-5. Chip P0 (Sheet 2 of 2)

Chip	Interface	Mode	Pins		Notes
P0	E1	×1	Data Lanes	Receive: PE_E1_PIN_P_P0_DAT_07_P/N Transmit: PE_E1_P0_P_PIN_DAT_07_P/N	
			Clocks	PV_E1A_P0_P_PIN_SLOT_CLK_P/N	
			Reset	$\overline{\text{PV\_E1A\_P0\_P\_PIN\_PERST\_B}}$	3, 4
			Present	$\overline{\text{PV\_E1A\_PIN\_P\_P0\_PRSNT\_B}}$	4, 5
P0	E1	×1	Data Lanes	Receive: PE_E1_PIN_P_P0_DAT_08_P/N Transmit: PE_E1_P0_P_PIN_DAT_08_P/N	
			Clocks	PV_E1B_P0_P_PIN_SLOT_CLK_P/N	
			Reset	$\overline{\text{PV\_E1B\_P0\_P\_PIN\_PERST\_B}}$	3, 4
			Present	$\overline{\text{PV\_E1B\_PIN\_P\_P0\_PRSNT\_B}}$	4, 5
P0	E2	×16	Data Lanes	Receive: PE_E2_PIN_P_P0_DAT_[00:15]_P/N Transmit: PE_E2_P0_P_PIN_DAT_[00:15]_P/N	6
			Clocks	PV_E2A_P0_P_PIN_SLOT_CLK_P/N PV_E2B_P0_P_PIN_SLOT_CLK_P/N PV_E2C_P0_P_PIN_SLOT_CLK_P/N	2
			Reset	PV_E2A_P0_P_PIN_PERST_B PV_E2B_P0_P_PIN_PERST_B PV_E2C_P0_P_PIN_PERST_B	3, 4
			Present	PV_E2A_PIN_P_P0_PRSNT_B PV_E2B_PIN_P_P0_PRSNT_B PV_E2C_PIN_P_P0_PRSNT_B	4, 5

1. This bus is ×16 mode only (non-bifurcatible). Thus, there is only one slot clock.
2. A 49.9 Ω pull-down to GND is required on each of the nets of a clock pair whether the bus is used or unused.
3. If this bus is used, include a 3.3 KΩ pull-down resistor to GND. If the bus is not used, this pin should be tied-off with a 3.3 KΩ pull-up resistor to 3.3 V_{AUX}.
4. PERST and PRSNT are 3.3 V tolerant. Pull-ups should be to the same rail as used to power the VSB_V3P3.
5. For PRSNT signals, if the bus goes to a PCIe slot, use a 3.3 KΩ pull-up to 3.3 V_{AUX}. If the bus is wired to a device that is always present, use a 49.9 Ω pull-down resistor to GND. Unused PRSNT signals (such as, PV_E0B_PIN_P_P0_PRSNT_B) are tied-off with a 3.3 KΩ pull-up to 3.3 V_{AUX}.
6. This bus can be bifurcated into the following modes: ×16, ×8 + ×8, or ×8 + ×4 + ×4.

3.4 DDR4 Interface

The POWER9 processor incorporates DDR PHY memory interface physical units capable of supporting several memory topologies. It is optimized for DDR4 memories, as defined by the JEDEC, and incorporates all of the required features and many optional ones.

At a high level, the DDR unit is responsible for:

- Transporting and mapping command, control, address, and data signals presented from the embedded memory controller.
- Providing all necessary configuration registers, state machines, control logic, and status monitoring to execute all required DDR calibration functions (that is, read calibration, fine and coarse write leveling, ZQ calibration, and so on).
- Providing elastic interface style FIFOs (PHYs) for purposes of sampling, de-skewing, bit aligning incoming data, buffering, and launching outgoing data. These FIFOs also assist in crossing clock domains.

Each DDR unit is self-contained and consists of four independent ports that connect to DIMM slots. This unit is replicated twice on the POWER9 processor to provide a maximum of eight ports.

The DDR PHY supports the following memory devices on each port.

- DDR4 RDIMMs and DDR4 LRDIMMs, including 3D stacks up to eight high
- DRAM data widths of ×4 and ×8
- DRAM densities of 4 Gb, 8 Gb, 12 Gb, and 16 Gb
- One or two DIMMs per port
- DRAM speeds of 1866, 2133, 2400, and 2666 Mbps

To accommodate DRAM timing variability, and POWER9 process, voltage, and temperature corners, the DDR PHY implements the following calibration sequences:

- Write leveling
- DQS alignment
- Read clock alignment
- Read centering
- Write centering
- Coarse write alignment
- Coarse read alignment
- TX output impedance calibration

To accommodate voltage and temperature drifts, DQS alignment, read clock alignment, and read centering can be run periodically after the initial calibrations.

The DDR PHY on the POWER9 processor supports two ranks per DIMM, and enables rank-switching in three memory clock cycles or fewer, depending on the speed of operation and device type. The maximum DDR PHY read latency is five memory cycles.

To support DDR4 JEDEC specifications above speeds of 2400 Mbps, the following features are supported:

- Programmable preamble
- CRC support
- RX V_{REF} training

Other features include:

- Per buffer addressability mode (PBA)
- Per DRAM addressability mode (PDA)
- DDR4 maximum power-saving mode
- Per-bit tuning on all address, command, control, clock, data, and strobe signals
- Programmable output impedance and slew rates
- Rank grouping feature
- Extensive RAS support
- Power-down modes
- Custom calibration modes to support custom calibration patterns

3.5 Inter-Node SMP X Bus

The POWER9 processor brings out one X-bus link on the Monza SCM. The X-bus link connects up to two POWER9 processor chips in a system. The X-bus link carries both coherency traffic and data and is inter-changeable as an inter-group processor link.

The differential X bus contains two clock groups. Each clock group consists of one clock, 16 data lanes, and one spare data lane. Both clock groups must be connected to the same processor. The X bus runs at 16 Gbps. Peak bandwidth is 60 GBps per link with a peak data bandwidth of 48 GBps due to CRC.

Note: CLK Group A within each bus must always connect to CLK Group A on another processor. Never connect CLK Group A to CLK Group B.

3.6 25G Link Bus

The POWER9 Monza SCM brings out six 25G Link interconnect bricks that provide a high-bandwidth cache-coherent interface between a POWER9 processor and a GPU cluster. Each 25G Link brick is composed of eight lanes and supports the peak bandwidth shown in *Table 3-6*.

Table 3-6. 25G Link Peak Bandwidths per Brick

Workload	25G Link Bandwidth (GBps)	Effective Bandwidth (GBps) with Command Overhead	Chip Total Effective Bandwidth
Read	25	23.5	141
Write	25	21.1	127

Table 3-7. 25G Link GPU Connectivity

25G Link Brick	RX Nets	TX Nets	Notes
Brick 1	NV_NV0_PIN_P_P0_DAT_[00:03]_P/N	NV_NV0_P0_PIN_P_DAT_[00:03]_P/N	
	NV_NV0_PIN_P_P0_DAT_[07:10]_P/N	NV_NV0_P0_PIN_P_DAT_[07:10]_P/N	
Brick 2	NV_NV0_PIN_P_P0_DAT_[04:06]_P/N	NV_NV0_P0_PIN_P_DAT_[04:06]_P/N	1
	NV_NV0_PIN_P_P0_DAT_[11:12]_P/N	NV_NV0_P0_PIN_P_DAT_[11:12]_P/N	1
	NV_NV0_PIN_P_P0_DAT_[17:19]_P/N	NV_NV0_P0_PIN_P_DAT_[17:19]_P/N	1
Brick 3	NV_NV0_PIN_P_P0_DAT_[13:16]_P/N	NV_NV0_P0_PIN_P_DAT_[13:16]_P/N	
	NV_NV0_PIN_P_P0_DAT_[20:23]_P/N	NV_NV0_P0_PIN_P_DAT_[20:23]_P/N	
Brick 4	NV_NV3_PIN_P_P0_DAT_[00:03]_P/N	NV_NV3_P0_PIN_P_DAT_[00:03]_P/N	
	NV_NV3_PIN_P_P0_DAT_[07:10]_P/N	NV_NV3_P0_PIN_P_DAT_[07:10]_P/N	
Brick 5	NV_NV3_PIN_P_P0_DAT_[04:06]_P/N	NV_NV3_P0_PIN_P_DAT_[04:06]_P/N	1
	NV_NV3_PIN_P_P0_DAT_[11:12]_P/N	NV_NV3_P0_PIN_P_DAT_[11:12]_P/N	1
	NV_NV3_PIN_P_P0_DAT_[17:19]_P/N	NV_NV3_P0_PIN_P_DAT_[17:19]_P/N	1
Brick 6	NV_NV3_PIN_P_P0_DAT_[13:16]_P/N	NV_NV3_P0_PIN_P_DAT_[13:16]_P/N	
	NV_NV3_PIN_P_P0_DAT_[20:23]_P/N	NV_NV3_P0_PIN_P_DAT_[20:23]_P/N	

1. NV_NV0_PIN_P_P0_DAT_[04:06, 11:12, 17:19]_P/N and NV_NV0_P0_PIN_P_DAT_[04:06, 11:12, 17:19]_P/N are unused for this application and should be left N/C.

3.7 CAPI

The coherent accelerator processor interface (CAPI) allows an FPGA or ASIC accelerator to connect coherently to the POWER9 SMP interconnect via the PCIe or the 25G Link interface.

The POWER9 Monza SCM provides a high-throughput CAPI-attach option over the 25G Link interface with four links available that supports a 25.78 Gbps transfer rate.

Table 3-8. 25G Link OpenCAPI Connectivity

25G Link Brick	RX Nets	TX Nets	Notes
Brick 1	NV_NV0_PIN_P_P0_DAT_[00:03]_P/N	NV_NV0_P0_PIN_P_DAT_[00:03]_P/N	
	NV_NV0_PIN_P_P0_DAT_[07:10]_P/N	NV_NV0_P0_PIN_P_DAT_[07:10]_P/N	
Brick 2	NV_NV0_PIN_P_P0_DAT_[04:06]_P/N	NV_NV0_P0_PIN_P_DAT_[04:06]_P/N	1
	NV_NV0_PIN_P_P0_DAT_[11:12]_P/N	NV_NV0_P0_PIN_P_DAT_[11:12]_P/N	1
	NV_NV0_PIN_P_P0_DAT_[17:19]_P/N	NV_NV0_P0_PIN_P_DAT_[17:19]_P/N	1
Brick 3	NV_NV0_PIN_P_P0_DAT_[13:16]_P/N	NV_NV0_P0_PIN_P_DAT_[13:16]_P/N	
	NV_NV0_PIN_P_P0_DAT_[20:23]_P/N	NV_NV0_P0_PIN_P_DAT_[20:23]_P/N	
Brick 4	NV_NV3_PIN_P_P0_DAT_[00:03]_P/N	NV_NV3_P0_PIN_P_DAT_[00:03]_P/N	
	NV_NV3_PIN_P_P0_DAT_[07:10]_P/N	NV_NV3_P0_PIN_P_DAT_[07:10]_P/N	
Brick 5	NV_NV3_PIN_P_P0_DAT_[04:06]_P/N	NV_NV3_P0_PIN_P_DAT_[04:06]_P/N	1
	NV_NV3_PIN_P_P0_DAT_[11:12]_P/N	NV_NV3_P0_PIN_P_DAT_[11:12]_P/N	1
	NV_NV3_PIN_P_P0_DAT_[17:19]_P/N	NV_NV3_P0_PIN_P_DAT_[17:19]_P/N	1
Brick 6	NV_NV3_PIN_P_P0_DAT_[13:16]_P/N	NV_NV3_P0_PIN_P_DAT_[13:16]_P/N	
	NV_NV3_PIN_P_P0_DAT_[20:23]_P/N	NV_NV3_P0_PIN_P_DAT_[20:23]_P/N	

1. NV_NV0_PIN_P_P0_DAT_[04:06, 11:12, 17:19]_P/N and NV_NV0_P0_PIN_P_DAT_[04:06, 11:12, 17:19]_P/N are unused for this application and should be left N/C.

4. Power Management

The POWER9 processor chip uses several traditional power-saving techniques to reduce peak power and thermal design-point (TDP) power. For example, latches and arrays are clock gated[1] when they are not required. Also, individual cores or full-core chiplets are dynamically power gated[2] when the cores are not in use.

The POWER9 processor uses adaptive power management techniques to reduce average power. These techniques, collectively known as IBM EnergyScale™, proactively take advantage of variations in workload, environmental condition, and overall system utilization. Coupled with a policy direction from the customer and feedback from the hypervisor or operating system that is running on the machine, this is used to determine modes of operation and the best power and performance trade-off to implement during runtime to meet customer goals and achieve the best possible performance.

4.1 Power Gating and On-Chip, Per-Core Voltage Regulation

Offering competitive chip and system designs requires the capability to dynamically adjust power consumption and performance levels to meet the needs of changing workloads. The POWER9 processor offers industry-leading features to achieve this goal.

During idle periods, each chiplet can individually power gate or “turn off” the supply to either the core or to both the core and the associated L3 cache region to reduce chiplet idle power. The gating header in the POWER9 processor is driven to an elevated voltage when off by using an on-chip charge pump. This technique increases the leakage power reduction, bringing the total DC power reduction achieved by power gating to 50 - 100x. As a result, the power-gated power consumption is less than 1% of the chiplet idle power.

Power gating can also be used to virtually eliminate the parasitic leakage power of deconfigured cores in a partial-good product offering by leaving the headers for unconfigured cores in an always gated state.

The idle power saved by power gating can be used to boost the frequency of the remaining operational cores. Using this technique, the base frequency of operating four cores can exceed the 12-core operating frequency by almost 30%.

4.2 Efficient Power Supply Oversubscription Capability

System bulk power supplies redundantly deliver worst-case power, which is significantly more power than is typically consumed. Typical workloads, parts, and environments use much less power than the worst case. Also, power delivery failure is very uncommon.

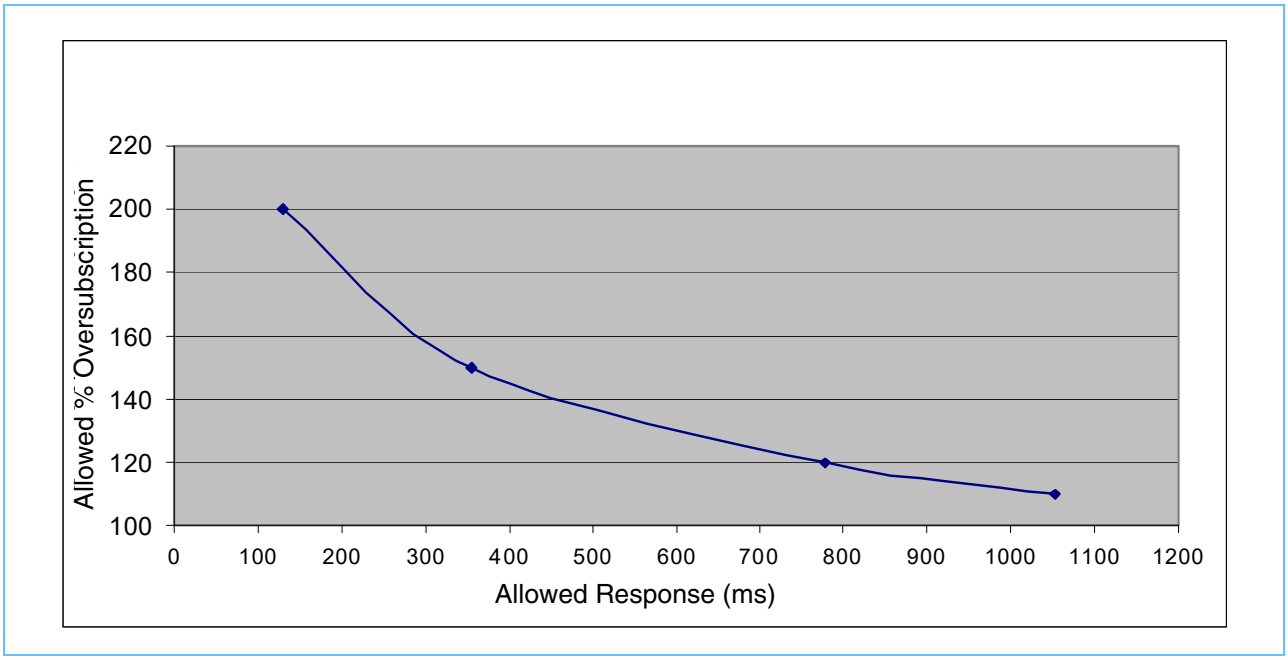
This excess power capacity can be converted into performance by using oversubscription. By oversubscribing the power supply, the processor is allowed to run at voltages and frequencies that exceed the power limit of the system under a worst-case workload and with failure of one of the redundant supplies.

Robust system operation must be maintained in spite of oversubscription. To do this, the processor must be able to throttle back power quickly enough to avoid an overcurrent condition in the remaining bulk power supply in case of a failure in the redundant supply or a sudden power spike.

1. Clock gating involves deactivating clocks for portions of a circuit that are not in use.
2. Power gating involves turning off the current to portions of a circuit that are not in use.

POWER9 systems increase oversubscription capabilities to 1.5x resulting in performance gains. The fundamental limit to power supply oversubscription is the circuit breakers in the utility or UPS when the redundant power fails. The system must be able to throttle back to consuming power less than the non-oversubscribed limit before the EXP(Current) × Time limit of the breaker is violated. *Figure 4-1* shows a representative curve of allowed oversubscription versus response time.

Figure 4-1. Oversubscriptions versus Response Time



To improve response time, a dedicated C4 pin directly signals a power-supply error to the on-chip controller (OCC).

The OCC engine can then use its internal power-actuation capabilities to rapidly reduce power. The POWER9 processor offers the following forms of power reduction:

- The OCC can force a halt in the fetch or issue of instructions to significantly reduce AC power within approximately 10 cycles.
- The OCC can use the DPLL to reduce frequency at a rate of approximately 25 MHz/µs. The AC power reduces linearly with the frequency reduction.

Using these capabilities, the POWER9 processor can reduce its power consumption in less than 5 ms after receiving the system signal indicating a power-supply failure.

The other key to enabling significant oversubscription is rapid detection of a power supply failure.

4.3 Chip Hardware Power-Management Features

4.3.1 Chiplet Voltage Control

The POWER9 processor supports several voltage regulator module (VRM) control mechanisms for multiple system configurations. The core chiplets are on a separate voltage plane than the other Nest components of the chip. The chip-level power-management control (PMC) macro and the OCC are, in combination, programmable to support these configurations.

Core chiplets all share the same voltage plane and must run with the “highest common denominator,” which means that the core demanding the highest voltage sets the value of the voltage rail. The OCC is responsible for establishing the best frequency and therefore, the voltage bounds based on the workload running, the power/performance efficiency policy selected by the customer, and the system budgets established by the thermal management component.

4.4 System Power Sequencing

The rails in *Table 4-1* must be enabled before main system power is turned on.

Table 4-1. System Standby/Auxiliary Power Sequence

Voltage Domain	Delta Time (ms)	Comments
VSB_1P10	0.1 - 20	
VSB0_3P30, VSB1_3P30	0.1 - 20	Connect VSB0_3P30 and VSB1_3P30 to the same voltage rail.

The power sequencing design must check the PGOOD status before continuing to the next step. The sequencer must allow for some amount of minimum time after PGOOD issues before continuing, as specified in *Table 4-2*.

Table 4-2. System Main Power Sequence

Voltage Domain	Delta Time (ms)	Comments
Typically, system rails associated with service processors, I/O, and storage are enabled before the processor/memory power is enabled. This guide does not cover these specifics.		
V_{PP}	0.1 - 20	Must always be greater than V_{DDR}.
V_{DN}	0.1 - 20	
AV_{DD}	0.1 - 20	This voltage can be combined for multiple POWER9 processors.
V_{IO}	0.1 - 20	
POWER9 V_{DD}	0.1 - 20	
POWER9 V_{CS}	0.1 - 20	
Additional processors can be added here in the same sequence or paralleled, so that all V_{DD} come on at the same time followed by all V_{CS}.		
V_{DDR} and V_{TT}	0.1 - 20	Must be less than 200 ms after V_{PP}. V_{TERM} tracks this domain/2 and comes on at the same time.

Notes:
1. Additional V_{PP}/V_{DDR} domains can be added in the same sequence or can be paralleled, so that they all come on together.
2. Deassert the signal to the PV_PRV_PIN_P_P0_STBY_RESET_B pin after PGOOD (SYS_PWROK) is released. It is recommend that the BMC also control the signal on this pin.

The recommendation for the power-down sequence is the reverse of the power-up sequence. V_{DN} must be brought down after AV_{DD}, V_{IO}, V_{DD}, and V_{CS}.

5. Signals

This section describes the POWER9 signal groups, which are arranged in functional groups according to their interface. *Table 5-1* lists the signal I/O type notation.

Table 5-1. Signal I/O Type Notation

Direction	Signal Type
Rec	Receiver (input).
RecDiff	Receiver differential pair signal polarity (P or N).
Drv	Driver (output).
DrvDiff	Driver differential pair signal polarity (P or N).
AnlgIn	Analog input.
AnlgOut	Analog output.
BiDi	Bi-directional input/output signal.

Table 5-2 lists the buffer types.

Table 5-2. Signal Family Type Notation

Signal	Description
Analog	Analog.
CMOS	CMOS buffers.
EDI	Elastic differential I/O.
OD	Open drain.
PCIe	PCI Express interface signals. These signals are compatible with PCI Express 3.0.

5.1 Pin Naming Convention

The general pin-naming pattern is:

prefix_source_connection type_sink_clock group_Sig Type_bit Number_diffBit_B

Prefix - the type of bus or signal type being connected. The following abbreviations are used:

DM	DDR4 memory
NX	X bus
PE	PCIe
PV	Pervasive
TS	Test

Source and Sink - the specific component and bus being connected. The following abbreviations are used:

E0	PCIe 0 bus
E1	PCIe 1 bus
E2	PCIe 2 bus
X1	X1 bus

Connection Type

P	Point-to-point
B	Bidirectional
M	Multipoint

Clock Group

CKA	Clock group A
CKB	Clock group B

Signal Type (sigType)

CLK	Clock signal
DAT	Data signal

Bit Number - bit strand number, if required; uses padding zeros.
Differential Bit (diffBit) - differential pair signal polarity (P or N), if required.
_B - denotes a negative active signal.

5.2 Signals by Group

5.2.1 Voltage and Ground Signals

Table 5-3 lists the voltage and ground signals.

Table 5-3. Voltage and Ground Signals

Signal	Description	Pin Count
AVDD_1P50	Analog V_{DD} PLL Power	2
DVDD_1P50	Digital V_{DD} PLL Power	2
VCS_0P96	V_{CS}	32
VDD_0P80	V_{DD}	163
VDDR03_1P20, VDDR47_1P20	V_{DDR}	98
VDN_0P70	V_{DN}	83
VIO_1P00	V_{IO}	31
VSB_1P10	V_{SB}	2
VSB0_3P30, VSB1_3P30	V_{SB}	4
GND	Ground	1593

5.2.2 APSS Signals

The APSS connections are only used with the first (master) processor of a system to connect to an APSS module. Use of this module is not required.

Signals on the second processor (or if no APSS is present in the system) are left as no connect (N/C); except for the MISO signal, which must be pulled down to GND through a 49.9 Ω resistor if it is unused. *Table 5-4* describes the APSS signals.

Table 5-4. APSS Signals

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
PV_APSS_P0_P_PIN_CS0	OCC SPI Chip Select	APSS	VSB0_3P30	CMOS	Drv	1	1
PV_APSS_P0_P_PIN_CS1	OCC SPI Chip Select	APSS	VSB0_3P30	CMOS	Drv	1	
PV_APSS_P0_P_PIN_MOSI	OCC SPI Master Out Slave In	APSS	VSB0_3P30	CMOS	Drv	1	1
PV_APSS_P0_P_PIN_SCLK	OCC SPI Clock	APSS	VSB0_3P30	CMOS	Drv	1	1
PV_APSS_PIN_P_P0_MISO	OCC SPI Master In Slave Out	APSS	VSB0_3P30	CMOS	Rec	1	2

1. Use a 0 Ω series resistor on the processor side of the net and connect a nopopped 47 pF capacitor to GND at the processor.
2. Use a 0 Ω series resistor on the processor side of the net, a 22 Ω series resistor at the APSS, and connect a nopopped 47 pF capacitor to GND at the processor. If the APSS SPI bus is unused, tie off MISO to GND using a 49.9 Ω resistor; other nets can be N/C.

5.2.3 AVS Signals

Table 5-5 describes the adaptive voltage scaling (AVS) signals. See the *PMBus Specification 1.3* for additional information.

Table 5-5. AVS Signals

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
PV_AVS0_P0_P_PIN_CLK	AVS 0 Clock	AVS	VIO	CMOS	Drv	1	1, 2
PV_AVS0_P0_P_PIN_MDATA	AVS 0 Master Data	AVS	VIO	CMOS	Drv	1	1, 2
PV_AVS0_PIN_P_P0_SDATA	AVS 0 Slave Data	AVS	VIO	CMOS	Rec	1	1, 2
PV_AVS1_P0_P_PIN_CLK	AVS 1 Clock	AVS	VIO	CMOS	Drv	1	1, 2
PV_AVS1_P0_P_PIN_MDATA	AVS 1 Master Data	AVS	VIO	CMOS	Drv	1	1, 2
PV_AVS1_PIN_P_P0_SDATA	AVS 1 Slave Data	AVS	VIO	CMOS	Rec	1	1, 2

1. Series resistor is 0 Ω (on the processor side).
2. Use a nopopped 47 pF capacitor to GND.

5.2.4 FSI Signals

Table 5-6 describes the FSI signals.

Table 5-6. FSI Signals

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
PV_CP1_P0_B_PIN_FSI_DAT	FSI Data Master	FSI	VSB_1P10	CMOS	BiDI	1	1, 2
PV_CP1_P0_P_PIN_FSI_CLK	FSI Clock Master	FSI	VSB_1P10	CMOS	Drv	1	1, 3
PV_FSP0_P0_B_PIN_FSI_DAT	FSI Data Slave	FSI	VSB_1P10	CMOS	BiDI	1	4
PV_FSP0_PIN_P_P0_FSI_CLK	FSI Clock Slave	FSI	VSB_1P10	CMOS	Rec	1	5
PV_PRV_PIN_P_P0_FSI_IN_ENA	FSI Enable	FSI	VSB_1P10	CMOS	Rec	1	6
PV_PRV_PIN_P_P0_FSI_SMD	FSI Secure Mode Disable	FSI	VSB_1P10	CMOS	Rec	1	6

1. Connect from the first CPU socket to the FSI slave port on the second CPU socket.
2. In a single-socket (1S) system, tie to GND with a 49.9 Ω resistor. In a two-socket (2S) system, tie processor #1 to GND with a 40.2 KΩ resistor placed near the socket and tie processor #2 to GND with a 49.9 Ω resistor.
3. N/C if unused (in a single-socket system or the second socket of a two-socket system).
4. For a single-socket system or the first processor of a two-socket system, connect to the BMC using a level translator and the debug connector through a mux (see the CRB for implementation details). Also, include a nopopped 3 KΩ pull-up to 1.1 V_{AUX} placed near the first processor. For the second processor, connect back to the FSI Master data port of the first processor and include a nopopped 3 KΩ pull-up to 1.1 V_{AUX} placed near the slave processor.
5. For a single-socket system or the first processor of a two-socket system, connect to the BMC using a level translator and the debug connector through a mux (see the CRB for implementation details). Place a nopopped 15 KΩ pull-down to GND near the first processor. For the second processor, connect back to the FSI Master clock on the first processor, and place a nopopped 15 KΩ pull-down resistor to GND near the slave processor.
6. Pull-up to 1.1 V_{AUX} using a 50 Ω resistor.

5.2.5 Clock System Signals

Table 5-7 lists the clock system signals.

Table 5-7. Clock System Signals

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
PV_SYS0_PIN_P_P0_REFCLK_N	System 133 MHz Reference Clock In	Clock System	VIO	CMOS	RecDiff	1	1
PV_SYS0_PIN_P_P0_REFCLK_P	System 133 MHz Reference Clock In	Clock System	VIO	CMOS	RecDiff	1	1
PV_PCI0_PIN_P_P0_REFCLK_N	PCIe 100 MHz Input Clock	Clock PCIe	VIO	PCIe	RecDiff	1	2
PV_PCI0_PIN_P_P0_REFCLK_P	PCIe 100 MHz Input Clock	Clock PCIe	VIO	PCIe	RecDiff	1	2

1. This REFCLK can use spread spectrum.
2. This REFCLK cannot use spread spectrum.

5.2.6 I²C Signals

Table 5-8 lists the I²C signals.

Table 5-8. I²C Signals

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
PV_LP_P0_B_PIN_I2C_SCL_B	LightPath I²C Serial Clock	I2C	VSB0_3P30	OD	BiDi	1	1, 2
PV_LP_P0_B_PIN_I2C_SDA_B	LightPath I²C Serial Clock	I2C	VSB0_3P30	OD	BiDi	1	1, 2
PV_PCI_P0_B_PIN_I2C_SCL_B	Hotplug PCI I²C Serial Clock	I2C	VSB0_3P30	OD	BiDi	1	1, 2
PV_PCI_P0_B_PIN_I2C_SDA_B	Hotplug PCI I²C Serial Clock	I2C	VSB0_3P30	OD	BiDi	1	1, 2
PV_NV0A_P0_B_PIN_I2C_SCL_B	25G Link 0 I²C Serial Clock	I2C	VSB0_3P30	OD	BiDi	1	1, 2
PV_NV0A_P0_B_PIN_I2C_SDA_B	25G Link 0 I²C Serial Data	I2C	VSB0_3P30	OD	BiDi	1	1, 2
PV_NV0B_P0_B_PIN_I2C_SCL_B	25G Link 1 I²C Serial Clock	I2C	VSB0_3P30	OD	BiDi	1	1, 2
PV_NV0B_P0_B_PIN_I2C_SDA_B	25G Link 1 I²C Serial Data	I2C	VSB0_3P30	OD	BiDi	1	1, 2
PV_NV3A_P0_B_PIN_I2C_SCL_B	25G Link 3 I²C Serial Clock	I2C	VSB0_3P30	OD	BiDi	1	1, 2
PV_NV3A_P0_B_PIN_I2C_SDA_B	25G Link 3 I²C Serial Data	I2C	VSB0_3P30	OD	BiDi	1	1, 2

1. If the port is unused, tie off with a pull-down to GND through a 49.9 Ω resistor.
2. Signal is an I²C master.

5.2.7 X-Bus Signals

Table 5-9 lists the X-bus signals.

Table 5-9. X-Bus Signals

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
NX_X1_P0_P_PIN_CKA_CLK_N	X Bus 1 Clock A Output	X Bus	VIO	EDI	DrvDiff	1	
NX_X1_P0_P_PIN_CKA_CLK_P	X Bus 1 Clock A Output	X Bus	VIO	EDI	DrvDiff	1	
NX_X1_P0_P_PIN_CKA_DAT_[00:16]_N	X Bus 1 Clock Group A Data Output	X Bus	VIO	EDI	DrvDiff	17	
NX_X1_P0_P_PIN_CKA_DAT_[00:16]_P	X Bus 1 Clock Group A Data Output	X Bus	VIO	EDI	DrvDiff	17	
NX_X1_P0_P_PIN_CKB_CLK_N	X Bus 1 Clock B Output	X Bus	VIO	EDI	DrvDiff	1	
NX_X1_P0_P_PIN_CKB_CLK_P	X Bus 1 Clock B Output	X Bus	VIO	EDI	DrvDiff	1	
NX_X1_P0_P_PIN_CKB_DAT_[00:16]_N	X Bus 1 Clock Group B Data Output	X Bus	VIO	EDI	DrvDiff	17	
NX_X1_P0_P_PIN_CKB_DAT_[00:16]_P	X Bus 1 Clock Group B Data Output	X Bus	VIO	EDI	DrvDiff	17	
NX_X1_PIN_P_P0_CKA_CLK_N	X Bus 1 Clock A Input	X Bus	VIO	EDI	RecDiff	1	
NX_X1_PIN_P_P0_CKA_CLK_P	X Bus 1 Clock A Input	X Bus	VIO	EDI	RecDiff	1	
NX_X1_PIN_P_P0_CKA_DAT_[00:16]_N	X Bus 1 Clock Group A Data Input	X Bus	VIO	EDI	RecDiff	17	
NX_X1_PIN_P_P0_CKA_DAT_[00:16]_P	X Bus 1 Clock Group A Data Input	X Bus	VIO	EDI	RecDiff	17	
NX_X1_PIN_P_P0_CKB_CLK_N	X Bus 1 Clock B Input	X Bus	VIO	EDI	RecDiff	1	
NX_X1_PIN_P_P0_CKB_CLK_P	X Bus 1 Clock B Input	X Bus	VIO	EDI	RecDiff	1	
NX_X1_PIN_P_P0_CKB_DAT_[00:16]_N	X Bus 1 Clock Group B Data Input	X Bus	VIO	EDI	RecDiff	17	
NX_X1_PIN_P_P0_CKB_DAT_[00:16]_P	X Bus 1 Clock Group B Data Input	X Bus	VIO	EDI	RecDiff	17	
PV_X1TX_P0_P_PIN_TERMREF_N	X Bus 1 Terminal Reference Negative	X Bus	Analog	Analog	Analogin	1	1
PV_X1TX_P0_P_PIN_TERMREF_P	X Bus 1 Terminal Reference Positive	X Bus	Analog	Analog	Analogin	1	1
TS_X1RXA_P0_P_PIN_ATST	X Bus 1 Analog Test	X Bus	Analog	Analog		1	2
TS_X1RXA_P0_P_PIN_HFC_N	X Bus 1 High Frequency Characterization	X Bus	VIO			1	2
TS_X1RXA_P0_P_PIN_HFC_P	X Bus 1 High Frequency Characterization	X Bus	VIO			1	2

1. TERMREF value is 169 Ω, 0.1%. For the external resistor value, a 0.1% tolerance is preferred, but a 1% tolerance is acceptable.
2. These nets are unused (N/C).

5.2.8 PCIe Controller and Clock Signals

Table 5-10 lists the PCIe controller and clock bus signals.

Table 5-10. PCIe Controller and Clock Bus Signals (Sheet 1 of 2)

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
PE_E0_P0_P_PIN_DAT_[00:15]_N	PCIe Controller 0 Data Output	PCIe	VIO	PCIe	DrvDiff	16	1
PE_E0_P0_P_PIN_DAT_[00:15]_P	PCIe Controller 0 Data Output	PCIe	VIO	PCIe	DrvDiff	16	1
PE_E0_PIN_P_P0_DAT_[00:15]_N	PCIe Controller 0 Data Input	PCIe	VIO	PCIe	RecDiff	16	1
PE_E0_PIN_P_P0_DAT_[00:15]_P	PCIe Controller 0 Data Input	PCIe	VIO	PCIe	RecDiff	16	1
PE_E1_P0_P_PIN_DAT_[00:15]_N	PCIe Controller 1 Data Output	PCIe	VIO	PCIe	DrvDiff	16	
PE_E1_P0_P_PIN_DAT_[00:15]_P	PCIe Controller 1 Data Output	PCIe	VIO	PCIe	DrvDiff	16	
PE_E1_PIN_P_P0_DAT_[00:15]_N	PCIe Controller 1 Data Input	PCIe	VIO	PCIe	RecDiff	16	
PE_E1_PIN_P_P0_DAT_[00:15]_P	PCIe Controller 1 Data Input	PCIe	VIO	PCIe	RecDiff	16	
PE_E2_P0_P_PIN_DAT_[00:15]_N	PCIe Controller 2 Data Output	PCIe	VIO	PCIe	DrvDiff	16	
PE_E2_P0_P_PIN_DAT_[00:15]_P	PCIe Controller 2 Data Output	PCIe	VIO	PCIe	DrvDiff	16	
PE_E2_PIN_P_P0_DAT_[00:15]_N	PCIe Controller 2 Data Input	PCIe	VIO	PCIe	RecDiff	16	
PE_E2_PIN_P_P0_DAT_[00:15]_P	PCIe Controller 2 Data Input	PCIe	VIO	PCIe	RecDiff	16	
PV_E0_P0_P_PIN_PERST_B	PCIe Controller 0 Reset Output	PCIe	VSB0_3P30	OD	Drv	1	2
PV_E1A_P0_P_PIN_PERST_B	PCIe Controller 1A Reset Output	PCIe	VSB0_3P30	OD	Drv	1	2
PV_E1B_P0_P_PIN_PERST_B	PCIe Controller 1B Reset Output	PCIe	VSB0_3P30	OD	Drv	1	2
PV_E2A_P0_P_PIN_PERST_B	PCIe Controller 2A Reset Output	PCIe	VSB0_3P30	OD	Drv	1	2
PV_E2B_P0_P_PIN_PERST_B	PCIe Controller 2B Reset Output	PCIe	VSB0_3P30	OD	Drv	1	2
PV_E2C_P0_P_PIN_PERST_B	PCIe Controller 2C Reset Output	PCIe	VSB0_3P30	OD	Drv	1	2
PV_E0A_PIN_P_P0_PRSNT_B	PCIe Controller 0A Present Input	PCIe	VSB0_3P30	OD	Rec	1	2
PV_E0B_PIN_P_P0_PRSNT_B	PCIe Controller 0B Present Input	PCIe	VSB0_3P30	OD	Rec	1	2, 3
PV_E1A_PIN_P_P0_PRSNT_B	PCIe Controller 1A Present Input	PCIe	VSB0_3P30	OD	Rec	1	2
PV_E1B_PIN_P_P0_PRSNT_B	PCIe Controller 1B Present Input	PCIe	VSB0_3P30	OD	Rec	1	2
PV_E2A_PIN_P_P0_PRSNT_B	PCIe Controller 2A Present Input	PCIe	VSB0_3P30	OD	Rec	1	2
PV_E2B_PIN_P_P0_PRSNT_B	PCIe Controller 2B Present Input	PCIe	VSB0_3P30	OD	Rec	1	2
PV_E2C_PIN_P_P0_PRSNT_B	PCIe Controller 2C Present Input	PCIe	VSB0_3P30	OD	Rec	1	2
PV_E0_P0_P_PIN_SLOT_CLK_N	PCIe Controller 0 Clock Output	PCIe	VIO	PCIe	DrvDiff	1	2
PV_E0_P0_P_PIN_SLOT_CLK_P	PCIe Controller 0 Clock Output	PCIe	VIO	PCIe	DrvDiff	1	2
PV_E1A_P0_P_PIN_SLOT_CLK_N	PCIe Controller 1A Clock Output	PCIe	VIO	PCIe	DrvDiff	1	2
PV_E1A_P0_P_PIN_SLOT_CLK_P	PCIe Controller 1A Clock Output	PCIe	VIO	PCIe	DrvDiff	1	2

1. The E0 bus is not bifurcatable.
2. See *Section 3.3.4* on page 25 for additional information on CLOCK, PERST, and PRSNT connectivity.
3. This input is not used and cannot be N/C. Tie off with a 3.3 KΩ pull-up to 3.3 V_{AUX}.
4. TERMREF must have a 200 Ω, 0.1% resistor between the P and N legs.
5. ATST nets are unused, N/C.

Table 5-10. PCIe Controller and Clock Bus Signals (Sheet 2 of 2)

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
PV_E1B_P0_P_PIN_SLOT_CLK_N	PCIe Controller 1B Clock Output	PCIe	VIO	PCIe	DrvDiff	1	2
PV_E1B_P0_P_PIN_SLOT_CLK_P	PCIe Controller 1B Clock Output	PCIe	VIO	PCIe	DrvDiff	1	2
PV_E2A_P0_P_PIN_SLOT_CLK_N	PCIe Controller 2A Clock Output	PCIe	VIO	PCIe	DrvDiff	1	2
PV_E2A_P0_P_PIN_SLOT_CLK_P	PCIe Controller 2A Clock Output	PCIe	VIO	PCIe	DrvDiff	1	2
PV_E2B_P0_P_PIN_SLOT_CLK_N	PCIe Controller 2B Clock Output	PCIe	VIO	PCIe	DrvDiff	1	2
PV_E2B_P0_P_PIN_SLOT_CLK_P	PCIe Controller 2B Clock Output	PCIe	VIO	PCIe	DrvDiff	1	2
PV_E2C_P0_P_PIN_SLOT_CLK_N	PCIe Controller 2C Clock Output	PCIe	VIO	PCIe	DrvDiff	1	2
PV_E2C_P0_P_PIN_SLOT_CLK_P	PCIe Controller 2C Clock Output	PCIe	VIO	PCIe	DrvDiff	1	2
PV_E0_P0_P_PIN_TERMREF_N	PCIe Controller 0 Terminal Reference	PCIe	Analog			1	4
PV_E0_P0_P_PIN_TERMREF_P	PCIe Controller 0 Terminal Reference	PCIe	Analog			1	4
PV_E1_P0_P_PIN_TERMREF_N	PCIe Controller 1 Terminal Reference	PCIe	Analog			1	4
PV_E1_P0_P_PIN_TERMREF_P	PCIe Controller 1 Terminal Reference	PCIe	Analog			1	4
PV_E2_P0_P_PIN_TERMREF_N	PCIe Controller 2C Clock Output	PCIe	Analog			1	4
PV_E2_P0_P_PIN_TERMREF_P	PCIe Controller 2C Clock Output	PCIe	Analog			1	4
TS_E0_P0_P_PIN_ATST	PCIe Controller 0 Analog Test Output	PCIe	Analog				5
TS_E1_P0_P_PIN_ATST	PCIe Controller 0 Analog Test Output	PCIe	Analog				5
TS_E2_P0_P_PIN_ATST	PCIe Controller 0 Analog Test Output	PCIe	Analog				5

1. The E0 bus is not bifurcatable.
2. See *Section 3.3.4* on page 25 for additional information on CLOCK, PERST, and PRSNT connectivity.
3. This input is not used and cannot be N/C. Tie off with a 3.3 KΩ pull-up to 3.3 V_{AUX}.
4. TERMREF must have a 200 Ω, 0.1% resistor between the P and N legs.
5. ATST nets are unused, N/C.

5.2.9 LPC Bus Signals

Table 5-11 lists the LPC bus signals.

Table 5-11. LPC Bus Signals

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
PV_PRV_P0_B_PIN_LPC_DAT_[0:3]	LPC Data 0 - 3	LPC	VSB0_3P30		BiDi	4	1
PV_PRV_P0_P_PIN_LPC_FRAME_B	LPC Frame Output	LPC	VSB0_3P30		Drv	1	2
PV_PRV_P0_P_PIN_LPC_RESET_B	LPC Reset Output	LPC	VSB0_3P30		BiDi	1	3
PV_PRV_PIN_P_P0_LPC_CLK	LPC 33 MHz Clock Input	LPC	VIO	CMOS	Rec	1	4
PV_PRV_PIN_P_P0_LPC_IRQ	LPC Interrupt BiDi	LPC	VSB0_3P30		Rec	1	5

1. For the first processor of a two-socket system, connect to the BMC through a 22 Ω series resistor placed at the CPU and a 33 Ω series resistor placed at the BMC. N/C for the second processor.
2. For the first processor of a two-socket system, connect to the BMC through a 22 Ω series resistor placed at the CPU. N/C for the second processor.
3. The first processor requires a 3.3 KΩ pull-up resistor to 3.3 V_{AUX}. IBM suggests a 10 nF cap to GND for noise. For the second processor of a two-socket system, tie off with a 49.9 Ω pull-up resistor to 3.3 V_{AUX}.
4. V_{MAX} is 1.26 V for this pin; a voltage divider might be required depending on the clock driver used. For the second processor of a two-socket system, tie off with 49.9 Ω pull-down resistor to GND.
5. For the first processor of a two-socket system, connect to the BMC through a 22 Ω series resistor placed at the processor and a 33 Ω series resistor placed at the BMC. For the second processor, tie off with a 49.9 Ω pull-up resistor to 3.3 V_{AUX}.

5.2.10 Memory Signals

Table 5-12 lists the memory signals.

Table 5-12. Memory Signals (Sheet 1 of 8)

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
DM_DDR0_BI_DQ_[0:71]	DDR Port0 Data Query	Memory	VDDR01			72	
DM_DDR0_BI_DQS_[00:17]_N	DDR Port0 Data Query Strobe	Memory	VDDR01			18	
DM_DDR0_BI_DQS_[00:17]_P	DDR Port0 Data Query Strobe	Memory	VDDR01			18	
DM_DDR0_P0_P_PIN_ACT_B	DDR Port 0 Address and Command	Memory	VDDR01			1	
DM_DDR0_P0_P_PIN_ADDR_[00:17]	DDR Port 0 Address and Command	Memory	VDDR01			18	
DM_DDR0_P0_P_PIN_BANK_ADR_[0:1]	DDR Port 0 Address and Command	Memory	VDDR01			2	

1. CKE[2:3] are N/C for single drop DIMMs.
2. This signal is N/C for single-drop DIMMs.
3. CS_B_[2:3] are N/C for single-drop DIMMs.
4. ODT_[2:3] are N/C for single-drop DIMMs.
5. Requires a 1 KΩ pull-down to GND. IBM also recommends a 1nF capacitor to GND for noise reduction.
6. Requires a 1 KΩ pull-up to V_{DDR}.
7. Each TERMREF requires a 240 Ω, 0.1% resistor connected between the P and N legs.
8. This signal is N/C; unused in the system.
9. All memory I^2C nets require a 1 KΩ pull-up to 2.5 V_{AUX}.

Table 5-12. Memory Signals (Sheet 2 of 8)

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
DM_DDR0_P0_P_PIN_BANK_GRP_[0:1]	DDR Port 0 Address and Command	Memory	VDDR01			2	
DM_DDR0_P0_P_PIN_CHIPID_[0:2]	DDR Port 0 Address and Command	Memory	VDDR01			3	
DM_DDR0_P0_P_PIN_CKE_[0:3]	DDR Port0 Control	Memory	VDDR01			4	1
DM_DDR0_P0_P_PIN_CLK_0_N	DDR Port 0 DIMM Clock	Memory	VDDR01			1	
DM_DDR0_P0_P_PIN_CLK_0_P	DDR Port 0 DIMM Clock	Memory	VDDR01			1	
DM_DDR0_P0_P_PIN_CLK_1_N	DDR Port 0 DIMM Clock	Memory	VDDR01			1	2
DM_DDR0_P0_P_PIN_CLK_1_P	DDR Port 0 DIMM Clock	Memory	VDDR01			1	2
DM_DDR0_P0_P_PIN_CS_B_[0:3]	DDR Port 0 Control	Memory	VDDR01			4	3
DM_DDR0_P0_P_PIN_ODT_[0:3]	DDR Port 0 Control	Memory	VDDR01			4	4
DM_DDR0_P0_P_PIN_PAR	DDR Port 0 Address and Command	Memory	VDDR01			1	
DM_DDR0_P0_P_PIN_RESET_B	DDR Port 0 Address and Command	Memory	VDDR01			1	5
DM_DDR0_PIN_P_P0_ERR_B	DDR Port 0 Address and Command	Memory	VDDR01			1	6
DM_DDR0_PIN_P_P0_EVENT_B	DDR Port 0 Address and Command	Memory	VDDR01			1	6
DM_DDR1_BI_DQ_[00:71]	DDR Port1 Data Query Signal	Memory	VDDR01			72	
DM_DDR1_BI_DQS_[00:17]_N	DDR Port1 Data Query Strobe	Memory	VDDR01			18	
DM_DDR1_BI_DQS_[00:17]_P	DDR Port1 Data Query Strobe	Memory	VDDR01			18	
DM_DDR1_P0_P_PIN_ACT_B	DDR Port1 Address and Command	Memory	VDDR01			1	
DM_DDR1_P0_P_PIN_ADDR_[00:17]	DDR Port1 Address and Command	Memory	VDDR01			18	
DM_DDR1_P0_P_PIN_BANK_ADR_[0:1]	DDR Port1 Address and Command	Memory	VDDR01			2	
DM_DDR1_P0_P_PIN_BANK_GRP_[0:1]	DDR Port1 Address and Command	Memory	VDDR01			2	
DM_DDR1_P0_P_PIN_CHIPID_[0:2]	DDR Port1 Address and Command	Memory	VDDR01			3	

1. CKE[2:3] are N/C for single drop DIMMs.
2. This signal is N/C for single-drop DIMMs.
3. CS_B_[2:3] are N/C for single-drop DIMMs.
4. ODT_[2:3] are N/C for single-drop DIMMs.
5. Requires a 1 KΩ pull-down to GND. IBM also recommends a 1nF capacitor to GND for noise reduction.
6. Requires a 1 KΩ pull-up to V_{DDR}.
7. Each TERMREF requires a 240 Ω, 0.1% resistor connected between the P and N legs.
8. This signal is N/C; unused in the system.
9. All memory I^2C nets require a 1 KΩ pull-up to 2.5 V_{AUX}.

Table 5-12. Memory Signals (Sheet 3 of 8)

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
DM_DDR1_P0_P_PIN_CKE_[0:3]	DDR Port1 Control	Memory	VDDR01			4	1
DM_DDR1_P0_P_PIN_CLK_0_N	DDR Port1 DIMM Clock	Memory	VDDR01			1	
DM_DDR1_P0_P_PIN_CLK_0_P	DDR Port1 DIMM Clock	Memory	VDDR01			1	
DM_DDR1_P0_P_PIN_CLK_1_N	DDR Port1 DIMM Clock	Memory	VDDR01			1	2
DM_DDR1_P0_P_PIN_CLK_1_P	DDR Port1 DIMM Clock	Memory	VDDR01			1	2
DM_DDR1_P0_P_PIN_CS_B_[0:3]	DDR Port1 Control	Memory	VDDR01			4	3
DM_DDR1_P0_P_PIN_ODT_[0:3]	DDR Port1 Control	Memory	VDDR01			4	4
DM_DDR1_P0_P_PIN_PAR	DDR Port1 Address and Command	Memory	VDDR01			1	
DM_DDR1_P0_P_PIN_RESET_B	DDR Port1 Address and Command	Memory	VDDR01			1	5
DM_DDR1_PIN_P_P0_ERR_B	DDR Port1 Address and Command	Memory	VDDR01			1	6
DM_DDR1_PIN_P_P0_EVENT_B	DDR Port1 Address and Command	Memory	VDDR01			1	6
DM_DDR2_BI_DQ_[00:71]	DDR Port2 Data Query Signal	Memory	VDDR03			72	
DM_DDR2_BI_DQS_[00:17]_N	DDR Port2 Data Query Strobe	Memory	VDDR03			18	
DM_DDR2_BI_DQS_[00:17]_P	DDR Port2 Data Query Strobe	Memory	VDDR03			18	
DM_DDR2_P0_P_PIN_ACT_B	DDR Port2 Address and Command	Memory	VDDR03			1	
DM_DDR2_P0_P_PIN_ADDR_[00:17]	DDR Port2 Address and Command	Memory	VDDR03			18	
DM_DDR2_P0_P_PIN_BANK_ADR_[0:1]	DDR Port2 Address and Command	Memory	VDDR03			2	
DM_DDR2_P0_P_PIN_BANK_GRP_[0:1]	DDR Port2 Address and Command	Memory	VDDR03			2	
DM_DDR2_P0_P_PIN_CHIPID_[0:2]	DDR Port2 Address and Command	Memory	VDDR03			3	
DM_DDR2_P0_P_PIN_CKE_[0:3]	DDR Port2 Control	Memory	VDDR03			4	1
DM_DDR2_P0_P_PIN_CLK_0_N	DDR Port2 DIMM Clock	Memory	VDDR03			1	
DM_DDR2_P0_P_PIN_CLK_0_P	DDR Port2 DIMM Clock	Memory	VDDR03			1	
DM_DDR2_P0_P_PIN_CLK_1_N	DDR Port2 DIMM Clock	Memory	VDDR03			1	2
DM_DDR2_P0_P_PIN_CLK_1_P	DDR Port2 DIMM Clock	Memory	VDDR03			1	2

1. CKE[2:3] are N/C for single drop DIMMs.
2. This signal is N/C for single-drop DIMMs.
3. CS_B_[2:3] are N/C for single-drop DIMMs.
4. ODT_[2:3] are N/C for single-drop DIMMs.
5. Requires a 1 KΩ pull-down to GND. IBM also recommends a 1nF capacitor to GND for noise reduction.
6. Requires a 1 KΩ pull-up to V_{DDR}.
7. Each TERMREF requires a 240 Ω, 0.1% resistor connected between the P and N legs.
8. This signal is N/C; unused in the system.
9. All memory I^2C nets require a 1 KΩ pull-up to 2.5 V_{AUX}.

Table 5-12. Memory Signals (Sheet 4 of 8)

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
DM_DDR2_P0_P_PIN_CS_B_[0:3]	DDR Port2 Control	Memory	VDDR03			4	3
DM_DDR2_P0_P_PIN_ODT_[0:3]	DDR Port2 Control	Memory	VDDR03			4	4
DM_DDR2_P0_P_PIN_PAR	DDR Port2 Address and Command	Memory	VDDR03			1	
DM_DDR2_P0_P_PIN_RESET_B	DDR Port2 Address and Command	Memory	VDDR03			1	5
DM_DDR2_PIN_P_P0_ERR_B	DDR Port2 Address and Command	Memory	VDDR03			1	6
DM_DDR2_PIN_P_P0_EVENT_B	DDR Port2 Address and Command	Memory	VDDR03			1	6
DM_DDR3_BI_DQ_[00:71]	DDR Port3 Data Query Signal	Memory	VDDR03			72	
DM_DDR3_BI_DQS_[00:17]_N	DDR Port3 Data Query Strobe	Memory	VDDR03			18	
DM_DDR3_BI_DQS_[00:17]_P	DDR Port3 Data Query Strobe	Memory	VDDR03			18	
DM_DDR3_P0_P_PIN_ACT_B	DDR Port3 Address and Command	Memory	VDDR03			1	
DM_DDR3_P0_P_PIN_ADDR_[00:17]	DDR Port3 Address and Command	Memory	VDDR03			18	
DM_DDR3_P0_P_PIN_BANK_ADR_[0:1]	DDR Port3 Address and Command	Memory	VDDR03			2	
DM_DDR3_P0_P_PIN_BANK_GRP_[0:1]	DDR Port3 Address and Command	Memory	VDDR03			2	
DM_DDR3_P0_P_PIN_CHIPID_[0:2]	DDR Port3 Address and Command	Memory	VDDR03			3	
DM_DDR3_P0_P_PIN_CKE_[0:3]	DDR Port3 Control	Memory	VDDR03			4	1
DM_DDR3_P0_P_PIN_CLK_0_N	DDR Port3 DIMM Clock	Memory	VDDR03			1	
DM_DDR3_P0_P_PIN_CLK_0_P	DDR Port3 DIMM Clock	Memory	VDDR03			1	
DM_DDR3_P0_P_PIN_CLK_1_N	DDR Port3 DIMM Clock	Memory	VDDR03			1	2
DM_DDR3_P0_P_PIN_CLK_1_P	DDR Port3 DIMM Clock	Memory	VDDR03			1	2
DM_DDR3_P0_P_PIN_CS_B_[0:3]	DDR Port3 Control	Memory	VDDR03			4	3
DM_DDR3_P0_P_PIN_ODT_[0:3]	DDR Port3 Control	Memory	VDDR03			4	4
DM_DDR3_P0_P_PIN_PAR	DDR Port3 Address and Command	Memory	VDDR03			1	
DM_DDR3_P0_P_PIN_RESET_B	DDR Port3 Address and Command	Memory	VDDR03			1	5

1. CKE[2:3] are N/C for single drop DIMMs.
2. This signal is N/C for single-drop DIMMs.
3. CS_B_[2:3] are N/C for single-drop DIMMs.
4. ODT_[2:3] are N/C for single-drop DIMMs.
5. Requires a 1 KΩ pull-down to GND. IBM also recommends a 1nF capacitor to GND for noise reduction.
6. Requires a 1 KΩ pull-up to V_{DDR}.
7. Each TERMREF requires a 240 Ω, 0.1% resistor connected between the P and N legs.
8. This signal is N/C; unused in the system.
9. All memory I^2C nets require a 1 KΩ pull-up to 2.5 V_{AUX}.

Table 5-12. Memory Signals (Sheet 5 of 8)

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
DM_DDR3_PIN_P_P0_ERR_B	DDR Port3 Address and Command	Memory	VDDR03			1	6
DM_DDR3_PIN_P_P0_EVENT_B	DDR Port3 Address and Command	Memory	VDDR03			1	6
DM_DDR4_BI_DQ_[00:71]	DDR Port4 Data Query Signal	Memory	VDDR47			72	
DM_DDR4_BI_DQS_[00:17]_N	DDR Port4 Data Query Strobe	Memory	VDDR47			18	
DM_DDR4_BI_DQS_[00:17]_P	DDR Port4 Data Query Strobe	Memory	VDDR47			18	
DM_DDR4_P0_P_PIN_ACT_B	DDR Port4 Address and Command	Memory	VDDR47			1	
DM_DDR4_P0_P_PIN_ADDR_[00:17]	DDR Port4 Address and Command	Memory	VDDR47			18	
DM_DDR4_P0_P_PIN_BANK_ADR_[0:1]	DDR Port4 Address and Command	Memory	VDDR47			2	
DM_DDR4_P0_P_PIN_BANK_GRP_[0:1]	DDR Port4 Address and Command	Memory	VDDR47			2	
DM_DDR4_P0_P_PIN_CHIPID_[0:2]	DDR Port4 Address and Command	Memory	VDDR47			3	
DM_DDR4_P0_P_PIN_CKE_[0:3]	DDR Port4 Control	Memory	VDDR47			4	1
DM_DDR4_P0_P_PIN_CLK_0_N	DDR Port4 DIMM Clock	Memory	VDDR47			1	
DM_DDR4_P0_P_PIN_CLK_0_P	DDR Port4 DIMM Clock	Memory	VDDR47			1	
DM_DDR4_P0_P_PIN_CLK_1_N	DDR Port4 DIMM Clock	Memory	VDDR47			1	2
DM_DDR4_P0_P_PIN_CLK_1_P	DDR Port4 DIMM Clock	Memory	VDDR47			1	2
DM_DDR4_P0_P_PIN_CS_B_[0:3]	DDR Port4 Control	Memory	VDDR47			4	3
DM_DDR4_P0_P_PIN_ODT_[0:3]	DDR Port4 Control	Memory	VDDR47			4	4
DM_DDR4_P0_P_PIN_PAR	DDR Port4 Address and Command	Memory	VDDR47			1	
DM_DDR4_P0_P_PIN_RESET_B	DDR Port4 Address and Command	Memory	VDDR47			1	5
DM_DDR4_PIN_P_P0_ERR_B	DDR Port4 Address and Command	Memory	VDDR47			1	6
DM_DDR4_PIN_P_P0_EVENT_B	DDR Port4 Address and Command	Memory	VDDR47			1	6
DM_DDR5_BI_DQ_[00:71]	DDR Port5 Data Query Signal	Memory	VDDR47			72	
DM_DDR5_BI_DQS_[00:17]_N	DDR Port5 Data Query Strobe	Memory	VDDR47			18	

1. CKE[2:3] are N/C for single drop DIMMs.
2. This signal is N/C for single-drop DIMMs.
3. CS_B_[2:3] are N/C for single-drop DIMMs.
4. ODT_[2:3] are N/C for single-drop DIMMs.
5. Requires a 1 KΩ pull-down to GND. IBM also recommends a 1nF capacitor to GND for noise reduction.
6. Requires a 1 KΩ pull-up to V_{DDR}.
7. Each TERMREF requires a 240 Ω, 0.1% resistor connected between the P and N legs.
8. This signal is N/C; unused in the system.
9. All memory I^2C nets require a 1 KΩ pull-up to 2.5 V_{AUX}.

Table 5-12. Memory Signals (Sheet 6 of 8)

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
DM_DDR5_BI_DQS_[00:17]_P	DDR Port5 Data Query Strobe	Memory	VDDR47			18	
DM_DDR5_P0_P_PIN_ACT_B	DDR Port5 Address and Command	Memory	VDDR47			1	
DM_DDR5_P0_P_PIN_ADDR_[00:17]	DDR Port5 Address and Command	Memory	VDDR47			18	
DM_DDR5_P0_P_PIN_BANK_ADR_[0:1]	DDR Port5 Address and Command	Memory	VDDR47			2	
DM_DDR5_P0_P_PIN_BANK_GRP_[0:1]	DDR Port5 Address and Command	Memory	VDDR47			2	
DM_DDR5_P0_P_PIN_CHIPID_[0:2]	DDR Port5 Address and Command	Memory	VDDR47			3	
DM_DDR5_P0_P_PIN_CKE_[0:3]	DDR Port5 Control	Memory	VDDR47			4	1
DM_DDR5_P0_P_PIN_CLK_0_N	DDR Port5 DIMM Clock	Memory	VDDR47			1	
DM_DDR5_P0_P_PIN_CLK_0_P	DDR Port5 DIMM Clock	Memory	VDDR47			1	
DM_DDR5_P0_P_PIN_CLK_1_N	DDR Port5 DIMM Clock	Memory	VDDR47			1	2
DM_DDR5_P0_P_PIN_CLK_1_P	DDR Port5 DIMM Clock	Memory	VDDR47			1	2
DM_DDR5_P0_P_PIN_CS_B_[0:3]	DDR Port5 Control	Memory	VDDR47			4	3
DM_DDR5_P0_P_PIN_ODT_[0:3]	DDR Port5 Control	Memory	VDDR47			4	4
DM_DDR5_P0_P_PIN_PAR	DDR Port5 Address and Command	Memory	VDDR47			1	
DM_DDR5_P0_P_PIN_RESET_B	DDR Port5 Address and Command	Memory	VDDR47			1	5
DM_DDR5_PIN_P_P0_ERR_B	DDR Port5 Address and Command	Memory	VDDR47			1	6
DM_DDR5_PIN_P_P0_EVENT_B	DDR Port5 Address and Command	Memory	VDDR47			1	6
DM_DDR6_BI_DQ_[00:71]	DDR Port6 Data Query Signal	Memory	VDDR67			72	
DM_DDR6_BI_DQS_[00:17]_N	DDR Port6 Data Query Strobe	Memory	VDDR67			18	
DM_DDR6_BI_DQS_[00:17]_P	DDR Port6 Data Query Strobe	Memory	VDDR67			18	
DM_DDR6_P0_P_PIN_ACT_B	DDR Port6 Address and Command	Memory	VDDR67			1	
DM_DDR6_P0_P_PIN_ADDR_[00:17]	DDR Port6 Address and Command	Memory	VDDR67			18	

1. CKE[2:3] are N/C for single drop DIMMs.
2. This signal is N/C for single-drop DIMMs.
3. CS_B_[2:3] are N/C for single-drop DIMMs.
4. ODT_[2:3] are N/C for single-drop DIMMs.
5. Requires a 1 KΩ pull-down to GND. IBM also recommends a 1nF capacitor to GND for noise reduction.
6. Requires a 1 KΩ pull-up to V_{DDR}.
7. Each TERMREF requires a 240 Ω, 0.1% resistor connected between the P and N legs.
8. This signal is N/C; unused in the system.
9. All memory I^2C nets require a 1 KΩ pull-up to 2.5 V_{AUX}.

Table 5-12. Memory Signals (Sheet 7 of 8)

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
DM_DDR6_P0_P_PIN_BANK_ADR_[0:1]	DDR Port6 Address and Command	Memory	VDDR67			2	
DM_DDR6_P0_P_PIN_BANK_GRP_[0:1]	DDR Port6 Address and Command	Memory	VDDR67			2	
DM_DDR6_P0_P_PIN_CHIPID_[0:2]	DDR Port6 Address and Command	Memory	VDDR67			3	
DM_DDR6_P0_P_PIN_CKE_[0:3]	DDR Port6 Control	Memory	VDDR67			4	1
DM_DDR6_P0_P_PIN_CLK_0_N	DDR Port6 DIMM Clock	Memory	VDDR67			1	
DM_DDR6_P0_P_PIN_CLK_0_P	DDR Port6 DIMM Clock	Memory	VDDR67			1	
DM_DDR6_P0_P_PIN_CLK_1_N	DDR Port6 DIMM Clock	Memory	VDDR67			1	2
DM_DDR6_P0_P_PIN_CLK_1_P	DDR Port6 DIMM Clock	Memory	VDDR67			1	2
DM_DDR6_P0_P_PIN_CS_B_[0:3]	DDR Port6 Control	Memory	VDDR67			4	3
DM_DDR6_P0_P_PIN_ODT_[0:3]	DDR Port6 Control	Memory	VDDR67			4	4
DM_DDR6_P0_P_PIN_PAR	DDR Port6 Address and Command	Memory	VDDR67			1	
DM_DDR6_P0_P_PIN_RESET_B	DDR Port6 Address and Command	Memory	VDDR67			1	5
DM_DDR6_PIN_P_P0_ERR_B	DDR Port6 Address and Command	Memory	VDDR67			1	6
DM_DDR6_PIN_P_P0_EVENT_B	DDR Port6 Address and Command	Memory	VDDR67			1	6
DM_DDR7_BI_DQ_[00:71]	DDR Port7 Data Query Signal	Memory	VDDR67			72	
DM_DDR7_BI_DQS_[00:17]_N	DDR Port7 Data Query Strobe	Memory	VDDR67			18	
DM_DDR7_BI_DQS_[00:17]_P	DDR Port7 Data Query Strobe	Memory	VDDR67			18	
DM_DDR7_P0_P_PIN_ACT_B	DDR Port7 Address and Command	Memory	VDDR67			1	
DM_DDR7_P0_P_PIN_ADDR_[00:17]	DDR Port7 Address and Command	Memory	VDDR67			18	
DM_DDR7_P0_P_PIN_BANK_ADR_[0:1]	DDR Port7 Address and Command	Memory	VDDR67			2	
DM_DDR7_P0_P_PIN_BANK_GRP_[0:1]	DDR Port7 Address and Command	Memory	VDDR67			2	
DM_DDR7_P0_P_PIN_CHIPID_[0:2]	DDR Port7 Address and Command	Memory	VDDR67			3	

1. CKE[2:3] are N/C for single drop DIMMs.
2. This signal is N/C for single-drop DIMMs.
3. CS_B_[2:3] are N/C for single-drop DIMMs.
4. ODT_[2:3] are N/C for single-drop DIMMs.
5. Requires a 1 KΩ pull-down to GND. IBM also recommends a 1nF capacitor to GND for noise reduction.
6. Requires a 1 KΩ pull-up to V_{DDR}.
7. Each TERMREF requires a 240 Ω, 0.1% resistor connected between the P and N legs.
8. This signal is N/C; unused in the system.
9. All memory I^2C nets require a 1 KΩ pull-up to 2.5 V_{AUX}.

Table 5-12. Memory Signals (Sheet 8 of 8)

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
DM_DDR7_P0_P_PIN_CKE_[0:3]	DDR Port7 Control	Memory	VDDR67			4	1
DM_DDR7_P0_P_PIN_CLK_0_N	DDR Port7 DIMM Clock	Memory	VDDR67			1	
DM_DDR7_P0_P_PIN_CLK_0_P	DDR Port7 DIMM Clock	Memory	VDDR67			1	
DM_DDR7_P0_P_PIN_CLK_1_N	DDR Port7 DIMM Clock	Memory	VDDR67			1	2
DM_DDR7_P0_P_PIN_CLK_1_P	DDR Port7 DIMM Clock	Memory	VDDR67			1	2
DM_DDR7_P0_P_PIN_CS_B_[0:3]	DDR Port7 Control	Memory	VDDR67			4	3
DM_DDR7_P0_P_PIN_ODT_[0:3]	DDR Port7 Control	Memory	VDDR67			4	4
DM_DDR7_P0_P_PIN_PAR	DDR Port7 Address and Command	Memory	VDDR67			1	
DM_DDR7_P0_P_PIN_RESET_B	DDR Port7 Address and Command	Memory	VDDR67			1	5
DM_DDR7_PIN_P_P0_ERR_B	DDR Port7 Address and Command	Memory	VDDR67			1	6
DM_DDR7_PIN_P_P0_EVENT_B	DDR Port7 Address and Command	Memory	VDDR67			1	6
PV_DDR0123_P0_P_PIN_TERMREF_N	DDR0123 Terminal Reference Negative	Memory	Analog			1	7
PV_DDR0123_P0_P_PIN_TERMREF_P	DDR0123 Terminal Reference Positive	Memory	Analog			1	7
PV_DDR4567_P0_P_PIN_TERMREF_N	DDR4567 Terminal Reference Negative	Memory	Analog			1	7
PV_DDR4567_P0_P_PIN_TERMREF_P	DDR4567 Terminal Reference Positive	Memory	Analog			1	7
TS_DDR0123_P0_P_PIN_ATST	DDR0123 Analog Test Output	Memory	Analog			1	8
TS_DDR4567_P0_P_PIN_ATST	DDR4567 Analog Test Output	Memory	Analog			1	8
PV_DDR0123_P0_B_PIN_I2C_SCL_B	DDR0123 I^2C Serial Clock	Memory	VSB0_3P30	OD	BiDi	1	9
PV_DDR0123_P0_B_PIN_I2C_SDA_B	DDR0123 I^2C Serial Data	Memory	VSB0_3P30	OD	BiDi	1	9
PV_DDR4567_P0_B_PIN_I2C_SCL_B	DDR4567 I^2C Serial Clock	Memory	VSB0_3P30	OD	BiDi	1	9
PV_DDR4567_P0_B_PIN_I2C_SDA_B	DDR4567 I^2C Serial Data	Memory	VSB0_3P30	OD	BiDi	1	9

1. CKE[2:3] are N/C for single drop DIMMs.
2. This signal is N/C for single-drop DIMMs.
3. CS_B_[2:3] are N/C for single-drop DIMMs.
4. ODT_[2:3] are N/C for single-drop DIMMs.
5. Requires a 1 KΩ pull-down to GND. IBM also recommends a 1nF capacitor to GND for noise reduction.
6. Requires a 1 KΩ pull-up to V_{DDR}.
7. Each TERMREF requires a 240 Ω, 0.1% resistor connected between the P and N legs.
8. This signal is N/C; unused in the system.
9. All memory I^2C nets require a 1 KΩ pull-up to 2.5 V_{AUX}.

5.2.11 JTAG Signals

Table 5-13 lists the JTAG signals.

Table 5-13. JTAG Signals

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
PV_PRV_P0_P_PIN_ATTENTION_B	OCC Attention Output	JTAG	VSB0_3P30	CMOS	Drv	1	1
TS_JTAG_P0_P_PIN_TDO	Test Data Out	JTAG	VIO	CMOS	Drv	1	2
TS_JTAG_PIN_P_P0_TDI	Test Data In	JTAG	VIO	CMOS	Rec	1	2
TS_JTAG_PIN_P_P0_TMS	Test Mode Select	JTAG	VIO	CMOS	Rec	1	2
TS_JTAG_PIN_P_P0_CARD_TEST	Card Test	JTAG	VSB_1P10	CMOS	Rec	1	3
TS_JTAG_PIN_P_P0_TCK	Test Clock	JTAG	VIO	OD	Rec	1	4

1. For a single-socket system or the first processor of a two-socket system, connect to the BMC with a 4.7 KΩ pull-up to 3.3 V_{AUX} and a 10 nF capacitor to GND at the BMC. For the second processor, this signal is unused, N/C.
2. Signal requires a 2 KΩ pull-up to V_{IO} whether the bus is used or unused.
3. Tie off with a 49.9 Ω pull-down to GND.
4. If the bus is used, the signal requires a 2 KΩ pull-down to GND. If the bus is unused, tie off with a 49.9 Ω pull-down to GND.

5.2.12 Miscellaneous Signals

Table 5-14 lists the miscellaneous signals.

Table 5-14. Miscellaneous Signals (Sheet 1 of 2)

Signal	Description	Interface	I/O Voltage Domain	Family	Pin Count	Type	Notes
SCM_PRESENT_B	SCM Socket Present Signal	Misc			1		1
PV_IVRM_V1_M_P0_VREF_N	iVRM External Voltage Reference	Misc	Analog		1		2
PV_IVRM_V1_M_P0_VREF_P	iVRM External Voltage Reference	Misc	Analog		1		2
PV_PRV_P0_B_PIN_GPIO0	GPIO0	Misc	VSB0_3P30		1	BiDi	3
PV_PRV_P0_B_PIN_GPIO1	GPIO1	Misc	VSB0_3P30		1	BiDi	3, 4
PV_PRV_P0_B_PIN_GPIO2	GPIO2	Misc	VSB0_3P30		1	BiDi	3
PV_PRV_P0_B_PIN_SPARE0	Spare 0	Misc	VSB_1P10	CMOS	1	BiDi	5
PV_PRV_P0_B_PIN_SPARE2	Spare 2	Misc	VSB_1P10	CMOS	BiDi	1	6
PV_PRV_PIN_P_P0_CHIP_MASTER	Chip Master Input	Misc	VSB_1P10	CMOS	1	Rec	7
PV_PRV_PIN_P_P0_STBY_RESET_B	Standby Reset Input	Misc	VSB_1P10	CMOS	1	Rec	8
PV_PRV_PIN_P_P0_VDN_PGOOD	Nest Voltage Power Good Input	Misc	VSB_1P10	CMOS	1	Rec	9
PV_SEEPROM0_P0_B_PIN_I2C_SDA_B	SEEPROM 0 I2C Serial Data	Misc	VSB0_3P30	OD	1	BiDi	10
PV_SEEPROM0_P0_P_PIN_I2C_SCL_B	SEEPROM 0 I2C Serial Clock	Misc	VSB0_3P30	OD	1	BiDi	10
PV_SEEPROM1_P0_B_PIN_I2C_SDA_B	SEEPROM 1 I2C Serial Data	Misc	VSB0_3P30	OD	1	BiDi	10

1. For the Master processor, tie to GND. For additional processors: tie to GND if the processor will always be there or to the BMC for presence detection.
2. Do not connect to anything (N/C).
3. If used, pull up to 3.3 V_{AUX} with a 3.3 KΩ resistor. If not used, tie to GND with a 49.9 Ω resistor.
4. IBM suggests using GPIO1 for GPU power braking.
5. Unused. Tie off with a nopopped 49.9 Ω pull-up to 1.1 V_{AUX} and a populated 49.9 Ω pull-down to GND.
6. Unused. Tie off with a nopopped 3.3 KΩ pull-up to 3.3 V_{AUX} and a populated 49.9 Ω pull-down to GND.
7. For a single-socket system or the first processor of a two-socket system, tie to GND through a 49.9 Ω resistor (this indicates the Master processor). For the second processor, tie to 1.1 V_{AUX} through a 49.9 Ω resistor (this indicates the Slave processor).
8. This signal has a 1 KΩ internal pull-up resistor; add a nopopped 10 KΩ pull-up resistor to 1.1 V_{AUX} on board. IBM recommends a 1 nF - 10 nF capacitor to GND for noise dampening.
9. Requires a 1.2 KΩ pull-up to 1.1 V_{AUX} or must always be actively driven (like an AUC17 gate). IBM recommends a 1 nF capacitor to GND for noise dampening.
10. This signal has an internal pull-up; N/C on the planar.
11. Tie off with a pull down to GND through a 49.9 Ω resistor.
12. Digital thermal sensor analog test output. This pin is used for debug only; leave as N/C on the system board.
13. Throttle signal, active low. This pin can be asserted through hardware in the case of an emergency power down to tell the OCC to go to the power state defined for N mode. Validate the throttle pin use case with your IBM AE. Created from power supply PGOOD signals. Connect using a 1 KΩ series resistor at the processor; also connect to the BMC. No pull-up is required if this signal is always actively driven. Otherwise, pull up with a resistor between 1 - 5 KΩ to 3.3 V_{AUX}. If not using this signal, tie off with a resistor between 1 - 4.7 KΩ to 3.3 V_{AUX}.
14. The first processor requires a 1 KΩ pull-up resistor to V_{IO}; combine with system reset and wire to reset the TPM device. For additional processors or an unused TPM, tie off with a 2 KΩ pull-up to V_{IO}.
15. The first processor requires a pull-up resistor ≤1 KΩ to V_{IO}; wire to the TPM interrupt logic. Note that the actual value of the pull-up might be system-application dependent. For additional processors or an unused TPM, tie off with a 1 KΩ pull-down to GND.

Table 5-14. Miscellaneous Signals (Sheet 2 of 2)

Signal	Description	Interface	I/O Voltage Domain	Family	Pin Count	Type	Notes
PV_SEEPROM1_P0_P_PIN_I2C_SCL_B	SEEPROM 1 I2C Serial Clock	Misc	VSB0_3P30	OD	1	BiDi	10
PV_SEEPROM2_P0_B_PIN_I2C_SDA_B	SEEPROM 2 I2C Serial Data	Misc	VSB0_3P30	OD	BiDi	1	10
PV_SEEPROM2_P0_P_PIN_I2C_SCL_B	SEEPROM 2 I2C Serial Clock	Misc	VSB0_3P30	OD	BiDi	1	10
PV_SEEPROM3_P0_B_PIN_I2C_SDA_B	SEEPROM 3 I2C Serial Data	Misc	VSB0_3P30	OD	1	BiDi	10
PV_SEEPROM3_P0_P_PIN_I2C_SCL_B	SEEPROM 3 I2C Serial Clock	Misc	VSB0_3P30	OD	1	BiDi	10
TS_DTSNPU_P0_P_PIN_TEST_OUT	Digital Thermal Sensor Analog Output	Misc	VDN	Analog	1		12
TS_EFUSE_PIN_P_P0_FSOURCE	Module Test Efuse Source	Misc	Analog	Analog	1	Rec	11
TS_NESTLCPLL_P0_P_PIN_ATST	Nest LC Analog Test	Misc	Analog		1		2
TS_NESTLCPLL_P0_P_PIN_HFC_N	Nest LC PLL High Frequency Characterization	Misc	VIO		1		2
TS_NESTLCPLL_P0_P_PIN_HFC_P	Nest LC PLL High Frequency Characterization	Misc	VIO		1		2
TS_OCC_PIN_P_P0_ALERT_B	OCC Alert Input	Misc	VSB0_3P30		1		13
TS_TST_PIN_P_P0_FORCE_PWR_ON	Force Power On	Misc	VIO	CMOS	1	Rec	11
TS_TST_PIN_P_P0_LSSD_TE	LSSD Test Enable	Misc	VSB_1P10	CMOS	1	Rec	11
PV_TPM_P0_P_PIN_RESET	TPM Reset Output	TPM	VIO	CMOS	1	Drv	14
PV_TPM_PIN_P_P0_INT	TPM Interrupt Input	TPM	VIO	CMOS	1	Rec	15

1. For the Master processor, tie to GND. For additional processors: tie to GND if the processor will always be there or to the BMC for presence detection.
2. Do not connect to anything (N/C).
3. If used, pull up to 3.3 V_{AUX} with a 3.3 KΩ resistor. If not used, tie to GND with a 49.9 Ω resistor.
4. IBM suggests using GPIO1 for GPU power braking.
5. Unused. Tie off with a nopopped 49.9 Ω pull-up to 1.1 V_{AUX} and a populated 49.9 Ω pull-down to GND.
6. Unused. Tie off with a nopopped 3.3 KΩ pull-up to 3.3 V_{AUX} and a populated 49.9 Ω pull-down to GND.
7. For a single-socket system or the first processor of a two-socket system, tie to GND through a 49.9 Ω resistor (this indicates the Master processor). For the second processor, tie to 1.1 V_{AUX} through a 49.9 Ω resistor (this indicates the Slave processor).
8. This signal has a 1 KΩ internal pull-up resistor; add a nopopped 10 KΩ pull-up resistor to 1.1 V_{AUX} on board. IBM recommends a 1 nF - 10 nF capacitor to GND for noise dampening.
9. Requires a 1.2 KΩ pull-up to 1.1 V_{AUX} or must always be actively driven (like an AUC17 gate). IBM recommends a 1 nF capacitor to GND for noise dampening.
10. This signal has an internal pull-up; N/C on the planar.
11. Tie off with a pull down to GND through a 49.9 Ω resistor.
12. Digital thermal sensor analog test output. This pin is used for debug only; leave as N/C on the system board.
13. Throttle signal, active low. This pin can be asserted through hardware in the case of an emergency power down to tell the OCC to go to the power state defined for N mode. Validate the throttle pin use case with your IBM AE. Created from power supply PGOOD signals. Connect using a 1 KΩ series resistor at the processor; also connect to the BMC. No pull-up is required if this signal is always actively driven. Otherwise, pull up with a resistor between 1 - 5 KΩ to 3.3 V_{AUX}. If not using this signal, tie off with a resistor between 1 - 4.7 KΩ to 3.3 V_{AUX}.
14. The first processor requires a 1 KΩ pull-up resistor to V_{IO}; combine with system reset and wire to reset the TPM device. For additional processors or an unused TPM, tie off with a 2 KΩ pull-up to V_{IO}.
15. The first processor requires a pull-up resistor ≤1 KΩ to V_{IO}; wire to the TPM interrupt logic. Note that the actual value of the pull-up might be system-application dependent. For additional processors or an unused TPM, tie off with a 1 KΩ pull-down to GND.

5.2.13 Test Signals

Table 5-15 lists the test signals.

Table 5-15. Test Signals (Sheet 1 of 2)

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
TS_CACHE0001_P0_P_PIN_VDD_ VSENSE	Internal Kelvin Monitors for Characterization Connector	Char	Analog			1	1
TS_CACHE0203_P0_P_PIN_GSENSE	Internal Kelvin Monitors for Characterization Connector	Char	Analog			1	1
TS_CACHE0203_P0_P_PIN_VCS_ VSENSE		Char	Analog			1	1
TS_CLK_P0_P_PIN_PROBE0_N	Characterization Probe 0 Output Negative	Char	VIO			1	1
TS_CLK_P0_P_PIN_PROBE0_P	Characterization Probe 0 Output Positive	Char	VIO			1	1
TS_CLK_P0_P_PIN_PROBE1_N	Characterization Probe 1 Output Negative	Char	VIO			1	1
TS_CLK_P0_P_PIN_PROBE1_P	Characterization Probe 1 Output Positive	Char	VIO			1	1
TS_EQ0_P0_P_PIN_GSENSE		Char	Analog			1	1
TS_EQ0_P0_P_PIN_VDDIN_VSENSE		Char	Analog			1	1
TS_EQ1_P0_P_PIN_VCSIN_VSENSE		Char	Analog			1	1
TS_EQALL_P0_P_PIN_AMUX_GSENSE		Char	Analog			1	1
TS_EQALL_P0_P_PIN_AMUX_VSENSE		Char	Analog			1	1
TS_EX00C0_P0_P_PIN_GSENSE		Char	Analog			1	1
TS_EX00C0_P0_P_PIN_VSENSE		Char	Analog			1	1
TS_EX00C1_P0_P_PIN_GSENSE		Char	Analog			1	1
TS_EX00C1_P0_P_PIN_VSENSE		Char	Analog			1	1
TS_EX01C0_P0_P_PIN_GSENSE		Char	Analog			1	1
TS_EX01C0_P0_P_PIN_VSENSE		Char	Analog			1	1
TS_EX01C1_P0_P_PIN_GSENSE		Char	Analog			1	1
TS_EX01C1_P0_P_PIN_VSENSE		Char	Analog			1	1
TS_EX0203_P0_P_PIN_L3_GSENSE		Char	Analog			1	1
TS_EX0203_P0_P_PIN_VBL_VSENSE		Char	Analog			1	2
TS_EX0203_P0_P_PIN_VPP_VSENSE		Char	Analog			1	2
TS_EX0203_P0_P_PIN_VWL_VSENSE		Char	Analog			1	1
TS_PRV_P0_P_PIN_PROBE2	Characterization Probe 2 Output	Char	VSB_1P10	CMOS	Drv	1	1
TS_PRV_P0_P_PIN_PROBE3	Characterization Probe 3 Output	Char	VSB_1P10	CMOS	Drv	1	1

1. Connect to debug connector as shown in the CRB.
2. Unused, N/C.

Table 5-15. Test Signals (Sheet 2 of 2)

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
TS_PRV_P0_P_PIN_PROBE4	Characterization Probe 4 Output	Char	VSB_1P10	CMOS	Drv	1	1
TS_VCS_P0_P_PIN_VSENSE	Internal Kelvin Monitors for Characterization Connector	Char	Analog			1	1
TS_VDDR0_P0_P_PIN_GSENSE	Internal Kelvin Monitors for Characterization Connector	Char	Analog			1	1
TS_VDDR0_P0_P_PIN_VSENSE	Internal Kelvin Monitors for Characterization Connector	Char	Analog			1	1
TS_VDDR6_P0_P_PIN_GSENSE	Internal Kelvin Monitors for Characterization Connector	Char	Analog			1	1
TS_VDDR6_P0_P_PIN_VSENSE	Internal Kelvin Monitors for Characterization Connector	Char	Analog			1	1
TS_VDN_P0_P_PIN_GSENSE	Internal Kelvin Monitors for Characterization Connector	Char	Analog			1	1
TS_VDN_P0_P_PIN_VSENSE	Internal Kelvin Monitors for Characterization Connector	Char	Analog			1	1
TS_VIO0_P0_P_PIN_GSENSE	Internal Kelvin Monitors for Characterization Connector	Char	Analog			1	1
TS_VIO0_P0_P_PIN_VSENSE	Internal Kelvin Monitors for Characterization Connector	Char	Analog			1	1

1. Connect to debug connector as shown in the CRB.
2. Unused, N/C.

5.2.14 Thermal Diode and Monitor Signals

Table 5-16 lists the thermal diode and monitor signals.

Table 5-16. Thermal Diode and Monitor Signals

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
TS_EX05_P0_P_PIN_TDIODE_A	Core 05 Thermal Diode Anode	Thermal Diode	Analog			1	1
TS_EX05_P0_P_PIN_TDIODE_C	Core 05 Thermal Diode Cathode	Thermal Diode	Analog			1	1
TS_EX06_P0_P_PIN_TDIODE_A	Core 06 Thermal Diode Anode	Thermal Diode	Analog			1	1
TS_EX06_P0_P_PIN_TDIODE_C	Core 06 Thermal Diode Cathode	Thermal Diode	Analog			1	1

1. Do not connect.

5.2.15 Regulator Sense Signals

Table 5-16 lists the regulator sense signals.

Table 5-17. Regulator Sense Signals

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
VCS_CHIP_GSENSE	Regulator GND Sense Point on Socket for VCS	Regulator Sense				1	1
VCS_CHIP_VSENSE	Regulator Positive Sense Point on Socket for VCS	Regulator Sense				1	2
VDD_CHIP_GSENSE	Regulator GND Sense Point on Socket for VDD	Regulator Sense				1	3
VDD_CHIP_VSENSE	Regulator Positive Sense Point on Socket for VDD	Regulator Sense				1	4
VDN_CHIP_GSENSE	Regulator GND Sense Point on Socket for VDN	Regulator Sense				1	5
VDN_CHIP_VSENSE	Regulator Positive Sense Point on Socket for VDN	Regulator Sense				1	6

1. Negative sense point for VCS regulator.
2. Positive sense point for VCS regulator.
3. Negative sense for VDD regulator.
4. Positive sense for VDD regulator.
5. Negative sense for VDN regulator.
6. Positive sense for VDN regulator.

5.2.16 PSI Signals

Table 5-18 lists the PSI signals.

Table 5-18. PSI Signals

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
PV_PSI_P0_P_PIN_CLK_N	PSI Clock Output	PSI	VIO	EI4	DrvDiff	1	1
PV_PSI_P0_P_PIN_CLK_P	PSI Clock Output	PSI	VIO	EI4	DrvDiff	1	1
PV_PSI_P0_P_PIN_DAT	PSI Data Output	PSI	VIO	EI4	Drive	1	1
PV_PSI_PIN_P_P0_CLK_N	PSI Clock Input	PSI	VIO	EI4	RecDiff	1	1
PV_PSI_PIN_P_P0_CLK_P	PSI Clock Input	PSI	VIO	EI4	RecDiff	1	1
PV_PSI_PIN_P_P0_DAT	PSI Data Input	PSI	VIO	EI4	Rec	1	1

1. Do not connect on BMC-based designs.

5.2.17 BEOL Sense Signals

Table 5-19 lists the BEOL sense signals.

Table 5-19. BEOL Sense Signals

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	Notes
PV_PRV_PIN_P_P0_BSENSE0	BEOL Sense 0	BEOL Sense	VIO	CMOS	Rec	1	1
PV_PRV_PIN_P_P0_BSENSE1	BEOL Sense 1	BEOL Sense	VIO	CMOS	Rec	1	1
PV_PRV_PIN_P_P0_BSENSE2	BEOL Sense 2	BEOL Sense	VIO	CMOS	Rec	1	1
PV_PRV_PIN_P_P0_BSENSE3	BEOL Sense 3	BEOL Sense	VIO	CMOS	Rec	1	1

1. Connect directly to GND on the board.

5.2.18 25G Link Signals

Table 5-20 lists the 25G Link signals.

Table 5-20. 25G Link Signals

Signal	Description	Interface	I/O Voltage Domain	Family	Type	Pin Count	
NV_NV0_P0_P_PIN_DAT_[0:23]_N	25G Link 0 Data Output N	25G Link	VIO		DrvDiff	24	
NV_NV0_P0_P_PIN_DAT_[0:23]_P	25G Link 0 Data Output P	25G Link	VIO		DrvDiff	24	
NV_NV0_PIN_P_P0_DAT_[0:23]_N	25G Link 0 Data Input N	25G Link	VIO		RecDiff	24	
NV_NV0_PIN_P_P0_DAT_[0:23]_P	25G Link 0 Data Input P	25G Link	VIO		RecDiff	24	
PV_NV0_P0_P_PIN_REFCLK_N	25G Link Reference Clock Output	25G Link	VIO		DrvDiff	1	1
PV_NV0_P0_P_PIN_REFCLK_P	25G Link Reference Clock Output	25G Link	VIO		DrvDiff		1
PV_NV0_P0_P_PIN_TERMREF_N	25G Link Terminal Reference Negative	25G Link	Analog	Analog	AnalogIn	1	2
PV_NV0_P0_P_PIN_TERMREF_P	25G Link Terminal Reference Positive	25G Link	Analog	Analog	AnalogIn	1	2
PV_NV1_P0_P_PIN_REFCLK_N	25G Link 1 Reference Clock Output	25G Link	VIO		DrvDiff	1	1
PV_NV1_P0_P_PIN_REFCLK_P	25G Link 1 Reference Clock Output	25G Link	VIO		DrvDiff	1	1
TS_NV0_P0_P_PIN_ATST	25G Link 0 Analog Test	25G Link	Analog	Analog		1	3
TS_NV0_P0_P_PIN_HFC_N	25G Link 0 High Frequency Characterization	25G Link	VIO			1	3
TS_NV0_P0_P_PIN_HFC_P	25G Link 0 High Frequency Characterization	25G Link	VIO			1	3

1. Requires a 49.9 Ω pull-down resistor on each leg.
2. Requires a 169 Ω, 0.1% resistor between the P and N legs.
3. Unused, N/C.

6. Electrical Characteristics

This section provides AC and DC electrical specifications and thermal characteristics for the POWER9 processor.

6.1 Frequency Domains

Table 6-1 lists the POWER9 chip frequency domains and scan frequency domains.

Table 6-1. POWER9 Frequency Domains (Sheet 1 of 2)

Region	IP	Ship Frequency	Maximum Frequecy	Minimum Frequency	Supply Type	Notes
Core/L2	Core, L2	Varied	4.2 GHz	1.2 GHz (200 MHz)	Adaptive & Dynamic	
Chiplet	L3, NCU	Varied	2.1 GHz	1.2 GHz (200 MHz)	Adaptive & Dynamic	
Nest Logic	Nest	2.0 GHz	2.4 GHz	1.6 GHz	Adapt, Static	1
MCA DDR Logic	DDR	2.667 GHz	2.667 GHz	1.866 GHz	Adapt, Static	2
		2.400 GHz	2.400 GHz	1.866 GHz		3
MCIO DDR	DDR	1.33 GHz	1.33 GHz	0.8 GHz	Adapt, Static (VDN)	
MCIO DDR	DDR	1.33 GHz	1.33 GHz	0.8 GHz	Adapt, Static (VDN)	
X Logic Async	X0 - 5	2.0 GHz	2.0 GHz	2.0 GHz	Adapt, Static	
XIO PHY Data	X0 - 5	2.0 GHz	2.0 GHz	2.0 GHz	Adapt, Static	
XIO PHY Data	X0 - 5	2.0 GHz	2.0 GHz	2.0 GHz	Mixed (VIO, VDN)	
XIO PHY	X0 - 5	8.0 GHz	8.0 GHz	8.0 GHz	Fixed (VIO)	
Optics Logic	Optics	1.611 GHz	1.611 GHz	1.2 GHz	Adapt, Static	
Opt 25G Link Logic	Optics	1.611 GHz	1.611 GHz	1.2 GHz	Adapt, Static	
Optics PHY Data	Optics	1.611 GHz	1.611 GHz	1.2 GHz	Adapt, Static	
Optics TX	Optics	1.611 GHz	1.611 GHz	1.2 GHz	Mixed	
Optics PHY	Optics	12.89 GHz	12.89 GHz	6.25 GHz	Fixed (VIO)	
OPTREF	Optics	156.25 MHz	156.25 MHz	133.33 MHz	Adapt, Static	

1. A nest frequency of 1.6 GHz limits the maximum DRAM frequency to 2400 MHz.
2. Memory is asynchronous to the nest.
3. Memory is synchronous with the nest.

Table 6-1. POWER9 Frequency Domains (Sheet 2 of 2)

Region	IP	Ship Frequency	Maximum Frequecy	Minimum Frequency	Supply Type	Notes
PCIe	PCIe	2.0 GHz	2.0 GHz	2.0 GHz	Adapt, Static	
PCI PHY	PCI	16/8/5.5/2.5 GHz	16/8/5.5/2.5 GHz	16/8/5.5/2.5 GHz	Fixed (VIO)	
PCI PHY	PCI	2.0 GHz	2.0 GHz	2.0 GHz	Adapt, Static (VDN)	
PCI PHY	PCI	2.0 GHz	2.0 GHz	2.0 GHz	Adapt, Static (VDN)	
PCIREF	PCI	100 MHz	100 MHz	100 MHz	Fixed (VDN)	
PCIFB	PCI	100 MHz	118.5 MHz	100 MHz	Fixed (VDN)	
PCIAPBCLK	PCI	250 MHz	250 MHz	250 MHz	Adapt, Static (VDN)	
PSI	PSI	333 MHz	333 MHz	166 MHz	Mixed (VIO, VDN)	
FSI	FSI	166 MHz	166 MHz	1 KHz	Fixed (VSB)	
JTAG	JTAG macro	50 MHz	50 MHz	50 Mhz	Fixed (VIO)	
JTAG TCK	DDR / PCIe	50 MHz	50 MHz	50 MHz	Adapt, Static (VDN)	
LPC	Perv	33 MHz	33 MHz	33 MHz	Adapt, Static	

1. A nest frequency of 1.6 GHz limits the maximum DRAM frequency to 2400 MHz.
2. Memory is asynchronous to the nest.
3. Memory is synchronous with the nest.

6.2 DC Electrical Characteristics

Table 6-2 through *Table 6-7* on page 66 provide the V_{DD}, V_{CS}, V_{DN}, V_{IO}, AV_{DD}/DV_{DD}, and V_{DDR} voltage requirements for the POWER9 processor.

Table 6-2. POWER9 Processor V_{DD} (Core) Voltage Requirements

DC Voltage[1]	Maximum	1.155 V			Specifies the DC voltage range at the remote sense pin.
	Boot Voltage	1.0 V			
	Minimum	0.6 V			
AC Voltage	Maximum	1.2			Duration must not exceed 20 µs at a time.
Load Line	200 - 300 µΩ				The value, 254 µΩ, is highly recommended to minimize system characterization and software coding.
Regulation Set-Point Tolerance	±5.0 mV				Based on the VID table for 5 mV settings.
Dynamic VID Slew Rate	±10.0 mV/µs				Deviations must be reviewed by IBM.
AC Noise (any source)	±9% at remote sense pin				AC noise budget contains an allowable regulation ripple and transient load-step/release response.
Maximum Current Load	250 W	268 A (TDC)	286 A (RDC)	343 A (Boost)[2]	TDC, RDC, and boost values.
Minimum Current Load	2 A				
Current Load Step[3]	250 W	207 A 248 A			Idle to TDP. Idle to RDP to boost peak current.
Load Step Slew Rate	400 A/µs				Slew rate as seen by the socket for the purpose of power validation testing.
Remote Sense Required?	Yes				

1. Voltage ID (VID) is set via the AVSBus using OCC code.
2. Boost current sustained for ≤ 4 ms at 5% duty cycle.
3. Both idle-to-TDP and idle-to-RDP assume boost is enabled.

Table 6-3. POWER9 Processor V_{CS} (Cache) Voltage Requirements

DC Voltage[1]	Maximum	1.155 V	Specifies the DC voltage range at the remote sense pin.
	Boot Voltage	1.03 V	
	Minimum	0.96 V	
Load Line	0 - 300 µΩ		A 0 µΩ value is highly recommended to minimize system characterization and software coding.
Regulation Set-Point Tolerance	±5.0 mV		
AC Noise (any source)	±4%		AC noise budget contains an allowable regulation ripple and transient load-step/release response.
Maximum Current Load	18 A (TDC)	20 A (RDC)	
Minimum Current Load	0 A		
Current Load Step	12 A		
Load Step Slew Rate	30 A/µs		
Remote Sense Required?	Yes		

1. Voltage is set via the AVSBus. It is recommended to use a second loop from the V_{DD} or V_{DN} regulator.

Table 6-4. POWER9 Processor V_{DN} Voltage Requirements

DC Voltage[1]	Maximum	1.155 V	Specifies the DC voltage range at the remote sense pin.
	Boot Voltage	0.9 V	
	Minimum Voltage	0.65 V	
Regulation Set-Point Tolerance	±5 mV		
Dynamic VID Slew Rate	±10 mV/µs		
AC Noise (any source)	±3.0%		AC noise budget contains an allowable regulation ripple.
Maximum Current Load	32 A (TDC)	40 A (RDC)	One-socket system.
	64 A (TDC)	72 A (RDC)	Two-socket system.
Minimum Current Load	10 A		
Current Load Step	25 A		
Load Step Slew Rate	100 A/µs		
Remote Sense Required?	Yes		

1. Voltage set via the AVSBus.

Table 6-5. POWER9 Processor V_{IO} Voltage Requirements

DC Voltage	1.10 V	Measured at the socket interface pin.
Regulation Set-Point Tolerance	±2.0%	Not to exceed the C4 maximum of 1.155 V.
AC Noise (any source)	±5.0%	AC noise budget contains an allowable regulation ripple and transient load-step/release response. **Note:** Measured at the socket interface pins.
Maximum Current Load	21 A	One-socket system.
	30 A	Two-socket system.
Current Load Step	7 A	
Load Step Slew Rate	30 A/µs	
Remote Sense Required?	Yes	Remote sense is required but socket pins are not dedicated to this voltage rail. The designer must ensure that the regulator DC voltage ± regulation setpoint tolerance is maintained at the socket interface pins.

Table 6-6. POWER9 Processor AV_{DD}/DV_{DD} Voltage Requirements

DC Voltage	1.5 V	
Regulation Set-Point Tolerance	±2%	
AC Noise (any source)	±8%	AC noise budget contains an allowable regulation ripple and transient load-step/release response. **Note:** Measured at the socket interface pins.
Maximum Current Load	2.0 A	**Note:** This is the total current for both AV_{DD} and DV_{DD}.
Maximum I_{AVDD}	1.0 A	
Maximum I_{DVDD}	1.0 A	
Current Load Step	0.1 A	
Load Step Slew Rate	1 A/µs	

Table 6-7. POWER9 DDR4 Voltage Requirements

DC Voltage	1.2 V	
Regulation Set-Point Tolerance	±0.5%	
DC and AC Noise (any source)	±5%	Required at each load by the JEDEC specification.
Maximum Current Load	13 A	Per V_{DDR} domain (two per processor socket, four ports per side).
	26 A	Total per socket.
Current Load Step	5 A	
Load Step Slew Rate	30 A/µs	

6.2.1 General System Voltage Requirements

Table 6-8 and *Table 6-9* show the voltages expected to be supplied to various loads around the system. These voltages can be shared with other devices in the system as long as the DC and AC levels are met at the processor.

Table 6-8. 1.1 V_{SB}: Standby/Auxiliary

DC Voltage	1.1 V	
Regulation Set-Point Tolerance	±1%	
AC Noise (any source)	±3.0%	AC noise budget contains an allowable regulation ripple and transient load-step/release response.
Maximum Current Load (Processor)	0.5 A	
Load Step Slew Rate	1 A/µs	

Table 6-9. 3.3 V_{SB}: Standby/Auxiliary

DC Voltage	3.3 V	
Regulation Set-Point Tolerance	±1.5%	
AC Noise (any source)	±4.5%	AC noise budget contains an allowable regulation ripple and transient load-step/release response.
Maximum Current Load (processor)	0.1 A	
Load Step Slew Rate	1 A/µs	

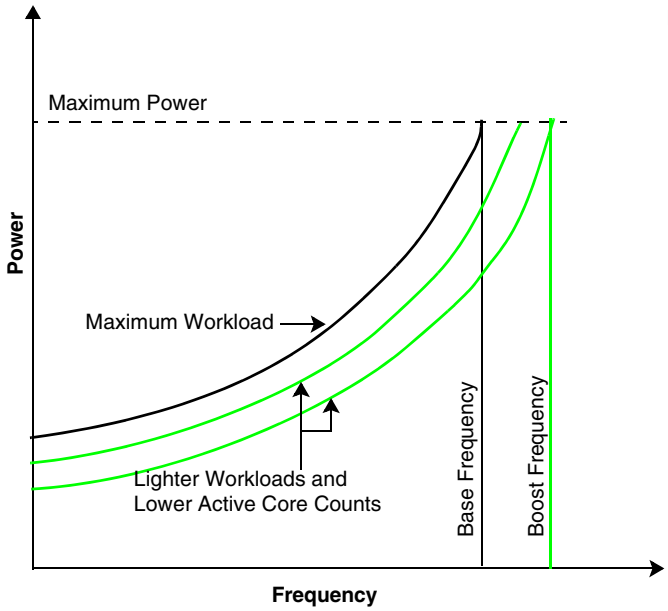
6.2.2 Power and Frequencies

The maximum socket power shown in *Table 6-10* represents the power consumed under maximum workload conditions with all cores active and in any allowed environmental condition (ambient temperature or altitude). It is possible to exceed this maximum power with a contrived power virus workload that toggles transistors in the processor on and off, but does not do any real work. This virus-like code can cause the processor to exceed the maximum power for a thermally-significant period of time. Consequently, the thermal subsystem must be designed such that the T_J (maximum) can be maintained while dissipating that maximum power and while under all specified environmental conditions. If T_J cannot be maintained as previously described, the frequency is reduced by the on-chip controller (OCC) to below base frequency and errors are surfaced to the user.

Additionally, the OCC takes advantage of inactive cores, lower-power consuming workloads, and favorable environmental conditions to allow the frequency to be increased above base frequency up to the boost frequency. The maximum socket power remains the same[3], but the frequency is increased to take advantage of the available power headroom. Note that the actual frequency is still selected by Linux based on the governor and that the OCC only sets the maximum frequency that is allowed.

Figure 6-1 on page 67 shows an example of frequency ranges and various governor settings.

Figure 6-1. Workloads and Frequencies



Notes:

- Maximum frequency attained.
  - Base frequency is guaranteed under all workloads, environmental conditions, and active core counts.
  - Boost frequency is attained under favorable environmental conditions, low workloads, and low active core counts.
- Standard Linux governors used to control frequency.
  - Ondemand: The frequency selected varies with utilization across the entire range from minimum to boost.
  - Maximum performance: Always try to run at the boost frequency.
  - Powersave: Always run at the minimum frequency.
  - User-defined fixed frequency: Try to run at a fixed point anywhere in the range from minimum to boost.

3. During boost conditions, a change in workload can cause a momentary spike in power that can exceed the socket power limit for a period no longer than 4 ms at a 5% duty cycle. To support boost frequency, the system and regulator should be designed with these conditions in mind.

Table 6-10 lists the power and frequencies for the POWER9 Monza SCM part numbers.

Table 6-10. Power, Frequencies, and Junction Temperature[1]

Part Number	Processor Design Revision	Active Cores	Maximum SMT Mode	Nest Frequency (GHz)	Boost Frequency (GHz)[1]	Base Frequency (GHz)	Maximum Socket Power (W)	L3 Cache (MB)	T_J Maximum (°C)
03JM924	DD2.3	24	SMT4	2.00	3.8	3.150	300	120	85
02CY598	DD2.3	22	SMT4	2.00	3.8	3.100	300	110	85
02CY599	DD2.3	20	SMT4	2.00	3.8	3.000	250	100	85
02CY600	DD2.3	18	SMT4	2.00	3.8	3.450	300	90	85
02CY601	DD2.3	16	SMT4	2.00	3.8	3.300	250	80	85

1. Indicates the maximum frequency achievable under favorable environmental condtions, low workloads, and low-active core counts.

6.2.3 Miscellaneous Signals

See the *I^2C Bus Specification (version 2.1)* for DC electrical details of the I^2C bus.

Table 6-11. I^2C DC Voltage

DC Voltage	Description
I^2C Voltage	3.3 V V_{DD}
V_{IH}	$V_{DD} \times 0.7 = 2.3$ V
V_{IL}	$V_{DD} \times 0.3 = 0.99$ V

See the *PCI Local Bus Specification (Revision 3.0)* for DC electrical details for the LPC bus.

6.3 AC Electrical Characteristics

This section provides the preliminary AC electrical characteristics for the POWER9 processor. After fabrication, parts are sorted by maximum processor core frequency and tested for conformance to the AC specifications for that frequency.

6.3.1 Clock AC Specifications

System reference clocks are 133.33 MHz and use host clock signal level (HCSL) differential levels, which are the same as the PCIe standard levels. The POWER9 processor defaults to no internal termination on the reference clock inputs. Care must be taken to ensure that the clocks are properly terminated.

Spread spectrum is only allowed on the system reference clocks. It is limited to a spread percentage of 0.5% in the downward direction, which is the specified maximum allowed by the DRAMs and PCIe.

The PCIe reference clocks are 100.0 MHz and use HCSL differential levels, which are the same as the PCIe standard levels. The POWER9 processor defaults to no internal termination on the reference clock inputs. Care must be taken to ensure that the clocks are properly terminated. The POWER9 processor chip can be configured to allow the system reference clock to be used to generate the PCIe reference clocks if spread spectrum on the PCIe interfaces is required.

The LPC clock to the processor is a 33.33 MHz single-ended CMOS with an MPUL of 1.1 V. The IBM system has a resistor divider network on the board to support this. The reference clock skew specification for LPC is 2.0 ns.

Figure 6-2 shows the differential HCSL reference clock waveforms.

Figure 6-2. Differential (HCSL) Reference Clock Waveform (System and PCIe)

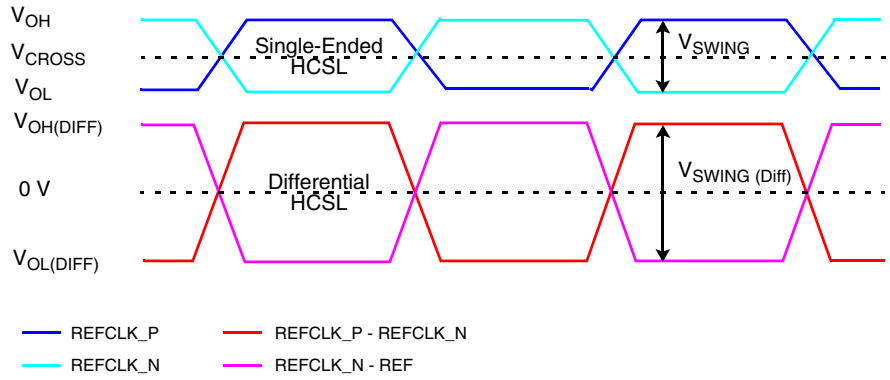


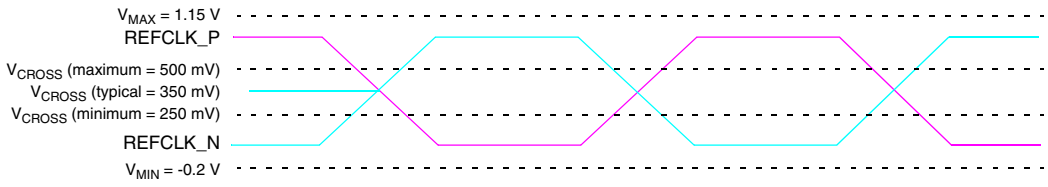
Table 6-12. Differential Reference Clock DC and AC Specification

Symbol	Parameter	Minimum	Typical	Maximum	Units	Notes
V_{OL}	Output low voltage	-0.10	0.0	0.1	V	1
V_{OH}	Output high voltage	0.50	0.70	0.90	V	1
V_{SWING}	Voltage swing	0.50	0.70	1.0	V	1
V_{CROSS}	Absolute crossing point (common mode voltage)	250	350	500	mV	1, 2, 3
V_{CROSS} Delta	Maximum variation in common mode voltage	–	–	100	mV	1, 2, 4
V_{MAX}	Absolute maximum voltage	–	–	1.15	V	1, 5
V_{MIN}	Absolute minimum voltage	-0.20	–	–	V	1, 6
V_{OL} (Diff)	Output low voltage	-0.5	-0.7	-0.9	V	7
V_{OH} (Diff)	Output high voltage	0.50	0.70	0.90	V	7
V_{SWING} (Diff)	Voltage swing (differential)	1.0	1.4	1.8	V	7
T_R, T_F (Diff)	Rising and falling edge rates (differential)	1.0	2.0	4.0	V/ns	7, 8
V_{RB}	Ringback voltage margin	-100	–	100	mV	7, 9
T_{STABLE}	Time before V_{RB} is allowed	500	–	–	ps	7, 9
Duty Cycle	Duty cycle	45	–	55	%	7
T Period Average	Average clock period accuracy	50	–	2550	PPM	7, 10, 11, 12

1. Measurement taken from a single-ended waveform (see *Table 6-2* on page 69).
2. Measured at the crossing point where the instantaneous voltage value of the rising edge of REFCLK_P equals the falling edge of REFCLK_N (see *Figure 6-3* on page 71).
3. Refers to the total variation from the lowest crossing point to the highest crossing point, regardless of which edges are crossing. Refers to all crossing points for this measurement (see *Figure 6-3* on page 71).
4. Defined as the total variation of all crossing voltages of rising REFCLK_P and falling REFCLK_N. This is the maximum allowed variance in V_{CROSS} for any system (see *Figure 6-4* on page 72).
5. Defined as the maximum instantaneous voltage including overshoot (see *Figure 6-3* on page 71).
6. Defined as the minimum instantaneous voltage including overshoot (see *Figure 6-3* on page 71).
7. Measurement taken from a differential waveform (see *Figure 6-2* on page 69).
8. Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK_P - REFCLK_N). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing (see *Figure 6-6* on page 72).
9. T_{STABLE} is the time that the differential clock must maintain a minimum ±150 mV differential voltage after the rising/falling edges before it is allowed to drop back into the V_{RB} ±100 mV differential range (see *Figure 6-7* on page 73).
10. Defined as the average period. This includes crystal PPM and spread spectrum.
11. Defined as the frequency accuracy specification of the crystal that is used to generate the reference clock (typically less than 100 PPM).
12. PPM refers to parts per million and is a DC absolute period accuracy specification. One PPM is 1/1,000,000 of the clock frequency. The period is measured with a frequency counter with the measurement window set to 100 ms or greater. For systems that use spread-spectrum clocking, there is an additional 2500 PPM average shift in the maximum period resulting from a 0.5% down spread.

Figure 6-3 shows the single-ended measurement points for absolute cross points and swing.

Figure 6-3. Single-Ended Measurement Points for Absolute Cross Points and Swing



6.3.2 Differential Reference Clock Measurements

Figure 6-4 shows the single-ended measurement points for the delta cross point.

Figure 6-4. Single-Ended Measurement Points for Delta Cross Point

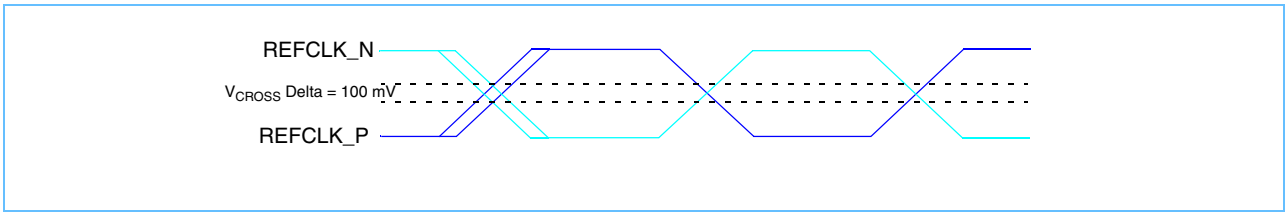


Figure 6-5 shows the differential measurement points for the duty cycle and period.

Figure 6-5. Differential Measurement Points for Duty Cycle and Period

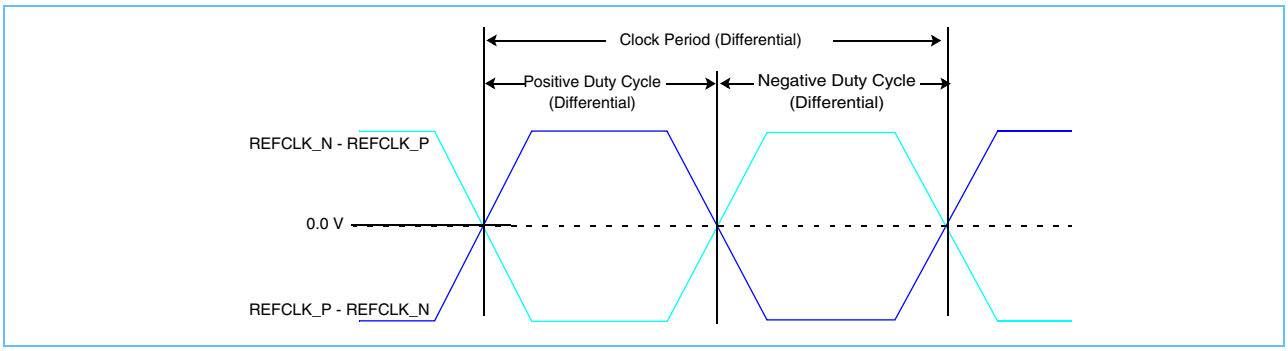


Figure 6-6 shows the differential measurement points for the rise and fall times.

Figure 6-6. Differential Measurement Points for Rise and Fall Times

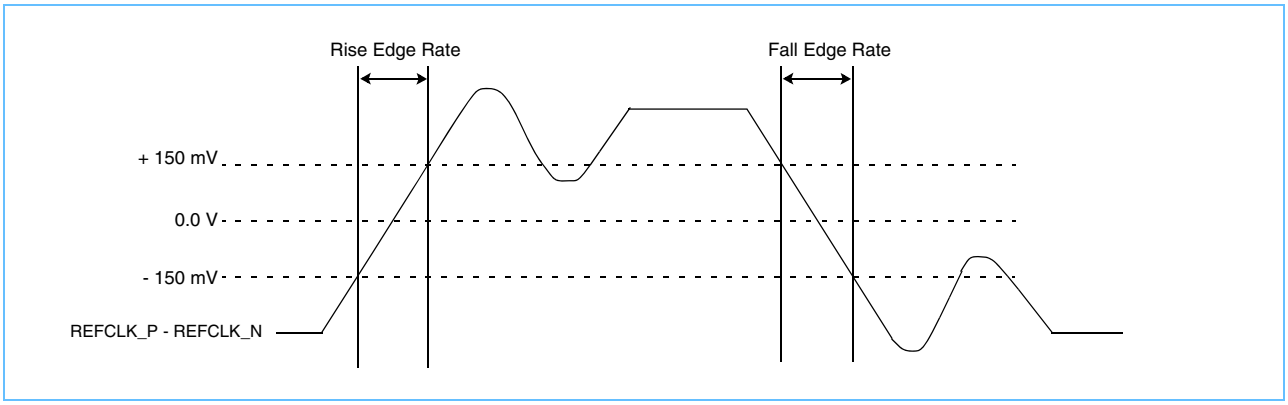


Figure 6-7 shows the differential measurement points for ringback.

Figure 6-7. Differential Measurement Points for Ringback

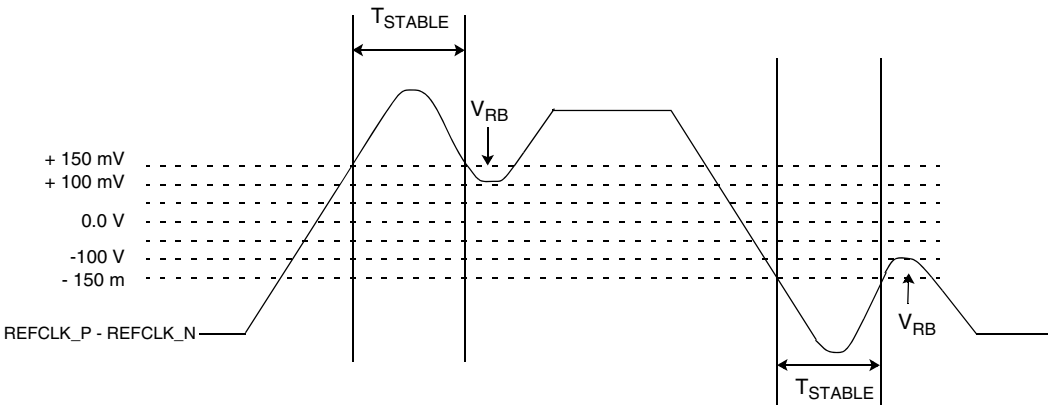


Table 6-13 lists general DC and AC specifications.

Table 6-13. DC and AC Specifications

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units	Notes
Output Voltage	V_{OL}	Output low voltage	–	0	0.2	V	1
	V_{OH}	Output high voltage	0.8	1.0	1.15	V	1
	V_{SWING}	Peak-peak, single-ended swing	0.8	1.0	1,15	V	1, 2
Rise and Fall Times	T_R, T_F	20% - 80%	–	1.5	3.0	ns	1, 3
Duty Cycle	DC	Measured at $V_{SWING}/2$	45	–	55	%	1, 2, 4
Clock Period	T_{AVG}	Clock period accuracy	-50	–	+50	PPM	1, 2, 4, 5

1. Measurements taken from a single-ended waveform (see *Figure 6-8* on page 74).
2. Voltage swing is equal to V_{OH} - V_{OL} (see *Figure 6-8* on page 74).
3. Rise and fall time measurements taken between 20% and 80% of V_{OH} and V_{OL} (see *Figure 6-8* on page 74).
4. Measurements taken at a voltage equal to $V_{SWING}/2$ (see *Figure 6-9* on page 74).
5. PPM refers to parts per million and is a DC absolute period accuracy specification. It includes only the accuracy of the crystal that is used to generate the clock because spread spectrum is not enabled. The period is to be measured with a frequency counter with the measurement window set to 100 ms or greater.

Figure 6-8 shows the single-ended processor reference clocks and highlights the voltage and transition time measurement points.

Figure 6-8. Single-Ended Processor Reference Clocks (Voltage and Transition Time Measurement Points)

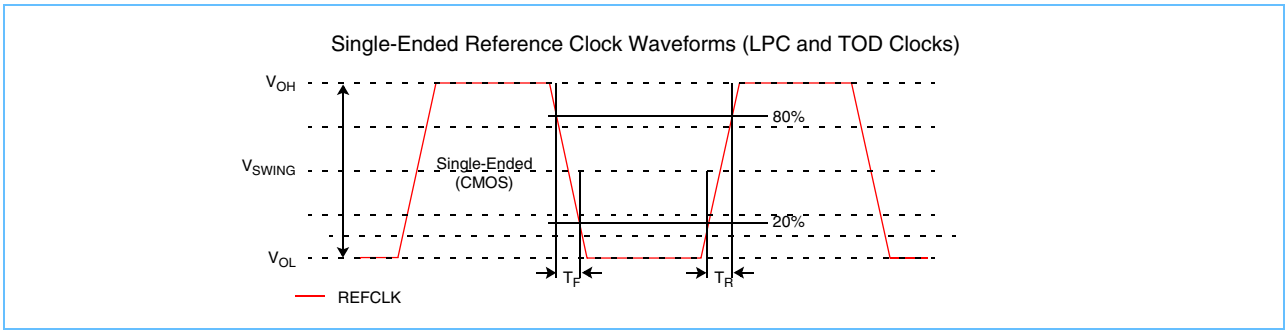
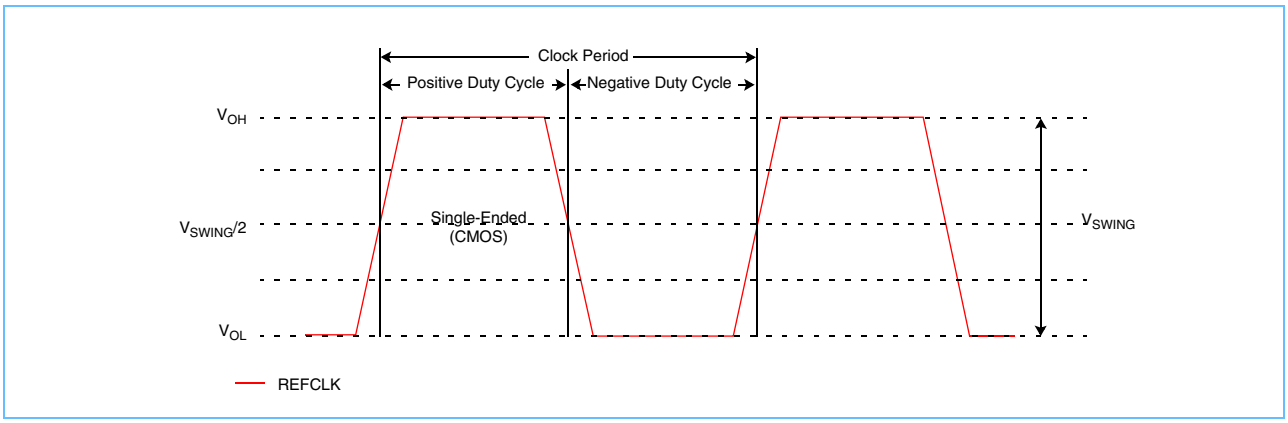


Figure 6-9 shows the single-ended processor reference clocks and highlights the period and duty cycle measurement points.

Figure 6-9. Single-Ended Processor Reference Clocks (Period and Duty-Cycle Measurement Points)



6.3.3 FSI AC Specifications

Table 6-14 lists the AC specifications for the FSI bus.

Table 6-14. FSI Electrical Specification

Description	Minimum	Typical	Maximum	Units	Notes
C4 V_{MAX}			1.15	V	Maximum voltage at the chip pad.
Receiver V_{IL}			$0.4 \times 1.1\ V_{SB}$	mV	For receiver input hysteresis.
Receiver V_{IH}	$0.6 \times 1.1\ V_{SB}$			mV	For receiver input hysteresis.
1 KΩ pull-up resistance	0.75	1.0	1.25	KΩ	Pull-up resistance without leakage. If external pull-ups are used, they must be returned to V_{DOUT} and have a combined impedance not less than 1 KΩ.
1 KΩ pull-down resistance	0.75	1.0	1.25	KΩ	Pull-down resistance without leakage. If external pull downs are used, they must have a combined impedance not less than 1 KΩ in parallel with 10 KΩ.
10 KΩ pull-down resistance	8	10	12	KΩ	Pull-up resistance without leakage.
Driver V_{OL}	$-0.1 \times 1.1\ V_{SB}$		$0.2 \times 1.1\ V_{SB}$	mV	Output pad driver levels.
Driver V_{OH}	$0.8 \times 1.1\ V_{SB}$		$1.1 \times 1.1\ V_{SB}$	mV	Output pad driver levels.
Rise/Fall time (10% - 90% of V_{DOUT} with a 2 pF load)	100	300	500	ps	

Table 6-15 lists the default settings for the internal FSI pull-up and pull-down resistors.

Table 6-15. Default FSI Settings

Function	SCM Pin	Pull-Up Internal Value	Pull-Down Internal Value
FSI0 Clock	CK50	–	1 KΩ
FSI0 Data	CL51	1 KΩ	–
FSI Master CP 1 Clock	CJ45	–	–
FSI Master CP 1 Data	CK44	–	10 KΩ

6.3.4 SPI AC Specifications

Table 6-16 list the AC specifications for the SPI bus.

Table 6-16. SPI AC Specification

Description	Minimum	Typical	Maximum	Units	Notes
C4 V_{MAX}			3.3 V	V	Maximum voltage at the chip pad.
Receiver V_{IL}			$0.3 \times 3.3\ V_{SB}$	mV	For receiver input hysteresis.
Receiver V_{IH}	$0.7 \times 3.3\ V_{SB}$			mV	For receiver input hysteresis.
1 KΩ Pull-up Resistance	1	1.25	1.5	KΩ	Pull-up resistance without leakage. If external pull ups are used, they must be returned to V_{DOUT} and have a combined impedance not less than 1 KΩ.
1 KΩ Pull-down Resistance	1	1.25	1.5	KΩ	Pull-down resistance without leakage. If external pull downs are used, they have a combined impedance not less than 1 KΩ in parallel with 10 KΩ.
10 KΩ Pull-down Resistance	10	12.5	15	KΩ	Pull-up resistance without leakage.
Driver V_{OL}	$-0.1 \times 3.3\ V_{SB}$		$0.2 \times 3.3\ V_{SB}$	mV	Output pad driver levels.
Driver V_{OH}	$0.8 \times 3.3\ V_{SB}$		$1.1 \times 3.3\ V_{SB}$	mV	Output pad driver levels.
Rise/Fall Time (10% - 90% of V_{DOUT} with a 2 pF load)	100	300	500	ps	

Table 6-17 lists the default settings for the internal SPI pull-up and pull-down resistors.

Table 6-17. Default SPI Settings

Function	Signal Name	SCM Pin	Pull-Up Internal Value	Pull-Down Internal Value	Notes
SPIPSS_MOSI	PV_APSS_P0_P_PIN_MOSI	CK38	–	10 KΩ	
SPIPSS_MISO	PV_APSS_PIN_P_P0_MISO	CJ41		10 KΩ	
SPIPSS_SCLK	PV_APSS_P0_P_PIN_SCLK	CL39		10 KΩ	1
SPIPSS_CS0	PV_APSS_P0_P_PIN_CS0	CH42	1 KΩ	–	
SPIPSS_CS1	PV_APSS_P0_P_PIN_CS1	CJ39	1 KΩ	–	

1. For the PV_APSS_P0_P_PIN_SCLK pin, the minimum clock frequency is 1 MHz and maximum clock frequency is 10 MHz.

6.3.5 AVS AC Specifications

Table 6-18 list the AC specifications for the AVSBus.

Table 6-18. AVS AC Specification

Description	Minimum	Typical	Maximum	Units	Notes
C4 V_{MAX}			1.15	V	Maximum voltage at the chip pad.
Receiver V_{IL}			$0.4 \times V_{IO}$	mV	For receiver input hysteresis.
Receiver V_{IH}	$0.6 \times V_{IO}$			mV	For receiver input hysteresis.
10 KΩ Pull-Down Resistance	8	10	12	KΩ	Internal pull-down.
Driver V_{OL}	$-0.1 \times V_{IO}$		$0.2 \times V_{IO}$	mV	Output pad driver levels.
Driver V_{OH}	$0.8 \times V_{IO}$		$1.1 \times V_{IO}$	mV	Output pad driver levels.
Rise/Fall Time (10% - 90% of V_{DOUT} with a 2 pF load)	100	300	500	ps	

Table 6-19 lists the default settings for the internal AVS pull-down resistors.

Table 6-19. Default AVS Settings

Function	Signal Name	SCM Pin	Pull-Down Internal Value	Pull-Up Internal Value	Notes
AVS 0 Clock	PV_AVS0_P0_P_PIN_CLK	BP64	1 KΩ		1, 2
AVS 0 Master Data	PV_AVS0_P0_P_PIN_MDATA	BN63		1 KΩ	
AVS 0 Slave Data	PV_AVS0_PIN_P_P0_SDATA	BR63		1 KΩ	
AVS 1 Clock	PV_AVS1_P0_P_PIN_CLK	BL63	1 KΩ		1, 2
AVS 1 Master Data	PV_AVS1_P0_P_PIN_MDATA	BL65		1 KΩ	
AVS 1 Slave Data	PV_AVS1_PIN_P_P0_SDATA	BM64		1 KΩ	

1. For the PV_AVS0_P0_P_PIN_CLK pin, the minimum clock frequency is 1 MHz and the maximum clock frequency is 25 MHz.
2. For DD 2.0, the pull-down internal value is 1 KΩ.

6.3.5.1 Recommended AVSBus Topology

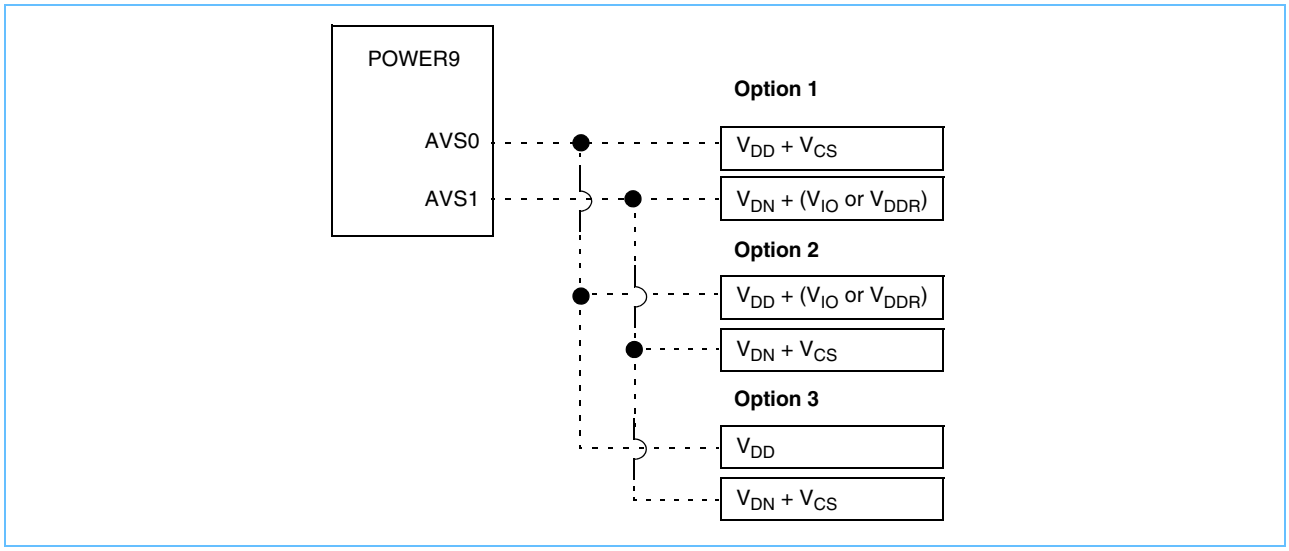
The AVSBus is part of the *PMBus 1.3 Specification*. See that document for more specific infomation. The AVSBus is a point-to-point communication interface for use with point-of-load (POL) control devices. The POWER9 processor makes use of both the Master data (MData) and Slave data (SData) connections. The Slave data connection is necessary for the OCC to get regulator telemetry. This section covers the three supported AVSBus topologies for use with the POWER9 processor.

Most AVS-compliant regulators have two regulation control loops. For both Option 1 and Option 2, the V_{DD} and V_{DN} rails should be on the first regulator control loops. V_{DD} must always be connected on AVS bus0 and V_{DN} must be connected to AVS bus1. The secondary control loop can either be V_{CS} or either V_{IO} or V_{DDR}. Option 3 is for designs that need all available regulation phases available on the controller to supply enough current for V_{DD}. In this case, V_{DN} should be on AVS bus1 and use V_{CS} on the secondary control loop. V_{IO} does not have to be connected to an AVS bus controller but should be a PMBus-compliant device. This device should be connected to the BMC.

In all options, it is highly recommended to connect the PMBus from the regulator controller to the BMC. This enables the system-management software to perform diagnostics and telemetry. It is also recommended that all voltage regulator controllers for a processor socket be on the same I^2C/PMBus. A different I^2C/PMBus should be used for each socket.

Figure 6-10 illustrates these regulation control loop options.

Figure 6-10. AVS-Compliant Regulator Options



7. Mechanical Specifications

This section describes the POWER9 SCM features and pin list.

7.1 Single-Chip Module

Table 7-1 describes the SCM.

Table 7-1. SCM Features

Feature	Description
Body Size	68.5 x 68.5 mm
Package Type	FC PLGA
Interconnect Technology	CMOS 14 nm technology
	Hybrid LGA socket
	1.016 mm hexagonal LGA pitch
	7-2-7 organic package construction
Buses	Eight DDR4 interfaces: • Up to 2666 MHz with one DIMM per channel • Up to 2400 MHz for two DIMMs per channel
	One X bus at 16 Gbps
	Two ×16 and one ×2 PCIe Generation4 buses at 16 GTps
	Six 25G Link bricks at 25 Gbps
Power	190 W and 250 W
Package Pin Assignments	3899 total
SEEPROM Structure	Dual SEEPROM

7.2 Electrostatic Discharge Considerations

The POWER9 processor is electrostatic discharge (ESD) sensitive. An appropriate ESD-handling procedure must be implemented and maintained by facilities handling this component. Handle according to the ANSI/ESD S20.20 or IEC 61340-5-1 standard. Packaging of this product in an ESD safe container must be maintained according to the ANSI/ESD S541 or IEC 61340-5-3 standard.

Table 7-2 on page 80 will be updated after the POWER9 processor has completed an ESD stress qualification in accordance with the JEDEC specification JESD47I.

Table 7-2. ESD Stress Qualification

ESD Model	Passing Level (V)	Reference
Human Body Model	1000	JS-001[1]
Charged Device Model (CDM)	200	JESD22-C101[2]

1. JS-001-2014 is the Joint JEDEC/ESDA Standard for Electrostatic Discharge Sensitivity Test - Human Body Model (HBM) Component Level.
2. JESD22-C101F is the Field-Induced Charged-Device Model Test Method for Electrostatic Discharge Withstand Thresholds of Microelectronic Components.

7.3 Mechanical Drawings

See the IBM Portal for OpenPOWER for the current mechanical drawings and recommended module layout.

7.4 Pinout

Table 7-3 POWER9 Monza SCM Pin List on page 81 shows the signal pins for the POWER9 Monza SCM by position.

Table 7-3. POWER9 Monza SCM Pin List

Pin Number	Signal Name
A03	DM_DDR6_P0_P_PIN_ADDR_05
A05	VDDR47_1P20
A07	DM_D-DR6_P0_P_PIN_BANK_GRP_0
A09	GND
A11	DM_DDR6_BI_DQ_67
A13	DM_DDR6_BI_DQ_71
A15	GND
A17	DM_DDR6_BI_DQ_65
A19	DM_DDR6_BI_DQ_68
A21	GND
A23	DM_DDR4_BI_DQ_68
A25	GND
A27	GND
A29	DM_DDR6_BI_DQ_17
A31	DM_DDR6_BI_DQ_20
A33	GND
A35	DM_DDR4_BI_DQ_20
A37	GND
A39	GND
A41	GND
A43	GND
A45	GND
A47	GND
A49	GND
A51	GND
A53	GND
A55	DM_DDR2_BI_DQ_20
A57	GND
A59	DM_DDR0_BI_DQ_05
A61	DM_DDR0_BI_DQ_00
A63	GND
A65	GND
A67	DM_DDR2_BI_DQ_68
A69	GND
A71	DM_DDR0_BI_DQ_70
A73	DM_DDR0_BI_DQ_66
A75	GND

Pin Number	Signal Name
A77	DM_DDR0_BI_DQ_68
A79	DM_DDR0_BI_DQ_64
A81	GND
B02	DM_DDR6_P0_P_PIN_ADDR_03
B04	DM_DDR6_P0_P_PIN_ADDR_08
B06	DM_DDR6_P0_P_PIN_ADDR_12
B08	DM_DDR6_P0_P_PIN_CKE_3
B10	GND
B12	DM_DDR6_BI_DQ_66
B14	GND
B16	DM_DDR6_BI_DQS_08_N
B18	DM_DDR6_BI_DQ_69
B20	GND
B22	DM_DDR4_BI_DQ_65
B24	GND
B26	GND
B28	DM_DDR6_BI_DQS_02_N
B30	DM_DDR6_BI_DQ_21
B32	GND
B34	DM_DDR4_BI_DQ_17
B36	GND
B38	GND
B40	NX_X1_PIN_P_P0_CKA_DAT_12_N
B42	GND
B44	NX_X1_PIN_P_P0_CKA_DAT_15_P
B46	GND
B48	NX_X1_P0_P_PIN_CKA_DAT_15_N
B50	NX_X1_P0_P_PIN_CKA_DAT_12_P
B52	GND
B54	GND
B56	DM_DDR2_BI_DQ_16
B58	GND
B60	DM_DDR0_BI_DQ_04
B62	DM_DDR0_BI_DQS_00_N
B64	GND
B66	GND
B68	DM_DDR2_BI_DQ_69
B70	GND

Pin Number	Signal Name
B72	DM_DDR0_BI_DQ_71
B74	DM_DDR0_BI_DQS_17_P
B76	GND
B78	DM_DDR0_BI_DQ_67
B80	GND
B82	DM_DDR2_P0_P_PIN_CKE_0
C01	DM_DDR6_P0_P_PIN_CLK_0_N
C03	GND
C05	DM_DDR6_P0_P_PIN_ADDR_07
C07	VDDR47_1P20
C09	DM_DDR6_P0_P_PIN_CKE_0
C11	GND
C13	GND
C15	DM_DDR6_BI_DQS_08_P
C17	DM_DDR6_BI_DQ_64
C19	GND
C21	DM_DDR4_BI_DQS_17_P
C23	DM_DDR4_BI_DQ_69
C25	GND
C27	DM_DDR6_BI_DQS_02_P
C29	DM_DDR6_BI_DQ_16
C31	GND
C33	DM_DDR4_BI_DQS_02_N
C35	DM_DDR4_BI_DQ_21
C37	GND
C39	GND
C41	NX_X1_PIN_P_P0_CKA_DAT_12_P
C43	NX_X1_PIN_P_P0_CKA_DAT_15_N
C45	GND
C47	NX_X1_P0_P_PIN_CKA_DAT_15_P
C49	GND
C51	NX_X1_P0_P_PIN_CKA_DAT_12_N
C53	GND
C55	DM_DDR2_BI_DQ_21
C57	DM_DDR2_BI_DQS_11_P
C59	GND
C61	DM_DDR0_BI_DQ_01
C63	DM_DDR0_BI_DQS_00_P

Pin Number	Signal Name
C65	GND
C67	DM_DDR2_BI_DQ_64
C69	DM_DDR2_BI_DQS_17_P
C71	GND
C73	DM_DDR0_BI_DQ_65
C75	DM_DDR0_BI_DQS_17_N
C77	GND
C79	GND
C81	DM_DDR2_P0_P_PIN_CKE_3
D02	DM_DDR6_P0_P_PIN_CLK_0_P
D04	DM_DDR6_P0_P_PIN_ADDR_04
D06	DM_DDR6_P0_P_PIN_ADDR_09
D08	DM_D-DR6_P0_P_PIN_BANK_GRP_1
D10	DM_DDR6_P0_P_PIN_CKE_1
D12	GND
D14	DM_DDR6_BI_DQ_70
D16	DM_DDR6_BI_DQS_17_P
D18	GND
D20	DM_DDR4_BI_DQS_17_N
D22	DM_DDR4_BI_DQ_64
D24	GND
D26	DM_DDR6_BI_DQ_23
D28	DM_DDR6_BI_DQS_11_P
D30	GND
D32	DM_DDR4_BI_DQS_02_P
D34	DM_DDR4_BI_DQ_16
D36	GND
D38	GND
D40	NX_X1_PIN_P_P0_CKA_DAT_11_N
D42	GND
D44	NX_X1_PIN_P_P0_CKA_DAT_16_P
D46	GND
D48	NX_X1_P0_P_PIN_CKA_DAT_16_N
D50	NX_X1_P0_P_PIN_CKA_DAT_11_P
D52	GND
D54	GND
D56	DM_DDR2_BI_DQ_17
D58	DM_DDR2_BI_DQS_11_N
D60	GND

Pin Number	Signal Name
D62	DM_DDR0_BI_DQS_09_P
D64	DM_DDR0_BI_DQ_07
D66	GND
D68	DM_DDR2_BI_DQ_65
D70	DM_DDR2_BI_DQS_17_N
D72	GND
D74	DM_DDR0_BI_DQS_08_N
D76	DM_DDR0_BI_DQ_69
D78	GND
D80	DM_DDR2_P0_P_PIN_CKE_2
D82	DM_D-DR2_P0_P_PIN_BANK_GRP_0
E01	VDDR47_1P20
E03	DM_DDR6_P0_P_PIN_CLK_1_N
E05	GND
E07	DM_DDR6_P0_P_PIN_ADDR_11
E09	VDDR47_1P20
E11	DM_DDR6_P0_P_PIN_RESET_B
E13	GND
E15	DM_DDR6_BI_DQS_17_N
E17	GND
E19	DM_DDR4_BI_DQ_70
E21	DM_DDR4_BI_DQS_08_N
E23	GND
E25	DM_DDR6_BI_DQ_19
E27	DM_DDR6_BI_DQS_11_N
E29	GND
E31	DM_DDR4_BI_DQ_23
E33	DM_DDR4_BI_DQS_11_P
E35	GND
E37	NX_X1_PIN_P_P0_CKA_DAT_09_N
E39	GND
E41	NX_X1_PIN_P_P0_CKA_DAT_11_P
E43	NX_X1_PIN_P_P0_CKA_DAT_16_N
E45	GND
E47	NX_X1_P0_P_PIN_CKA_DAT_16_P
E49	GND
E51	NX_X1_P0_P_PIN_CKA_DAT_11_N
E53	GND
E55	GND

Pin Number	Signal Name
E57	DM_DDR2_BI_DQS_02_N
E59	DM_DDR2_BI_DQ_22
E61	GND
E63	DM_DDR0_BI_DQS_09_N
E65	DM_DDR0_BI_DQ_02
E67	GND
E69	DM_DDR2_BI_DQS_08_N
E71	DM_DDR2_BI_DQ_70
E73	GND
E75	DM_DDR0_BI_DQS_08_P
E77	GND
E79	DM_DDR2_P0_P_PIN_ACT_B
E81	VDDR03_1P20
F02	DM_DDR6_P0_P_PIN_PAR
F04	DM_DDR6_P0_P_PIN_CLK_1_P
F06	DM_DDR6_P0_P_PIN_ADDR_02
F08	DM_DDR6_P0_P_PIN_ADDR_06
F10	DM_DDR6_PIN_P_P0_ERR_B
F12	DM_DDR6_P0_P_PIN_CKE_2
F14	GND
F16	GND
F18	DM_DDR4_BI_DQ_66
F20	DM_DDR4_BI_DQS_08_P
F22	GND
F24	DM_DDR6_BI_DQ_29
F26	DM_DDR6_BI_DQ_22
F28	GND
F30	DM_DDR4_BI_DQ_19
F32	DM_DDR4_BI_DQS_11_N
F34	GND
F36	GND
F38	NX_X1_PIN_P_P0_CKA_DAT_09_P
F40	NX_X1_PIN_P_P0_CKA_DAT_10_N
F42	GND
F44	NX_X1_PIN_P_P0_CKA_DAT_14_P
F46	GND
F48	NX_X1_P0_P_PIN_CKA_DAT_14_N
F50	NX_X1_P0_P_PIN_CKA_DAT_13_P
F52	GND

Pin Number	Signal Name
F54	NX_X1_P0_P_PIN_CKA_DAT_09_N
F56	GND
F58	DM_DDR2_BI_DQS_02_P
F60	DM_DDR2_BI_DQ_18
F62	GND
F64	DM_DDR0_BI_DQ_06
F66	DM_DDR0_BI_DQ_29
F68	GND
F70	DM_DDR2_BI_DQS_08_P
F72	DM_DDR2_BI_DQ_71
F74	GND
F76	GND
F78	DM_D-DR2_P0_P_PIN_BANK_GRP_1
F80	DM_DDR2_P0_P_PIN_ADDR_12
F82	DM_DDR2_P0_P_PIN_ADDR_09
G01	DM_DDR4_PIN_P_P0_ERR_B
G03	VDDR47_1P20
G05	DM_DDR6_P0_P_PIN_ADDR_00
G07	GND
G09	DM_DDR6_P0_P_PIN_ADDR_01
G11	VDDR47_1P20
G13	DM_DDR6_P0_P_PIN_ACT_B
G15	GND
G17	GND
G19	DM_DDR4_BI_DQ_71
G21	GND
G23	DM_DDR6_BI_DQ_25
G25	DM_DDR6_BI_DQ_18
G27	GND
G29	DM_DDR4_BI_DQ_29
G31	DM_DDR4_BI_DQ_22
G33	GND
G35	GND
G37	NX_X1_PIN_P_P0_CKA_DAT_08_N
G39	GND
G41	NX_X1_PIN_P_P0_CKA_DAT_10_P
G43	NX_X1_PIN_P_P0_CKA_DAT_14_N
G45	GND
G47	NX_X1_P0_P_PIN_CKA_DAT_14_P

Pin Number	Signal Name
G49	GND
G51	NX_X1_P0_P_PIN_CKA_DAT_13_N
G53	NX_X1_P0_P_PIN_CKA_DAT_09_P
G55	GND
G57	GND
G59	DM_DDR2_BI_DQ_23
G61	DM_DDR2_BI_DQ_28
G63	GND
G65	DM_DDR0_BI_DQ_03
G67	DM_DDR0_BI_DQ_25
G69	GND
G71	DM_DDR2_BI_DQ_66
G73	GND
G75	GND
G77	DM_DDR2_PIN_P_P0_ERR_B
G79	VDDR03_1P20
G81	DM_DDR2_P0_P_PIN_ADDR_06
G83	DM_DDR2_P0_P_PIN_ADDR_08
H02	DM_DDR4_P0_P_PIN_ADDR_09
H04	DM_DDR6_P0_P_PIN_ADDR_10
H06	DM_D-DR6_P0_P_PIN_BANK_ADR_0
H08	DM_DDR6_P0_P_PIN_ADDR_16
H10	DM_DDR6_P0_P_PIN_CS_B_2
H12	DM_D-DR6_P0_P_PIN_BANK_ADR_1
H14	DM_DDR6_PIN_P_P0_EVENT_B
H16	GND
H18	DM_DDR4_BI_DQ_67
H20	GND
H22	DM_DDR6_BI_DQS_03_N
H24	DM_DDR6_BI_DQ_28
H26	GND
H28	DM_DDR4_BI_DQ_25
H30	DM_DDR4_BI_DQ_18
H32	GND
H34	GND
H36	GND
H38	NX_X1_PIN_P_P0_CKA_DAT_08_P
H40	NX_X1_PIN_P_P0_CKA_DAT_13_N

Pin Number	Signal Name
H42	GND
H44	NX_X1_PIN_P_P0_CKB_DAT_16_P
H46	GND
H48	NX_X1_P0_P_PIN_CKB_DAT_14_N
H50	NX_X1_P0_P_PIN_CKA_DAT_10_P
H52	GND
H54	NX_X1_P0_P_PIN_CKA_DAT_08_N
H56	GND
H58	GND
H60	DM_DDR2_BI_DQ_19
H62	DM_DDR2_BI_DQ_24
H64	GND
H66	DM_DDR0_BI_DQ_28
H68	DM_DDR0_BI_DQS_12_P
H70	GND
H72	DM_DDR2_BI_DQ_67
H74	DM_DDR2_P0_P_PIN_RESET_B
H76	DM_DDR2_P0_P_PIN_ADDR_11
H78	DM_DDR2_P0_P_PIN_ADDR_05
H80	DM_DDR2_P0_P_PIN_ADDR_01
H82	DM_DDR2_P0_P_PIN_ADDR_03
H84	DM_DDR2_P0_P_PIN_ADDR_04
H86	DM_DDR2_P0_P_PIN_ADDR_02
H88	VDDR03_1P20
J01	GND
J03	DM_DDR4_P0_P_PIN_ADDR_11
J05	VDDR47_1P20
J07	DM_DDR6_P0_P_PIN_ADDR_14
J09	GND
J11	DM_DDR6_P0_P_PIN_ODT_0
J13	VDDR47_1P20
J15	DM_DDR6_P0_P_PIN_ADDR_15
J17	GND
J19	GND
J21	DM_DDR6_BI_DQS_03_P
J23	DM_DDR6_BI_DQ_24
J25	GND
J27	DM_DDR4_BI_DQS_12_P
J29	DM_DDR4_BI_DQ_28

Pin Number	Signal Name
J31	GND
J33	GND
J35	NX_X1_PIN_P_P0_CKB_CLK_N
J37	NX_X1_PIN_P_P0_CKB_DAT_10_N
J39	GND
J41	NX_X1_PIN_P_P0_CKA_DAT_13_P
J43	NX_X1_PIN_P_P0_CKB_DAT_16_N
J45	GND
J47	NX_X1_P0_P_PIN_CKB_DAT_14_P
J49	GND
J51	NX_X1_P0_P_PIN_CKA_DAT_10_N
J53	NX_X1_P0_P_PIN_CKA_DAT_08_P
J55	GND
J57	GND
J59	GND
J61	DM_DDR2_BI_DQ_29
J63	DM_DDR2_BI_DQS_12_P
J65	GND
J67	DM_DDR0_BI_DQ_24
J69	DM_DDR0_BI_DQS_12_N
J71	GND
J73	GND
J75	DM_DDR2_P0_P_PIN_ADDR_07
J77	VDDR03_1P20
J79	DM_DDR2_P0_P_PIN_CHIPID_2
J81	GND
J83	DM_DDR2_P0_P_PIN_PAR
J85	VDDR03_1P20
J87	DM_DDR2_P0_P_PIN_CLK_0_P
J89	DM_DDR2_P0_P_PIN_CLK_1_N
K02	DM_DDR4_P0_P_PIN_ADDR_06
K04	DM_DDR4_P0_P_PIN_ADDR_07
K06	DM_DDR6_P0_P_PIN_CS_B_0
K08	DM_DDR6_P0_P_PIN_ODT_2
K10	DM_DDR6_P0_P_PIN_ADDR_17
K12	DM_DDR6_P0_P_PIN_ODT_1
K14	DM_DDR6_P0_P_PIN_CHIPID_2
K16	DM_DDR6_P0_P_PIN_CS_B_3
K18	GND

Pin Number	Signal Name
K20	DM_DDR6_BI_DQ_31
K22	DM_DDR6_BI_DQS_12_P
K24	GND
K26	DM_DDR4_BI_DQS_12_N
K28	DM_DDR4_BI_DQ_24
K30	GND
K32	GND
K34	NX_X1_PIN_P_P0_CKB_CLK_P
K36	GND
K38	NX_X1_PIN_P_P0_CKB_DAT_10_P
K40	NX_X1_PIN_P_P0_CKB_DAT_13_N
K42	GND
K44	NX_X1_PIN_P_P0_CKB_DAT_15_P
K46	GND
K48	NX_X1_P0_P_PIN_CKB_DAT_13_N
K50	NX_X1_P0_P_PIN_CKB_DAT_11_P
K52	GND
K54	NX_X1_P0_P_PIN_CKA_CLK_N
K56	NX_X1_P0_P_PIN_CKB_DAT_06_P
K58	GND
K60	GND
K62	DM_DDR2_BI_DQ_25
K64	DM_DDR2_BI_DQS_12_N
K66	GND
K68	DM_DDR0_BI_DQS_03_N
K70	DM_DDR0_BI_DQ_31
K72	GND
K74	DM_DDR2_P0_P_PIN_CKE_1
K76	DM_DDR2_P0_P_PIN_CHIPID_1
K78	DM_DDR2_P0_P_PIN_CHIPID_0
K80	DM_DDR2_P0_P_PIN_ODT_3
K82	DM_DDR2_P0_P_PIN_ADDR_15
K84	DM_D-DR2_P0_P_PIN_BANK_ADR_1
K86	DM_DDR2_P0_P_PIN_CLK_0_N
K88	DM_DDR2_P0_P_PIN_CLK_1_P
L01	DM_DDR4_P0_P_PIN_ADDR_03
L03	GND
L05	DM_DDR4_P0_P_PIN_ADDR_08
L07	VDDR47_1P20

Pin Number	Signal Name
L09	DM_DDR6_P0_P_PIN_CS_B_1
L11	GND
L13	DM_DDR6_P0_P_PIN_CHIPID_0
L15	VDDR47_1P20
L17	GND
L19	DM_DDR6_BI_DQ_26
L21	DM_DDR6_BI_DQS_12_N
L23	GND
L25	DM_DDR4_BI_DQ_30
L27	DM_DDR4_BI_DQS_03_N
L29	GND
L31	GND
L33	GND
L35	NX_X1_PIN_P_P0_CKB_DAT_07_P
L37	NX_X1_PIN_P_P0_CKB_DAT_09_N
L39	GND
L41	NX_X1_PIN_P_P0_CKB_DAT_13_P
L43	NX_X1_PIN_P_P0_CKB_DAT_15_N
L45	GND
L47	NX_X1_P0_P_PIN_CKB_DAT_13_P
L49	GND
L51	NX_X1_P0_P_PIN_CKB_DAT_11_N
L53	NX_X1_P0_P_PIN_CKA_CLK_P
L55	GND
L57	NX_X1_P0_P_PIN_CKB_DAT_06_N
L59	GND
L61	GND
L63	DM_DDR2_BI_DQS_03_N
L65	DM_DDR2_BI_DQ_30
L67	GND
L69	DM_DDR0_BI_DQS_03_P
L71	DM_DDR0_BI_DQ_26
L73	GND
L75	VDDR03_1P20
L77	DM_DDR0_P0_P_PIN_CKE_0
L79	GND
L81	DM_DDR2_P0_P_PIN_ODT_1
L83	VDDR03_1P20
L85	DM_DDR2_PIN_P_P0_EVENT_B

Pin Number	Signal Name
L87	GND
L89	DM_DDR2_P0_P_PIN_ADDR_00
M02	DM_DDR4_P0_P_PIN_ADDR_02
M04	DM_DDR4_P0_P_PIN_ADDR_01
M06	DM_DDR4_P0_P_PIN_ADDR_12
M08	DM_DDR6_P0_P_PIN_ADDR_13
M10	DM_DDR6_P0_P_PIN_ODT_3
M12	DM_DDR6_P0_P_PIN_CHIPID_1
M14	DM_DDR4_P0_P_PIN_CKE_1
M16	GND
M18	DM_DDR6_BI_DQ_27
M20	DM_DDR6_BI_DQ_30
M22	GND
M24	DM_DDR4_BI_DQ_26
M26	DM_DDR4_BI_DQS_03_P
M28	GND
M30	GND
M32	NX_X1_PIN_P_P0_CKA_DAT_03_P
M34	NX_X1_PIN_P_P0_CKB_DAT_07_N
M36	GND
M38	NX_X1_PIN_P_P0_CKB_DAT_09_P
M40	NX_X1_PIN_P_P0_CKA_CLK_N
M42	GND
M44	NX_X1_PIN_P_P0_CKB_DAT_14_P
M46	GND
M48	NX_X1_P0_P_PIN_CKB_DAT_15_N
M50	NX_X1_P0_P_PIN_CKB_DAT_10_P
M52	GND
M54	NX_X1_P0_P_PIN_CKA_DAT_07_N
M56	NX_X1_P0_P_PIN_CKB_DAT_05_P
M58	GND
M60	GND
M62	GND
M64	DM_DDR2_BI_DQS_03_P
M66	DM_DDR2_BI_DQ_31
M68	GND
M70	DM_DDR0_BI_DQ_30
M72	DM_DDR0_BI_DQ_27
M74	GND

Pin Number	Signal Name
M76	DM_DDR0_P0_P_PIN_CKE_1
M78	DM_DDR0_P0_P_PIN_CKE_2
M80	DM_DDR0_PIN_P_P0_ERR_B
M82	DM_DDR2_P0_P_PIN_ADDR_17
M84	DM_DDR2_P0_P_PIN_CS_B_0
M86	DM_D-DR2_P0_P_PIN_BANK_ADR_0
M88	DM_DDR2_P0_P_PIN_ADDR_10
N01	VDDR47_1P20
N03	DM_DDR4_P0_P_PIN_CLK_1_N
N05	GND
N07	DM_D-DR4_P0_P_PIN_BANK_GRP_1
N09	VDDR47_1P20
N11	DM_DDR4_P0_P_PIN_CKE_2
N13	GND
N15	DM_DDR4_P0_P_PIN_CKE_0
N17	GND
N19	GND
N21	GND
N23	DM_DDR4_BI_DQ_27
N25	DM_DDR4_BI_DQ_31
N27	GND
N29	GND
N31	NX_X1_PIN_P_P0_CKA_DAT_03_N
N33	GND
N35	NX_X1_PIN_P_P0_CKB_DAT_06_P
N37	NX_X1_PIN_P_P0_CKB_DAT_08_N
N39	GND
N41	NX_X1_PIN_P_P0_CKA_CLK_P
N43	NX_X1_PIN_P_P0_CKB_DAT_14_N
N45	GND
N47	NX_X1_P0_P_PIN_CKB_DAT_15_P
N49	GND
N51	NX_X1_P0_P_PIN_CKB_DAT_10_N
N53	NX_X1_P0_P_PIN_CKA_DAT_07_P
N55	GND
N57	NX_X1_P0_P_PIN_CKB_DAT_05_N
N59	NX_X1_P0_P_PIN_CKA_DAT_03_P
N61	GND

Pin Number	Signal Name
N63	GND
N65	GND
N67	DM_DDR2_BI_DQ_26
N69	GND
N71	GND
N73	GND
N75	DM_DDR0_P0_P_PIN_RESET_B
N77	GND
N79	DM_D-DR0_P0_P_PIN_BANK_GRP_0
N81	VDDR03_1P20
N83	DM_DDR2_P0_P_PIN_CS_B_1
N85	GND
N87	DM_DDR2_P0_P_PIN_ADDR_16
N89	VDDR03_1P20
P02	DM_DDR4_P0_P_PIN_CLK_1_P
P04	DM_DDR4_P0_P_PIN_CLK_0_P
P06	DM_DDR4_P0_P_PIN_ADDR_04
P08	DM_D-DR4_P0_P_PIN_BANK_GRP_0
P10	DM_DDR4_P0_P_PIN_ACT_B
P12	DM_DDR4_P0_P_PIN_CKE_3
P14	GND
P16	DM_DDR4_P0_P_PIN_RESET_B
P18	GND
P20	GND
P22	GND
P24	GND
P26	GND
P28	GND
P30	GND
P32	NX_X1_PIN_P_P0_CKA_DAT_02_P
P34	NX_X1_PIN_P_P0_CKB_DAT_06_N
P36	GND
P38	NX_X1_PIN_P_P0_CKB_DAT_08_P
P40	NX_X1_PIN_P_P0_CKA_DAT_07_N
P42	GND
P44	NX_X1_PIN_P_P0_CKB_DAT_12_P
P46	GND
P48	NX_X1_P0_P_PIN_CKB_DAT_16_N

Pin Number	Signal Name
P50	NX_X1_P0_P_PIN_CKB_DAT_09_P
P52	GND
P54	NX_X1_P0_P_PIN_CKA_DAT_06_N
P56	NX_X1_P0_P_PIN_CKB_DAT_04_P
P58	GND
P60	NX_X1_P0_P_PIN_CKA_DAT_03_N
P62	GND
P64	GND
P66	DM_DDR2_BI_DQ_11
P68	DM_DDR2_BI_DQ_27
P70	GND
P72	DM_DDR0_BI_DQ_18
P74	GND
P76	DM_DDR0_P0_P_PIN_CKE_3
P78	DM_DDR0_P0_P_PIN_ACT_B
P80	DM_DDR0_P0_P_PIN_ADDR_12
P82	DM_DDR0_P0_P_PIN_ADDR_08
P84	DM_DDR2_P0_P_PIN_ADDR_13
P86	DM_DDR2_P0_P_PIN_ODT_0
P88	DM_DDR2_P0_P_PIN_CS_B_2
R01	DM_DDR4_PIN_P_P0_EVENT_B
R03	VDDR47_1P20
R05	DM_DDR4_P0_P_PIN_CLK_0_N
R07	GND
R09	DM_DDR4_P0_P_PIN_ADDR_05
R11	VDDR47_1P20
R13	GND
R15	GND
R17	GND
R19	DM_DDR4_BI_DQ_11
R21	DM_DDR4_BI_DQ_14
R23	GND
R25	DM_DDR6_BI_DQ_11
R27	DM_DDR6_BI_DQS_01_P
R29	GND
R31	NX_X1_PIN_P_P0_CKA_DAT_02_N
R33	GND
R35	NX_X1_PIN_P_P0_CKB_DAT_04_P
R37	NX_X1_PIN_P_P0_CKA_DAT_05_N

Pin Number	Signal Name
R39	GND
R41	NX_X1_PIN_P_P0_CKA_DAT_07_P
R43	NX_X1_PIN_P_P0_CKB_DAT_12_N
R45	GND
R47	NX_X1_P0_P_PIN_CKB_DAT_16_P
R49	GND
R51	NX_X1_P0_P_PIN_CKB_DAT_09_N
R53	NX_X1_P0_P_PIN_CKA_DAT_06_P
R55	GND
R57	NX_X1_P0_P_PIN_CKB_DAT_04_N
R59	NX_X1_P0_P_PIN_CKA_DAT_02_P
R61	GND
R63	GND
R65	DM_DDR2_BI_DQ_15
R67	DM_DDR2_BI_DQ_10
R69	GND
R71	DM_DDR0_BI_DQ_23
R73	DM_DDR0_BI_DQ_19
R75	VDDR03_1P20
R77	DM_D-DR0_P0_P_PIN_BANK_GRP_1
R79	VDDR03_1P20
R81	DM_DDR0_P0_P_PIN_ADDR_07
R83	GND
R85	DM_DDR2_P0_P_PIN_CS_B_3
R87	VDDR03_1P20
R89	DM_DDR2_P0_P_PIN_ADDR_14
T02	DM_D-DR4_P0_P_PIN_BANK_ADR_1
T04	DM_DDR4_P0_P_PIN_ADDR_00
T06	DM_DDR4_P0_P_PIN_ADDR_16
T08	DM_DDR4_P0_P_PIN_ADDR_10
T10	DM_DDR4_P0_P_PIN_PAR
T12	GND
T14	DM_DDR6_BI_DQ_59
T16	GND
T18	GND
T20	DM_DDR4_BI_DQ_10
T22	DM_DDR4_BI_DQS_01_P
T24	GND

Pin Number	Signal Name
T26	DM_DDR6_BI_DQ_10
T28	DM_DDR6_BI_DQS_01_N
T30	GND
T32	GND
T34	NX_X1_PIN_P_P0_CKB_DAT_04_N
T36	GND
T38	NX_X1_PIN_P_P0_CKA_DAT_05_P
T40	NX_X1_PIN_P_P0_CKA_DAT_06_N
T42	GND
T44	NX_X1_PIN_P_P0_CKB_DAT_11_P
T46	GND
T48	NX_X1_P0_P_PIN_CKB_DAT_12_N
T50	NX_X1_P0_P_PIN_CKB_CLK_P
T52	GND
T54	NX_X1_P0_P_PIN_CKA_DAT_05_N
T56	NX_X1_P0_P_PIN_CKA_DAT_01_P
T58	GND
T60	NX_X1_P0_P_PIN_CKA_DAT_02_N
T62	GND
T64	DM_DDR2_BI_DQS_01_P
T66	DM_DDR2_BI_DQ_14
T68	GND
T70	DM_DDR0_BI_DQS_02_P
T72	DM_DDR0_BI_DQ_22
T74	GND
T76	DM_DDR0_P0_P_PIN_ADDR_09
T78	DM_DDR0_P0_P_PIN_ADDR_11
T80	DM_DDR0_P0_P_PIN_ADDR_06
T82	DM_DDR0_P0_P_PIN_ADDR_05
T84	DM_DDR0_P0_P_PIN_ADDR_03
T86	DM_DDR0_P0_P_PIN_ADDR_02
T88	DM_DDR2_P0_P_PIN_ODT_2
U01	GND
U03	DM_D-DR4_P0_P_PIN_BANK_ADR_0
U05	VDDR47_1P20
U07	DM_DDR4_P0_P_PIN_CS_B_2
U09	GND
U11	GND
U13	DM_DDR6_BI_DQ_58

Pin Number	Signal Name
U15	DM_DDR6_BI_DQ_56
U17	DM_DDR6_BI_DQ_63
U19	GND
U21	DM_DDR4_BI_DQ_15
U23	DM_DDR4_BI_DQS_01_N
U25	GND
U27	DM_DDR6_BI_DQ_15
U29	DM_DDR6_BI_DQ_09
U31	GND
U33	GND
U35	NX_X1_PIN_P_P0_CKA_DAT_00_P
U37	NX_X1_PIN_P_P0_CKA_DAT_04_N
U39	GND
U41	NX_X1_PIN_P_P0_CKA_DAT_06_P
U43	NX_X1_PIN_P_P0_CKB_DAT_11_N
U45	GND
U47	NX_X1_P0_P_PIN_CKB_DAT_12_P
U49	GND
U51	NX_X1_P0_P_PIN_CKB_CLK_N
U53	NX_X1_P0_P_PIN_CKA_DAT_05_P
U55	GND
U57	NX_X1_P0_P_PIN_CKA_DAT_01_N
U59	GND
U61	GND
U63	DM_DDR2_BI_DQS_10_N
U65	DM_DDR2_BI_DQS_01_N
U67	GND
U69	DM_DDR0_BI_DQS_11_N
U71	DM_DDR0_BI_DQS_02_N
U73	GND
U75	GND
U77	DM_DDR0_P0_P_PIN_ADDR_04
U79	DM_DDR0_P0_P_PIN_ADDR_01
U81	VDDR03_1P20
U83	DM_DDR0_P0_P_PIN_CLK_0_N
U85	VDDR03_1P20
U87	DM_DDR0_P0_P_PIN_CLK_1_N
U89	GND
V02	DM_DDR4_P0_P_PIN_ADDR_14
V04	DM_DDR4_P0_P_PIN_CS_B_0
V06	DM_DDR4_P0_P_PIN_ODT_0
V08	DM_DDR4_P0_P_PIN_ODT_2
V10	GND
V12	DM_DDR6_BI_DQ_34
V14	DM_DDR6_BI_DQ_61
V16	DM_DDR6_BI_DQ_57
V18	DM_DDR6_BI_DQ_62
V20	GND
V22	DM_DDR4_BI_DQS_10_N
V24	DM_DDR4_BI_DQ_09
V26	GND
V28	DM_DDR6_BI_DQ_14
V30	DM_DDR6_BI_DQ_08
V32	GND
V34	NX_X1_PIN_P_P0_CKA_DAT_00_N
V36	GND
V38	NX_X1_PIN_P_P0_CKA_DAT_04_P
V40	NX_X1_PIN_P_P0_CKB_DAT_03_N
V42	GND
V44	NX_X1_PIN_P_P0_CKB_DAT_05_P
V46	GND
V48	NX_X1_P0_P_PIN_CKB_DAT_08_N
V50	NX_X1_P0_P_PIN_CKB_DAT_03_P
V52	GND
V54	NX_X1_P0_P_PIN_CKA_DAT_04_N
V56	NX_X1_P0_P_PIN_CKA_DAT_00_P
V58	GND
V60	GND
V62	DM_DDR2_BI_DQ_09
V64	DM_DDR2_BI_DQS_10_P
V66	GND
V68	DM_DDR0_BI_DQ_16
V70	DM_DDR0_BI_DQS_11_P
V72	GND
V74	DM_DDR0_BI_DQ_54
V76	GND
V78	GND
V80	DM_DDR0_P0_P_PIN_ADDR_14
V82	DM_DDR0_P0_P_PIN_ADDR_10
V84	DM_DDR0_P0_P_PIN_CLK_0_P
V86	DM_DDR0_P0_P_PIN_CLK_1_P
V88	DM_DDR0_P0_P_PIN_PAR
W01	DM_DDR4_P0_P_PIN_ADDR_15
W03	GND
W05	DM_DDR4_P0_P_PIN_ADDR_13
W07	VDDR47_1P20
W09	GND
W11	DM_DDR6_BI_DQ_38
W13	DM_DDR6_BI_DQ_60
W15	GND
W17	DM_DDR6_BI_DQS_16_N
W19	DM_DDR6_BI_DQS_07_P
W21	GND
W23	DM_DDR4_BI_DQS_10_P
W25	DM_DDR4_BI_DQ_08
W27	GND
W29	DM_DDR6_BI_DQS_10_N
W31	DM_DDR6_BI_DQ_12
W33	GND
W35	GND
W37	NX_X1_PIN_P_P0_CKB_DAT_01_N
W39	GND
W41	NX_X1_PIN_P_P0_CKB_DAT_03_P
W43	NX_X1_PIN_P_P0_CKB_DAT_05_N
W45	GND
W47	NX_X1_P0_P_PIN_CKB_DAT_08_P
W49	GND
W51	NX_X1_P0_P_PIN_CKB_DAT_03_N
W53	NX_X1_P0_P_PIN_CKA_DAT_04_P
W55	GND
W57	NX_X1_P0_P_PIN_CKA_DAT_00_N
W59	GND
W61	DM_DDR2_BI_DQ_13
W63	DM_DDR2_BI_DQ_08
W65	GND
W67	DM_DDR0_BI_DQ_20
W69	DM_DDR0_BI_DQ_17

Pin Number	Signal Name
W71	GND
W73	DM_DDR0_BI_DQ_55
W75	GND
W77	GND
W79	GND
W81	DM_DDR0_P0_P_PIN_ODT_2
W83	VDDR03_1P20
W85	DM_DDR0_PIN_P_P0_EVENT_B
W87	GND
W89	DM_D-DR0_P0_P_PIN_BANK_ADR_1
Y02	DM_DDR4_P0_P_PIN_CS_B_3
Y04	DM_DDR4_P0_P_PIN_CS_B_1
Y06	DM_DDR4_P0_P_PIN_CHIPID_2
Y08	GND
Y10	DM_DDR6_BI_DQS_13_N
Y12	DM_DDR6_BI_DQ_35
Y14	GND
Y16	GND
Y18	DM_DDR6_BI_DQS_16_P
Y20	DM_DDR6_BI_DQS_07_N
Y22	GND
Y24	DM_DDR4_BI_DQ_13
Y26	DM_DDR4_BI_DQ_12
Y28	GND
Y30	DM_DDR6_BI_DQS_10_P
Y32	DM_DDR6_BI_DQ_02
Y34	GND
Y36	GND
Y38	NX_X1_PIN_P_P0_CKB_DAT_01_P
Y40	NX_X1_PIN_P_P0_CKA_DAT_01_N
Y42	GND
Y44	NX_X1_PIN_P_P0_CKB_DAT_02_P
Y46	GND
Y48	NX_X1_P0_P_PIN_CKB_DAT_07_N
Y50	NX_X1_P0_P_PIN_CKB_DAT_01_P
Y52	GND
Y54	NX_X1_P0_P_PIN_CKB_DAT_02_N
Y56	GND
Y58	GND

Pin Number	Signal Name
Y60	DM_DDR2_BI_DQ_03
Y62	DM_DDR2_BI_DQ_12
Y64	GND
Y66	DM_DDR0_BI_DQ_11
Y68	DM_DDR0_BI_DQ_21
Y70	GND
Y72	GND
Y74	GND
Y76	DM_DDR3_BI_DQ_20
Y78	DM_DDR3_BI_DQ_21
Y80	GND
Y82	DM_DDR0_P0_P_PIN_CHIPID_1
Y84	DM_DDR0_P0_P_PIN_CS_B_2
Y86	DM_DDR0_P0_P_PIN_ADDR_00
Y88	DM_D-DR0_P0_P_PIN_BANK_ADR_0
AA01	VDDR47_1P20
AA03	DM_DDR4_P0_P_PIN_ADDR_17
AA05	GND
AA07	GND
AA09	DM_DDR6_BI_DQS_13_P
AA11	DM_DDR6_BI_DQ_39
AA13	GND
AA15	DM_DDR6_BI_DQ_48
AA17	GND
AA19	GND
AA21	GND
AA23	GND
AA25	DM_DDR4_BI_DQ_03
AA27	DM_DDR4_BI_DQ_02
AA29	GND
AA31	DM_DDR6_BI_DQ_13
AA33	DM_DDR6_BI_DQ_06
AA35	GND
AA37	GND
AA39	GND
AA41	NX_X1_PIN_P_P0_CKA_DAT_01_P
AA43	NX_X1_PIN_P_P0_CKB_DAT_02_N
AA45	GND
AA47	NX_X1_P0_P_PIN_CKB_DAT_07_P

Pin Number	Signal Name
AA49	GND
AA51	NX_X1_P0_P_PIN_CKB_DAT_01_N
AA53	NX_X1_P0_P_PIN_CKB_DAT_02_P
AA55	GND
AA57	GND
AA59	DM_DDR2_BI_DQ_07
AA61	DM_DDR2_BI_DQ_02
AA63	GND
AA65	DM_DDR0_BI_DQ_14
AA67	DM_DDR0_BI_DQ_10
AA69	GND
AA71	DM_DDR0_BI_DQS_07_P
AA73	GND
AA75	GND
AA77	DM_DDR3_BI_DQ_16
AA79	DM_DDR3_BI_DQS_11_P
AA81	GND
AA83	DM_DDR0_P0_P_PIN_CHIPID_0
AA85	VDDR03_1P20
AA87	DM_DDR0_P0_P_PIN_ADDR_16
AA89	VDDR03_1P20
AB02	DM_DDR4_P0_P_PIN_ODT_1
AB04	DM_DDR4_P0_P_PIN_CHIPID_0
AB06	GND
AB08	DM_DDR6_BI_DQ_32
AB10	DM_DDR6_BI_DQS_04_P
AB12	GND
AB14	DM_DDR6_BI_DQ_52
AB16	DM_DDR6_BI_DQ_49
AB18	GND
AB20	GND
AB22	DM_DDR4_BI_DQ_52
AB24	GND
AB26	DM_DDR4_BI_DQ_07
AB28	DM_DDR4_BI_DQ_06
AB30	GND
AB32	DM_DDR6_BI_DQ_03
AB34	DM_DDR6_BI_DQS_09_N
AB36	GND

Pin Number	Signal Name
AB38	GND
AB40	NX_X1_PIN_P_P0_CKB_DAT_00_N
AB42	GND
AB44	GND
AB46	GND
AB48	GND
AB50	NX_X1_P0_P_PIN_CKB_DAT_00_P
AB52	GND
AB54	GND
AB56	GND
AB58	DM_DDR2_BI_DQS_00_P
AB60	DM_DDR2_BI_DQ_06
AB62	GND
AB64	DM_DDR0_BI_DQS_01_P
AB66	DM_DDR0_BI_DQ_15
AB68	GND
AB70	DM_DDR0_BI_DQ_59
AB72	DM_DDR0_BI_DQS_07_N
AB74	DM_DDR0_BI_DQS_15_N
AB76	GND
AB78	DM_DDR3_BI_DQ_17
AB80	DM_DDR3_BI_DQS_11_N
AB82	GND
AB84	DM_DDR0_P0_P_PIN_CS_B_3
AB86	DM_DDR0_P0_P_PIN_ADDR_15
AB88	DM_DDR0_P0_P_PIN_CS_B_0
AC01	DM_DDR4_P0_P_PIN_ODT_3
AC03	VDDR47_1P20
AC05	GND
AC07	DM_DDR6_BI_DQ_36
AC09	DM_DDR6_BI_DQS_04_N
AC11	GND
AC13	GND
AC15	DM_DDR6_BI_DQ_53
AC17	DM_DDR6_BI_DQS_15_N
AC19	GND
AC21	DM_DDR4_BI_DQ_53
AC23	DM_DDR4_BI_DQ_48
AC25	GND

Pin Number	Signal Name
AC27	DM_DDR4_BI_DQS_00_P
AC29	DM_DDR4_BI_DQS_09_N
AC31	GND
AC33	DM_DDR6_BI_DQ_07
AC35	DM_DDR6_BI_DQS_09_P
AC37	GND
AC39	GND
AC41	NX_X1_PIN_P_P0_CKB_DAT_00_P
AC43	GND
AC45	GND
AC47	GND
AC49	GND
AC51	NX_X1_P0_P_PIN_CKB_DAT_00_N
AC53	GND
AC55	GND
AC57	DM_DDR2_BI_DQS_09_N
AC59	DM_DDR2_BI_DQS_00_N
AC61	GND
AC63	DM_DDR0_BI_DQS_10_N
AC65	DM_DDR0_BI_DQS_01_N
AC67	GND
AC69	DM_DDR0_BI_DQ_63
AC71	DM_DDR0_BI_DQ_58
AC73	GND
AC75	DM_DDR0_BI_DQS_15_P
AC77	GND
AC79	DM_DDR3_BI_DQS_02_N
AC81	DM_DDR3_BI_DQ_22
AC83	GND
AC85	DM_DDR0_P0_P_PIN_CS_B_1
AC87	VDDR03_1P20
AC89	DM_DDR0_P0_P_PIN_ODT_0
AD02	DM_DDR4_P0_P_PIN_CHIPID_1
AD04	GND
AD06	DM_DDR6_BI_DQ_44
AD08	DM_DDR6_BI_DQ_33
AD10	GND
AD12	DM_DDR4_BI_DQ_36
AD14	GND

Pin Number	Signal Name
AD16	DM_DDR6_BI_DQS_15_P
AD18	DM_DDR6_BI_DQS_06_P
AD20	GND
AD22	DM_DDR4_BI_DQ_49
AD24	DM_DDR4_BI_DQS_15_P
AD26	GND
AD28	DM_DDR4_BI_DQS_00_N
AD30	DM_DDR4_BI_DQS_09_P
AD32	GND
AD34	DM_DDR6_BI_DQS_00_P
AD36	DM_DDR6_BI_DQ_00
AD38	GND
AD40	GND
AD42	GND
AD44	GND
AD46	GND
AD48	TS_X1RXA_P0_P_PIN_ATST
AD50	GND
AD52	GND
AD54	GND
AD56	DM_DDR2_BI_DQ_01
AD58	DM_DDR2_BI_DQS_09_P
AD60	GND
AD62	DM_DDR0_BI_DQ_09
AD64	DM_DDR0_BI_DQS_10_P
AD66	GND
AD68	GND
AD70	DM_DDR0_BI_DQ_62
AD72	GND
AD74	DM_DDR0_BI_DQS_06_P
AD76	DM_DDR0_BI_DQ_48
AD78	GND
AD80	DM_DDR3_BI_DQS_02_P
AD82	DM_DDR3_BI_DQ_23
AD84	GND
AD86	DM_DDR0_P0_P_PIN_ADDR_17
AD88	DM_DDR0_P0_P_PIN_ADDR_13
AE01	GND
AE03	GND

Pin Number	Signal Name
AE05	DM_DDR6_BI_DQ_45
AE07	DM_DDR6_BI_DQ_37
AE09	GND
AE11	DM_DDR4_BI_DQ_37
AE13	GND
AE15	GND
AE17	DM_DDR6_BI_DQS_06_N
AE19	DM_DDR6_BI_DQ_55
AE21	GND
AE23	DM_DDR4_BI_DQS_15_N
AE25	DM_DDR4_BI_DQS_06_N
AE27	GND
AE29	DM_DDR4_BI_DQ_01
AE31	DM_DDR4_BI_DQ_00
AE33	GND
AE35	DM_DDR6_BI_DQS_00_N
AE37	DM_DDR6_BI_DQ_05
AE39	GND
AE41	GND
AE43	TS_VIO0_P0_P_PIN_VSENSE
AE45	GND
AE47	TS_X1RXA_P0_P_PIN_HFC_N
AE49	PV_X1TX_P0_P_PIN_TERMREF_P
AE51	GND
AE53	TS_CLK_P0_P_PIN_PROBE1_N
AE55	DM_DDR2_BI_DQ_05
AE57	DM_DDR2_BI_DQ_00
AE59	GND
AE61	DM_DDR0_BI_DQ_12
AE63	DM_DDR0_BI_DQ_08
AE65	GND
AE67	DM_DDR2_BI_DQ_44
AE69	GND
AE71	GND
AE73	GND
AE75	DM_DDR0_BI_DQS_06_N
AE77	DM_DDR0_BI_DQ_52
AE79	GND
AE81	DM_DDR3_BI_DQ_18

Pin Number	Signal Name
AE83	GND
AE85	GND
AE87	DM_DDR0_P0_P_PIN_ODT_1
AE89	VDDR03_1P20
AF02	GND
AF04	DM_DDR6_BI_DQ_41
AF06	DM_DDR6_BI_DQ_43
AF08	GND
AF10	DM_DDR4_BI_DQ_32
AF12	DM_DDR4_BI_DQS_13_P
AF14	GND
AF16	GND
AF18	DM_DDR6_BI_DQ_54
AF20	DM_DDR6_BI_DQ_51
AF22	GND
AF24	DM_DDR4_BI_DQS_06_P
AF26	DM_DDR4_BI_DQ_54
AF28	PV_PRV_PIN_P_P0_BSENSE2
AF30	DM_DDR4_BI_DQ_05
AF32	DM_DDR4_BI_DQ_04
AF34	GND
AF36	DM_DDR6_BI_DQ_01
AF38	DM_DDR6_BI_DQ_04
AF40	GND
AF42	TS_VIO0_P0_P_PIN_GSENSE
AF44	GND
AF46	GND
AF48	TS_X1RXA_P0_P_PIN_HFC_P
AF50	PV_X1TX_P0_P_PIN_TERMREF_N
AF52	TS_CLK_P0_P_PIN_PROBE1_P
AF54	GND
AF56	DM_DDR2_BI_DQ_04
AF58	GND
AF60	DM_DDR0_BI_DQ_13
AF62	GND
AF64	GND
AF66	DM_DDR2_BI_DQ_40
AF68	DM_DDR2_BI_DQ_45
AF70	GND

Pin Number	Signal Name
AF72	DM_DDR0_BI_DQ_51
AF74	GND
AF76	DM_DDR0_BI_DQ_49
AF78	DM_DDR0_BI_DQ_39
AF80	GND
AF82	DM_DDR3_BI_DQ_19
AF84	DM_DDR2_BI_DQ_34
AF86	GND
AF88	DM_DDR0_P0_P_PIN_ODT_3
AG01	GND
AG03	DM_DDR6_BI_DQ_40
AG05	DM_DDR6_BI_DQ_42
AG07	GND
AG09	DM_DDR4_BI_DQ_33
AG11	DM_DDR4_BI_DQS_13_N
AG13	GND
AG15	GND
AG17	GND
AG19	DM_DDR6_BI_DQ_50
AG21	GND
AG23	GND
AG25	DM_DDR4_BI_DQ_55
AG27	GND
AG29	VIO_1P00
AG31	VIO_1P00
AG33	VIO_1P00
AG35	VIO_1P00
AG37	VIO_1P00
AG39	VIO_1P00
AG41	VIO_1P00
AG43	VIO_1P00
AG45	VIO_1P00
AG47	VIO_1P00
AG49	VIO_1P00
AG51	VIO_1P00
AG53	VIO_1P00
AG55	VIO_1P00
AG57	VIO_1P00
AG59	VIO_1P00

Pin Number	Signal Name
AG61	VIO_1P00
AG63	GND
AG65	DM_DDR2_BI_DQS_14_P
AG67	DM_DDR2_BI_DQ_41
AG69	GND
AG71	DM_DDR0_BI_DQ_61
AG73	DM_DDR0_BI_DQ_50
AG75	GND
AG77	DM_DDR0_BI_DQ_53
AG79	DM_DDR0_BI_DQ_38
AG81	GND
AG83	GND
AG85	DM_DDR2_BI_DQ_38
AG87	GND
AG89	DM_DDR0_P0_P_PIN_CHIPID_2
AH02	DM_DDR6_BI_DQS_14_P
AH04	DM_DDR6_BI_DQS_05_N
AH06	GND
AH08	DM_DDR4_BI_DQS_04_N
AH10	DM_DDR4_BI_DQ_34
AH12	GND
AH14	DM_DDR7_BI_DQ_14
AH16	DM_DDR7_BI_DQS_01_N
AH18	GND
AH20	GND
AH22	DM_DDR4_BI_DQ_61
AH24	GND
AH26	DM_DDR4_BI_DQ_50
AH28	GND
AH30	VDN_0P70
AH32	GND
AH34	VDN_0P70
AH36	GND
AH38	VDN_0P70
AH40	GND
AH42	GND
AH44	VDN_0P70
AH46	GND
AH48	VDN_0P70

Pin Number	Signal Name
AH50	GND
AH52	VDN_0P70
AH54	GND
AH56	VDN_0P70
AH58	GND
AH60	VDN_0P70
AH62	PV_PRV_PIN_P_P0_BSENSE0
AH64	DM_DDR2_BI_DQS_05_N
AH66	DM_DDR2_BI_DQS_14_N
AH68	GND
AH70	DM_DDR0_BI_DQ_57
AH72	DM_DDR0_BI_DQ_60
AH74	GND
AH76	GND
AH78	DM_DDR0_BI_DQ_35
AH80	DM_DDR0_BI_DQS_13_N
AH82	GND
AH84	DM_DDR2_BI_DQ_35
AH86	DM_DDR2_BI_DQ_36
AH88	GND
AJ01	DM_DDR6_BI_DQS_14_N
AJ03	DM_DDR6_BI_DQS_05_P
AJ05	GND
AJ07	DM_DDR4_BI_DQS_04_P
AJ09	DM_DDR4_BI_DQ_35
AJ11	GND
AJ13	DM_DDR7_BI_DQ_10
AJ15	DM_DDR7_BI_DQS_01_P
AJ17	DM_DDR7_BI_DQS_10_N
AJ19	GND
AJ21	DM_DDR4_BI_DQ_60
AJ23	DM_DDR4_BI_DQ_57
AJ25	GND
AJ27	DM_DDR4_BI_DQ_51
AJ29	VDDR47_1P20
AJ31	GND
AJ33	VDD_0P80
AJ35	VDD_0P80
AJ37	VCS_0P96

Pin Number	Signal Name
AJ39	VDD_0P80
AJ41	VDN_0P70
AJ43	VDD_0P80
AJ45	VDD_0P80
AJ47	VDD_0P80
AJ49	VCS_0P96
AJ51	VDD_0P80
AJ53	VCS_0P96
AJ55	VDD_0P80
AJ57	VDD_0P80
AJ59	GND
AJ61	VDDR03_1P20
AJ63	DM_DDR2_BI_DQ_46
AJ65	DM_DDR2_BI_DQS_05_P
AJ67	GND
AJ69	DM_DDR0_BI_DQS_16_N
AJ71	DM_DDR0_BI_DQ_56
AJ73	GND
AJ75	TS_DDR0123_P0_P_PIN_ATST
AJ77	GND
AJ79	DM_DDR0_BI_DQ_34
AJ81	DM_DDR0_BI_DQS_13_P
AJ83	GND
AJ85	DM_DDR2_BI_DQ_39
AJ87	DM_DDR2_BI_DQ_37
AJ89	GND
AK02	DM_DDR6_BI_DQ_46
AK04	GND
AK06	DM_DDR4_BI_DQ_38
AK08	DM_DDR4_BI_DQ_43
AK10	GND
AK12	DM_DDR7_BI_DQ_20
AK14	DM_DDR7_BI_DQ_11
AK16	DM_DDR7_BI_DQ_15
AK18	DM_DDR7_BI_DQS_10_P
AK20	GND
AK22	DM_DDR4_BI_DQ_56
AK24	DM_DDR4_BI_DQS_16_N
AK26	GND

Pin Number	Signal Name
AK28	GND
AK30	VDN_0P70
AK32	VDD_0P80
AK34	GND
AK36	GND
AK38	GND
AK40	GND
AK42	GND
AK44	GND
AK46	GND
AK48	GND
AK50	GND
AK52	GND
AK54	TS_EX00C0_P0_P_PIN_VSENSE
AK56	GND
AK58	VDD_0P80
AK60	VDN_0P70
AK62	GND
AK64	DM_DDR2_BI_DQ_47
AK66	GND
AK68	GND
AK70	DM_DDR0_BI_DQS_16_P
AK72	GND
AK74	DM_DDR3_BI_DQ_03
AK76	GND
AK78	GND
AK80	DM_DDR0_BI_DQS_04_P
AK82	DM_DDR0_BI_DQ_37
AK84	GND
AK86	DM_DDR2_BI_DQS_13_P
AK88	DM_DDR2_BI_DQ_32
AL01	DM_DDR6_BI_DQ_47
AL03	GND
AL05	DM_DDR4_BI_DQ_39
AL07	DM_DDR4_BI_DQ_42
AL09	GND
AL11	DM_DDR7_BI_DQ_16
AL13	DM_DDR7_BI_DQ_21
AL15	GND

Pin Number	Signal Name
AL17	DM_DDR7_BI_DQ_09
AL19	DM_DDR7_BI_DQ_08
AL21	GND
AL23	DM_DDR4_BI_DQS_16_P
AL25	DM_DDR4_BI_DQS_07_P
AL27	GND
AL29	VDDR47_1P20
AL31	GND
AL33	VDD_0P80
AL35	VDD_0P80
AL37	VCS_0P96
AL39	VDD_0P80
AL41	VDN_0P70
AL43	VDD_0P80
AL45	VDD_0P80
AL47	VDD_0P80
AL49	VCS_0P96
AL51	VDD_0P80
AL53	TS_EX00C0_P0_P_PIN_GSENSE
AL55	VDD_0P80
AL57	VDD_0P80
AL59	GND
AL61	VDDR03_1P20
AL63	DM_DDR2_BI_DQ_42
AL65	GND
AL67	DM_DDR2_BI_DQ_52
AL69	GND
AL71	GND
AL73	DM_DDR3_BI_DQ_02
AL75	DM_DDR3_BI_DQ_07
AL77	GND
AL79	GND
AL81	DM_DDR0_BI_DQS_04_N
AL83	DM_DDR0_BI_DQ_36
AL85	GND
AL87	DM_DDR2_BI_DQS_13_N
AL89	DM_DDR2_BI_DQ_33
AM02	GND
AM04	DM_DDR4_BI_DQ_41

Pin Number	Signal Name
AM06	DM_DDR4_BI_DQ_47
AM08	GND
AM10	DM_DDR7_BI_DQS_11_P
AM12	DM_DDR7_BI_DQ_17
AM14	GND
AM16	GND
AM18	DM_DDR7_BI_DQ_13
AM20	DM_DDR7_BI_DQ_12
AM22	GND
AM24	DM_DDR4_BI_DQS_07_N
AM26	DM_DDR4_BI_DQ_63
AM28	GND
AM30	GND
AM32	VDD_0P80
AM34	GND
AM36	GND
AM38	GND
AM40	GND
AM42	GND
AM44	GND
AM46	GND
AM48	GND
AM50	VDN_0P70
AM52	GND
AM54	GND
AM56	GND
AM58	VDD_0P80
AM60	GND
AM62	DM_DDR2_BI_DQ_43
AM64	GND
AM66	DM_DDR2_BI_DQ_48
AM68	DM_DDR2_BI_DQ_53
AM70	GND
AM72	DM_DDR3_BI_DQS_00_P
AM74	DM_DDR3_BI_DQ_06
AM76	GND
AM78	GND
AM80	GND
AM82	DM_DDR0_BI_DQ_33

Pin Number	Signal Name
AM84	DM_DDR0_BI_DQ_45
AM86	GND
AM88	DM_DDR2_BI_DQS_04_N
AN01	GND
AN03	DM_DDR4_BI_DQ_40
AN05	DM_DDR4_BI_DQ_46
AN07	GND
AN09	DM_DDR7_BI_DQS_02_N
AN11	DM_DDR7_BI_DQS_11_N
AN13	GND
AN15	GND
AN17	GND
AN19	DM_DDR7_BI_DQ_03
AN21	DM_DDR7_BI_DQ_02
AN23	GND
AN25	DM_DDR4_BI_DQ_62
AN27	DM_DDR4_BI_DQ_59
AN29	VDDR47_1P20
AN31	GND
AN33	VDD_0P80
AN35	VDD_0P80
AN37	VCS_0P96
AN39	VDD_0P80
AN41	VDN_0P70
AN43	VDD_0P80
AN45	VDD_0P80
AN47	VDD_0P80
AN49	VCS_0P96
AN51	VDD_0P80
AN53	VCS_0P96
AN55	VDD_0P80
AN57	VDD_0P80
AN59	GND
AN61	VDDR03_1P20
AN63	GND
AN65	DM_DDR2_BI_DQS_15_P
AN67	DM_DDR2_BI_DQ_49
AN69	GND
AN71	DM_DDR3_BI_DQS_00_N

Pin Number	Signal Name
AN73	DM_DDR3_BI_DQS_09_N
AN75	GND
AN77	DM_DDR3_BI_DQ_12
AN79	DM_DDR3_BI_DQ_08
AN81	GND
AN83	DM_DDR0_BI_DQ_32
AN85	DM_DDR0_BI_DQ_44
AN87	GND
AN89	DM_DDR2_BI_DQS_04_P
AP02	DM_DDR4_BI_DQ_44
AP04	DM_DDR4_BI_DQS_05_P
AP06	GND
AP08	DM_DDR7_BI_DQ_22
AP10	DM_DDR7_BI_DQS_02_P
AP12	GND
AP14	DM_DDR5_BI_DQ_10
AP16	DM_DDR5_BI_DQS_01_P
AP18	GND
AP20	DM_DDR7_BI_DQ_07
AP22	DM_DDR7_BI_DQ_06
AP24	GND
AP26	DM_DDR4_BI_DQ_58
AP28	GND
AP30	VDN_0P70
AP32	VDD_0P80
AP34	GND
AP36	GND
AP38	GND
AP40	GND
AP42	GND
AP44	GND
AP46	GND
AP48	TS_CACHE0001_P0_P_PIN_VDD_V-SENSE
AP50	GND
AP52	GND
AP54	TS_EX00C1_P0_P_PIN_GSENSE
AP56	GND
AP58	VDD_0P80
AP60	VDN_0P70

Pin Number	Signal Name
AP62	GND
AP64	DM_DDR2_BI_DQS_06_N
AP66	DM_DDR2_BI_DQS_15_N
AP68	GND
AP70	DM_DDR3_BI_DQ_01
AP72	DM_DDR3_BI_DQS_09_P
AP74	GND
AP76	GND
AP78	DM_DDR3_BI_DQ_13
AP80	DM_DDR3_BI_DQ_09
AP82	GND
AP84	DM_DDR0_BI_DQ_43
AP86	DM_DDR0_BI_DQ_41
AP88	GND
AR01	DM_DDR4_BI_DQ_45
AR03	DM_DDR4_BI_DQS_05_N
AR05	GND
AR07	DM_DDR7_BI_DQ_18
AR09	DM_DDR7_BI_DQ_23
AR11	GND
AR13	DM_DDR5_BI_DQ_20
AR15	DM_DDR5_BI_DQ_11
AR17	DM_DDR5_BI_DQS_01_N
AR19	GND
AR21	DM_DDR7_BI_DQS_00_P
AR23	DM_DDR7_BI_DQS_09_N
AR25	GND
AR27	GND
AR29	VDDR47_1P20
AR31	GND
AR33	VDD_0P80
AR35	VDD_0P80
AR37	VCS_0P96
AR39	VDD_0P80
AR41	VDN_0P70
AR43	VDD_0P80
AR45	VDD_0P80
AR47	VDD_0P80
AR49	TS_EQ0_P0_P_PIN_GSENSE

Pin Number	Signal Name
AR51	VDD_0P80
AR53	TS_EX00C1_P0_P_PIN_VSENSE
AR55	VDD_0P80
AR57	VDD_0P80
AR59	GND
AR61	VDDR03_1P20
AR63	DM_DDR2_BI_DQ_54
AR65	DM_DDR2_BI_DQS_06_P
AR67	GND
AR69	DM_DDR3_BI_DQ_00
AR71	DM_DDR3_BI_DQ_05
AR73	GND
AR75	DM_DDR1_BI_DQ_08
AR77	GND
AR79	DM_DDR3_BI_DQS_10_P
AR81	DM_DDR3_BI_DQS_01_N
AR83	GND
AR85	DM_DDR0_BI_DQS_05_N
AR87	DM_DDR0_BI_DQ_40
AR89	GND
AT02	DM_DDR4_BI_DQS_14_P
AT04	GND
AT06	DM_DDR7_BI_DQ_28
AT08	DM_DDR7_BI_DQ_19
AT10	GND
AT12	DM_DDR5_BI_DQ_21
AT14	GND
AT16	DM_DDR5_BI_DQ_15
AT18	DM_DDR5_BI_DQS_10_N
AT20	GND
AT22	DM_DDR7_BI_DQS_00_N
AT24	DM_DDR7_BI_DQS_09_P
AT26	GND
AT28	GND
AT30	GND
AT32	VDD_0P80
AT34	GND
AT36	GND
AT38	GND

Pin Number	Signal Name
AT40	GND
AT42	GND
AT44	GND
AT46	GND
AT48	TS_EQ0_P0_P_PIN_VDDIN_ VSENSE
AT50	VDN_0P70
AT52	GND
AT54	GND
AT56	GND
AT58	VDD_0P80
AT60	GND
AT62	GND
AT64	DM_DDR2_BI_DQ_55
AT66	GND
AT68	PV_DDR0123_P0_P_PIN_ TERMREF_P
AT70	DM_DDR3_BI_DQ_04
AT72	GND
AT74	DM_DDR1_BI_DQ_12
AT76	DM_DDR1_BI_DQ_09
AT78	GND
AT80	DM_DDR3_BI_DQS_10_N
AT82	DM_DDR3_BI_DQS_01_P
AT84	GND
AT86	DM_DDR0_BI_DQS_05_P
AT88	DM_DDR0_BI_DQS_14_P
AU01	DM_DDR4_BI_DQS_14_N
AU03	GND
AU05	DM_DDR7_BI_DQ_24
AU07	DM_DDR7_BI_DQ_29
AU09	GND
AU11	DM_DDR5_BI_DQ_17
AU13	DM_DDR5_BI_DQ_16
AU15	GND
AU17	DM_DDR5_BI_DQ_14
AU19	DM_DDR5_BI_DQS_10_P
AU21	GND
AU23	DM_DDR7_BI_DQ_01
AU25	DM_DDR7_BI_DQ_05

Pin Number	Signal Name
AU27	PV_DDR4567_P0_P_PIN_ TERMREF_N
AU29	VDDR47_1P20
AU31	GND
AU33	VDD_0P80
AU35	VDD_0P80
AU37	VCS_0P96
AU39	VDD_0P80
AU41	VDN_0P70
AU43	VDD_0P80
AU45	VDD_0P80
AU47	VDD_0P80
AU49	VCS_0P96
AU51	VDD_0P80
AU53	VCS_0P96
AU55	VDD_0P80
AU57	VDD_0P80
AU59	GND
AU61	VDDR03_1P20
AU63	DM_DDR2_BI_DQ_50
AU65	GND
AU67	DM_DDR2_BI_DQ_60
AU69	PV_DDR0123_P0_P_PIN_ TERMREF_N
AU71	GND
AU73	DM_DDR1_BI_DQS_01_N
AU75	DM_DDR1_BI_DQ_15
AU77	DM_DDR1_BI_DQ_00
AU79	GND
AU81	DM_DDR3_BI_DQ_14
AU83	DM_DDR3_BI_DQ_15
AU85	GND
AU87	DM_DDR0_BI_DQ_42
AU89	DM_DDR0_BI_DQS_14_N
AV02	GND
AV04	DM_DDR7_BI_DQS_12_P
AV06	DM_DDR7_BI_DQ_25
AV08	GND
AV10	DM_DDR5_BI_DQS_02_N
AV12	DM_DDR5_BI_DQS_11_P

Pin Number	Signal Name
AV14	GND
AV16	GND
AV18	DM_DDR5_BI_DQ_09
AV20	DM_DDR5_BI_DQ_13
AV22	GND
AV24	DM_DDR7_BI_DQ_00
AV26	GND
AV28	GND
AV30	VDN_0P70
AV32	VDD_0P80
AV34	GND
AV36	GND
AV38	GND
AV40	GND
AV42	GND
AV44	GND
AV46	GND
AV48	GND
AV50	GND
AV52	GND
AV54	GND
AV56	GND
AV58	VDD_0P80
AV60	VDN_0P70
AV62	DM_DDR2_BI_DQ_51
AV64	GND
AV66	DM_DDR2_BI_DQ_56
AV68	DM_DDR2_BI_DQ_61
AV70	GND
AV72	DM_DDR1_BI_DQS_10_P
AV74	DM_DDR1_BI_DQS_01_P
AV76	GND
AV78	DM_DDR1_BI_DQ_03
AV80	GND
AV82	DM_DDR3_BI_DQ_10
AV84	DM_DDR3_BI_DQ_11
AV86	GND
AV88	DM_DDR0_BI_DQ_46
AW01	GND

Pin Number	Signal Name
AW03	DM_DDR7_BI_DQS_03_N
AW05	DM_DDR7_BI_DQS_12_N
AW07	GND
AW09	DM_DDR5_BI_DQS_02_P
AW11	DM_DDR5_BI_DQS_11_N
AW13	GND
AW15	DM_DDR7_BI_DQ_68
AW17	GND
AW19	DM_DDR5_BI_DQ_08
AW21	DM_DDR5_BI_DQ_12
AW23	GND
AW25	DM_DDR7_BI_DQ_04
AW27	PV_DDR4567_P0_P_PIN_TERM-REF_P
AW29	VDDR47_1P20
AW31	GND
AW33	VDD_0P80
AW35	VDD_0P80
AW37	TS_VDN_P0_P_PIN_GSENSE
AW39	VDD_0P80
AW41	VDN_0P70
AW43	VDD_0P80
AW45	VDD_0P80
AW47	VDD_0P80
AW49	TS_EX05_P0_P_PIN_TDIODE_C
AW51	VDD_0P80
AW53	TS_EX01C0_P0_P_PIN_VSENSE
AW55	VDD_0P80
AW57	VDD_0P80
AW59	GND
AW61	VDDR03_1P20
AW63	GND
AW65	DM_DDR2_BI_DQS_16_P
AW67	DM_DDR2_BI_DQ_57
AW69	GND
AW71	DM_DDR1_BI_DQ_10
AW73	DM_DDR1_BI_DQS_10_N
AW75	GND
AW77	DM_DDR1_BI_DQ_04
AW79	DM_DDR1_BI_DQ_06

Pin Number	Signal Name
AW81	GND
AW83	DM_DDR3_BI_DQ_28
AW85	DM_DDR3_BI_DQ_29
AW87	GND
AW89	DM_DDR0_BI_DQ_47
AY02	DM_DDR7_BI_DQ_30
AY04	DM_DDR7_BI_DQS_03_P
AY06	GND
AY08	DM_DDR5_BI_DQ_23
AY10	DM_DDR5_BI_DQ_22
AY12	GND
AY14	GND
AY16	DM_DDR7_BI_DQ_69
AY18	GND
AY20	DM_DDR5_BI_DQ_03
AY22	DM_DDR5_BI_DQ_07
AY24	GND
AY26	TS_VDDR6_P0_P_PIN_GSENSE
AY28	GND
AY30	GND
AY32	VDD_0P80
AY34	GND
AY36	TS_VCS_P0_P_PIN_VSENSE
AY38	TS_VDN_P0_P_PIN_VSENSE
AY40	GND
AY42	GND
AY44	GND
AY46	GND
AY48	TS_EX05_P0_P_PIN_TDIODE_A
AY50	VDN_0P70
AY52	GND
AY54	TS_EX01C0_P0_P_PIN_GSENSE
AY56	GND
AY58	VDD_0P80
AY60	GND
AY62	GND
AY64	DM_DDR2_BI_DQS_07_N
AY66	DM_DDR2_BI_DQS_16_N
AY68	GND

Pin Number	Signal Name
AY70	DM_DDR1_BI_DQ_14
AY72	DM_DDR1_BI_DQ_11
AY74	GND
AY76	GND
AY78	DM_DDR1_BI_DQS_09_P
AY80	DM_DDR1_BI_DQS_00_N
AY82	GND
AY84	DM_DDR3_BI_DQ_24
AY86	DM_DDR3_BI_DQ_25
AY88	GND
BA01	DM_DDR7_BI_DQ_26
BA03	DM_DDR7_BI_DQ_31
BA05	GND
BA07	DM_DDR5_BI_DQ_19
BA09	DM_DDR5_BI_DQ_18
BA11	GND
BA13	DM_DDR5_BI_DQ_31
BA15	GND
BA17	DM_DDR7_BI_DQ_64
BA19	GND
BA21	DM_DDR5_BI_DQ_02
BA23	DM_DDR5_BI_DQ_06
BA25	GND
BA27	TS_DDR4567_P0_P_PIN_ATST
BA29	VDDR47_1P20
BA31	GND
BA33	VDD_0P80
BA35	VDD_0P80
BA37	VCS_0P96
BA39	VDD_0P80
BA41	VDN_0P70
BA43	VDD_0P80
BA45	VDD_0P80
BA47	VDD_0P80
BA49	VCS_0P96
BA51	VDD_0P80
BA53	VCS_0P96
BA55	VDD_0P80
BA57	VDD_0P80

Pin Number	Signal Name
BA59	GND
BA61	VDDR03_1P20
BA63	DM_DDR2_BI_DQ_62
BA65	DM_DDR2_BI_DQS_07_P
BA67	GND
BA69	GND
BA71	DM_DDR1_BI_DQ_13
BA73	GND
BA75	GND
BA77	GND
BA79	DM_DDR1_BI_DQS_09_N
BA81	DM_DDR1_BI_DQS_00_P
BA83	GND
BA85	DM_DDR3_BI_DQS_12_P
BA87	DM_DDR3_BI_DQS_03_N
BA89	GND
BB02	DM_DDR7_BI_DQ_27
BB04	GND
BB06	DM_DDR5_BI_DQ_29
BB08	DM_DDR5_BI_DQ_28
BB10	GND
BB12	DM_DDR5_BI_DQ_30
BB14	GND
BB16	DM_DDR7_BI_DQ_65
BB18	DM_DDR7_BI_DQS_17_P
BB20	GND
BB22	DM_DDR5_BI_DQS_00_P
BB24	DM_DDR5_BI_DQS_09_N
BB26	TS_VDDR6_P0_P_PIN_VSENSE
BB28	GND
BB30	VDN_0P70
BB32	VDD_0P80
BB34	GND
BB36	GND
BB38	GND
BB40	VCS_CHIP_GSENSE
BB42	GND
BB44	GND
BB46	GND

Pin Number	Signal Name
BB48	GND
BB50	VDD_CHIP_GSENSE
BB52	GND
BB54	GND
BB56	TS_VDDR0_P0_P_PIN_GSENSE
BB58	VDD_0P80
BB60	VDN_0P70
BB62	DM_DDR2_BI_DQ_58
BB64	DM_DDR2_BI_DQ_63
BB66	GND
BB68	DM_DDR3_BI_DQ_69
BB70	GND
BB72	GND
BB74	DM_DDR1_BI_DQ_17
BB76	DM_DDR1_BI_DQ_05
BB78	GND
BB80	DM_DDR1_BI_DQ_01
BB82	DM_DDR1_BI_DQ_02
BB84	GND
BB86	DM_DDR3_BI_DQS_12_N
BB88	DM_DDR3_BI_DQS_03_P
BC01	GND
BC03	GND
BC05	DM_DDR5_BI_DQS_12_P
BC07	DM_DDR5_BI_DQ_24
BC09	GND
BC11	DM_DDR5_BI_DQS_03_N
BC13	DM_DDR5_BI_DQ_27
BC15	GND
BC17	DM_DDR7_BI_DQS_17_N
BC19	DM_DDR7_BI_DQS_08_N
BC21	GND
BC23	DM_DDR5_BI_DQS_00_N
BC25	DM_DDR5_BI_DQS_09_P
BC27	GND
BC29	GND
BC31	VDD_0P80
BC33	VDD_0P80
BC35	VDD_0P80

Pin Number	Signal Name
BC37	VCS_0P96
BC39	VDD_0P80
BC41	VCS_CHIP_VSENSE
BC43	VDN_0P70
BC45	TS_EFUSE_PIN_P_P0_FSOURCE
BC47	VDN_0P70
BC49	VDN_0P70
BC51	VDD_CHIP_VSENSE
BC53	VDN_0P70
BC55	VDN_0P70
BC57	TS_VDDR0_P0_P_PIN_VSENSE
BC59	VDN_0P70
BC61	VDDR03_1P20
BC63	DM_DDR2_BI_DQ_59
BC65	GND
BC67	DM_DDR3_BI_DQ_65
BC69	DM_DDR3_BI_DQ_68
BC71	GND
BC73	DM_DDR1_BI_DQ_18
BC75	GND
BC77	DM_DDR1_BI_DQ_07
BC79	GND
BC81	DM_DDR1_BI_DQ_31
BC83	DM_DDR1_BI_DQ_29
BC85	GND
BC87	DM_DDR3_BI_DQ_30
BC89	DM_DDR3_BI_DQ_31
BD02	GND
BD04	DM_DDR5_BI_DQS_12_N
BD06	DM_DDR5_BI_DQ_25
BD08	GND
BD10	DM_DDR5_BI_DQS_03_P
BD12	DM_DDR5_BI_DQ_26
BD14	GND
BD16	GND
BD18	DM_DDR7_BI_DQS_08_P
BD20	DM_DDR7_BI_DQ_70
BD22	GND
BD24	DM_DDR5_BI_DQ_01

Pin Number	Signal Name
BD26	DM_DDR5_BI_DQ_05
BD28	DVDD_1P50
BD30	VDDR47_1P20
BD32	VDN_0P70
BD34	VDN_0P70
BD36	VDN_0P70
BD38	VDN_CHIP_VSENSE
BD40	VDN_0P70
BD42	VDN_0P70
BD44	GND
BD46	VDN_0P70
BD48	GND
BD50	VDN_0P70
BD52	VDN_0P70
BD54	VDN_0P70
BD56	VDN_0P70
BD58	VDN_0P70
BD60	GND
BD62	GND
BD64	GND
BD66	DM_DDR3_BI_DQS_17_N
BD68	DM_DDR3_BI_DQ_64
BD70	GND
BD72	DM_DDR1_BI_DQS_02_P
BD74	DM_DDR1_BI_DQ_21
BD76	DM_DDR1_BI_DQ_24
BD78	DM_DDR1_BI_DQS_12_P
BD80	GND
BD82	DM_DDR1_BI_DQS_03_N
BD84	DM_DDR1_BI_DQ_30
BD86	GND
BD88	DM_DDR3_BI_DQ_26
BE03	GND
BE05	GND
BE07	GND
BE09	GND
BE11	GND
BE13	GND
BE15	GND

Pin Number	Signal Name
BE17	GND
BE19	DM_DDR7_BI_DQ_71
BE21	DM_DDR7_BI_DQ_66
BE23	GND
BE25	DM_DDR5_BI_DQ_00
BE27	DM_DDR5_BI_DQ_04
BE29	DVDD_1P50
BE31	VDN_0P70
BE33	GND
BE35	GND
BE37	VDN_CHIP_GSENSE
BE39	GND
BE53	GND
BE55	GND
BE57	GND
BE59	GND
BE61	VDDR03_1P20
BE63	GND
BE65	DM_DDR3_BI_DQ_70
BE67	DM_DDR3_BI_DQS_17_P
BE69	GND
BE71	DM_DDR1_BI_DQS_02_N
BE73	DM_DDR1_BI_DQ_20
BE75	GND
BE77	DM_DDR1_BI_DQ_27
BE79	DM_DDR1_BI_DQS_12_N
BE81	GND
BE83	DM_DDR1_BI_DQS_03_P
BE85	DM_DDR1_BI_DQ_25
BE87	GND
BE89	DM_DDR3_BI_DQ_27
BF02	DM_DDR5_BI_DQ_70
BF04	DM_DDR5_BI_DQ_71
BF06	DM_DDR5_BI_DQS_08_N
BF08	DM_DDR5_BI_DQS_17_P
BF10	DM_DDR5_BI_DQ_64
BF12	DM_DDR5_BI_DQ_68
BF14	GND
BF16	PV_IVRM_V1_M_P0_VREF_P

Pin Number	Signal Name
BF18	GND
BF20	DM_DDR7_BI_DQ_67
BF22	GND
BF24	GND
BF26	GND
BF28	GND
BF30	VDDR47_1P20
BF32	VDN_0P70
BF34	VDN_0P70
BF36	VDN_0P70
BF38	VDN_0P70
BF52	VDN_0P70
BF54	VDN_0P70
BF56	VDN_0P70
BF58	VDN_0P70
BF60	VDN_0P70
BF62	GND
BF64	DM_DDR3_BI_DQ_71
BF66	DM_DDR3_BI_DQS_08_P
BF68	GND
BF70	DM_DDR1_BI_DQ_16
BF72	DM_DDR1_BI_DQS_11_N
BF74	GND
BF76	GND
BF78	DM_DDR1_BI_DQ_28
BF80	DM_DDR1_BI_DQ_26
BF82	GND
BF84	DM_DDR1_BI_DQ_66
BF86	DM_DDR1_BI_DQS_08_N
BF88	GND
BG01	DM_DDR5_BI_DQ_67
BG03	DM_DDR5_BI_DQ_66
BG05	DM_DDR5_BI_DQS_08_P
BG07	DM_DDR5_BI_DQS_17_N
BG09	DM_DDR5_BI_DQ_65
BG11	DM_DDR5_BI_DQ_69
BG13	GND
BG15	PV_IVRM_V1_M_P0_VREF_N
BG17	GND

Pin Number	Signal Name
BG19	GND
BG21	GND
BG23	DM_DDR7_BI_DQ_39
BG25	GND
BG27	GND
BG29	AVDD_1P50
BG31	GND
BG33	VDD_0P80
BG35	VDD_0P80
BG37	VCS_0P96
BG39	VDD_0P80
BG41	VDN_0P70
BG43	VDD_0P80
BG45	VDD_0P80
BG47	VDD_0P80
BG49	VCS_0P96
BG51	VDD_0P80
BG53	VCS_0P96
BG55	VDD_0P80
BG57	VDD_0P80
BG59	GND
BG61	VDDR03_1P20
BG63	DM_DDR3_BI_DQ_67
BG65	DM_DDR3_BI_DQS_08_N
BG67	GND
BG69	DM_DDR1_BI_DQ_19
BG71	DM_DDR1_BI_DQS_11_P
BG73	GND
BG75	GND
BG77	GND
BG79	DM_DDR1_BI_DQ_68
BG81	DM_DDR1_BI_DQ_71
BG83	GND
BG85	DM_DDR1_BI_DQS_17_P
BG87	DM_DDR1_BI_DQS_08_P
BG89	GND
BH02	GND
BH04	GND
BH06	GND

Pin Number	Signal Name
BH08	GND
BH10	GND
BH12	GND
BH14	GND
BH16	GND
BH18	GND
BH20	GND
BH22	DM_DDR7_BI_DQ_38
BH24	DM_DDR7_BI_DQ_34
BH26	DM_DDR7_BI_DQ_35
BH28	AVDD_1P50
BH30	GND
BH32	VDD_0P80
BH34	GND
BH36	GND
BH38	GND
BH40	GND
BH42	GND
BH44	GND
BH46	GND
BH48	GND
BH50	GND
BH52	GND
BH54	TS_EX01C1_P0_P_PIN_GSENSE
BH56	GND
BH58	VDD_0P80
BH60	GND
BH62	GND
BH64	DM_DDR3_BI_DQ_66
BH66	GND
BH68	GND
BH70	DM_DDR1_BI_DQ_22
BH72	GND
BH74	GND
BH76	GND
BH78	GND
BH80	DM_DDR1_BI_DQ_64
BH82	DM_DDR1_BI_DQ_69
BH84	GND

Pin Number	Signal Name
BH86	DM_DDR1_BI_DQS_17_N
BH88	DM_DDR1_BI_DQ_70
BJ01	GND
BJ03	GND
BJ05	GND
BJ07	GND
BJ09	GND
BJ11	GND
BJ13	VDDR47_1P20
BJ15	GND
BJ17	GND
BJ19	GND
BJ21	DM_DDR7_BI_DQS_13_N
BJ23	DM_DDR7_BI_DQS_04_P
BJ25	GND
BJ27	GND
BJ29	GND
BJ31	GND
BJ33	VDD_0P80
BJ35	VDD_0P80
BJ37	VCS_0P96
BJ39	VDD_0P80
BJ41	VDN_0P70
BJ43	VDD_0P80
BJ45	VDD_0P80
BJ47	VDD_0P80
BJ49	VCS_0P96
BJ51	VDD_0P80
BJ53	TS_EX01C1_P0_P_PIN_VSENSE
BJ55	VDD_0P80
BJ57	VDD_0P80
BJ59	GND
BJ61	VDDR03_1P20
BJ63	GND
BJ65	GND
BJ67	GND
BJ69	DM_DDR1_BI_DQ_23
BJ71	GND
BJ73	GND

Pin Number	Signal Name
BJ75	DM_DDR3_P0_P_PIN_RESET_B
BJ77	VDDR03_1P20
BJ79	GND
BJ81	GND
BJ83	GND
BJ85	GND
BJ87	DM_DDR1_BI_DQ_67
BJ89	DM_DDR1_BI_DQ_65
BK02	DM_DDR7_P0_P_PIN_CKE_2
BK04	DM_DDR7_P0_P_PIN_CKE_3
BK06	DM_DDR7_P0_P_PIN_CKE_0
BK08	DM_DDR7_P0_P_PIN_CKE_1
BK10	DM_DDR7_P0_P_PIN_RESET_B
BK12	DM_DDR7_P0_P_PIN_ACT_B
BK14	DM_DDR5_P0_P_PIN_CKE_0
BK16	DM_DDR5_P0_P_PIN_RESET_B
BK18	GND
BK20	DM_DDR7_BI_DQS_13_P
BK22	DM_DDR7_BI_DQS_04_N
BK24	GND
BK26	GND
BK28	GND
BK30	VDN_0P70
BK32	VDD_0P80
BK34	GND
BK36	GND
BK38	GND
BK40	GND
BK42	GND
BK44	GND
BK46	GND
BK48	GND
BK50	VDN_0P70
BK52	GND
BK54	GND
BK56	GND
BK58	VDD_0P80
BK60	VDN_0P70
BK62	GND

Pin Number	Signal Name
BK64	GND
BK66	GND
BK68	GND
BK70	GND
BK72	GND
BK74	DM_DDR3_P0_P_PIN_CKE_1
BK76	GND
BK78	DM_DDR3_P0_P_PIN_CKE_0
BK80	GND
BK82	GND
BK84	GND
BK86	GND
BK88	GND
BL01	DM_DDR7_P0_P_PIN_BANK_GRP_1
BL03	VDDR47_1P20
BL05	DM_DDR7_PIN_P_P0_ERR_B
BL07	GND
BL09	DM_DDR7_P0_P_PIN_BANK_GRP_0
BL11	VDDR47_1P20
BL13	DM_DDR5_P0_P_PIN_CKE_3
BL15	GND
BL17	VDDR47_1P20
BL19	DM_DDR7_BI_DQ_37
BL21	DM_DDR7_BI_DQ_33
BL23	GND
BL25	DM_DDR5_BI_DQ_58
BL27	GND
BL29	VDDR47_1P20
BL31	GND
BL33	VDD_0P80
BL35	VDD_0P80
BL37	VCS_0P96
BL39	VDD_0P80
BL41	VDN_0P70
BL43	VDD_0P80
BL45	VDD_0P80
BL47	VDD_0P80
BL49	VCS_0P96

Pin Number	Signal Name
BL51	VDD_0P80
BL53	VCS_0P96
BL55	VDD_0P80
BL57	VDD_0P80
BL59	GND
BL61	VDDR03_1P20
BL63	PV_AVS1_P0_P_PIN_CLK
BL65	PV_AVS1_P0_P_PIN_MDATA
BL67	GND
BL69	GND
BL71	VDDR03_1P20
BL73	DM_DDR1_P0_P_PIN_RESET_B
BL75	VDDR03_1P20
BL77	DM_DDR3_P0_P_PIN_CKE_2
BL79	GND
BL81	DM_D-DR3_P0_P_PIN_BANK_GRP_0
BL83	VDDR03_1P20
BL85	DM_DDR3_P0_P_PIN_ACT_B
BL87	GND
BL89	GND
BM02	DM_DDR7_P0_P_PIN_ADDR_09
BM04	DM_DDR7_P0_P_PIN_ADDR_11
BM06	DM_DDR7_P0_P_PIN_ADDR_12
BM08	DM_DDR7_P0_P_PIN_ADDR_07
BM10	DM_DDR7_PIN_P_P0_EVENT_B
BM12	DM_DDR5_P0_P_PIN_ACT_B
BM14	DM_DDR5_P0_P_PIN_CKE_2
BM16	DM_DDR5_P0_P_PIN_CKE_1
BM18	GND
BM20	DM_DDR7_BI_DQ_32
BM22	GND
BM24	DM_DDR5_BI_DQ_62
BM26	DM_DDR5_BI_DQ_59
BM28	GND
BM30	GND
BM32	VDD_0P80
BM34	GND
BM36	TS_DTSNPU_P0_P_PIN_TEST_OUT

Pin Number	Signal Name
BM38	GND
BM40	GND
BM42	GND
BM44	GND
BM46	GND
BM48	GND
BM50	GND
BM52	GND
BM54	TS_CACHE0203_P0_P_PIN_VCS_V-SENSE
BM56	GND
BM58	VDD_0P80
BM60	GND
BM62	GND
BM64	PV_AVS1_PIN_P_P0_SDATA
BM66	GND
BM68	GND
BM70	DM_DDR1_P0_P_PIN_CKE_1
BM72	DM_DDR1_P0_P_PIN_CKE_0
BM74	DM_DDR1_P0_P_PIN_CKE_3
BM76	DM_DDR3_P0_P_PIN_CKE_3
BM78	DM_DDR3_P0_P_PIN_CS_B_1
BM80	DM_DDR3_P0_P_PIN_ADDR_07
BM82	DM_DDR3_P0_P_PIN_ADDR_09
BM84	DM_DDR3_P0_P_PIN_ADDR_12
BM86	DM_D-DR3_P0_P_PIN_BANK_GRP_1
BM88	DM_DDR3_PIN_P_P0_ERR_B
BN01	VDDR47_1P20
BN03	DM_DDR7_P0_P_PIN_ADDR_08
BN05	GND
BN07	DM_DDR7_P0_P_PIN_ADDR_05
BN09	VDDR47_1P20
BN11	DM_DDR5_PIN_P_P0_ERR_B
BN13	GND
BN15	DM_D-DR5_P0_P_PIN_BANK_GRP_0
BN17	GND
BN19	DM_DDR7_BI_DQ_36
BN21	GND
BN23	DM_DDR5_BI_DQS_07_N

Pin Number	Signal Name
BN25	DM_DDR5_BI_DQ_63
BN27	GND
BN29	VDDR47_1P20
BN31	GND
BN33	VDD_0P80
BN35	VDD_0P80
BN37	TS_EQALL_P0_P_PIN_AMUX_GSENSE
BN39	VDD_0P80
BN41	VDN_0P70
BN43	VDD_0P80
BN45	VDD_0P80
BN47	VDD_0P80
BN49	VCS_0P96
BN51	VDD_0P80
BN53	TS_CACHE0203_P0_P_PIN_GSENSE
BN55	VDD_0P80
BN57	VDD_0P80
BN59	GND
BN61	VDDR03_1P20
BN63	PV_AVS0_P0_P_PIN_MDATA
BN65	GND
BN67	GND
BN69	GND
BN71	DM_DDR1_P0_P_PIN_CKE_2
BN73	VDDR03_1P20
BN75	DM_DDR1_P0_P_PIN_ACT_B
BN77	GND
BN79	DM_DDR3_P0_P_PIN_CHIPID_0
BN81	VDDR03_1P20
BN83	DM_DDR3_P0_P_PIN_ADDR_06
BN85	GND
BN87	DM_DDR3_P0_P_PIN_ADDR_11
BN89	VDDR03_1P20
BP02	DM_DDR7_P0_P_PIN_ADDR_06
BP04	DM_DDR7_P0_P_PIN_ADDR_03
BP06	DM_DDR7_P0_P_PIN_ADDR_01
BP08	DM_DDR7_P0_P_PIN_ODT_3
BP10	DM_DDR5_P0_P_PIN_ADDR_11

Pin Number	Signal Name
BP12	DM_DDR5_P0_P_PIN_ADDR_12
BP14	DM_D-DR5_P0_P_PIN_BANK_GRP_1
BP16	DM_DDR5_P0_P_PIN_ADDR_09
BP18	GND
BP20	GND
BP22	DM_DDR5_BI_DQS_16_P
BP24	DM_DDR5_BI_DQS_07_P
BP26	GND
BP28	GND
BP30	VDN_0P70
BP32	VDD_0P80
BP34	GND
BP36	TS_EQALL_P0_P_PIN_AMUX_VSENSE
BP38	GND
BP40	GND
BP42	GND
BP44	GND
BP46	GND
BP48	GND
BP50	VDN_0P70
BP52	GND
BP54	TS_EQ1_P0_P_PIN_VCSIN_VSENSE
BP56	GND
BP58	VDD_0P80
BP60	VDN_0P70
BP62	GND
BP64	PV_AVS0_P0_P_PIN_CLK
BP66	DM_DDR3_BI_DQ_58
BP68	GND
BP70	GND
BP72	DM_DDR1_P0_P_PIN_ODT_3
BP74	DM_D-DR1_P0_P_PIN_BANK_GRP_0
BP76	DM_D-DR1_P0_P_PIN_BANK_GRP_1
BP78	DM_DDR3_P0_P_PIN_CHIPID_1
BP80	DM_DDR3_P0_P_PIN_ODT_3
BP82	DM_DDR3_P0_P_PIN_ODT_2
BP84	DM_DDR3_P0_P_PIN_ADDR_03

Pin Number	Signal Name
BP86	DM_DDR3_P0_P_PIN_ADDR_04
BP88	DM_DDR3_P0_P_PIN_ADDR_08
BR01	DM_DDR7_P0_P_PIN_ADDR_04
BR03	GND
BR05	DM_DDR7_P0_P_PIN_CLK_0_N
BR07	VDDR47_1P20
BR09	DM_DDR7_P0_P_PIN_CHIPID_1
BR11	GND
BR13	DM_DDR5_P0_P_PIN_ADDR_07
BR15	VDDR47_1P20
BR17	GND
BR19	GND
BR21	DM_DDR5_BI_DQ_56
BR23	DM_DDR5_BI_DQS_16_N
BR25	GND
BR27	PV_NV3_P0_P_PIN_TERMREF_N
BR29	VDDR47_1P20
BR31	GND
BR33	VDD_0P80
BR35	VDD_0P80
BR37	VCS_0P96
BR39	VDD_0P80
BR41	VDN_0P70
BR43	VDD_0P80
BR45	VDD_0P80
BR47	VDD_0P80
BR49	VCS_0P96
BR51	VDD_0P80
BR53	VCS_0P96
BR55	VDD_0P80
BR57	VDD_0P80
BR59	GND
BR61	VDN_0P70
BR63	PV_AVS0_PIN_P_P0_SDATA
BR65	GND
BR67	DM_DDR3_BI_DQ_62
BR69	GND
BR71	GND
BR73	DM_DDR1_P0_P_PIN_CHIPID_0

Pin Number	Signal Name
BR75	GND
BR77	DM_DDR1_P0_P_PIN_ADDR_12
BR79	VDDR03_1P20
BR81	DM_DDR3_P0_P_PIN_ODT_1
BR83	GND
BR85	DM_DDR3_P0_P_PIN_ADDR_02
BR87	VDDR03_1P20
BR89	DM_DDR3_P0_P_PIN_ADDR_05
BT02	DM_DDR7_P0_P_PIN_ADDR_02
BT04	DM_DDR7_P0_P_PIN_CLK_0_P
BT06	DM_DDR7_P0_P_PIN_ODT_2
BT08	DM_DDR7_P0_P_PIN_CHIPID_2
BT10	DM_DDR5_P0_P_PIN_ADDR_05
BT12	DM_DDR5_P0_P_PIN_ADDR_08
BT14	DM_DDR5_P0_P_PIN_ADDR_06
BT16	DM_DDR5_P0_P_PIN_ADDR_04
BT18	GND
BT20	DM_DDR5_BI_DQ_60
BT22	DM_DDR5_BI_DQ_57
BT24	GND
BT26	PV_NV3_P0_P_PIN_TERMREF_P
BT28	GND
BT30	GND
BT32	VDD_0P80
BT34	GND
BT36	GND
BT38	GND
BT40	GND
BT42	VDD_0P80
BT44	GND
BT46	GND
BT48	GND
BT50	GND
BT52	GND
BT54	GND
BT56	GND
BT58	VDD_0P80
BT60	GND
BT62	GND

Pin Number	Signal Name
BT64	PV_E1B_PIN_P_P0_PRSNT_B
BT66	DM_DDR3_BI_DQ_59
BT68	DM_DDR3_BI_DQS_16_N
BT70	GND
BT72	GND
BT74	DM_DDR1_P0_P_PIN_ODT_1
BT76	DM_DDR1_PIN_P_P0_ERR_B
BT78	DM_DDR1_P0_P_PIN_ADDR_11
BT80	DM_DDR3_P0_P_PIN_CHIPID_2
BT82	DM_DDR3_P0_P_PIN_ADDR_13
BT84	DM_DDR3_PIN_P_P0_EVENT_B
BT86	DM_DDR3_P0_P_PIN_CLK_0_P
BT88	DM_DDR3_P0_P_PIN_ADDR_01
BU01	GND
BU03	DM_DDR7_P0_P_PIN_CLK_1_P
BU05	VDDR47_1P20
BU07	DM_DDR7_P0_P_PIN_ODT_1
BU09	GND
BU11	DM_DDR5_P0_P_PIN_ADDR_03
BU13	VDDR47_1P20
BU15	DM_DDR5_P0_P_PIN_ADDR_01
BU17	GND
BU19	GND
BU21	DM_DDR5_BI_DQ_61
BU23	GND
BU25	TS_JTAG_PIN_P_P0_CARD_TEST
BU27	TS_NV3_P0_P_PIN_ATST
BU29	VDDR47_1P20
BU31	GND
BU33	VDD_0P80
BU35	VDD_0P80
BU37	TS_EX06_P0_P_PIN_TDIODE_A
BU39	VDD_0P80
BU41	VDN_0P70
BU43	VDD_0P80
BU45	VDD_0P80
BU47	VDD_0P80
BU49	VDD_0P80
BU51	TS_EX0203_P0_P_PIN_VPP_ VSENSE

Pin Number	Signal Name
BU53	TS_EX0203_P0_P_PIN_VBL_ VSENSE
BU55	VDD_0P80
BU57	VDD_0P80
BU59	GND
BU61	VDN_0P70
BU63	GND
BU65	GND
BU67	DM_DDR3_BI_DQ_63
BU69	DM_DDR3_BI_DQS_16_P
BU71	GND
BU73	GND
BU75	DM_DDR1_P0_P_PIN_ADDR_09
BU77	VDDR03_1P20
BU79	DM_DDR1_P0_P_PIN_ADDR_08
BU81	GND
BU83	DM_DDR3_P0_P_PIN_CS_B_3
BU85	VDDR03_1P20
BU87	DM_DDR3_P0_P_PIN_CLK_0_N
BU89	GND
BV02	DM_DDR7_P0_P_PIN_CLK_1_N
BV04	DM_D-DR7_P0_P_PIN_BANK_ADR_1
BV06	DM_DDR7_P0_P_PIN_CS_B_1
BV08	DM_DDR7_P0_P_PIN_CHIPID_0
BV10	DM_DDR5_P0_P_PIN_ADDR_02
BV12	DM_DDR5_P0_P_PIN_CLK_0_N
BV14	DM_DDR5_P0_P_PIN_ADDR_00
BV16	GND
BV18	DM_DDR7_BI_DQ_51
BV20	GND
BV22	GND
BV24	GND
BV26	GND
BV28	GND
BV30	VDN_0P70
BV32	VDD_0P80
BV34	GND
BV36	TS_EX06_P0_P_PIN_TDIODE_C
BV38	GND

Pin Number	Signal Name
BV40	GND
BV42	GND
BV44	GND
BV46	GND
BV48	GND
BV50	VDN_0P70
BV52	TS_EX0203_P0_P_PIN_L3_GSENSE
BV54	TS_EX0203_P0_P_PIN_VWL_ VSENSE
BV56	GND
BV58	VDD_0P80
BV60	VIO_1P00
BV62	GND
BV64	PV_E1A_PIN_P_P0_PRSNT_B
BV66	GND
BV68	DM_DDR3_BI_DQS_07_P
BV70	DM_DDR3_BI_DQ_56
BV72	GND
BV74	GND
BV76	DM_DDR1_P0_P_PIN_ADDR_06
BV78	DM_DDR1_P0_P_PIN_ADDR_07
BV80	DM_DDR1_P0_P_PIN_ADDR_05
BV82	DM_DDR3_P0_P_PIN_ADDR_17
BV84	DM_DDR3_P0_P_PIN_CS_B_2
BV86	DM_DDR3_P0_P_PIN_PAR
BV88	DM_DDR3_P0_P_PIN_CLK_1_N
BW01	DM_DDR7_P0_P_PIN_PAR
BW03	VDDR47_1P20
BW05	DM_DDR7_P0_P_PIN_CS_B_2
BW07	GND
BW09	DM_DDR5_P0_P_PIN_CLK_1_N
BW11	VDDR47_1P20
BW13	DM_DDR5_P0_P_PIN_CLK_0_P
BW15	GND
BW17	DM_DDR7_BI_DQ_50
BW19	GND
BW21	GND
BW23	GND
BW25	GND
BW27	GND

Pin Number	Signal Name
BW29	VIO_1P00
BW31	VDD_0P80
BW33	VDD_0P80
BW35	VDD_0P80
BW37	VCS_0P96
BW39	VDD_0P80
BW41	VDN_0P70
BW43	VDD_0P80
BW45	VDD_0P80
BW47	VDD_0P80
BW49	VCS_0P96
BW51	VDD_0P80
BW53	VCS_0P96
BW55	VDD_0P80
BW57	VDD_0P80
BW59	VDD_0P80
BW61	VIO_1P00
BW63	PV_E1B_P0_P_PIN_PERST_B
BW65	GND
BW67	GND
BW69	DM_DDR3_BI_DQS_07_N
BW71	DM_DDR3_BI_DQ_60
BW73	GND
BW75	GND
BW77	DM_DDR1_P0_P_PIN_ADDR_04
BW79	GND
BW81	DM_DDR1_P0_P_PIN_ADDR_01
BW83	VDDR03_1P20
BW85	DM_DDR3_P0_P_PIN_ADDR_10
BW87	GND
BW89	DM_DDR3_P0_P_PIN_CLK_1_P
BY02	DM_DDR7_P0_P_PIN_ADDR_00
BY04	DM_DDR7_P0_P_PIN_ADDR_16
BY06	DM_DDR7_P0_P_PIN_ADDR_17
BY08	DM_DDR5_P0_P_PIN_CLK_1_P
BY10	DM_DDR5_P0_P_PIN_PAR
BY12	DM_D-DR5_P0_P_PIN_BANK_ADR_0
BY14	GND
BY16	GND

Pin Number	Signal Name
BY18	DM_DDR7_BI_DQ_55
BY20	GND
BY22	VSB1_3P30
BY24	TS_PRV_P0_P_PIN_PROBE3
BY26	GND
BY28	GND
BY30	GND
BY32	VDD_0P80
BY34	GND
BY36	GND
BY38	GND
BY40	GND
BY42	VDD_0P80
BY44	GND
BY46	GND
BY48	GND
BY50	GND
BY52	GND
BY54	GND
BY56	GND
BY58	VDD_0P80
BY60	GND
BY62	GND
BY64	PV_E1A_P0_P_PIN_PERST_B
BY66	DM_DDR1_BI_DQ_39
BY68	GND
BY70	DM_DDR3_BI_DQ_57
BY72	DM_DDR3_BI_DQ_50
BY74	GND
BY76	GND
BY78	DM_DDR1_P0_P_PIN_CLK_0_N
BY80	DM_DDR1_P0_P_PIN_ADDR_03
BY82	DM_DDR1_P0_P_PIN_ADDR_02
BY84	DM_DDR3_P0_P_PIN_ODT_0
BY86	DM_D-DR3_P0_P_PIN_BANK_ADR_1
BY88	DM_DDR3_P0_P_PIN_ADDR_00
CA01	VDDR47_1P20
CA03	DM_DDR7_P0_P_PIN_ADDR_10
CA05	GND

Pin Number	Signal Name
CA07	DM_DDR5_PIN_P_P0_EVENT_B
CA09	VDDR47_1P20
CA11	DM_DDR5_P0_P_PIN_ADDR_15
CA13	GND
CA15	GND
CA17	DM_DDR7_BI_DQ_54
CA19	GND
CA21	GND
CA23	VSB1_3P30
CA25	TS_PRV_P0_P_PIN_PROBE4
CA27	TS_NV3_P0_P_PIN_HFC_P
CA29	VIO_1P00
CA31	VDN_0P70
CA33	VDN_0P70
CA35	VDN_0P70
CA37	VDN_0P70
CA39	VDN_0P70
CA41	VDN_0P70
CA43	GND
CA45	VDN_0P70
CA47	GND
CA49	VDN_0P70
CA51	GND
CA53	VDN_0P70
CA55	GND
CA57	VDN_0P70
CA59	GND
CA61	VIO_1P00
CA63	PV_E0A_PIN_P_P0_PRSNT_B
CA65	GND
CA67	DM_DDR1_BI_DQ_38
CA69	GND
CA71	DM_DDR3_BI_DQ_61
CA73	DM_DDR3_BI_DQ_54
CA75	GND
CA77	GND
CA79	DM_DDR1_P0_P_PIN_CLK_0_P
CA81	VDDR03_1P20
CA83	DM_DDR1_P0_P_PIN_CLK_1_N

Pin Number	Signal Name
CA85	GND
CA87	DM_D-DR3_P0_P_PIN_BANK_ADR_0
CA89	VDDR03_1P20
CB02	DM_D-DR7_P0_P_PIN_BANK_ADR_0
CB04	DM_DDR7_P0_P_PIN_CS_B_0
CB06	DM_D-DR5_P0_P_PIN_BANK_ADR_1
CB08	DM_DDR5_P0_P_PIN_ADDR_16
CB10	DM_DDR5_P0_P_PIN_CS_B_0
CB12	GND
CB14	GND
CB16	DM_DDR7_BI_DQS_06_P
CB18	GND
CB20	DM_DDR5_BI_DQ_50
CB22	GND
CB24	GND
CB26	TS_NV3_P0_P_PIN_HFC_N
CB28	GND
CB30	VDN_0P70
CB32	VIO_1P00
CB34	VIO_1P00
CB36	GND
CB38	VSB0_3P30
CB40	GND
CB42	VSB_1P10
CB44	GND
CB46	VDN_0P70
CB48	VIO_1P00
CB50	VIO_1P00
CB52	VIO_1P00
CB54	VIO_1P00
CB56	VIO_1P00
CB58	VIO_1P00
CB60	VIO_1P00
CB62	SCM_PRESENT_B
CB64	PV_NV0_P0_P_PIN_TERMREF_P
CB66	DM_DDR1_BI_DQ_35
CB68	DM_DDR1_BI_DQS_13_N
CB70	GND

Pin Number	Signal Name
CB72	DM_DDR3_BI_DQ_51
CB74	DM_DDR3_BI_DQS_15_N
CB76	GND
CB78	GND
CB80	DM_DDR1_PIN_P_P0_EVENT_B
CB82	DM_DDR1_P0_P_PIN_PAR
CB84	DM_DDR1_P0_P_PIN_CLK_1_P
CB86	DM_DDR3_P0_P_PIN_CS_B_0
CB88	DM_DDR3_P0_P_PIN_ADDR_16
CC01	DM_DDR7_P0_P_PIN_ADDR_14
CC03	GND
CC05	DM_DDR5_P0_P_PIN_ADDR_10
CC07	VDDR47_1P20
CC09	DM_DDR5_P0_P_PIN_CHIPID_1
CC11	GND
CC13	GND
CC15	DM_DDR7_BI_DQS_06_N
CC17	GND
CC19	DM_DDR5_BI_DQ_54
CC21	DM_DDR5_BI_DQ_51
CC23	GND
CC25	GND
CC27	PV_E2C_P0_P_PIN_PERST_B
CC29	PV_PRV_PIN_P_P0_BSENSE3
CC31	GND
CC33	GND
CC35	GND
CC37	VSB0_3P30
CC39	GND
CC41	VSB_1P10
CC43	GND
CC45	TS_NESTLCPLL_P0_P_PIN_ATST
CC47	TS_NESTLCPLL_P0_P_PIN_HFC_P
CC49	PV_NV2_P0_P_PIN_REFCLK_P
CC51	GND
CC53	GND
CC55	GND
CC57	TS_E0_P0_P_PIN_ATST
CC59	TS_E1_P0_P_PIN_ATST

Pin Number	Signal Name
CC61	GND
CC63	PV_NV0_P0_P_PIN_TERMREF_N
CC65	GND
CC67	DM_DDR1_BI_DQ_34
CC69	DM_DDR1_BI_DQS_13_P
CC71	GND
CC73	DM_DDR3_BI_DQ_55
CC75	DM_DDR3_BI_DQS_15_P
CC77	GND
CC79	GND
CC81	DM_D-DR1_P0_P_PIN_BANK_ADR_1
CC83	GND
CC85	DM_DDR1_P0_P_PIN_ADDR_00
CC87	VDDR03_1P20
CC89	DM_DDR3_P0_P_PIN_ADDR_14
CD02	DM_DDR7_P0_P_PIN_ADDR_15
CD04	DM_DDR5_P0_P_PIN_CS_B_2
CD06	DM_DDR5_P0_P_PIN_ADDR_14
CD08	DM_DDR5_P0_P_PIN_CHIPID_0
CD10	GND
CD12	GND
CD14	DM_DDR7_BI_DQ_49
CD16	DM_DDR7_BI_DQS_15_N
CD18	GND
CD20	DM_DDR5_BI_DQ_55
CD22	GND
CD24	NV_NV3_PIN_P_P0_DAT_23_P
CD26	GND
CD28	PV_E2B_P0_P_PIN_PERST_B
CD30	TS_E2_P0_P_PIN_ATST
CD32	PV_E2A_P0_P_PIN_PERST_B
CD34	PV_E2_P0_P_PIN_TERMREF_N
CD36	GND
CD38	PV_PRV_PIN_P_P0_LPC_CLK
CD40	GND
CD42	PV_PRV_PIN_P_P0_LPC_IRQ
CD44	GND
CD46	TS_NESTLCPLL_P0_P_PIN_HFC_N
CD48	PV_NV2_P0_P_PIN_REFCLK_N

Pin Number	Signal Name
CD50	GND
CD52	PV_SYS0_PIN_P_P0_REFCLK_N
CD54	GND
CD56	PV_E0_P0_P_PIN_TERMREF_N
CD58	PV_E1_P0_P_PIN_TERMREF_N
CD60	PE_E1_PIN_P_P0_DAT_07_P
CD62	PV_PRV_PIN_P_P0_BSENSE1
CD64	GND
CD66	GND
CD68	DM_DDR1_BI_DQS_04_P
CD70	DM_DDR1_BI_DQ_37
CD72	GND
CD74	DM_DDR3_BI_DQS_06_P
CD76	DM_DDR3_BI_DQ_48
CD78	GND
CD80	GND
CD82	DM_DDR1_P0_P_PIN_ADDR_10
CD84	DM_DDR1_P0_P_PIN_ADDR_16
CD86	DM_D-DR1_P0_P_PIN_BANK_ADR_0
CD88	DM_DDR3_P0_P_PIN_ADDR_15
CE01	GND
CE03	DM_DDR7_P0_P_PIN_ODT_0
CE05	VDDR47_1P20
CE07	DM_DDR5_P0_P_PIN_ODT_0
CE09	GND
CE11	GND
CE13	DM_DDR7_BI_DQ_48
CE15	DM_DDR7_BI_DQS_15_P
CE17	GND
CE19	DM_DDR5_BI_DQS_06_P
CE21	GND
CE23	NV_NV3_PIN_P_P0_DAT_23_N
CE25	GND
CE27	PV_E2C_PIN_P_P0_PRSNT_B
CE29	PV_E2B_PIN_P_P0_PRSNT_B
CE31	PV_E2A_PIN_P_P0_PRSNT_B
CE33	PV_E2_P0_P_PIN_TERMREF_P
CE35	PV_E2C_P0_P_PIN_SLOT_CLK_N
CE37	GND

Pin Number	Signal Name
CE39	PV_PRV_P0_P_PIN_LPC_FRAME_B
CE41	PV_PRV_P0_P_PIN_LPC_RESET_B
CE43	GND
CE45	PV_NV0_P0_P_PIN_REFCLK_P
CE47	PV_NV1_P0_P_PIN_REFCLK_P
CE49	GND
CE51	GND
CE53	PV_SYS0_PIN_P_P0_REFCLK_P
CE55	PV_E0_P0_P_PIN_TERMREF_P
CE57	PV_E1_P0_P_PIN_TERMREF_P
CE59	GND
CE61	PE_E1_PIN_P_P0_DAT_07_N
CE63	GND
CE65	PV_E0_P0_P_PIN_SLOT_CLK_N
CE67	GND
CE69	DM_DDR1_BI_DQS_04_N
CE71	DM_DDR1_BI_DQ_36
CE73	GND
CE75	DM_DDR3_BI_DQS_06_N
CE77	DM_DDR3_BI_DQ_52
CE79	GND
CE81	GND
CE83	DM_DDR1_P0_P_PIN_CS_B_2
CE85	VDDR03_1P20
CE87	DM_DDR1_P0_P_PIN_ADDR_14
CE89	GND
CF02	DM_DDR7_P0_P_PIN_CS_B_3
CF04	DM_DDR5_P0_P_PIN_ODT_2
CF06	DM_DDR5_P0_P_PIN_CS_B_3
CF08	GND
CF10	GND
CF12	DM_DDR7_BI_DQ_43
CF14	DM_DDR7_BI_DQ_53
CF16	GND
CF18	DM_DDR5_BI_DQS_06_N
CF20	GND
CF22	GND
CF24	NV_NV3_PIN_P_P0_DAT_22_P
CF26	GND

Pin Number	Signal Name
CF28	PE_E2_P0_P_PIN_DAT_01_N
CF30	PE_E2_P0_P_PIN_DAT_00_N
CF32	GND
CF34	PV_E2C_P0_P_PIN_SLOT_CLK_P
CF36	GND
CF38	PV_PRV_P0_B_PIN_LPC_DAT_0
CF40	GND
CF42	GND
CF44	PV_NV0_P0_P_PIN_REFCLK_N
CF46	PV_NV1_P0_P_PIN_REFCLK_N
CF48	GND
CF50	PV_PCI0_PIN_P_P0_REFCLK_P
CF52	GND
CF54	GND
CF56	TS_TST_PIN_P_P0_FORCE_P-WR_ON
CF58	GND
CF60	PE_E1_PIN_P_P0_DAT_08_P
CF62	GND
CF64	PV_E0_P0_P_PIN_SLOT_CLK_P
CF66	PV_E1A_P0_P_PIN_SLOT_CLK_N
CF68	GND
CF70	DM_DDR1_BI_DQ_33
CF72	DM_DDR1_BI_DQ_55
CF74	GND
CF76	DM_DDR3_BI_DQ_49
CF78	DM_DDR3_BI_DQ_42
CF80	GND
CF82	GND
CF84	DM_DDR1_P0_P_PIN_CS_B_0
CF86	DM_DDR1_P0_P_PIN_ODT_2
CF88	DM_DDR1_P0_P_PIN_ADDR_15
CG01	DM_DDR7_P0_P_PIN_ADDR_13
CG03	VDDR47_1P20
CG05	DM_DDR5_P0_P_PIN_CS_B_1
CG07	GND
CG09	GND
CG11	DM_DDR7_BI_DQ_47
CG13	DM_DDR7_BI_DQ_52
CG15	GND

Pin Number	Signal Name
CG17	DM_DDR5_BI_DQS_15_N
CG19	GND
CG21	NV_NV3_PIN_P_P0_DAT_21_P
CG23	NV_NV3_PIN_P_P0_DAT_22_N
CG25	GND
CG27	PE_E2_P0_P_PIN_DAT_01_P
CG29	GND
CG31	PE_E2_P0_P_PIN_DAT_00_P
CG33	GND
CG35	PV_E2B_P0_P_PIN_SLOT_CLK_N
CG37	GND
CG39	PV_PRV_P0_B_PIN_LPC_DAT_1
CG41	PV_PRV_P0_B_PIN_LPC_DAT_2
CG43	GND
CG45	GND
CG47	GND
CG49	GND
CG51	PV_PCI0_PIN_P_P0_REFCLK_N
CG53	GND
CG55	TS_JTAG_PIN_P_P0_TDI
CG57	TS_JTAG_PIN_P_P0_TMS
CG59	GND
CG61	PE_E1_PIN_P_P0_DAT_08_N
CG63	GND
CG65	PV_E1A_P0_P_PIN_SLOT_CLK_P
CG67	GND
CG69	GND
CG71	DM_DDR1_BI_DQ_32
CG73	DM_DDR1_BI_DQ_54
CG75	GND
CG77	DM_DDR3_BI_DQ_53
CG79	DM_DDR3_BI_DQ_46
CG81	GND
CG83	GND
CG85	DM_DDR1_P0_P_PIN_CS_B_3
CG87	GND
CG89	DM_DDR1_P0_P_PIN_ODT_0
CH02	DM_DDR5_P0_P_PIN_ADDR_13
CH04	DM_DDR5_P0_P_PIN_ADDR_17

Pin Number	Signal Name
CH06	GND
CH08	GND
CH10	DM_DDR7_BI_DQ_46
CH12	DM_DDR7_BI_DQ_42
CH14	GND
CH16	DM_DDR5_BI_DQS_15_P
CH18	GND
CH20	NV_NV3_PIN_P_P0_DAT_21_N
CH22	GND
CH24	NV_NV3_PIN_P_P0_DAT_20_N
CH26	GND
CH28	PE_E2_P0_P_PIN_DAT_03_N
CH30	PE_E2_P0_P_PIN_DAT_02_N
CH32	GND
CH34	PV_E2B_P0_P_PIN_SLOT_CLK_P
CH36	GND
CH38	PV_PRV_P0_B_PIN_LPC_DAT_3
CH40	GND
CH42	PV_APSS_P0_P_PIN_CS0
CH44	GND
CH46	GND
CH48	PV_PSI_P0_P_PIN_CLK_N
CH50	GND
CH52	GND
CH54	GND
CH56	TS_JTAG_P0_P_PIN_TDO
CH58	GND
CH60	GND
CH62	GND
CH64	PV_E1B_P0_P_PIN_SLOT_CLK_N
CH66	GND
CH68	GND
CH70	GND
CH72	DM_DDR1_BI_DQ_51
CH74	DM_DDR1_BI_DQS_15_N
CH76	GND
CH78	DM_DDR3_BI_DQ_43
CH80	DM_DDR3_BI_DQS_14_N
CH82	GND

Pin Number	Signal Name
CH84	GND
CH86	DM_DDR1_P0_P_PIN_ADDR_13
CH88	DM_DDR1_P0_P_PIN_CS_B_1
CJ01	VDDR47_1P20
CJ03	DM_DDR5_P0_P_PIN_ODT_1
CJ05	GND
CJ07	GND
CJ09	DM_DDR7_BI_DQS_14_N
CJ11	DM_DDR7_BI_DQS_05_P
CJ13	GND
CJ15	DM_DDR5_BI_DQ_53
CJ17	DM_DDR5_BI_DQ_49
CJ19	GND
CJ21	NV_NV3_PIN_P_P0_DAT_19_P
CJ23	NV_NV3_PIN_P_P0_DAT_20_P
CJ25	GND
CJ27	PE_E2_P0_P_PIN_DAT_03_P
CJ29	GND
CJ31	PE_E2_P0_P_PIN_DAT_02_P
CJ33	GND
CJ35	PV_E2A_P0_P_PIN_SLOT_CLK_N
CJ37	GND
CJ39	PV_APSS_P0_P_PIN_CS1
CJ41	PV_APSS_PIN_P_P0_MISO
CJ43	GND
CJ45	PV_CP1_P0_P_PIN_FSI_CLK
CJ47	PV_PSI_P0_P_PIN_CLK_P
CJ49	GND
CJ51	GND
CJ53	PV_PSI_PIN_P_P0_DAT
CJ55	GND
CJ57	GND
CJ59	PE_E1_P0_P_PIN_DAT_08_N
CJ61	GND
CJ63	PV_E1B_P0_P_PIN_SLOT_CLK_P
CJ65	GND
CJ67	NV_NV0_PIN_P_P0_DAT_22_N
CJ69	NV_NV0_PIN_P_P0_DAT_16_P
CJ71	GND

Pin Number	Signal Name
CJ73	DM_DDR1_BI_DQ_50
CJ75	DM_DDR1_BI_DQS_15_P
CJ77	GND
CJ79	DM_DDR3_BI_DQ_47
CJ81	DM_DDR3_BI_DQS_14_P
CJ83	GND
CJ85	GND
CJ87	DM_DDR1_P0_P_PIN_ADDR_17
CJ89	VDDR03_1P20
CK02	DM_DDR5_P0_P_PIN_ODT_3
CK04	GND
CK06	GND
CK08	DM_DDR7_BI_DQS_14_P
CK10	DM_DDR7_BI_DQS_05_N
CK12	GND
CK14	DM_DDR5_BI_DQ_43
CK16	DM_DDR5_BI_DQ_48
CK18	GND
CK20	NV_NV3_PIN_P_P0_DAT_19_N
CK22	GND
CK24	NV_NV3_PIN_P_P0_DAT_14_P
CK26	GND
CK28	PE_E2_P0_P_PIN_DAT_05_N
CK30	PE_E2_P0_P_PIN_DAT_04_P
CK32	GND
CK34	PV_E2A_P0_P_PIN_SLOT_CLK_P
CK36	GND
CK38	PV_APSS_P0_P_PIN_MOSI
CK40	GND
CK42	GND
CK44	PV_CP1_P0_B_PIN_FSI_DAT
CK46	GND
CK48	GND
CK50	PV_FSP0_PIN_P_P0_FSI_CLK
CK52	GND
CK54	PV_PSI_PIN_P_P0_CLK_P
CK56	GND
CK58	GND
CK60	PE_E1_P0_P_PIN_DAT_08_P

Pin Number	Signal Name
CK62	PV_E0_P0_P_PIN_PERST_B
CK64	GND
CK66	NV_NV0_PIN_P_P0_DAT_22_P
CK68	GND
CK70	NV_NV0_PIN_P_P0_DAT_16_N
CK72	GND
CK74	DM_DDR1_BI_DQS_06_P
CK76	DM_DDR1_BI_DQ_53
CK78	GND
CK80	DM_DDR3_BI_DQS_05_P
CK82	DM_DDR3_BI_DQ_33
CK84	GND
CK86	GND
CK88	DM_DDR1_P0_P_PIN_CHIPID_2
CL01	DM_DDR5_P0_P_PIN_CHIPID_2
CL03	GND
CL05	GND
CL07	DM_DDR7_BI_DQ_45
CL09	DM_DDR7_BI_DQ_41
CL11	GND
CL13	DM_DDR5_BI_DQ_47
CL15	DM_DDR5_BI_DQ_52
CL17	GND
CL19	GND
CL21	NV_NV3_PIN_P_P0_DAT_15_P
CL23	NV_NV3_PIN_P_P0_DAT_14_N
CL25	GND
CL27	PE_E2_P0_P_PIN_DAT_05_P
CL29	GND
CL31	PE_E2_P0_P_PIN_DAT_04_N
CL33	GND
CL35	GND
CL37	GND
CL39	PV_APSS_P0_P_PIN_SCLK
CL41	PV_SEEPROM0_P0_P_PIN_I2C_SCL_B
CL43	GND
CL45	GND
CL47	PV_PSI_P0_P_PIN_DAT
CL49	GND

Pin Number	Signal Name
CL51	PV_FSP0_P0_B_PIN_FSI_DAT
CL53	GND
CL55	PV_PSI_PIN_P_P0_CLK_N
CL57	PV_E0B_PIN_P_P0_PRSNT_B
CL59	PE_E1_P0_P_PIN_DAT_07_P
CL61	GND
CL63	GND
CL65	GND
CL67	NV_NV0_PIN_P_P0_DAT_23_N
CL69	NV_NV0_PIN_P_P0_DAT_20_N
CL71	GND
CL73	GND
CL75	DM_DDR1_BI_DQS_06_N
CL77	DM_DDR1_BI_DQ_52
CL79	GND
CL81	DM_DDR3_BI_DQS_05_N
CL83	DM_DDR3_BI_DQ_32
CL85	GND
CL87	GND
CL89	DM_DDR1_P0_P_PIN_CHIPID_1
CM02	GND
CM04	GND
CM06	DM_DDR7_BI_DQ_44
CM08	DM_DDR7_BI_DQ_40
CM10	GND
CM12	DM_DDR5_BI_DQ_46
CM14	DM_DDR5_BI_DQ_42
CM16	GND
CM18	NV_NV3_PIN_P_P0_DAT_16_P
CM20	NV_NV3_PIN_P_P0_DAT_15_N
CM22	GND
CM24	GND
CM26	GND
CM28	PE_E2_P0_P_PIN_DAT_07_N
CM30	PE_E2_P0_P_PIN_DAT_06_P
CM32	GND
CM34	GND
CM36	GND
CM38	GND

Pin Number	Signal Name
CM40	GND
CM42	PV_SEEPROM0_P0_B_PIN_I2C_SDA_B
CM44	GND
CM46	GND
CM48	GND
CM50	GND
CM52	GND
CM54	GND
CM56	GND
CM58	GND
CM60	PE_E1_P0_P_PIN_DAT_07_N
CM62	GND
CM64	GND
CM66	NV_NV0_PIN_P_P0_DAT_23_P
CM68	GND
CM70	NV_NV0_PIN_P_P0_DAT_20_P
CM72	NV_NV0_PIN_P_P0_DAT_13_P
CM74	GND
CM76	DM_DDR1_BI_DQ_49
CM78	DM_DDR1_BI_DQ_60
CM80	GND
CM82	DM_DDR3_BI_DQ_41
CM84	DM_DDR3_BI_DQ_36
CM86	GND
CM88	GND
CN01	GND
CN03	GND
CN05	DM_DDR7_BI_DQ_60
CN07	DM_DDR7_BI_DQ_61
CN09	GND
CN11	DM_DDR5_BI_DQS_14_N
CN13	DM_DDR5_BI_DQS_05_P
CN15	GND
CN17	NV_NV3_PIN_P_P0_DAT_16_N
CN19	GND
CN21	NV_NV3_PIN_P_P0_DAT_13_P
CN23	GND
CN25	TS_CLK_P0_P_PIN_PROBE0_P
CN27	PE_E2_P0_P_PIN_DAT_07_P

Pin Number	Signal Name
CN29	GND
CN31	PE_E2_P0_P_PIN_DAT_06_N
CN33	GND
CN35	PE_E2_PIN_P_P0_DAT_15_P
CN37	PE_E2_PIN_P_P0_DAT_00_N
CN39	GND
CN41	GND
CN43	PV_PRV_PIN_P_P0_VDN_PGOOD
CN45	PV_SEEPROM2_P0_B_PIN_I2C_SDA_B
CN47	GND
CN49	PE_E0_PIN_P_P0_DAT_15_P
CN51	GND
CN53	PE_E0_PIN_P_P0_DAT_00_P
CN55	GND
CN57	PE_E0_P0_P_PIN_DAT_14_P
CN59	PE_E0_P0_P_PIN_DAT_15_N
CN61	GND
CN63	NV_NV0_P0_P_PIN_DAT_23_P
CN65	GND
CN67	GND
CN69	NV_NV0_PIN_P_P0_DAT_21_P
CN71	GND
CN73	NV_NV0_PIN_P_P0_DAT_13_N
CN75	GND
CN77	DM_DDR1_BI_DQ_48
CN79	DM_DDR1_BI_DQ_61
CN81	GND
CN83	DM_DDR3_BI_DQ_40
CN85	DM_DDR3_BI_DQ_37
CN87	GND
CN89	GND
CP02	GND
CP04	DM_DDR7_BI_DQ_56
CP06	DM_DDR7_BI_DQS_16_P
CP08	GND
CP10	DM_DDR5_BI_DQS_14_P
CP12	DM_DDR5_BI_DQS_05_N
CP14	GND
CP16	GND

Pin Number	Signal Name
CP18	NV_NV3_PIN_P_P0_DAT_18_P
CP20	NV_NV3_PIN_P_P0_DAT_13_N
CP22	GND
CP24	GND
CP26	GND
CP28	PE_E2_P0_P_PIN_DAT_15_N
CP30	PE_E2_P0_P_PIN_DAT_08_N
CP32	GND
CP34	PE_E2_PIN_P_P0_DAT_15_N
CP36	GND
CP38	PE_E2_PIN_P_P0_DAT_00_P
CP40	GND
CP42	PV_SEEPROM3_P0_B_PIN_I2C_SDA_B
CP44	PV_SEEPROM2_P0_P_PIN_I2C_SCL_B
CP46	PV_SEEPROM1_P0_P_PIN_I2C_SCL_B
CP48	GND
CP50	PE_E0_PIN_P_P0_DAT_15_N
CP52	PE_E0_PIN_P_P0_DAT_00_N
CP54	GND
CP56	PE_E0_P0_P_PIN_DAT_14_N
CP58	GND
CP60	PE_E0_P0_P_PIN_DAT_15_P
CP62	GND
CP64	NV_NV0_P0_P_PIN_DAT_23_N
CP66	GND
CP68	GND
CP70	NV_NV0_PIN_P_P0_DAT_21_N
CP72	NV_NV0_PIN_P_P0_DAT_14_P
CP74	GND
CP76	GND
CP78	DM_DDR1_BI_DQ_56
CP80	DM_DDR1_BI_DQS_16_P
CP82	GND
CP84	DM_DDR3_BI_DQS_04_N
CP86	DM_DDR3_BI_DQS_13_P
CP88	GND
CR01	GND
CR03	DM_DDR7_BI_DQ_57

Pin Number	Signal Name
CR05	DM_DDR7_BI_DQS_16_N
CR07	GND
CR09	DM_DDR5_BI_DQ_45
CR11	DM_DDR5_BI_DQ_41
CR13	GND
CR15	NV_NV3_PIN_P_P0_DAT_11_P
CR17	NV_NV3_PIN_P_P0_DAT_18_N
CR19	GND
CR21	GND
CR23	NV_NV3_P0_P_PIN_DAT_00_P
CR25	TS_CLK_P0_P_PIN_PROBE0_N
CR27	PE_E2_P0_P_PIN_DAT_15_P
CR29	GND
CR31	PE_E2_P0_P_PIN_DAT_08_P
CR33	GND
CR35	PE_E2_PIN_P_P0_DAT_14_P
CR37	PE_E2_PIN_P_P0_DAT_01_P
CR39	GND
CR41	PV_SEEPROM3_P0_P_PIN_I2C_SCL_B
CR43	GND
CR45	PV_SEEPROM1_P0_B_PIN_I2C_SDA_B
CR47	GND
CR49	PE_E0_PIN_P_P0_DAT_14_P
CR51	GND
CR53	PE_E0_PIN_P_P0_DAT_01_N
CR55	GND
CR57	PE_E0_P0_P_PIN_DAT_12_P
CR59	PE_E0_P0_P_PIN_DAT_13_N
CR61	GND
CR63	NV_NV0_P0_P_PIN_DAT_22_P
CR65	GND
CR67	NV_NV0_P0_P_PIN_DAT_00_N
CR69	GND
CR71	GND
CR73	NV_NV0_PIN_P_P0_DAT_14_N
CR75	NV_NV0_PIN_P_P0_DAT_00_N
CR77	GND
CR79	DM_DDR1_BI_DQ_57

Pin Number	Signal Name
CR81	DM_DDR1_BI_DQS_16_N
CR83	GND
CR85	DM_DDR3_BI_DQS_04_P
CR87	DM_DDR3_BI_DQS_13_N
CR89	GND
CT02	DM_DDR7_BI_DQS_07_N
CT04	DM_DDR7_BI_DQ_62
CT06	GND
CT08	DM_DDR5_BI_DQ_44
CT10	DM_DDR5_BI_DQ_40
CT12	GND
CT14	NV_NV3_PIN_P_P0_DAT_11_N
CT16	GND
CT18	NV_NV3_PIN_P_P0_DAT_17_N
CT20	GND
CT22	NV_NV3_P0_P_PIN_DAT_00_N
CT24	GND
CT26	GND
CT28	PE_E2_P0_P_PIN_DAT_12_P
CT30	PE_E2_P0_P_PIN_DAT_09_N
CT32	GND
CT34	PE_E2_PIN_P_P0_DAT_14_N
CT36	GND
CT38	PE_E2_PIN_P_P0_DAT_01_N
CT40	GND
CT42	PV_PRV_PIN_P_P0_CHIP_MASTER
CT44	GND
CT46	TS_JTAG_PIN_P_P0_TCK
CT48	GND
CT50	PE_E0_PIN_P_P0_DAT_14_N
CT52	PE_E0_PIN_P_P0_DAT_01_P
CT54	GND
CT56	PE_E0_P0_P_PIN_DAT_12_N
CT58	GND
CT60	PE_E0_P0_P_PIN_DAT_13_P
CT62	GND
CT64	NV_NV0_P0_P_PIN_DAT_22_N
CT66	NV_NV0_P0_P_PIN_DAT_00_P
CT68	GND

Pin Number	Signal Name
CT70	GND
CT72	NV_NV0_PIN_P_P0_DAT_15_P
CT74	GND
CT76	NV_NV0_PIN_P_P0_DAT_00_P
CT78	GND
CT80	DM_DDR1_BI_DQS_07_N
CT82	DM_DDR1_BI_DQ_62
CT84	GND
CT86	DM_DDR3_BI_DQ_39
CT88	DM_DDR3_BI_DQ_38
CU01	DM_DDR7_BI_DQS_07_P
CU03	DM_DDR7_BI_DQ_63
CU05	GND
CU07	DM_DDR5_BI_DQ_32
CU09	DM_DDR5_BI_DQ_36
CU11	GND
CU13	GND
CU15	NV_NV3_PIN_P_P0_DAT_06_N
CU17	NV_NV3_PIN_P_P0_DAT_17_P
CU19	GND
CU21	GND
CU23	GND
CU25	GND
CU27	PE_E2_P0_P_PIN_DAT_12_N
CU29	GND
CU31	PE_E2_P0_P_PIN_DAT_09_P
CU33	GND
CU35	PE_E2_PIN_P_P0_DAT_13_N
CU37	PE_E2_PIN_P_P0_DAT_02_N
CU39	GND
CU41	TS_PRV_P0_P_PIN_PROBE2
CU43	GND
CU45	PV_PRV_P0_B_PIN_SPARE0
CU47	GND
CU49	PE_E0_PIN_P_P0_DAT_13_P
CU51	GND
CU53	PE_E0_PIN_P_P0_DAT_02_P
CU55	GND
CU57	PE_E0_P0_P_PIN_DAT_10_P

Pin Number	Signal Name
CU59	PE_E0_P0_P_PIN_DAT_11_P
CU61	GND
CU63	NV_NV0_P0_P_PIN_DAT_21_P
CU65	GND
CU67	NV_NV0_P0_P_PIN_DAT_01_N
CU69	GND
CU71	GND
CU73	NV_NV0_PIN_P_P0_DAT_15_N
CU75	NV_NV0_PIN_P_P0_DAT_01_N
CU77	GND
CU79	GND
CU81	DM_DDR1_BI_DQS_07_P
CU83	DM_DDR1_BI_DQ_63
CU85	GND
CU87	DM_DDR3_BI_DQ_35
CU89	DM_DDR3_BI_DQ_34
CV02	DM_DDR7_BI_DQ_58
CV04	GND
CV06	DM_DDR5_BI_DQ_33
CV08	DM_DDR5_BI_DQ_37
CV10	GND
CV12	NV_NV3_PIN_P_P0_DAT_07_N
CV14	NV_NV3_PIN_P_P0_DAT_06_P
CV16	GND
CV18	NV_NV3_PIN_P_P0_DAT_12_P
CV20	GND
CV22	NV_NV3_P0_P_PIN_DAT_01_N
CV24	NV_NV3_P0_P_PIN_DAT_02_N
CV26	GND
CV28	PE_E2_P0_P_PIN_DAT_13_N
CV30	PE_E2_P0_P_PIN_DAT_10_N
CV32	GND
CV34	PE_E2_PIN_P_P0_DAT_13_P
CV36	GND
CV38	PE_E2_PIN_P_P0_DAT_02_P
CV40	GND
CV42	PV_PRV_P0_B_PIN_GPIO1
CV44	GND
CV46	PV_PRV_P0_B_PIN_SPARE2

Pin Number	Signal Name
CV48	GND
CV50	PE_E0_PIN_P_P0_DAT_13_N
CV52	PE_E0_PIN_P_P0_DAT_02_N
CV54	GND
CV56	PE_E0_P0_P_PIN_DAT_10_N
CV58	GND
CV60	PE_E0_P0_P_PIN_DAT_11_N
CV62	GND
CV64	NV_NV0_P0_P_PIN_DAT_21_N
CV66	NV_NV0_P0_P_PIN_DAT_01_P
CV68	GND
CV70	GND
CV72	GND
CV74	GND
CV76	NV_NV0_PIN_P_P0_DAT_01_P
CV78	NV_NV0_PIN_P_P0_DAT_02_N
CV80	GND
CV82	DM_DDR1_BI_DQ_58
CV84	DM_DDR1_BI_DQ_44
CV86	GND
CV88	DM_DDR3_BI_DQ_44
CW01	DM_DDR7_BI_DQ_59
CW03	GND
CW05	DM_DDR5_BI_DQS_04_N
CW07	DM_DDR5_BI_DQS_13_P
CW09	GND
CW11	NV_NV3_PIN_P_P0_DAT_07_P
CW13	GND
CW15	NV_NV3_PIN_P_P0_DAT_04_N
CW17	NV_NV3_PIN_P_P0_DAT_12_N
CW19	GND
CW21	NV_NV3_P0_P_PIN_DAT_01_P
CW23	NV_NV3_P0_P_PIN_DAT_02_P
CW25	GND
CW27	PE_E2_P0_P_PIN_DAT_13_P
CW29	GND
CW31	PE_E2_P0_P_PIN_DAT_10_P
CW33	GND
CW35	PE_E2_PIN_P_P0_DAT_12_P

Pin Number	Signal Name
CW37	PE_E2_PIN_P_P0_DAT_03_P
CW39	GND
CW41	PV_PRV_P0_B_PIN_GPIO0
CW43	PV_PRV_P0_B_PIN_GPIO2
CW45	PV_PRV_PIN_P_P0_FSI_SMD
CW47	GND
CW49	PE_E0_PIN_P_P0_DAT_12_N
CW51	GND
CW53	PE_E0_PIN_P_P0_DAT_03_N
CW55	GND
CW57	PE_E0_P0_P_PIN_DAT_08_P
CW59	PE_E0_P0_P_PIN_DAT_09_P
CW61	GND
CW63	NV_NV0_P0_P_PIN_DAT_20_P
CW65	GND
CW67	NV_NV0_P0_P_PIN_DAT_03_N
CW69	NV_NV0_P0_P_PIN_DAT_02_N
CW71	GND
CW73	GND
CW75	NV_NV0_PIN_P_P0_DAT_03_N
CW77	GND
CW79	NV_NV0_PIN_P_P0_DAT_02_P
CW81	GND
CW83	DM_DDR1_BI_DQ_59
CW85	DM_DDR1_BI_DQ_45
CW87	GND
CW89	DM_DDR3_BI_DQ_45
CY02	GND
CY04	DM_DDR5_BI_DQS_04_P
CY06	DM_DDR5_BI_DQS_13_N
CY08	GND
CY10	GND
CY12	NV_NV3_PIN_P_P0_DAT_08_P
CY14	NV_NV3_PIN_P_P0_DAT_04_P
CY16	GND
CY18	GND
CY20	GND
CY22	GND
CY24	GND

Pin Number	Signal Name
CY26	GND
CY28	PE_E2_P0_P_PIN_DAT_14_P
CY30	PE_E2_P0_P_PIN_DAT_11_N
CY32	GND
CY34	PE_E2_PIN_P_P0_DAT_12_N
CY36	GND
CY38	PE_E2_PIN_P_P0_DAT_03_N
CY40	GND
CY42	GND
CY44	GND
CY46	TS_TST_PIN_P_P0_LSSD_TE
CY48	GND
CY50	PE_E0_PIN_P_P0_DAT_12_P
CY52	PE_E0_PIN_P_P0_DAT_03_P
CY54	GND
CY56	PE_E0_P0_P_PIN_DAT_08_N
CY58	GND
CY60	PE_E0_P0_P_PIN_DAT_09_N
CY62	GND
CY64	NV_NV0_P0_P_PIN_DAT_20_N
CY66	NV_NV0_P0_P_PIN_DAT_03_P
CY68	GND
CY70	NV_NV0_P0_P_PIN_DAT_02_P
CY72	GND
CY74	GND
CY76	NV_NV0_PIN_P_P0_DAT_03_P
CY78	NV_NV0_PIN_P_P0_DAT_08_N
CY80	GND
CY82	GND
CY84	DM_DDR1_BI_DQ_40
CY86	DM_DDR1_BI_DQS_14_P
CY88	GND
DA01	GND
DA03	DM_DDR5_BI_DQ_34
DA05	DM_DDR5_BI_DQ_38
DA07	GND
DA09	NV_NV3_PIN_P_P0_DAT_00_P
DA11	NV_NV3_PIN_P_P0_DAT_08_N
DA13	GND

Pin Number	Signal Name
DA15	NV_NV3_PIN_P_P0_DAT_05_P
DA17	GND
DA19	NV_NV3_P0_P_PIN_DAT_03_N
DA21	NV_NV3_P0_P_PIN_DAT_07_N
DA23	NV_NV3_P0_P_PIN_DAT_08_P
DA25	GND
DA27	PE_E2_P0_P_PIN_DAT_14_N
DA29	GND
DA31	PE_E2_P0_P_PIN_DAT_11_P
DA33	GND
DA35	PE_E2_PIN_P_P0_DAT_11_P
DA37	PE_E2_PIN_P_P0_DAT_04_N
DA39	GND
DA41	TS_OCC_PIN_P_P0_ALERT_B
DA43	PV_TPM_PIN_P_P0_INT
DA45	PV_PRV_PIN_P_P0_FSI_IN_ENA
DA47	GND
DA49	PE_E0_PIN_P_P0_DAT_11_N
DA51	GND
DA53	PE_E0_PIN_P_P0_DAT_04_P
DA55	GND
DA57	PE_E0_P0_P_PIN_DAT_07_N
DA59	PE_E0_P0_P_PIN_DAT_00_N
DA61	GND
DA63	NV_NV0_P0_P_PIN_DAT_16_P
DA65	GND
DA67	NV_NV0_P0_P_PIN_DAT_12_N
DA69	NV_NV0_P0_P_PIN_DAT_08_P
DA71	GND
DA73	NV_NV0_P0_P_PIN_DAT_07_N
DA75	GND
DA77	GND
DA79	NV_NV0_PIN_P_P0_DAT_08_P
DA81	NV_NV0_PIN_P_P0_DAT_07_N
DA83	GND
DA85	DM_DDR1_BI_DQ_41
DA87	DM_DDR1_BI_DQS_14_N
DA89	GND
DB02	DM_DDR5_BI_DQ_35

Pin Number	Signal Name
DB04	DM_DDR5_BI_DQ_39
DB06	GND
DB08	NV_NV3_PIN_P_P0_DAT_00_N
DB10	GND
DB12	NV_NV3_PIN_P_P0_DAT_10_P
DB14	NV_NV3_PIN_P_P0_DAT_05_N
DB16	GND
DB18	NV_NV3_P0_P_PIN_DAT_03_P
DB20	NV_NV3_P0_P_PIN_DAT_07_P
DB22	NV_NV3_P0_P_PIN_DAT_08_N
DB24	GND
DB26	GND
DB28	GND
DB30	GND
DB32	GND
DB34	PE_E2_PIN_P_P0_DAT_11_N
DB36	GND
DB38	PE_E2_PIN_P_P0_DAT_04_P
DB40	GND
DB42	PV_PRV_P0_P_PIN_ATTENTION_B
DB44	PV_TPM_P0_P_PIN_RESET
DB46	PV_PRV_PIN_P_P0_STBY_RE-SET_B
DB48	GND
DB50	PE_E0_PIN_P_P0_DAT_11_P
DB52	PE_E0_PIN_P_P0_DAT_04_N
DB54	GND
DB56	PE_E0_P0_P_PIN_DAT_07_P
DB58	GND
DB60	PE_E0_P0_P_PIN_DAT_00_P
DB62	GND
DB64	NV_NV0_P0_P_PIN_DAT_16_N
DB66	NV_NV0_P0_P_PIN_DAT_12_P
DB68	GND
DB70	NV_NV0_P0_P_PIN_DAT_08_N
DB72	NV_NV0_P0_P_PIN_DAT_07_P
DB74	GND
DB76	GND
DB78	GND
DB80	GND

Pin Number	Signal Name
DB82	NV_NV0_PIN_P_P0_DAT_07_P
DB84	GND
DB86	DM_DDR1_BI_DQS_05_N
DB88	DM_DDR1_BI_DQ_46
DC07	GND
DC09	NV_NV3_PIN_P_P0_DAT_01_P
DC11	NV_NV3_PIN_P_P0_DAT_10_N
DC13	GND
DC15	GND
DC17	GND
DC19	GND
DC21	GND
DC23	GND
DC25	GND
DC27	GND
DC29	GND
DC31	GND
DC33	GND
DC35	PE_E2_PIN_P_P0_DAT_08_N
DC37	PE_E2_PIN_P_P0_DAT_05_P
DC39	GND
DC41	PV_NV3A_P0_B_PIN_I2C_SDA_B
DC43	GND
DC45	GND
DC47	GND
DC49	PE_E0_PIN_P_P0_DAT_10_N
DC51	GND
DC53	PE_E0_PIN_P_P0_DAT_05_N
DC55	GND
DC57	PE_E0_P0_P_PIN_DAT_04_P
DC59	PE_E0_P0_P_PIN_DAT_01_P
DC61	GND
DC63	NV_NV0_P0_P_PIN_DAT_15_P
DC65	GND
DC67	NV_NV0_P0_P_PIN_DAT_17_N
DC69	NV_NV0_P0_P_PIN_DAT_10_P
DC71	GND
DC73	NV_NV0_P0_P_PIN_DAT_09_N
DC75	GND

Pin Number	Signal Name
DC77	GND
DC79	GND
DC81	NV_NV0_PIN_P_P0_DAT_10_N
DC83	GND
DC85	GND
DC87	DM_DDR1_BI_DQS_05_P
DC89	DM_DDR1_BI_DQ_47
DD08	NV_NV3_PIN_P_P0_DAT_01_N
DD10	GND
DD12	NV_NV3_PIN_P_P0_DAT_09_P
DD14	GND
DD16	NV_NV3_P0_P_PIN_DAT_09_P
DD18	NV_NV3_P0_P_PIN_DAT_10_P
DD20	NV_NV3_P0_P_PIN_DAT_12_N
DD22	NV_NV3_P0_P_PIN_DAT_16_P
DD24	NV_NV3_P0_P_PIN_DAT_14_N
DD26	NV_NV3_P0_P_PIN_DAT_18_P
DD28	NV_NV3_P0_P_PIN_DAT_21_N
DD30	NV_NV3_P0_P_PIN_DAT_23_N
DD32	GND
DD34	PE_E2_PIN_P_P0_DAT_08_P
DD36	GND
DD38	PE_E2_PIN_P_P0_DAT_05_N
DD40	GND
DD42	PV_NV0B_P0_B_PIN_I2C_SDA_B
DD44	PV_NV0A_P0_B_PIN_I2C_SDA_B
DD46	PV_NV0A_P0_B_PIN_I2C_SCL_B
DD48	GND
DD50	PE_E0_PIN_P_P0_DAT_10_P
DD52	PE_E0_PIN_P_P0_DAT_05_P
DD54	GND
DD56	PE_E0_P0_P_PIN_DAT_04_N
DD58	GND
DD60	PE_E0_P0_P_PIN_DAT_01_N
DD62	GND
DD64	NV_NV0_P0_P_PIN_DAT_15_N
DD66	NV_NV0_P0_P_PIN_DAT_17_P
DD68	GND
DD70	NV_NV0_P0_P_PIN_DAT_10_N

Pin Number	Signal Name
DD72	NV_NV0_P0_P_PIN_DAT_09_P
DD74	GND
DD76	NV_NV0_PIN_P_P0_DAT_19_P
DD78	NV_NV0_PIN_P_P0_DAT_17_P
DD80	GND
DD82	NV_NV0_PIN_P_P0_DAT_10_P
DD84	NV_NV0_PIN_P_P0_DAT_09_N
DD86	GND
DD88	DM_DDR1_BI_DQ_42
DE09	NV_NV3_PIN_P_P0_DAT_02_P
DE11	NV_NV3_PIN_P_P0_DAT_09_N
DE13	GND
DE15	NV_NV3_P0_P_PIN_DAT_09_N
DE17	NV_NV3_P0_P_PIN_DAT_10_N
DE19	GND
DE21	NV_NV3_P0_P_PIN_DAT_12_P
DE23	NV_NV3_P0_P_PIN_DAT_16_N
DE25	NV_NV3_P0_P_PIN_DAT_14_P
DE27	NV_NV3_P0_P_PIN_DAT_18_N
DE29	NV_NV3_P0_P_PIN_DAT_21_P
DE31	NV_NV3_P0_P_PIN_DAT_23_P
DE33	GND
DE35	PE_E2_PIN_P_P0_DAT_10_N
DE37	PE_E2_PIN_P_P0_DAT_07_P
DE39	GND
DE41	PV_NV3A_P0_B_PIN_I2C_SCL_B
DE43	PV_NV0B_P0_B_PIN_I2C_SCL_B
DE45	PV_DDR4567_P0_B_PIN_I2C_S-DA_B
DE47	GND
DE49	PE_E0_PIN_P_P0_DAT_08_N
DE51	GND
DE53	PE_E0_PIN_P_P0_DAT_07_P
DE55	GND
DE57	PE_E0_P0_P_PIN_DAT_05_N
DE59	PE_E0_P0_P_PIN_DAT_02_P
DE61	GND
DE63	NV_NV0_P0_P_PIN_DAT_13_P
DE65	GND
DE67	NV_NV0_P0_P_PIN_DAT_19_N

Pin Number	Signal Name
DE69	NV_NV0_P0_P_PIN_DAT_06_P
DE71	GND
DE73	NV_NV0_P0_P_PIN_DAT_05_N
DE75	GND
DE77	NV_NV0_PIN_P_P0_DAT_19_N
DE79	NV_NV0_PIN_P_P0_DAT_17_N
DE81	GND
DE83	GND
DE85	NV_NV0_PIN_P_P0_DAT_09_P
DE87	GND
DE89	DM_DDR1_BI_DQ_43
DF08	NV_NV3_PIN_P_P0_DAT_02_N
DF10	GND
DF12	GND
DF14	GND
DF16	GND
DF18	GND
DF20	GND
DF22	GND
DF24	GND
DF26	GND
DF28	GND
DF30	GND
DF32	GND
DF34	PE_E2_PIN_P_P0_DAT_10_P
DF36	GND
DF38	PE_E2_PIN_P_P0_DAT_07_N
DF40	GND
DF42	GND
DF44	GND
DF46	PV_DDR4567_P0_B_PIN_I2C_S-CL_B
DF48	GND
DF50	PE_E0_PIN_P_P0_DAT_08_P
DF52	PE_E0_PIN_P_P0_DAT_07_N
DF54	GND
DF56	PE_E0_P0_P_PIN_DAT_05_P
DF58	GND
DF60	PE_E0_P0_P_PIN_DAT_02_N
DF62	GND

Pin Number	Signal Name
DF64	NV_NV0_P0_P_PIN_DAT_13_N
DF66	NV_NV0_P0_P_PIN_DAT_19_P
DF68	GND
DF70	NV_NV0_P0_P_PIN_DAT_06_N
DF72	NV_NV0_P0_P_PIN_DAT_05_P
DF74	GND
DF76	GND
DF78	GND
DF80	GND
DF82	GND
DF84	GND
DF86	GND
DF88	GND
DG09	GND
DG11	GND
DG13	NV_NV3_P0_P_PIN_DAT_04_N
DG15	NV_NV3_P0_P_PIN_DAT_05_N
DG17	NV_NV3_P0_P_PIN_DAT_06_P
DG19	NV_NV3_P0_P_PIN_DAT_11_P
DG21	NV_NV3_P0_P_PIN_DAT_17_P
DG23	NV_NV3_P0_P_PIN_DAT_19_P
DG25	NV_NV3_P0_P_PIN_DAT_13_P
DG27	NV_NV3_P0_P_PIN_DAT_15_P
DG29	NV_NV3_P0_P_PIN_DAT_20_N
DG31	NV_NV3_P0_P_PIN_DAT_22_P
DG33	GND
DG35	PE_E2_PIN_P_P0_DAT_09_N
DG37	PE_E2_PIN_P_P0_DAT_06_P
DG39	GND
DG41	PV_PCI_P0_B_PIN_I2C_SCL_B
DG43	PV_LP_P0_B_PIN_I2C_SDA_B
DG45	PV_DDR0123_P0_B_PIN_I2C_S-DA_B
DG47	GND
DG49	PE_E0_PIN_P_P0_DAT_09_N
DG51	GND
DG53	PE_E0_PIN_P_P0_DAT_06_N
DG55	GND
DG57	PE_E0_P0_P_PIN_DAT_06_P
DG59	PE_E0_P0_P_PIN_DAT_03_P

Pin Number	Signal Name
DG61	GND
DG63	NV_NV0_P0_P_PIN_DAT_14_P
DG65	GND
DG67	NV_NV0_P0_P_PIN_DAT_18_N
DG69	NV_NV0_P0_P_PIN_DAT_11_P
DG71	GND
DG73	NV_NV0_P0_P_PIN_DAT_04_N
DG75	GND
DG77	NV_NV0_PIN_P_P0_DAT_18_P
DG79	NV_NV0_PIN_P_P0_DAT_12_P
DG81	NV_NV0_PIN_P_P0_DAT_11_P
DG83	NV_NV0_PIN_P_P0_DAT_06_P
DG85	NV_NV0_PIN_P_P0_DAT_05_P
DG87	NV_NV0_PIN_P_P0_DAT_04_P
DG89	GND
DH08	NV_NV3_PIN_P_P0_DAT_03_N
DH10	GND
DH12	NV_NV3_P0_P_PIN_DAT_04_P
DH14	NV_NV3_P0_P_PIN_DAT_05_P
DH16	NV_NV3_P0_P_PIN_DAT_06_N
DH18	NV_NV3_P0_P_PIN_DAT_11_N
DH20	NV_NV3_P0_P_PIN_DAT_17_N
DH22	NV_NV3_P0_P_PIN_DAT_19_N
DH24	NV_NV3_P0_P_PIN_DAT_13_N
DH26	NV_NV3_P0_P_PIN_DAT_15_N
DH28	NV_NV3_P0_P_PIN_DAT_20_P
DH30	NV_NV3_P0_P_PIN_DAT_22_N
DH32	GND
DH34	PE_E2_PIN_P_P0_DAT_09_P
DH36	GND
DH38	PE_E2_PIN_P_P0_DAT_06_N
DH40	GND
DH42	PV_PCI_P0_B_PIN_I2C_SDA_B
DH44	PV_LP_P0_B_PIN_I2C_SCL_B
DH46	PV_DDR0123_P0_B_PIN_I2C_S-CL_B
DH48	GND
DH50	PE_E0_PIN_P_P0_DAT_09_P
DH52	PE_E0_PIN_P_P0_DAT_06_P
DH54	GND

Pin Number	Signal Name
DH56	PE_E0_P0_P_PIN_DAT_06_N
DH58	GND
DH60	PE_E0_P0_P_PIN_DAT_03_N
DH62	GND
DH64	NV_NV0_P0_P_PIN_DAT_14_N
DH66	NV_NV0_P0_P_PIN_DAT_18_P
DH68	GND
DH70	NV_NV0_P0_P_PIN_DAT_11_N
DH72	NV_NV0_P0_P_PIN_DAT_04_P
DH74	GND
DH76	GND
DH78	NV_NV0_PIN_P_P0_DAT_18_N
DH80	NV_NV0_PIN_P_P0_DAT_12_N
DH82	NV_NV0_PIN_P_P0_DAT_11_N
DH84	NV_NV0_PIN_P_P0_DAT_06_N
DH86	NV_NV0_PIN_P_P0_DAT_05_N
DH88	NV_NV0_PIN_P_P0_DAT_04_N
DJ09	NV_NV3_PIN_P_P0_DAT_03_P
DJ11	GND
DJ13	GND
DJ15	GND
DJ17	GND
DJ19	GND
DJ21	GND
DJ23	GND
DJ25	GND
DJ27	GND
DJ29	GND
DJ31	GND
DJ33	GND
DJ35	GND
DJ37	GND
DJ39	GND
DJ41	GND
DJ43	GND
DJ45	GND
DJ47	GND
DJ49	GND
DJ51	GND

Pin Number	Signal Name
DJ53	GND
DJ55	GND
DJ57	GND
DJ59	GND
DJ61	GND
DJ63	GND
DJ65	GND
DJ67	GND
DJ69	GND
DJ71	GND
DJ73	GND
DJ75	GND
DJ77	GND
DJ79	GND
DJ81	GND
DJ83	GND
DJ85	GND
DJ87	GND
DJ89	GND

Glossary

AES	Advanced Encryption Standard
APSS	Analog power subsystem sweep
ASIC	Application-specific integrated circuit
AVS	Adaptive voltage scaling
BEOL	Back-end of the line
BMC	Baseboard management controller
CAPI	Coherent accelerator processor interface
CAPP	Coherent accelerator processor proxy
CDR	Clock and data recovery
CMOS	Complementary metal–oxide–semiconductor
CRB	Customer reference board
CRC	Cyclic redundancy check
CTLE	Continuous time linear equalizer
DAC	Digital-to-analog converter
DDR	Double data rate
DFE	Decision feedback equalizer
DIMM	Dual in-line memory module
DMA	Direct memory attach
DRAM	Dynamic random-access memory
DTS	Digital thermal sensor
ECO	Extended cache option
ECRC	End-to-end CRC
EDI	Elastic differential I/O
EEH	Enhance error handling
EI4	Elastic interface 4
ET	Early time
eVRM	External voltage regulator module
FBC	Fabric controller

FC PLGA	Flip-chip plastic land grid array
FFE	Feed-forward equalizer
FPGA	Field-programmable gate array
FRU	Field replaceable unit
FSI	FRU service interface
GTps	Gigatransfers per second
GPU	Graphics processing unit
HCSL	Host clock signal level
HSS	High-speed serial
I^2C	Inter-integrated circuit
IEEE	Institute of Electrical and Electronics Engineers
IODA	I/O Design Architecture
IP	Intellectual property
ISA	Instruction set architecture
iVRM	Internal voltage regulator module
JEDEC	Formerly the Joint Electron Device Engineering Council
JTAG	Joint Test Action Group
LED	Light-emitting diode
LGA	Land grid array
LPAR	Logical partition
LPC	Low pin count bus or lowest point of coherency
LRDIMM	Load-reduced dual in-line memory module
LSI	Level signalled interrup
LSSD	Level-sensitive scan design
LTE	Long-tail equalizer
MFSI	Master FSI
MPUL	Most-positive up level
MSI	Message signalled interrupt
Mux	Multiplexer

NPU	NVLink processing unit
OCC	On-chip controller
PAPR	Power Architecture Platform Reference
PBA	Per buffer addressability mode
PCIe	Peripheral Component Interconnect Express
PDA	Per DRAM addressability mode
PE	Partitionable endpoints
PEC	PCI Express controller
PHB	PCI Host Bridge
PHY	Physical layer
PLL	Phase-locked loop
PMC	Power management control
PMCR	Power Management Control Register
PMICR	Power Management Idle Control Register
PMSR	Power Management Status Register
POL	Point of load
PPE	Programmable PowerPC-lite engine
PPM	Parts per million
PRBS	Pseudo-random binary sequence
PSI	Processor support interface
PVR	Processor Version Register
QR	Quad rank
RC	Root complex
RDC	Regulator design current
RDIMM	Registered dual in-line memory module
RDP	Regulator design power
RX	Receive
SBE	Self-boot engine
SCM	Single-chip module

SCOM	Scan communications
SEEPROM	Serial electrically erasable programmable read-only memory
SerDes	Serializer/deserializer
SMP	Symmetric multiprocessor
SMT	Simultaneous multithreading
SHA	Secure hash algorithm
SOI	Silicon-on-insulator
SPI	Serial peripheral interconnect
SPR	Special Purpose Register
SRAM	Static random access memory
SST	Source series terminated
TCE	Translation control entry
TDC	Thermal design current
TDP	Thermal design power
TDR	Time domain reflectometer
T_A	Thermal junction temperature
T_J	Thermal junction temperature
TLP	Transaction layer packet
TPM	Trusted platform module
TX	Transmit
UPS	Uninterrupted power system
VID	Voltage ID
VPD	Vital product data
VRM	Voltage regulator module