



POWER8 Processor SCM and Memory Buffer

Hardware Errata Notice

DD 2.x

Advance

Version 1.2
5 May 2015



© Copyright International Business Machines Corporation 2014, 2015

Printed in the United States of America May 2015

IBM, the IBM logo, and ibm.com are trademarks or registered trademarks of International Business Machines Corp., registered in many jurisdictions worldwide. Other product and service names might be trademarks of IBM or other companies. A current list of IBM trademarks is available on the Web at "Copyright and trademark information" at www.ibm.com/legal/copytrade.shtml.

Other company, product, and service names may be trademarks or service marks of others.

All information contained in this document is subject to change without notice. The products described in this document are NOT intended for use in applications such as implantation, life support, or other hazardous uses where malfunction could result in death, bodily injury, or catastrophic property damage. The information contained in this document does not affect or change IBM product specifications or warranties. Nothing in this document shall operate as an express or implied license or indemnity under the intellectual property rights of IBM or third parties. All information contained in this document was obtained in specific environments, and is presented as an illustration. The results obtained in other operating environments may vary.

While the information contained herein is believed to be accurate, such information is preliminary, and should not be relied upon for accuracy or completeness, and no representations or warranties of accuracy or completeness are made.

Note: This document contains information on products in the design, sampling and/or initial production phases of development. This information is subject to change without notice. Verify with your IBM field applications engineer that you have the latest version of this document before finalizing a design.

This document is intended for development of technology products compatible with Power Architecture®. You may use this document, for any purpose (commercial or personal) and make modifications and distribute; however, modifications to this document may violate Power Architecture and should be carefully considered. Any distribution of this document or its derivative works shall include this Notice page including but not limited to the IBM warranty disclaimer and IBM liability limitation. No other licenses, expressed or implied, by estoppel or otherwise to any intellectual property rights are granted by this document.

THE INFORMATION CONTAINED IN THIS DOCUMENT IS PROVIDED ON AN "AS IS" BASIS. IBM makes no representations or warranties, either express or implied, including but not limited to, warranties of merchantability, fitness for a particular purpose, or non-infringement, or that any practice or implementation of the IBM documentation will not infringe any third party patents, copyrights, trade secrets, or other rights. In no event will IBM be liable for damages arising directly or indirectly from any use of the information contained in this document.

IBM Systems and Technology Group
2070 Route 52, Bldg. 330
Hopewell Junction, NY 12533-6351

The IBM home page can be found at ibm.com®.

Version 1.2
5 May 2015

Introduction

For the design revision levels specified (DD 2.x), this document identifies differences between the actual operation of the IBM® POWER8™ Processor SCM and IBM POWER8 Memory Buffer devices and what is described in the POWER8 User Manuals and Datasheets.

Differences that are not visible to the user are not described. If a difference is hidden or compensated for by IBM-supplied firmware or by IBM-supplied system software, it is not included in this document.

This is a working document. Check regularly with your IBM technical representative to verify that you have the most current version. For more information, contact OpenPOWER@us.ibm.com.

Note: Some of the workarounds described in this document might involve the use of IBM software or firmware modules to affect or reduce the effect of the erratum. These modules are typically supplied with the POWER8 devices. If, however, you do not have the module required for a workaround, contact IBM to acquire it.

Revision Levels Covered

This document includes information about errata that apply to the following design revision levels:

- POWER8 Processor SCM revision DD 2.0 and later
- POWER8 Memory Buffer revision DD 2.0 and later

This document does not contain information about POWER8 Processor or POWER8 Memory Buffer levels before DD 2.0. Any statements in this document about other revision levels of these products are for reference only. For errata information about these revision levels, see the current Errata Notice for the specific revision of the product.

Errata Categories

Each erratum is assigned to a category numbered 1 - 5 based on its impact on system performance and the ability of any proposed workaround to minimize that impact. *Table 1* explains the meaning of each category.

Table 1. Errata Categories

Errata Category	Definition
1	Major impact; no workaround available. An erratum is said to have a major impact if it results in a system crash, a hard failure, an unrecoverable soft failure, significant performance degradation, or the storage of incorrect data.
2	Major impact; workaround is impractical to implement, or a substantial risk exists of encountering the same problem or additional problems, including performance issues, after the workaround is implemented.
3	Major impact; workaround available. Application of the workaround either eliminates the problem, or reduces it to a minor impact issue.
4	Minor impact; no workaround available. An erratum is said to have a minor impact if it results in slight to moderate performance degradation or is a functional variance from the specification.
5	Minor impact; workaround is available. An erratum is said to have a minor impact if it results in slight to moderate performance degradation or is a functional variance from the specification. Application of the workaround eliminates the problem.

Terminology

The following section headings and terms are used in this document:

Design Notes	Design notes are clarifications or additions to the published documentation about topics that IBM considers of special interest.
Erratum #n	The errata are numbered sequentially.
Erratum	An erratum is any difference between the actual operation of the specific design revision level and the design specification.
Abstract	The abstract is a brief description of the erratum.
Impact	A category is assigned to an erratum based on its impact on system performance and the ability of any proposed workaround to minimize that impact. See <i>Table 1</i> on page 3.
Published Date	The date that the erratum was first published.
Applies to	Indicates which devices and revision levels are affected by the erratum.
Status	This is the current status of the erratum discussion and the current plan for the future.
Description	This section provides a description of the erratum.
Workarounds	This section lists any actions that customers can take to reduce or eliminate the effects of the erratum. These actions supplement any workarounds embedded in the IBM code. If you are not using the operating system or firmware supplied or recommended by IBM, contact OpenPOWER@us.ibm.com .

Summary of Errata

Table 2 summarizes the errata described in this document.

Table 2. Summary of Errata (Page 1 of 2)

Erratum Number	Abstract	Errata Category	Workaround Available?	See Page
1	HID4 bit 33 must remain static after boot.	5	Yes	7
2	<u>NX CBB</u> reported as both killed and completed.	5	Yes	8
3	Incorrect data during scrub and steer cleanup with <u>UE</u> trap mode enabled.	5	Yes	9
4	Cfam_reset after V _{IO} power on does not trigger selfboot.	5	Yes	10
5	Multithreaded <u>XSCOM</u> causes false Done and delayed error handling.	5	Yes	11
6	Certain software sequences result in ignored <u>PMU</u> interrupts.	5	Yes	12
7	Micropartition prefetch incompatible with 2 <u>LPAR</u> and 4 LPAR mode.	5	Yes	14



Table 2. Summary of Errata (Page 2 of 2)

Erratum Number	Abstract	Errata Category	Workaround Available?	See Page
8	During a PMU state save routine, MMCR0[PMAO] and MMCR0[PMAE] are inconsistent for one cycle on every counter overflow while exceptions are enabled.	5	Yes	15
9	All PMU events that measure reload latency (PM_MRK_DATA_FROM_*_CYC) overcount the latency of marked noncacheable loads.	4	No	17
10	The X-Bus is disabled on all OpenPOWER POWER8 Processor SCMs manufactured after 1 May 2015. If older versions of firmware are executed on POWER8 Processor SCMs manufactured after this date with the X-Bus disabled, the POWER8 Processor SCM will fail to boot and error messages will be displayed.	3	Yes	19

Design Note 1

Abstract: Powering off V_{CS} during IPL is not supported.

Published Date: 16 May 2014

Applies To: POWER8 Memory Buffer

Status: No fix is planned.

Description

System power dissipation can be reduced by disabling the L4 cache and turning off V_{CS} when not in use. However, V_{CS} must be on during system power on or IML/IPL (specifically during scan ring rotation), because some of the logic that is powered by V_{CS} is required for this function.

Workarounds

None.



Erratum #1

Abstract:	HID4 bit 33 must remain static after boot.
Impact:	Category 5. Minor impact; workaround is available. An erratum is said to have a minor impact if it results in slight to moderate performance degradation or is a functional variance from the specification. Application of the workaround eliminates the problem.
Published Date:	16 May 2014
Applies To:	POWER8 Processor SCM
Status:	No fix is planned.

Description

Changing the state of HID4[33] RMSC_EN with an **mtspr** IBM PowerPC® instruction can cause a core checkstop.

Workarounds

Set the state of HID4[33] RMSC_EN at POR scan time and do not change it.

Erratum #2

Abstract:	<u>NX CRB</u> reported as both killed and completed.
Impact:	Category 5. Minor impact; workaround is available. An erratum is said to have a minor impact if it results in slight to moderate performance degradation or is a functional variance from the specification. Application of the workaround eliminates the problem.
Published Date:	16 May 2014
Applies To:	POWER8 Processor SCM
Status:	No fix is planned.

Description

This erratum is triggered when all of the following conditions are met:

1. Two `cop_req1` commands for the same NX coprocessor type (CT) are received in the same cycle on NX ports `rcmd0` and `rcmd1`.
2. The destination CT engines and the DMA channels servicing those engines are busy with older jobs so the NX processor bus interface (PBCQ) uses at least one floating queue slot to store one of the received `cop_req` CRBs.
3. A CRB Kill ISN or LPID is issued and hits the more recent job in a floating queue.

This erratum can cause the job in the floating queue to be reported as both killed and also completed. A job should be reported as killed or completed, but not both. The erratum can also cause an arbitrary job to be executed twice, either on the same or a different CT.

Workarounds

The workaround is to align CRBs on 256-byte boundaries. This forces all `cop_req` to the NX `rcmd0` port. Therefore, trigger condition 1 cannot occur. The PHYP already aligns CRBs on 4 KB boundaries, so there is no impact.

1. A `cop_req` is the processor bus command that results from an **icswx**. instruction. It has a 128-byte operand called a CRB that is pushed to the NX some time after the `cop_req` command is issued to the bus.

Erratum #3

Abstract:	Incorrect data during scrub and steer cleanup with <u>UE</u> trap mode enabled.
Impact:	Category 5. Minor impact; workaround is available. An erratum is said to have a minor impact if it results in slight to moderate performance degradation or is a functional variance from the specification. Application of the workaround eliminates the problem.
Published Date:	16 May 2014
Applies To:	POWER8 Memory Buffer
Status:	No fix is planned.

Description

When performing a scrub or steer cleanup maintenance command while UE trap mode is enabled, the write back data is incorrect.

Note: IBM hardware procedures only enable UE trap mode during the Superfast Read command that is used during IPL memory diagnostics. This traps the actual UE data so that it can be compared to the known pattern that was written to identify which bits contributed to the UE. UE trap mode is not used during normal run-time operation.

Workarounds

Do not enable UE trap mode when performing scrub or steer cleanup operations.

Erratum #4

Abstract:	Cfam_reset after V _{IO} power on does not trigger selfboot.
Impact:	Category 5. Minor impact; workaround is available. An erratum is said to have a minor impact if it results in slight to moderate performance degradation or is a functional variance from the specification. Application of the workaround eliminates the problem.
Published Date:	16 May 2014
Applies To:	POWER8 Processor SCM
Status:	No fix is planned.

Description

In a selfboot environment, the SCAN0 in ClockControl is not triggered after cfam_reset_b.

Workarounds

After a cfam_reset, a manual trigger is required. This is done by providing the appropriate pattern at the flexible service interface (FSI).

Erratum #5

Abstract:	Multithreaded <u>XSCOM</u> causes a false Done and delayed error handling.
Impact:	Category 5. Minor impact; workaround is available. An erratum is said to have a minor impact if it results in slight to moderate performance degradation or is a functional variance from the specification. Application of the workaround eliminates the problem.
Published Date:	16 May 2014
Applies To:	POWER8 Processor SCM
Status:	No fix is planned.

Description

During XSCOM operations, both of the following events can occur:

- The XSCOM error status on thread0 is delayed by one cycle relative to Done.
- Multithreaded XSCOMs can cause a false Done indication on thread0 HMER.

Workarounds

The workaround involves two steps:

1. Read the HMER a second time after Done to get the correct status.
2. Ensure that there is a single-threaded XSCOM on a per-core level via a software mutex.

Erratum #6

Abstract:	Certain software sequences result in ignored <u>PMU</u> interrupts.
Impact:	Category 5. Minor impact; workaround is available. An erratum is said to have a minor impact if it results in slight to moderate performance degradation or is a functional variance from the specification. Application of the workaround eliminates the problem.
Published Date:	16 May 2014
Applies To:	POWER8 Processor SCM
Status:	No fix is planned.

Description

PMU interrupts are raised to the core through an internal latch that is asserted exclusively when either of the following events occurs:

- PMC1 overflows while MMCR0[PMAE] and MMCR0[PMC1CE] are enabled.
- At least one of PMC2 - PMC6 overflows while MMCR0[PMAE] and MMCR0[PMCjCE] are enabled.

The following four sequences fail to produce a PMU interrupt:

1. PMC1 is negative, followed by both MMCR0[PMAE] and MMCR0[PMC1CE] being enabled, in any order.
2. At least one of PMC2 - PMC6 is negative, followed by both MMCR0[PMAE] and MMCR0[PMCjCE] being enabled, in any order.
3. Both MMCR0[PMAE] and MMCR0[PMC1CE] are enabled, followed by software writing a negative value to PMC1.
4. Both MMCR0[PMAE] and MMCR0[PMCjCE] are enabled, followed by software writing a negative value to at least one of PMC2 - PMC6.

Workarounds

All three of the following actions must be taken to work around the erratum:

1. Before enabling random sampling (by asserting MMCR0[PMAE] and at least one of MMCR0[PMC1CE] or MMCR0[PMCjCE]), clear the PMCs.
2. Do not write negative values to any of the PMCs outside of save/restore routines.
3. Before performing a PMU state restore, check MMCR0 and the PMC values captured by the save routine.

Note: This step assumes that the previous state of the PMU was saved as copies of the PMC_n , MMCR0, SIER, SIAR, SDAR, and MMCR2 registers that will be restored.

If either of the following conditions is true, follow the *Workaround Sequence* on page 13 while the External Interrupt Enable (MSR[EE]) bit is 0. Otherwise, follow the normal restore routine.

- PMC1 is negative, MMCR0[PMAO] is clear, and both MMCR0[PMAE] and MMCR0[PMC1CE] are enabled.

- At least one of PMC2 - PMC6 is negative, MMCR0[PMAO] is clear, and both MMCR0[PMAE] and MMCR0[PMCjCE] are enabled.

Workaround Sequence

1. Write 0x000000006004100 to MMCR0 (the actual register, not the saved copy).
2. Write 0x0000000000000000 to MMCR2 (the actual register, not the saved copy).
3. Write 0x7FFFFFFF to PMC6 (the actual register, not the saved copy).
4. Restore the saved copies of the PMCs.
5. Restore the saved copies of SIER, SIAR, and SDAR.
6. Restore the saved copy of MMCR2.
7. Restore the saved copy of MMCR0.
8. Continue.

This sequence checks for a counter negative condition on the running thread. If there is one, instead of restoring the negative PMC with MMCR0[PMAO] set to zero and ignoring the interrupt, it forces a new interrupt on PMC6. Thus, when this hypervisor sequence returns and the EE bit is restored to 1, the hardware takes the new interrupt using the restored data as if it was the original counter negative condition before random sampling was enabled.

Erratum #7

Abstract:	Micropartition prefetch incompatible with 2 <u>LPAR</u> and 4 LPAR mode.
Impact:	Category 5. Minor impact; workaround is available. An erratum is said to have a minor impact if it results in slight to moderate performance degradation or is a functional variance from the specification. Application of the workaround eliminates the problem.
Published Date:	16 May 2014
Applies To:	POWER8 Processor SCM
Status:	No fix is planned.

Description

The micropartition prefetch mechanism does not perform the desired partition data prefetch in 2 LPAR or 4 LPAR mode.

In 2 LPAR or 4 LPAR mode, incomplete and or excessive prefetching can occur. If a micropartition prefetch is performed in 2 LPAR or 4 LPAR mode, prefetch state machines are left in a state that makes them unavailable for subsequent data prefetch operations.

The micropartition prefetch mechanism functions correctly only in 1 LPAR mode.

Workarounds

System partition management software must not activate micropartition prefetch through the MPPR register if the POWER8 processor is running in 2 LPAR or 4 LPAR mode.

Erratum #8

Abstract:	During a <u>PMU</u> state save routine, MMCR0[PMAO] and MMCR0[PMAE] are inconsistent for one cycle on every counter overflow while exceptions are enabled.
Impact:	Category 5. Minor impact; workaround is available. An erratum is said to have a minor impact if it results in slight to moderate performance degradation or is a functional variance from the specification. Application of the workaround eliminates the problem.
Published Date:	16 May 2014
Applies To:	POWER8 Processor SCM
Status:	No fix is planned

Description

PMU interrupts are raised to the core through an internal latch that is asserted exclusively when either of the following events occurs:

- PMC1 overflows while MMCR0[PMAE] and MMCR0[PMC1CE] are enabled.
- At least one of PMC2 - PMC6 overflows while MMCR0[PMAE] and MMCR0[PMCjCE] are enabled.

It takes one cycle for MMCR0[PMAO] to be set and MMCR0[PMAE] to be cleared after the overflow happens. It is possible for software to read MMCR0 in this inconsistent state at the time of a PMU state save routine and potentially drop the pending interrupt.

Workaround

Before performing a PMU state restore, check MMCR0 and the PMC values captured by the save routine.

Note: This workaround assumes that the previous state of the PMU was saved as copies of the PMC_n , MMCR0, SIER, SIAR, SDAR, and MMCR2 registers that will be restored.

If either of the following conditions is true, follow the *Workaround Sequence* on page 15 while the External Interrupt Enable (MSR[EE]) bit is 0. Otherwise, follow the normal restore routine.

- PMC1 is negative, MMCR0[PMAO] is clear, and both MMCR0[PMAE] and MMCR0[PMC1CE] are enabled.
- At least one of PMC2 - PMC6 is negative, MMCR0[PMAO] is clear, and both MMCR0[PMAE] and MMCR0[PMCjCE] are enabled.

Workaround Sequence

1. Write 0x000000006004100 to MMCR0 (the actual register, not the saved copy).
2. Write 0x0000000000000000 to MMCR2 (the actual register, not the saved copy).
3. Write 0x7FFFFFFF to PMC6 (the actual register, not the saved copy).
4. Restore the saved copies of the PMCs.
5. Restore the saved copies of SIER, SIAR, and SDAR.

6. Restore the saved copy of MMCR2.
7. Restore the saved copy of MMCR0.
8. Continue.

This sequence checks for a counter negative condition on the running thread. If there is one, instead of restoring the negative PMC with MMCR0[PMAO] set to zero and ignoring the interrupt, it forces a new interrupt on PMC6. Thus, when this hypervisor sequence returns and the EE bit is restored to 1, the hardware takes the new interrupt using the restored data as if it was the original counter negative condition.

Erratum #9

Abstract:	All <u>PMU</u> events that measure reload latency (PM_MRK_DATA_FROM_*_CYC) overcount the latency of marked noncacheable loads.
Impact:	Category 4. Minor impact; no workaround available. An erratum is said to have a minor impact if it results in slight to moderate performance degradation or is a functional variance from the specification.
Published Date:	10 March 2015
Applies To:	POWER8 Processor SCM
Status:	No fix is planned.

Description

Marked reload-source cycle events are intended to count cycles from the time a marked L1 miss is reported until the time the corresponding reload arrives at the core. An internal latch is set when the marked L1 miss occurs, and it is cleared when the reload occurs. However, for noncacheable loads, this latch does not get cleared at reload time. The latch remains set until the next marked reload occurs. This results in overcounting for the following events whenever noncacheable loads are eligible for marking with either random instruction sampling or random event sampling.

PM_MRK_DATA_FROM_DL2L3_MOD_CYC
 PM_MRK_DATA_FROM_DL2L3_SHR_CYC
 PM_MRK_DATA_FROM_DL4_CYC
 PM_MRK_DATA_FROM_DMEM_CYC
 PM_MRK_DATA_FROM_L2_1_MOD_CYC
 PM_MRK_DATA_FROM_L2_1_SHR_CYC
 PM_MRK_DATA_FROM_L2_CYC
 PM_MRK_DATA_FROM_L2_DISP_CONFLICT_LD_HITST_CYC
 PM_MRK_DATA_FROM_L2_DISP_CONFLICT_OTHER_CYC
 PM_MRK_DATA_FROM_L2_MEPF_CYC
 PM_MRK_DATA_FROM_L2_MISS_CYC
 PM_MRK_DATA_FROM_L2_NO_CONFLICT_CYC
 PM_MRK_DATA_FROM_L3_1_ECO_MOD_CYC
 PM_MRK_DATA_FROM_L3_1_ECO_SHR_CYC
 PM_MRK_DATA_FROM_L3_1_MOD_CYC
 PM_MRK_DATA_FROM_L3_1_SHR_CYC
 PM_MRK_DATA_FROM_L3_CYC
 PM_MRK_DATA_FROM_L3_DISP_CONFLICT_CYC
 PM_MRK_DATA_FROM_L3_MEPF_CYC
 PM_MRK_DATA_FROM_L3_MISS_CYC
 PM_MRK_DATA_FROM_L3_NO_CONFLICT_CYC
 PM_MRK_DATA_FROM_LL4_CYC
 PM_MRK_DATA_FROM_LMEM_CYC
 PM_MRK_DATA_FROM_MEMORY_CYC
 PM_MRK_DATA_FROM_OFF_CHIP_CACHE_CYC
 PM_MRK_DATA_FROM_ON_CHIP_CACHE_CYC
 PM_MRK_DATA_FROM_RL2L3_MOD_CYC

PM_MRK_DATA_FROM_RL2L3_SHR_CYC
PM_MRK_DATA_FROM_RL4_CYC
PM_MRK_DATA_FROM_RMEM_CYC
PM_MRK_LD_MISS_EXPOSED_CYC
PM_MRK_LD_MISS_L1_CYC

To estimate the reliability of these latency events, the following two events can be counted for the application of interest. The sum of these events shows the total number of unmarked noncacheable loads. A high value indicates probable inaccuracies for the latency events.

- PM_LSU0_NCLD
- PM_LSU1_NCLD

Workaround

No workaround is available.

Erratum #10

Abstract:	The X-Bus is disabled on all OpenPOWER POWER8 Processor SCMs manufactured after 1 May 2015. If older versions of firmware are executed on POWER8 Processor SCMs manufactured after this date with the X-Bus disabled, the POWER8 Processor SCM will fail to boot and error messages will be displayed.
Impact:	Category 3. Major impact; workaround available. Application of the workaround either eliminates the problem, or reduces it to a minor impact issue.
Published Date:	4 May 2015
Applies To:	POWER8 Processor SCM
Status:	No fix is planned.

Description

All OpenPOWER POWER8 Processor SCMs manufactured after 1 May 2015 will be produced with the X-bus disabled. OpenPOWER systems do not use the X-Bus so there is no loss of function.

To use the new modules produced after 1 May 2015, the user must acquire and use a new level of the hostboot. If older firmware levels are executed on modules that have the X-Bus disabled, the firmware reports an error on the host serial console:

```
| Error reported by xscom (0x0400)
| XSCom access error
| ModuleId 0x07 XSCOM_DO_OP
| ReasonCode 0x0401 XSCOM_STATUS_ERR
| UserData1 HMER value (piberr in bits 21:23) : 0x00c0030000000000
| UserData2 XSCom address : 0x0000000040000020
```

The address (40000020) corresponds to an access to the unused X-Bus unit on the POWER8 SCM module.

Workaround

This issue is fixed by the firmware levels in op-build v1.1 or above:

<https://github.com/open-power/op-build/releases/tag/v1.1>

The issue can also be fixed on older firmware levels by manually applying the following fix to the hostboot firmware component:

<https://github.com/open-power/hostboot/commit/a0f4a934254572ce49a1ddf5e4d5d944b52779be>





Revision Log

Each release of this document supersedes all previously released versions. The revision log lists all significant changes made to the document since its initial release. In the rest of the document, change bars in the margin indicate that the adjacent text was modified from the previous release of this document.

Revision Date	Description
5 May 2015	Version 1.2. Updated <i>Table 2 Summary of Errata</i> on page 4. Added <i>Erratum #10</i> on page 19.
10 March 2015	Version 1.1. Updated <i>Table 2 Summary of Errata</i> on page 4. Added <i>Erratum #9</i> on page 17.
16 May 2014	Version 1.0 (initial release).