



POWER8 Processor Registers Specification

15 June 2016
Version 1.2



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Revision Log

Each release of this document supersedes all previously released versions. The revision log lists all significant changes made to the document since its initial release.

Version	Revision Date	Description
1.2	15 June 2016	Added Overview section. Added PSIHB registers.
1.1	6 January 2016	Added the following registers: I2CS Configuration Register (EH.TPCHIP.PIB.I2CS.TP_I2CS_COMP.I2CSCONFIG) I2CS Status Register (EH.TPCHIP.PIB.I2CS.TP_I2CS_COMP.I2CSSTATUS) I2CS Error Register (EH.TPCHIP.PIB.I2CS.TP_I2CS_COMP.I2CSERRORS)
1.0	31 July 2014	Initial Release.

About this Document

This document describes the IBM® POWER8® registers used by the POWER8 processor. These registers are referred to as POWER8 registers. Throughout this document, the term “processor” refers to the POWER8 processor and “memory buffer” refers to the POWER8 memory buffer.

To ensure you have the most current version of this document, contact your IBM technical representative or visit the [OpenPOWER Connect](#) website.

Who Should Read this Document

This manual is intended for system software and hardware developers and application programmers who want to develop products for the POWER8 processor. It is assumed that the reader understands operating systems, microprocessor system design, basic principles of reduced instruction set computer (RISC) processing, and details of the Power ISA.

Representation of Numbers

Numbers are generally shown in decimal format, unless designated as follows:

- Hexadecimal values are usually preceded by “0x.”
For example: 0x000000000204000D
- Binary values in sentences are usually preceded by “0b.”
For example: 0b1

Note: A bit value that is immaterial, which is called a “don't care” bit, is represented by an “X” or “x.”

Bit Significance

In the POWER8 documentation, the smallest bit number represents the most significant bit of a field, and the largest bit number represents the least significant bit of a field.

Organization

The table of contents shows the major sections of the document. Address maps within each section list the registers in alphabetical order by mnemonic. The registers themselves are arranged by their addresses. A register can have multiple addresses with a different addresses for different units. The types of access permitted can vary by unit.

Terminology

For definitions of the acronyms and abbreviations used in this document, see the *Glossary* on page 20.

Related Documents

The following documents can be helpful when reading this specification. They are available through [OpenPOWER Connect](#).

POWER8 Processor User's Manual for the Single-Chip Module

POWER8 Processor Single-Chip Module Datasheet

POWER8 Processor Common Registers Specification

POWER8 Memory Buffer Datasheet

POWER8 Memory Buffer User's Manual

POWER8 Memory Buffer Registers Specification

Power ISA User Instruction Set Architecture - Book I (Version 2.07)

Power ISA Virtual Environment Architecture - Book II (Version 2.07)

Power ISA Operating Environment Architecture (Server Environment) - Book III-S (Version 2.07)

1. Overview

The POWER8 processor is a superscalar symmetric multi-processor (SMP) designed for use in servers and large cluster systems. It uses IBM's complementary metal-oxide semiconductor (CMOS) 22 nm silicon-on-insulator (SOI) technology with 15 metal layers. The POWER8 processor can have up to 12 cores enabled on a single chip in the single-chip module (SCM) configuration. Each core has eight threads using simultaneous multithreading (SMT). The SMT is dynamically tunable, so that each core can have one, two, four, or eight threads.

The IBM POWER8 memory buffer supports multiple system configurations. It uses a high-speed differential interface to communicate with a processor chip using a memory-agnostic protocol. The memory controller and associated memory-interface maintenance and calibration functions are initiated and contained within the memory buffer chip. The buffer also contains a 16 MB on-board cache to support prefetching and improve system performance.

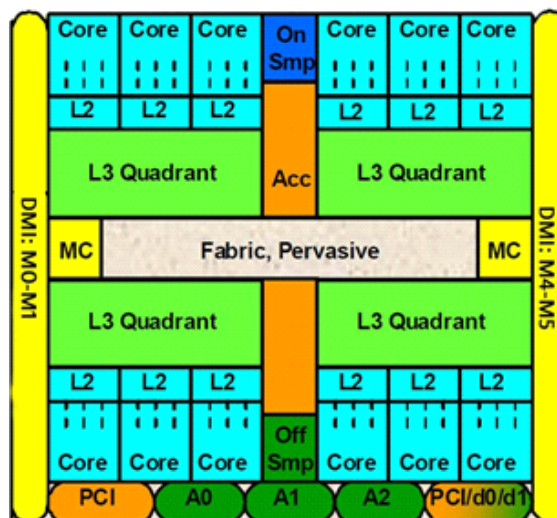
This document describes the POWER8 registers and related accessing method. Throughout this document, the term “processor” refers to POWER8 processor.

1.1 POWER8 Processor

Figure 1: POWER8 Processor General Diagram shows the POWER8 processor, consisting of the following main components:

- Up to twelve POWER8 chiplets which contain:
 - A POWER8 core
 - An L2 cache
 - An L3 cache
- One on-chip accelerator engine
- Two memory controllers that support the POWER8 memory buffer chip
- A processor bus interconnect
- The interface controllers support the following interfaces:
 - Four differential memory interface (DMI) buses (M0-1 and M4-5)
 - Three inter-node SMP buses (A0 – A2)
 - 32 lanes of configurable PCIe 3.0 buses (two x16 or one x16 and two x8)
- Pervasive functions including support for FSI, I²C, LPC, SPI and other interfaces

Figure 1: POWER8 Processor General Diagram



1.2 POWER8 Processor Pervasive

Figure 2 shows the POWER8 chip from a pervasive centric point of view. Different colors denote different frequency domains. The chip contains twelve cores capable of running at different frequencies. The pervasive logic is built to support a seamless extension to sixteen cores.

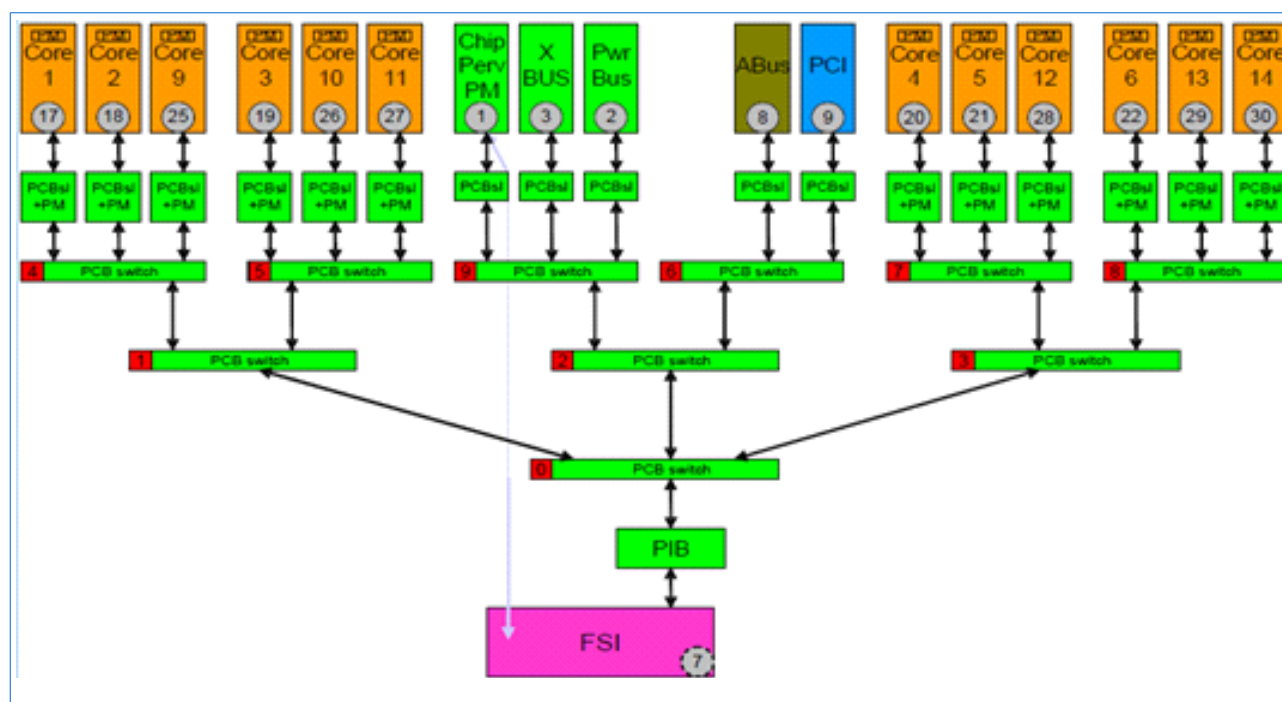
[illegible]

The Pervasive Control Bus (PCB) provides a generic, modular structure for communication between the pervasive elements. The PCB provides the POWER8 pervasive with an interface to the pervasive functions on the various POWER8 processor chiplets. For this purpose, a PCB master is implemented inside the

POWER8 pervasive logic. This master, by means of the PCB interconnect, can communicate with the PCB slave located in each chiplet. The PCB master can send commands, such as read and write requests, to the PCB slaves. The slaves, on the other hand, can respond to the commands received from the master, and can also notify the master of interrupts that occur in the slave's chiplet.

Figure 3 on page 10 shows the PCB structure that services all the chiplets (at the top of the picture) from the service element (FSI).

Figure 3: Pervasive Control Bus Structure and Chiplets



The PCB switch features two independent channels for the PCB topology. The downstream input channel provides a fan-out to the downstream output ports, which are connected either to another switch in a multistage topology or directly to a slave. The upstream output channel is arbitrated between requests from the upstream input ports, which is the case when replying to a multicast operation.

The Pervasive Interconnect Bus (PIB) provides access from the masters via external interfaces (JTAG, I²C slave, and FSI) and internal masters Power On Reset Engine (PORE), FSI shift engine, FSI2PIB, XSCOM/ Alter-Display Unit (ADU)) to common PIB attached slaves (PCB Master, PIB2OPB, general-purpose register (GPR) register, I²C master, I²C slave). The PIB bus facilitates transaction between multiple PIB masters and multiple PIB slaves. For each transaction, the PIB arbiter establishes a point-to-point connection between a single requesting master and a single slave uniquely addressed by the master.

1.2.2 PCB Address Space

Figure 4: Common Pervasive Address Map Format shows the address format used to access all pervasive facilities. The legacy 32-bit format is shown as well as the translation in the new 64-bit format (add 32 zeros as the most significant bits). The new extended address format that enables access to the large address SCOM satellites (up to 31 bits) is also listed. The most significant bit is '1' in that case.

Figure 4: Common Pervasive Address Map Format

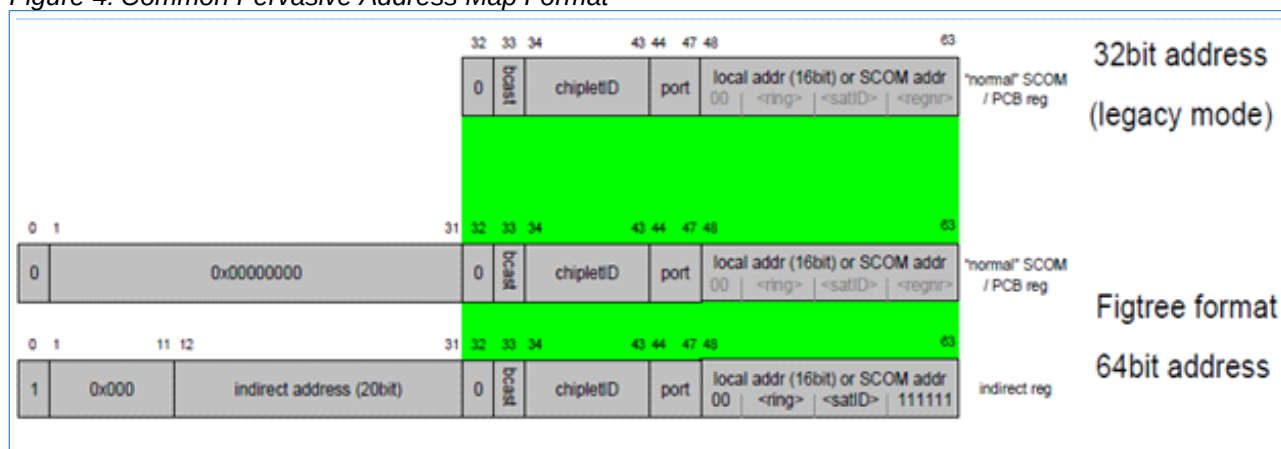


Table 1 lists the chiplets in the design and their controlling pervasive blocks. It also lists the address map to access all these components on the PCB.

Table 1: PCB Address Description

Chiplet Name	Description	Block	PCB Address
PERV	Chip Pervasive Logic (TP, PIB, OCC)	<LBUS FSI reserved>	0x0000xxxx
		OTPROM	0x0001xxxx
		MFSI0	0x0002xxxx
		MFSI1	0x0003xxxx
		TOD	0x0004xxxx
		MBOX	0x0005xxxx
		OCB	0x0006xxxx
		SPIADC	0x0007xxxx
		PIBMEM	0x0008xxxx
		<reserved>	0x0009xxxx
		I2CMS PROM	0x000A00(0:1)x
		I2CMS PCI/TPM	0x000A00(2:3)x
		LPCM	0x000Bxxxx
		ECCAX	0x000Cxxxx
		<reserved>	0x000Dxxxx
		SBE	0x000Exxxx
		PCBMS	0x000Fxxxx
		GPIO	0x0100xxxx
		SCOM	0x0101xxxx
		<reserved>	0x0102xxxx
		CLOCK CTL	0x0103xxxx
		FIR	0x0104xxxx
		<reserved>	0x010(5:E)xxxx
		PCB SLAVE	0x010Fxxxx
NEST (PB)	Processor Bus Pervasive Logic	GPIO	0x0200xxxx
		SCOM	0x0201xxxx
		ADU	0x0202xxxx
		CLOCK CTL	0x0203xxxx
		FIR	0x0204xxxx
		<reserved>	0x0205xxxx -- 0x020Exxxx
		PCB SLAVE	0x020Fxxxx
<reserved>	<reserved>	<reserved>	0x0(3:7)xxxxxx



Chiplet Name	Description	Block	PCB Address
ABUS	A Fabric Pervasive Logic	GPIO	0x0800xxxx
		SCOM	0x0801xxxx
		<reserved>	0x0802xxxx
		CLOCK CTL	0x0803xxxx
		FIR	0x0804xxxx
		THERM	0x0805xxxx
		<reserved>	0x0806xxxx -- 0x080Exxxx
		PCB SLAVE	0x080Fxxxx
PCIE	PCI-Express Bus Pervasive Logic	GPIO	0x0900xxxx
		SCOM	0x0901xxxx
		<reserved>	0x0902xxxx
		CLOCK CTL	0x0903xxxx
		FIR	0x0904xxxx
		<reserved>	0x0906xxxx -- 0x090Exxxx
		PCB SLAVE	0x090Fxxxx
<EX0 reserved>	<reserved>	<reserved>	0x100xxxxx
EX1 (Core)	EX Pervasive Logic	GPIO	0x1100xxxx
		SCOM	0x1101xxxx
		OHA	0x1102xxxx
		CLOCK CTL	0x1103xxxx
		FIR	0x1104xxxx
		THERM	0x1105xxxx
		<reserved>	0x1106xxxx -- 0x110Exxxx
		PCB SLAVE	0x110Fxxxx
EX2 (Core)	EX Pervasive logic	See EX1	0x120xxxxx
EX3 (Core)	EX Pervasive logic	See EX1	0x130xxxxx
EX4 (Core)	EX Pervasive logic	See EX1	0x140xxxxx
EX5 (Core)	EX Pervasive logic	See EX1	0x150xxxxx
EX6 (Core)	EX Pervasive logic	See EX1	0x160xxxxx
<EX7,8 reserved>	<reserved>	<reserved>	0x1(7:8)0xxxxx
EX9 (Core)	EX Pervasive logic	See EX1	0x190xxxxx
EX10 (Core)	EX Pervasive logic	See EX1	0x1A0xxxxx
EX11 (Core)	EX Pervasive logic	See EX1	0x1B0xxxxx
EX12 (Core)	EX Pervasive logic	See EX1	0x1C0xxxxx

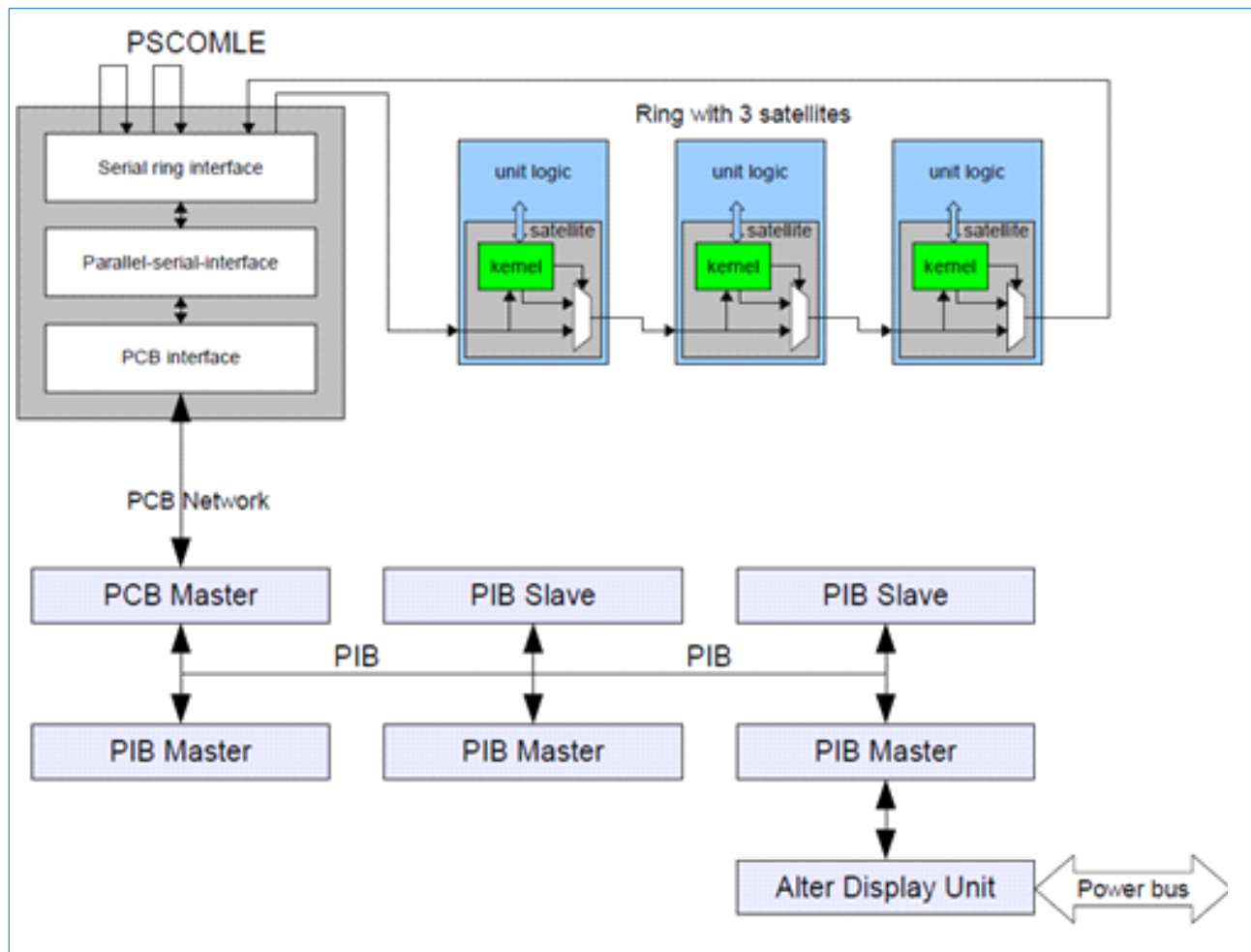
Chiplet Name	Description	Block	PCB Address
EX13 (Core)	EX Pervasive logic	See EX1	0x1D0xxxxx
EX14 (Core)	EX Pervasive logic	See EX1	0x1E0xxxxx
<EX15 reserved>	<reserved>	<reserved>	0x1F0xxxxx

1.3 SCOM

SCOM provides a serial communication infrastructure within the pervasive infrastructure. The central control unit is referred to as PSCOMLE. It controls all communication with respect to the serial interface. The end-point nodes are referred to as satellites. A satellite is located in the unit logic. The satellites are connected to PSCOMLE and each other in a physical ring. PSCOMLE can support up to 15 rings. Each ring has a local address space that is used to address an individual satellite in a given ring and within the unit logic that uses the satellite with a dedicated register. If this address space is not sufficient, an indirect address can be used to further extend the address range within a satellite.

Figure 5 shows the principal pervasive infrastructure to access the SCOM-enabled registers in a chiplet. A SCOM access can be initiated either from the masters connected to the PIB or via the Alter/Display unit (ADU). SCOM satellites are distributed inside the chiplet and are organized in serial SCOM rings. For each chiplet, there is one instance of the PSCOMLE macro that receives the request from the PCB network.

Figure 5: Infrastructure to Access SCOM Registers

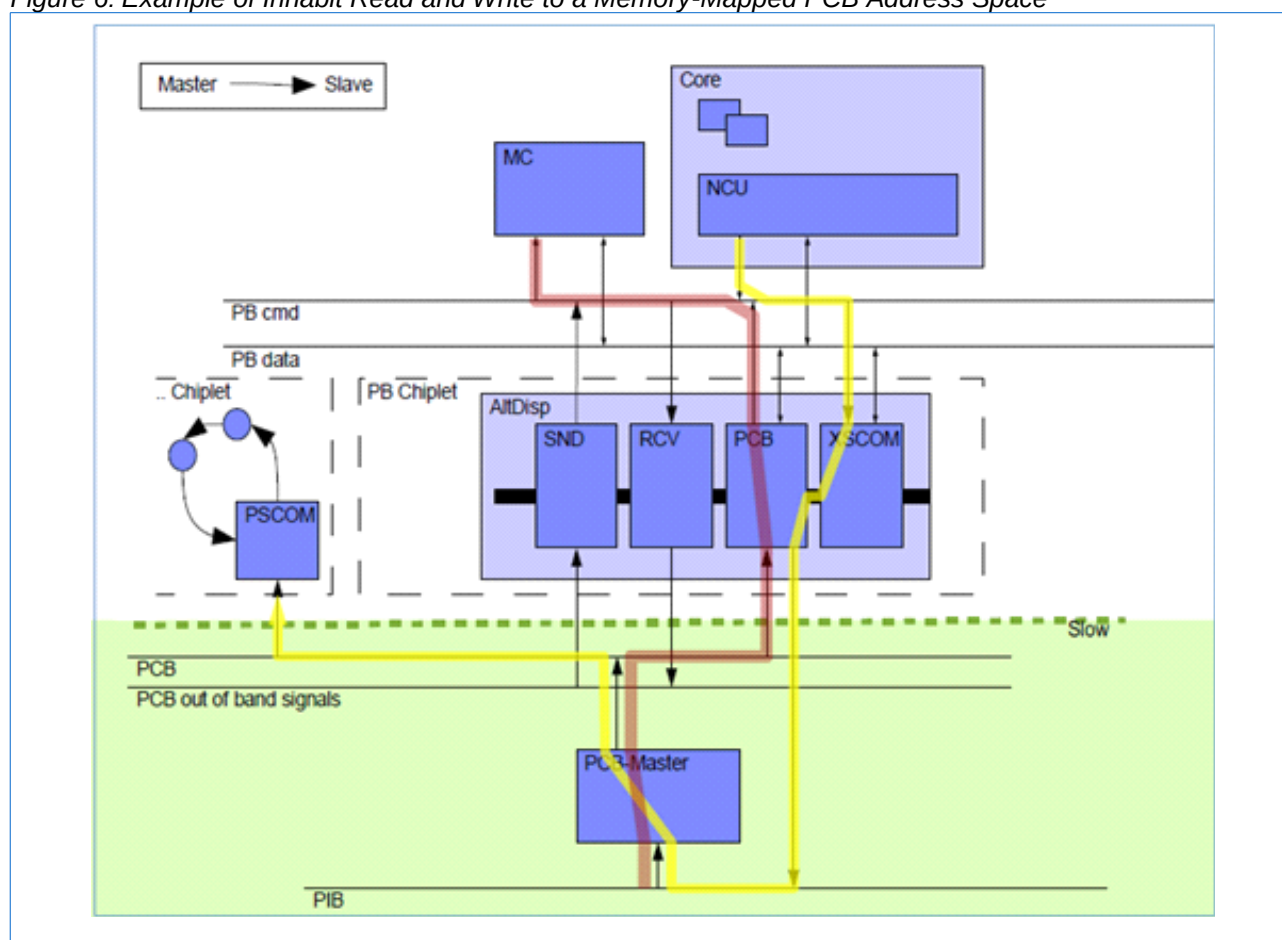


1.4 XSCOM

The Alter/Display Unit acts as a bridge between the processor bus and the PCB. The ADU enables access to any memory-mapped PIB/PCB register in the system by external SCOM (XSCOM.) The XSCOM is responsible for handling memory-mapped PIB/PCB register access, which originates from the non-pervasive logic of the processor. For example, a read/write operation can originate from a processor core and is presented on the processor bus by the non-cacheable unit (NCU). The Alter/Display Unit XSCOM routes the request through a PIB master to the PIB. The PIB master notifies the ADU when it is complete. For a read operation, the ADU routes the resulting data to the processor bus which sends the information back to the requestor (in the example, the NCU) and then it finally arrives at the core. The XSCOM memory-mapped address range by default locates at 0x0003FC0000000000.

Figure 6 shows an example of an inhibit read and write to a memory-mapped PCB address space.

Figure 6: Example of Inhibit Read and Write to a Memory-Mapped PCB Address Space



1.5 Register Accessing Type

A register can have multiple addresses with a different address for different chiplets. The types of access permitted can vary by chiplets. The *Table 2* summarizes the valid register access types.

Table 2: Register Access Types

Access Type	Description
RW	Readable and writable.
RW_WOR	Readable and writable. A write ORs written data with existing data and stores the result.
RW_WAND	Readable and writable. A write ANDs written data with existing data and stores the result.
RW_WCLEAR	Readable and writable. A write of a '1' clears the bit. A write of a '0' does nothing.
RW_WCLRPART	Readable and writable. Any write to the address clears the bits regardless of the value.



Access Type	Description
RW_WSETPART	Readable and writable. Any write to the address sets the bits regardless of the value.
WO	Same as RW, but bits are write-only.
WO_OR	Same as RW_WOR, but bits are write-only.
WO_AND	Same as RW_WAND, but bits are write-only.
WO_CLEAR	Same as RW_WCLEAR, but bits are write-only.
WO_CLRPART	Same as RW_WCLRPART, but bits are write-only.
WO_SETPART	Same as RW_WSETPART, but bits are write-only.
WO_nP	Write-only pulsed. A write of '1' creates a pulse for n register clocks. A read returns '0'.
WO_n_mP	Write-only pulsed. A write of '1' creates a pulse for a minimum of n register clocks and a maximum of m register clocks. A read returns '0'.
RO	Read only. Only to be used if a bit is tied. Status bits should be ROX.
NC	Not connected; that is, the data cannot be written or read by that access.
RWX	Same as RW, but unstable. Can be changed functionally.
RWX_WOR	Same as RW_WOR, but unstable. Can be changed functionally.
RWX_WAND	Same as RW_WAND, but unstable. Can be changed functionally.
RWX_WCLEAR	Same as RW_WCLEAR, but unstable. Can be changed functionally.
RWX_WCLRPART	Same as RW_WCLRPART, but unstable. Can be changed functionally.
RWX_WSETPART	Same as RW_WSETPART, but unstable. Can be changed functionally.
WOX	Same as WO, but unstable. Can be changed functionally.
WOX_OR	Same as WO_OR, but unstable. Can be changed functionally.
WOX_AND	Same as WO_AND, but unstable. Can be changed functionally.
WOX_CLEAR	Same as WO_CLEAR, but unstable. Can be changed functionally.
WOX_CLRPART	Same as WO_CLRPART, but unstable. Can be changed functionally.
WOX_SETPART	Same as WO_SETPART, but unstable. Can be changed functionally.
WOX_nP	Same as WO_nP, but unstable. Can be changed functionally.
WOX_n_mP	Same as WO_n_mP, but unstable. Can be changed functionally.
ROX	Same as RO, but unstable. Can be changed functionally.
ROX_CLRPART	Same as ROX, but a read access will clear the bits after they have been accessed.
NCX	Same as NC, but unstable. Can be changed functionally.



2. Glossary

ABIST	Array built-in self test
AC	Alternating current
ACK	Acknowledgment or acknowledge
AMux	Analog multiplexer
AND write	Current register content is ANDed with write data and the result is stored in the register (access type WO_AND / WOX_AND).
ARE	Address error
ARY	Array
ATPG	Advanced test pattern generator
AVP	Architectural verification program
BCDE	Block copy download engine
BCUE	Block copy upload engine
BI	Burn in
BNDY	Boundary I/Os
BYPASSN	Bypass low active
CC	Congruence class
cmd	Command
cMFSI	Cascade master FSI
CMSK	LBIST channel mask
CP	Chip pump

CPS	Cycle-per-step
CRC	Cyclic-redundancy check
DCM	Dual-chip module
diag	Diagnostic
DMA	Direct memory access
DPLL	Digital phase-locked loop
DRAM	Dynamic random access memory
DSMP	Distributed symmetric multiprocessing
ECC	Error correction code
eDRAM	Embedded dynamic random-access memory
EH	Exclusive access hint
FARR	Fast array unload
fb	Feedback
fbclk	Feedback clock
FIFO	First-in, first-out
FIR	Fault isolation register
fmax	Maximum frequency
fmin	Minimum frequency
FSI	Flexible service interface. FSI covers all resources except FSI slave 0 and slave 1, when addressed from an external service element via the FSI interface.
FSI_BYTE	Flexible service interface byte. FSI_BYTE describes a special byte addressing mode of the FSP.

FSI0	Flexible service interface 0. FSI0 covers resources located in FSI slave 0, when addressed from an external service element via the FSI interface.
FSI1	Flexible service interface 1. FSI1 covers resources located in FSI slave 1, when addressed from an external service element via the FSI interface.
FSM	Finite state machine
Full write	Current register content is replaced by new write data (access type RWX).
func	Functional
GB	Gigabyte
GPIO	General-purpose input/output
GPR	General-purpose register
GPTR	General-purpose test register
HCA	Hot/cold affinity
I2C	Inter-integrated circuit
I2CM	Inter-integrated circuit master
I2CS	Inter-integrated circuit slave
ICP	Interrupt control presenter
IF	Interface
INTP	Interrupt presenter
LBIST	Logical built-in self test
LCB	Log-on control block or local clock buffer
LPC	Low pin count, lowest point of coherency
MC	Memory channel, memory controller

MCD	Memory coherency directory
MFSI	Master FSI
MISR	Multiple input shift register
MSB	Most-significant byte
NACK	Negative acknowledgment
NC	Not connected; that is, the data cannot be written or read by that access.
NCX	Same as NC, but unstable (can be changed functionally)
NOP	No operation
NX	Nest accelerator
OCC	On-chip controller
OCI	On-chip-controller interface. Interface used by power management.
OPB	On-chip peripheral bus
OPCG	On-product clock generator
OR write	Current register content is ORed with write data and the result is stored in the register (access type WO_OR / WOX_OR).
OSC	Oscillator
OSCSW	Oscillator switch
OTPROM	One-time programmable read-only memory
PB	Processor bus
Pb	Lead
PBA	Power management processor bus interface
PCB	Pervasive control bus. PCB is used for read and full write access.

PCB1	Pervasive control bus 1. PCB1 is used for AND write access.
PCB2	Pervasive control bus 2. PCB2 is used for OR write access.
PCBIF	Pervasive control bus interface
PCI	Peripheral Component Interface
PCle	Peripheral Component Interface Express
PCIEX	Peripheral Component Interface Express
PCLK	Processor clock
PERV	Pervasive
PIB	Pervasive interconnect bus. PIB is used for read and full write access.
PIB1	Pervasive interconnect bus. PIB1 is used for AND write access.
PIB2	Pervasive interconnect bus. PIB2 is used for OR write access.
PLL	Phase-locked loop
PLLREG	Phase-locked loop register
PMC	Performance monitor counter, power management control
PRPG	Pseudo-random pattern generator
PSI	Processor support interface
PSRO	Performance sort-ring oscillator
RDDACK	Read acknowledgment
RDIV	Reference clock divide
Refclk	Reference clock

REGF	Register file
REPR	Array repair
RO	Read only. Only used if a bit is tied. Status bits should be ROX.
ROM	Read-only memory
ROX	Same as RO, but unstable. Can be changed functionally.
ROX_CLRPART	Same as ROX, but a read access will clear the bits after they have been accessed.
RW	Readable and writable
RW_WAND	Readable and writable. A write ANDs written data with existing data and stores the result.
RW_WCLEAR	Readable and writable. A write of a '1' clears the bit. A write of a '0' does nothing.
RW_WCLRPART	Readable and writable. Any write to the address clears the bits regardless of value.
RW_WOR	Readable and writable. A write ORs written data with existing data and stores the result.
RW_WSETPART	Readable and writable. Any write to the address sets the bits regardless of value.
RWX	Same as RW, but unstable. Can be changed functionally.
RWX_WAND	Same as RW_WAND, but unstable. Can be changed functionally.
RWX_WCLEAR	Same as RW_WCLEAR, but unstable. Can be changed functionally.
RWX_WCLRPART	Same as RW_WCLRPART, but unstable. Can be changed functionally.
RWX_WOR	Same as RW_WOR, but unstable. Can be changed functionally.
RWX_WSETPART	Same as RW_WSETPART, but unstable. Can be changed functionally.
RX	Receive
SBE	Self-boot engine

SCM	Single-chip module
SCOM	Serial communications. SCOM is used for read and full write access.
SCOM1	Serial communications 1. SCOM1 is used for AND write access.
SCOM2	Serial communications 2. SCOM2 is used for OR write access.
SCOMFSI0	Scan communications to flexible service interface 0. SCOMFSI0 covers resources located in FSI slave 0, when addressed from the PIB.
SCOMFSI1	Scan communications to flexible service interface 1. SCOMFSI1 covers resources located in FSI slave 1, when addressed from the PIB.
SEL	Select
Slvrst	Slave reset
SPATTN	Special attention
SPR	Special-purpose register
SPRD	Special-purpose register data
SPRD_T0	Special-purpose register thread 0
SPRD_T1	Special-purpose register thread 1
SPRD_T3	Special-purpose register thread 3
SPRD_T5	Special-purpose register thread 5
SPS	Steps per sync, sleep Pstate
TFMR	Time Facility Management Register
TOD	Time of day
TX	Transmit
UE	Uncorrectable error

VCO	Voltage controlled oscillator
VIO	Voltage I/O
Vref	Voltage reference
wdata	Write data
WO	Same as RW, but bits are write-only.
WO_AND	Same as RW_WAND, but bits are write-only.
WO_CLEAR	Same as RW_WCLEAR, but bits are write-only.
WO_CLRPART	Same as RW_WCLRPART, but bits are write-only.
WO_n_mP	Write only pulsed. A write of '1' creates a pulse for a minimum of n register clocks and maximum of m register clocks. A read returns '0'.
WO_nP Write	Only pulsed. A write of '1' creates a pulse for n register clocks. A read returns '0'.
WO_OR	Same as RW_WOR, but bits are write-only.
WO_SETPART	Same as RW_WSETPART, but bits are write-only.
WOF	Who's on first?
WOX	Same as WO, but unstable. Can be changed functionally.
WOX_AND	Same as WO_AND, but unstable. Can be changed functionally.
WOX_CLEAR	Same as WO_CLEAR, but unstable. Can be changed functionally.
WOX_CLRPART	Same as WO_CLRPART, but unstable. Can be changed functionally.
WOX_n_mP	Same as WO_n_mP, but unstable. Can be changed functionally.
WOX_nP	Same as WO_nP, but unstable. Can be changed functionally.
WOX_OR	Same as WO_OR, but unstable. Can be changed functionally.
WOX_SETPART	Same as WO_SETPART, but unstable. Can be changed functionally.

XER	Fixed-Point Exception Register
XFIR	X Fault Isolation Register
XOR	Exclusive OR

3. POWER8: TP, PB, XBUS, ABUS, & PCIE Chiplets

The POWER8 Processor registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
ABUS.BUSCTL.SCOM.FIR_MASK_REG	0x0000000008010C03	614
ABUS.BUSCTL.SCOM.FIR_REG	0x0000000008010C00	612
ABUS.BUSCTL.SCOM.SCOM_MODE_PB	0x0000000008010C20	615
EH.PB.MCD.MCDCTL.FIR_ACTION0_REG	0x0000000002013406	561
EH.PB.MCD.MCDCTL.FIR_ACTION1_REG	0x0000000002013407	561
EH.PB.MCD.MCDCTL.FIR_MASK_REG	0x0000000002013403	560
EH.PB.MCD.MCDCTL.FIR_REG	0x0000000002013400	560
EH.PB.MCD.MCDCTL.MCD_BOT	0x000000000201340E	564
EH.PB.MCD.MCDCTL.MCD_CHA	0x000000000201340F	565
EH.PB.MCD.MCDCTL.MCD_PRE_EP	0x000000000201340B	562
EH.PB.MCD.MCDCTL.MCD_REC_EVEN	0x0000000002013410	566
EH.PB.MCD.MCDCTL.MCD_REC_ODD	0x0000000002013411	567
EH.PB.MCD.MCDCTL.MCD_STR	0x000000000201340D	563
EH.PB.MCD.MCDCTL.MCD_TOP	0x000000000201340C	562
EH.PB.MISC.EXTFIR_ACTION0_REG	0x0000000002010C74	434
EH.PB.MISC.EXTFIR_ACTION1_REG	0x0000000002010C75	434
EH.PB.MISC.EXTFIR_MASK_REG	0x0000000002010C71	434
EH.PB.MISC.EXTFIR_REG	0x0000000002010C6E	433
EH.PB.MISC.PB_CENT_CR_ERROR	0x0000000002010C6C	423
EH.PB.MISC.PB_CENT_EVENT_COMPA	0x0000000002010C6A	422
EH.PB.MISC.PB_CENT_EVENT_COMPB	0x0000000002010C6B	423
EH.PB.MISC.PB_CENT_EVENT_SEL	0x0000000002010C69	420
EH.PB.MISC.PB_CENT_EXTDAT_COUNTER	0x0000000002010C53	404
EH.PB.MISC.PB_CENT_FIR_ACTION0_REG	0x0000000002010C46	429



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EH.PB.MISC.PB_CENT_FIR_ACTION1_REG	0x0000000002010C47	429
EH.PB.MISC.PB_CENT_FIR_MASK_REG	0x0000000002010C43	428
EH.PB.MISC.PB_CENT_FIR_REG	0x0000000002010C40	427
EH.PB.MISC.PB_CENT_FLMCFG0	0x0000000002010C5E	357
EH.PB.MISC.PB_CENT_FLMCFG1	0x0000000002010C5F	357
EH.PB.MISC.PB_CENT_FLMCFGM0	0x0000000002010C60	358
EH.PB.MISC.PB_CENT_FLMCFGM1	0x0000000002010C61	359
EH.PB.MISC.PB_CENT_GP_CMD_RATE_DP0	0x0000000002010C62	410
EH.PB.MISC.PB_CENT_GP_CMD_RATE_DP1	0x0000000002010C63	411
EH.PB.MISC.PB_CENT_HPX_MODE_CURR	0x0000000002010C4E	353
EH.PB.MISC.PB_CENT_HPX_MODE_NEXT	0x0000000002010C4D	350
EH.PB.MISC.PB_CENT_HP_MODE_CURR	0x0000000002010C4C	345
EH.PB.MISC.PB_CENT_HP_MODE_NEXT	0x0000000002010C4B	341
EH.PB.MISC.PB_CENT_LPM_COUNTER	0x0000000002010C51	398
EH.PB.MISC.PB_CENT_MODE	0x0000000002010C4A	334
EH.PB.MISC.PB_CENT_NMPM_COUNTER	0x0000000002010C50	393
EH.PB.MISC.PB_CENT_PMU	0x0000000002010C68	414
EH.PB.MISC.PB_CENT_RCMD_INTDAT_COUNTER	0x0000000002010C52	404
EH.PB.MISC.PB_CENT_RGMCFG00	0x0000000002010C58	406
EH.PB.MISC.PB_CENT_RGMCFG01	0x0000000002010C59	407
EH.PB.MISC.PB_CENT_RGMCFG10	0x0000000002010C5A	408
EH.PB.MISC.PB_CENT_RGMCFGM00	0x0000000002010C5B	408
EH.PB.MISC.PB_CENT_RGMCFGM01	0x0000000002010C5C	409
EH.PB.MISC.PB_CENT_RGMCFGM10	0x0000000002010C5D	410
EH.PB.MISC.PB_CENT_RGP_CMD_RATE_DP0	0x0000000002010C64	412
EH.PB.MISC.PB_CENT_RGP_CMD_RATE_DP1	0x0000000002010C65	412
EH.PB.MISC.PB_CENT_SCONFIG_LOAD	0x0000000002010C6D	360
EH.PB.MISC.PB_CENT_SP_CMD_RATE_DP0	0x0000000002010C66	413
EH.PB.MISC.PB_CENT_SP_CMD_RATE_DP1	0x0000000002010C67	413
EH.PB.MISC.PB_CENT_TRACE	0x0000000002010C4F	390
EH.PB.MISC.PB_EAST_FIR_ACTION0_REG	0x0000000002010C86	432
EH.PB.MISC.PB_EAST_FIR_ACTION1_REG	0x0000000002010C87	433
EH.PB.MISC.PB_EAST_FIR_MASK_REG	0x0000000002010C83	431
EH.PB.MISC.PB_EAST_FIR_REG	0x0000000002010C80	430
EH.PB.MISC.PB_EAST_FLMCFG0	0x0000000002010C92	386
EH.PB.MISC.PB_EAST_FLMCFG1	0x0000000002010C93	386
EH.PB.MISC.PB_EAST_FLMCFGM0	0x0000000002010C94	387
EH.PB.MISC.PB_EAST_FLMCFGM1	0x0000000002010C95	388
EH.PB.MISC.PB_EAST_HPX_MODE_CURR	0x0000000002010C8E	382
EH.PB.MISC.PB_EAST_HPX_MODE_NEXT	0x0000000002010C8D	379
EH.PB.MISC.PB_EAST_HP_MODE_CURR	0x0000000002010C8C	374
EH.PB.MISC.PB_EAST_HP_MODE_NEXT	0x0000000002010C8B	370
EH.PB.MISC.PB_EAST_MODE	0x0000000002010C8A	361
EH.PB.MISC.PB_EAST_SCONFIG_LOAD	0x0000000002010C96	389
EH.PB.MISC.PB_WEST_FIR_ACTION0_REG	0x0000000002010C06	427
EH.PB.MISC.PB_WEST_FIR_ACTION1_REG	0x0000000002010C07	427
EH.PB.MISC.PB_WEST_FIR_MASK_REG	0x0000000002010C03	425
EH.PB.MISC.PB_WEST_FIR_REG	0x0000000002010C00	424



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EH.PB.MISC.PB_WEST_FLMCFG0	0x0000000002010C12	329
EH.PB.MISC.PB_WEST_FLMCFG1	0x0000000002010C13	330
EH.PB.MISC.PB_WEST_FLMCFGM0	0x0000000002010C14	331
EH.PB.MISC.PB_WEST_FLMCFGM1	0x0000000002010C15	332
EH.PB.MISC.PB_WEST_HPX_MODE_CURR	0x0000000002010C0E	326
EH.PB.MISC.PB_WEST_HPX_MODE_NEXT	0x0000000002010C0D	322
EH.PB.MISC.PB_WEST_HP_MODE_CURR	0x0000000002010C0C	318
EH.PB.MISC.PB_WEST_HP_MODE_NEXT	0x0000000002010C0B	314
EH.PB.MISC.PB_WEST_MODE	0x0000000002010C0A	305
EH.PB.MISC.PB_WEST_SCONFIG_LOAD	0x0000000002010C16	333
EH.PB.PB_CENT_PMU0_COUNTER	0x0000000002010C54	405
EH.PB.PB_CENT_PMU1_COUNTER	0x0000000002010C55	405
EH.PB.PB_CENT_PMU2_COUNTER	0x0000000002010C56	405
EH.PB.PB_CENT_PMU3_COUNTER	0x0000000002010C57	406
EH.TPC.HCA.EHCA_FIR_MASK_REG	0x0000000002010983	296
EH.TPC.HCA.EHCA_FIR_REG	0x0000000002010980	294
EH.TPC.HCA.HCA_BAR	0x000000000201098A	297
EH.TPC.HCA.HCA_COUNT_BAR	0x000000000201098B	298
EH.TPC.HCA.HCA_FLUSH	0x0000000002010990	299
EH.TPC.HCA.HCA_MIRROR_BAR	0x0000000002010993	300
EH.TPC.HCA.HCA_MODES	0x000000000201098F	298
EH.TPC.HCA.HCA_REF_BAR	0x000000000201098E	298
EH.TPC.HCA.HCA_RESET	0x0000000002010992	299
EH.TPC.SYNC_CONFIG	0x0000000002030000	239
EH.TPC.TR1.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	0x0000000002010440	233
EH.TPC.TR1.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	0x0000000002010441	234
EH.TPC.TR2.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	0x0000000002010480	234
EH.TPC.TR2.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	0x0000000002010481	234
EH.TPC.TR3.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	0x00000000020104C0	235
EH.TPC.TR3.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	0x00000000020104C1	235
EH.TPC.TR4.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	0x0000000002010500	235
EH.TPC.TR4.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	0x0000000002010501	235
EH.TPC.TR5.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	0x0000000002010540	236
EH.TPC.TR5.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	0x0000000002010541	236
EH.TPC.TR6.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	0x0000000002010580	236
EH.TPC.TR6.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	0x0000000002010581	237
EH.TPC.TR7.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	0x00000000020105C0	237
EH.TPC.TR7.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	0x00000000020105C1	237
EH.TPC.TR8.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	0x0000000002010600	238
EH.TPC.TR8.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	0x0000000002010601	238
EH.TPC.TR9.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	0x0000000002010640	238
EH.TPC.TR9.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	0x0000000002010641	238
EH.TPCHIP.NET.PCBSLAB.GP3_REG	0x00000000080F0012	620
EH.TPCHIP.NET.PCBSLAB.HANG_PULSE_0_REG	0x00000000080F0020	621
EH.TPCHIP.NET.PCBSLAB.HANG_PULSE_6_REG	0x00000000080F0026	621
EH.TPCHIP.NET.PCBSLAB.MULTICAST_GROUP_1	0x00000000080F0001	619
EH.TPCHIP.NET.PCBSLAB.MULTICAST_GROUP_2	0x00000000080F0002	619
EH.TPCHIP.NET.PCBSLAB.MULTICAST_GROUP_3	0x00000000080F0003	619



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EH.TPCHIP.NET.PCBSLAB.MULTICAST_GROUP_4	0x00000000080F0004	620
EH.TPCHIP.NET.PCBSLAB.PLL_LOCK_REG	0x00000000080F0019	617
EH.TPCHIP.NET.PCBSLAB.PRE_COUNTER_REG	0x00000000080F0028	621
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.GP3_REG	0x00000000110F0012	660
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.GP3_REG	0x00000000120F0012	661
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.GP3_REG	0x00000000130F0012	662
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.GP3_REG	0x00000000140F0012	663
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.GP3_REG	0x00000000150F0012	664
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.GP3_REG	0x00000000160F0012	664
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.GP3_REG	0x00000000190F0012	665
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.GP3_REG	0x000000001A0F0012	666
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.GP3_REG	0x000000001B0F0012	667
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.GP3_REG	0x000000001C0F0012	668
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.GP3_REG	0x000000001D0F0012	669
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.GP3_REG	0x000000001E0F0012	670
EH.TPCHIP.NET.PCBSLNEST.PLL_LOCK_REG	0x00000000020F0019	435
EH.TPCHIP.NET.PCBSLPCI.GP3_REG	0x00000000090F0012	657
EH.TPCHIP.NET.PCBSLPCI.HANG_PULSE_6_REG	0x00000000090F0026	658
EH.TPCHIP.NET.PCBSLPCI.MULTICAST_GROUP_1	0x00000000090F0001	656
EH.TPCHIP.NET.PCBSLPCI.MULTICAST_GROUP_2	0x00000000090F0002	656
EH.TPCHIP.NET.PCBSLPCI.MULTICAST_GROUP_3	0x00000000090F0003	656
EH.TPCHIP.NET.PCBSLPCI.MULTICAST_GROUP_4	0x00000000090F0004	657
EH.TPCHIP.NET.PCBSLPCI.PLL_LOCK_REG	0x00000000090F0019	655
EH.TPCHIP.NET.PCBSLPCI.PRE_COUNTER_REG	0x00000000090F0028	658
EH.TPCHIP.NET.PCBSLXB.CLK_ADJ_SET	0x00000000040F0016	569
EH.TPCHIP.NET.PCBSLXB.GP3_REG	0x00000000040F0012	598
EH.TPCHIP.NET.PCBSLXB.HANG_PULSE_0_REG	0x00000000040F0020	599
EH.TPCHIP.NET.PCBSLXB.HANG_PULSE_6_REG	0x00000000040F0026	600
EH.TPCHIP.NET.PCBSLXB.MULTICAST_GROUP_1	0x00000000040F0001	597
EH.TPCHIP.NET.PCBSLXB.MULTICAST_GROUP_2	0x00000000040F0002	598
EH.TPCHIP.NET.PCBSLXB.MULTICAST_GROUP_3	0x00000000040F0003	598
EH.TPCHIP.NET.PCBSLXB.MULTICAST_GROUP_4	0x00000000040F0004	598
EH.TPCHIP.NET.PCBSLXB.PLL_LOCK_REG	0x00000000040F0019	599
EH.TPCHIP.NET.PCBSLXB.PRE_COUNTER_REG	0x00000000040F0028	600
EH.TPCHIP.OCC.OCI.OCB.JTG_PIB_OJCFG	0x000000000006B004	112
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBICR0	0x000000000006A207	120
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBICR1	0x000000000006A217	129
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBICR2	0x000000000006A227	138
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWCR0	0x000000000006A208	121
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWCR1	0x000000000006A218	130
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWCR2	0x000000000006A228	139
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWSBR0	0x000000000006A20C	121
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWSBR1	0x000000000006A21C	130
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWSBR2	0x000000000006A22C	139
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSES0	0x000000000006A206	120
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSES1	0x000000000006A216	129
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSES2	0x000000000006A226	138
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHBR0	0x000000000006A203	118



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EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHBR1	0x000000000006A213	127
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHBR2	0x000000000006A223	136
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHCS0	0x000000000006A204	118
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHCS1	0x000000000006A214	127
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHCS2	0x000000000006A224	136
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLBR0	0x000000000006A200	115
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLBR1	0x000000000006A210	124
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLBR2	0x000000000006A220	133
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLCS0	0x000000000006A201	116
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLCS1	0x000000000006A211	125
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLCS2	0x000000000006A221	134
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCIR0	0x000000000006A00A	157
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCIR1	0x000000000006A01A	157
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_ODHER0	0x000000000006A00E	158
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_ODHER1	0x000000000006A01E	158
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OIEPR0	0x000000000006A009	156
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OIEPR1	0x000000000006A019	156
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OIMR0	0x000000000006A004	153
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OIMR1	0x000000000006A014	153
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OISR0	0x000000000006A000	151
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OISR1	0x000000000006A010	152
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OITR0	0x000000000006A008	154
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OITR1	0x000000000006A018	154
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OTR0	0x000000000006A100	159
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OTR1	0x000000000006A101	160
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OUDER0	0x000000000006A00C	158
EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OUDER1	0x000000000006A01C	159
EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBAR0	0x000000000006B010	113
EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBAR1	0x000000000006B030	122
EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBAR2	0x000000000006B050	131
EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBAR3	0x000000000006B070	140
EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBCSR0	0x000000000006B011	113
EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBCSR1	0x000000000006B031	122
EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBCSR2	0x000000000006B051	131
EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBCSR3	0x000000000006B071	140
EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBDR0	0x000000000006B015	115
EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBDR1	0x000000000006B035	124
EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBDR2	0x000000000006B055	133
EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBDR3	0x000000000006B075	142
EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBESR0	0x000000000006B014	115
EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBESR1	0x000000000006B034	124
EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBESR2	0x000000000006B054	133
EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBESR3	0x000000000006B074	142
EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCDBG	0x000000000006B003	112
EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCR	0x000000000006B000	111
EH.TPCHIP.OCC.OCI.POREGPE.I0_CONTROL_REG	0x0000000000060001	75
EH.TPCHIP.OCC.OCI.POREGPE.I0_DATA0_REG	0x0000000000060015	85
EH.TPCHIP.OCC.OCI.POREGPE.I0_DBG0_REG	0x000000000006000F	81



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EH.TPCHIP.OCC.OCI.POREGPE.I0_DBG1_REG	0x0000000000060010	82
EH.TPCHIP.OCC.OCI.POREGPE.I0_ERROR_MASK_REG	0x0000000000060003	76
EH.TPCHIP.OCC.OCI.POREGPE.I0_EXE_TRIGGER_REG	0x0000000000060009	80
EH.TPCHIP.OCC.OCI.POREGPE.I0_I2C_E0_PARAM_REG	0x0000000000060017	85
EH.TPCHIP.OCC.OCI.POREGPE.I0_I2C_E1_PARAM_REG	0x0000000000060018	86
EH.TPCHIP.OCC.OCI.POREGPE.I0_I2C_E2_PARAM_REG	0x0000000000060019	86
EH.TPCHIP.OCC.OCI.POREGPE.I0_IBUF_2_REG	0x000000000006000E	81
EH.TPCHIP.OCC.OCI.POREGPE.I0_IBUF_LO_REG	0x000000000006000D	81
EH.TPCHIP.OCC.OCI.POREGPE.I0_ID_FLAGS_REG	0x0000000000060014	84
EH.TPCHIP.OCC.OCI.POREGPE.I0_MEMORY_RELOC_REG	0x0000000000060016	85
EH.TPCHIP.OCC.OCI.POREGPE.I0_OCI_BASE_ADDRESS_0_REG	0x0000000000060006	78
EH.TPCHIP.OCC.OCI.POREGPE.I0_OCI_BASE_ADDRESS_1_REG	0x0000000000060007	79
EH.TPCHIP.OCC.OCI.POREGPE.I0_PC_STACK0_REG	0x0000000000060011	83
EH.TPCHIP.OCC.OCI.POREGPE.I0_PC_STACK1_REG	0x0000000000060012	84
EH.TPCHIP.OCC.OCI.POREGPE.I0_PC_STACK2_REG	0x0000000000060013	84
EH.TPCHIP.OCC.OCI.POREGPE.I0_PERV_BASE_ADDRESS_0_REG	0x0000000000060004	78
EH.TPCHIP.OCC.OCI.POREGPE.I0_PERV_BASE_ADDRESS_1_REG	0x0000000000060005	78
EH.TPCHIP.OCC.OCI.POREGPE.I0_RESET_REG	0x0000000000060002	76
EH.TPCHIP.OCC.OCI.POREGPE.I0_SCRATCH0_REG	0x000000000006000A	80
EH.TPCHIP.OCC.OCI.POREGPE.I0_SCRATCH1_REG	0x000000000006000B	80
EH.TPCHIP.OCC.OCI.POREGPE.I0_SCRATCH2_REG	0x000000000006000C	81
EH.TPCHIP.OCC.OCI.POREGPE.I0_STATUS_REG	0x0000000000060000	51
EH.TPCHIP.OCC.OCI.POREGPE.I0_TABLE_BASE_ADDRESS_REG	0x0000000000060008	79
EH.TPCHIP.OCC.OCI.POREGPE.I1_CONTROL_REG	0x0000000000060021	87
EH.TPCHIP.OCC.OCI.POREGPE.I1_DATA0_REG	0x0000000000060035	98
EH.TPCHIP.OCC.OCI.POREGPE.I1_DBG0_REG	0x000000000006002F	94
EH.TPCHIP.OCC.OCI.POREGPE.I1_DBG1_REG	0x0000000000060030	95
EH.TPCHIP.OCC.OCI.POREGPE.I1_ERROR_MASK_REG	0x0000000000060023	90
EH.TPCHIP.OCC.OCI.POREGPE.I1_EXE_TRIGGER_REG	0x0000000000060029	93
EH.TPCHIP.OCC.OCI.POREGPE.I1_I2C_E0_PARAM_REG	0x0000000000060037	98
EH.TPCHIP.OCC.OCI.POREGPE.I1_I2C_E1_PARAM_REG	0x0000000000060038	99
EH.TPCHIP.OCC.OCI.POREGPE.I1_I2C_E2_PARAM_REG	0x0000000000060039	99
EH.TPCHIP.OCC.OCI.POREGPE.I1_IBUF_2_REG	0x000000000006002E	94
EH.TPCHIP.OCC.OCI.POREGPE.I1_IBUF_LO_REG	0x000000000006002D	94
EH.TPCHIP.OCC.OCI.POREGPE.I1_ID_FLAGS_REG	0x0000000000060034	97
EH.TPCHIP.OCC.OCI.POREGPE.I1_MEMORY_RELOC_REG	0x0000000000060036	98
EH.TPCHIP.OCC.OCI.POREGPE.I1_OCI_BASE_ADDRESS_0_REG	0x0000000000060026	92
EH.TPCHIP.OCC.OCI.POREGPE.I1_OCI_BASE_ADDRESS_1_REG	0x0000000000060027	92
EH.TPCHIP.OCC.OCI.POREGPE.I1_PC_STACK0_REG	0x0000000000060031	96
EH.TPCHIP.OCC.OCI.POREGPE.I1_PC_STACK1_REG	0x0000000000060032	97
EH.TPCHIP.OCC.OCI.POREGPE.I1_PC_STACK2_REG	0x0000000000060033	97
EH.TPCHIP.OCC.OCI.POREGPE.I1_PERV_BASE_ADDRESS_0_REG	0x0000000000060024	91
EH.TPCHIP.OCC.OCI.POREGPE.I1_PERV_BASE_ADDRESS_1_REG	0x0000000000060025	91
EH.TPCHIP.OCC.OCI.POREGPE.I1_RESET_REG	0x0000000000060022	89
EH.TPCHIP.OCC.OCI.POREGPE.I1_SCRATCH0_REG	0x000000000006002A	93
EH.TPCHIP.OCC.OCI.POREGPE.I1_SCRATCH1_REG	0x000000000006002B	93
EH.TPCHIP.OCC.OCI.POREGPE.I1_SCRATCH2_REG	0x000000000006002C	94
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EH.TPCHIP.OCC.OCI.PORESLOW.I0_DATA0_REG	0x0000000000068015	110
EH.TPCHIP.OCC.OCI.PORESLOW.I0_DBG0_REG	0x000000000006800F	107
EH.TPCHIP.OCC.OCI.PORESLOW.I0_DBG1_REG	0x0000000000068010	107
EH.TPCHIP.OCC.OCI.PORESLOW.I0_ERROR_MASK_REG	0x0000000000068003	102
EH.TPCHIP.OCC.OCI.PORESLOW.I0_EXE_TRIGGER_REG	0x0000000000068009	105
EH.TPCHIP.OCC.OCI.PORESLOW.I0_I2C_E0_PARAM_REG	0x0000000000068017	110
EH.TPCHIP.OCC.OCI.PORESLOW.I0_I2C_E1_PARAM_REG	0x0000000000068018	110
EH.TPCHIP.OCC.OCI.PORESLOW.I0_I2C_E2_PARAM_REG	0x0000000000068019	111
EH.TPCHIP.OCC.OCI.PORESLOW.I0_IBUF_2_REG	0x000000000006800E	106
EH.TPCHIP.OCC.OCI.PORESLOW.I0_IBUF_LO_REG	0x000000000006800D	106
EH.TPCHIP.OCC.OCI.PORESLOW.I0_ID_FLAGS_REG	0x0000000000068014	109
EH.TPCHIP.OCC.OCI.PORESLOW.I0_MEMORY_RELOC_REG	0x0000000000068016	110
EH.TPCHIP.OCC.OCI.PORESLOW.I0_OCI_BASE_ADDRESS_0_REG	0x0000000000068006	104
EH.TPCHIP.OCC.OCI.PORESLOW.I0_OCI_BASE_ADDRESS_1_REG	0x0000000000068007	104
EH.TPCHIP.OCC.OCI.PORESLOW.I0_PC_STACK0_REG	0x0000000000068011	108
EH.TPCHIP.OCC.OCI.PORESLOW.I0_PC_STACK1_REG	0x0000000000068012	109
EH.TPCHIP.OCC.OCI.PORESLOW.I0_PC_STACK2_REG	0x0000000000068013	109
EH.TPCHIP.OCC.OCI.PORESLOW.I0_PERV_BASE_ADDRESS_0_REG	0x0000000000068004	103
EH.TPCHIP.OCC.OCI.PORESLOW.I0_PERV_BASE_ADDRESS_1_REG	0x0000000000068005	103
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EH.TPCHIP.OCC.OCI.PORESLOW.I0_SCRATCH0_REG	0x000000000006800A	105
EH.TPCHIP.OCC.OCI.PORESLOW.I0_SCRATCH1_REG	0x000000000006800B	106
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EH.TPCHIP.OCC.OCI.PORESLOW.I0_STATUS_REG	0x0000000000068000	100
EH.TPCHIP.OCC.OCI.PORESLOW.I0_TABLE_BASE_ADDRESS_REG	0x0000000000068008	104
EH.TPCHIP.OCC.OCI.SCOM.OCC_SCOM_OCCLFIR	0x0000000001010800	142
EH.TPCHIP.OCC.OCI.SCOM.OCC_SCOM_OCCLFIRACT0	0x0000000001010806	147
EH.TPCHIP.OCC.OCI.SCOM.OCC_SCOM_OCCLFIRACT1	0x0000000001010807	148
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EH.TPCHIP.OCC.PMC.PMC_ERROR_INT_MASK_LO_REG	0x0000000000062068	200
EH.TPCHIP.OCC.PMC.PMC_FSMSTATE_STATUS_REG	0x0000000000062020	167
EH.TPCHIP.OCC.PMC.PMC_GLOBAL_PSTATE_BOUNDS_REG	0x0000000000062004	164
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EH.TPCHIP.OCC.PMC.PMC_O2S_CTRL_REG0A	0x0000000000062050	188
EH.TPCHIP.OCC.PMC.PMC_O2S_CTRL_REG0B	0x0000000000062051	189
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EH.TPCHIP.OCC.PMC.PMC_O2S_RDATA_REG	0x0000000000062059	192
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EH.TPCHIP.OCC.PMC.PMC_O2S_WDATA_REG	0x0000000000062058	192
EH.TPCHIP.OCC.PMC.PMC_OCC_HEARTBEAT_REG	0x0000000000062066	166
EH.TPCHIP.OCC.PMC.PMC_PARAMETER_REG0	0x0000000000062005	183
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EH.TPCHIP.OCC.PMC.PMC_PEND_IDLE_REQ_REG1	0x0000000000062081	170
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EH.TPCHIP.OCC.PMC.PMC_PORE_REQ_REG0	0x000000000006208E	176
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EH.TPCHIP.OCC.PMC.PMC_PORE_REQ_STAT_REG	0x0000000000062090	178
EH.TPCHIP.OCC.PMC.PMC_PORE_SCRATCH_REG0	0x000000000006209D	200
EH.TPCHIP.OCC.PMC.PMC_PORE_SCRATCH_REG1	0x000000000006209E	200
EH.TPCHIP.OCC.PMC.PMC_PSTATE_MONITOR_AND_CTRL_REG	0x0000000000062002	162
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EH.TPCHIP.OCC.PMC.PMC_SPIV_COMMAND_REG	0x0000000000062047	188
EH.TPCHIP.OCC.PMC.PMC_SPIV_CTRL_REG0A	0x0000000000062040	184
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EH.TPCHIP.OCC.SRAM.SRAM_CTL.SRAM_SRBV0	0x0000000000066004	149
EH.TPCHIP.OCC.SRAM.SRAM_CTL.SRAM_SRBV1	0x0000000000066005	150
EH.TPCHIP.OCC.SRAM.SRAM_CTL.SRAM_SRBV2	0x0000000000066006	150
EH.TPCHIP.OCC.SRAM.SRAM_CTL.SRAM_SRBV3	0x0000000000066007	150
EH.TPCHIP.OTPROM.MULT_OTP_ROM_ECC_2_8.OTPROM_GEN#0.DATA_OTPROM.ECID_PART0_REGISTER	0x0000000000018000	55
EH.TPCHIP.OTPROM.MULT_OTP_ROM_ECC_2_8.OTPROM_GEN#0.DATA_OTPROM.ECID_PART12_REGISTER	0x000000000001800C	55
EH.TPCHIP.OTPROM.MULT_OTP_ROM_ECC_2_8.OTPROM_GEN#0.DATA_OTPROM.ECID_PART13_REGISTER	0x000000000001800D	55
EH.TPCHIP.OTPROM.MULT_OTP_ROM_ECC_2_8.OTPROM_GEN#0.DATA_OTPROM.ECID_PART14_REGISTER	0x000000000001800E	56
EH.TPCHIP.OTPROM.MULT_OTP_ROM_ECC_2_8.OTPROM_GEN#0.DATA_OTPROM.ECID_PART15_REGISTER	0x000000000001800F	56
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EH.TPCHIP.OTPROM.MULT_OTP_ROM_ECC_2_8.OTPROM_GEN#0.DATA_OTPROM.ECID_PART19_REGISTER	0x00000000000018013	57
EH.TPCHIP.OTPROM.MULT_OTP_ROM_ECC_2_8.OTPROM_GEN#0.DATA_OTPROM.ECID_PART1_REGISTER	0x00000000000018001	55
EH.TPCHIP.OTPROM.MULT_OTP_ROM_ECC_2_8.OTPROM_GEN#0.DATA_OTPROM.ECID_PART20_REGISTER	0x00000000000018014	57
EH.TPCHIP.OTPROM.MULT_OTP_ROM_ECC_2_8.OTPROM_GEN#0.DATA_OTPROM.ECID_PART21_REGISTER	0x00000000000018015	57
EH.TPCHIP.OTPROM.MULT_OTP_ROM_ECC_2_8.OTPROM_GEN#0.DATA_OTPROM.ECID_PART22_REGISTER	0x00000000000018016	58
EH.TPCHIP.OTPROM.MULT_OTP_ROM_ECC_2_8.OTPROM_GEN#0.DATA_OTPROM.ECID_PART23_REGISTER	0x00000000000018017	58
EH.TPCHIP.PIB.ECCB.CONTROL_REG	0x000000000000C0000	219
EH.TPCHIP.PIB.ECCB.DATA_REG	0x000000000000C0003	221
EH.TPCHIP.PIB.ECCB.STATUS_REG	0x000000000000C0002	220
EH.TPCHIP.PIB.I2CM.COMMAND_REGISTER_1	0x000000000000A0025	213
EH.TPCHIP.PIB.I2CM.CONTROL_REGISTER_1	0x000000000000A0020	209
EH.TPCHIP.PIB.I2CM.DATA_REGISTER_1	0x000000000000A0023	213
EH.TPCHIP.PIB.I2CM.RESET_REGISTER_1	0x000000000000A0021	210
EH.TPCHIP.PIB.I2CM.STATUS_REGISTER_1	0x000000000000A0022	210
EH.TPCHIP.PIB.I2CS.TP_I2CS_COMP.I2CSCONFIG	0x000000000000D0000	211
EH.TPCHIP.PIB.I2CS.TP_I2CS_COMP.I2CSERRORS	0x000000000000D0002	212
EH.TPCHIP.PIB.I2CS.TP_I2CS_COMP.I2CSSTATUS	0x000000000000D0001	212
EH.TPCHIP.PIB.LPCM.ECCB.CONTROL_REG	0x000000000000B0000	214
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EH.TPCHIP.PIB.LPCM.ECCB.RESET_REG	0x000000000000B0001	215
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EH.TPCHIP.PIB.LPCM.LPC.SYNC_FIR_ACTION1_REG	0x0000000000001010C07	233
EH.TPCHIP.PIB.LPCM.LPC.SYNC_FIR_MASK_REG	0x0000000000001010C03	149
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EH.TPCHIP.PIB.POREMEM.PIBMEM.CTRL.PIBMEM_REPAIR_REGISTER_0	0x00000000000088007	209
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EH.TPCHIP.PIB.SBE.DATA0_REG	0x00000000000E0015	230
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EH.TPCHIP.PIB.SBE.ERROR_MASK_REG	0x00000000000E0003	223
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EH.TPCHIP.PIB.SBE.I2C_E1_PARAM_REG	0x00000000000E0018	231
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EH.TPCHIP.PIB.SBE.ID_FLAGS_REG	0x00000000000E0014	230
EH.TPCHIP.PIB.SBE.MEMORY_RELOC_REG	0x00000000000E0016	230
EH.TPCHIP.PIB.SBE.OCI_BASE_ADDRESS_0_REG	0x00000000000E0006	224
EH.TPCHIP.PIB.SBE.OCI_BASE_ADDRESS_1_REG	0x00000000000E0007	225
EH.TPCHIP.PIB.SBE.PC_STACK0_REG	0x00000000000E0011	229
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EH.TPCHIP.PIB.SBE.PERV_BASE_ADDRESS_1_REG	0x00000000000E0005	224
EH.TPCHIP.PIB.SBE.RESET_REG	0x00000000000E0002	222
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EH.TPCHIP.PIB.SBE.TABLE_BASE_ADDRESS_REG	0x00000000000E0008	225
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EH.TPCHIP.PIB.SPIADC.SPIPSS_ADC_CMD_REG	0x0000000000070004	202
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EN.NX.CXA.CXA_APC1.FOREIGN_FAR_BAR1	0x0000000002013034	532
EN.NX.CXA.CXA_APC1.FOREIGN_LOC_BAR0	0x0000000002013031	531
EN.NX.CXA.CXA_APC1.FOREIGN_LOC_BAR1	0x0000000002013033	532
EN.NX.CXA.CXA_APC1.GLOBAL_BAR0	0x000000000201302F	530
EN.NX.CXA.CXA_APC1.GLOBAL_BAR1	0x0000000002013030	531
EN.NX.CXA.CXA_APC1.NODAL_BAR0	0x000000000201302D	530
EN.NX.CXA.CXA_APC1.NODAL_BAR1	0x000000000201302E	530
EN.NX.CXA.CXA_SNPFE.SNP_REGS.CXA_SNP_CNTL_REG	0x000000000201301B	436
EN.NX.CXA.CXA_SNPFE.SNP_REGS.CXA_SNP_ERROR_REPORT_REG	0x000000000201300A	546
EN.NX.CXA.CXA_XPT.XPT_EPT.CAPP_EPOCH_AND_RECOVERY_TMR_CONTROL	0x000000000201302C	551
EN.NX.CXA.CXA_XPT.XPT_EPT.CAPP_ERR_STATUS_CONTROL	0x000000000201300E	550
EN.NX.CXA.CXA_XPT.XPT_SCOMFIR.DEBUG_CONTROL	0x0000000002013011	552
EN.NX.CXA.CXA_XPT.XPT_SCOMFIR.FIR_ACTION0_REG	0x0000000002013006	546
EN.NX.CXA.CXA_XPT.XPT_SCOMFIR.FIR_ACTION1_REG	0x0000000002013007	546
EN.NX.CXA.CXA_XPT.XPT_SCOMFIR.FIR_MASK_REG	0x0000000002013003	543
EN.NX.CXA.CXA_XPT.XPT_SCOMFIR.FIR_REG	0x0000000002013000	541



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EN.NX.CXA.CXA_XPT.XPT_SCOMFIR.TLBI_ERROR_REPORT	0x000000000201300D	549
EN.NX.CXA.XPT_ERROR_REPORT	0x000000000201300C	548
EN.NX.DBG.NX_DEBUGMUX_CTRL	0x000000000201310A	555
EN.NX.DBG.NX_DMA_ENG_FIR	0x0000000002013100	553
EN.NX.DBG.NX_DMA_ENG_FIR_MASK	0x0000000002013103	555
EN.NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_AS_MMIO_BAR	0x000000000201309E	541
EN.NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_CQ_FIR_MASK_REG	0x0000000002013083	556
EN.NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_CQ_FIR_REG	0x0000000002013080	556
EN.NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_EPSILON_COUNTER_VALUE	0x000000000201309D	540
EN.NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_FOREIGN_F_BAR0	0x000000000201309B	538
EN.NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_FOREIGN_F_BAR1	0x000000000201309C	539
EN.NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_FOREIGN_L_BAR0	0x0000000002013099	536
EN.NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_FOREIGN_L_BAR1	0x000000000201309A	537
EN.NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_GROUP_BAR0	0x0000000002013097	534
EN.NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_GROUP_BAR1	0x0000000002013098	535
EN.NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_MMIO_BAR	0x000000000201308D	532
EN.NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_NODAL_BAR0	0x0000000002013095	533
EN.NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_NODAL_BAR1	0x0000000002013096	533
EN.NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_PB_DEBUG_REG	0x0000000002013090	553
EN.NX.PBI.CQ_WRAP.NX_DEBUG_SNAPSHOT_0	0x00000000020130A4	553
EN.NX.PBI.CQ_WRAP.NX_DEBUG_SNAPSHOT_1	0x00000000020130A5	553
EN.PB.PBEN.MISC_IO.SCOM.FIR_MASK_REG	0x0000000004010C03	572
EN.PB.PBEN.MISC_IO.SCOM.FIR_REG	0x0000000004010C00	571
EN.PB.PBEN.MISC_IO.SCOM.FIR_REG_ACTION0	0x0000000004010C06	573
EN.PB.PBEN.MISC_IO.SCOM.FIR_REG_ACTION1	0x0000000004010C07	573
EN.PB.PBEN.MISC_IO.SCOM.PB_X_MODE	0x0000000004010C0A	573
EN.PB.TPC.CC_PROTECT_MODE_REG	0x00000000040303FE	585
EN.PB.TPC.CLK_REGION	0x0000000004030006	582
EN.PB.TPC.CLOCK_STAT	0x0000000004030008	584
EN.PB.TPC.EPS.FIR.LOCAL_FIR_ACTION0	0x0000000004040010	589
EN.PB.TPC.EPS.FIR.LOCAL_FIR_ACTION1	0x0000000004040011	589
EN.PB.TPC.EPS.FIR.LOCAL_FIR_MASK	0x000000000404000D	589
EN.PB.TPC.EPS.FIR.MODE_REG	0x0000000004040008	588
EN.PB.TPC.EPS.PSC.DEBUG_STATUS_REG	0x0000000004010004	569
EN.PB.TPC.EPS.PSC.PSCOM_MODE_REG	0x0000000004010000	569
EN.PB.TPC.EPS.THERM.CPM_CONFIG_WRITE_REG0	0x0000000004050000	595
EN.PB.TPC.EPS.THERM.DTS_RESULT0	0x0000000004050000	597
EN.PB.TPC.ERROR_STATUS	0x0000000004030009	585
EN.PB.TPC.FIR_MASK	0x0000000004040002	587
EN.PB.TPC.GP1	0x0000000004000001	568
EN.PB.TPC.GP2	0x0000000004000002	568
EN.PB.TPC.LOCAL_FIR	0x000000000404000A	588
EN.PB.TPC.OPCG_REG0	0x0000000004030002	580
EN.PB.TPC.OPCG_REG1	0x0000000004030003	580
EN.PB.TPC.OPCG_REG2	0x0000000004030004	581
EN.PB.TPC.OPCG_REG3	0x0000000004030005	582
EN.PB.TPC.RFIR	0x0000000004040001	586
EN.PB.TPC.SCANSELQ	0x0000000004030007	583



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EN.PB.TPC.SPATTN	0x0000000004040004	587
EN.PB.TPC.SPA_MASK	0x0000000004040007	587
EN.PB.TPC.TRA0.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	0x0000000004010400	570
EN.PB.TPC.TRA0.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	0x0000000004010401	570
EN.PB.TPC.TRA1.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	0x0000000004010800	570
EN.PB.TPC.TRA1.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	0x0000000004010801	571
EN.PB.TPC.XFIR	0x0000000004040000	586
EN.TPC.AD.ADS_IOS_LINK_EN_REG	0x0000000002020019	478
EN.TPC.AD.ADU_HANG_DIV_REG	0x0000000002020018	478
EN.TPC.AD.ALTD_CMD_REG	0x0000000002020001	472
EN.TPC.AD.ALTD_CONTROL_REG	0x0000000002020000	471
EN.TPC.AD.ALTD_DATA_REG	0x0000000002020003	475
EN.TPC.AD.ALTD_STATUS_REG	0x0000000002020002	474
EN.TPC.AD.ALTD_UNTRUSTED_BAR_ADDR_REG	0x0000000002020015	477
EN.TPC.AD.ALTD_UNTRUSTED_BAR_MASK_ADDR_REG	0x0000000002020016	477
EN.TPC.AD.ALTD_XSCOM_BASE_REG	0x0000000002020005	475
EN.TPC.AD.FORCE_ECC_REG	0x0000000002020010	475
EN.TPC.AD.RCV_ERRLOG_REG	0x0000000002020011	476
EN.TPC.AD.SND_MODE_REG	0x000000000202000B	476
EN.TPC.AD.TBROM_BASE_REG	0x0000000002020017	478
EN.TPC.BRIDGE.HCA.ENHCA_FIR_MASK_REG	0x0000000002010943	291
EN.TPC.BRIDGE.HCA.ENHCA_FIR_REG	0x0000000002010940	290
EN.TPC.BRIDGE.HCA.HCA_BAR	0x000000000201094A	291
EN.TPC.BRIDGE.HCA.HCA_COUNT_BAR	0x000000000201094B	292
EN.TPC.BRIDGE.HCA.HCA_DECAY1	0x000000000201094C	292
EN.TPC.BRIDGE.HCA.HCA_DECAY2	0x000000000201094D	293
EN.TPC.BRIDGE.HCA.HCA_MIRROR_BAR	0x0000000002010953	294
EN.TPC.BRIDGE.HCA.HCA_MODES	0x000000000201094F	293
EN.TPC.BRIDGE.HCA.HCA_REF_BAR	0x000000000201094E	293
EN.TPC.BRIDGE.HCA.HCA_RESET	0x0000000002010952	294
EN.TPC.INTP.INTR_INJECT_REG	0x00000000020109CC	301
EN.TPC.INTP.SYNC_BAR_REG	0x00000000020109CA	300
EN.TPC.INTP.SYNC_FIR_MASK_REG	0x00000000020109C3	303
EN.TPC.INTP.SYNC_FIR_REG	0x00000000020109C0	301
EN.TPC.INTP.SYNC_MODE_REG0	0x00000000020109CB	300
EN.TPC.PBA.BCDE_CTL	0x0000000000064010	270
EN.TPC.PBA.BCDE_OCIBAR	0x0000000000064014	272
EN.TPC.PBA.BCDE_PBADR	0x0000000000064013	272
EN.TPC.PBA.BCDE_SET	0x0000000000064011	271
EN.TPC.PBA.BCDE_STAT	0x0000000000064012	271
EN.TPC.PBA.BCUE_CTL	0x0000000000064015	273
EN.TPC.PBA.BCUE_OCIBAR	0x0000000000064019	275
EN.TPC.PBA.BCUE_PBADR	0x0000000000064018	274
EN.TPC.PBA.BCUE_SET	0x0000000000064016	273
EN.TPC.PBA.BCUE_STAT	0x0000000000064017	273
EN.TPC.PBA.PBACFG	0x000000000201084B	245
EN.TPC.PBA.PBAERRRPT0	0x000000000201084C	247
EN.TPC.PBA.PBAERRRPT1	0x000000000201084D	247



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EN.TPC.PBA.PBAERRRPT2	0x000000000201084E	248
EN.TPC.PBA.PBAFIR	0x0000000002010840	240
EN.TPC.PBA.PBAFIRACT0	0x0000000002010846	244
EN.TPC.PBA.PBAFIRACT1	0x0000000002010847	245
EN.TPC.PBA.PBAFIRMASK	0x0000000002010843	243
EN.TPC.PBA.PBAMODE	0x0000000000064000	257
EN.TPC.PBA.PBAOCCACT	0x000000000201084A	245
EN.TPC.PBA.PBARBUFVAL0	0x0000000002010850	249
EN.TPC.PBA.PBARBUFVAL1	0x0000000002010851	250
EN.TPC.PBA.PBARBUFVAL2	0x0000000002010852	251
EN.TPC.PBA.PBARBUFVAL3	0x0000000002010853	252
EN.TPC.PBA.PBARBUFVAL4	0x0000000002010854	253
EN.TPC.PBA.PBARBUFVAL5	0x0000000002010855	254
EN.TPC.PBA.PBASLVCTL0	0x0000000000064004	261
EN.TPC.PBA.PBASLVCTL1	0x0000000000064005	264
EN.TPC.PBA.PBASLVCTL2	0x0000000000064006	266
EN.TPC.PBA.PBASLVCTL3	0x0000000000064007	268
EN.TPC.PBA.PBASLVRST	0x0000000000064001	261
EN.TPC.PBA.PBAWBUFVAL0	0x0000000002010858	255
EN.TPC.PBA.PBAWBUFVAL1	0x0000000002010859	256
EN.TPC.PBA.PBAXCFG	0x0000000000064021	276
EN.TPC.PBA.PBAXRCVSTAT	0x0000000000064024	277
EN.TPC.PBA.PBAXSHBR0	0x0000000000064026	281
EN.TPC.PBA.PBAXSHBR1	0x000000000006402A	283
EN.TPC.PBA.PBAXSHCS0	0x0000000000064027	282
EN.TPC.PBA.PBAXSHCS1	0x000000000006402B	283
EN.TPC.PBA.PBAXSNDAT	0x0000000000064023	277
EN.TPC.PBA.PBAXSNDSTAT	0x0000000000064022	277
EN.TPC.PBA.PBAXSNDTX	0x0000000000064020	275
EN.TPC.PBA.SCOMTRUST.PBABAR0	0x0000000002013F00	278
EN.TPC.PBA.SCOMTRUST.PBABAR1	0x0000000002013F01	279
EN.TPC.PBA.SCOMTRUST.PBABAR2	0x0000000002013F02	280
EN.TPC.PBA.SCOMTRUST.PBABAR3	0x0000000002013F03	280
EN.TPC.PBA.SCOMTRUST.PBABARMSK0	0x0000000002013F04	279
EN.TPC.PBA.SCOMTRUST.PBABARMSK1	0x0000000002013F05	279
EN.TPC.PBA.SCOMTRUST.PBABARMSK2	0x0000000002013F06	280
EN.TPC.PBA.SCOMTRUST.PBABARMSK3	0x0000000002013F07	281
EN.TPC.PSI.PSI_WRAP.RX_CH_INTADDR_REG	0x0000000002010818	289
EN.TPC.PSI.PSI_WRAP.RX_CH_MISC_REG	0x000000000201081B	290
EN.TPC.PSI.PSI_WRAP.RX_CTRL_STAT_REG	0x0000000002010808	286
EN.TPC.PSI.PSI_WRAP.RX_DF_FSM_REG	0x000000000201080E	288
EN.TPC.PSI.PSI_WRAP.RX_ERROR_REG	0x000000000201080A	287
EN.TPC.PSI.PSI_WRAP.TX_CH_INTADDR_REG	0x0000000002010810	288
EN.TPC.PSI.PSI_WRAP.TX_CH_MISC_REG	0x0000000002010813	289
EN.TPC.PSI.PSI_WRAP.TX_CTRL_STAT_REG	0x0000000002010800	284
EN.TPC.PSI.PSI_WRAP.TX_DF_FSM_REG	0x0000000002010806	286
EN.TPC.PSI.PSI_WRAP.TX_ERROR_REG	0x0000000002010802	285
EN.TPC.TR1.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	0x0000000002010A00	239



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EN.TPC.TR1.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	0x0000000002010A01	239
ES.PBES_WRAP_TOP.PBES_TOP.MISC_IO.SCOM.PB_IOA_FIR_ACTION0_REG	0x0000000008010806	624
ES.PBES_WRAP_TOP.PBES_TOP.MISC_IO.SCOM.PB_IOA_FIR_ACTION1_REG	0x0000000008010807	625
ES.PBES_WRAP_TOP.PBES_TOP.MISC_IO.SCOM.PB_IOA_FIR_MASK_REG	0x0000000008010803	623
ES.PBES_WRAP_TOP.PBES_TOP.MISC_IO.SCOM.PB_IOA_FIR_REG	0x0000000008010800	622
ES.PBES_WRAP_TOP.PBES_TOP.MISC_IO.SCOM.PB_IOA_FMR_CFG	0x0000000008010813	627
ES.PBES_WRAP_TOP.PBES_TOP.MISC_IO.SCOM.PB_IOA_MODE	0x000000000801080A	625
ES.PBES_WRAP_TOP.PBES_TOP.MISC_IO.SCOM.PB_IOA_TRACE_CFG	0x0000000008010812	626
ES.PBES_WRAP_TOP.PBES_TOP.MISC_IOF.SCOM.PB_IOF1_ERR_DETAIL	0x0000000009010812	631
ES.PBES_WRAP_TOP.PBES_TOP.MISC_IOF.SCOM.PB_IOF_FIR_MASK_REG	0x0000000009010803	648
ES.PBES_WRAP_TOP.PBES_TOP.MISC_IOF.SCOM.PB_IOF_FIR_REG	0x0000000009010800	646
ES.PBES_WRAP_TOP.PBES_TOP.MISC_IOF.SCOM.PB_IOF_FMR_CFG	0x0000000009010813	632
ES.PBES_WRAP_TOP.TPC.CC.PROTECT_MODE_REG	0x00000000080303FE	608
ES.PBES_WRAP_TOP.TPC.CLK_REGION	0x0000000008030006	605
ES.PBES_WRAP_TOP.TPC.CLOCK_STAT	0x0000000008030008	607
ES.PBES_WRAP_TOP.TPC.EPS.FIR.LOCAL_FIR_ACTION0	0x0000000008040010	612
ES.PBES_WRAP_TOP.TPC.EPS.FIR.LOCAL_FIR_ACTION1	0x0000000008040011	612
ES.PBES_WRAP_TOP.TPC.EPS.FIR.LOCAL_FIR_MASK	0x000000000804000D	611
ES.PBES_WRAP_TOP.TPC.EPS.FIR.MODE_REG	0x0000000008040008	610
ES.PBES_WRAP_TOP.TPC.EPS.PSC.DEBUG_STATUS_REG	0x0000000008010004	602
ES.PBES_WRAP_TOP.TPC.EPS.PSC.PSCOM_MODE_REG	0x0000000008010000	601
ES.PBES_WRAP_TOP.TPC.EPS.THERM.CPM_CONFIG_WRITE_REG0	0x0000000008050000	617
ES.PBES_WRAP_TOP.TPC.EPS.THERM.DTS_RESULT0	0x0000000008050000	619
ES.PBES_WRAP_TOP.TPC.ERROR_STATUS	0x0000000008030009	608
ES.PBES_WRAP_TOP.TPC.FIR_MASK	0x0000000008040002	609
ES.PBES_WRAP_TOP.TPC.GP0	0x0000000008000000	48
ES.PBES_WRAP_TOP.TPC.GP1	0x0000000008000001	600
ES.PBES_WRAP_TOP.TPC.GP2	0x0000000008000002	601
ES.PBES_WRAP_TOP.TPC.LOCAL_FIR	0x000000000804000A	611
ES.PBES_WRAP_TOP.TPC.OPCG_REG0	0x0000000008030002	603
ES.PBES_WRAP_TOP.TPC.OPCG_REG1	0x0000000008030003	603
ES.PBES_WRAP_TOP.TPC.OPCG_REG2	0x0000000008030004	604
ES.PBES_WRAP_TOP.TPC.OPCG_REG3	0x0000000008030005	605
ES.PBES_WRAP_TOP.TPC.RFIR	0x0000000008040001	609
ES.PBES_WRAP_TOP.TPC.SCANSELQ	0x0000000008030007	606
ES.PBES_WRAP_TOP.TPC.SPATTN	0x0000000008040004	610
ES.PBES_WRAP_TOP.TPC.SPA_MASK	0x0000000008040007	610
ES.PBES_WRAP_TOP.TPC.TRA.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	0x0000000008010400	602
ES.PBES_WRAP_TOP.TPC.TRA.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	0x0000000008010401	602
ES.PBES_WRAP_TOP.TPC.XFIR	0x0000000008040000	609
ES.PE_WRAP_TOP.PE0.PEPBCQ.PBAIB.PEAIBREGS.PE_ETU_RESET_REG	0x000000000901200A	634
ES.PE_WRAP_TOP.PE0.PEPBCQ.PBAIB.PEAIBREGS.PE_SYS_PH3_BASEADDR_REG	0x000000000901200B	634
ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.FIR_ACTION0_REG	0x0000000002012006	481
ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.FIR_ACTION1_REG	0x0000000002012007	482
ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.FIR_MASK_REG	0x0000000002012003	480
ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.FIR_REG	0x0000000002012000	479
ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.FIR_WOF_REG	0x0000000002012008	482
ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.PEBARS.PE_BUS_BAR_EN_REG	0x0000000002012045	495



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ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.PEBARS.PE_BUS_IO_BAR0_REG	0x0000000002012040	490
ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.PEBARS.PE_BUS_IO_BAR1_REG	0x0000000002012041	491
ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.PEBARS.PE_BUS_IO_BAR2_REG	0x0000000002012042	491
ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.PEBARS.PE_BUS_IO_MASK0_REG	0x0000000002012043	491
ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.PEBARS.PE_BUS_IO_MASK1_REG	0x0000000002012044	493
ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.PEPBREGS.FORF0BAR_REG	0x0000000002012015	487
ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.PEPBREGS.FORF1BAR_REG	0x0000000002012017	489
ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.PEPBREGS.FORL0BAR_REG	0x0000000002012014	486
ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.PEPBREGS.FORL1BAR_REG	0x0000000002012016	488
ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.PEPBREGS.GROUPBAR0_REG	0x0000000002012012	484
ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.PEPBREGS.GROUPBAR1_REG	0x0000000002012013	485
ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.PEPBREGS.NODALBAR0_REG	0x0000000002012010	482
ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.PEPBREGS.NODALBAR1_REG	0x0000000002012011	483
ES.PE_WRAP_TOP.PE1.PEPBCQ.PBAIB.PEAIBREGS.PE_ETU_RESET_REG	0x000000000901240A	634
ES.PE_WRAP_TOP.PE1.PEPBCQ.PBAIB.PEAIBREGS.PE_SYS_PH3_BASEADDR_REG	0x000000000901240B	634
ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.FIR_ACTION0_REG	0x0000000002012406	498
ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.FIR_ACTION1_REG	0x0000000002012407	499
ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.FIR_MASK_REG	0x0000000002012403	497
ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.FIR_REG	0x0000000002012400	496
ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.FIR_WOF_REG	0x0000000002012408	499
ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.PEBARS.PE_BUS_BAR_EN_REG	0x0000000002012445	512
ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.PEBARS.PE_BUS_IO_BAR0_REG	0x0000000002012440	507
ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.PEBARS.PE_BUS_IO_BAR1_REG	0x0000000002012441	508
ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.PEBARS.PE_BUS_IO_BAR2_REG	0x0000000002012442	508
ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.PEBARS.PE_BUS_IO_MASK0_REG	0x0000000002012443	508
ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.PEBARS.PE_BUS_IO_MASK1_REG	0x0000000002012444	510
ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.PEPBREGS.FORF0BAR_REG	0x0000000002012415	504
ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.PEPBREGS.FORF1BAR_REG	0x0000000002012417	506
ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.PEPBREGS.FORL0BAR_REG	0x0000000002012414	503
ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.PEPBREGS.FORL1BAR_REG	0x0000000002012416	505
ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.PEPBREGS.GROUPBAR0_REG	0x0000000002012412	501
ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.PEPBREGS.GROUPBAR1_REG	0x0000000002012413	502
ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.PEPBREGS.NODALBAR0_REG	0x0000000002012410	499
ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.PEPBREGS.NODALBAR1_REG	0x0000000002012411	500
ES.PE_WRAP_TOP.PE2.PEPBCQ.PBAIB.PEAIBREGS.PE_ETU_RESET_REG	0x000000000901280A	635
ES.PE_WRAP_TOP.PE2.PEPBCQ.PBAIB.PEAIBREGS.PE_SYS_PH3_BASEADDR_REG	0x000000000901280B	635
ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.FIR_ACTION0_REG	0x0000000002012806	515
ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.FIR_ACTION1_REG	0x0000000002012807	516
ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.FIR_MASK_REG	0x0000000002012803	514
ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.FIR_REG	0x0000000002012800	513
ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.FIR_WOF_REG	0x0000000002012808	516
ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.PEBARS.PE_BUS_BAR_EN_REG	0x0000000002012845	529
ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.PEBARS.PE_BUS_IO_BAR0_REG	0x0000000002012840	524
ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.PEBARS.PE_BUS_IO_BAR1_REG	0x0000000002012841	525
ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.PEBARS.PE_BUS_IO_BAR2_REG	0x0000000002012842	525
ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.PEBARS.PE_BUS_IO_MASK0_REG	0x0000000002012843	525
ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.PEBARS.PE_BUS_IO_MASK1_REG	0x0000000002012844	527
ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.PEPBREGS.FORF0BAR_REG	0x0000000002012815	521



Mnemonic	Address	Page
ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.PEPBREGS.FORF1BAR_REG	0x0000000002012817	523
ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.PEPBREGS.FORL0BAR_REG	0x0000000002012814	520
ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.PEPBREGS.FORL1BAR_REG	0x0000000002012816	522
ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.PEPBREGS.GROUPBAR0_REG	0x0000000002012812	518
ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.PEPBREGS.GROUPBAR1_REG	0x0000000002012813	519
ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.PEPBREGS.NODALBAR0_REG	0x0000000002012810	516
ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.PEPBREGS.NODALBAR1_REG	0x0000000002012811	517
ES.PE_WRAP_TOP.TPC.CC_PROTECT_MODE_REG	0x00000000090303FE	642
ES.PE_WRAP_TOP.TPC.CLK_REGION	0x0000000009030006	639
ES.PE_WRAP_TOP.TPC.CLOCK_STAT	0x0000000009030008	640
ES.PE_WRAP_TOP.TPC.EPS.FIR.LOCAL_FIR_ACTION0	0x0000000009040010	646
ES.PE_WRAP_TOP.TPC.EPS.FIR.LOCAL_FIR_ACTION1	0x0000000009040011	646
ES.PE_WRAP_TOP.TPC.EPS.FIR.LOCAL_FIR_MASK	0x000000000904000D	646
ES.PE_WRAP_TOP.TPC.EPS.FIR.MODE_REG	0x0000000009040008	645
ES.PE_WRAP_TOP.TPC.EPS.PSC.DEBUG_STATUS_REG	0x0000000009010004	633
ES.PE_WRAP_TOP.TPC.EPS.PSC.PSCOM_MODE_REG	0x0000000009010000	630
ES.PE_WRAP_TOP.TPC.EPS.THERM.CPM_CONFIG_WRITE_REG0	0x0000000009050000	655
ES.PE_WRAP_TOP.TPC.EPS.THERM.DTS_RESULT0	0x0000000009050000	656
ES.PE_WRAP_TOP.TPC.ERROR_STATUS	0x0000000009030009	642
ES.PE_WRAP_TOP.TPC.FIR_MASK	0x0000000009040002	644
ES.PE_WRAP_TOP.TPC.GP0	0x0000000009000000	47
ES.PE_WRAP_TOP.TPC.GP1	0x0000000009000001	628
ES.PE_WRAP_TOP.TPC.GP2	0x0000000009000002	628
ES.PE_WRAP_TOP.TPC.GP4	0x0000000009000003	629
ES.PE_WRAP_TOP.TPC.LOCAL_FIR	0x000000000904000A	645
ES.PE_WRAP_TOP.TPC.OPCG_REG0	0x0000000009030002	635
ES.PE_WRAP_TOP.TPC.OPCG_REG1	0x0000000009030003	636
ES.PE_WRAP_TOP.TPC.OPCG_REG2	0x0000000009030004	636
ES.PE_WRAP_TOP.TPC.OPCG_REG3	0x0000000009030005	638
ES.PE_WRAP_TOP.TPC.RFIR	0x0000000009040001	643
ES.PE_WRAP_TOP.TPC.SCANSELQ	0x0000000009030007	639
ES.PE_WRAP_TOP.TPC.SPATTN	0x0000000009040004	644
ES.PE_WRAP_TOP.TPC.SPA_MASK	0x0000000009040007	644
ES.PE_WRAP_TOP.TPC.TRA.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	0x0000000009010400	633
ES.PE_WRAP_TOP.TPC.TRA.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	0x0000000009010401	633
ES.PE_WRAP_TOP.TPC.XFIR	0x0000000009040000	643
EX03.EC.FX.T2_XER	0x0000000000010002	52
EX03.EC.FX.T3_XER	0x0000000000010003	53
EX03.EC.FX.T5_XER	0x0000000000010005	54
EXP.EC.PC.SCR0	0x0000000000000008	671
EXP.EC.PC.SCR1	0x0000000000000009	671
EXP.TP.ECO_DOM.GP0	0x0000000010000000	658
IOMC0.BUSCTL.SCOM.FIR_MASK_REG	0x0000000002011A03	456
IOMC0.BUSCTL.SCOM.FIR_REG	0x0000000002011A00	454
IOMC0.BUSCTL.SCOM.SCOM_MODE_PB	0x0000000002011A20	453
IOMC1.BUSCTL.SCOM.FIR_REG	0x0000000002011E00	457
IOP.IOP_X880.IOP_PMA0.IOP_PMA_PLL0.IOP_PMA_PLL_RLM.IOP_PMA_PLL_REG_CON TROL.FIR_ACTION0_REG	0x0000000009011406	651



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Mnemonic	Address	Page
IOP.IOP_X880.IOP_PMA0.IOP_PMA_PLL0.IOP_PMA_PLL_RLM.IOP_PMA_PLL_REG_CON TROL.FIR_ACTION1_REG	0x0000000009011407	652
IOP.IOP_X880.IOP_PMA0.IOP_PMA_PLL0.IOP_PMA_PLL_RLM.IOP_PMA_PLL_REG_CON TROL.FIR_MASK_REG	0x0000000009011403	651
IOP.IOP_X880.IOP_PMA0.IOP_PMA_PLL0.IOP_PMA_PLL_RLM.IOP_PMA_PLL_REG_CON TROL.FIR_STATUS_REG	0x0000000009011400	650
IOP.IOP_X880.IOP_PMA0.IOP_PMA_PLL0.IOP_PMA_PLL_RLM.IOP_PMA_PLL_REG_CON TROL.FIR_WOF_REG	0x0000000009011408	652
IOP.IOP_X881.IOP_PMA0.IOP_PMA_PLL0.IOP_PMA_PLL_RLM.IOP_PMA_PLL_REG_CON TROL.FIR_ACTION0_REG	0x0000000009011846	654
IOP.IOP_X881.IOP_PMA0.IOP_PMA_PLL0.IOP_PMA_PLL_RLM.IOP_PMA_PLL_REG_CON TROL.FIR_ACTION1_REG	0x0000000009011847	654
IOP.IOP_X881.IOP_PMA0.IOP_PMA_PLL0.IOP_PMA_PLL_RLM.IOP_PMA_PLL_REG_CON TROL.FIR_MASK_REG	0x0000000009011843	653
IOP.IOP_X881.IOP_PMA0.IOP_PMA_PLL0.IOP_PMA_PLL_RLM.IOP_PMA_PLL_REG_CON TROL.FIR_STATUS_REG	0x0000000009011840	652
IOP.IOP_X881.IOP_PMA0.IOP_PMA_PLL0.IOP_PMA_PLL_RLM.IOP_PMA_PLL_REG_CON TROL.FIR_WOF_REG	0x0000000009011848	654
MC0.MCS0.LEFT.LEFT.MCEPSQ	0x0000000002011816	445
MC0.MCS0.LEFT.LEFT.MCFGPAQ	0x0000000002011814	444
MC0.MCS0.LEFT.LEFT.MCFGPMAQ	0x0000000002011815	445
MC0.MCS0.LEFT.LEFT.MCFGPMQ	0x0000000002011801	437
MC0.MCS0.LEFT.LEFT.MCFGPQ	0x0000000002011800	437
MC0.MCS0.LEFT.LEFT.MCFGPRQ	0x0000000002011802	438
MC0.MCS0.LEFT.LEFT.MCMODE0Q	0x0000000002011807	438
MC0.MCS0.LEFT.LEFT.MCMODE1Q	0x0000000002011808	440
MC0.MCS0.LEFT.LEFT.MCMODE3Q	0x000000000201180A	442
MC0.MCS0.LEFT.LEFT.MCMODE4Q	0x000000000201181A	443
MC0.MCS0.LEFT.LEFT.MCSYNQ	0x000000000201180B	441
MC0.MCS0.RIGHT.MCICFGQ	0x000000000201184A	451
MC0.MCS0.RIGHT.MCICRCSYNQ	0x000000000201184C	453
MC0.MCS0.RIGHT.MCIFIRACT0	0x0000000002011846	450
MC0.MCS0.RIGHT.MCIFIRACT1	0x0000000002011847	451
MC0.MCS0.RIGHT.MCIFIRMASK	0x0000000002011843	449
MC0.MCS0.RIGHT.MCIFIRQ	0x0000000002011840	446
MC0.MCS0.RIGHT.MCISTATQ	0x000000000201184B	452
MC2.MCS0.RIGHT.MCIFIRQ	0x0000000002011C40	459
MC2.MCS1.RIGHT.MCIFIRQ	0x0000000002011CC0	462
MC3.MCS0.RIGHT.MCIFIRQ	0x0000000002011D40	465
MC3.MCS1.RIGHT.MCIFIRQ	0x0000000002011DC0	468
PSI.PSI_MAC.PSI_SCOM.FIR_MASK_REG	0x0000000004012403	576
PSI.PSI_MAC.PSI_SCOM.FIR_REG	0x0000000004012400	576
PSI.PSI_MAC.PSI_SCOM.PSI_SCOM_REGS.RX_PSI_CNTL	0x0000000004012420	576
PSI.PSI_MAC.PSI_SCOM.PSI_SCOM_REGS.RX_PSI_STATUS	0x0000000004012422	578
PSI.PSI_MAC.PSI_SCOM.PSI_SCOM_REGS.TX_PSI_CNTL	0x0000000004012430	578
TPC.FSI.FSI_MAILBOX.FSXCOMP.FSXLOG.GPWRP	0x0000000000002818	51
XBUS01.X0.BUSCTL.SCOM.FIR_MASK_REG	0x0000000004011003	591
XBUS01.X0.BUSCTL.SCOM.FIR_REG	0x0000000004011000	589
XBUS01.X0.BUSCTL.SCOM.SCOM_MODE_PB	0x0000000004011020	595
XBUS01.X1.BUSCTL.SCOM.FIR_REG	0x0000000004011400	593

The POWER8 Processor registers are listed in the following tables.

Register Name		GP Register 0		
Mnemonic		ES.PE_WRAP_TOP.TPC.GP0		
Address		0000000009000000 (PCB) 0000000009000004 (PCB1) 0000000009000005 (PCB2)		
Attributes				
Description				
Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	NOT_USED0: Not used. Reset (0b0).
1	RWX	WOX_AND	WOX_OR	TC_SYNCCLK_MUXSEL_DC: Select the sync clock for asynchronous latches (initial value is 1). Reset (0b1).
2	RWX	WOX_AND	WOX_OR	TC_GPIO_FLUSHMODE_INH_DC: Prevent plats from going into flush mode (initial value is 1), Reset (0b1).
3	RWX	WOX_AND	WOX_OR	TC_GPIO_FORCEALIGN: Force align signal to be sent (initial value is 1, drop before dropping flushmode_inh). Reset (0b1).
4	RWX	WOX_AND	WOX_OR	NOT_USED1: Not used. Reset (0b0).
5	RWX	WOX_AND	WOX_OR	NOT_USED2: Not used. Reset (0b0).
6	RWX	WOX_AND	WOX_OR	TC_SCAN_DIS_DC_B: Disable scan; set output of scan chain to zero. Reset (0b0).
7	RWX	WOX_AND	WOX_OR	NOT_USED3: Not used. Reset (0b0).
8	RWX	WOX_AND	WOX_OR	TC_LBIST_EN_DC: LBIST mode. Reset (0b0).
9	RWX	WOX_AND	WOX_OR	TC_LBIST_AC_MODE_DC: LBIST ac mode. Reset (0b0).
10	RWX	WOX_AND	WOX_OR	TC_LBIST_ARY_WRT_THRU_DC: Array write-through mode; set array in bypass mode. Reset (0b0).
11	RWX	WOX_AND	WOX_OR	TC_ABIST_MODE_DC: Set during ABIST. Reset (0b0).
12	RWX	WOX_AND	WOX_OR	TC_ABIST_START_TEST_DC: Set to start ABIST testing. Reset (0b0).
13	RWX	WOX_AND	WOX_OR	NOT_USED4: Not used. Reset (0b0).
14	RWX	WOX_AND	WOX_OR	TC_ATPG_EN_DC: ATPG mode. Reset (0b0).
15	RWX	WOX_AND	WOX_OR	TC_SCAN_PROTECT_DC: Scan protection enable (initial value is 1). Reset (0b1).
16	RWX	WOX_AND	WOX_OR	NOT_USED5: Not used. Reset (0b1).
17	RWX	WOX_AND	WOX_OR	NOT_USED6: Not used. Reset (0b0).
18	RWX	WOX_AND	WOX_OR	NOT_USED7: Not used. Reset (0b0).
19	RWX	WOX_AND	WOX_OR	NOT_USED8: not used. Reset (0b1).
20	RWX	WOX_AND	WOX_OR	TC_DBG_TRACE_START: Start trace to debug macros. Reset (0b0).
21	RWX	WOX_AND	WOX_OR	TC_DBG_TRACE_STOP: Stop trace to debug macros. Reset (0b0).
22	RWX	WOX_AND	WOX_OR	TC_DBG_TRACE_RESET: Reset trace to debug macros. Reset (0b0).



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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
23	RWX	WOX_AND	WOX_OR	NOT_USED9: Not used. Reset (0b0).
24:25	RWX	WOX_AND	WOX_OR	TC_GPIO_CLKDIV_SEL_DC: Select clock divider ratio for probing. Reset (0b0).
26	RWX	WOX_AND	WOX_OR	NOT_USED10: Not used. Reset (0b0).
27	RWX	WOX_AND	WOX_OR	TC_IOBIST_TX_WRAP_ENABLE_DC: 0. Reset (0b0).
28:31	RWX	WOX_AND	WOX_OR	TC_DBG_MUXSEL_DC: Nest debug bus selects(0:3). Reset (0b0).
32:39	RWX	WOX_AND	WOX_OR	TC_PSRO_SEL_DC: PSRO selects(0:7). Reset (0b0).
40:42	RWX	WOX_AND	WOX_OR	TC_NODE_ID_DC: Node ID. Reset (0b0).
43:45	RWX	WOX_AND	WOX_OR	TC_CHIP_ID_DC: Chip ID. Reset (0b0).
46	RWX	WOX_AND	WOX_OR	TC_BSC_WRAPSEL_DC: Wrap select for BSC. Reset (0b0).
47	RWX	WOX_AND	WOX_OR	TC_BSC_INTMODE_DC: Int mode for BSC. Reset (0b0).
48	RWX	WOX_AND	WOX_OR	TC_PCI0_IOVALID_DC: I/O valid for PCI0. Reset (0b0).
49	RWX	WOX_AND	WOX_OR	TC_PCI1_IOVALID_DC: I/O valid for PCI1. Reset (0b0).
50	RWX	WOX_AND	WOX_OR	TC_PCI2_IOVALID_DC: I/O valid for PCI2. Reset (0b0).
51	RWX	WOX_AND	WOX_OR	NOT_USED11: Not used. Reset (0b0).
52	RWX	WOX_AND	WOX_OR	TP_PCI0_REFCLK_DRVR_EN_DC: High-Z the PCI0 refclk driver. Reset (0b0).
53	RWX	WOX_AND	WOX_OR	TP_PCI1_REFCLK_DRVR_EN_DC: High-Z the PCI1 refclk driver. Reset (0b0).
54	RWX	WOX_AND	WOX_OR	TP_PCI2_REFCLK_DRVR_EN_DC: High-Z the PCI2 refclk driver. Reset (0b0).
55	RWX	WOX_AND	WOX_OR	NOT_USED12: Not used. Reset (0b0).
56	RWX	WOX_AND	WOX_OR	NOT_USED13: Not used. Reset (0b0).
57	RWX	WOX_AND	WOX_OR	NOT_USED14: Not used. Reset (0b0).
58	RWX	WOX_AND	WOX_OR	NOT_USED15: Not used. Reset (0b0).
59	RWX	WOX_AND	WOX_OR	NOT_USED16: Not used. Reset (0b0).
60	RWX	WOX_AND	WOX_OR	TC_MASK_CC_PCB_ERR_DC: Mask for pcb error (access or parity) in CC. Reset (0b0).
61	RWX	WOX_AND	WOX_OR	TC_MASK_CC_SCAN_OPCG_ERR_DC: Mask for pcb write while OPCG_IP / scan collision in CC. Reset (0b0).
62	RWX	WOX_AND	WOX_OR	NOT_USED17: Not used. Reset (0b1).
63	RWX	WOX_AND	WOX_OR	TC_FENCE_PERV_DC: Fence pervasive logic during scan (initial value is 1), Reset (0b1).

Register Name	GP Register 0
Mnemonic	ES.PBES_WRAP_TOP.TPC.GP0
Address	0000000008000000 (PCB) 0000000008000004 (PCB1) 0000000008000005 (PCB2)
Attributes	
Description	



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	NOT_USED0: Not used. Reset (0b0).
1	RWX	WOX_AND	WOX_OR	TC_SYNCCLK_MUXSEL_DC: Select the sync clock for asynchronous latches (initial value is 1). Reset (0b1).
2	RWX	WOX_AND	WOX_OR	TC_GPIO_FLUSHMODE_INH_DC: Prevent plats from going into flush mode (initial value is 1). Reset (0b1).
3	RWX	WOX_AND	WOX_OR	TC_GPIO_FORCEALIGN: Force align signal to be sent (initial value is 1; drop before dropping flushmode_inh). Reset (0b1).
4	RWX	WOX_AND	WOX_OR	NOT_USED1: Not used. Reset (0b0).
5	RWX	WOX_AND	WOX_OR	NOT_USED2: Not used. Reset (0b0).
6	RWX	WOX_AND	WOX_OR	TC_SCAN_DIS_DC_B: Disable scan; set output of scan chain to zero. Reset (0b0).
7	RWX	WOX_AND	WOX_OR	TC_SKIT_MODE_BIST_DC: Enable skitter measuring during BIST. Reset (0b0).



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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
8	RWX	WOX_AND	WOX_OR	TC_LBIST_EN_DC: LBIST mode. Reset (0b0).
9	RWX	WOX_AND	WOX_OR	TC_LBIST_AC_MODE_DC: LBIST ac mode. Reset (0b0).
10	RWX	WOX_AND	WOX_OR	TC_LBIST_ARY_WRT_THRU_DC: Array write-through mode; set array in bypass mode. Reset (0b0).
11	RWX	WOX_AND	WOX_OR	TC_ABIST_MODE_DC: Set during ABIST. Reset (0b0).
12	RWX	WOX_AND	WOX_OR	TC_ABIST_START_TEST_DC: Set to start ABIST testing. Reset (0b0).
13	RWX	WOX_AND	WOX_OR	NOT_USED3: Not used. Reset (0b0).
14	RWX	WOX_AND	WOX_OR	TC_ATPG_EN_DC: ATPG mode. Reset (0b0).
15	RWX	WOX_AND	WOX_OR	TC_SCAN_PROTECT_DC: Scan protection enable (initial value is 1). Reset (0b1).
16	RWX	WOX_AND	WOX_OR	NOT_USED4: Not used. Reset (0b1)
17	RWX	WOX_AND	WOX_OR	NOT_USED5: Not used. Reset (0b0).
18	RWX	WOX_AND	WOX_OR	NOT_USED6: Not used. Reset (0b0).
19	RWX	WOX_AND	WOX_OR	NOT_USED7: Not used. Reset (0b1).
20	RWX	WOX_AND	WOX_OR	TC_DBG_TRACE_START: Start trace to debug macros. Reset (0b0).
21	RWX	WOX_AND	WOX_OR	TC_DBG_TRACE_STOP: Stop trace to debug macros. Reset (0b0).
22	RWX	WOX_AND	WOX_OR	TC_DBG_TRACE_RESET: Reset trace to debug macros. Reset (0b0).
23	RWX	WOX_AND	WOX_OR	NOT_USED8: Not used. Reset (0b0).
24:25	RWX	WOX_AND	WOX_OR	TC_GPIO_CLKDIV_SEL_DC: Select clock divider ratio for probing. Reset (0b0).
26	RWX	WOX_AND	WOX_OR	NOT_USED9: Not used. Reset (0b0).
27	RWX	WOX_AND	WOX_OR	TC_IOBIST_TX_WRAP_ENABLE_DC: 0. Reset (0b0).
28:31	RWX	WOX_AND	WOX_OR	TC_DBG_MUXSEL_DC: Nest debug bus selects(0:3). Reset (0b0).
32:39	RWX	WOX_AND	WOX_OR	TC_PSRO_SEL_DC: PSRO selects(0:7). Reset (0b0).
40:42	RWX	WOX_AND	WOX_OR	TC_NODE_ID_DC: Node ID. Reset (0b0).
43:45	RWX	WOX_AND	WOX_OR	TC_CHIP_ID_DC: Chip ID. Reset (0b0).
46	RWX	WOX_AND	WOX_OR	TC_BSC_WRAPSEL_DC: Wrap select for BSC. Reset (0b0).
47	RWX	WOX_AND	WOX_OR	TC_BSC_INTMODE_DC: Int mode for BSC. Reset (0b0).
48	RWX	WOX_AND	WOX_OR	TC_AB0_IOVALID_DC: I/O valid for AB0. Reset (0b0).
49	RWX	WOX_AND	WOX_OR	TC_AB1_IOVALID_DC: I/O valid for AB1. Reset (0b0).
50	RWX	WOX_AND	WOX_OR	TC_AB2_IOVALID_DC: I/O valid for AB2. Reset (0b0).
51	RWX	WOX_AND	WOX_OR	NOT_USED10: Not used. Reset (0b0).
52	RWX	WOX_AND	WOX_OR	NOT_USED11: Not used. Reset (0b0).
53	RWX	WOX_AND	WOX_OR	NOT_USED12: Not used. Reset (0b0).
54	RWX	WOX_AND	WOX_OR	NOT_USED13: Not used. Reset (0b0).
55	RWX	WOX_AND	WOX_OR	NOT_USED14: Not used. Reset (0b0).
56	RWX	WOX_AND	WOX_OR	NOT_USED15: Not used. Reset (0b0).
57	RWX	WOX_AND	WOX_OR	NOT_USED16: Not used. Reset (0b0).
58	RWX	WOX_AND	WOX_OR	NOT_USED17: Not used. Reset (0b0).
59	RWX	WOX_AND	WOX_OR	NOT_USED18: Not used. Reset (0b0).



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
60	RWX	WOX_AND	WOX_OR	TC_MASK_CC_PCB_ERR_DC: Mask for pcb error (access or parity) in CC. Reset (0b0).
61	RWX	WOX_AND	WOX_OR	TC_MASK_CC_SCAN_OPCG_ERR_DC: Mask for pcb write while OPCG_IP / scan collision in CC. Reset (0b0).
62	RWX	WOX_AND	WOX_OR	NOT_USED19: Not used. Reset (0b1).
63	RWX	WOX_AND	WOX_OR	TC_FENCE_PERV_DC: Fence pervasive logic during scan (initial value is 1). Reset (0b1).

Register Name	POR IBUF0: Status Register
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.IO_STATUS_REG
Address	0000000000060000 (PIB) 0000000040000000 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:7	ROX	ROX	I0_SM_STAT: Instruction engine state machine state: 000 & state_vector(0:3) & bad_instruction_parity
8	ROX	ROX	I0_FREEZE_PORE_ACTION_MASKED: Operation frozen due to SBE/PORE freeze action input (for example, system checkstop).
9	ROX	ROX	I0_EXE_TRIGGER_WR_REQ_Q: Interrupt pending. 0 = No interrupt pending. 1 = An interrupt is pending.
10:11	RO	RO	Constant = 0b00
12:15	ROX	ROX	I0_PC_STACK_CURRENT_STATE: Stack pointer. 0001 = Empty 0010 = Filled up to level 1 0100 = Filled up to level 2 0100 = Filled up to level 3 (error handler only)
16:63	ROX	ROX	I0_PC_Q: Program counter is fetch-address for POR instructions in 48-bit representation, counting in bytes. Initial value is x8000000000000000.

Register Name	GP Write Protection Register
Mnemonic	TPC.FSI.FSI_MAILBOX.FSXCOMP.FSXLOG.GPWRP
Address	0000000000002818 (FSI) 0000000000002860 (FSI_BYTE) 0000000000050018 (PIB)
Attributes	
Description	

Bits	FSI	FSI_BYTE	PIB	Field Mnemonic: Description
0:15	RWX	RWX	RWX	MAGIC_COOKIE: It needs to be programmed to 0x4453 for enabling write protection

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Bits	FSI	FSI_BYTE	PIB	Field Mnemonic: Description
16:31	RWX	RWX	RWX	EN_OR_DIS_WRITE_PROTECTION: If equal to xFFFF, disable write protection. If it is unequal to xFFFF, then this part along with magic cookie forms the: if equal to x'0003' : register number of GP3 if equal to x'0004' : register number of GP4 if equal to x'0005' : register number of GP5 if equal to x'0006' : register number of GP6 if equal to x'0007' : register number of GP7 if equal to x'0008' : register number of GProcessor if equal to x'001B' : register number of PERV_GP3

Register Name	Status Register
Mnemonic	EH.TPCHIP.PIB.OTP.OTPC_M.STATUS_REGISTER
Address	0000000000010002 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	ROX	STATUS_ADDR_NVLD: Address invalid
1	ROX	STATUS_WRITE_NVLD: Write invalid
2	ROX	STATUS_READ_NVLD: Read invalid
3	ROX	STATUS_INVLD_CMD_ERR: Invalid command register fields programmed
4	ROX	STATUS_CORR_ERR: ECC Correctable error
5	ROX	STATUS_UNCORR_ERROR: ECC uncorrectable error
6:37	ROX	STATUS_DATA_REG_0_31: Data Register (0 - 31)
38	RO	Constant = 0b0
39:43	ROX	STATUS_UNUSED_39_43: Unused
44	ROX	STATUS_CTRL_BUSY: OTP ROM controller busy
45	ROX	STATUS_DCOMP_ERR: Decompression engine error
46	ROX	STATUS_INVLD_PRGM_ERR: Invalid program operation error
47:51	ROX	STATUS_UNUSED_47_51: Unused
52	ROX	STATUS_COMMAND_COMPLETE: Operation complete - fast-mode read operation/programming operation
53	ROX	STATUS_UNUSED_53: Unused
54	ROX	STATUS_RDWR_OP_BUSY: Read/write operation controller Logic busy
55	ROX	STATUS_DCOMP_ENGINE_BUSY: Decompression engine busy
56:63	ROX	STATUS_RD_DATA_COUNT: Valid read data count - 0x08 for OTP ROM

Register Name	T2_XER
Mnemonic	EX03.EC.FX.T2_XER
Address	0000000000010002 (SPR_T2)
Attributes	
Description	Architected XER for Thread 20 (XER0)



Bits	SPR_T2	Field Mnemonic: Description
0:15	RO	Constant = 0b0000000000000000
16:63	RW	

Register Name	<i>Data Register for Fast Mode Read Data</i>
Mnemonic	EH.TPCHIP.PIB.OTP.OTPC_M.DATA_REGISTER
Address	0000000000010003 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	ROX	OTP_DATA_REGISTER: Fast-mode read data

Register Name	<i>T3 XER</i>
Mnemonic	EX03.EC.FX.T3_XER
Address	0000000000010003 (SPR_T3)
Attributes	
Description	Architected XER for Thread 30 (XER0)

Bits	SPR_T3	Field Mnemonic: Description
0:15	RO	Constant = 0b0000000000000000
16:63	RW	

Register Name	<i>Security Switch Register (For Secure Boot Features)</i>
Mnemonic	EH.TPCHIP.PIB.OTP.OTPC_M.SECURITY_SWITCH_REGISTER
Address	0000000000010005 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	ROX	SECURITY_SWITCH_SECURE_MODE: Indicates Trusted Boot Enabled from Jumper. '1' - In trusted mode
1	RWX	SECURITY_SWITCH_TRUSTED_BOOT: Trusted Boot Enable
2	RWX	SECURITY_SWITCH_PROT_SCOM_WR: Prevent write access to any SCOM (single or bulk access)
3	RWX	SECURITY_SWITCH_PROT_SCOM_RD: Prevent read access to any SCOM (single or bulk access)
4	RWX	SECURITY_SWITCH_PROT_SCAN: Prevent scan access (scan engine, side path, scan per SCOM)
5	RWX	SECURITY_SWITCH_PROT_EDRAM: Block L3 refresh on L3 clock stop and prevent access to core RAMing
6	RWX	SECURITY_SWITCH_PROT_MFSI: Prevent access to any master FSI links (POWER8 Memory Buffer or other PU)
7	RWX	SECURITY_SWITCH_PROT_I2C_PROM: Prevent write access to trusted SEEPROM from host (sticky!)
8	RWX	SECURITY_SWITCH_CORE_XSTOP: Prevent reopening SCOM and SCAN on core XSTOP
9	RWX	SECURITY_SWITCH_SYS_XSTOP: Prevent reopening SCOM and SCAN on System XSTOP

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Bits	PIB	Field Mnemonic: Description
10	RWX	SECURITY_SWITCH_PROT_EX_SPARE0: Spare going to EX
11	RWX	SECURITY_SWITCH_PROT_EX_SPARE1: Spare going to EX
12	RWX	SECURITY_SWITCH_PROT_TP_SPARE0: TP Spare
13	RWX	SECURITY_SWITCH_PROT_I2C_EXPANDER: Prevent read access to I2C expander from host (sticky)
14	RWX	SECURITY_SWITCH_PROT_CLKSTART: Prevent restarting clocks in chiplets and override scan protect
15	RWX	SECURITY_SWITCH_PROT_TP_SPARE1: TP spare

Register Name	T5 XER
Mnemonic	EX03.EC.FX.T5_XER
Address	0000000000010005 (SPR_T5)
Attributes	
Description	Architected XER for Thread 50 (XER0)

Bits	SPR_T5	Field Mnemonic: Description
0:15	RO	Constant = 0b0000000000000000
16:63	RW	

Register Name	Mode Register To Enable Features - Decomp Engine Enable, ECC Checking, Programming Enable
Mnemonic	EH.TPCHIP.PIB.OTP.OTPC_M.MODE_REGISTER
Address	0000000000010008 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	RW	MODE_DCOMP_ENABLE: To Enable Decompression Engine
1	RW	MODE_ECC_ENABLE: Write invalid
2	RW	MODE_PROGRAM_ENABLE: Read invalid
3:15	RW	MODE_UNUSED_3_15: Unused
16:31	RW	MODE_CLK_RATE_SEL: To select clock rate. Based on Tprg requirement of OTP ROM. Current Values – 40 MHz:0xC8, 200 MHz:0x3E8, 800 MHz : 0xFA0

Register Name	To Program eFuse Locations
Mnemonic	EH.TPCHIP.PIB.OTP.OTPC_M.PRGM_REGISTER
Address	0000000000010009 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:31	RW	PRGM_PRGM_ADDR: Address of OTP ROM location to be programmed
32:37	RW	PRGM_PRG_BIT_LOCATION: Bit location in 64 bits to be fused



Register Name		<i>Contains Part 0 of the eFuse</i>
Mnemonic		EH.TPCHIP.OTPROM.MULT_OTP_ROM_ECC_2_8.OTPROM_GEN#0.DATA_OTPROM.ECID_PART0_REGISTER
Address		0000000000018000 (PIB)
Attributes		
Description		
Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_0: 0 address location

Register Name		<i>Contains Part 1 of the eFuse</i>
Mnemonic		EH.TPCHIP.OTPROM.MULT_OTP_ROM_ECC_2_8.OTPROM_GEN#0.DATA_OTPROM.ECID_PART1_REGISTER
Address		0000000000018001 (PIB)
Attributes		
Description		
Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_1: 1 address location

Register Name		<i>Contains Part 12 of the eFuse</i>
Mnemonic		EH.TPCHIP.OTPROM.MULT_OTP_ROM_ECC_2_8.OTPROM_GEN#0.DATA_OTPROM.ECID_PART12_REGISTER
Address		000000000001800C (PIB)
Attributes		
Description		
Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_12: 12 address location

Register Name		<i>Contains Part 13 of the eFuse</i>
Mnemonic		EH.TPCHIP.OTPROM.MULT_OTP_ROM_ECC_2_8.OTPROM_GEN#0.DATA_OTPROM.ECID_PART13_REGISTER
Address		000000000001800D (PIB)
Attributes		
Description		
Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_13: 13 address location



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Register Name			<i>Contains Part 14 of the eFuse</i>
Mnemonic			EH.TPCHIP.OTPROM.MULT_OTP_ROM_ECC_2_8.OTPROM_GEN#0.DATA_OTPROM.ECID_PART14_REGISTER
Address			000000000001800E (PIB)
Attributes			
Description			
Bits	PIB	Field Mnemonic: Description	
0:63	RW	ECID_PART_14: 14 address location	

Register Name			<i>Contains Part 15 of the eFuse</i>
Mnemonic			EH.TPCHIP.OTPROM.MULT_OTP_ROM_ECC_2_8.OTPROM_GEN#0.DATA_OTPROM.ECID_PART15_REGISTER
Address			000000000001800F (PIB)
Attributes			
Description			
Bits	PIB	Field Mnemonic: Description	
0:63	RW	ECID_PART_15: 15 address location	

Register Name			<i>Contains Part 16 of the eFuse</i>
Mnemonic			EH.TPCHIP.OTPROM.MULT_OTP_ROM_ECC_2_8.OTPROM_GEN#0.DATA_OTPROM.ECID_PART16_REGISTER
Address			0000000000018010 (PIB)
Attributes			
Description			
Bits	PIB	Field Mnemonic: Description	
0:63	RW	ECID_PART_16: 16 address location	

Register Name			<i>Contains Part 17 of the eFuse</i>
Mnemonic			EH.TPCHIP.OTPROM.MULT_OTP_ROM_ECC_2_8.OTPROM_GEN#0.DATA_OTPROM.ECID_PART17_REGISTER
Address			0000000000018011 (PIB)
Attributes			
Description			
Bits	PIB	Field Mnemonic: Description	
0:63	RW	ECID_PART_17: 17 address location	



Register Name			<i>Contains Part 18 of the eFuse</i>
Mnemonic			EH.TPCHIP.OTPROM.MULT_OTP_ROM_ECC_2_8.OTPROM_GEN#0.DATA_OTPROM.ECID_PART18_REGISTER
Address			0000000000018012 (PIB)
Attributes			
Description			
Bits	PIB	Field Mnemonic: Description	
0:63	RW	ECID_PART_18: 18 address location	

Register Name			<i>Contains Part 19 of the eFuse</i>
Mnemonic			EH.TPCHIP.OTPROM.MULT_OTP_ROM_ECC_2_8.OTPROM_GEN#0.DATA_OTPROM.ECID_PART19_REGISTER
Address			0000000000018013 (PIB)
Attributes			
Description			
Bits	PIB	Field Mnemonic: Description	
0:63	RW	ECID_PART_19: 19 address location	

Register Name			<i>Contains Part 20 of the eFuse</i>
Mnemonic			EH.TPCHIP.OTPROM.MULT_OTP_ROM_ECC_2_8.OTPROM_GEN#0.DATA_OTPROM.ECID_PART20_REGISTER
Address			0000000000018014 (PIB)
Attributes			
Description			
Bits	PIB	Field Mnemonic: Description	
0:63	RW	ECID_PART_20: 20 address location	

Register Name			<i>Contains Part 21 of the eFuse</i>
Mnemonic			EH.TPCHIP.OTPROM.MULT_OTP_ROM_ECC_2_8.OTPROM_GEN#0.DATA_OTPROM.ECID_PART21_REGISTER
Address			0000000000018015 (PIB)
Attributes			
Description			
Bits	PIB	Field Mnemonic: Description	
0:63	RW	ECID_PART_21: 21 address location	

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Register Name		<i>Contains Part 22 of the eFuse</i>
Mnemonic		EH.TPCHIP.OTPROM.MULT_OTP_ROM_ECC_2_8.OTPROM_GEN#0.DATA_OTPROM.ECID_PART22_REGISTER
Address		0000000000018016 (PIB)
Attributes		
Description		
Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_22: 22 address location

Register Name		<i>Contains Part 23 of the eFuse</i>
Mnemonic		EH.TPCHIP.OTPROM.MULT_OTP_ROM_ECC_2_8.OTPROM_GEN#0.DATA_OTPROM.ECID_PART23_REGISTER
Address		0000000000018017 (PIB)
Attributes		
Description		
Bits	PIB	Field Mnemonic: Description
0:63	RW	ECID_PART_23: 23 address location

Register Name		<i>TOD: Secondary Configuration: Distribution Port-0 Control Register</i>
Mnemonic		EH.TPCHIP.PIB.TOD.TOD_SEC_PORT_0_CTRL_REG
Address		0000000000040003 (PIB)
Attributes		
Description		
Bits	PIB	Field Mnemonic: Description
0:2	RW	SEC_PORT_0_RX_SELECT: Distribution: secondary configuration: port-0 rx select: A0_PORT_0=>0b000 A1_PORT_0=>0b001 A2_PORT_0=>0b010 X0_PORT_0=>0b011 X1_PORT_0=>0b100 X2_PORT_0=>0b101 X3_PORT_0=>0b110 X4_PORT_0=>0b111
3	RW	REG_0X03_SPARE_03: spares
4:5	RWX	SEC_A0_PORT_0_TX_SELECT: Distribution: secondary configuration: A0 port-0 tx select: S_PATH_0=>0b00 S_PATH_1=>0b01 M_PATH_0=>0b10 M_PATH_1=>0b11
6:7	RWX	SEC_A1_PORT_0_TX_SELECT: Distribution: secondary configuration: A1 port-0 tx select: S_PATH_0=>0b00 S_PATH_1=>0b01 M_PATH_0=>0b10 M_PATH_1=>0b11

Bits	PIB	Field Mnemonic: Description
8:9	RWX	SEC_A2_PORT_0_TX_SELECT: Distribution: secondary configuration: A2 port-0 tx select: S_PATH_0=>0b00 S_PATH_1=>0b01 M_PATH_0=>0b10 M_PATH_1=>0b11
10:11	RWX	SEC_X0_PORT_0_TX_SELECT: Distribution: secondary configuration: X0 port-0 tx select: S_PATH_0=>0b00 S_PATH_1=>0b01 M_PATH_0=>0b10 M_PATH_1=>0b11
12:13	RWX	SEC_X1_PORT_0_TX_SELECT: Distribution: secondary configuration: X1 port-0 tx select: S_PATH_0=>0b00 S_PATH_1=>0b01 M_PATH_0=>0b10 M_PATH_1=>0b11
14:15	RWX	SEC_X2_PORT_0_TX_SELECT: Distribution: secondary configuration: X2 port-0 tx select: S_PATH_0=>0b00 S_PATH_1=>0b01 M_PATH_0=>0b10 M_PATH_1=>0b11
16:17	RWX	SEC_X3_PORT_0_TX_SELECT: Distribution: secondary configuration: X3 port-0 tx select: S_PATH_0=>0b00 S_PATH_1=>0b01 M_PATH_0=>0b10 M_PATH_1=>0b11
18:19	RWX	SEC_X4_PORT_0_TX_SELECT: Distribution: secondary configuration: X3 port-0 tx select: S_PATH_0=>0b00 S_PATH_1=>0b01 M_PATH_0=>0b10 M_PATH_1=>0b11
20	RW	SEC_A0_PORT_0_TX_ENABLE: Distribution: secondary configuration: A0 port-0 tx enable OFF: Port configured as receiver ON: Port configured as sender
21	RW	SEC_A1_PORT_0_TX_ENABLE: Distribution: secondary configuration: A1 port-0 tx enable OFF: Port configured as receiver ON: Port configured as sender
22	RW	SEC_A2_PORT_0_TX_ENABLE: Distribution: secondary configuration: A2 port-0 tx enable OFF: Port configured as receiver ON: Port configured as sender
23	RW	SEC_X0_PORT_0_TX_ENABLE: Distribution: secondary configuration: X0 port-0 tx enable OFF: Port configured as receiver ON: Port configured as sender
24	RW	SEC_X1_PORT_0_TX_ENABLE: Distribution: secondary configuration: X1 port-0 tx enable OFF: Port configured as receiver ON: Port configured as sender
25	RW	SEC_X2_PORT_0_TX_ENABLE: Distribution: secondary configuration: X2 port-0 tx enable OFF: Port configured as receiver ON: Port configured as sender

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Bits	PIB	Field Mnemonic: Description
26	RW	SEC_X3_PORT_0_TX_ENABLE: Distribution: secondary configuration: X3 port-0 tx enable OFF: Port configured as receiver ON: Port configured as sender
27	RW	SEC_X4_PORT_0_TX_ENABLE: Distribution: secondary configuration: X4 port-0 tx enable OFF: Port configured as receiver ON: Port configured as sender
28:31	RW	REG_0X03_SPARE_28_31: Spares
32:39	RW	SEC_I_PATH_DELAY_VALUE: Internal path: secondary configuration: delay value
40:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	TOD: Master Path Status Register
Mnemonic	EH.TPCHIP.PIB.TOD.TOD_M_PATH_STATUS_REG
Address	0000000000040009 (PIB)
Attributes	
Description	TOD: Master Path Status Register Containing: - Step Alignment Threshold - Cycle-per-step (CPS) TOD Reset Triggering: A write into this register triggers the following resets (if the corresponding enable bits in reg_0x0B are active. - Master Path-0 Step Creation CPS Counter Reset - Master Path-0 Step Alignment Threshold Reset - Master Path-1 Step Creation CPS Counter Reset - Master Path-1 Step Alignment Threshold Reset

Bits	PIB	Field Mnemonic: Description
0:7	RWX	M_PATH_0_STEP_ALIGN_THRESHOLD: Master path-0: step align threshold
8:15	RWX	M_PATH_0_CPS: Master path-0: CPS
16:23	RWX	M_PATH_1_STEP_ALIGN_THRESHOLD: Master path-1: step align threshold
24:31	RWX	M_PATH_1_CPS: Master path-1: CPS
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name		TOD: TX TTYPE-1 Triggering Register
Mnemonic		EH.TPCHIP.PIB.TOD.TOD_TX_TTYPE_1_REG
Address		0000000000040012 (PIB)
Attributes		
Description		
Bits	PIB	Field Mnemonic: Description
0	WO	TX_TTYPE_1_TRIGGER: TX TTYPE-1 trigger
1:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000



Register Name		<i>TOD: TX TTYPE-2 Triggering Register</i>
Mnemonic		EH.TPCHIP.PIB.TOD.TOD_TX_TTYPE_2_REG
Address		000000000040013 (PIB)
Attributes		
Description		
Bits	PIB	Field Mnemonic: Description
0	WO	TX_TTYPE_2_TRIGGER: TX TTYPE-2 trigger
1:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name		<i>TOD: TX TTYPE-3 Triggering Register</i>
Mnemonic		EH.TPCHIP.PIB.TOD.TOD_TX_TTYPE_3_REG
Address		000000000040014 (PIB)
Attributes		
Description		
Bits	PIB	Field Mnemonic: Description
0	WO	TX_TTYPE_3_TRIGGER: TX TTYPE-3 trigger
1:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name		<i>TOD: TX TTYPE-4 Triggering Register</i>
Mnemonic		EH.TPCHIP.PIB.TOD.TOD_TX_TTYPE_4_REG
Address		000000000040015 (PIB)
Attributes		
Description		
Bits	PIB	Field Mnemonic: Description
0	WO	TX_TTYPE_4_TRIGGER: TX TTYPE-4 trigger
1:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name		<i>TOD: TX TTYPE-5 Triggering Register</i>
Mnemonic		EH.TPCHIP.PIB.TOD.TOD_TX_TTYPE_5_REG
Address		000000000040016 (PIB)
Attributes		
Description		
Bits	PIB	Field Mnemonic: Description
0	WO	TX_TTYPE_5_TRIGGER: TX TTYPE-5 trigger
1:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000



Register Name		TOD: Trace Data-67 Register
Mnemonic		EH.TPCHIP.PIB.TOD.TOD_TRACE_DATA_3_REG
Address		000000000004001F (PIB)
Attributes		
Description		
Bits	PIB	Field Mnemonic: Description
0:63	RO	REG_0X1F_SPARE_00_63: spares

Register Name		TOD: Time Value Register 60-bit TOD And 4-bit Who's-On-first(WOF) Incrementers
Mnemonic		EH.TPCHIP.PIB.TOD.TOD_VALUE_REG
Address		0000000000040020 (PIB)
Attributes		
Description		
Bits	PIB	Field Mnemonic: Description
0:59	ROX	TOD_VALUE: Internal path: Time-of-day register value
60:63	RWX	WOF_COUNTER_VALUE: Who's-On-first (WOF): counter value

Register Name		TOD: Load Register TOD Incrementer
Mnemonic		EH.TPCHIP.PIB.TOD.TOD_LOAD_TOD_REG
Address		0000000000040021 (PIB)
Attributes		
Description		TOD: Load Register TOD Incrementer: 60-bit TOD and 4-bit WOF, on read: returns all ZEROS. When TOD not running, on write: go to wait for sync state when DataBit(63) = 0 (load TOD), else go to stopped state (load TOD Data63).
Bits	PIB	Field Mnemonic: Description
0:59	RWX	LOAD_TOD_VALUE: Internal path: load TOD value
60:63	RWX	WOF: Who's-On-first(WOF) incrementer

Register Name		TOD: Start TOD Triggering Register
Mnemonic		EH.TPCHIP.PIB.TOD.TOD_START_TOD_REG
Address		0000000000040022 (PIB)
Attributes		
Description		TOD: Start TOD Triggering Register go to running state when DataBit(02) = 0, else go to wait for sync state
Bits	PIB	Field Mnemonic: Description
0	WO	FSM_START_TOD_TRIGGER: FSM: start_tod trigger
1	RW	REG_0X22_SPARE_01: Spares
2	WO	FSM_START_TOD_DATA02: FSM: start_tod_data02 trigger
3:7	RW	REG_0X22_SPARE_03_07: spares
8:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

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Register Name	TOD: Low Order Step Register	
Mnemonic	EH.TPCHIP.PIB.TOD.TOD_LOW_ORDER_STEP_REG	
Address	000000000040023 (PIB)	
Attributes		
Description		

Bits	PIB	Field Mnemonic: Description
0:5	RWX	LOW_ORDER_STEP_COUNTER_VALUE: Low Order Step: counter value used for USE_OSC_B configuration for internal step creation.
6:7	RW	REG_0X23_SPARE_06_07: spares
8:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	TOD: FSM Register	
Mnemonic	EH.TPCHIP.PIB.TOD.TOD_FSM_REG	
Address	000000000040024 (PIB)	
Attributes		
Description		

Bits	PIB	Field Mnemonic: Description
0:3	RWX	I_PATH_FSM_STATE: Internal path. TOD FSM state (TOD is running in the following states: x'02', x'0A', x'0E') 0000 = ERROR NOT_SET=>0b0111 STOPPED=>0b0001 WAIT_FOR_SYNC=>0b1101 RUNNING_2=>0b0010 RUNNING_A=>0b1010 RUNNING_E=>0b1110
4	ROX	TOD_IS_RUNNING: TOD running indicator.
5:7	RW	REG_0X24_SPARE_05_07: Spares
8:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	TOD: TX TType Control Register	
Mnemonic	EH.TPCHIP.PIB.TOD.TOD_TX_TTYPE_CTRL_REG	
Address	000000000040027 (PIB)	
Attributes		
Description		

Bits	PIB	Field Mnemonic: Description
0:2	ROX	TX_TTYPE_PIB_FSM_STATE: TX TType: PIB master FSM state PS_IDLE=>0b000 PS_REQFBC=>0b100 PS_REQTOD=>0b101 PS_WAITFBC=>0b110 PS_WAITTOD=>0b111
3:23	RW	REG_0X27_SPARE_03_23: spares



Bits	PIB	Field Mnemonic: Description
24:31	RW	TX_TTYPE_PIB_MST_ADDR_CFG: TX TType: PIB master address configuration. Configuration of PIB core chiplet address. Needs to be configured before issuing a move_chip_TOD_to_TB command. 0: reserved 1: Multicast Bit (0b1 for multicast) 2-7: PIB slave address = 0b01xxxx where xxxx is the core ID
32	RW	TX_TTYPE_4_SEND_MODE: TX TType: Ttype-4 send mode. Qualifying of TType4 sent out via Fabric when receiving a TType-3 via Fabric. Needs to be configured before issuing a TType-3 command. OFF: Send out TType-4 if TOD is master ON: Send out TType-4 if enabled (bit 33)
33	RW	TX_TTYPE_4_SEND_ENABLE: TX TType: Ttype-4 send enable. OFF: Disabled to send out TType-4 ON: Enabled to send out TType-4
34:39	RW	REG_0X27_SPARE_34_39: Spares.
40:63	RO	Constant = 0b000000000000000000000000

Register Name	TOD: RX TType Control Register Register
Mnemonic	EH.TPCHIP.PIB.TOD.TOD_RX_TTYPE_CTRL_REG
Address	0000000000040029 (PIB)
Attributes	
Description	RX TType Control Register Register used by the Alter-Display Unit (ADU) to transmit the TType data it receives from the processor bus.

Bits	PIB	Field Mnemonic: Description
0:63	RW	RX_TTYPE_DATA: RX TType: data Refer to section 1.7.7.1. TType Format of the workbook for the data format.

Register Name	TOD: Error And Interrupt Register
Mnemonic	EH.TPCHIP.PIB.TOD.TOD_ERROR_REG
Address	0000000000040030 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	RWX	REG_0X00_DATA_PARITY_ERROR: Error: master path control register (0x00): data parity error
1	RWX	M_PATH_0_PARITY_ERROR: Error: master path-0: parity error
2	RWX	M_PATH_1_PARITY_ERROR: Error: master path-1: parity error
3	RWX	REG_0X01_DATA_PARITY_ERROR: Error: port-0 primary configuration register (0x01): data parity error
4	RWX	REG_0X02_DATA_PARITY_ERROR: Error: port-1 primary configuration register (0x02): data parity error
5	RWX	REG_0X03_DATA_PARITY_ERROR: Error: port-0 secondary configuration register (0x03): data parity error
6	RWX	REG_0X04_DATA_PARITY_ERROR: Error: port-1 secondary configuration register (0x04): data parity error
7	RWX	REG_0X05_DATA_PARITY_ERROR: Error: slave path control register (0x05): data parity error
8	RWX	REG_0X06_DATA_PARITY_ERROR: Error: internal path control register (0x06): data parity error
9	RWX	REG_0X07_DATA_PARITY_ERROR: Error: primary/secondary master/slave control register (0x07): data parity error

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Bits	PIB	Field Mnemonic: Description
10	RWX	S_PATH_0_PARITY_ERROR: Error: slave path-0: parity error
11	RWX	REG_0X08_DATA_PARITY_ERROR: Error: primary/secondary master/slave status register (0x07): data parity error
12	RWX	REG_0X09_DATA_PARITY_ERROR: Error: master path status register (0x09): data parity error
13	RWX	REG_0X0A_DATA_PARITY_ERROR: Error: slave path status register (0x0a): data parity error
14	RWX	M_PATH_0_STEP_CHECK_ERROR: Error: master path-0: step check error
15	RWX	M_PATH_1_STEP_CHECK_ERROR: Error: master path-1: step check error
16	RWX	S_PATH_0_STEP_CHECK_ERROR: Error: slave path-0: step check error
17	RWX	I_PATH_STEP_CHECK_ERROR: Error: internal path: step check error
18	RWX	PSS_HAM: Error: PSS Hamming Distance
19	RWX	REG_0X0B_DATA_PARITY_ERROR: Error: miscellaneous, reset register (0x0b): data parity error
20	RWX	S_PATH_1_PARITY_ERROR: Error: slave path-0: parity error
21	RWX	S_PATH_1_STEP_CHECK_ERROR: Error: slave path-1: step check error
22	RWX	I_PATH_DELAY_STEP_CHECK_PARITY_ERROR: Error: internal path: delay, step check components: parity error
23	RWX	REG_0X0C_DATA_PARITY_ERROR: Error: probe data select register (0x0c): data parity error
24	RWX	REG_0X11_0X12_0X13_0X14_0X15_0X16_DATA_PARITY_ERROR: Error: data parity error on one of the following TX-TType trigger registers: - TX Ttype-0 triggering register (0x11) - TX Ttype-1 triggering register (0x12) - TX Ttype-2 triggering register (0x13) - TX Ttype-3 triggering register (0x14) - TX Ttype-4 triggering register (0x15) - TX Ttype-5 triggering register (0x16)
25	RWX	REG_0X17_0X18_0X21_0X22_DATA_PARITY_ERROR: Error: data parity error on one of the following trigger registers: - move-TOD-to-timebase triggering register (0x17) - load-TOD-mod register (0x18) - load register (0x21) - start-TOD register (0x22)
26	RWX	REG_0X1D_0X1E_0X1F_DATA_PARITY_ERROR: Error: data parity error on one of the following trace data registers: - Trace Data Set-1 Register (0x1d) - Trace Data Set-2 Register (0x1e) - Trace Data Set-3 Register (0x1f)
27	RWX	REG_0X20_DATA_PARITY_ERROR: Error: time value register (0x20): data parity error
28	RWX	REG_0X23_DATA_PARITY_ERROR: Error: low order step register (0x23): data parity error
29	RWX	REG_0X24_DATA_PARITY_ERROR: Error: FSM register (0x24): data parity error
30	RWX	REG_0X29_DATA_PARITY_ERROR: Error: RX-TType control register: data parity error
31	RWX	REG_0X30_0X31_0X32_0X33_DATA_PARITY_ERROR: Error: data parity error on one of the following error handling registers: - Error Register (0x30) - Error Inject Register (0x31) - Error Mask Register (0x32) - Core Interrupt Mask Register (0x33)
32	RWX	REG_0X10_DATA_PARITY_ERROR: Error: chip control register (0x10): data parity error
33	RWX	I_PATH_SYNC_CHECK_ERROR: Error: internal path: sync check



Bits	PIB	Field Mnemonic: Description
34	RWX	I_PATH_FSM_STATE_PARITY_ERROR: Error: internal path: FSM state parity error
35	RWX	I_PATH_TIME_REG_PARITY_ERROR: Error: internal path. Time register parity error
36	RWX	I_PATH_TIME_REG_OVERFLOW: Error: internal path: time register overflow in year 2042
37	RWX	WOF_LOW_ORDER_STEP_COUNTER_PARITY_ERROR: Error: WOF counter or Low-Order-Step counter: parity error
38	RWX	RX_TTYPE_0: Status: received Ttype-0
39	RWX	RX_TTYPE_1: Status: received Ttype-1
40	RWX	RX_TTYPE_2: Status: received Ttype-2
41	RWX	RX_TTYPE_3: Status: received Ttype-3
42	RWX	RX_TTYPE_4: Status: received Ttype-4
43	RWX	RX_TTYPE_5: Status: received Ttype-5 when FSM is in running state
44	RWX	PIB_SLAVE_ADDR_INVALID_ERROR: Error: PIB slave: invalid address
45	RWX	PIB_SLAVE_WRITE_INVALID_ERROR: Error: PIB slave: invalid write
46	RWX	PIB_SLAVE_READ_INVALID_ERROR: Error: PIB slave: invalid read
47	RWX	PIB_SLAVE_ADDR_PARITY_ERROR: Error: PIB slave: address parity error
48	RWX	PIB_SLAVE_DATA_PARITY_ERROR: Error: PIB slave: data parity error
49	RWX	REG_0X27_DATA_PARITY_ERROR: Error: TType control register(0x27): data parity error
50:52	RWX	PIB_MASTER_RSP_INFO_ERROR: Error: PIB master: response infoerror info = 000: no error info > 000: error
53	RWX	RX_TTYPE_INVALID_ERROR: Error: received invalid TType via register 0x21
54	RWX	RX_TTYPE_4_DATA_PARITY_ERROR: Error: data parity error on received TType-4 via register 0x21
55	RWX	PIB_MASTER_REQUEST_ERROR: Error: PIB master; request while busy error
56	RWX	PIB_RESET_DURING_PIB_ACCESS_ERROR: Error: PIB reset received during a PIB master or PIB slave operation.
57	RWX	EXTERNAL_XSTOP_ERROR: Error: TOD received an external checkstop
58	RWX	SPARE_ERROR_58: Error: Spare.
59	RWX	SPARE_ERROR_59: Error: Spare.
60	RWX	SPARE_ERROR_60: Error: Spare.
61	RWX	SPARE_ERROR_61: Error: Spare.
62	RWX	SPARE_ERROR_62: Error: Spare.
63	RWX	SPARE_ERROR_63: Error: Spare.

Register Name	TOD: Error And Interrupt Inject Register	
Mnemonic	EH.TPCHIP.PIB.TOD.TOD_ERROR_INJECT_REG	
Address	0000000000040031 (PIB)	
Attributes		
Description		
Bits	PIB	Field Mnemonic: Description
0	WO	REG_0X00_DATA_PARITY_ERROR_INJECT: Error inject: master path control register (0x00): data parity error

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Bits	PIB	Field Mnemonic: Description
1	WO	M_PATH_0_PARITY_ERROR_INJECT: Error inject: master path-0: parity error
2	WO	M_PATH_1_PARITY_ERROR_INJECT: Error inject: master path-1: parity error
3	WO	REG_0X01_DATA_PARITY_ERROR_INJECT: Error inject: port-0 primary configuration register (0x01): data parity error
4	WO	REG_0X02_DATA_PARITY_ERROR_INJECT: Error inject: port-1 primary configuration register (0x02): data parity error
5	WO	REG_0X03_DATA_PARITY_ERROR_INJECT: Error inject: port-0 secondary configuration register (0x03): data parity error
6	WO	REG_0X04_DATA_PARITY_ERROR_INJECT: Error inject: port-1 secondary configuration register (0x04): data parity error
7	WO	REG_0X05_DATA_PARITY_ERROR_INJECT: Error inject: slave path control register (0x05): data parity error
8	WO	REG_0X06_DATA_PARITY_ERROR_INJECT: Error inject: internal path control register (0x06): data parity error
9	WO	REG_0X07_DATA_PARITY_ERROR_INJECT: Error inject: primarysecondary masterslave control register (0x07): data parity error
10	WO	S_PATH_0_PARITY_ERROR_INJECT: Error inject: slave path-0: parity error
11	WO	REG_0X08_DATA_PARITY_ERROR_INJECT: Error inject: primarysecondary masterslave status register (0x07): data parity error
12	WO	REG_0X09_DATA_PARITY_ERROR_INJECT: Error inject: master path status register (0x09): data parity error
13	WO	REG_0X0A_DATA_PARITY_ERROR_INJECT: Error inject: slave path status register (0x0a): data parity error
14	WO	M_PATH_0_STEP_CHECK_ERROR_INJECT: Error inject: master path-0: step check error
15	WO	M_PATH_1_STEP_CHECK_ERROR_INJECT: Error inject: master path-1: step check error
16	WO	S_PATH_0_STEP_CHECK_ERROR_INJECT: Error inject: slave path-0: step check error
17	WO	I_PATH_STEP_CHECK_ERROR_INJECT: Error inject: internal path: step check error
18	WO	PSS_HAM_INJECT: Error inject: PSS Hamming Distance
19	WO	REG_0X0B_DATA_PARITY_ERROR_INJECT: Error inject: miscellaneous, reset register (0x0b): data parity error
20	WO	S_PATH_1_PARITY_ERROR_INJECT: Error inject: slave path-0: parity error
21	WO	S_PATH_1_STEP_CHECK_ERROR_INJECT: Error inject: slave path-1: step check error
22	WO	I_PATH_DELAY_STEP_CHECK_PARITY_ERROR_INJECT: Error inject: internal path: delay, step check components: parity error
23	WO	REG_0X0C_DATA_PARITY_ERROR_INJECT: Error inject: probe data select register (0x0c): data parity error
24	WO	REG_0X11_0X12_0X13_0X14_0X15_0X16_DATA_PARITY_ERROR_INJECT: Error inject: data parity error on the following TX-TType trigger registers: - TX Ttype-0 triggering register (0x11) - TX Ttype-1 triggering register (0x12) - TX Ttype-2 triggering register (0x13) - TX Ttype-3 triggering register (0x14) - TX Ttype-4 triggering register (0x15) - TX Ttype-5 triggering register (0x16)

Bits	PIB	Field Mnemonic: Description
25	WO	REG_0X17_0X18_0X21_0X22_DATA_PARITY_ERROR_INJECT: Error inject: data parity error on the following trigger registers: - Move-TOD-to-Timebase Triggering Register (0x17) - Load-TOD-mod Register (0x18) - Load Register (0x21) - Start-TOD Register (0x22)
26	WO	REG_0X1D_0X1E_0X1F_DATA_PARITY_ERROR_INJECT: Error inject: data parity error on the following trace data registers: - Trace Data Set-1 Register (0x1d) - Trace Data Set-2 Register (0x1e) - Trace Data Set-3 Register (0x1f)
27	WO	REG_0X20_DATA_PARITY_ERROR_INJECT: Error inject: time value register (0x20): data parity error
28	WO	REG_0X23_DATA_PARITY_ERROR_INJECT: Error inject: low order step register (0x23): data parity error
29	WO	REG_0X24_DATA_PARITY_ERROR_INJECT: Error inject: FSM register (0x24): data parity error
30	WO	REG_0X29_DATA_PARITY_ERROR_INJECT: Error inject: RX-TType control register: data parity error
31	WO	REG_0X30_0X31_0X32_0X33_DATA_PARITY_ERROR_INJECT: Error inject: data parity error on the following error handling registers: - Error Register (0x30) - Error Mask Register (0x32) - Core Interrupt Mask Register (0x33)
32	WO	REG_0X10_DATA_PARITY_ERROR_INJECT: Error inject: chip control register (0x10): data parity error
33	WO	I_PATH_SYNC_CHECK_ERROR_INJECT: Error inject: internal path: sync check
34	WO	I_PATH_FSM_STATE_PARITY_ERROR_INJECT: Error inject: internal path: FSM state parity error
35	WO	I_PATH_TIME_REG_PARITY_ERROR_INJECT: Error inject: time register: parity error
36	WO	I_PATH_TIME_REG_OVERFLOW_INJECT: Error inject: internal path: time register overflow in year 2042
37	WO	WOF_LOW_ORDER_STEP_COUNTER_PARITY_ERROR_INJECT: Error inject: WOF counter or Low-Order-Step counter: parity error
38	WO	RX_TTYPE_0_INJECT: Error inject: received Ttype-0
39	WO	RX_TTYPE_1_INJECT: Error inject: received Ttype-1
40	WO	RX_TTYPE_2_INJECT: Error inject: received Ttype-2
41	WO	RX_TTYPE_3_INJECT: Error inject: received Ttype-3
42	WO	RX_TTYPE_4_INJECT: Error inject: received Ttype-4
43	WO	RX_TTYPE_5_INJECT: Error inject: received Ttype-5 when FSM is in running state
44	WO	PIB_SLAVE_ADDR_INVALID_ERROR_INJECT: Error inject: PIB slave: invalid address
45	WO	PIB_SLAVE_WRITE_INVALID_ERROR_INJECT: Error inject: PIB slave: invalid write
46	WO	PIB_SLAVE_READ_INVALID_ERROR_INJECT: Error inject: PIB slave: invalid read
47	WO	PIB_SLAVE_ADDR_PARITY_ERROR_INJECT: Error inject: PIB slave: address parity error
48	WO	PIB_SLAVE_DATA_PARITY_ERROR_INJECT: Error inject: PIB slave: data parity error
49	WO	REG_0X27_DATA_PARITY_ERROR_INJECT: Error inject: TType control register(0x27): data parity error
50:52	WO	PIB_MASTER_RSP_INFO_ERROR_INJECT: Error inject: PIB master: response info error
53	WO	RX_TTYPE_INVALID_ERROR_INJECT: Error inject: received invalid TType via register 0x21
54	WO	RX_TTYPE_4_DATA_PARITY_ERROR_INJECT: Error inject: data parity error on received TType-4 via register 0x21
55	WO	PIB_MASTER_REQUEST_ERROR_INJECT: Error inject: PIB master; request while busy error

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Bits	PIB	Field Mnemonic: Description
56	WO	PIB_RESET_DURING_PIB_ACCESS_ERROR_INJECT: Error inject: PIB reset received during a PIB master or PIB slave operation
57	WO	EXTERNAL_XSTOP_ERROR_INJECT: Error inject: TOD received an external checkstop
58	WO	SPARE_ERROR_INJECT_58: Error inject: spare
59	WO	SPARE_ERROR_INJECT_59: Error inject: spare
60	WO	SPARE_ERROR_INJECT_60: Error inject: spare
61	WO	SPARE_ERROR_INJECT_61: Error inject: spare
62	WO	SPARE_ERROR_INJECT_62: Error inject: spare
63	WO	CORE_STEP_ERROR_INJECT: Error inject: to suppress one step to core timebase

Register Name	TOD: Error Mask Register Mask of the Error Reporting Component (c_err_rpt)
Mnemonic	EH.TPCHIP.PIB.TOD.TOD_ERROR_MASK_REG
Address	0000000000040032 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	RWX	REG_0X00_DATA_PARITY_ERROR_MASK: Error mask: master path control register (0x00): data parity error
1	RWX	M_PATH_0_PARITY_ERROR_MASK: Error mask: master path-0: parity error
2	RWX	M_PATH_1_PARITY_ERROR_MASK: Error mask: master path-1: parity error
3	RWX	REG_0X01_DATA_PARITY_ERROR_MASK: Error mask: port-0 primary configuration register (0x01): data parity error
4	RWX	REG_0X02_DATA_PARITY_ERROR_MASK: Error mask: port-1 primary configuration register (0x02): data parity error
5	RWX	REG_0X03_DATA_PARITY_ERROR_MASK: Error mask: port-0 secondary configuration register (0x03): data parity error
6	RWX	REG_0X04_DATA_PARITY_ERROR_MASK: Error mask: port-1 secondary configuration register (0x04): data parity error
7	RWX	REG_0X05_DATA_PARITY_ERROR_MASK: Error mask: slave path control register (0x05): data parity error
8	RWX	REG_0X06_DATA_PARITY_ERROR_MASK: Error mask: internal path control register (0x06): data parity error
9	RWX	REG_0X07_DATA_PARITY_ERROR_MASK: Error mask: primary/secondary master/slave control register (0x07): data parity error
10	RWX	S_PATH_0_PARITY_ERROR_MASK: Error mask: slave path-0: parity error
11	RWX	REG_0X08_DATA_PARITY_ERROR_MASK: Error mask: primarysecondary masterslave status register (0x07): data parity error
12	RWX	REG_0X09_DATA_PARITY_ERROR_MASK: Error mask: master path status register (0x09): data parity error
13	RWX	REG_0X0A_DATA_PARITY_ERROR_MASK: Error mask: slave path status register (0x0a): data parity error
14	RWX	M_PATH_0_STEP_CHECK_ERROR_MASK: Error mask: master path-0: step check error
15	RWX	M_PATH_1_STEP_CHECK_ERROR_MASK: Error mask: master path-1: step check error
16	RWX	S_PATH_0_STEP_CHECK_ERROR_MASK: Error mask: slave path-0: step check error

Bits	PIB	Field Mnemonic: Description
17	RWX	I_PATH_STEP_CHECK_ERROR_MASK: Error mask: internal path: step check error
18	RWX	PSS_HAM_MASK: Error mask: PSS Hamming Distance
19	RWX	REG_0X0B_DATA_PARITY_ERROR_MASK: Error mask: miscellaneous, reset register (0x0b): data parity error
20	RWX	S_PATH_1_PARITY_ERROR_MASK: Error mask: slave path-0: parity error
21	RWX	S_PATH_1_STEP_CHECK_ERROR_MASK: Error mask: slave path-1: step check error
22	RWX	I_PATH_DELAY_STEP_CHECK_PARITY_ERROR_MASK: Error mask: internal path: delay , step check components: parity error
23	RWX	REG_0X0C_DATA_PARITY_ERROR_MASK: Error mask: probe data select register (0x0c): data parity error
24	RWX	REG_0X11_0X12_0X13_0X14_0X15_0X16_DATA_PARITY_ERROR_MASK: Error mask: data parity error on one of the following TX-TType trigger registers: - TX Ttype-0 Triggering Register (0x11) - TX Ttype-1 Triggering Register (0x12) - TX Ttype-2 Triggering Register (0x13) - TX Ttype-3 Triggering Register (0x14) - TX Ttype-4 Triggering Register (0x15) - TX Ttype-5 Triggering Register (0x16)
25	RWX	REG_0X17_0X18_0X21_0X22_DATA_PARITY_ERROR_MASK: Error mask: data parity error on one of the following trigger registers: - Move-TOD-to-Timebase Triggering Register (0x17) - Load-TOD-mod Register (0x18) - Load Register (0x21) - Start-TOD Register (0x22)
26	RWX	REG_0X1D_0X1E_0X1F_DATA_PARITY_ERROR_MASK: Error mask: data parity error on one of the following trace data registers: - Trace Data Set-1 Register (0x1d) - Trace Data Set-2 Register (0x1e) - Trace Data Set-3 Register (0x1f)
27	RWX	REG_0X20_DATA_PARITY_ERROR_MASK: Error mask: time value register (0x20): data parity error
28	RWX	REG_0X23_DATA_PARITY_ERROR_MASK: Error mask: low order step register (0x23): data parity error
29	RWX	REG_0X24_DATA_PARITY_ERROR_MASK: Error mask: FSM register (0x24): data parity error
30	RWX	REG_0X29_DATA_PARITY_ERROR_MASK: Error mask: RX-TType control register: data parity error
31	RWX	REG_0X30_0X31_0X32_0X33_DATA_PARITY_ERROR_MASK: Error mask: data parity error on one of the following error handling registers: - Error Register (0x30) - Error Inject Register (0x31) - Error Mask Register (0x32) - Core Interrupt Mask Register (0x33)
32	RWX	REG_0X10_DATA_PARITY_ERROR_MASK: Error mask: chip control register (0x10): data parity error
33	RWX	I_PATH_SYNC_CHECK_ERROR_MASK: Error mask: internal path: sync check
34	RWX	I_PATH_FSM_STATE_PARITY_ERROR_MASK: Error mask: internal path: FSM state parity error
35	RWX	I_PATH_TIME_REG_PARITY_ERROR_MASK: Error mask: internal path: time register: parity error
36	RWX	I_PATH_TIME_REG_OVERFLOW_MASK: Error mask: internal path: time register overflow in year 2042
37	RWX	WOF_LOW_ORDER_STEP_COUNTER_PARITY_ERROR_MASK: Error mask: WOF counter or Low-Order-Step counter: parity error
38	RWX	RX_TTYPE_0_MASK: Error mask: received Ttype-0
39	RWX	RX_TTYPE_1_MASK: Error mask: received Ttype-1
40	RWX	RX_TTYPE_2_MASK: Error mask: received Ttype-2

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Bits	PIB	Field Mnemonic: Description
41	RWX	RX_TTYPE_3_MASK: Error mask: received Ttype-3
42	RWX	RX_TTYPE_4_MASK: Error mask: received Ttype-4
43	RWX	RX_TTYPE_5_MASK: Error mask: received Ttype-5 when FSM is in running state
44	RWX	PIB_SLAVE_ADDR_INVALID_ERROR_MASK: Error mask: PIB slave: invalid address
45	RWX	PIB_SLAVE_WRITE_INVALID_ERROR_MASK: Error mask: PIB slave: invalid write
46	RWX	PIB_SLAVE_READ_INVALID_ERROR_MASK: Error mask: PIB slave: invalid read
47	RWX	PIB_SLAVE_ADDR_PARITY_ERROR_MASK: Error mask: PIB slave: address parity error
48	RWX	PIB_SLAVE_DATA_PARITY_ERROR_MASK: Error mask: PIB slave: data parity error
49	RWX	REG_0X27_DATA_PARITY_ERROR_MASK: Error mask: TType control register(0x27): data parity error
50:52	RWX	PIB_MASTER_RSP_INFO_ERROR_MASK: Error mask: PIB master: response infoerror
53	RWX	RX_TTYPE_INVALID_ERROR_MASK: Error mask: received invalid TType via register 0x21
54	RWX	RX_TTYPE_4_DATA_PARITY_ERROR_MASK: Error mask: data parity error on received TType-4 via register 0x21
55	RWX	PIB_MASTER_REQUEST_ERROR_MASK: Error mask: PIB master; request while busy error
56	RWX	PIB_RESET_DURING_PIB_ACCESS_ERROR_MASK: Error mask: PIB reset received during a PIB master or PIB slave operation
57	RWX	EXTERNAL_XSTOP_ERROR_MASK: Error mask: TOD received an external checkstop
58	RWX	SPARE_ERROR_MASK_58: Error mask: spare
59	RWX	SPARE_ERROR_MASK_59: Error mask: spare
60	RWX	SPARE_ERROR_MASK_60: Error mask: spare
61	RWX	SPARE_ERROR_MASK_61: Error mask: spare
62	RWX	SPARE_ERROR_MASK_62: Error mask: spare
63	RWX	SPARE_ERROR_MASK_63: Error mask: spare

Register Name	TOD: To Route Specific Errors Either to the CORE or to the FIR
Mnemonic	EH.TPCHIP.PIB.TOD.TOD_ERROR_ROUTING_REG
Address	000000000040033 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	RW	REG_0X00_DATA_PARITY_ERROR_ROUTING: Error routing: master path control register (0x00): data parity error
1	RW	M_PATH_0_PARITY_ERROR_ROUTING: Error routing: master path-0: parity error
2	RW	M_PATH_1_PARITY_ERROR_ROUTING: Error routing: master path-1: parity error
3	RW	REG_0X01_DATA_PARITY_ERROR_ROUTING: Error routing: port-0 primary configuration register (0x01): data parity error
4	RW	REG_0X02_DATA_PARITY_ERROR_ROUTING: Error routing: port-1 primary configuration register (0x02): data parity error
5	RW	REG_0X03_DATA_PARITY_ERROR_ROUTING: Error routing: port-0 secondary configuration register (0x03): data parity error

Bits	PIB	Field Mnemonic: Description
6	RW	REG_0X04_DATA_PARITY_ERROR_ROUTING: Error routing: port-1 secondary configuration register (0x04): data parity error
7	RW	REG_0X05_DATA_PARITY_ERROR_ROUTING: Error routing: slave path control register (0x05): data parity error
8	RW	REG_0X06_DATA_PARITY_ERROR_ROUTING: Error routing: internal path control register (0x06): data parity error
9	RW	REG_0X07_DATA_PARITY_ERROR_ROUTING: Error routing: primarysecondary masterslave control register (0x07): data parity error
10	RW	S_PATH_0_PARITY_ERROR_ROUTING: Error routing: slave path-0: parity error
11	RW	REG_0X08_DATA_PARITY_ERROR_ROUTING: Error routing: primarysecondary masterslave status register (0x08): data parity error
12	RW	REG_0X09_DATA_PARITY_ERROR_ROUTING: Error routing: master path status register (0x09): data parity error
13	RW	REG_0X0A_DATA_PARITY_ERROR_ROUTING: Error routing: slave path status register (0x0a): data parity error
14	RW	M_PATH_0_STEP_CHECK_ERROR_ROUTING: Error routing: master path-0: step check error
15	RW	M_PATH_1_STEP_CHECK_ERROR_ROUTING: Error routing: master path-1: step check error
16	RW	S_PATH_0_STEP_CHECK_ERROR_ROUTING: Error routing: slave path-0: step check error
17	RW	I_PATH_STEP_CHECK_ERROR_ROUTING: Error routing: internal path: step check error
18	RW	PSS_HAM_CORE_INTERRUPT_MASK: Error routing: PSS Hamming Distance
19	RW	REG_0X0B_DATA_PARITY_ERROR_ROUTING: Error routing: miscellaneous, reset register (0x0b): data parity error
20	RW	S_PATH_1_PARITY_ERROR_ROUTING: Error routing: slave path-0: parity error
21	RW	S_PATH_1_STEP_CHECK_ERROR_ROUTING: Error routing: slave path-1: step check error
22	RW	I_PATH_DELAY_STEP_CHECK_PARITY_ERROR_ROUTING: Error routing: internal path: delay, step check components: parity error
23	RW	REG_0X0C_DATA_PARITY_ERROR_ROUTING: Error routing: probe data select register (0x0c): data parity error
24	RW	REG_0X11_0X12_0X13_0X14_0X15_0X16_DATA_PARITY_ERROR_ROUTING: Error routing: data parity error on one of the following TX-Ttype trigger registers: - TX Ttype-0 Triggering Register (0x11) - TX Ttype-1 Triggering Register (0x12) - TX Ttype-2 Triggering Register (0x13) - TX Ttype-3 Triggering Register (0x14) - TX Ttype-4 Triggering Register (0x15) - TX Ttype-5 Triggering Register (0x16)
25	RW	REG_0X17_0X18_0X21_0X22_DATA_PARITY_ERROR_ROUTING: Error routing: data parity error on one of the following trigger registers: - Move-TOD-to-Timebase Triggering Register (0x17) - Load-TOD-mod Register (0x18) - Load Register (0x21) - Start-TOD Register (0x22)
26	RW	REG_0X1D_0X1E_0X1F_DATA_PARITY_ERROR_ROUTING: Error routing: data parity error on one of the following trace data registers: - Trace Data Set-1 Register (0x1d) - Trace Data Set-2 Register (0x1e) - Trace Data Set-3 Register (0x1f)
27	RW	REG_0X20_DATA_PARITY_ERROR_ROUTING: Error routing: time value register (0x20): data parity error

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Bits	PIB	Field Mnemonic: Description
28	RW	REG_0X23_DATA_PARITY_ERROR_ROUTING: Error routing: low order step register (0x23): data parity error
29	RW	REG_0X24_DATA_PARITY_ERROR_ROUTING: Error routing: FSM register (0x24): data parity error
30	RW	REG_0X29_DATA_PARITY_ERROR_ROUTING: Error routing: RX-TType control register: data parity error
31	RW	REG_0X30_0X31_0X32_0X33_DATA_PARITY_ERROR_ROUTING: Error routing: data parity error on one of the following error handling registers: - Error Register (0x30) - Error Inject Register (0x31) - Error Mask Register (0x32) - Core Interrupt Mask Register (0x33)
32	RW	REG_0X10_DATA_PARITY_ERROR_ROUTING: Error routing: chip control register (0x10): data parity error
33	RW	I_PATH_SYNC_CHECK_ERROR_ROUTING: Error routing: internal path: sync check
34	RW	I_PATH_FSM_STATE_PARITY_ERROR_ROUTING: Error routing: internal path: FSM state parity error
35	RW	I_PATH_TIME_REG_PARITY_ERROR_ROUTING: Error routing: internal path: time register: parity error
36	RW	I_PATH_TIME_REG_OVERFLOW_CORE_INTERRUPT: Error routing: internal path: time register overflow in year 2042
37	RW	WOF_LOW_ORDER_STEP_COUNTER_PARITY_ERROR_ROUTING: Error routing: WOF counter or low-order-step counter: parity error
38	RW	RX_TTYPE_0_ERROR_ROUTING: Error routing: received Ttype-0
39	RW	RX_TTYPE_1_ERROR_ROUTING: Error routing: received Ttype-1
40	RW	RX_TTYPE_2_ERROR_ROUTING: Error routing: received Ttype-2
41	RW	RX_TTYPE_3_ERROR_ROUTING: Error routing: received Ttype-3
42	RW	RX_TTYPE_4_ERROR_ROUTING: Error routing: received Ttype-4
43	RW	RX_TTYPE_5_ERROR_ROUTING: Error routing: received Ttype-5 when FSM is in running state
44	RW	PIB_SLAVE_ADDR_INVALID_ERROR_ROUTING: Error routing: PIB slave: invalid address
45	RW	PIB_SLAVE_WRITE_INVALID_ERROR_ROUTING: Error routing: PIB slave: invalid write
46	RW	PIB_SLAVE_READ_INVALID_ERROR_ROUTING: Error routing: PIB slave: invalid read
47	RW	PIB_SLAVE_ADDR_PARITY_ERROR_ROUTING: Error routing: PIB slave: address parity error
48	RW	PIB_SLAVE_DATA_PARITY_ERROR_ROUTING: Error routing: PIB slave: data parity error
49	RW	REG_0X27_DATA_PARITY_ERROR_ROUTING: Error routing: TType control register(0x27): data parity error
50:52	RW	PIB_MASTER_RSP_INFO_ERROR_ROUTING: Error routing: PIB master: response infoerror
53	RW	RX_TTYPE_INVALID_ERROR_ROUTING: Error routing: received invalid TType via register 0x21
54	RW	RX_TTYPE_4_DATA_PARITY_ERROR_ROUTING: Error routing: data parity error on received TType-4 via register 0x21
55	RW	PIB_MASTER_REQUEST_ERROR_ROUTING: Error routing: PIB master; request while busy error
56	RW	PIB_RESET_DURING_PIB_ACCESS_ERROR_ROUTING: Error routing: PIB reset received during a PIB master or PIB slave operation
57	RW	EXTERNAL_XSTOP_ERROR_ROUTING: Error routing: TOD received an external checkstop
58	RW	SPARE_ERROR_ROUTING_58: Error routing: spare
59	RW	SPARE_ERROR_ROUTING_59: Error routing: spare
60	RW	SPARE_ERROR_ROUTING_60: Error routing: spare
61	RW	SPARE_ERROR_ROUTING_61: Error routing: spare



Bits	PIB	Field Mnemonic: Description
62	RW	SPARE_ERROR_ROUTING_62: Error routing: spare
63	RW	SPARE_ERROR_ROUTING_63: Error routing: spare

Register Name	<i>POR IBUF0: Control And Debug Register</i>
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.IO_CONTROL_REG
Address	0000000000060001 (PIB) 0000000040000008 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0	RWX	RWX	I0_CTL_NO_LB: IE Stop/Run bit: 0-> Automatic run-mode. 1-> STOP/debug mode. This gets cleared (run mode) on SCOM write or Write to EXE Trigger Register. This gets set (STOP/debug mode) on SCOM write or exec WAIT 0 or System Check Stop (when enabled) or Stop on error (when enabled) or PORE IE RESET from user (SCOM Operation).
1	NCX	NCX	I0_CTL_POR_CONT: IE Continue bit (writing '1' makes pulse) when stopped at breakpoint or SCAND-CRC-error; unaffected by Bit(3).
2	NCX	NCX	I0_CTL_POR_SKIP: IE Skip Instruction (writing '1' makes pulse), when stopped, PC<--PC+1, to skip a long instruction write into this bit 3 times, unaffected by Bit(3).
3	NCX	NCX	I0_CTL_SETPC: IE Set-PC (writing '1' makes pulse): Set PC to value in bits 16:63.
4:6	RWX	RWX	I0_CTL_SCAN_CLKDIV: IE Scanclk divider setting for SCAND instruction. 000 = nclk/32 (default) 001 = nclk/64 01x = nclk/128 111 = nclk/16 110 = nclk/8 101 = nclk/4 100 = nclk/2, not written when Bit(3) = '1'.
7	RWX	RWX	I0_CTL_EXE_LOCK: EXE register lock bit, NOT written when Bit(3)='1', Control register never gets locked.
8	RWX	RWX	I0_CTL_FREEZE_PORE_ACTION_MASK: Mask bit to freeze action based on system xstop, 0 = Not masked (default), pore_freeze_action possible 1 = Masked
9	RWX	RWX	I0_CTL_INSTR_PAR_EN: Instruction parity check enable. 0 = Parity check disabled. 1 = Parity check enabled.
10	RWX	RWX	I0_CTL_PIB_PAR_EN_B: PIB parity check disable. 0 = Parity check enabled. 1 = Parity check disabled.
11	RWX	RWX	I0_CTL_TRAP_EN: Trap enable. 0 = Disabled. 1 = Enabled.
12	RWX	RWX	I0_CTL_TRC_NARROW_EN: Trace Bus narrow mode, 0 = Drive all 88 trace bus pins. 1 = Drive only first 8 bits of trace bus (remaining 80 bits are forced to zero).

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Bits	PIB	OCI	Field Mnemonic: Description
13	RWX	RWX	I0_CTL_INT_ENABLE: Indicates if PORE can be interrupted (only valid for PORE instances that can be interrupted). 0 = PORE can not be interrupted. 1 = PORE can be interrupted.
14	RWX	RWX	I0_CTL_DONE_OVR: PORE done overwrite. 0 = No overwrite of PMC done indicator. 1 = Force PMC done indicator to 1.
15	RWX	RWX	I0_CTL_INTERRUPT_CHKSW: Interruptible PORE feature on/off. 0 = This PORE instance can not be interrupted. 1 = This PORE instance can be interrupted.
16:63	RWX	RWX	I0_CTL_ABR: IE When written with Bit(3)=0':sets Program Counter break point address, When written with Bit(3)=1':Value is written into PC(breakpoint address unchanged). On a read, the PC breakpoint address is always returned.

Register Name	POR IBUF0: Reset Register
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.I0_RESET_REG
Address	0000000000060002 (PIB) 0000000040000010 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0	RWX	RWX	I0_PORE_IE_RESET_TRIGGER: Trigger functional reset of PORE/SBE IE, clears all register include debug regs, but does not clear ERROR MASK register.
1	RWX	RWX	I0_PORE_OCI_RESET_TRIGGER: Trigger PORE to OCI reset.
2	RWX	RWX	I0_UNUSED_RESET_REG_BIT: Reserved.
3	RWX	RWX	I0_CHKSW_HW215170: Debug switch for HW215170. 0b0 : Fix enabled (default). 0b1: Fix disabled.
4	RWX	RWX	I0_CHKSW_HW217012: Debug switch for HW217012. 0b0 : Fix enabled (default). 0b1: Fix disabled.
5	RWX	RWX	I0_CHKSW_HW237648: Debug switch for HW237648. 0b0 : Fix enabled (default). 0b1: Fix disabled.

Register Name	POR IBUF0: Error Mask Register
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.I0_ERROR_MASK_REG
Address	0000000000060003 (PIB) 0000000040000018 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:4	RW	RW	I0_ERROR_INTERRUPT_ENABLE: bit 0: Error event 0 bit 1: Error event 1 bit 2: Error event 2 bit 3: Error event 3 bit 4: Spare bit set to 1 triggers corresponding error handler
5:9	RW	RW	I0_ERROR_FIR_ENABLE: bit 0: Error event 0 bit 1: Error event 1 bit 2: Error event 2 bit 3: Error event 3 bit 4: Error event 4 bit set to 1 triggers pulse on PORE_error_out line
10:14	RW	RW	I0_ERROR_FATAL_ENABLE: bit 0: Error event 0 bit 1: Error event 1 bit 2: Error event 2 bit 3: Error event 3 bit 4: Error event 4 bit set to 1 triggers pulse on PORE_fatal_error_out line
15:19	RW	RW	I0_STOP_PORE: bit 0: Error event 0 bit 1: Error event 1 bit 2: Error event 2 bit 3: Error event 3 bit 4: Error event 4 bit set to 1 stops PORE execution
20	RW	RW	I0_GATE_PIB_CHIPLET_OFFLINE: Chiplet offline return code (010) triggers error event 0 if reset; otherwise, does not trigger error event.
21:24	RW	RW	I0_I2C_ERROR_MASK: bit 0: Mask I2C errors type 1 (I2CM internal and parity) bit 1: Mask I2C error type 2 (Bad PIB resp I2CM -> ECCAX) bit 2: Mask I2C error type 3 (ECCAX internal) bit 3: Mask I2C error type 4 (I2C bus errors)



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Bits	PIB	OCI	Field Mnemonic: Description
25:29	RW	RW	I0_GROUP_PARITY_MASK: Masks for parity error detection of registers bit25 : Debug, status, error mask, pc stack registers bit 26: Control, exe trigger, exe t_mask, i2c param registers bit 27: perv/oci base addr, table base addr, memory reloc bit 28: scr0, scr1, scr2, and data scr0 registers bit 29: ibuf register

Register Name	POR IBUF0: Pervasive Base Address 0 Register
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.I0_PERV_BASE_ADDRESS_0_REG
Address	0000000000060004 (PIB) 0000000040000020 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:24	RO	RO	Constant = 0b000000000000000000000000
25	RWX	RWX	I0_MULTICAST_BIT_0: Multicast bit for Base Address0 used for pervasive accesses during execution phase of instructions.
26:31	RWX	RWX	I0_CHIPLET_ID_0: Base Address0 used for pervasive accesses during execution phase of instructions. Bits used as chiplet ID or Multicast Group part of the pervasive addresses leaving PRV PIBMS. This value can be incremented using the ADDI instruction from PORE instruction set.

Register Name	POR IBUF0: Pervasive Base Address 1 Register
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.I0_PERV_BASE_ADDRESS_1_REG
Address	0000000000060005 (PIB) 0000000040000028 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:24	RO	RO	Constant = 0b000000000000000000000000
25	RWX	RWX	I0_MULTICAST_BIT_1: Multicast Bit for Base Address1 used for pervasive accesses during execution phase of instructions.
26:31	RWX	RWX	I0_CHIPLET_ID_1: Base Address1 used for pervasive accesses during execution phase of instructions. Bits used as chiplet ID part of the pervasive addresses leaving PRV PIBMS. This value can be incremented using the ADDI instruction from the PORE instruction set.

Register Name	POR IBUF0: OCI Base Address 0 Register
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.I0_OCI_BASE_ADDRESS_0_REG
Address	0000000000060006 (PIB) 0000000040000030 (OCI)
Attributes	
Description	



Bits	PIB	OCI	Field Mnemonic: Description
0:17	RO	RO	Constant = 0b000000000000000000
18:31	RWX	RWX	I0_UNUSED_OCI_BASE_ADDRESS_0_BITS: reserved
32:63	RWX	RWX	I0_OCI_BASE_ADDR_0: Base Address0 used for OCI/FI2C accesses during execution phase of instructions. Added to address parameter of instruction. This value can be incremented using the ADDI instruction from the PORE instruction set.

Register Name	<i>POR IBUF0: OCI Base Address 1 Register</i>
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.I0_OCI_BASE_ADDRESS_1_REG
Address	000000000060007 (PIB) 0000000040000038 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:17	RO	RO	Constant = 0b000000000000000000
18:31	RWX	RWX	I0_UNUSED_OCI_BASE_ADDRESS_1_BITS: Reserved.
32:63	RWX	RWX	I0_OCI_BASE_ADDR_1: Base Address1 used for OCI/FI2C accesses during execution phase of instructions. Added to address parameter of instruction. This value can be incremented using the ADDI instruction from the PORE instruction set

Register Name	<i>POR IBUF0: Table Base Address Register</i>
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.I0_TABLE_BASE_ADDRESS_REG
Address	000000000060008 (PIB) 0000000040000040 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:15	RO	RO	Constant = 0b0000000000000000
16	RWX	RWX	I0_TABLE_BASE_ADDR_INTERFACE: Interface used to access the Base Table (used for Start Vectors and Error Handlers): 0 = PIB/PERV 1 = OCI/FI2C
17	RWX	RWX	I0_UNUSED_TABLE_BASE_ADDRESS_BIT: Reserved.
18:23	RWX	RWX	I0_TABLE_BASE_ADDR_CHIPLET_ID: In case of PIB/PERV or FI2C interface, this field defines the pervasive chiplet ID, unused for OCI
24:27	RWX	RWX	I0_TABLE_BASE_ADDR_PIB_ID: In case of PIB/PERV or FI2C interface, this field defines the PIB master ID, unused for OCI.
28:31	RWX	RWX	I0_TABLE_BASE_ADDR_PORT_ID: In case of PIB/PERV or FI2C interface, this field defines the pervasive port ID, unused for OCI.
32:63	RWX	RWX	I0_TABLE_BASE_ADDR: Table base address for jump table. This value can be incremented using the ADDI instruction from the PORE instruction set.

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Register Name	POR IBUF0: EXE Trigger Register
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.I0_EXE_TRIGGER_REG
Address	0000000000060009 (PIB) 0000000040000048 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:7	RO	RO	Constant = 0b00000000
8:11	RWX	RWX	I0_START_VECTOR: Writing to start_vector causes PORE to enter run mode at the corresponding address given by (start_vector X 3) + 0x0018. This register is locked when CONTROL_REG bit(0) is '0' (in run mode) or if CONTROL_REG bit(7) is '1' (CTL_EXE_LOCK). The start vector is cleared on PORE IE RESET.
12:31	RO	RO	Constant = 0b00000000000000000000
32:63	RWX	RWX	I0_START_PARAMETER: One bit for each chiplet, bits (32 - 47) -> chiplets 0 – 15, that determines whether this chiplet is part of the mc accesses. This register is locked when CONTROL_REG bit(0) is '0' (in run mode) or if CONTROL_REG bit(7) is '1' (CTL_EXE_LOCK). The start_parameter is cleared on PORE IE RESET.

Register Name	POR IBUF0: Scratch0 Register, Address
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.I0_SCRATCH0_REG
Address	000000000006000A (PIB) 0000000040000050 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:7	RO	RO	Constant = 0b00000000
8:31	RWX	RWX	I0_SCRATCH0: POR IE Scratch0 register, 24 bits. This register is locked when CONTROL_REG bit(0) is '0'.

Register Name	POR IBUF0: Scratch1 Register, Data
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.I0_SCRATCH1_REG
Address	000000000006000B (PIB) 0000000040000058 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:63	RWX	RWX	I0_SCRATCH1: POR IE Scratch1 register, 64-bit data buffer, This register is locked when CONTROL_REG bit(0) is '0'.



Register Name		<i>POR IBUF0: Scratch2 Register, Data</i>	
Mnemonic		EH.TPCHIP.OCC.OCI.POREGPE.I0_SCRATCH2_REG	
Address		000000000006000C (PIB) 0000000040000060 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:63	RWX	RWX	I0_SCRATCH2: POR IE Scratch2 register, 64-bit data buffer, This register is locked when CONTROL_REG bit(0) is '0'.

Register Name		<i>POR IBUF0: First 64 Bits of the Instruction Buffer</i>	
Mnemonic		EH.TPCHIP.OCC.OCI.POREGPE.I0_IBUF_LO_REG	
Address		000000000006000D (PIB) 0000000040000068 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:63	RWX	RWX	I0_IBUF_LO: POR IE Instruction Buffer, bits 0-63, This register is locked when CONTROL_REG bit(0) is '0'.

Register Name		<i>POR IBUF0: Last 32 Bits of the Instruction Buffer</i>	
Mnemonic		EH.TPCHIP.OCC.OCI.POREGPE.I0_IBUF_2_REG	
Address		000000000006000E (PIB) 0000000040000070 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:31	RWX	RWX	I0_IBUF_2: POR IE Instruction Buffer, bits 64-95. This register is locked when CONTROL_REG bit(0) is '0'.

Register Name		<i>POR IBUF0: Debug 0 Register</i>	
Mnemonic		EH.TPCHIP.OCC.OCI.POREGPE.I0_DBG0_REG	
Address		000000000006000F (PIB) 0000000040000078 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:31	RWX_WCLRR EG	RWX_WCLRREG	I0_LAST_PIBMS_ACCESS_ADDRESS: POR PIB Master: Address of last completed access. Register gets cleared on PORE IE Reset.
32	RWX_WCLRR EG	RWX_WCLRREG	I0_PIB_DATA_READ_P_ERR: Parity error in read data from PRV PIB.

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Bits	PIB	OCI	Field Mnemonic: Description
33:35	RWX_WCLRR EG	RWX_WCLRREG	I0_LAST_PIBMS_ACCESS_RETURN_CODE: POR PIB Master: Last Return Code from PIB/PCB (SCRESP): For example: 000: OK 010: Chiplet offline 100: Invalid address 110: Parity error / unexpected/wrong packet 111: Timeout
36	RWX_WCLRR EG	RWX_WCLRREG	I0_I2C_BAD_STATUS_0: I2CM internal errors including parity errors.
37	RWX_WCLRR EG	RWX_WCLRREG	I0_I2C_BAD_STATUS_1: Bad PIB response code error for ECCAX to I2CM communication.
38	RWX_WCLRR EG	RWX_WCLRREG	I0_I2C_BAD_STATUS_2: ECCAX internal errors (UCE or PIB master resets).
39	RWX_WCLRR EG	RWX_WCLRREG	I0_I2C_BAD_STATUS_3: I2C bus issues (I2C bus busy, NACK, stop bit error).
40	RWX_WCLRR EG	RWX_WCLRREG	I0_GROUP_PARITY_ERROR_0: Parity error from debug or status or error mask or pc stack regs.
41	RWX_WCLRR EG	RWX_WCLRREG	I0_GROUP_PARITY_ERROR_1: Parity error from control or exe trigger or exe t_mask or i2c param regs.
42	RWX_WCLRR EG	RWX_WCLRREG	I0_GROUP_PARITY_ERROR_2: Parity error from perv/oci base address or table base address or memory reloc
43	RWX_WCLRR EG	RWX_WCLRREG	I0_GROUP_PARITY_ERROR_3: Parity error from scr0, scr1, scr2, or data scr0 register
44	RWX_WCLRR EG	RWX_WCLRREG	I0_GROUP_PARITY_ERROR_4: Parity error from ibuf register
45:52	ROX	ROX	I0_INTERRUPT_COUNTER_Q: Counter, that tracks the number of instructions executed after the exe trigger write request is queued and interrupt enable is not set.

Register Name	POR IBUF0: Debug 1 Register
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.I0_DBG1_REG
Address	000000000060010 (PIB) 000000004000080 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:31	RWX_WCLRR EG	RWX_WCLRREG	I0_LAST_PC_ACCESS_ADDRESS_0_31: POR PC: Address of last completed PC access: Register gets cleared on PORE IE Reset.
32:47	RWX_WCLRR EG	RWX_WCLRREG	I0_LAST_PC_ACCESS_ADDRESS_32_47: POR PC: Address of last completed PC access: Register gets cleared on PORE IE Reset.
48	RWX_WCLRR EG	RWX_WCLRREG	I0_OCI_DATA_READ_P_ERR: Parity error in read data from OCI.
49:51	RWX_WCLRR EG	RWX_WCLRREG	I0_LAST_OCIMS_ACCESS_RETURN_CODE: POR OCI Master: Last Return Code from OCI (Error).
52	RWX_WCLRR EG	RWX_WCLRREG	I0_BAD_PAR: Bad instruction parity



Bits	PIB	OCI	Field Mnemonic: Description
53	RWX_WCLRR EG	RWX_WCLRREG	I0_BAD_INSTRUCTION: Invalid instruction.
54	RWX_WCLRR EG	RWX_WCLRREG	I0_BAD_PC: PC Overflow/underflow.
55	RWX_WCLRR EG	RWX_WCLRREG	I0_SCAN_DATA_CRC: Scan data CRC error.
56	RWX_WCLRR EG	RWX_WCLRREG	I0_PC_STACK_ERR: PC stack PUSH error or POP error.
57	RWX_WCLRR EG	RWX_WCLRREG	I0_INSTR_FETCH_ERROR: Nonzero return code or read data parity error was received when during fetch phase
58	RWX_WCLRR EG	RWX_WCLRREG	I0_BAD_OPERAND: Invalid instruction operand.
59	RWX_WCLRR EG	RWX_WCLRREG	I0_BAD_INSTRUCTION_PATH: Invalid instruction path (for example, FI2C parameter miss).
60	RWX_WCLRR EG	RWX_WCLRREG	I0_BAD_START_VECTOR_TRIGGER: Invalid start vector triggered.
61	RWX_WCLRR EG	RWX_WCLRREG	I0_FI2C_PROTOCOL_HANG: Fast I2C protocol hang detected - exceeded poll limit for FI2C engine.
62	RWX_WCLRR EG	RWX_WCLRREG	I0_ROTATE_INVALID: Rotate invalid.
63	RWX_WCLRR EG	RWX_WCLRREG	I0_PIBMS_DBG_LOCK: Lock debug0/1 registers on occurrence of error events 0-3. That is, when any one of PIBMS DBG0 Register(32:35) OR PIBMS DBG1 Register(48:55) is set.

Register Name	POR IBUF0: Stack Level 0 Register
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.I0_PC_STACK0_REG
Address	0000000000060011 (PIB) 0000000040000088 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:47	RWX	RWX	I0_STACK0_DATA: stack data level 0
48:58	RO	RO	Constant = 0b000000000000
59	RWX	RWX	I0_SET_STACK_POINTER: If set, the value in bits 60:63 is applied as new Stack Pointer
60:63	RWX	RWX	I0_NEW_STACK_POINTER: If bit 59 is set, the Stack Pointer is overwritten: 0001 = Stack empty 0010 = Stack filled up to level 0 0100 = Stack filled up to level 1 1000 = Stack filled up to level 2

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Register Name		<i>POR IBUF0: Stack Level 1 Register</i>	
Mnemonic		EH.TPCHIP.OCC.OCI.POREGPE.I0_PC_STACK1_REG	
Address		0000000000060012 (PIB) 0000000040000090 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:47	RWX	RWX	I0_STACK1_DATA: stack data level 1

Register Name		<i>POR IBUF0: Stack Level 2 Register</i>	
Mnemonic		EH.TPCHIP.OCC.OCI.POREGPE.I0_PC_STACK2_REG	
Address		0000000000060013 (PIB) 0000000040000098 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:47	RWX	RWX	I0_STACK2_DATA: Stack data level 2

Register Name		<i>POR IBUF0: ID Flags Register</i>	
Mnemonic		EH.TPCHIP.OCC.OCI.POREGPE.I0_ID_FLAGS_REG	
Address		0000000000060014 (PIB) 00000000400000A0 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:31	RO	RO	Constant = 0b00000000000000000000000000000000
32	ROX	ROX	I0_PIB_EXECUTION_PARITY_FAIL: PIB execution phase parity error indicator: Holds the PIB parity error indicator bit for the last execution phase access.
33:35	ROX	ROX	I0_PIB_EXECUTION_STATUS_FIELD: PIB execution phase status indicator: Holds the PIB response status of the last execution phase access.
36	ROX	ROX	I0_OCI_EXECUTION_PARITY_FAIL: OCI execution phase parity error indicator: Holds the OCI parity error indication bit for the last execution phase access.
37:39	ROX	ROX	I0_OCI_EXECUTION_STATUS_FIELD: OCI execution phase status indicator: Holds the OCI response status of the last execution phase access.
40:47	RO	RO	Constant = 0b00000000
48:55	RWX	RWX	I0_ALU_FLAGS: Alu flags: UGT,ULT,SGT,SLT,C,O,N,Z
56:63	RO	RO	Constant = 0b00000000



Register Name		POR IBUF0: Data0 Register	
Mnemonic		EH.TPCHIP.OCC.OCI.POREGPE.I0_DATA0_REG	
Address		0000000000060015 (PIB) 00000000400000A8 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:31	RWX	RWX	I0_DATA0: Scratch Data 0

Register Name		POR IBUF0: Memory Relocation Register	
Mnemonic		EH.TPCHIP.OCC.OCI.POREGPE.I0_MEMORY_RELOC_REG	
Address		0000000000060016 (PIB) 00000000400000B0 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:29	RO	RO	Constant = 0b00000000000000000000000000000000
30:31	RWX	RWX	I0_MEM_RELOC_REGION: Memory Relocation Region
32:51	RWX	RWX	I0_MEM_RELOC_BASE: Memory Relocation Base Address

Register Name		POR IBUF0: Fast I2C Parameter Set 0 Register	
Mnemonic		EH.TPCHIP.OCC.OCI.POREGPE.I0_I2C_E0_PARAM_REG	
Address		0000000000060017 (PIB) 00000000400000B8 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:3	RWX	RWX	I0_I2C_E0_ENGINE_ID: Fast I2C Parameter Set 0: Engine ID (equals to PIB ID of the addressed Fast I2C engine)
4	RWX	RWX	I0_UNUSED_BIT_4_I0_I2C_E0_PARAM_REG: Spare
5:7	RWX	RWX	I0_I2C_E0_ADDRESS_RANGE: Fast I2C Parameter Set 0: Memory Device Local Address Range: 001 = 8-bit local addressing 010 = 16-bit local addressing 011 = 24-bit local addressing 100 = 32-bit local addressing
8:9	RWX	RWX	I0_UNUSED_BIT_8_9_I0_I2C_E0_PARAM_REG: spare
10:15	RWX	RWX	I0_I2C_E0_ENGINE_PORT: Fast I2C Parameter Set 0: Engine Port.
16	RWX	RWX	I0_UNUSED_BIT_16_I0_I2C_E0_PARAM_REG: Spare
17:23	RWX	RWX	I0_I2C_E0_DEVICE_ID: Fast I2C Parameter Set 0: Target Device ID.
24:25	RWX	RWX	I0_UNUSED_BIT_24_25_I0_I2C_E0_PARAM_REG: Spare.
26:27	RWX	RWX	I0_I2C_E0_ENGINE_SPEED: Fast I2C Parameter Set 0: Engine Speed Setting.

Registers Specification

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Bits	PIB	OCI	Field Mnemonic: Description
28:31	RWX	RWX	I0_I2C_POLL_THRESHOLD: Fast I2C poll threshold for DONE polling. 0000 = disabled 0001 = 2 ³ polls 0010 = 2 ⁵ polls, ...1101 = 2 ²⁷ polls, 1110 and 1111 = 2 ²⁸ polls

Register Name	POR IBUF0: Fast I2C Parameter Set 1 Register
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.I0_I2C_E1_PARAM_REG
Address	0000000000060018 (PIB) 00000000400000C0 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:3	RWX	RWX	I0_I2C_E1_ENGINE_ID: Fast I2C Parameter Set 1: Engine ID (equals to PIB ID of the addressed Fast I2C engine)
4	RWX	RWX	I0_UNUSED_BIT_4_I0_I2C_E1_PARAM_REG: spare
5:7	RWX	RWX	I0_I2C_E1_ADDRESS_RANGE: Fast I2C Parameter Set 1: Memory Device Local Address Range. 001 = 8-bit local addressing 010 = 16-bit local addressing 011 = 24-bit local addressing 100 = 32-bit local addressing
8:9	RWX	RWX	I0_UNUSED_BIT_8_9_I0_I2C_E1_PARAM_REG: Spare
10:15	RWX	RWX	I0_I2C_E1_ENGINE_PORT: Fast I2C Parameter Set 1: Engine Port
16	RWX	RWX	I0_UNUSED_BIT_16_I0_I2C_E1_PARAM_REG: Spare
17:23	RWX	RWX	I0_I2C_E1_DEVICE_ID: Fast I2C Parameter Set 1: Target Device ID
24:25	RWX	RWX	I0_UNUSED_BIT_24_25_I0_I2C_E1_PARAM_REG: spare
26:27	RWX	RWX	I0_I2C_E1_ENGINE_SPEED: Fast I2C Parameter Set 1: Engine Speed Setting
28:31	RWX	RWX	I0_UNUSED_BIT_4_I28_31_I2C_E1_PARAM_REG: Spare

Register Name	POR IBUF0: Fast I2C Parameter Set 2 Register
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.I0_I2C_E2_PARAM_REG
Address	0000000000060019 (PIB) 00000000400000C8 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:3	RWX	RWX	I0_I2C_E2_ENGINE_ID: Fast I2C Parameter Set 2: Engine ID (equals to PIB ID of the addressed Fast I2C engine)
4	RWX	RWX	I0_UNUSED_BIT_4_I0_I2C_E2_PARAM_REG: spare



Bits	PIB	OCI	Field Mnemonic: Description
5:7	RWX	RWX	I0_I2C_E2_ADDRESS_RANGE: Fast I2C Parameter Set 2: Memory Device Local Address Range. 001 = 8-bit local addressing 010 = 16-bit local addressing 011 = 24-bit local addressing 100 = 32-bit local addressing
8:9	RWX	RWX	I0_UNUSED_BIT_8_9_I0_I2C_E2_PARAM_REG: Spare
10:15	RWX	RWX	I0_I2C_E2_ENGINE_PORT: Fast I2C Parameter Set 2: Engine Port
16	RWX	RWX	I0_UNUSED_BIT_16_I0_I2C_E2_PARAM_REG: Spare
17:23	RWX	RWX	I0_I2C_E2_DEVICE_ID: Fast I2C Parameter Set 2: Target Device ID
24:25	RWX	RWX	I0_UNUSED_BIT_24_25_I0_I2C_E2_PARAM_REG: Spare
26:27	RWX	RWX	I0_I2C_E2_ENGINE_SPEED: Fast I2C Parameter Set 2: Engine Speed Setting
28:31	RWX	RWX	I0_UNUSED_BIT_28_31_I0_I2C_E2_PARAM_REG: Spare

Register Name	POR IBUF1: Status Register
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.I1_STATUS_REG
Address	0000000000060020 (PIB) 0000000040000100 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:7	ROX	ROX	I1_SM_STAT: Instruction engine state machine state: 000 & state_vector(0:3) & bad_instruction_parity.
8	ROX	ROX	I1_FREEZE_PORE_ACTION_MASKED: Operation frozen due to SBE/PORE freeze action input (that is, system checkstop).
9	ROX	ROX	I1_EXE_TRIGGER_WR_REQ_Q: Interrupt pending. 0 = No interrupt pending. 1 = An interrupt is pending.
10:11	RO	RO	Constant = 0b00
12:15	ROX	ROX	I1_PC_STACK_CURRENT_STATE: Stack Pointer. 0001 = Empty. 0010 = Filled up to level 1. 0100 = Filled up to level 2. 0100 = Filled up to level 3 (error handler only).
16:63	ROX	ROX	I1_PC_Q: Program Counter has the fetch-address for POR instructions in 48-bit representation, counting in bytes, initial value is x8000000000000000

Register Name	POR IBUF1: Control And Debug Register
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.I1_CONTROL_REG
Address	0000000000060021 (PIB) 0000000040000108 (OCI)
Attributes	
Description	

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Bits	PIB	OCI	Field Mnemonic: Description
0	RWX	RWX	I1_CTL_NO_LB: IE Stop/Run bit: 0-> Automatic run-mode. 1-> STOP/debug mode. This gets cleared (run mode) on SCOM write or Write to EXE Trigger register. This gets set (STOP/debug mode) on SCOM write or exec WAIT 0 or System Check Stop (when enabled) or Stop on error (when enabled) or PORE IE RESET from user (SCOM operation).
1	NCX	NCX	I1_CTL_POR_CONT: IE Continue bit (writing '1' makes pulse) when stopped at breakpoint or SCAND-CRC-error, unaffected by Bit(3).
2	NCX	NCX	I1_CTL_POR_SKIP: IE Skip instruction (writing '1' makes pulse), when stopped, PC<--PC+1, to skip a long instruction write into this bit 3 times, unaffected by Bit(3).
3	NCX	NCX	I1_CTL_SETPC: IE Set-PC (writing '1' makes pulse): Set PC to value in bits 16:63.



Bits	PIB	OCI	Field Mnemonic: Description
4:6	RWX	RWX	I1_CTL_SCAN_CLKDIV: IE Scanclock divider setting for SCAND instruction. 000 = nclk/32 (default) 001 = nclk/64 01x = nclk/128 111 = nclk/16 110 = nclk/8 101 = nclk/4 100 = nclk/2, not written when Bit(3)='1'
7	RWX	RWX	I1_CTL_EXE_LOCK: EXE register lock bit, NOT written when Bit(3)='1', Control register never gets locked
8	RWX	RWX	I1_CTL_FREEZE_PORE_ACTION_MASK: Mask bit to freeze action based on system xstop. '0' : Not masked (default), pore_freeze_action possible '1' : Masked
9	RWX	RWX	I1_CTL_INSTR_PAR_EN: Instruction parity check enable. 0 = Parity check disabled 1 = Parity check enabled
10	RWX	RWX	I1_CTL_PIB_PAR_EN_B: PIB parity check disable. 0 = Parity check enabled 1 = Parity check disabled
11	RWX	RWX	I1_CTL_TRAP_EN: Trap enable. 0 = Disabled 1 = Enabled
12	RWX	RWX	I1_CTL_TRC_NARROW_EN: Trace bus narrow mode. 0 = Drive all 88 trace bus pins 1 = Drive only first 8 bits of trace bus (remaining 80 bits are forced to zero)
13	RWX	RWX	I1_CTL_INT_ENABLE: PORE interruptible indication (only valid for PORE instances that can be interrupted) 0 = PORE can not be interrupted. 1 = PORE can be interrupted.
14	RWX	RWX	I1_CTL_DONE_OVR: PORE done overwrite. 0 = No overwrite of PMC done indicator. 1 = Force PMC done indicator to 1.
15	RWX	RWX	I1_CTL_INTERRUPT_CHKSW: Interruptible PORE feature on/off. 0 = This PORE instance can not be interrupted. 1 = This PORE instance can be interrupted.
16:63	RWX	RWX	I1_CTL_ABR: IE when written with Bit(3)='0': sets Program Counter break point address. When written with Bit(3)='1', value is written into PC (breakpoint address unchanged). On a read, the PC breakpoint address is always returned.

Register Name		POR IBUF1: Reset Register	
Mnemonic		EH.TPCHIP.OCC.OCI.POREGPE.I1_RESET_REG	
Address		0000000000060022 (PIB) 0000000040000110 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0	RWX	RWX	I1_PORE_IE_RESET_TRIGGER: Trigger functional reset of PORE/SBE IE, clears all register include debug registers, but does not clear ERROR MASK register.

Registers Specification

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Bits	PIB	OCI	Field Mnemonic: Description
1	RWX	RWX	I1_PORE_OCI_RESET_TRIGGER: Trigger PORE to OCI reset.
2	RWX	RWX	I1_SBE_RESTART_TRIGGER: Trigger functional and OCI reset and then restarts the SBE.
3	RWX	RWX	I1_CHKSW_HW215170: Debug switch for HW215170. 0b0 : Fix enabled (debug) (default) 0b1: Fix disabled
4	RWX	RWX	I1_CHKSW_HW217012: Debug switch for HW217012. 0b0 : Fix enabled (default) 0b1: Fix disabled
5	RWX	RWX	I1_CHKSW_HW237648: Debug switch for HW237648. 0b0 : Fix enabled (default) 0b1: Fix disabled

Register Name	POR IBUF1: Error Mask Register
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.I1_ERROR_MASK_REG
Address	0000000000060023 (PIB) 0000000040000118 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:4	RW	RW	I1_ERROR_INTERRUPT_ENABLE: bit 0: Error event 0 bit 1: Error event 1 bit 2: Error event 2 bit 3: Error event 3 bit 4: Spare bit set to 1 triggers corresponding error handler
5:9	RW	RW	I1_ERROR_FIR_ENABLE: bit 0: Error event 0 bit 1: Error event 1 bit 2: Error event 2 bit 3: Error event 3 bit 4: Error event 4 bit set to 1 triggers pulse on PORE_error_out line
10:14	RW	RW	I1_ERROR_FATAL_ENABLE: bit 0: Error event 0 bit 1: Error event 1 bit 2: Error event 2 bit 3: Error event 3 bit 4: Error event 4 bit set to 1 triggers pulse on PORE_fatal_error_out line
15:19	RW	RW	I1_STOP_PORE: bit 0: Error event 0 bit 1: Error event 1 bit 2: Error event 2 bit 3: Error event 3 bit 4: Error event 4 bit set to 1 stops PORE execution
20	RW	RW	I1_GATE_PIB_CHIPLT_OFFLINE: Chiplet offline return code (010) triggers error event 0 if reset; otherwise, it does not trigger an error event.



Bits	PIB	OCI	Field Mnemonic: Description
21:24	RW	RW	I1_I2C_ERROR_MASK: bit 0: Mask i2c errors type 1 (I2CM internal and parity) bit 1: Mask i2c error type 2 (Bad PIB resp I2CM -> ECCAX) bit 2: Mask i2c error type 3 (ECCAX internal) bit 3: Mask i2c error type 4 (I2C bus errors)
25:29	RW	RW	I1_GROUP_PARITY_MASK: Masks for parity error detection of registers bit25 : Debug, status, error mask, pc stack regs bit 26: Control, exe trigger, exe t_mask, i2c param regs bit 27: Perv/oci base addr, table base addr, memory reloc bit 28: scr0, scr1, scr2, and data scr0 reg bit 29: ibuf reg

Register Name	POR IBUF1: Pervasive Base Address 0 Register
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.I1_PERV_BASE_ADDRESS_0_REG
Address	0000000000060024 (PIB) 0000000040000120 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:24	RO	RO	Constant = 0b000000000000000000000000
25	RWX	RWX	I1_MULTICAST_BIT_0: Multicast Bit for Base Address0 used for pervasive accesses during execution phase of instructions.
26:31	RWX	RWX	I1_CHIPLT_ID_0: Base Address0 used for pervasive accesses during execution phase of instructions. Bits used as chiplet ID or Multicast Group part of the pervasive addresses leaving PRV PIBMS. This value can be incremented using the ADDI instruction from PORE instruction set.

Register Name	POR IBUF1: Pervasive Base Address 1 Register
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.I1_PERV_BASE_ADDRESS_1_REG
Address	0000000000060025 (PIB) 0000000040000128 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:24	RO	RO	Constant = 0b000000000000000000000000
25	RWX	RWX	I1_MULTICAST_BIT_1: Multicast Bit for Base Address1 used for pervasive accesses during execution phase of instructions.
26:31	RWX	RWX	I1_CHIPLT_ID_1: Base Address1 used for Pervasive accesses during execution phase of instructions. Bits used as chiplet ID part of the pervasive addresses leaving PRV PIBMS. This value can be incremented using the ADDI instruction from PORE instruction set.

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Register Name		POR IBUF1: OCI Base Address 0 Register	
Mnemonic		EH.TPCHIP.OCC.OCI.POREGPE.I1_OCI_BASE_ADDRESS_0_REG	
Address		0000000000060026 (PIB) 0000000040000130 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:17	RO	RO	Constant = 0b000000000000000000
18:31	RWX	RWX	I1_UNUSED_OCI_BASE_ADDRESS_0_BITS: unused, reads 0
32:63	RWX	RWX	I1_OCI_BASE_ADDR_0: Base Address0 used for OCI/FI2C accesses during execution phase of instructions. Added to address parameter of instruction. This value can be incremented using the ADDI instruction from PORE instruction set

Register Name		POR IBUF1: OCI Base Address 1 Register	
Mnemonic		EH.TPCHIP.OCC.OCI.POREGPE.I1_OCI_BASE_ADDRESS_1_REG	
Address		0000000000060027 (PIB) 0000000040000138 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:17	RO	RO	Constant = 0b000000000000000000
18:31	RWX	RWX	I1_UNUSED_OCI_BASE_ADDRESS_1_BITS: unused, reads 0
32:63	RWX	RWX	I1_OCI_BASE_ADDR_1: Base Address1 used for OCI/FI2C accesses during execution phase of instructions. Added to address parameter of instruction. This value can be incremented using the ADDI instruction from PORE instruction set

Register Name		POR IBUF1: Table Base Address Register	
Mnemonic		EH.TPCHIP.OCC.OCI.POREGPE.I1_TABLE_BASE_ADDRESS_REG	
Address		0000000000060028 (PIB) 0000000040000140 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:15	RO	RO	Constant = 0b0000000000000000
16	RWX	RWX	I1_TABLE_BASE_ADDR_INTERFACE: Interface used to access the Base Table (used for Start Vectors and Error Handlers): 0 = PIB/PERV 1 = OCI/FI2C
17	RWX	RWX	I1_UNUSED_TABLE_BASE_ADDRESS_BIT: unused, reads 0
18:23	RWX	RWX	I1_TABLE_BASE_ADDR_CHIPLET_ID: In case of PIB/PERV or FI2C interface, this field defines the pervasive chiplet ID, unused for OCI
24:27	RWX	RWX	I1_TABLE_BASE_ADDR_PIB_ID: In case of PIB/PERV or FI2C interface, this field defines the PIB master ID, unused for OCI



Bits	PIB	OCI	Field Mnemonic: Description
28:31	RWX	RWX	I1_TABLE_BASE_ADDR_PORT_ID: In case of PIB/PERV or FI2C interface, this field defines the pervasive port ID, unused for OCI
32:63	RWX	RWX	I1_TABLE_BASE_ADDR: Table base address for jump table. This value can be incremented using the ADDI instruction from PORE instruction set

Register Name	<i>POR IBUF1: EXE Trigger Register</i>
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.I1_EXE_TRIGGER_REG
Address	0000000000060029 (PIB) 0000000040000148 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:7	RO	RO	Constant = 0b00000000
8:11	RWX	RWX	I1_START_VECTOR: Writing to start_vector causes PORE to enter run mode at the corresponding address given by (start_vector X 3) + 0x0018. This register is locked when CONTROL_REG bit(0) is '0' (in run mode) or if CONTROL_REG bit(7) is '1' (CTL_EXE_LOCK). The start vector is cleared on PORE IE RESET
12:31	RO	RO	Constant = 0b00000000000000000000
32:63	RWX	RWX	I1_START_PARAMETER: One bit for each chiplet, bit(32 - 47) -> chiplets 0 - 15, which determines whether this chiplet is part of the mc accesses. This register is locked when CONTROL_REG bit(0) is '0' (in run mode) or if CONTROL_REG bit(7) is '1' (CTL_EXE_LOCK). The start_parameter is cleared on PORE IE RESET.

Register Name	<i>POR IBUF1: Scratch0 Register, Address</i>
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.I1_SCRATCH0_REG
Address	000000000006002A (PIB) 0000000040000150 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:7	RO	RO	Constant = 0b00000000
8:31	RWX	RWX	I1_SCRATCH0: POR IE Scratch0 register, 24 bits, This register is locked when CONTROL_REG bit(0) is '0'.

Register Name	<i>POR IBUF1: Scratch1 Register, Data</i>
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.I1_SCRATCH1_REG
Address	000000000006002B (PIB) 0000000040000158 (OCI)
Attributes	
Description	

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Bits	PIB	OCI	Field Mnemonic: Description
0:63	RWX	RWX	I1_SCRATCH1: POR IE Scratch1 register, 64-bit data buffer, This register is locked when CONTROL_REG bit(0) is '0'.

Register Name	POR IBUF1: Scratch2 Register, Data		
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.I1_SCRATCH2_REG		
Address	000000000006002C (PIB) 0000000040000160 (OCI)		
Attributes			
Description			

Bits	PIB	OCI	Field Mnemonic: Description
0:63	RWX	RWX	I1_SCRATCH2: POR IE Scratch2 register, 64-bit data buffer, This register is locked when CONTROL_REG bit(0) is '0'.

Register Name	POR IBUF1: First 64 Bits of the Instruction Buffer		
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.I1_IBUF_LO_REG		
Address	000000000006002D (PIB) 0000000040000168 (OCI)		
Attributes			
Description			

Bits	PIB	OCI	Field Mnemonic: Description
0:63	RWX	RWX	I1_IBUF_LO: POR IE Instruction Buffer, bits 0 - 63. This register is locked when CONTROL_REG bit(0) is '0'.

Register Name	POR IBUF1: Last 32 Bits of the Instruction Buffer		
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.I1_IBUF_2_REG		
Address	000000000006002E (PIB) 0000000040000170 (OCI)		
Attributes			
Description			

Bits	PIB	OCI	Field Mnemonic: Description
0:31	RWX	RWX	I1_IBUF_2: POR IE Instruction Buffer, bits 64-95. This register is locked when CONTROL_REG bit(0) is '0'.

Register Name	POR IBUF1: Debug 0 Register		
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.I1_DBG0_REG		
Address	000000000006002F (PIB) 0000000040000178 (OCI)		
Attributes			
Description			



Bits	PIB	OCI	Field Mnemonic: Description
0:31	RWX_WCLRR EG	RWX_WCLRREG	I1_LAST_PIBMS_ACCESS_ADDRESS: POR PIB Master: Address of last completed access. Register is cleared on PORE IE Reset.
32	RWX_WCLRR EG	RWX_WCLRREG	I1_PIB_DATA_READ_P_ERR: Parity error in read data from PRV PIB.
33:35	RWX_WCLRR EG	RWX_WCLRREG	I1_LAST_PIBMS_ACCESS_RETURN_CODE: POR PIB Master: Last Return Code from PIB/PCB (SCRESP): For example: 000: OK 010: Chiplet offline 100: Invalid address 110: Parity error / unexpected/wrong packet 111: Timeout
36	RWX_WCLRR EG	RWX_WCLRREG	I1_I2C_BAD_STATUS_0: I2CM internal errors including parity errors.
37	RWX_WCLRR EG	RWX_WCLRREG	I1_I2C_BAD_STATUS_1: Bad PIB response code error for ECCAX to I2CM communication.
38	RWX_WCLRR EG	RWX_WCLRREG	I1_I2C_BAD_STATUS_2: ECCAX internal errors (UCE or PIB master resets).
39	RWX_WCLRR EG	RWX_WCLRREG	I1_I2C_BAD_STATUS_3: I2C bus issues (I2C bus busy, NACK, stop bit error).
40	RWX_WCLRR EG	RWX_WCLRREG	I1_GROUP_PARITY_ERROR_0: Parity error from debug or status or error mask or pc stack registers.
41	RWX_WCLRR EG	RWX_WCLRREG	I1_GROUP_PARITY_ERROR_1: Parity error from control or exe trigger or exe t_mask or i2c param registers.
42	RWX_WCLRR EG	RWX_WCLRREG	I1_GROUP_PARITY_ERROR_2: Parity error from perv/oci base addr or table base addr or memory reloc
43	RWX_WCLRR EG	RWX_WCLRREG	I1_GROUP_PARITY_ERROR_3: Parity error from scr0, scr1, scr2, or data scr0 register.
44	RWX_WCLRR EG	RWX_WCLRREG	I1_GROUP_PARITY_ERROR_4: Parity error from ibuf register.
45:52	ROX	ROX	I1_INTERRUPT_COUNTER_Q: Counter, that tracks the number of instructions executed after the exe trigger write request is queued and interrupt enable is not set.

Register Name	POR IBUF1: Debug 1 Register
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.I1_DBG1_REG
Address	0000000000060030 (PIB) 0000000040000180 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:31	RWX_WCLRR EG	RWX_WCLRREG	I1_LAST_PC_ACCESS_ADDRESS_0_31: POR PC: Address of last completed PC access : Register gets cleared upon PORE IE Reset.
32:47	RWX_WCLRR EG	RWX_WCLRREG	I1_LAST_PC_ACCESS_ADDRESS_32_47: POR PC: Address of last completed PC access : Register gets cleared upon PORE IE Reset.
48	RWX_WCLRR EG	RWX_WCLRREG	I1_OCI_DATA_READ_P_ERR: Parity error in read data from OCI.

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Bits	PIB	OCI	Field Mnemonic: Description
49:51	RWX_WCLRR EG	RWX_WCLRREG	I1_LAST_OCIMS_ACCESS_RETURN_CODE: POR OCI Master: Last Return Code from OCI (Error).
52	RWX_WCLRR EG	RWX_WCLRREG	I1_BAD_PAR: Bad instruction parity.
53	RWX_WCLRR EG	RWX_WCLRREG	I1_BAD_INSTRUCTION: Invalid instruction.
54	RWX_WCLRR EG	RWX_WCLRREG	I1_BAD_PC: PC overflow/underflow.
55	RWX_WCLRR EG	RWX_WCLRREG	I1_SCAN_DATA_CRC: Scan data CRC error.
56	RWX_WCLRR EG	RWX_WCLRREG	I1_PC_STACK_ERR: PC stack PUSH error or POP error.
57	RWX_WCLRR EG	RWX_WCLRREG	I1_INSTR_FETCH_ERROR: Non-zero return code or read data parity error was received when during fetch phase.
58	RWX_WCLRR EG	RWX_WCLRREG	I1_BAD_OPERAND: Invalid instruction operand.
59	RWX_WCLRR EG	RWX_WCLRREG	I1_BAD_INSTRUCTION_PATH: Invalid instruction path (for example, FI2C parameter miss).
60	RWX_WCLRR EG	RWX_WCLRREG	I1_BAD_START_VECTOR_TRIGGER: Invalid start vector triggered.
61	RWX_WCLRR EG	RWX_WCLRREG	I1_FI2C_PROTOCOL_HANG: Fast I2C protocol hang detected - exceeded poll limit for FI2C engine.
62	RWX_WCLRR EG	RWX_WCLRREG	I1_ROTATE_INVALID: Rotate invalid.
63	RWX_WCLRR EG	RWX_WCLRREG	I1_PIBMS_DBG_LOCK: Lock debug0/1 registers on occurrence of error events 0-3, that is, when any one of PIBMS DBG0 Register(32:35) or PIBMS DBG1 Register(48:55) is set.

Register Name	POR IBUF1: Stack Level 0 Register
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.I1_PC_STACK0_REG
Address	0000000000060031 (PIB) 0000000040000188 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:47	RWX	RWX	I1_STACK0_DATA: Stack data level 0
48:58	RO	RO	Constant = 0b000000000000
59	RWX	RWX	I1_SET_STACK_POINTER: If set, the value in bits 60:63 is applied as new Stack Pointer
60:63	RWX	RWX	I1_NEW_STACK_POINTER: If bit 59 is set, the Stack Pointer is overwritten. 0001 = Stack empty 0010 = Stack filled up to level 0, 0100 = Stack filled up to level 1 1000 = Stack filled up to level 2



Register Name		<i>POR IBUF1: Stack Level 1 Register</i>	
Mnemonic		EH.TPCHIP.OCC.OCI.POREGPE.I1_PC_STACK1_REG	
Address		0000000000060032 (PIB) 0000000040000190 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:47	RWX	RWX	I1_STACK1_DATA: Stack data level 1

Register Name		<i>POR IBUF1: Stack Level 2 Register</i>	
Mnemonic		EH.TPCHIP.OCC.OCI.POREGPE.I1_PC_STACK2_REG	
Address		0000000000060033 (PIB) 0000000040000198 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:47	RWX	RWX	I1_STACK2_DATA: Stack data level 2

Register Name		<i>POR IBUF1: ID Flags Register</i>	
Mnemonic		EH.TPCHIP.OCC.OCI.POREGPE.I1_ID_FLAGS_REG	
Address		0000000000060034 (PIB) 00000000400001A0 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:31	RO	RO	Constant = 0b00000000000000000000000000000000
32	ROX	ROX	I1_PIB_EXECUTION_PARITY_FAIL: PIB execution phase parity error indicator: Holds the PIB parity error indicator bit for the last execution phase access.
33:35	ROX	ROX	I1_PIB_EXECUTION_STATUS_FIELD: PIB execution phase status indicator: Holds the PIB response status of the last execution phase access.
36	ROX	ROX	I1_OCI_EXECUTION_PARITY_FAIL: OCI execution phase parity error indicator: Holds the OCI parity error indication bit for the last execution phase access.
37:39	ROX	ROX	I1_OCI_EXECUTION_STATUS_FIELD: OCI execution phase status indicator: Holds the OCI response status of the last execution phase access.
40:47	RO	RO	Constant = 0b00000000
48:55	RWX	RWX	I1_ALU_FLAGS: Alu flags: UGT,ULT,SGT,SLT,C,O,N,Z
56:63	RO	RO	Constant = 0b00000001



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Register Name		POR IBUF1: Data0 Register	
Mnemonic		EH.TPCHIP.OCC.OCI.POREGPE.I1_DATA0_REG	
Address		0000000000060035 (PIB) 00000000400001A8 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:31	RWX	RWX	I1_DATA0: Scratch Data 0

Register Name		POR IBUF1: Memory Relocation Register	
Mnemonic		EH.TPCHIP.OCC.OCI.POREGPE.I1_MEMORY_RELOC_REG	
Address		0000000000060036 (PIB) 00000000400001B0 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:29	RO	RO	Constant = 0b00000000000000000000000000000000
30:31	RWX	RWX	I1_MEM_RELOC_REGION: Memory Relocation Region
32:51	RWX	RWX	I1_MEM_RELOC_BASE: Memory Relocation Base Address

Register Name		POR IBUF1: Fast I2C Parameter Set 0 Register	
Mnemonic		EH.TPCHIP.OCC.OCI.POREGPE.I1_I2C_E0_PARAM_REG	
Address		0000000000060037 (PIB) 00000000400001B8 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:3	RWX	RWX	I1_I2C_E0_ENGINE_ID: Fast I2C Parameter Set 0: Engine ID (equals to PIB ID of the addressed Fast I2C engine)
4	RWX	RWX	I1_UNUSED_BIT_4_I0_I2C_E0_PARAM_REG: spare
5:7	RWX	RWX	I1_I2C_E0_ADDRESS_RANGE: Fast I2C Parameter Set 0: Memory Device Local Address Range 001 = 8-bit local addressing 010 = 16-bit local addressing 011 = 24-bit local addressing 100 = 32-bit local addressing
8:9	RWX	RWX	I1_UNUSED_BIT_8_9_I0_I2C_E0_PARAM_REG: spare
10:15	RWX	RWX	I1_I2C_E0_ENGINE_PORT: Fast I2C Parameter Set 0: Engine Port
16	RWX	RWX	I1_UNUSED_BIT_16_I0_I2C_E0_PARAM_REG: Spare
17:23	RWX	RWX	I1_I2C_E0_DEVICE_ID: Fast I2C Parameter Set 0: Target Device ID
24:25	RWX	RWX	I1_UNUSED_BIT_24_25_I0_I2C_E0_PARAM_REG: spare
26:27	RWX	RWX	I1_I2C_E0_ENGINE_SPEED: Fast I2C Parameter Set 0: Engine Speed Setting



Bits	PIB	OCI	Field Mnemonic: Description
28:31	RWX	RWX	I1_I2C_POLL_THRESHOLD: Fast I2C poll threshold for DONE polling 0000 = disabled 0001 = 2 ³ polls 0010 = 2 ⁵ polls, ..., 1101 = 2 ²⁷ polls 1110 and 1111 = 2 ²⁸ polls

Register Name	POR IBUF1: Fast I2C Parameter Set 1 Register
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.I1_I2C_E1_PARAM_REG
Address	0000000000060038 (PIB) 00000000400001C0 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:3	RWX	RWX	I1_I2C_E1_ENGINE_ID: Fast I2C Parameter Set 1: Engine ID (equals to PIB ID of the addressed Fast I2C engine)
4	RWX	RWX	I1_UNUSED_BIT_4_I0_I2C_E1_PARAM_REG: Spare
5:7	RWX	RWX	I1_I2C_E1_ADDRESS_RANGE: Fast I2C Parameter Set 1: Memory Device Local Address Range 001 = 8-bit local addressing 010 = 16-bit local addressing 011 = 24-bit local addressing 100 = 32-bit local addressing
8:9	RWX	RWX	I1_UNUSED_BIT_8_9_I0_I2C_E1_PARAM_REG: Spare
10:15	RWX	RWX	I1_I2C_E1_ENGINE_PORT: Fast I2C Parameter Set 1: Engine Port
16	RWX	RWX	I1_UNUSED_BIT_16_I0_I2C_E1_PARAM_REG: Spare
17:23	RWX	RWX	I1_I2C_E1_DEVICE_ID: Fast I2C Parameter Set 1: Target Device ID
24:25	RWX	RWX	I1_UNUSED_BIT_24_25_I0_I2C_E1_PARAM_REG: Spare
26:27	RWX	RWX	I1_I2C_E1_ENGINE_SPEED: Fast I2C Parameter Set 1: Engine Speed Setting
28:31	RWX	RWX	I1_UNUSED_BIT_4_I28_31_I2C_E1_PARAM_REG: Spare

Register Name	POR IBUF1: Fast I2C Parameter Set 2 Register
Mnemonic	EH.TPCHIP.OCC.OCI.POREGPE.I1_I2C_E2_PARAM_REG
Address	0000000000060039 (PIB) 00000000400001C8 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:3	RWX	RWX	I1_I2C_E2_ENGINE_ID: Fast I2C Parameter Set 2: Engine ID (equals to PIB ID of the addressed Fast I2C engine)
4	RWX	RWX	I1_UNUSED_BIT_4_I0_I2C_E2_PARAM_REG: Spare

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Bits	PIB	OCI	Field Mnemonic: Description
5:7	RWX	RWX	I1_I2C_E2_ADDRESS_RANGE: Fast I2C Parameter Set 2: Memory Device Local Address Range 001 = 8-bit local addressing 010 = 16-bit local addressing 011 = 24-bit local addressing 100 = 32-bit local addressing
8:9	RWX	RWX	I1_UNUSED_BIT_8_9_I0_I2C_E2_PARAM_REG: Spare
10:15	RWX	RWX	I1_I2C_E2_ENGINE_PORT: Fast I2C Parameter Set 2: Engine Port.
16	RWX	RWX	I1_UNUSED_BIT_16_I0_I2C_E2_PARAM_REG: Spare
17:23	RWX	RWX	I1_I2C_E2_DEVICE_ID: Fast I2C Parameter Set 2: Target Device ID.
24:25	RWX	RWX	I1_UNUSED_BIT_24_25_I0_I2C_E2_PARAM_REG: Spare
26:27	RWX	RWX	I1_I2C_E2_ENGINE_SPEED: Fast I2C Parameter Set 2: Engine Speed Setting.
28:31	RWX	RWX	I1_UNUSED_BIT_28_31_I0_I2C_E2_PARAM_REG: spare

Register Name	<i>I/O Status Register</i>
Mnemonic	EH.TPCHIP.OCC.OCI.PORESLOW.I0_STATUS_REG
Address	0000000000068000 (PIB) 0000000040040000 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:7	ROX	ROX	SM_STAT: Instruction engine State Machine State: 000 & state_vector(0:3) & bad_instruction_parity
8	ROX	ROX	FREEZE_PORE_ACTION_MASKED: Operation frozen due to SBE/PORE freeze action input (for example, system checkstop).
9	ROX	ROX	EXE_TRIGGER_WR_REQ_Q: Interrupt Pending. 0 = No interrupt pending. 1 = An interrupt is pending.
10:11	RO	RO	Constant = 0b00
12:15	ROX	ROX	PC_STACK_CURRENT_STATE: Stack Pointer. 0001 = Empty. 0010 = Filled up to level 1. 0100 = Filled up to level 2. 0100 = Filled up to level 3 (error handler only).
16:63	ROX	ROX	PC_Q: Program Counter is Fetch-address for POR instructions in 48b representation, counting in bytes, initial value is x8000000000000000

Register Name	<i>I/O Control And Debug Register</i>
Mnemonic	EH.TPCHIP.OCC.OCI.PORESLOW.I0_CONTROL_REG
Address	0000000000068001 (PIB) 0000000040040008 (OCI)
Attributes	
Description	



Bits	PIB	OCI	Field Mnemonic: Description
0	RWX	RWX	CTL_NO_LB: IE Stop/Run bit: 0-> automatic run-mode, 1-> STOP/debug mode. This gets cleared (run mode) upon SCOM write or Write to EXE Trigger register. This gets set (STOP/debug mode) upon SCOM write or exec WAIT 0 or System Check Stop (when enabled) or Stop on error(when enabled) or PORE IE RESET from user (SCOM Operation).
1	NCX	NCX	CTL_POR_CONT: IE Continue bit (writing '1' makes pulse) when stopped at breakpoint or SCAND-CRC-error, unaffected by Bit(3).
2	NCX	NCX	CTL_POR_SKIP: IE Skip Instruction (writing '1' makes pulse), when stopped, PC<--PC+1, to skip a long instruction write into this bit 3 times, unaffected by Bit(3)
3	NCX	NCX	CTL_SETPC: IE Set-PC (writing '1' makes pulse): Set PC to value in bits 16:63.
4:6	RWX	RWX	CTL_SCAN_CLKDIV: IE Scanclock divider setting for SCAND instruction. 000 = nclk/32 (default) 001 = nclk/64 01x = nclk/128 111 = nclk/16 110 = nclk/8 101 = nclk/4 100 = nclk/2, not written when Bit(3) = '1'
7	RWX	RWX	CTL_EXE_LOCK: EXE register lock bit, not written when Bit(3) = '1'. Control register never gets locked.
8	RWX	RWX	CTL_FREEZE_PORE_ACTION_MASK: Mask bit to freeze action based on system xstop, 0 = Not masked (default), pore_freeze_action possible 1 = Masked
9	RWX	RWX	CTL_INSTR_PAR_EN: Instruction parity check enable. 0 = Parity check disabled 1 = Parity check enabled
10	RWX	RWX	CTL_PIB_PAR_EN_B: PIB parity check disable. 0 = Parity check enabled 1 = Parity check disabled
11	RWX	RWX	CTL_TRAP_EN: Trap enable. 0 = Disabled 1 = Enabled
12	RWX	RWX	CTL_TRC_NARROW_EN: Trace bus narrow mode. 0 = Drive all 88 trace bus pins 1 = Drive only first 8 bits of trace bus (remaining 80 bits are forced to zero)
13	RWX	RWX	CTL_INT_ENABLE: PORE interrupt indication (only valid for PORE instances that can be interrupted) 0 = PORE can not be interrupted 1 = PORE can be interrupted
14	RWX	RWX	CTL_DONE_OVR: PORE done overwrite. 0 = No overwrite of PMC done indicator 1 = Force PMC done indicator to 1
15	RWX	RWX	CTL_INTERRUPT_CHKSW: Interruptible PORE feature on/off 0 = This PORE instance can not be interrupted 1 = This PORE instance can be interrupted
16:63	RWX	RWX	CTL_ABR: IE When written with Bit(3) = '0'; sets Program Counter breakpoint address. When written with Bit(3) = '1';value is written into PC (breakpoint address unchanged). On a read, the PC breakpoint address is always returned.

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Register Name	<i>I/O Reset Register</i>
Mnemonic	EH.TPCHIP.OCC.OCI.PORESLOW.IO_RESET_REG
Address	0000000000068002 (PIB) 0000000040040010 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0	RWX	RWX	PORE_IE_RESET_TRIGGER: Trigger functional reset of PORE/SBE IE, clears all register include debug registers, but does not clear ERROR MASK register.
1	RWX	RWX	PORE_OCI_RESET_TRIGGER: Trigger PORE to OCI reset.
2	RWX	RWX	SBE_RESTART_TRIGGER: Trigger functional and OCI reset and then restarts the SBE.
3	RWX	RWX	CHKSW_HW215170: Debug switch for HW215170. 0b0 : Fix enabled (default) 0b1: Fix disabled
4	RWX	RWX	CHKSW_HW217012: Debug switch for HW217012. 0b0 : Fix enabled (default) 0b1: Fix disabled
5	RWX	RWX	CHKSW_HW237648: Debug switch for HW237648. 0b0 : Fix enabled (default) 0b1: Fix disabled

Register Name	<i>POR: Error Mask Register</i>
Mnemonic	EH.TPCHIP.OCC.OCI.PORESLOW.IO_ERROR_MASK_REG
Address	0000000000068003 (PIB) 0000000040040018 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:4	RW	RW	ERROR_INTERRUPT_ENABLE: bit 0: Error event 0 bit 1: Error event 1 bit 2: Error event 2 bit 3: Error event 3 bit 4: Spare bit, set to 1 triggers corresponding error handler
5:9	RW	RW	ERROR_FIR_ENABLE: bit 0: Error event 0 bit 1: Error event 1 bit 2: Error event 2 bit 3: Error event 3 bit 4: Error event 4 bit set to 1, triggers pulse on PORE_error_out line.
10:14	RW	RW	ERROR_FATAL_ENABLE: bit 0: Error event 0 bit 1: Error event 1 bit 2: Error event 2 bit 3: Error event 3 bit 4: Error event 4 bit set to 1 triggers pulse on PORE_fatal_error_out line



Bits	PIB	OCI	Field Mnemonic: Description
15:19	RW	RW	STOP_PORE: bit 0: Error event 0 bit 1: Error event 1 bit 2: Error event 2 bit 3: Error event 3 bit 4: Error event 4 bit set to 1, stops PORE execution
20	RW	RW	GATE_PIB_CHIPLET_OFFLINE: Chiplet offline return code (010) triggers error event 0 if reset; otherwise, does not trigger error event.
21:24	RW	RW	I2C_ERROR_MASK: bit 0: Mask I2C errors type 1 (I2CM internal and parity) bit 1: Mask I2C error type 2 (Bad PIB resp I2CM -> ECCAX) bit 2: Mask I2C error type 3 (ECCAX internal) bit 3: Mask I2C error type 4 (I2C bus errors)
25:29	RW	RW	GROUP_PARITY_MASK: Masks for parity error detection of registers bit25 : Debug, status, error mask, pc stack registers bit 26: Control, exe trigger, exe t_mask, i2c param registers bit 27: Perv/oci base addr, table base addr, memory reloc bit 28: Scr0, scr1, scr2, and data scr0 registers bit 29: ibuf register

Register Name	<i>I/O Pervasive Base Address 0 Register</i>
Mnemonic	EH.TPCHIP.OCC.OCI.PORESLW.I0_PERV_BASE_ADDRESS_0_REG
Address	0000000000068004 (PIB) 0000000040040020 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:24	RO	RO	Constant = 0b000000000000000000000000
25	RWX	RWX	MULTICAST_BIT_0: Multicast bit for Base Address0, used for pervasive accesses during execution phase of instructions.
26:31	RWX	RWX	CHIPLET_ID_0: Base Address0 used for pervasive accesses during execution phase of instructions. Bits used as chiplet ID or Multicast Group part of the pervasive addresses leaving PRV PIBMS. This value can be incremented using the ADDI instruction from the PORE instruction set.

Register Name	<i>POR: Pervasive Base Address 1 Register</i>
Mnemonic	EH.TPCHIP.OCC.OCI.PORESLW.I0_PERV_BASE_ADDRESS_1_REG
Address	0000000000068005 (PIB) 0000000040040028 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:24	RO	RO	Constant = 0b000000000000000000000000
25	RWX	RWX	MULTICAST_BIT_1: Multicast Bit for Base Address1 used for pervasive accesses during execution phase of instructions.

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Bits	PIB	OCI	Field Mnemonic: Description
26:31	RWX	RWX	CHIPLET_ID_1: Base Address1 used for pervasive accesses during execution phase of instructions. Bits used as chiplet ID part of the pervasive addresses leaving PRV PIBMS. This value can be incremented using the ADDI instruction from the PORE instruction set.

Register Name		POR: OCI Base Address 0 Register	
Mnemonic		EH.TPCHIP.OCC.OCI.PORESLW.I0_OCI_BASE_ADDRESS_0_REG	
Address		000000000068006 (PIB) 0000000040040030 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:17	RO	RO	Constant = 0b000000000000000000
18:31	RWX	RWX	UNUSED_OCI_BASE_ADDRESS_0_BITS: reserved for SBE usage
32:63	RWX	RWX	OCI_BASE_ADDR_0: Base Address0 used for OCI/FI2C accesses during execution phase of instructions. Added to address parameter of instruction. This value can be incremented using the ADDI instruction from PORE instruction set.

Register Name		POR: OCI Base Address 1 Register	
Mnemonic		EH.TPCHIP.OCC.OCI.PORESLW.I0_OCI_BASE_ADDRESS_1_REG	
Address		000000000068007 (PIB) 0000000040040038 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:17	RO	RO	Constant = 0b000000000000000000
18:31	RWX	RWX	UNUSED_OCI_BASE_ADDRESS_1_BITS: reserved for SBE usage
32:63	RWX	RWX	OCI_BASE_ADDR_1: Base Address1 used for OCI/FI2C accesses during execution phase of instructions. Added to address parameter of instruction. This value can be incremented using the ADDI instruction from PORE instruction set.

Register Name		POR: Table Base Address Register	
Mnemonic		EH.TPCHIP.OCC.OCI.PORESLW.I0_TABLE_BASE_ADDRESS_REG	
Address		000000000068008 (PIB) 0000000040040040 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:15	RO	RO	Constant = 0b0000000000000000



Bits	PIB	OCI	Field Mnemonic: Description
16	RWX	RWX	TABLE_BASE_ADDR_INTERFACE: Interface used to access the Base Table (used for Start Vectors and Error Handlers) 0 = PIB/PERV 1 = OCI/FI2C
17	RWX	RWX	RESERVED_TABLE_BASE_ADDRESS_BITS: Reserved.
18:23	RWX	RWX	TABLE_BASE_ADDR_CHIPLLET_ID: In case of PIB/PERV or FI2C interface, this field defines the pervasive chiplet ID, unused for OCI.
24:27	RWX	RWX	TABLE_BASE_ADDR_PIB_ID: In case of PIB/PERV or FI2C interface, this field defines the PIB master ID, unused for OCI.
28:31	RWX	RWX	TABLE_BASE_ADDR_PORT_ID: In case of PIB/PERV or FI2C interface, this field defines the pervasive port ID, unused for OCI.
32:63	RWX	RWX	TABLE_BASE_ADDR: Table base address for jump table. This value can be incremented using the ADDI instruction from PORE instruction set.

Register Name	POR: EXE Trigger Register
Mnemonic	EH.TPCHIP.OCC.OCI.PORESLOW.IO_EXE_TRIGGER_REG
Address	0000000000068009 (PIB) 0000000040040048 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:7	RO	RO	Constant = 0b00000000
8:11	RWX	RWX	START_VECTOR: Writing to start_vector causes PORE to enter run mode at the corresponding address given by (start_vector X 3) + 0x0018. This register is locked when CONTROL_REG bit(0) is '0' (in run mode) or if CONTROL_REG bit(7) is '1' (CTL_EXE_LOCK). The start vector is cleared upon PORE IE RESET.
12:31	RO	RO	Constant = 0b00000000000000000000
32:63	RWX	RWX	START_PARAMETER: One bit for each chiplet, bit(32 - 47) -> chiplets 0 - 15, which determines whether this chiplet is part of the MC accesses. This register is locked when CONTROL_REG bit(0) is '0' (in run mode) or if CONTROL_REG bit(7) is '1' (CTL_EXE_LOCK). The start_parameter is cleared upon PORE IE RESET.

Register Name	POR: Scratch0 Register, Address
Mnemonic	EH.TPCHIP.OCC.OCI.PORESLOW.IO_SCRATCH0_REG
Address	000000000006800A (PIB) 0000000040040050 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:7	RO	RO	Constant = 0b00000000
8:31	RWX	RWX	SCRATCH0: POR IE Scratch0 Register, 24 bits. This register is locked when CONTROL_REG bit(0) is '0'.



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Register Name		<i>POR: Scratch1 Register, Data</i>	
Mnemonic		EH.TPCHIP.OCC.OCI.PORESLW.I0_SCRATCH1_REG	
Address		000000000006800B (PIB) 0000000040040058 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:63	RWX	RWX	SCRATCH1: POR IE Scatch1 Register, 64-bit data buffer. This register is locked when CONTROL_REG bit(0) is '0'.

Register Name		<i>POR: Scratch2 Register, Data</i>	
Mnemonic		EH.TPCHIP.OCC.OCI.PORESLW.I0_SCRATCH2_REG	
Address		000000000006800C (PIB) 0000000040040060 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:63	RWX	RWX	SCRATCH2: POR IE Scatch2 Register, 64-bit data buffer. This register is locked when CONTROL_REG bit(0) is '0'.

Register Name		<i>I/O First 64 Bits of the Instruction Buffer</i>	
Mnemonic		EH.TPCHIP.OCC.OCI.PORESLW.I0_IBUF_LO_REG	
Address		000000000006800D (PIB) 0000000040040068 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:63	RWX	RWX	IBUF_LO: POR IE Instruction Buffer, bits 0-63, This register is locked when CONTROL_REG bit(0) is '0'

Register Name		<i>I/O Last 32 Bits of the Instruction Buffer</i>	
Mnemonic		EH.TPCHIP.OCC.OCI.PORESLW.I0_IBUF_2_REG	
Address		000000000006800E (PIB) 0000000040040070 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:31	RWX	RWX	IBUF_2: POR IE Instruction Buffer, bits 64-95, This register is locked when CONTROL_REG bit(0) is '0'



Register Name	<i>I/O Debug 0 Register</i>
Mnemonic	EH.TPCHIP.OCC.OCI.PORESLOW.IO_DBG0_REG
Address	000000000006800F (PIB) 0000000040040078 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:31	RWX_WCLRR EG	RWX_WCLRRREG	LAST_PIBMS_ACCESS_ADDRESS: POR PIB Master: Address of last completed access : Register gets cleared upon PORE IE Reset.
32	RWX_WCLRR EG	RWX_WCLRRREG	PIB_DATA_READ_P_ERR: Parity error in read data from PRV PIB.
33:35	RWX_WCLRR EG	RWX_WCLRRREG	LAST_PIBMS_ACCESS_RETURN_CODE: POR PIB Master: Last Return Code from PIB/PCB (SCRESP): For example: 000: OK 010: Chiplet offline 100: Invalid address 110: Parity error / unexpected/wrong packet 111: Timeout
36	RWX_WCLRR EG	RWX_WCLRRREG	I2C_BAD_STATUS_0: I2CM internal errors including parity errors.
37	RWX_WCLRR EG	RWX_WCLRRREG	I2C_BAD_STATUS_1: Bad PIB response code error for ECCAX to I2CM communication.
38	RWX_WCLRR EG	RWX_WCLRRREG	I2C_BAD_STATUS_2: ECCAX internal errors (UCE or PIB master resets).
39	RWX_WCLRR EG	RWX_WCLRRREG	I2C_BAD_STATUS_3: I2C bus issues (I2C bus busy, NACK, stop bit error).
40	RWX_WCLRR EG	RWX_WCLRRREG	GROUP_PARITY_ERROR_0: Parity error from debug or status or error mask or pc stack registers
41	RWX_WCLRR EG	RWX_WCLRRREG	GROUP_PARITY_ERROR_1: Parity error from control or exe trigger or exe t_mask or I2C param registers.
42	RWX_WCLRR EG	RWX_WCLRRREG	GROUP_PARITY_ERROR_2: Parity error from perv/oci base addr or table base addr or memory reloc.
43	RWX_WCLRR EG	RWX_WCLRRREG	GROUP_PARITY_ERROR_3: Parity error from scr0, scr1, scr2, or data scr0 register.
44	RWX_WCLRR EG	RWX_WCLRRREG	GROUP_PARITY_ERROR_4: Parity error from ibuf register
45:52	ROX	ROX	INTERRUPT_COUNTER_Q: Counter that tracks the number of instructions executed after the exe trigger write request is queued and interrupt enable is not set.

Register Name	<i>I/O Debug 1 Register</i>
Mnemonic	EH.TPCHIP.OCC.OCI.PORESLOW.IO_DBG1_REG
Address	0000000000068010 (PIB) 0000000040040080 (OCI)
Attributes	
Description	

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Bits	PIB	OCI	Field Mnemonic: Description
0:31	RWX_WCLRR EG	RWX_WCLRREG	LAST_PC_ACCESS_ADDRESS_0_31: POR PC: Address of last completed PC access. Register gets cleared upon PORE IE Reset.
32:47	RWX_WCLRR EG	RWX_WCLRREG	LAST_PC_ACCESS_ADDRESS_32_47: POR PC: Address of last completed PC access. Register gets cleared upon PORE IE Reset.
48	RWX_WCLRR EG	RWX_WCLRREG	OCI_DATA_READ_P_ERR: Parity error in read data from OCI.
49:51	RWX_WCLRR EG	RWX_WCLRREG	LAST_OCIMS_ACCESS_RETURN_CODE: POR OCI Master: Last Return Code from OCI (error).
52	RWX_WCLRR EG	RWX_WCLRREG	BAD_PAR: Bad instruction parity.
53	RWX_WCLRR EG	RWX_WCLRREG	BAD_INSTRUCTION: Invalid instruction.
54	RWX_WCLRR EG	RWX_WCLRREG	BAD_PC: PC Overflow/underflow.
55	RWX_WCLRR EG	RWX_WCLRREG	SCAN_DATA_CRC: Scan data CRC error.
56	RWX_WCLRR EG	RWX_WCLRREG	PC_STACK_ERR: PC stack PUSH error or POP error.
57	RWX_WCLRR EG	RWX_WCLRREG	INSTR_FETCH_ERROR: Nonzero return code or read data parity error was received during fetch phase.
58	RWX_WCLRR EG	RWX_WCLRREG	BAD_OPERAND: Invalid instruction operand.
59	RWX_WCLRR EG	RWX_WCLRREG	BAD_INSTRUCTION_PATH: Invalid instruction path (for example, FI2C parameter miss).
60	RWX_WCLRR EG	RWX_WCLRREG	BAD_START_VECTOR_TRIGGER: Invalid start vector triggered.
61	RWX_WCLRR EG	RWX_WCLRREG	FI2C_PROTOCOL_HANG: Fast I2C protocol hang detected - exceeded poll limit for FI2C engine
62	RWX_WCLRR EG	RWX_WCLRREG	ROL_INVALID: Unused, reads 0.
63	RWX_WCLRR EG	RWX_WCLRREG	PIBMS_DBG_LOCK: Lock debug0/1 registers on occurrence of error events 0-3. That is, when any one of PIBMS DBG0 Register (32:35) OR PIBMS DBG1 Register (48:55) is set.

Register Name	<i>I/O Stack Level 0 Register</i>
Mnemonic	EH.TPCHIP.OCC.OCI.PORESLOW.I0_PC_STACK0_REG
Address	0000000000068011 (PIB) 0000000040040088 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:47	RWX	RWX	STACK0_DATA: Stack data level 0
48:58	RO	RO	Constant = 0b000000000000
59	RWX	RWX	SET_STACK_POINTER: If set, the value in bits 60:63 is applied as a new stack pointer.



Bits	PIB	OCI	Field Mnemonic: Description
60:63	RWX	RWX	NEW_STACK_POINTER: If bit 59 is set, the Stack Pointer is overwritten: 0001 = Stack empty 0010 = Stack filled up to level 0 0100 = Stack filled up to level 1 1000 = Stack filled up to level 2

Register Name	<i>I/O Stack Level 1 Register</i>
Mnemonic	EH.TPCHIP.OCC.OCI.PORESLOW.I0_PC_STACK1_REG
Address	0000000000068012 (PIB) 0000000040040090 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:47	RWX	RWX	STACK1_DATA: Stack data level 1

Register Name	<i>I/O Stack Level 2 Register</i>
Mnemonic	EH.TPCHIP.OCC.OCI.PORESLOW.I0_PC_STACK2_REG
Address	0000000000068013 (PIB) 0000000040040098 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:47	RWX	RWX	STACK2_DATA: stack data level 2

Register Name	<i>I/O ID Flags Register</i>
Mnemonic	EH.TPCHIP.OCC.OCI.PORESLOW.I0_ID_FLAGS_REG
Address	0000000000068014 (PIB) 00000000400400A0 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:31	RO	RO	Constant = 0b00000000000000000000000000000000
32	ROX	ROX	PIB_EXECUTION_PARITY_FAIL: PIB execution phase parity error indicator: Holds the PIB parity error indicator bit for the last execution phase access
33:35	ROX	ROX	PIB_EXECUTION_STATUS_FIELD: PIB execution phase status indicator: Holds the PIB response status of the last execution phase access
36	ROX	ROX	OCI_EXECUTION_PARITY_FAIL: OCI execution phase parity error indicator: Holds the OCI parity error indication bit for the last execution phase access
37:39	ROX	ROX	OCI_EXECUTION_STATUS_FIELD: OCI execution phase status indicator: Holds the OCI response status of the last execution phase access
40:47	RO	RO	Constant = 0b00000000
48:55	RWX	RWX	ALU_FLAGS: Alu flags: UGT,ULT,SGT,SLT,C,O,N,Z



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Bits	PIB	OCI	Field Mnemonic: Description
56:63	RO	RO	Constant = 0b00001000

Register Name	<i>I/O Data0 Register</i>
Mnemonic	EH.TPCHIP.OCC.OCI.PORESLW.I0_DATA0_REG
Address	0000000000068015 (PIB) 00000000400400A8 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:31	RWX	RWX	DATA0: Scratch Data 0

Register Name	<i>I/O Memory Relocation Register</i>
Mnemonic	EH.TPCHIP.OCC.OCI.PORESLW.I0_MEMORY_RELOC_REG
Address	0000000000068016 (PIB) 00000000400400B0 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:29	RO	RO	Constant = 0b00000000000000000000000000000000
30:31	RWX	RWX	MEM_RELOC_REGION: Memory Relocation Region
32:51	RWX	RWX	MEM_RELOC_BASE: Memory Relocation Base Address

Register Name	<i>I/O Fast I2C Parameter Set 0 Register</i>
Mnemonic	EH.TPCHIP.OCC.OCI.PORESLW.I0_I2C_E0_PARAM_REG
Address	0000000000068017 (PIB) 00000000400400B8 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:31	RWX	RWX	UNUSED_I2C_E0_PARAM_BITS: reserved for SBE usage

Register Name	<i>I/O Fast I2C Parameter Set 1 Register</i>
Mnemonic	EH.TPCHIP.OCC.OCI.PORESLW.I0_I2C_E1_PARAM_REG
Address	0000000000068018 (PIB) 00000000400400C0 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:31	RWX	RWX	UNUSED_I2C_E1_PARAM_BITS: reserved for SBE usage



Register Name		<i>I/O Fast I2C Parameter Set 2 Register</i>	
Mnemonic		EH.TPCHIP.OCC.OCI.PORESLOW.I0_I2C_E2_PARAM_REG	
Address		0000000000068019 (PIB) 00000000400400C8 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:31	RWX	RWX	UNUSED_I2C_E2_PARAM_BITS: reserved for SBE usage

Register Name		<i>Register For Low Level Control of the PPC405</i>	
Mnemonic		EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCR	
Address		000000000006B000 (PIB) 000000000006B001 (PIB1) 000000000006B002 (PIB2)	
Attributes			
Description			

Bits	PIB	PIB1	PIB2	Field Mnemonic: Description
0	ROX	WOX_AND	WOX_OR	OCB_PIB_OCR_CORE_RESET: Controls the core_reset pin to the PPC405. Note: - the reset value puts the PPC405 into reset - a PIB slave reset may or may not set this bit as well. See bit 9 (pib_slave_reset_to_405_enable) which controls this behavior.
1	RO	WO_AND	WO_OR	OCB_PIB_OCR_CHIP_RESET: Controls the chip_reset pin to the PPC405.
2	RO	WO_AND	WO_OR	OCB_PIB_OCR_SYSTEM_RESET: Controls the system_reset pin to the PPC405.
3	RO	WO_AND	WO_OR	OCB_PIB_OCR_OCI_ARB_RESET: Controls the reset pin to the OCI arbiter
4	RO	WO_AND	WO_OR	OCB_PIB_OCR_TRACE_DISABLE: Disables the PPC405 Trace function when set
5	RO	WO_AND	WO_OR	OCB_PIB_OCR_TRACE_EVENT: Asserts a trigger event to the PPC405
6	RO	WO_AND	WO_OR	OCB_PIB_OCR_DBG_UNCONDITIONAL_EVENT: Asserted the unconditional debug event (UDE) and sets the UDE bit of the debug status register (DBSR) if enabled.
7	RO	WO_AND	WO_OR	OCB_PIB_OCR_EXT_INTERRUPT: Asserts an external interrupt to the PPC405
8	RO	WO_AND	WO_OR	OCB_PIB_OCR_CRITICAL_INTERRUPT: Asserts a critical interrupt to the PPC405
9	RO	WO_AND	WO_OR	OCB_PIB_OCR_PIB_SLAVE_RESET_TO_405_ENABLE: Controls whether a PIB slave reset will put the PPC405 into reset or not. 0 - PIB slave reset does not cause PPC405 reset (default) 1 - PIB slave reset causes PPC405 reset (sets bit 0)
10:15	RO	WO_AND	WO_OR	OCB_PIB_OCR_SPARE: Implemented but unused
16:63	RO	RO	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

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Register Name		Register For Debug Control Of OCI Masters And Slaves
Mnemonic		EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCDBG
Address		000000000006B003 (PIB)
Attributes		
Description		
Bits	PIB	Field Mnemonic: Description
0	RW	OCB_PIB_OCDBG_MST_DIS_ABUSPAREN: Disable ADBUS_PAREN - Disable address parity generation
1	RW	OCB_PIB_OCDBG_MST_DIS_BEPAEN: Disable BE_PAREN - Disable byte enable parity generation
2	RW	OCB_PIB_OCDBG_MST_DIS_WRDBUSPAREN: Disable WRDATA_PAREN - Disable write data parity generation
3	RW	OCB_PIB_OCDBG_MST_DIS_RDDBUSPAR: Disable read data parity checking - Parity checking on read data will be disabled and data will be forwarded to unit
4	RW	OCB_PIB_OCDBG_MST_SPARE: Spare debug signal for OCI Master
5	RW	OCB_PIB_OCDBG_SLV_DIS_SACK: Disable acknowledge of secondary requests - 'savalid' will be ignored and interface component will respond only to 'pavalid'
6	RW	OCB_PIB_OCDBG_SLV_DIS_ABUSPAR: Disable address parity checking - Address parity error will be ignored
7	RW	OCB_PIB_OCDBG_SLV_DIS_BEPAEN: Disable byte enable parity checking - Byte enable parity error will be ignored
8	RW	OCB_PIB_OCDBG_SLV_DIS_BE: Disable byte enable correctness checking - Invalid combinations of Byte Enable will be ignored and transfer will be allowed to progress to Unit with all '1' byte_enable.
9	RW	OCB_PIB_OCDBG_SLV_DIS_WRDBUSPAR: Disable write data parity checking - Parity checking on write data will be disabled and data will be forwarded to Unit.
10	RW	OCB_PIB_OCDBG_SLV_DIS_RDDBUSPAREN: Disable RDDBUS_PAREN - Disable read data parity generation.
11	RW	OCB_PIB_OCDBG_SLV_SPARE: Spare debug signal for OCI Slave
12:15	RW	OCB_PIB_OCDBG_SPARE: Implemented but unused
16:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name		This Register Contains The Configuration Bits For Setting Up To Communicate With The PPC405 Via JTAG		
Mnemonic		EH.TPCHIP.OCC.OCI.OCB.JTG_PIB_OJCFG		
Address		000000000006B004 (PIB) 000000000006B005 (PIB1) 000000000006B006 (PIB2)		
Attributes				
Description				
Bits	PIB	PIB1	PIB2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	JTG_PIB_OJCFG_JTAG_SRC_SEL: Select source to drive the 405 JTAG pins 0 : OCC FSM 1 : FSI (toad mode)
1	RW	WO_AND	WO_OR	JTG_PIB_OJCFG_RUN_TCK: Control TCK clock (also used as act to enable all associated JTAG driver latches) 0 : off 1 : on

[illegible]

Register Name	<i>This PIB Accessible Register Captures The OCI Address That Is Desired To Be Accessed</i>
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBAR0
Address	000000000006B010 (PIB)
Attributes	Magic=true
Description	

Bits	PIB	Field Mnemonic: Description
0:1	RW	OCB_PIB_OCBAR0_OCI_REGION: OCI Address Space Region 00 – Processor bus 01 – Registers Reserved (register space access not supported) 10 - Reserved 11 - SRAM
2:28	RW	OCB_PIB_OCBAR0_OCB_ADDRESS: Address of 8-byte quantity the OCI for this channel field contents depends on accessed oci_region Registers 2:13 – Reserved 13:15 - OCI Slave 16:28 - Register # Processor Bus 2:11 - Maskable Alignment 12:28 - Offset SRAM 2:13 - SRAM Tank BAR (FFs) 14:28 - Offset
29:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>This PIB Accessible Register That Controls The Function of the OCB Channel And Provides Status Of It</i>
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBCSR0
Address	000000000006B011 (PIB) 000000000006B012 (PIB1) 000000000006B013 (PIB2)
Attributes	Magic=true
Description	

Bits	PIB	PIB1	PIB2	Field Mnemonic: Description
0	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR0_PULL_READ_UNDERFLOW: Pull Queue Read Underflow Underflow is defined as a read to the OCB Data [n] Register and the pull_empty facility is already set. This bit is cleared only by a firmware write of this bit to 0.Writes store the value. UNDERFLOW_NOT_DETECTED=>0b0 UNDERFLOW_DETECTED=>0b1

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Bits	PIB	PIB1	PIB2	Field Mnemonic: Description
1	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR0_PUSH_WRITE_OVERFLOW: Push Queue Write Overflow Overflow is defined as a store to the OCB Data [n] Register and the push_full facility is already set. This bit is cleared only by a firmware write of this bit to 0. OVERFLOW_NOT_DETECTED=>0b0 OVERFLOW_DETECTED=>0b1
2	RO	WO_AND	WO_OR	OCB_PIB_OCBCSR0_PULL_READ_UNDERFLOW_EN: Enable the setting of pull_read_underflow by hardware. 0 - Underflow detection disabled 1 - Underflow detection enabled This bit is set using the OR mask register and cleared using the AND mask register.
3	RO	WO_AND	WO_OR	OCB_PIB_OCBCSR0_PUSH_WRITE_OVERFLOW_EN: Enable the setting of push_write_overflow by hardware. 0 - Overflow detection disabled 1 - Overflow detection enabled This bit is set using the OR mask register and cleared using the AND mask register.
4	RO	WO_AND	WO_OR	OCB_PIB_OCBCSR0_OCB_STREAM_MODE: Put the bridge channel in streaming mode with the behavior further defined by the setting of ocb_stream_type 0 - Stream Mode Disabled 1 - Stream Mode Enabled This bit is set using the OR mask register and cleared using the AND mask register.
5	RO	WO_AND	WO_OR	OCB_PIB_OCBCSR0_OCB_STREAM_TYPE: Type of streaming enabled by ocb_stream_mode = 1 0 - Linear 1 - Circular For Linear type, the ocb_address field is incremented by 8 with each access to the OCB Data [n] Register. In Circular type, the address manipulation via access to OCB Stream [PushPull] Increment registers This bit is set using the OR mask register and cleared using the AND mask register.
6:7	RO	WO_AND	WO_OR	OCB_PIB_OCBCSR0_SPARE0: Implemented but not used
8	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR0_OCB_OCI_TIMEOUT: Indicates the MnTimeout signal on the OCI for the OCB Master was asserted to flag that no OCI slave acknowledged the request. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
9	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR0_OCB_OCI_READ_DATA_PARITY: Indicates the OCI read data parity was in error This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
10	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR0_OCB_OCI_SLAVE_ERROR: Indicates the SlvError signal on the OCI for the OCB Master was asserted. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
11	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR0_OCB_PIB_ADDR_PARITY_ERR: Indicates the PIB address parity was in error (PIB read or write operation) This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
12	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR0_OCB_PIB_DATA_PARITY_ERR: Indicates the PIB data parity was in error for a PIB write operation This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
13	RO	WO_AND	WO_OR	OCB_PIB_OCBCSR0_SPARE1: Implemented but not used
14	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR0_OCB_FSM_ERR: Catastrophic state machine error This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.



Bits	PIB	PIB1	PIB2	Field Mnemonic: Description
15	RO	WO_AND	WO_OR	OCB_PIB_OCBCSR0_SPARE2: Implemented but not used Writes store the value. Reads return the last value written.
16:63	RO	RO	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>This PIB Accessible Register</i>		
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBESR0		
Address	000000000006B014 (PIB)		
Attributes			
Description	See OCB Control/Status [n] Register for the specific error(s) detected. Set and Locked by hardware, Write to clear and Unlock. This PIB accessible register Indicates The OCI Address Of A Channel Operation That Detected The First Error		

Bits	PIB	Field Mnemonic: Description
0:31	RWX_WCLRR EG	OCB_PIB_OCBESR0_OCB_ERROR_ADDR: OCI address being accessed when the first channel error is detected. This register is cleared when writing any value.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>PIB Accessible Register</i>		
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBDR0		
Address	000000000006B015 (PIB)		
Attributes			
Description	Captures The PIB Data To Be Written On The OCI Or The OCI Data Read Returned Without Errors From The OCI Address That Is Desired To Be Accessed		

Bits	PIB	Field Mnemonic: Description
0:63	WOX	OCB_PIB_OCBDR0_OCB_DATA: Data to/from OCI for this channel

Register Name	<i>EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLBR0</i>		
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLBR0		
Address	000000000006A200 (PIB) 0000000040051000 (OCI)		
Attributes			
Description			

Bits	PIB	OCI	Field Mnemonic: Description
0:1	RW	RW	OCB_OCI_OCBSLBR0_PULL_OCI_REGION: Pull OCI Region allowed values: 00 - PBA 11 - SRAM Others are reserved
2:28	RW	RW	OCB_OCI_OCBSLBR0_PULL_START: Starting address of Pull Queue (8-byte alignment)
29:63	RO	RO	Constant = 0b00000000000000000000000000000000

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Register Name		<i>Writes To This Register Cause The Pull Queue To Be Reset</i>	
Mnemonic		EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLCS0	
Address		000000000006A201 (PIB) 0000000040051008 (OCI)	
Attributes		Magic=true	
Description		OCB0. Writes to this register cause the Pull queue to be reset.	

Bits	PIB	OCI	Field Mnemonic: Description
0	RWX_WCLRPART	RWX_WCLRPART	OCB_OCI_OCBSLCS0_PULL_FULL: Reads indicate the Pull Queue is full condition. Any write to this register clears this indicator and clears pull_write_ptr and pull_read_ptr to 0s. (This is a means for resetting the queue hardware.) RWX_WCLRPART NOT_FULL=>0b0 FULL=>0b1
1	RWX_WSETPART	RWX_WSETPART	OCB_OCI_OCBSLCS0_PULL_EMPTY: Reads indicate the Pull Queue empty condition. Any write to this register sets this indicator and clears pull_write_ptr and pull_read_ptr to 0s. This is a means for resetting the queue hardware.) RWX_WSETPART NOT_EMPTY=>0b0 EMPTY=>0b1
2:3	RW	RW	OCB_OCI_OCBSLCS0_SPARE: Implemented but not used. Writes store the value. Reads return the last value written.
4:5	RW	RW	OCB_OCI_OCBSLCS0_PULL_INTR_ACTION_0_1: Pull Interrupt Action. This field controls the condition which will assert the pull interrupt signal for this channel to the OCB interrupt controller. b00 = Full (default upon hardware initialization) b01 = Non Full b10 = Empty (the more useful firmware default) b11 = Not Empty

Bits	PIB	OCI	Field Mnemonic: Description
6:10	RW	RW	OCB_OCI_OCBSLCS0_PULL_LENGTH: Pull Queue length in (pull_length + 1) * 8 bytes. Value mapping: 0b00000: 8 bytes 0b00001: 16 bytes 0b00010: 24 bytes 0b00011: 32 bytes 0b00100: 40 bytes 0b00101: 48 bytes 0b00110: 56 bytes 0b00111: 64 bytes 0b01000: 72 bytes 0b01001: 80 bytes 0b01010: 88 bytes 0b01011: 96 bytes 0b01100: 104 bytes 0b01101: 112 bytes 0b01110: 120 bytes 0b01111: 128 bytes 0b10000: 136 bytes 0b10001: 144 bytes 0b10010: 152 bytes 0b10011: 160 bytes 0b10100: 168 bytes 0b10101: 176 bytes 0b10110: 184 bytes 0b10111: 192 bytes 0b11000: 200 bytes 0b11001: 208 bytes 0b11010: 216 bytes 0b11011: 224 bytes 0b11100: 232 bytes 0b11101: 240 bytes 0b11110: 248 bytes 0b11111: 256 bytes
11:12	RO	RO	Constant = 0b00
13:17	RWX_WCLRPART	RWX_WCLRPART	OCB_OCI_OCBSLCS0_PULL_WRITE_PTR: Pull write pointer Reads indicate the current Pull Queue write pointer in increments of 8 bytes. The actual address used is pull_oci_region pull_start + pull_write_ptr 00000. Writes to this field are ignored. Hardware performs all modifications. This field is cleared with a write to this register. ROX_WCLRPART
18:20	RO	RO	Constant = 0b000
21:25	RWX_WCLRPART	RWX_WCLRPART	OCB_OCI_OCBSLCS0_PULL_READ_PTR: Pull read pointer Reads indicate the current Pull Queue read pointer in increments of 8 bytes. The actual address used is pull_oci_region pull_start + pull_write_ptr 00000. This field is cleared with a write to this register. ROX_WCLRPART
26:30	RO	RO	Constant = 0b00000
31	RW	RW	OCB_OCI_OCBSLCS0_PULL_ENABLE: Enables the Pull Queue function If Disabled, PIB Reads to OCB Data [n] Register to perform a pull will result in an offline PIB error back to the PIB Master. Note: OCI Reads to OCB Stream Pull Increment [n] Register to cause incrementation are unaffected by the setting of this bit. Full and/or empty conditions may still arise to the OCC even if this bit indicates disabled. DISABLED=>0b0 ENABLED=>0b1

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Bits	PIB	OCI	Field Mnemonic: Description
32:63	RO	RO	Constant = 0b00000000000000000000000000000000 DISABLED=>0b0 ENABLED=>0b1

Register Name	<i>EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHBR0</i>
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHBR0
Address	000000000006A203 (PIB) 0000000040051018 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:1	RW	RW	OCB_OCI_OCBSHBR0_PUSH_OCI_REGION: Push OCI Region Allowed values: 00 - PBA 11 - SRAM Others are reserved
2:28	RW	RW	OCB_OCI_OCBSHBR0_PUSH_START: Starting address of Push Queue (8-byte alignment)
29:63	RO	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>Controls the Behavior Of Push Queue N</i>
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHCS0
Address	000000000006A204 (PIB) 0000000040051020 (OCI)
Attributes	Magic=true
Description	Writes to this register cause the queue hardware to be reset.

Bits	PIB	OCI	Field Mnemonic: Description
0	RWX_WCLRPART	RWX_WCLRPART	OCB_OCI_OCBSHCS0_PUSH_FULL: Reads indicate the Push Queue is full condition Any write to this register clears this indicator and clears push_write_ptr and push_read_ptr to 0s. (this is a means for resetting the queue hardware) RWX_WCLR NOT_FULL=>0b0 FULL=>0b1
1	RWX_WSETPART	RWX_WSETPART	OCB_OCI_OCBSHCS0_PUSH_EMPTY: Read indicates the Push Queue empty condition. Any write to this register sets this indicator and clears push_write_ptr and push_read_ptr to 0s. (This is a means for resetting the queue hardware.) RWX_WSETPART NOT_EMPTY=>0b0 EMPTY=>0b1
2:3	RW	RW	OCB_OCI_OCBSHCS0_SPARE: Implemented but not used. Writes store the value. Reads return the last value written.

Bits	PIB	OCI	Field Mnemonic: Description
4:5	RW	RW	OCB_OCI_OCBSHCS0_PUSH_INTR_ACTION_0_1: Push Interrupt Action This field controls the condition which will assert the push interrupt signal for this channel to the OCB interrupt controller. b00 = Full (default upon hardware initialization) b01 = Non Full b10 = Empty b11 = Not Empty
6:10	RW	RW	OCB_OCI_OCBSHCS0_PUSH_LENGTH: Push queue length in (push_length + 1) * 8 bytes. Value mapping: 0b00000: 8 bytes 0b00001: 16 bytes 0b00010: 24 bytes 0b00011: 32 bytes 0b00100: 40 bytes 0b00101: 48 bytes 0b00110: 56 bytes 0b00111: 64 bytes 0b01000: 72 bytes 0b01001: 80 bytes 0b01010: 88 bytes 0b01011: 96 bytes 0b01100: 104 bytes 0b01101: 112 bytes 0b01110: 120 bytes 0b01111: 128 bytes 0b10000: 136 bytes 0b10001: 144 bytes 0b10010: 152 bytes 0b10011: 160 bytes 0b10100: 168 bytes 0b10101: 176 bytes 0b10110: 184 bytes 0b10111: 192 bytes 0b11000: 200 bytes 0b11001: 208 bytes 0b11010: 216 bytes 0b11011: 224 bytes 0b11100: 232 bytes 0b11101: 240 bytes 0b11110: 248 bytes 0b11111: 256 bytes
11:12	RO	RO	Constant = 0b00
13:17	RWX_WCLRPART	RWX_WCLRPART	OCB_OCI_OCBSHCS0_PUSH_WRITE_PTR: Push write pointer. Reads indicate the current Push Queue write pointer in increments of 8 bytes. The actual address used is push_oci_region push_start + push_write_ptr 00000. Writes to this field are ignored. Hardware performs all modifications. This field is cleared on a write to this register. ROX_WCLRPART.
18:20	RO	RO	Constant = 0b000
21:25	RWX_WCLRPART	RWX_WCLRPART	OCB_OCI_OCBSHCS0_PUSH_READ_PTR: Push read pointer. Reads indicate the current Push Queue read pointer in increments of 8 bytes. The actual address used is push_oci_region push_start + push_read_ptr 00000. This field is cleared on a write to this register. ROX_WCLRPART.
26:30	RO	RO	Constant = 0b00000

[illegible]

Register Name	<i>OCI Accessible Register Controls the Linear Write Window Access Facility</i>
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCI_OCBLWCR0
Address	000000000006A208 (PIB) 0000000040051040 (OCI)
Attributes	Magic=true
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0	RW	RW	OCB_OCI_OCBLWCR0_LINEAR_WINDOW_ENABLE: Linear Window Enable 0: Window facility disabled. 1: Window facility enabled. If OCBCSR[n].ocb_stream_type= linear, Linear Window BAR and Mask are valid and operations are to be honored. sc_resp codes are the same as for the OCB indirect facility to reflect the status of the OCI operation.
1:3	RW	RW	OCB_OCI_OCBLWCR0_SPARE_0: Implemented but not used. Writes store the value. Reads return the last value written.
4:19	RW	RW	OCB_OCI_OCBLWCR0_LINEAR_WINDOW_BAR: Linear Window Base Address Register Defines OCI address(13:28) - 16 bits to define the starting offset within the region addressed
20:31	RW	RW	OCB_OCI_OCBLWCR0_LINEAR_WINDOW_MASK: Linear Window Address Mask. Register masks OCI address (17:28) - 12 bits to define the window size.
32:63	RO	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>OCI Accessible Register that Defines the Placement of the SRAM Base Address</i>
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWSBR0
Address	000000000006A20C (PIB) 0000000040051060 (OCI)
Attributes	Magic=true
Description	This OCI Accessible Register that defines the placement of the SRAM Base Address for use by the OCB Linear Write Window Function of the Indirect Channel

Bits	PIB	OCI	Field Mnemonic: Description
0:1	RW	RW	OCB_OCI_OCBLWSBR0_LINEAR_WINDOW_REGION: Linear Window Region. If linear_window_enable = 1, this field defines the OCI region (OCI Address(0:1) that is enabled for accessing the Linear Window. If the value written into OCBAR[n] does not match this value and the OCBDR[n] is accessed, a PIB sresp error is produced. Only the SRAM region (0b11) is supported.



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Bits	PIB	OCI	Field Mnemonic: Description
2:9	RW	RW	OCB_OCI_OCBLWSBR0_LINEAR_WINDOW_BASE: Linear Window Base. If linear_window_enable = 1, OCI Address(5:12) is established; 128-byte aliases still apply (for example, OCI Address[2:4]). With linear_window_region = SRAM (0b11), this field must be set to the SRAM address base. (See SRAM Base Address Register.)
10:63	RO	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>PIB Accessible Register Captures the OCI Address that is Desired to be Accessed</i>
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBAR1
Address	000000000006B030 (PIB)
Attributes	Magic=true
Description	

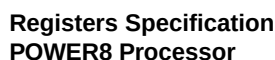
Bits	PIB	Field Mnemonic: Description
0:1	RW	OCB_PIB_OCBAR1_OCI_REGION: OCI Address Space Region 00 - Processor bus 01 - Registers Reserved (register space access not supported) 10 - Reserved 11 - SRAM
2:28	RW	OCB_PIB_OCBAR1_OCB_ADDRESS: Address of 8-byte quantity the OCI for this channel field contents depends on accessed oci_region. Registers: 2:13 - Reserved; 13:15 - OCI Slave; 16:28 - Register # Processor Bus 2:11 - Maskable Alignment; 12:28 - Offset SRAM 2:13 - SRAM Tank BAR (FFs); 14:28 - Offset
29:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>PIB Accessible Register that Controls the Function of the OCB Channel and Provides Status</i>
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBCSR1
Address	000000000006B031 (PIB) 000000000006B032 (PIB1) 000000000006B033 (PIB2)
Attributes	Magic=true
Description	This PIB Accessible Register that controls the function of the OCB channel and provides status of it.

Bits	PIB	PIB1	PIB2	Field Mnemonic: Description
0	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR1_PULL_READ_UNDERFLOW: Pull Queue Read Underflow. Underflow is defined as a read to the OCB Data [n] Register and the pull_empty facility is already set. This bit is cleared only by a firmware write of this bit to 0. Writes store the value. UNDERFLOW_NOT_DETECTED=>0b0 UNDERFLOW_DETECTED=>0b1
1	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR1_PUSH_WRITE_OVERFLOW: Push Queue Write Overflow. Overflow is defined as a store to the OCB Data [n] Register and the push_full facility is already set. This bit is cleared only by a firmware write of this bit to 0. OVERFLOW_NOT_DETECTED=>0b0 OVERFLOW_DETECTED=>0b1



Bits	PIB	PIB1	PIB2	Field Mnemonic: Description
2	RO	WO_AND	WO_OR	OCB_PIB_OCBCSR1_PULL_READ_UNDERFLOW_EN: Enable the setting of pull_read_underflow by hardware. 0 - Underflow detection disabled. 1 - Underflow detection enabled. This bit is set using the OR mask register and cleared using the AND mask register.
3	RO	WO_AND	WO_OR	OCB_PIB_OCBCSR1_PUSH_WRITE_OVERFLOW_EN: Enable the setting of push_write_overflow by hardware. 0 - Overflow detection disabled. 1 - Overflow detection enabled. This bit is set using the OR mask register and cleared using the AND mask register.
4	RO	WO_AND	WO_OR	OCB_PIB_OCBCSR1_OCB_STREAM_MODE: Put the bridge channel in streaming mode with the behavior further defined by the setting of ocb_stream_type. 0 - Stream mode disabled. 1 - Stream mode enabled. This bit is set using the OR mask register and cleared using the AND mask register.
5	RO	WO_AND	WO_OR	OCB_PIB_OCBCSR1_OCB_STREAM_TYPE: Type of streaming enabled by ocb_stream_mode = 1 0 - Linear 1 - Circular for Linear type. The ocb_address field is incremented by 8 with each access to the OCB Data [n] Register. In Circular type, the address manipulation via access to OCB Stream [PushPull] Increment registers. This bit is set using the OR mask register and cleared using the AND mask register.
6:7	RO	WO_AND	WO_OR	OCB_PIB_OCBCSR1_SPARE0: Implemented but not used.
8	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR1_OCB_OCI_TIMEOUT: Indicates the MnTimeout signal on the OCI for the OCB Master was asserted to flag that no OCI slave acknowledged the request. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
9	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR1_OCB_OCI_READ_DATA_PARITY: Indicates the OCI read data parity was in error. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
10	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR1_OCB_OCI_SLAVE_ERROR: Indicates the SlvError signal on the OCI for the OCB Master was asserted. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
11	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR1_OCB_PIB_ADDR_PARITY_ERR: Indicates the PIB address parity was in error (PIB read or write operation). This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
12	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR1_OCB_PIB_DATA_PARITY_ERR: Indicates the PIB data parity was in error for a PIB write operation. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
13	RO	WO_AND	WO_OR	OCB_PIB_OCBCSR1_SPARE1: Implemented but not used.
14	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR1_OCB_FSM_ERR: Catastrophic state machine error. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
15	RO	WO_AND	WO_OR	OCB_PIB_OCBCSR1_SPARE2: Implemented but not used. Writes store the value. Reads return the last value written.





Register Name	<i>Writes To This Register Cause The Pull Queue To Be Reset</i>
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLCS1
Address	000000000006A211 (PIB) 0000000040051088 (OCI)
Attributes	Magic=true
Description	OCB0

Bits	PIB	OCI	Field Mnemonic: Description
0	RWX_WCLRPART	RWX_WCLRPART	OCB_OCI_OCBSLCS1_PULL_FULL: Reads indicate the Pull Queue is full condition Any write to this register clears this indicator and clears pull_write_ptr and pull_read_ptr to 0s. (this is a means for resetting the queue hardware) RWX_WCLRPART NOT_FULL=>0b0 FULL=>0b1
1	RWX_WSETPART	RWX_WSETPART	OCB_OCI_OCBSLCS1_PULL_EMPTY: Reads indicate the Pull Queue empty condition. Any write to this register sets this indicator and clears pull_write_ptr and pull_read_ptr to 0s. (This is a means for resetting the queue hardware.) RWX_WSETPART NOT_EMPTY=>0b0 EMPTY=>0b1
2:3	RW	RW	OCB_OCI_OCBSLCS1_SPARE: Implemented but not used Writes store the value. Reads return the last value written.
4:5	RW	RW	OCB_OCI_OCBSLCS1_PULL_INTR_ACTION_0_1: Pull Interrupt Action. This field controls the condition that asserts the pull interrupt signal for this channel to the OCB interrupt controller. 0b00 = Full (default upon hardware initialization) 0b01 = Non-Full 0b10 = Empty (the more useful firmware default) 0b11 = Not Empty

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Bits	PIB	OCI	Field Mnemonic: Description
6:10	RW	RW	OCB_OCI_OCBSLCS1_PULL_LENGTH: Pull Queue length in (pull_length + 1) * 8 bytes Value mapping: 0b00000: 8 bytes 0b00001: 16 bytes 0b00010: 24 bytes 0b00011: 32 bytes 0b00100: 40 bytes 0b00101: 48 bytes 0b00110: 56 bytes 0b00111: 64 bytes 0b01000: 72 bytes 0b01001: 80 bytes 0b01010: 88 bytes 0b01011: 96 bytes 0b01100: 104 bytes 0b01101: 112 bytes 0b01110: 120 bytes 0b01111: 128 bytes 0b10000: 136 bytes 0b10001: 144 bytes 0b10010: 152 bytes 0b10011: 160 bytes 0b10100: 168 bytes 0b10101: 176 bytes 0b10110: 184 bytes 0b10111: 192 bytes 0b11000: 200 bytes 0b11001: 208 bytes 0b11010: 216 bytes 0b11011: 224 bytes 0b11100: 232 bytes 0b11101: 240 bytes 0b11110: 248 bytes 0b11111: 256 bytes
11:12	RO	RO	Constant = 0b00
13:17	RWX_WCLRPART	RWX_WCLRPART	OCB_OCI_OCBSLCS1_PULL_WRITE_PTR: Pull write pointer. Reads indicate the current Pull queue write pointer in increments of 8 bytes. The actual address used is pull_oci_region pull_start + pull_write_ptr 00000. Writes to this field are ignored. Hardware performs all modifications. This field is cleared when writing to this register. ROX_WCLRPART
18:20	RO	RO	Constant = 0b000
21:25	RWX_WCLRPART	RWX_WCLRPART	OCB_OCI_OCBSLCS1_PULL_READ_PTR: Pull read pointer. Reads indicate the current Pull Queue read pointer in increments of 8 bytes. The actual address used is pull_oci_region pull_start + pull_write_ptr 00000. This field is cleared when writing to this register. ROX_WCLRPART
26:30	RO	RO	Constant = 0b00000
31	RW	RW	OCB_OCI_OCBSLCS1_PULL_ENABLE: Enables the Pull queue function. If disabled, PIB reads to OCB Data [n] Register to perform a pull results in an offline PIB error back to the PIB Master. Note: OCI Reads to OCB Stream Pull Increment [n] Register to cause incrementation are unaffected by the setting of this bit. Full and/or empty conditions can still arise to the OCC, even if this bit indicates disabled. DISABLED=>0b0 ENABLED=>0b1



Bits	PIB	OCI	Field Mnemonic: Description
32:63	RO	RO	Constant = 0b00000000000000000000000000000000 DISABLED=>0b0 ENABLED=>0b1

Register Name	<i>EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHBR1</i>
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHBR1
Address	000000000006A213 (PIB) 0000000040051098 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:1	RW	RW	OCB_OCI_OCBSHBR1_PUSH_OCI_REGION: Push OCI Region. Allowed values: 00 - PBA 11 - SRAM Others are reserved
2:28	RW	RW	OCB_OCI_OCBSHBR1_PUSH_START: Starting address of Push queue (8-byte alignment).
29:63	RO	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>Controls The Behavior Of Push Queue N</i>
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHCS1
Address	000000000006A214 (PIB) 00000000400510A0 (OCI)
Attributes	Magic=true
Description	Writes to this register cause the queue hardware to be reset.

Bits	PIB	OCI	Field Mnemonic: Description
0	RWX_WCLRPART	RWX_WCLRPART	OCB_OCI_OCBSHCS1_PUSH_FULL: Reads indicate the Push queue is full condition. A write to this register clears this indicator and clears push_write_ptr and push_read_ptr to 0s. (This is a means for resetting the queue hardware.) RWX_WCLR NOT_FULL=>0b0 FULL=>0b1
1	RWX_WSETPART	RWX_WSETPART	OCB_OCI_OCBSHCS1_PUSH_EMPTY: Reads indicate a Push queue empty condition. Any write to this register sets this indicator and clears push_write_ptr and push_read_ptr to 0s. (This is a means for resetting the queue hardware.) RWX_WSETPART NOT_EMPTY=>0b0 EMPTY=>0b1
2:3	RW	RW	OCB_OCI_OCBSHCS1_SPARE: Implemented but not used. Writes store the value. Reads return the last value written.

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Bits	PIB	OCI	Field Mnemonic: Description
4:5	RW	RW	OCB_OCI_OCBSHCS1_PUSH_INTR_ACTION_0_1: Push Interrupt Action. This field controls the condition that asserts the push interrupt signal for this channel to the OCB interrupt controller. b00 = Full (default on hardware initialization) b01 = Non-full b10 = Empty b11 = Not empty
6:10	RW	RW	OCB_OCI_OCBSHCS1_PUSH_LENGTH: Push Queue length in (push_length + 1) * 8 bytes. Value mapping: 0b00000: 8 bytes 0b00001: 16 bytes 0b00010: 24 bytes 0b00011: 32 bytes 0b00100: 40 bytes 0b00101: 48 bytes 0b00110: 56 bytes 0b00111: 64 bytes 0b01000: 72 bytes 0b01001: 80 bytes 0b01010: 88 bytes 0b01011: 96 bytes 0b01100: 104 bytes 0b01101: 112 bytes 0b01110: 120 bytes 0b01111: 128 bytes 0b10000: 136 bytes 0b10001: 144 bytes 0b10010: 152 bytes 0b10011: 160 bytes 0b10100: 168 bytes 0b10101: 176 bytes 0b10110: 184 bytes 0b10111: 192 bytes 0b11000: 200 bytes 0b11001: 208 bytes 0b11010: 216 bytes 0b11011: 224 bytes 0b11100: 232 bytes 0b11101: 240 bytes 0b11110: 248 bytes 0b11111: 256 bytes
11:12	RO	RO	Constant = 0b00
13:17	RWX_WCLRPART	RWX_WCLRPART	OCB_OCI_OCBSHCS1_PUSH_WRITE_PTR: Push write pointer. Reads indicate the current Push queue write pointer in increments of 8 bytes. The actual address used is push_oci_region push_start + push_write_ptr 00000. Writes to this field are ignored. Hardware performs all modifications. This field is cleared upon a write to this register. ROX_WCLRPART
18:20	RO	RO	Constant = 0b000
21:25	RWX_WCLRPART	RWX_WCLRPART	OCB_OCI_OCBSHCS1_PUSH_READ_PTR: Push read pointer. Reads indicate the current Push queue read pointer in increments of 8 bytes. The actual address used is push_oci_region push_start + push_read_ptr 00000. This field is cleared on a write to this register. ROX_WCLRPART
26:30	RO	RO	Constant = 0b00000

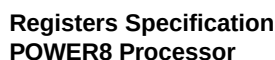


Bits	PIB	OCI	Field Mnemonic: Description
31	RW	RW	OCB_OCI_OCBSHCS1_PUSH_ENABLE: Enables the Push queue function. If disabled, PIB Writes to OCB Data [n] Register to perform a push results in an offline PIB error back to the PIB Master. Note: OCI Writes to OCB Stream Push Increment [n] Register to cause incrementation are unaffected by the setting of this bit. Full and/or empty conditions can still arise to the OCC even if this bit indicates disabled. DISABLED=>0b0 ENABLED=>0b1
32:63	RO	RO	Constant = 0b00000000000000000000000000000000 DISABLED=>0b0 ENABLED=>0b1

Register Name	Indicates Errors That Occur In An Indirect Channel When In A Streaming Mode (Linear Or Circular)
Mnemonic	EH.TPCHIP.OCC.OCI.OCB_OCI_OCBSES1
Address	000000000006A216 (PIB) 00000000400510B0 (OCI)
Attributes	Magic=true
Description	Indicates errors that occur in an indirect channel when in a streaming mode (linear or circular)

[illegible]

Register Name	<i>OCI Accessible Register Defines Control Bits that Pertain to an Entire Indirect Channel [Indirect, Linear (including Linear Window)], Circular Pull and Circular Push</i>
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBICR1
Address	000000000006A217 (PIB) 00000000400510B8 (OCI)
Attributes	Magic=true
Description	This OCI Accessible Register defines control bits that pertain to an entire indirect channel [indirect, linear (including linear window)], circular pull, and circular push.

[illegible]

Register Name	OCI Accessible Register - Controls the Linear Write Window Access Facility
Mnemonic	EH.TPCHIP.OCC.OCI.OCB_OCI_OCBLWCR1
Address	000000000006A218 (PIB) 00000000400510C0 (OCI)
Attributes	Magic=true
Description	This OCI Accessible Register controls the Linear Write Window Access Facility

Bits	PIB	OCI	Field Mnemonic: Description
0	RW	RW	OCB_OCI_OCBLWCR1_LINEAR_WINDOW_ENABLE: Linear Window Enable. 0: Window facility disabled. 1: Window facility enabled. If OCBCSR[n].ocb_stream_type = linear, Linear Window BAR and Mask are valid and operations are to be honored. sc_resp codes are the same as for the OCB indirect facility to reflect the status of the OCI operation.
1:3	RW	RW	OCB_OCI_OCBLWCR1_SPARE_0: Implemented but not used Writes store the value. Reads return the last value written.
4:19	RW	RW	OCB_OCI_OCBLWCR1_LINEAR_WINDOW_BAR: Linear Window Base Address Register Defines OCI address(13:28) - 16 bits to define the starting offset within the region addressed
20:31	RW	RW	OCB_OCI_OCBLWCR1_LINEAR_WINDOW_MASK: Linear Window Address Mask Register Masks OCI address (17:28) - 12 bits to define the window size
32:63	RO	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>OCI Accessible Register (that Defines the Placement of the SRAM Base Address For Use by the OCB Linear Write Window Function of the Indirect Channel)</i>
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWSBR1
Address	000000000006A21C (PIB) 00000000400510E0 (OCI)
Attributes	Magic=true
Description	This OCI Accessible Register defines the placement of the SRAM Base Address for use by the OCB Linear Write Window Function of the Indirect Channel

[illegible]

Register Name	PIB Accessible Register Captures OCI Address To Be Accessed
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBAR2
Address	000000000006B050 (PIB)
Attributes	Magic=true
Description	This PIB Accessible Register captures the OCI Address that is desired to be accessed.

Bits	PIB	Field Mnemonic: Description
0:1	RW	OCB_PIB_OCBAR2_OCI_REGION: OCI Address Space Region 00 – Processor Bus 01 – Registers Reserved (register space access not supported) 10 - Reserved 11 - SRAM
2:28	RW	OCB_PIB_OCBAR2_OCB_ADDRESS: Address of 8-byte quantity the OCI for this channel. Field contents depends on accessed oci_region Registers 2:13 - Reserved 13:15 - OCI Slave 16:28 - Register # Processor Bus 2:11 - Maskable Alignment 12:28 - Offset SRAM 2:13 - SRAM Tank BAR (FFs) 14:28 - Offset
29:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>PIB Accessible Register Controls Function of the OCB Channel and Provides Status of It</i>
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBCSR2
Address	000000000006B051 (PIB) 000000000006B052 (PIB1) 000000000006B053 (PIB2)
Attributes	Magic=true
Description	This PIB Accessible Register controls the function of the OCB Channel and provides Status of it.

Bits	PIB	PIB1	PIB2	Field Mnemonic: Description
0	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR2_PULL_READ_UNDERFLOW: Pull Queue Read Underflow Underflow is defined as a read to the OCB Data [n] Register and the pull_empty facility is already set. This bit is cleared only by a firmware write of this bit to 0.Writes store the value. UNDERFLOW_NOT_DETECTED=>0b0 UNDERFLOW_DETECTED=>0b1

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Bits	PIB	PIB1	PIB2	Field Mnemonic: Description
1	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR2_PUSH_WRITE_OVERFLOW: Push Queue Write Overflow Overflow is defined as a store to the OCB Data [n] Register and the push_full facility is already set. This bit is cleared only by a firmware write of this bit to 0. OVERFLOW_NOT_DETECTED=>0b0 OVERFLOW_DETECTED=>0b1
2	RO	WO_AND	WO_OR	OCB_PIB_OCBCSR2_PULL_READ_UNDERFLOW_EN: Enable the setting of pull_read_underflow by hardware. 0 - Underflow detection disabled 1 - Underflow detection enabled This bit is set using the OR mask register and cleared using the AND mask register.
3	RO	WO_AND	WO_OR	OCB_PIB_OCBCSR2_PUSH_WRITE_OVERFLOW_EN: Enable the setting of push_write_overflow by hardware. 0 - Overflow detection disabled 1 - Overflow detection enabled This bit is set using the OR mask register and cleared using the AND mask register.
4	RO	WO_AND	WO_OR	OCB_PIB_OCBCSR2_OCB_STREAM_MODE: Put the bridge channel in streaming mode with the behavior further defined by the setting of ocb_stream_type 0 - Stream Mode Disabled 1 - Stream Mode Enabled This bit is set using the OR mask register and cleared using the AND mask register.
5	RO	WO_AND	WO_OR	OCB_PIB_OCBCSR2_OCB_STREAM_TYPE: Type of streaming enabled by ocb_stream_mode = 1 0 - Linear 1 - Circular For Linear type, the ocb_address field is incremented by 8 with each access to the OCB Data [n] Register. In Circular type, the address manipulation via access to OCB Stream [PushPull] Increment registers This bit is set using the OR mask register and cleared using the AND mask register.
6:7	RO	WO_AND	WO_OR	OCB_PIB_OCBCSR2_SPARE0: Implemented but not used
8	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR2_OCB_OCI_TIMEOUT: Indicates the MnTimeout signal on the OCI for the OCB Master was asserted to flag that no OCI slave acknowledged the request. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
9	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR2_OCB_OCI_READ_DATA_PARITY: Indicates the OCI read data parity was in error This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
10	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR2_OCB_OCI_SLAVE_ERROR: Indicates the SlvError signal on the OCI for the OCB Master was asserted. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
11	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR2_OCB_PIB_ADDR_PARITY_ERR: Indicates the PIB address parity was in error (PIB read or write operation) This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
12	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR2_OCB_PIB_DATA_PARITY_ERR: Indicates the PIB data parity was in error for a PIB write operation This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
13	RO	WO_AND	WO_OR	OCB_PIB_OCBCSR2_SPARE1: Implemented but not used
14	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR2_OCB_FSM_ERR: Catastrophic state machine error This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.



Bits	PIB	PIB1	PIB2	Field Mnemonic: Description
15	RO	WO_AND	WO_OR	OCB_PIB_OCBCSR2_SPARE2: Implemented but not used Writes store the value. Reads return the last value written.
16:63	RO	RO	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>PIB Accessible Register that Indicates the OCI Address of a Channel Operation That Detected the First Error</i>		
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBESR2		
Address	000000000006B054 (PIB)		
Attributes			
Description	This PIB Accessible Register indicates the OCI Address of a channel operation that detected the first error. See OCB Control/Status [n] Register for the specific error(s) detected. Set and Locked by hardware, Write to clear and Unlock.		

Bits	PIB	Field Mnemonic: Description
0:31	RWX_WCLRR EG	OCB_PIB_OCBESR2_OCB_ERROR_ADDR: OCI address being accessed when the first channel error is detected. This register is cleared upon writing any value.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>PIB Accessible Register Captures PIB Data Written on the OCI or OCI Data Read Returned Without Errors From The OCI Address to be Accessed</i>		
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBDR2		
Address	000000000006B055 (PIB)		
Attributes			
Description	This PIB Accessible Register captures the PIB data to be written on the OCI or the OCI data read returned without errors from the OCI address that is desired to be accessed		

Bits	PIB	Field Mnemonic: Description
0:63	WOX	OCB_PIB_OCBDR2_OCB_DATA: Data to/from OCI for this channel

Register Name	<i>EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLBR2</i>		
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLBR2		
Address	000000000006A220 (PIB) 0000000040051100 (OCI)		
Attributes			
Description			

Bits	PIB	OCI	Field Mnemonic: Description
0:1	RW	RW	OCB_OCI_OCBSLBR2_PULL_OCI_REGION: Pull OCI Region allowed values: 00 - PBA 11 - SRAM Others are reserved
2:28	RW	RW	OCB_OCI_OCBSLBR2_PULL_START: Starting address of Pull Queue (8-byte alignment)
29:63	RO	RO	Constant = 0b00000000000000000000000000000000

Registers Specification

POWER8 Processor

Register Name		<i>Writes To This Register Cause The Pull Queue To Be Reset</i>	
Mnemonic		EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSLCS2	
Address		000000000006A221 (PIB) 0000000040051108 (OCI)	
Attributes		Magic=true	
Description		OCB0	

Bits	PIB	OCI	Field Mnemonic: Description
0	RWX_WCLRPART	RWX_WCLRPART	OCB_OCI_OCBSLCS2_PULL_FULL: Reads indicate the Pull Queue is full condition Any write to this register clears this indicator and clears pull_write_ptr and pull_read_ptr to 0s. (this is a means for resetting the queue hardware) RWX_WCLRPART NOT_FULL=>0b0 FULL=>0b1
1	RWX_WSETPART	RWX_WSETPART	OCB_OCI_OCBSLCS2_PULL_EMPTY: Reads indicate the Pull Queue empty condition Any write to this register sets this indicator and clears pull_write_ptr and pull_read_ptr to 0s. (this is a means for resetting the queue hardware) RWX_WSETPART NOT_EMPTY=>0b0 EMPTY=>0b1
2:3	RW	RW	OCB_OCI_OCBSLCS2_SPARE: Implemented but not used Writes store the value. Reads return the last value written.
4:5	RW	RW	OCB_OCI_OCBSLCS2_PULL_INTR_ACTION_0_1: Pull Interrupt Action. This field controls the condition that asserts the pull interrupt signal for this channel to the OCB interrupt controller. b00 = Full (default upon hardware initialization) b01 = Non-full b10 = Empty (the more useful firmware default) b11 = Not empty

Bits	PIB	OCI	Field Mnemonic: Description
6:10	RW	RW	OCB_OCI_OCBSLCS2_PULL_LENGTH: Pull Queue length in (pull_length + 1) * 8 bytes. Value mapping: 0b00000: 8 bytes 0b00001: 16 bytes 0b00010: 24 bytes 0b00011: 32 bytes 0b00100: 40 bytes 0b00101: 48 bytes 0b00110: 56 bytes 0b00111: 64 bytes 0b01000: 72 bytes 0b01001: 80 bytes 0b01010: 88 bytes 0b01011: 96 bytes 0b01100: 104 bytes 0b01101: 112 bytes 0b01110: 120 bytes 0b01111: 128 bytes 0b10000: 136 bytes 0b10001: 144 bytes 0b10010: 152 bytes 0b10011: 160 bytes 0b10100: 168 bytes 0b10101: 176 bytes 0b10110: 184 bytes 0b10111: 192 bytes 0b11000: 200 bytes 0b11001: 208 bytes 0b11010: 216 bytes 0b11011: 224 bytes 0b11100: 232 bytes 0b11101: 240 bytes 0b11110: 248 bytes 0b11111: 256 bytes
11:12	RO	RO	Constant = 0b00
13:17	RWX_WCLRPART	RWX_WCLRPART	OCB_OCI_OCBSLCS2_PULL_WRITE_PTR: Pull write pointer Reads indicate the current Pull Queue write pointer in increments of 8 bytes. The actual address used is pull_oci_region pull_start + pull_write_ptr 00000. Writes to this field are ignored. Hardware performs all modifications. This field is cleared upon a write to this register. ROX_WCLRPART
18:20	RO	RO	Constant = 0b000
21:25	RWX_WCLRPART	RWX_WCLRPART	OCB_OCI_OCBSLCS2_PULL_READ_PTR: Pull read pointer Reads indicate the current Pull Queue read pointer in increments of 8 bytes. The actual address used is pull_oci_region pull_start + pull_write_ptr 00000. This field is cleared upon a write to this register. ROX_WCLRPART
26:30	RO	RO	Constant = 0b00000
31	RW	RW	OCB_OCI_OCBSLCS2_PULL_ENABLE: Enables the Pull Queue function If Disabled, PIB Reads to OCB Data [n] Register to perform a pull will result in an offline PIB error back to the PIB Master. Note: OCI Reads to OCB Stream Pull Increment [n] Register to cause incrementation are unaffected by the setting of this bit. Full and/or empty conditions may still arise to the OCC even if this bit indicates disabled. DISABLED=>0b0 ENABLED=>0b1

Registers Specification

POWER8 Processor

Bits	PIB	OCI	Field Mnemonic: Description
32:63	RO	RO	Constant = 0b00000000000000000000000000000000 DISABLED=>0b0 ENABLED=>0b1

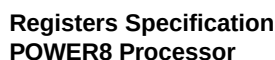
Register Name	<i>EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHBR2</i>
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHBR2
Address	000000000006A223 (PIB) 0000000040051118 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:1	RW	RW	OCB_OCI_OCBSHBR2_PUSH_OCI_REGION: Push OCI Region Allowed values: 00 - PBA 11 - SRAM Others are reserved
2:28	RW	RW	OCB_OCI_OCBSHBR2_PUSH_START: Starting address of Push queue (8-byte alignment).
29:63	RO	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>Controls The Behavior Of Push Queue N</i>
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBSHCS2
Address	000000000006A224 (PIB) 0000000040051120 (OCI)
Attributes	Magic=true
Description	Writes to this register cause the queue hardware to be reset.

Bits	PIB	OCI	Field Mnemonic: Description
0	RWX_WCLRPART	RWX_WCLRPART	OCB_OCI_OCBSHCS2_PUSH_FULL: Reads indicate the Push Queue is full condition Any write to this register clears this indicator and clears push_write_ptr and push_read_ptr to 0s. (this is a means for resetting the queue hardware) RWX_WCLR NOT_FULL=>0b0 FULL=>0b1
1	RWX_WSETPART	RWX_WSETPART	OCB_OCI_OCBSHCS2_PUSH_EMPTY: Read indicate the Push Queue empty condition Any write to this register sets this indicator and clears push_write_ptr and push_read_ptr to 0s. (this is a means for resetting the queue hardware) RWX_WSETPART NOT_EMPTY=>0b0 EMPTY=>0b1
2:3	RW	RW	OCB_OCI_OCBSHCS2_SPARE: Implemented but not used. Writes store the value. Reads return the last value written.

Bits	PIB	OCI	Field Mnemonic: Description
4:5	RW	RW	OCB_OCI_OCBSHCS2_PUSH_INTR_ACTION_0_1: Push Interrupt Action. This field controls the condition that asserts the push interrupt signal for this channel to the OCB interrupt controller. b00 = Full (default upon hardware initialization) b01 = Non-full b10 = Empty b11 = Not empty
6:10	RW	RW	OCB_OCI_OCBSHCS2_PUSH_LENGTH: Push queue length in (push_length + 1) * 8 bytes. Value mapping: 0b00000: 8 bytes 0b00001: 16 bytes 0b00010: 24 bytes 0b00011: 32 bytes 0b00100: 40 bytes 0b00101: 48 bytes 0b00110: 56 bytes 0b00111: 64 bytes 0b01000: 72 bytes 0b01001: 80 bytes 0b01010: 88 bytes 0b01011: 96 bytes 0b01100: 104 bytes 0b01101: 112 bytes 0b01110: 120 bytes 0b01111: 128 bytes 0b10000: 136 bytes 0b10001: 144 bytes 0b10010: 152 bytes 0b10011: 160 bytes 0b10100: 168 bytes 0b10101: 176 bytes 0b10110: 184 bytes 0b10111: 192 bytes 0b11000: 200 bytes 0b11001: 208 bytes 0b11010: 216 bytes 0b11011: 224 bytes 0b11100: 232 bytes 0b11101: 240 bytes 0b11110: 248 bytes 0b11111: 256 bytes
11:12	RO	RO	Constant = 0b00
13:17	RWX_WCLRPART	RWX_WCLRPART	OCB_OCI_OCBSHCS2_PUSH_WRITE_PTR: Push write pointer. Reads indicate the current Push queue write pointer in increments of 8 bytes. The actual address used is push_oci_region push_start + push_write_ptr 00000. Writes to this field are ignored. Hardware performs all modifications. This field is cleared on a write to this register. ROX_WCLRPART
18:20	RO	RO	Constant = 0b000
21:25	RWX_WCLRPART	RWX_WCLRPART	OCB_OCI_OCBSHCS2_PUSH_READ_PTR: Push read pointer Reads indicate the current Push queue read pointer in increments of 8 bytes. The actual address used is push_oci_region push_start + push_read_ptr 00000. This field is cleared on a write to this register. ROX_WCLRPART
26:30	RO	RO	Constant = 0b00000



Register Name	Indicates Errors That Occur in an Indirect Channel When in a Streaming Mode (Linear or Circular)
Mnemonic	EH.TPCHIP.OCC.OCI.OCB_OCI_OCBSES2
Address	000000000006A226 (PIB) 0000000040051130 (OCI)
Attributes	Magic=true
Description	

[illegible]

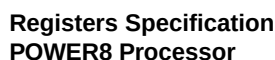
Register Name	<i>OCI Accessible Register Defines Control Bits That Pertain To An Entire Indirect Channel (Indirect, Linear (including Linear Window), Circular Pull, and Circular Push</i>
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBICR2
Address	000000000006A227 (PIB) 0000000040051138 (OCI)
Attributes	Magic=true
Description	This OCI Accessible Register defines control bits that pertain to an entire indirect Channel (Indirect, Linear (including Linear Window), Circular Pull, and Circular Push.

[illegible]

Register Name	<i>OCI Accessible Register: Controls Linear Write Window Access Facility</i>
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWCR2
Address	000000000006A228 (PIB) 0000000040051140 (OCI)
Attributes	Magic=true
Description	This OCI Accessible Register controls the Linear Write Window Access Facility

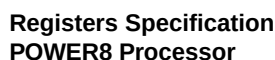
Bits	PIB	OCI	Field Mnemonic: Description
0	RW	RW	OCB_OCI_OCBLWCR2_LINEAR_WINDOW_ENABLE: Linear Window Enable 0: Window facility disabled. 1: Window facility enabled. If OCBCSR[n].ocb_stream_type = linear, Linear Window BAR and Mask are valid and operations are to be honored. sc_resp codes are the same as for the OCB indirect facility to reflect the status of the OCI operation.
1:3	RW	RW	OCB_OCI_OCBLWCR2_SPARE_0: Implemented but not used. Writes store the value. Reads return the last value written.
4:19	RW	RW	OCB_OCI_OCBLWCR2_LINEAR_WINDOW_BAR: Linear Window Base Address Register. Defines OCI address(13:28) - 16 bits to define the starting offset within the region addressed.
20:31	RW	RW	OCB_OCI_OCBLWCR2_LINEAR_WINDOW_MASK: Linear Window Address Mask. Register masks OCI address (17:28) - 12 bits to define the window size.
32:63	RO	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>OCI Accessible Register Defines Placement of the SRAM Base Address For Use by OCB Linear Write Window Function of the Indirect Channel</i>
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCBLWSBR2
Address	000000000006A22C (PIB) 0000000040051160 (OCI)
Attributes	Magic=true
Description	This OCI Accessible Register That Defines The Placement of the SRAM Base Address For Use By The OCB Linear Write Window Function of the Indirect Channel



Bits	PIB	PIB1	PIB2	Field Mnemonic: Description
0	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR3_PULL_READ_UNDERFLOW: Pull Queue Read Underflow Underflow is defined as a read to the OCB Data [n] Register and the pull_empty facility is already set. This bit is cleared only by a firmware write of this bit to 0.Writes store the value. UNDERFLOW_NOT_DETECTED=>0b0 UNDERFLOW_DETECTED=>0b1

Bits	PIB	PIB1	PIB2	Field Mnemonic: Description
1	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR3_PUSH_WRITE_OVERFLOW: Push Queue Write Overflow Overflow is defined as a store to the OCB Data [n] Register and the push_full facility is already set. This bit is cleared only by a firmware write of this bit to 0. OVERFLOW_NOT_DETECTED=>0b0 OVERFLOW_DETECTED=>0b1
2	RO	WO_AND	WO_OR	OCB_PIB_OCBCSR3_PULL_READ_UNDERFLOW_EN: Enable the setting of pull_read_underflow by hardware. 0 - Underflow detection disabled 1 - Underflow detection enabled This bit is set using the OR mask register and cleared using the AND mask register.
3	RO	WO_AND	WO_OR	OCB_PIB_OCBCSR3_PUSH_WRITE_OVERFLOW_EN: Enable the setting of push_write_overflow by hardware. 0 - Overflow detection disabled 1 - Overflow detection enabled This bit is set using the OR mask register and cleared using the AND mask register.
4	RO	WO_AND	WO_OR	OCB_PIB_OCBCSR3_OCB_STREAM_MODE: Put the bridge channel in streaming mode with the behavior further defined by the setting of ocb_stream_type 0 - Stream Mode Disabled 1 - Stream Mode Enabled This bit is set using the OR mask register and cleared using the AND mask register.
5	RO	WO_AND	WO_OR	OCB_PIB_OCBCSR3_OCB_STREAM_TYPE: Type of streaming enabled by ocb_stream_mode = 1 0 - Linear 1 - Circular For Linear type, the ocb_address field is incremented by 8 with each access to the OCB Data [n] Register. In Circular type, the address manipulation via access to OCB Stream [PushPull] Increment registers This bit is set using the OR mask register and cleared using the AND mask register.
6:7	RO	WO_AND	WO_OR	OCB_PIB_OCBCSR3_SPARE0: Implemented but not used
8	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR3_OCB_OCI_TIMEOUT: Indicates the MnTimeout signal on the OCI for the OCB Master was asserted to flag that no OCI slave acknowledged the request. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
9	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR3_OCB_OCI_READ_DATA_PARITY: Indicates the OCI read data parity was in error This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
10	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR3_OCB_OCI_SLAVE_ERROR: Indicates the SlvError signal on the OCI for the OCB Master was asserted. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
11	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR3_OCB_PIB_ADDR_PARITY_ERR: Indicates the PIB address parity was in error (PIB read or write operation) This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
12	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR3_OCB_PIB_DATA_PARITY_ERR: Indicates the PIB data parity was in error for a PIB write operation This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
13	RO	WO_AND	WO_OR	OCB_PIB_OCBCSR3_SPARE1: Implemented but not used
14	ROX	WOX_AND	WOX_OR	OCB_PIB_OCBCSR3_OCB_FSM_ERR: Catastrophic state machine error This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.

[illegible]

Register Name	<i>PIB Accessible Register Indicates OCI Address of a Channel Operation That Detected the First Error</i>
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_PIB_OCBESR3
Address	000000000006B074 (PIB)
Attributes	
Description	This PIB Accessible Register that indicates the OCI address of a channel operation that detected the first error. See OCB Control/Status [n] Register for the specific error(s) detected. Set and Locked by hardware, Write to clear and Unlock.

Bits	PIB	Field Mnemonic: Description
0:31	RWX_WCLRR EG	OCB_PIB_OCBESR3_OCB_ERROR_ADDR: OCI address being accessed when the first channel error is detected. This register is cleared upon writing any value.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>PIB Accessible Register Captures PIB Data to be Written On The OCI or the OCI Data Read Returned Without Errors From the OCI Address that is to Be Accessed</i>
Mnemonic	EH.TPCHIP.OCC.OCI.OCB_OCB_PIB_OCBDR3
Address	000000000006B075 (PIB)
Attributes	
Description	This PIB Accessible Register captures the PIB data to be Written on the OCI or the OCI data read returned without errors from the OCI Address that is desired to be accessed.

Bits	PIB	Field Mnemonic: Description
0:63	WOX	OCB PIB OCBDR3 OCB DATA: Data to/from OCI for this channel

Register Name	<i>OCC Local Fault Isolation Register</i>
Mnemonic	EH.TPCHIP.OCC.OCI.SCOM.OCC_SCOM_OCCLFIR
Address	0000000001010800 (SCOM) 0000000001010801 (SCOM1) 0000000001010802 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
2	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIR_OCC_FW2: Input tied to 0. Used by OCC Firmware to produce an attention to the FSP. FW Convention: (Potential) eVRM Fault
3	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIR_OCC_FW3: Input tied to 0. Used by OCC Firmware to produce an attention to the FSP. FW Convention: Spare
4	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_PMC_PORE_SW_MALF: PMC PORE-SW Timeout Error (malfunction alert)
5	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_PMC_OCC_HB_MALF: PMC OCC Heartbeat Error (malfunction alert)
6	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_PORE_GPE0_FATAL_ERR: PORE-GPE Thread 0 Fatal Error (recoverable (product) - chip is going to Safe Mode)
7	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_PORE_GPE1_FATAL_ERR: PORE-GPE Thread 1 Fatal Error (recoverable (product) - logging) -> handled by OCC Interrupt
8	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_OCB_ERROR: OCB Error (recoverable error)
9	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_SRT_UE: SRAM Uncorrectable Error (recoverable error) Note: this being on will also have either a srt_read_error or srt_write_error on as well as these each have the UE error included. UE is broken out specifically to allow for array faster characterization.
10	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_SRT_CE: SRAM Correctable Error (masked (product); recoverable error (mfg))
11	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_SRT_READ_ERROR: SRAM Read Error - asserts if a read operation and any of the following: SRAM Tank Address Parity error; SRAM Uncorrectable error
12	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_SRT_WRITE_ERROR: SRAM Read Error - asserts if a read operation and any of the following: SRAM Tank Address Parity error; if <8-byte write (requiring a read, modify, write operation), then (SRAM Tank Byte Enable Parity error; SRAM Write Data Parity error; SRAM Uncorrectable error).
13	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_SRT_DATAOUT_PERR: Indicates a parity error was detected by the SRAM controller on the read data coming from the tanks.
14	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_SRT_OCI_WRITE_DATA_PARITY: Indicates a OCI write data parity error by the SRAM controller.
15	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_SRT_OCI_BE_PARITY_ERR: Indicates an OCI byte enable parity error was detected by the SRAM controller
16	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_SRT_OCI_ADDR_PARITY_ERR: Indicates an OCI address parity error was detected by the SRAM controller.
17	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_PORE_SW_ERROR_ERR: PORE-SW Error [masked (product)]
18	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_PORE_GPE0_ERROR_ERR: PORE-GPE Thread 0 Error [masked (product) -> handled by OCC Interrupt]
19	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_PORE_GPE1_ERROR_ERR: PORE-GPE Thread 1 Error [masked (product) -> handled by OCC Interrupt]
20	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_EXTERNAL_TRAP: External Trigger pin active [recoverable (product)]
21	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_PPC405_CORE_RESET: PPC405 Core Reset Output asserted.

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
22	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_PPC405_CHIP_RESET: PPC405 Chip Reset Output asserted.
23	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_PPC405_SYSTEM_RESET: PPC405 System Reset Output asserted.
24	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_PPC405_DBGMSRWE: PPC405 Wait State asserted.
25	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_PPC405_DBGSTOPACK: PPC405 Stop Ack output asserted (recoverable -> logging). Process stopped execution.
26	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_OCB_DB_OCI_TIMEOUT: Indicates the MnTimeout signal on the OCI for the OCB Master was asserted to flag that no OCI slave acknowledged the direct bridge request. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
27	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_OCB_DB_OCI_READ_DATA_PARITY: Indicates a OCI read data parity error for the direct bridge operation This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
28	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_OCB_DB_OCI_SLAVE_ERROR: Indicates the SlvError signal on the OCI for the OCB Master was asserted. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
29	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_OCB_PIB_ADDR_PARITY_ERR: Indicates a PIB address parity error was detected (PIB read or write operation). Note: may be set for either direct bridge or indirect channel operations. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
30	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_OCB_DB_PIB_DATA_PARITY_ERR: Indicates the PIB data parity was in error for a PIB write operation to a direct bridge address. Note: write data parity errors to an indirect bridge address are captured in the the OCB Control Status [n] Register for the addressed channel. This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
31	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_OCB_IDC0_ERROR: Indirect Channel 0 Error. See OCB ControlStatus 0 Register for the reason.
32	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_OCB_IDC1_ERROR: Indirect Channel 1 Error. See OCB ControlStatus 1 Register for the reason.
33	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_OCB_IDC2_ERROR: Indirect Channel 2 Error. See OCB ControlStatus 2 Register for the reason.
34	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_OCB_IDC3_ERROR: Indirect Channel 3 Error. See OCB ControlStatus 2 Register for the reasonCatastrophic direct bridge state machine error This bit is set by hardware under normal operations but can be forced using the OR mask register. This bit can be cleared using the AND mask register.
35	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_SRT_FSM_ERR: Indicates an fsm error in the read or write machines of the SRAM controller.
36	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_JTAGACC_ERR: JTAG accelerator error. See OJSTAT register for reason.
37	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_SPARE_ERR_37: Spare error.
38	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_C405_ECC_UE: PPC405 cache UE.
39	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_C405_ECC_CE: PPC405 cache CE.



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
40	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_C405_OCI_MACHINECHECK: PPC405 Machine Check
41	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_SRAM_SPARE_DIRECT_ERROR0: SRAM spare direct error.
42	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_SRAM_SPARE_DIRECT_ERROR1: SRAM spare direct error.
43	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_SRAM_SPARE_DIRECT_ERROR2: SRAM spare direct error.
44	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_SRAM_SPARE_DIRECT_ERROR3: SRAM spare direct error.
45	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_SLW_OCISLV_ERR: Indicates OCI slave error in SLW PORE.
46	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_GPE_OCISLV_ERR: Indicates OCI slave error in GPE PORE.
47	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_OCB_OCISLV_ERR: Indicates OCI slave error in OCB.
48	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_C405ICU_M_TIMEOUT: Indicates PPC405 ICU received timeout on PLB request.
49	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_C405DCU_M_TIMEOUT: Indicates PPC405 DCU received timeout on PLB request.
50:61	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIR_SPARE_FIR: Implemented but not used.
62	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_FIR_PARITY_ERR_DUP: Internal fir parity error duplicate (same as bit 63).
63	RWX	WOX_AND	WOX_OR	OCC_SCOM_OCCLFIR_FIR_PARITY_ERR: Internal fir parity error.

Register Name	OCC Local Fault Isolation Mask Register
Mnemonic	EH.TPCHIP.OCC.OCI.SC.COM.OCC_SCOM_OCCLFIRMASK
Address	0000000001010803 (SCOM) 0000000001010804 (SCOM1) 0000000001010805 (SCOM2)
Attributes	
Description	OCC Local Fault Isolation Mask Register (Action0, Action1, Mask) = Action Select (0,0,x) = No Error Reported (0,1,0) = Recoverable Error (1,0,0) = Checkstop Error (1,1,0) = Local Core Checkstop (x,x,1) = MASKED

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_OCC_FW0_MASK: occ_fw0_mask
1	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_OCC_FW1_MASK: occ_fw1_mask
2	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_OCC_FW2_MASK: occ_fw2_mask
3	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_OCC_FW3_MASK: occ_fw3_mask
4	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_PMC_PORE_SW_MALF_MASK: pmc_pore_sw_malf_mask
5	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_PMC_OCC_HB_MALF_MASK: pmc_occ_hb_malf_mask
6	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_PORE_GPE0_FATAL_ERR_MASK: pore_gpe0_fatal_err_mask

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
7	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_PORE_GPE1_FATAL_ERR_MASK: pore_gpe1_fatal_err_mask
8	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_OCB_ERROR_MASK: ocb_error_mask
9	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SRT_UE_MASK: srt_ue_mask
10	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SRT_CE_MASK: srt_ce_mask
11	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SRT_READ_ERROR_MASK: srt_read_error_mask
12	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SRT_WRITE_ERROR_MASK: srt_write_error_mask
13	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SRT_DATAOUT_PERR_MASK: srt_dataout_perr_mask
14	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SRT_OCI_WRITE_DATA_PARITY_MASK: srt_oci_write_data_parity_mask
15	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SRT_OCI_BE_PARITY_ERR_MASK: srt_oci_be_parity_err_mask
16	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SRT_OCI_ADDR_PARITY_ERR_MASK: srt_oci_addr_parity_err_mask
17	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_PORE_SW_ERROR_ERR_MASK: pore_sw_error_err_mask
18	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_PORE_GPE0_ERROR_ERR_MASK: pore_gpe0_error_err_mask
19	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_PORE_GPE1_ERROR_ERR_MASK: pore_gpe1_error_err_mask
20	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_EXTERNAL_TRAP_MASK: external_trap_mask
21	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_PPC405_CORE_RESET_MASK: ppc405_core_reset_mask
22	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_PPC405_CHIP_RESET_MASK: ppc405_chip_reset_mask
23	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_PPC405_SYSTEM_RESET_MASK: ppc405_system_reset_mask
24	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_PPC405_DBGMSRWE_MASK: ppc405_dbgmsrwe_mask
25	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_PPC405_DBGSTOPACK_MASK: ppc405_dbgstopack_mask
26	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_OCB_DB_OCI_TIMEOUT_MASK: ocb_db_oci_timeout_mask
27	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_OCB_DB_OCI_READ_DATA_PARITY_MAS SK: ocb_db_oci_read_data_parity_mask
28	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_OCB_DB_OCI_SLAVE_ERROR_MASK: ocb_db_oci_slave_error_mask
29	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_OCB_PIB_ADDR_PARITY_ERR_MASK: ocb_pib_addr_parity_err_mask
30	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_OCB_DB_PIB_DATA_PARITY_ERR_MAS K: ocb_db_pib_data_parity_err_mask
31	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_OCB_IDC0_ERROR_MASK: ocb_idc0_error_mask



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
32	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_OCB_IDC1_ERROR_MASK: ocb_idc1_error_mask
33	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_OCB_IDC2_ERROR_MASK: ocb_idc2_error_mask
34	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_OCB_IDC3_ERROR_MASK: ocb_idc3_error_mask
35	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SRT_FSM_ERR_MASK: srt_fsm_err_mask
36	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_JTAGACC_ERR_MASK: jtagacc_err_mask
37	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SPARE_ERR_37_MASK: spare_err_37_mask
38	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_C405_ECC_UE_MASK: c405_ecc_ue_mask
39	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_C405_ECC_CE_MASK: c405_ecc_ce_mask
40	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_C405_OCI_MACHINECHECK_MASK: c405_oci_machinecheck_mask
41	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SRAM_SPARE_DIRECT_ERROR0_MASK: sram_spare_direct_error0_mask
42	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SRAM_SPARE_DIRECT_ERROR1_MASK: sram_spare_direct_error1_mask
43	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SRAM_SPARE_DIRECT_ERROR2_MASK: sram_spare_direct_error2_mask
44	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SRAM_SPARE_DIRECT_ERROR3_MASK: sram_spare_direct_error3_mask
45	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SLW_OCISLV_ERR_MASK: slw_ocislv_err_mask
46	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_GPE_OCISLV_ERR_MASK: gpe_ocislv_err_mask
47	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_OCB_OCISLV_ERR_MASK: ocb_ocislv_err_mask
48	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_C405ICU_M_TIMEOUT_MASK: c405icu_m_timeout_mask
49	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_C405DCU_M_TIMEOUT_MASK: c405dcu_m_timeout_mask
50:61	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_SPARE_FIR_MASK: spare_fir_mask
62	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_FIR_PARITY_ERR_DUP_MASK: fir_parity_err_dup_mask
63	RW	WO_AND	WO_OR	OCC_SCOM_OCCLFIRMASK_FIR_PARITY_ERR_MASK: fir_parity_err_mask

Register Name	<i>OCC Local Fault Isolation Action0 Register</i>
Mnemonic	EH.TPCHIP.OCC.OCI.SC.COM.OCC_SCOM_OCCLFIRACT0
Address	0000000001010806 (SCOM)
Attributes	
Description	

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Bits	SCOM	Field Mnemonic: Description
0:63	RW	OCC_SCOM_OCCLFIRACT0_FIR_ACTION0: MSB of action select for corresponding bit in FIR (Action0, Action1, Mask) = Action Select (0,0,0) = Checkstop Error (0,1,0) = Recoverable Error (1,0,0) = Recoverable Interrupt (1,1,0) = Local Core Machine Check (x,x,1) = MASKED

Register Name	<i>OCC Local Fault Isolation Action1 Register</i>
Mnemonic	EH.TPCHIP.OCC.OCI.SC.COM.OCC_SCOM_OCCLFIRACT1
Address	0000000001010807 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	OCC_SCOM_OCCLFIRACT1_FIR_ACTION1: MSB of action select for corresponding bit in FIR (Action0, Action1, Mask) = Action Select (0,0,0) = Checkstop Error (0,1,0) = Recoverable Error (1,0,0) = Recoverable Interrupt (1,1,0) = Local Core Machine Check (x,x,1) = MASKED

Register Name	<i>PBAM Low Sped Part FIR Register</i>
Mnemonic	EH.TPCHIP.PIB.LPCM.LPC.SYNC_FIR_REG
Address	0000000001010C00 (SCOM) 0000000001010C01 (SCOM1) 0000000001010C02 (SCOM2)
Attributes	
Description	PBAM low sped part FIR Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	INVALID_TRANSFER_SIZE: OPB_Master_LS_received_a_transfer_size_value_unequal_to_1-_or_2-_or_4-Byte
1	RWX	WOX_AND	WOX_OR	INVALID_COMMAND: OPB_Master_LS_received_a_invalid_command_no_ci_store_and_no_ci_load
2	RWX	WOX_AND	WOX_OR	INVALID_ADDRESS_ALIGNMENT: OPB_Master_LS_received_a_address_which_was_not_aligned_to_the_received_transfer_size
3	RWX	WOX_AND	WOX_OR	OPB_ERROR: OPB_Master_LS_detected_OPB_ErrAck_which_was_activated_by_the_accessed_OPB_slave
4	RWX	WOX_AND	WOX_OR	OPB_TIMEOUT: the_OPB_arbiter_activated_the_OPB_Timeout_signal_Typical_reason_is_that_the_OPB_access_did_not_hit_any_available_OPB_slave
5	RWX	WOX_AND	WOX_OR	OPB_MASTER_HANG_TIMEOUT: the_OPB_Master_LS_was_not_able_to_end_the_requested_OPB_access_within_the_OPB_Master_LS_hang_timeout_time
6	RWX	WOX_AND	WOX_OR	CMD_BUFFER_PAR_ERR: a parity_error_was_detected_in_the_OPB_Master_LS_command_buffer
7	RWX	WOX_AND	WOX_OR	DAT_BUFFER_PAR_ERR: a parity_error_was_detected_in_the_OPB_Master_LS_data_buffer
8	RWX	WOX_AND	WOX_OR	RETURNQ_ERR: reserved_bit_1_tied_to_zero

[illegible]

Register Name	<i>PBAM_low_speed_part_FIR_Mask_Register</i>
Mnemonic	EH.TPCHIP.PIB.LPCM.LPC.SYNC_FIR_MASK_REG
Address	0000000001010C03 (SCOM) 0000000001010C04 (SCOM1) 0000000001010C05 (SCOM2)
Attributes	
Description	PBAM_low_speed_part_FIR_Mask_Register

[illegible]

Register Name	<i>Register Contains Boot Vector Instruction Word 0</i>
Mnemonic	EH.TPCHIP.OCC.SRAM.SRAM_CTL.SRAM_SRBV0
Address	0000000000066004 (PIB) 0000000040030020 (OCI)
Attributes	Magic=true
Description	This register contains Boot Vector Instruction Word 0



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Bits	PIB	OCI	Field Mnemonic: Description
0:31	RW	RW	SRAM_SRBV0_BOOT_VECTOR_WORD0: Boot Vector Word 0 instruction word 0 returned from SRAM when PPC405 fetches from boot vector address. This register corresponds to address 0xFFFFFFF0 of the cache line holding the boot vector.
32:63	RO	RO	Constant = 0b00000000000000000000000000000000

Register Name	Register Contains Boot Vector Instruction Word 1
Mnemonic	EH.TPCHIP.OCC.SRAM.SRAM_CTL.SRAM_SRBV1
Address	000000000066005 (PIB) 0000000040030028 (OCI)
Attributes	Magic=true
Description	This register contains Boot Vector Instruction Word 1

Bits	PIB	OCI	Field Mnemonic: Description
0:31	RW	RW	SRAM_SRBV1_BOOT_VECTOR_WORD1: Boot Vector Word 1 instruction word 1 returned from SRAM when PPC405 fetches from boot vector address. This register corresponds to address 0xFFFFFFF4 of the cache line holding the boot vector.
32:63	RO	RO	Constant = 0b00000000000000000000000000000000

Register Name	Register Contains Boot Vector Instruction Word 2
Mnemonic	EH.TPCHIP.OCC.SRAM.SRAM_CTL.SRAM_SRBV2
Address	000000000066006 (PIB) 0000000040030030 (OCI)
Attributes	Magic=true
Description	This register contains Boot Vector Instruction Word 2

Bits	PIB	OCI	Field Mnemonic: Description
0:31	RW	RW	SRAM_SRBV2_BOOT_VECTOR_WORD2: Boot Vector Word 2 instruction word 2 returned from SRAM when PPC405 fetches from boot vector address. This register corresponds to address 0xFFFFFFF8 of the cache line holding the boot vector.
32:63	RO	RO	Constant = 0b00000000000000000000000000000000

Register Name	Register Contains Boot Vector Instruction Word 3
Mnemonic	EH.TPCHIP.OCC.SRAM.SRAM_CTL.SRAM_SRBV3
Address	000000000066007 (PIB) 0000000040030038 (OCI)
Attributes	Magic=true
Description	This register contains Boot Vector Instruction Word 3

Bits	PIB	OCI	Field Mnemonic: Description
0:31	RW	RW	SRAM_SRBV3_BOOT_VECTOR_WORD3: Boot Vector Word 3 instruction word 3 returned from SRAM when PPC405 fetches from boot vector address. This register corresponds to address 0xFFFFFFF4 of the cache line holding the boot vector. Init value is a Branch Absolute 0x00000010
32:63	RO	RO	Constant = 0b00000000000000000000000000000000



Register Name	<i>Register Indicates Pending Interrupts to OCC as Enabled by OIMR0 and Configured by Combination of OITR0 (Edge Or Level) and OIEPR0 (Significant Edge or Polarity)</i>
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OISR0
Address	000000000006A000 (PIB) 000000000006A001 (PIB1) 000000000006A002 (PIB2) 0000000040050000 (OCI) 0000000040050008 (OCI1) 0000000040050010 (OCI2)
Attributes	
Description	This register indicates the pending interrupts to the OCC as enabled by the OIMR0 and configured by the combination of OITR0 (Edge or Level) And OIEPR0 (Significant Edge or Polarity). See notes on OITR0 on the set (for injection) or clearing (for interrupt handling) of the bit in this register.

Bits	PIB	PIB1	PIB2	Field Mnemonic: Description
0	ROX	WOX_AND	WOX_OR	ROX
1	ROX	WOX_AND	WOX_OR	ROX
2	ROX	WOX_AND	WOX_OR	ROX
3	ROX	WOX_AND	WOX_OR	ROX
4	ROX	WOX_AND	WOX_OR	ROX
5	ROX	WOX_AND	WOX_OR	ROX
6	ROX	WOX_AND	WOX_OR	ROX
7	ROX	WOX_AND	WOX_OR	ROX
8	ROX	WOX_AND	WOX_OR	ROX
9	ROX	WOX_AND	WOX_OR	ROX
10	ROX	WOX_AND	WOX_OR	ROX
11	ROX	WOX_AND	WOX_OR	ROX
12	ROX	WOX_AND	WOX_OR	ROX
13	ROX	WOX_AND	WOX_OR	ROX
14	ROX	WOX_AND	WOX_OR	ROX
15	ROX	WOX_AND	WOX_OR	ROX
16	ROX	WOX_AND	WOX_OR	ROX
17	ROX	WOX_AND	WOX_OR	ROX
18	ROX	WOX_AND	WOX_OR	ROX
19	ROX	WOX_AND	WOX_OR	ROX
20	ROX	WOX_AND	WOX_OR	ROX
21	ROX	WOX_AND	WOX_OR	ROX
22	ROX	WOX_AND	WOX_OR	ROX
23	ROX	WOX_AND	WOX_OR	ROX
24	ROX	WOX_AND	WOX_OR	ROX
25	ROX	WOX_AND	WOX_OR	ROX
26	ROX	WOX_AND	WOX_OR	ROX
27	ROX	WOX_AND	WOX_OR	ROX

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Bits	PIB	PIB1	PIB2	Field Mnemonic: Description
28	ROX	WOX_AND	WOX_OR	ROX
29	ROX	WOX_AND	WOX_OR	ROX
30	ROX	WOX_AND	WOX_OR	ROX
31	ROX	WOX_AND	WOX_OR	ROX
32:63	RO	RO	RO	RO

Register Name	<i>Register Indicates Pending Interrupts to OCC as Enabled by OIMR and Configured By Combination of OITR (Edge Or Level) and OIEPR (Significant Edge or Polarity)</i>
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OISR1
Address	000000000006A010 (PIB) 000000000006A011 (PIB1) 000000000006A012 (PIB2) 0000000040050080 (OCI) 0000000040050088 (OCI1) 0000000040050090 (OCI2)
Attributes	
Description	This register indicates the pending interrupts to the OCC as enabled by the OIMR and configured by the combination of OITR (Edge or Level) and OIEPR (Significant Edge or Polarity). See notes on OITR on the set (for injection) or clearing (for interrupt handling) of the bit in this register.

Bits	PIB	PIB1	PIB2	Field Mnemonic: Description
0	ROX	WOX_AND	WOX_OR	ROX
1	ROX	WOX_AND	WOX_OR	ROX
2	ROX	WOX_AND	WOX_OR	ROX
3	ROX	WOX_AND	WOX_OR	ROX
4	ROX	WOX_AND	WOX_OR	ROX
5	ROX	WOX_AND	WOX_OR	ROX
6	ROX	WOX_AND	WOX_OR	ROX
7	ROX	WOX_AND	WOX_OR	ROX
8	ROX	WOX_AND	WOX_OR	ROX
9	ROX	WOX_AND	WOX_OR	ROX
10	ROX	WOX_AND	WOX_OR	ROX
11	ROX	WOX_AND	WOX_OR	ROX
12	ROX	WOX_AND	WOX_OR	ROX
13	ROX	WOX_AND	WOX_OR	ROX
14	ROX	WOX_AND	WOX_OR	ROX
15	ROX	WOX_AND	WOX_OR	ROX
16	ROX	WOX_AND	WOX_OR	ROX
17	ROX	WOX_AND	WOX_OR	ROX
18	ROX	WOX_AND	WOX_OR	ROX
19	ROX	WOX_AND	WOX_OR	ROX
20	ROX	WOX_AND	WOX_OR	ROX



Bits	PIB	PIB1	PIB2	Field Mnemonic: Description
21	ROX	WOX_AND	WOX_OR	ROX
22	ROX	WOX_AND	WOX_OR	ROX
23	ROX	WOX_AND	WOX_OR	ROX
24	ROX	WOX_AND	WOX_OR	ROX
25	ROX	WOX_AND	WOX_OR	ROX
26	ROX	WOX_AND	WOX_OR	ROX
27	ROX	WOX_AND	WOX_OR	ROX
28	ROX	WOX_AND	WOX_OR	ROX
29	ROX	WOX_AND	WOX_OR	ROX
30	ROX	WOX_AND	WOX_OR	ROX
31	ROX	WOX_AND	WOX_OR	ROX
32:63	RO	RO	RO	RO

Register Name	<i>Register Masks Interrupts to OCC</i>
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OIMR0
Address	000000000006A004 (PIB) 000000000006A005 (PIB1) 000000000006A006 (PIB2) 0000000040050020 (OCI) 0000000040050028 (OCI1) 0000000040050030 (OCI2)
Attributes	
Description	This register masks interrupts to the OCC.

Bits	PIB	PIB1	PIB2	Field Mnemonic: Description
0:31	RW	WO_AND	WO_OR	RW
32:63	RO	RO	RO	RO

Register Name	<i>Register Masks Interrupts to OCC</i>
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OIMR1
Address	000000000006A014 (PIB) 000000000006A015 (PIB1) 000000000006A016 (PIB2) 00000000400500A0 (OCI) 00000000400500A8 (OCI1) 00000000400500B0 (OCI2)
Attributes	
Description	This register masks interrupts to the OCC.

Bits	PIB	PIB1	PIB2	Field Mnemonic: Description
0:31	RW	WO_AND	WO_OR	RW
32:63	RO	RO	RO	RO

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Register Name		<i>Register Establishes Type of Interrupt Monitored - Level or Edge</i>	
Mnemonic		EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OITR0	
Address		000000000006A008 (PIB) 0000000040050040 (OCI)	
Attributes			
Description		This register establishes the type of interrupt that is monitored: Level or Edge.	
Bits	PIB	OCI	Field Mnemonic: Description
0:31	RW	RW	OCB_OCI_OITR0_INTERRUPT_TYPE: See OCC Interrupt Source 0 for bit definitions. Establish the type of interrupt that is monitored. 0 = Level 1 = Edge When set to Level, the respective OISR bit follows the input to the OISR from the unit driving the signal but with the polarity defined by the OIEPR. Specifically, if the respective OIEPR bit is set to High, this register retains the polarity of the incoming signal; if the respective OIEPR bit is set to Low, this register captures the inverted polarity of the incoming signal. When set to Edge, the respective OISR bit is asserted upon the transition defined by the OIEPR of the input from the unit driving the signal. Specifically, if the respective OIEPR bit is set to Rising, a transition from 0 to 1 sets the bit; if the respective OIEPR bit is set to Falling, a transition from 1 to 0 sets the bit. Note: When set to Level, attempts to override the signal setting via WAND or WOR to the OISR will not stick as the signal input is the priority. Firmware must control the source of the Level signal to control the state of the OISR bit. When set to Edge, AND and OR operations to the OISR will stick (clear or set respectively) in the OISR. Engineering Note: For firmware testing, a potential interrupt injection technique for Level interrupts is to override their definition to Edge and then use the OR register associated with the OISR. This allows the injected transition to stick, because the logic will not follow the input interrupt signal. However, if the firmware is expecting to find status in the driving unit, this technique might not be appropriate.
32:63	RO	RO	Constant = 0b00000000000000000000000000000000

Register Name		<i>Register Establishes Type of Interrupt Monitored - Level or Edge</i>	
Mnemonic		EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OITR1	
Address		000000000006A018 (PIB) 00000000400500C0 (OCI)	
Attributes			
Description		This register establishes the type of interrupt that is monitored: Level or Edge.	

Bits	PIB	OCI	Field Mnemonic: Description
0:31	RW	RW	OCB_OCI_OITR1_INTERRUPT_TYPE: See OCC Interrupt Source 1 for bit definitions. Establish the type of interrupt that is monitored. 0 = Level 1 = Edge When set to Level, the respective OISR bit follows the input to the OISR from the unit driving the signal but with the polarity defined by the OIEPR. Specifically, if the respective OIEPR bit is set to High, this register retains the polarity of the incoming signal; if the respective OIEPR bit is set to Low, this register captures the inverted polarity of the incoming signal. When set to Edge, the respective OISR bit is asserted upon the transition defined by the OIEPR of the input from the unit driving the signal. Specifically, if the respective OIEPR bit is set to Rising, a transition from 0 to 1 sets the bit; if the respective OIEPR bit is set to Falling, a transition from 1 to 0 sets the bit. Note: When set to Level, attempts to override the signal setting via WAND or WOR to the OISR will not stick as the signal input is the priority. Firmware must control the source of the Level signal to control the state of the OISR bit. When set to Edge, WAND and WOR operations to the OISR will stick (clear or set respectively) in the OISR. Engineering Note: For firmware testing, a potential interrupt injection technique for Level interrupts is to override their definition to Edge and then use the WOR register associated with the OISR. This allows the injected transition to stick as the logic will not follow the input interrupt signal. However, if the firmware is expecting to find status in the driving unit, this technique might not be appropriate.

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Bits	PIB	OCI	Field Mnemonic: Description
32:63	RO	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>Register Establishes Either the Significant Edge of an Edge-Enabled Interrupt or Significant Polarity of a Level Enabled That Will Be Detected for Enabled-Interrupt Sources</i>		
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OIEPR0		
Address	000000000006A009 (PIB) 0000000040050048 (OCI)		
Attributes			
Description	This register establishes either the significant edge of an edge-enabled interrupt or the significant polarity of a level enabled that will be detected for enabled interrupt sources.		

Bits	PIB	OCI	Field Mnemonic: Description
0:31	RW	RW	OCB_OCI_OIEPR0_INTERRUPT_EDGE_POL: See OCC Interrupt Source 0 for bit definitions. Establish the edge or polarity of interrupt. 0 = Falling Low 1 = Rising High When set, the respective bit in the OITR is set to Level, then the Low and High meanings apply as follows: If this bit is set to Low, the respective OISR bit follows the inverted input to the OISR from the unit driving the signal. If this bit is set to High, the respective OISR bit follows the direct input to the OISR from the unit driving the signal. When set the respective bit in the OITR is set to Edge, then the Falling and Rising meanings apply as follows: If this bit is set to Falling, a transition from 1 to 0 of the input signal to the OISR sets the respective OISR bit. If this bit is set to Rising, a transition from 0 to 1 of the input signal to the OISR sets the respective OISR bit.
32:63	RO	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>Register Establishes Either the Significant Edge of an Edge-Enabled Interrupt or the Significant Polarity of a Level Enabled That Will Be Detected For Enabled-Interrupt Sources</i>		
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OIEPR1		
Address	000000000006A019 (PIB) 00000000400500C8 (OCI)		
Attributes			
Description	This register establishes either the significant edge of an edge-enabled interrupt or the significant polarity of a level enabled that will be detected for enabled-interrupt sources.		

Bits	PIB	OCI	Field Mnemonic: Description
0:31	RW	RW	OCB_OCI_OIEPR1_INTERRUPT_EDGE_POL: See OCC Interrupt Source 1 for bit definitions. Establish the edge or polarity of interrupt. 0 = Falling Low 1 = Rising High When set, the respective bit in the OITR is set to Level, then the Low and High meanings apply as follows: If this bit is set to Low, the respective OISR bit follows the inverted input to the OISR from the unit driving the signal. If this bit is set to High, the respective OISR bit follows the direct input to the OISR from the unit driving the signal. When set the respective bit in the OITR is set to Edge, then the Falling and Rising meanings apply as follows: If this bit is set to Falling, a transition from 1 to 0 of the input signal to the OISR sets the respective OISR bit. If this bit is set to Rising, a transition from 0 to 1 of the input signal to the OISR sets the respective OISR bit.
32:63	RO	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>Register Determines Whether Interrupts Captured In The Corresponding Fields of the OISR Generate Non-critical (external) Or Critical Interrupts To The OCC</i>
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCIR0
Address	000000000006A00A (PIB) 0000000040050050 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:31	RW	RW	OCB_OCI_OCIR0_INTERRUPT_CRIT: See OCC Interrupt Source 0 for bit definitions. 0 = Interrupt is non-critical (for example, external) 1 = Interrupt is critical
32:63	RO	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>Register Determines Whether Interrupts Captured in Corresponding Fields of OISR Generate Noncritical (external) Or Critical Interrupts to OCC</i>
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OCIR1
Address	000000000006A01A (PIB) 00000000400500D0 (OCI)
Attributes	
Description	This Register determines whether interrupts captured in the corresponding fields of the OISR generate non-critical (external) or critical interrupts to the OCC.

Bits	PIB	OCI	Field Mnemonic: Description
0:31	RW	RW	OCB_OCI_OCIR1_INTERRUPT_CRIT: See OCC Interrupt Source 1 for bit definitions 0 = Interrupt is non-critical (for example, external) 1 = Interrupt is critical
32:63	RO	RO	Constant = 0b00000000000000000000000000000000

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Register Name		<i>Register Controls Whether Pending Unmasked Interrupts Activate Debug Halt Input to OCC</i>	
Mnemonic		EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_ODHER0	
Address		000000000006A00E (PIB) 0000000040050070 (OCI)	
Attributes			
Description		This register controls whether pending unmasked interrupts activate the Debug Halt Input to the OCC.	
Bits	PIB	OCI	Field Mnemonic: Description
0:31	RW	RW	OCB_OCI_ODHER0_DBG_HALT_EN: See OCC Interrupt Source 0 for bit definitions Causes the Debug Halt input of OCC to be asserted if the corresponding interrupt is pending and enabled. 0 = Interrupt Debug Halt disabled. 1 = Interrupt Debug Halt enabled.
32:63	RO	RO	Constant = 0b00000000000000000000000000000000

Register Name		<i>Register Controls Whether Pending Unmasked Interrupts Activate Debug Halt Input to OCC</i>	
Mnemonic		EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_ODHER1	
Address		000000000006A01E (PIB) 00000000400500F0 (OCI)	
Attributes			
Description		This register controls whether pending unmasked interrupts activate the Debug Halt input to the OCC.	
Bits	PIB	OCI	Field Mnemonic: Description
0:31	RW	RW	OCB_OCI_ODHER1_DBG_HALT_EN: See OCC Interrupt Source 1 for bit definitions Causes the Debug Halt input of OCC to be asserted if the corresponding interrupt is pending and enabled. 0 = Interrupt Debug Halt disabled 1 = Interrupt Debug Halt enabled
32:63	RO	RO	Constant = 0b00000000000000000000000000000000

Register Name		<i>Register Controls Whether Pending Unmasked Interrupts Activate the Unconditional Debug Event Input to the OCC</i>	
Mnemonic		EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OUDER0	
Address		000000000006A00C (PIB) 0000000040050060 (OCI)	
Attributes			
Description		This register controls whether pending unmasked interrupts activate the unconditional debug event input to the OCC.	
Bits	PIB	OCI	Field Mnemonic: Description
0:31	RW	RW	OCB_OCI_OUDER0_UNCOND_DBG_EVT: See OCC Interrupt Source 0 for bit definitions. Causes the Unconditional Debug Event input of OCC to be asserted if the corresponding interrupt is pending and enabled. 0 = Interrupt Unconditional Debug Event disabled 1 = Interrupt Unconditional Debug Event enabled
32:63	RO	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>Register Controls Whether Pending Unmasked Interrupts Activate the Unconditional Debug Event Input to the OCC</i>
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OUDER1
Address	000000000006A01C (PIB) 00000000400500E0 (OCI)
Attributes	
Description	This register controls whether pending unmasked interrupts activate the unconditional debug event input to the OCC.

Bits	PIB	OCI	Field Mnemonic: Description
0:31	RW	RW	OCB_OCI_OUDER1_UNCOND_DBG_EVT: See OCC Interrupt Source 1 for bit definitions Causes the Unconditional Debug Event input of OCC to be asserted if the corresponding interrupt is pending and enabled. 0 = Interrupt Unconditional Debug Event disabled 1 = Interrupt Unconditional Debug Event enabled
32:63	RO	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>Timer Control and Status for OCC Timer 0</i>
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OTR0
Address	000000000006A100 (PIB) 0000000040050800 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0	RWX_WCLEAR	RWX_WCLEAR	OCB_OCI_OTR0_TIMEOUT: This bit is set by hardware on any 1 -> 0 transition of the timer. This value of this bit is provided to the interrupt controller as the occ_timer0 status. The interrupt controller would typically be programmed to recognize occ_timer0 as an active-high, level sensitive interrupt. This bit is reset by writing the register with a '1' in this bit position. If the hardware timer value transition from 1 -> 0 occurs concurrently with the updating of this register to perform a reset, then this bit is reset and the hardware transition is lost.
1	WO	WO	OCB_OCI_OTR0_CONTROL: Reading this bit always returns 0. If the register is written with a '1' in this bit position, then all other fields other than timeout are updated. Otherwise the write has no effect other than to clear the timeout field if the timeout bit is set in the write data. If the register is written with a '1' in this bit position and a '0' in the timeout bit position which occurs concurrently with the hardware timer value making a 1 -> 0 transition, the timeout bit will be set per the previous timer settings.
2	RW	RW	OCB_OCI_OTR0_AUTO_RELOAD: If set, the timer operates in auto-reload mode. In auto-reload mode, every timeout of the timer sets the timeout bit and reinitializes the timer counter from the hidden auto-reload value. If clear, then a timeout of the timer simply sets the timeout bit. This field can only be written if the control bit is set on a write of the register.
3:15	RW	RW	OCB_OCI_OTR0_SPARE: Writes store the value only if the control bit is set on a write of this register. Reads return the last value written.
16:31	RWX	RWX	OCB_OCI_OTR0_TIMER: When the register is read, this field returns the current value of the hardware timer. When written, the value of the field goes into the hardware timer and the hidden auto-reload register, and the hardware timer begins to decrement. This field can only be written if the control bit is set on a write of the register.
32:63	RO	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>Timer Control And Status For OCC Timer 1</i>
Mnemonic	EH.TPCHIP.OCC.OCI.OCB.OCB_OCI_OTR1
Address	000000000006A101 (PIB) 0000000040050808 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0	RWX_WCLEAR	RWX_WCLEAR	OCB_OCI_OTR1_TIMEOUT: This bit is set by hardware on any 1 -> 0 transition of the timer. This value of this bit is provided to the interrupt controller as the occ_timer1 status. The interrupt controller would typically be programmed to recognize occ_timer1 as an active-high, level sensitive interrupt. This bit is reset by writing the register with a '1' in this bit position. If the hardware timer value transition from 1 -> 0 occurs concurrently with the updating of this register to perform a reset, then this bit is reset and the hardware transition is lost.
1	WO	WO	OCB_OCI_OTR1_CONTROL: Reading this bit always returns 0. If the register is written with a '1' in this bit position, then all other fields other than timeout are updated. Otherwise the write has no effect other than to clear the timeout field if the timeout bit is set in the write data. If the register is written with a '1' in this bit position and a '0' in the timeout bit position which occurs concurrently with the hardware timer value making a 1 -> 0 transition, the timeout bit will be set per the previous timer settings.
2	RW	RW	OCB_OCI_OTR1_AUTO_RELOAD: If set, the timer operates in auto-reload mode. In auto-reload mode, every timeout of the timer sets the timeout bit and reinitializes the timer counter from the hidden auto-reload value. If clear, then a timeout of the timer simply sets the timeout bit. This field can only be written if the control bit is set on a write of the register.
3:15	RW	RW	OCB_OCI_OTR1_SPARE: Writes store the value only if the control bit is set on a write of this register. Reads return the last value written.
16:31	RWX	RWX	OCB_OCI_OTR1_TIMER: When the register is read, this field returns the current value of the hardware timer. When written, the value of the field goes into the hardware timer and the hidden auto-reload register, and the hardware timer begins to decrement. This field can only be written if the control bit is set on a write of the register.
32:63	RO	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>Basic Modes Of Operation For PMC</i>
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_MODE_REG
Address	0000000000062000 (PIB) 0000000040010000 (OCI)
Attributes	
Description	Note that the bits enable_hw_pstate_mode, enable_fw_auction_pstate_mode, and enable_fw_pstate_mode represent mutually exclusive modes and only one of these modes can be set at a time.

Bits	PIB	OCI	Field Mnemonic: Description
0	RWX	RWX	ENABLE_HW_PSTATE_MODE: If asserted, the hardware controls the Pstate auctioning and the actuation (eVID changes, broadcasts) in a full automatic mode without FW-interaction. Note that if this bit is asserted, the bits enable_fw_auction_pstate_mode and enable_fw_pstate_mode must not be asserted.

Bits	PIB	OCI	Field Mnemonic: Description
1	RWX	RWX	ENABLE_FW_AUCTION_PSTATE_MODE: If asserted, FW exclusively controls the Global Auction Pstate Request field in PMC_Pstate_Monitor_and_Ctrl_Reg and, thus, performs the Pstate auction process in software. The remaining operations (changing eVID voltages and broadcasts to the chiplets) are performed by hardware in this mode. Note that if this bit is set, the bits enable_hw_pstate_mode and enable_fw_pstate_mode must not be asserted.
2	RWX	RWX	ENABLE_FW_PSTATE_MODE: If asserted, FW controls the voltage register that feeds the SPI interface (PGAVR), as well as the registers that contain the global actual Pstate (PPMACR and PEGAVR), the maximum regulation VIDs, and the effective eVID values (that are forwarded to the chiplets). Note: If this bit is asserted, the bits enable_fw_auction_pstate_mode and enable_fw_pstate_mode must not be asserted.
3	RWX	RWX	ENABLE_PSTATE_VOLTAGE_CHANGES: If 1, voltage changes are performed using the SPI interface. If 0, only updates to register PMC_Global_Actual_Voltage_Reg are performed by the hardware and no SPI transaction are triggered. Note: For normal operation, this bit needs to be asserted.
4	RWX	RWX	ENABLE_GLOBAL_ACTUAL_PSTATE_FORWARDING: If this bit is 1, the PMC forwards the global actual Pstate, the eVIDs and the maximum regulation VID to PCBS every time the Pstate protocol requires it.
5	RWX	RWX	HALT_PSTATE_MASTER_FSM: If set to 1, this bit causes the Pstate master FSM (MPS) to complete any on-going operation and then stay in its inactive state.
6	RWX	RWX	ENABLE_INTERCHIP_INTERFACE: If this bit is 1, the interchip interface is enabled for operations based on 'interchip_mode' and the settings of PMIC0.
7	RWX	RWX	INTERCHIP_MODE: Interchip Interface Mode. If enable_interchip_mode = 1, this bit defines the behavior of the interchip interface. 0 = Slave (default). Accepts global actual and msg packets.
8	RWX	RWX	ENABLE_INTERCHIP_PSTATE_IN_HAPS: If asserted, the Pstate request received from the interchip interface is added to the Pstate auction. Should be asserted if interchip_mode = 1 (master) and deasserted if interchip_mode = 0 (slave). In fw_pstate_mode, FW can decide to deassert this bit if it wants to read the haps value for only its own chip and conditionally combine it with the interchip_pstate value from the slave chip (available in PMC_INTCHP_PSTATE_REG).
9	RWX	RWX	ENABLE_PSTATE_STEPPING: If asserted, stepping of Pstates is enabled (which is needed if iVRMs are enabled). Otherwise, Pstates are not stepped and a new request effectively causes a jump to the new Pstate.
10	RWX	RWX	HONOR_OHA_IDLE_STATE_REQUESTS: PMC will honor OHA idle state requests only if this bit is asserted.
11	RWX	RWX	VID_ENDIANESS: Write data LSB within a data byte will be left when bit = 1, right when 0. For example, if bit=1 byte0=bit 7 to 0 and byte1=15 to 8 for arbiter port 0 requests.
12	RWX	RWX	RESET_ALL_PMC_REGISTERS: Writing a 1 to this bit performs a functional reset of all internal pmc registers. Afterwards, firmware has to setup all PMC SCOM registers.
13	RWX	RWX	SAFE_MODE_WITHOUT_SPIVID: If asserted, the spivid macro is not used. Write is suppressed and rdata is filled with a good status, including crc: 0xAAAAAAC0 for write commands, and 0x808080CE for read state commands 0xFFFFFFFF81 for read voltage status Spivid control behaves as if the spivid macro was there (start -> done, error checking, and so on.) This can be used in the lab if there is no connection to external VRMs.

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Bits	PIB	OCI	Field Mnemonic: Description
14	RWX	RWX	HALT_IDLE_STATE_MASTER_FSM: If set to 1, this bit causes the Master Idle State (MIS) FSM to complete any on-going operation and then stay in its inactive state
15	RWX	RWX	INTERCHIP_HALT_IF: If set to 1, this bit prevents a new frame send/receive, but finishes a current one.
16	RWX	RWX	UNFREEZE_PSTATE_PROCESSING: If written with a 1, this bit resets pstate_processing_is_suspended and the GPSA errors in PMC_STATUS_REG. This bit is self-resetting.
17	RWX	RWX	SPIVID_RESET_IF: If set to 1, this bit causes all state regs and counts of the SPI Master Interface to be reset.
18	RWX	RWX	UNFREEZE_ISTATE_PROCESSING: If written with a 1, this bit resets istate_processing_is_suspended in PMC_STATUS_REG. This bit is self-resetting.

Register Name	<i>PPMACR Allows Firmware to Monitor the Internal Pstates Inside PMC and Control the Auctioning by FW and the Setting of the GPSA</i>
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_PSTATE_MONITOR_AND_CTRL_REG
Address	0000000000062002 (PIB) 0000000040010010 (OCI)
Attributes	
Description	The PPMACR allows firmware to monitor the internal Pstates inside PMC, to control the auctioning by FW, and the setting of the GPSA (see the description of the Primary PMC Modes in PMC_MODE_REG).

Bits	PIB	OCI	Field Mnemonic: Description
0:7	ROX	ROX	GPST_VAL: Global Pstate Target The Global Pstate Target field represents the Pstate value that is the result of an auction process (Global Auction Pstate Request) clipped by Pmin_rail and Pmax_rail. This value will eventually be established as Global Pstate Actual after the PMC has performed a complete Pstate transition (possibly including many small babysteps that temporarily change the Global Pstate Actual to intermediate values). The gpst_val field can be updated by hardware or OCC at any time, because the Pstate transition process is continuous. Value is an 8-bit signed integer representing an offset from Fnominal. A read from the field returns the current Global Pstate Target (that was either established by the PMC hardware or by OCC firmware, see above) The gpsa_inprogress and PMC Status Register[gpsa_*]. bits indicates the protocol status.
8:15	ROX	ROX	GPSST: Global Pstate Step Target This field represents the value of the next (baby) step Pstate for the transition from the current Global Pstate Actual in the direction of the Global Pstate Target. This value is updated before the next (baby) step is attempted (that is, before attempting to broadcast it as the next Global Actual Pstate and before changing the external voltage). Because the Global Pstate Target can change at any time, the direction of the step is computed for every update. A step will never overshoot and go beyond the Global Pstate Target, that is, the last step will possibly be clipped by gpst_val. Value is an 8-bit signed integer representing an offset from Fnominal. A read from the field returns the current Global Pstate Step Target. The PMC Status Register[gpsa_*] bits indicates the protocol status.

Bits	PIB	OCI	Field Mnemonic: Description
16:23	RWX	RWX	GPSA: Global Pstate Actual This field represents the value of the Global Pstate Actual. This value is updated, after each successful voltage change and, thus, always represents the Pstate for the last successfully set external rail voltage. If an error happens when changing the voltage, the old PState value that was present before the voltage change attempt will be kept in this field Value is an 8-bit signed integer representing an offset from Fnominal. A read from the field returns the current Global Pstate Actual. A write to this dial is only performed, if the switch enable_fw_pstate_mode is asserted. This allows FW to set the Global Actual Pstate that is eventually broadcast to the chiplets. The PMC Status Register[gpsa_*] bits indicates the protocol status for the case that the HW controls the protocol.
24:31	RWX	RWX	GAPR: Global Auction Pstate Request The Global Auction Pstate Request field represents the Pstate value that is the result of an auction process (the auction is either performed by OCC if enable_fw_auction_pstate_mode is asserted, or by the PMC hardware, if enable_fw_auction_pstate_mode is deasserted). This value - clipped by Pmax_rail and Pmin_rail - will eventually be established as Global Pstate Target. The gapr field can be updated by hardware or OCC at any time, because the Pstate transition process is continuous. Value is an 8-bit signed integer representing an offset from Fnominal. A read from the field returns the current Global Auction Pstate Request (that was either established by the PMC hardware or by OCC firmware, see above) A write to this register is only performed, if enable_fw_auction_pstate_mode is asserted. If the write is performed, it causes the well-defined sequence of voltage change and hardware multicast of the new Global Actual Pstate (including acknowledgment collection from each EX chiplet) to be performed. If enable_fw_auction_pstate_mode is deasserted, this register updates every cycle with the hardware auction pstate value (refer to dial haps) The gpsa_inprogress and gpsa_error bits indicates the protocol status.

Register Name	PRBR Register
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_RAIL_BOUNDS_REGISTER
Address	0000000000062003 (PIB) 0000000040010018 (OCI)
Attributes	
Description	The PRBR establishes the minimum and maximum values. In Pstate terms, for the Chip Voltage rail. These settings allow firmware to clip, both high and low, the output of the hardware Pstate voting mechanisms.

Bits	PIB	OCI	Field Mnemonic: Description
0:7	RW	RW	PMIN_RAIL: minimum Pstate (set to -128 to disable this limits)
8:15	RW	RW	PMAX_RAIL: maximum Pstate (set to +127 to disable this limits)

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Register Name	PGPBR Registers
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_GLOBAL_PSTATE_BOUNDS_REG
Address	0000000000062004 (PIB) 0000000040010020 (OCI)
Attributes	
Description	The PGPBR establishes the minimum and maximum Global Pstates Indexes represented in the Global Pstate Table. These registers are used to clip the minimum and maximum voltages produced.

Bits	PIB	OCI	Field Mnemonic: Description
0:7	RW	RW	GPSI_MIN: Minimum Pstate index, unsigned because it points to the index in the global table, which is defined as Index = Pstate + 128 (which is ≥ 0 in any case).
8:14	RW	RW	GPST_NUMBER_OF_ENTRIES_MINUS_ONE: Number of entries in global Pstate table (unsigned, 7 bit, a value of N means N+1 entries). Note that FW has to ensure, that $gpsi\_min + gpst\_number\_entries \leq 255$ otherwise, the hardware behavior is undefined.

Register Name	PMC Parameter Register 1
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_PARAMETER_REG1
Address	0000000000062006 (PIB) 0000000040010030 (OCI)
Attributes	
Description	Basic parameters of operation for PMC

Bits	PIB	OCI	Field Mnemonic: Description
0:21	RW	RW	BA_SRAM_PSTATE_TABLE: Base address for the Pstate table in the SRAM (21 MSBs only, the remaining bits are computed using the Pstate and three, zero bits are used as LSBs of the final address for the 8-byte alignment)
22:29	RW	RW	PVSAFE: Pstate value which is set at IPL time and defines the voltage Pstate to force an override of the Global Pstate Target upon the OCC Heartbeat loss. Given the PMC does not detect a voltage error that produces a voltage freeze condition, the forced target would be stepped naturally to put the external rails at a predefined external voltage

Register Name	PEGAVR Register
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_EFF_GLOBAL_ACTUAL_VOLTAGE_REG
Address	0000000000062007 (PIB) 0000000040010038 (OCI)
Attributes	
Description	The PEGAVR allows firmware to overwrite the maximum regulation and the effective external VID values. Used in the Global Pstate Actual Hardware Protocol if Dial Enable_fw_pstate_mode is set. In this case, the write to this register causes a broadcast of the global actual Pstate as well as the maxreg and eff_eVID values. If dial enable_fw_pstate_mode is not set, SCOM writes to this register are ignored and the hardware is in control of this register. Note that this register gets updated with the voltages that correspond to the next gpsst after the data have been read from the SRAM tank and before the gpsa is updated.

Bits	PIB	OCI	Field Mnemonic: Description
0:7	RWX	RWX	MAXREG_VDD: Maximum Regulation VID - VDD Rail. This field represents the voltage at which the internal VDD Voltage Regulation Macros (VRMs) are to be bypassed as these VRMs will not be able to regulate above this value. The value present here is a function of the chip rail voltage setting as driven by the external VDD VRM and must be set 100 mV below the external VDD VRM value. This field is encoded in iVRM format, a simple 7bit linear encode that spans from .6 V (zero encode point) to 1.39375 V in 6.25 mV increments.
8:15	RWX	RWX	MAXREG_VCS: Maximum Regulation VID - VCS Rail. This field represents the voltage at which the internal VCS Voltage Regulation Macros (VRMs) are to be bypassed as the VRM will not be able to regulate above this value. The value present here is a function of the chip rail voltage setting as driven by the external VCS VRM and must be set 100 mV below the external VCS VRM value. This field is encoded in iVRM format, a simple 7-bit linear encode that spans from .6 V (zero encode point) to 1.39375 V in 6.25 mV increments.
16:23	RWX	RWX	EFF_EVID_VDD: Effective external VDD voltage This field represents the effective external VDD voltage taking into account the setting of the external VRMs and the IR-drop effect. The intent of this value is to be forwarded to PCBS and to be used in PCBS for the iVRM strength computation. This field is encoded in iVRM format, a simple 7-bit linear encode that spans from .6 V (zero encode point) to 1.39375 V in 6.25 mV increments
24:31	RWX	RWX	EFF_EVID_VCS: Effective external VCS voltage. This field represents the effective external VCS voltage taking into account the setting of the external VRMs and the IR-drop effect. The intent of this value is to be forwarded to PCBS and to be used in PCBS for the iVRM strength computation. This field is encoded in iVRM format, a simple 7-bit linear encode that spans from .6 V (zero encode point) to 1.39375 V in 6.25 mV increments.

Register Name	PMCSR Register
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_STATUS_REG
Address	0000000000062009 (PIB) 0000000040010048 (OCI)
Attributes	
Description	The PMCSR provides the status on the operations of the PMC.

Bits	PIB	OCI	Field Mnemonic: Description
0	ROX	ROX	PSTATE_PROCESSING_IS_SUSPENDED: If this bit is asserted, PMC does not perform any voltage changes nor global actual Pstate broadcasts due to a configurable error that has happened (configuration mask is). In order to re-enable Pstate processing, the dial unfreeze_pstate_processing needs to be set.
1	ROX	ROX	GPSA_BDCST_ERROR: Global Pstate Actual Protocol Broadcast Error. This bit is set if the PIB broadcast of the Global Pstate Actual has returned an unexpected PIB return code. This bit is reset, when unfreeze_pstate_processing is asserted.
2:4	ROX	ROX	GPSA_BDCST_RESP_INFO: Global Pstate Actual Protocol Broadcast Error PIB response info. This field contains the PIB response info after an unsuccessful gpsa broadcast. This field is reset, when unfreeze_pstate_processing is asserted.
5	ROX	ROX	GPSA_VCHG_ERROR: Global Pstate Actual Protocol Voltage Change Error. This bit is set if the voltage change for the Global Pstate Actual Protocol has failed. Further information about the nature of the fail can be found in PMC_SPI_STATUS_REG.

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Bits	PIB	OCI	Field Mnemonic: Description
6	ROX	ROX	GPSA_TIMEOUT_ERROR: Global Pstate Actual Protocol Timeout. This bit is set if all acknowledgments have not been received from the EX chiplet after the timeout defined in TBD. This bit is reset, when unfreeze_pstate_processing is asserted.
7	ROX	ROX	GPSA_CHG_ONGOING: Global Pstate Actual Protocol In-Progress 0 = Protocol is complete. 1 = Protocol is in progress. This bit will be set when the hardware initiated a Global Pstate actuation in the hw_pstate_mode and in the fw_auction_pstate_mode. This bit will be cleared by hardware upon the receipt of all acknowledgments from the EX chiplets that the Global Pstate is in effect and after a successful voltage change (in the right order of course). If after the timeout defined by TBD dial all acknowledgments have not been received, this bit should remain asserted and the PMC Status Register[gpsa_timeout] will be set.
8	ROX	ROX	VOLT_CHG_ONGOING: Voltage change ongoing bit 0 = Voltage change is complete. 1 = Voltage change is in progress. This bit will be set when the PMC is in fw_pstate_mode and when FW has written the register PGAVR to start a voltage change for the external VRMs using the SPIVID interface. This bit will be cleared by hardware upon successful completion of the SPIVID transaction and after waiting the regular wait time after a voltage change. In case of an SPIVID error, this bit will not e cleared.
9	ROX	ROX	BRD_CST_ONGOING: Global Pstate Actual (GPSA) Broadcast ongoing bit 0 = GPSA broadcast is complete and all Acks have been received. 1 = GPSA broadcast is in progress. This bit will be set when the PMC is in fw_pstate_mode and when FW has written the register PEGAVR to start a GPSA broadcast. This bit will be cleared by hardware upon receiving all ACKs for the GPSA broadcast. This bit will not be cleared in case of an error (that is, missing ACK).
10	ROX	ROX	GPS_TABLE_ERROR: Global Pstate Table read error. This bit is set if during a PState table read operation the OCI master reports a read error, a parity error, a timeout error, or if the received gpst checkbyte is wrong.
11	ROX	ROX	PSTATE_INTERCHIP_ERROR: Interchip interface error. This bit is set if an UE on the own Interchip interface or on the Interchip interface of the companion chip has occurred.
12	ROX	ROX	ISTATE_PROCESSING_IS_SUSPENDED: If this bit is asserted, PMC does not perform any idle_state changes due to an error not masked by PMC_IDLE_SUSPEND_MASK_REG. In order to re-enable idle_state processing, PMC_Reset is required (PMC_MODE_REG.reset_all_pmc_registers=1).
13	ROX	ROX	SAFE_MODE_ENGAGED: If this bit is asserted, PMC is in Pvsafe mode. This means that the value defined in PMC_PARAMETER_REG1.pvsafe is forced to be used as the Global Pstate Target. Pvsafe mode is used when PMC detects a OCC heartbeat loss.

Register Name	PMCOHBR Register
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_OCC_HEARTBEAT_REG
Address	000000000062066 (PIB) 0000000040010330 (OCI)
Attributes	
Description	The PMCOHBR controls the behavior of the PMC OCC heartbeat function.

Bits	PIB	OCI	Field Mnemonic: Description
0:15	RW	RW	PMC_OCC_HEARTBEAT_TIME: OCC Heartbeat Time Value This field defines the number of hang timer pulses multiplied by (hangpulse_predivider + 1) in which an OCI read of the PMCSR is not detected that will constitute the loss of the OCC heartbeat. If pmc_occ_heartbeat_en is set and and upon this loss detection, a the malfunction alert is surfaced and, if enabled, TBD FIR is activated to notify the FSP. 0x0000 - For debug purposes only, immediate heartbeat_lost if pmc_occ_heartbeat_en = 1 0x0001 - 1 x hang timer pulse/(hangpulse_predivider+1) 0x0002 - 2 x hang timer pulses/(hangpulse_predivider+1) ... 0xFFFF - 65535 x hang timer pulses/(hangpulse_predivider+1) This value is loaded into a decremter on every PCB read of the PMCSR. The pulses used for this function come from a free running pervasive hang timer pulse programmed to be ~1us that has up to a 6 bit precounter whose carryout forms a decrement pulse. Upon the writing of this register (to set and enable) or the reading or writing of the configurable heartbeat trigger register, the precounter is cleared and will begin counting upon the next PM_Hang_Pulse. This PM_Hang_Pulse may arrive immediately or a full duration later. Upon the divided hang pulse, the decremter ticks. if the decremter reaches x0000, the heartbeat loss event is triggered. Note: For hangpulse_predivider=0, the decremter ticks with nest_nclk/4. Reads return the last value written. Writes store the value written. However, the action of the underlying hardware (as described) must have occ_heartbeat_en set.
16	RW	RW	PMC_OCC_HEARTBEAT_EN: PMC OCC Heartbeat Timer Enable 0 = Disable the OCC Heartbeat function. Write to PMCOHBR does not cause decremter reloads nor does the lack of reads to the PMCSR cause heartbeat loss events to be triggered (no FIRs are set nor are malfunctions alerts surfaced). 1 = Enable the OCC Heartbeat function.

Register Name	<i>PMC Core Deconfiguration Register</i>
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_CORE_DECONFIGURATION_REG
Address	00000000006200D (PIB) 0000000040010068 (OCI)
Attributes	
Description	This register avoids talking to deconfigured or partial good chiplets and determines which chiplets are in ECO mode for the PMC.

Bits	PIB	OCI	Field Mnemonic: Description
0:15	RW	RW	CORE_CHIPLET_DECONF_VECTOR: An asserted bit means a bad core chiplet. bit 0 = core 0; bit 1 = core 1; and so on.

Register Name	<i>PMC FSM State and Status Register (PMCFSSR)</i>
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_FSMSTATE_STATUS_REG
Address	000000000062020 (PIB) 0000000040010100 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:2	ROX	ROX	MIS_FSM_STATE: Current state of the Master Idle State Sequencer

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Bits	PIB	OCI	Field Mnemonic: Description
3:7	ROX	ROX	MPS_FSM_STATE: Current state of the Master Pstate Sequencer
8:11	ROX	ROX	SVS_FSM_STATE: Current state of the SPIVID Sequencer
12:15	ROX	ROX	O2S_FSM_STATE: Current state of the OCI to SPI Bridge Sequencer
16:19	ROX	ROX	M2P_FSM_STATE: Current state of the Master to PIB Sequencer
20:23	ROX	ROX	O2P_FSM_STATE: Current state of the OCI to PIB Bridge Sequencer
24:28	ROX	ROX	ICP_MSG_FSM_STATE: Current state of the Interchip Message Transfer Sequencer

Register Name	PMC Pending Idle State Request Register (PIRR0)
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_PEND_IDLE_REQ_REG0
Address	0000000000062080 (PIB) 0000000040010400 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0	ROX	ROX	IDLE_PENDING_0: 0 = Not Pending 1 = Pending This bit is set upon the decoding of a valid waking interrupt from Chiplet 0. This bit is cleared once this chiplet participates in an exit event.
1:2	ROX	ROX	IDLE_OP_0: 00 = Run 01 = Nap 10 = Sleep 11 = Winkle These bits are only valid if Chiplet 0 Idle Pending = 1. When Chiplet 0 Idle Pending becomes 0, these bits do not change.
3	ROX	ROX	IDLE_TYPE_0: 0 = Entry 1 = Exit This bit is only valid if Chiplet 0 Idle Pending = 1. When Chiplet 0 Idle Pending becomes 0, this bit does not change.
4	ROX	ROX	IDLE_SCOPE_0: 0 = Non-Power Off 1 = Power Off This bit is only valid if Chiplet 0 Idle Pending = 1. When Chiplet 0 Idle Pending becomes 0, this bit does not change.
5	ROX	ROX	ASSIST_MODE_0: 0 = No assist 1 = Assist This bit is only valid if Chiplet 0 Idle Pending = 1. When Chiplet 0 Idle Pending becomes 0, this bit does not change.
6:7	ROX	ROX	RESERVED_PIRR_0: reserved bits
8	ROX	ROX	IDLE_PENDING_1: 0 = Not Pending 1 = Pending See Chiplet 0 Idle Pending description though applicable to Chiplet 1



Bits	PIB	OCI	Field Mnemonic: Description
9:10	ROX	ROX	IDLE_OP_1: 00 = Run 01 = Nap 10 = Sleep 11 = Winkle See Chiplet 0 Idle Pending description though applicable to Chiplet 1
11	ROX	ROX	IDLE_TYPE_1: 0 = Entry 1 = Exit See Chiplet 0 Idle Pending description though applicable to Chiplet 1
12	ROX	ROX	IDLE_SCOPE_1: 0 = Non-Power Off 1 = Power Off See Chiplet 0 Idle Pending description though applicable to Chiplet 1
13	ROX	ROX	ASSIST_MODE_1: 0 = No assist 1 = Assist See Chiplet 0 Idle Pending description though applicable to Chiplet 1
14:15	ROX	ROX	RESERVED_PIRR_1: reserved bits
16	ROX	ROX	IDLE_PENDING_2: 0 = Not Pending 1 = Pending See Chiplet 0 Idle Pending description though applicable to Chiplet 2
17:18	ROX	ROX	IDLE_OP_2: 00 = Run 01 = Nap 10 = Sleep 11 = Winkle See Chiplet 0 Idle Pending description though applicable to Chiplet 2
19	ROX	ROX	IDLE_TYPE_2: 0 = Entry 1 = Exit See Chiplet 0 Idle Pending description though applicable to Chiplet 2
20	ROX	ROX	IDLE_SCOPE_2: 0 = Non-Power Off 1 = Power Off See Chiplet 0 Idle Pending description though applicable to Chiplet 2
21	ROX	ROX	ASSIST_MODE_2: 0 = No assist 1 = Assist See Chiplet 0 Idle Pending description though applicable to Chiplet 2
22:23	ROX	ROX	RESERVED_PIRR_2: reserved bits
24	ROX	ROX	IDLE_PENDING_3: 0 = Not Pending 1 = Pending See Chiplet 0 Idle Pending description though applicable to Chiplet 3
25:26	ROX	ROX	IDLE_OP_3: 00 = Run 01 = Nap 10 = Sleep 11 = Winkle See Chiplet 0 Idle Pending description though applicable to Chiplet 3

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Bits	PIB	OCI	Field Mnemonic: Description
27	ROX	ROX	IDLE_TYPE_3: 0 = Entry 1 = Exit See Chiplet 0 Idle Pending description though applicable to Chiplet 3
28	ROX	ROX	IDLE_SCOPE_3: 0 = Non-Power Off 1 = Power Off See Chiplet 0 Idle Pending description though applicable to Chiplet 3
29	ROX	ROX	ASSIST_MODE_3: 0 = No assist 1 = Assist See Chiplet 0 Idle Pending description though applicable to Chiplet 3
30:31	ROX	ROX	RESERVED_PIRR_3: reserved bits

Register Name	<i>PMC Pending Idle State Request Register (PIRR1)</i>
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_PEND_IDLE_REQ_REG1
Address	0000000000062081 (PIB) 0000000040010408 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0	ROX	ROX	IDLE_PENDING_4: 0 = Not Pending 1 = Pending This bit is set upon the decoding of a valid waking interrupt from Chiplet 4. This bit is cleared once this chiplet participates in an exit event.
1:2	ROX	ROX	IDLE_OP_4: 00 = Run 01 = Nap 10 = Sleep 11 = Winkle These bits are only valid if Chiplet 4 Idle Pending = 1. When Chiplet 4 Idle Pending becomes 0, these bits do not change.
3	ROX	ROX	IDLE_TYPE_4: 0 = Entry 1 = Exit This bit is only valid if Chiplet 4 Idle Pending = 1. When Chiplet 4 Idle Pending becomes 0, this bit does not change.
4	ROX	ROX	IDLE_SCOPE_4: 0 = Non-Power Off 1 = Power Off This bit is only valid if Chiplet 4 Idle Pending = 1. When Chiplet 4 Idle Pending becomes 0, this bit does not change.
5	ROX	ROX	ASSIST_MODE_4: 0 = No assist 1 = Assist This bit is only valid if Chiplet 4 Idle Pending = 1. When Chiplet 4 Idle Pending becomes 0, this bit does not change.
6:7	ROX	ROX	RESERVED_PIRR_4: reserved bits



Bits	PIB	OCI	Field Mnemonic: Description
8	ROX	ROX	IDLE_PENDING_5: 0 = Not Pending 1 = Pending See Chiplet 4 Idle Pending description though applicable to Chiplet 5
9:10	ROX	ROX	IDLE_OP_5: 00 = Run 01 = Nap 10 = Sleep 11 = Winkle See Chiplet 4 Idle Pending description though applicable to Chiplet 5
11	ROX	ROX	IDLE_TYPE_5: 0 = Entry 1 = Exit See Chiplet 4 Idle Pending description though applicable to Chiplet 5
12	ROX	ROX	IDLE_SCOPE_5: 0 = Non-Power Off 1 = Power Off See Chiplet 4 Idle Pending description though applicable to Chiplet 5
13	ROX	ROX	ASSIST_MODE_5: 0 = No assist 1 = Assist See Chiplet 4 Idle Pending description though applicable to Chiplet 5
14:15	ROX	ROX	RESERVED_PIRR_5: reserved bits
16	ROX	ROX	IDLE_PENDING_6: 0 = Not Pending 1 = Pending See Chiplet 4 Idle Pending description though applicable to Chiplet 6
17:18	ROX	ROX	IDLE_OP_6: 00 = Run 01 = Nap 10 = Sleep 11 = Winkle See Chiplet 4 Idle Pending description though applicable to Chiplet 6
19	ROX	ROX	IDLE_TYPE_6: 0 = Entry 1 = Exit See Chiplet 4 Idle Pending description though applicable to Chiplet 6
20	ROX	ROX	IDLE_SCOPE_6: 0 = Non-Power Off 1 = Power Off See Chiplet 4 Idle Pending description though applicable to Chiplet 6
21	ROX	ROX	ASSIST_MODE_6: 0 = No assist 1 = Assist See Chiplet 4 Idle Pending description though applicable to Chiplet 6
22:23	ROX	ROX	RESERVED_PIRR_6: reserved bits
24	ROX	ROX	IDLE_PENDING_7: 0 = Not Pending 1 = Pending See Chiplet 4 Idle Pending description though applicable to Chiplet 7

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Bits	PIB	OCI	Field Mnemonic: Description
25:26	ROX	ROX	IDLE_OP_7: 00 = Run 01 = Nap 10 = Sleep 11 = Winkle See Chiplet 4 Idle Pending description though applicable to Chiplet 7
27	ROX	ROX	IDLE_TYPE_7: 0 = Entry 1 = Exit See Chiplet 4 Idle Pending description though applicable to Chiplet 7
28	ROX	ROX	IDLE_SCOPE_7: 0 = Non-Power Off 1 = Power Off See Chiplet 4 Idle Pending description though applicable to Chiplet 7
29	ROX	ROX	ASSIST_MODE_7: 0 = No assist 1 = Assist See Chiplet 4 Idle Pending description though applicable to Chiplet 7
30:31	ROX	ROX	RESERVED_PIRR_7: Reserved bits

Register Name	<i>PMC Pending Idle State Request Register (PIRR2)</i>
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_PEND_IDLE_REQ_REG2
Address	0000000000062082 (PIB) 0000000040010410 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0	ROX	ROX	IDLE_PENDING_8: 0 = Not Pending 1 = Pending This bit is set upon the decoding of a valid waking interrupt from Chiplet 8. This bit is cleared once this chiplet participates in an exit event.
1:2	ROX	ROX	IDLE_OP_8: 00 = Run 01 = Nap 10 = Sleep 11 = Winkle These bits are only valid if Chiplet 8 Idle Pending = 1. When Chiplet 8 Idle Pending becomes 0, these bits do not change.
3	ROX	ROX	IDLE_TYPE_8: 0 = Entry 1 = Exit This bit is only valid if Chiplet 8 Idle Pending = 1. When Chiplet 8 Idle Pending becomes 0, this bit does not change.
4	ROX	ROX	IDLE_SCOPE_8: 0 = Non-Power Off 1 = Power Off This bit is only valid if Chiplet 8 Idle Pending = 1. When Chiplet 8 Idle Pending becomes 0, this bit does not change.



Bits	PIB	OCI	Field Mnemonic: Description
5	ROX	ROX	ASSIST_MODE_8: 0 = No assist 1 = Assist This bit is only valid if Chiplet 8 Idle Pending = 1. When Chiplet 8 Idle Pending becomes 0, this bit does not change.
6:7	ROX	ROX	RESERVED_PIRR_8: reserved bits
8	ROX	ROX	IDLE_PENDING_9: 0 = Not Pending 1 = Pending See Chiplet 8 Idle Pending description though applicable to Chiplet 9
9:10	ROX	ROX	IDLE_OP_9: 00 = Run 01 = Nap 10 = Sleep 11 = Winkle See Chiplet 8 Idle Pending description though applicable to Chiplet 9
11	ROX	ROX	IDLE_TYPE_9: 0 = Entry 1 = Exit See Chiplet 8 Idle Pending description though applicable to Chiplet 9
12	ROX	ROX	IDLE_SCOPE_9: 0 = Non-Power Off 1 = Power Off See Chiplet 8 Idle Pending description though applicable to Chiplet 9
13	ROX	ROX	ASSIST_MODE_9: 0 = No assist 1 = Assist See Chiplet 8 Idle Pending description though applicable to Chiplet 9
14:15	ROX	ROX	RESERVED_PIRR_9: Reserved bits
16	ROX	ROX	IDLE_PENDING_10: 0 = Not Pending 1 = Pending See Chiplet 8 Idle Pending description though applicable to Chiplet 10
17:18	ROX	ROX	IDLE_OP_10: 00 = Run 01 = Nap 10 = Sleep 11 = Winkle See Chiplet 8 Idle Pending description though applicable to Chiplet 10
19	ROX	ROX	IDLE_TYPE_10: 0 = Entry 1 = Exit See Chiplet 8 Idle Pending description though applicable to Chiplet 10
20	ROX	ROX	IDLE_SCOPE_10: 0 = Non-Power Off 1 = Power Off See Chiplet 8 Idle Pending description though applicable to Chiplet 10
21	ROX	ROX	ASSIST_MODE_10: 0 = No assist 1 = Assist See Chiplet 8 Idle Pending description though applicable to Chiplet 10
22:23	ROX	ROX	RESERVED_PIRR_10: Reserved bits

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Bits	PIB	OCI	Field Mnemonic: Description
24	ROX	ROX	IDLE_PENDING_11: 0 = Not Pending 1 = Pending See Chiplet 8 Idle Pending description though applicable to Chiplet 11
25:26	ROX	ROX	IDLE_OP_11: 00 = Run 01 = Nap 10 = Sleep 11 = Winkle See Chiplet 8 Idle Pending description though applicable to Chiplet 11
27	ROX	ROX	IDLE_TYPE_11: 0 = Entry 1 = Exit See Chiplet 8 Idle Pending description though applicable to Chiplet 11
28	ROX	ROX	IDLE_SCOPE_11: 0 = Non-Power Off 1 = Power Off See Chiplet 8 Idle Pending description though applicable to Chiplet 11
29	ROX	ROX	ASSIST_MODE_11: 0 = No assist 1 = Assist See Chiplet 8 Idle Pending description though applicable to Chiplet 11
30:31	ROX	ROX	RESERVED_PIRR_11: reserved bits

Register Name	PMC Pending Idle State Request Register (PIRR3)
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_PEND_IDLE_REQ_REG3
Address	0000000000062083 (PIB) 0000000040010418 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0	ROX	ROX	IDLE_PENDING_12: 0 = Not Pending 1 = Pending This bit is set upon the decoding of a valid waking interrupt from Chiplet 12. This bit is cleared once this chiplet participates in an exit event.
1:2	ROX	ROX	IDLE_OP_12: 00 = Run 01 = Nap 10 = Sleep 11 = Winkle These bits are only valid if Chiplet 12 Idle Pending = 1. When Chiplet 12 Idle Pending becomes 0, these bits do not change.
3	ROX	ROX	IDLE_TYPE_12: 0 = Entry 1 = Exit This bit is only valid if Chiplet 12 Idle Pending = 1. When Chiplet 12 Idle Pending becomes 0, this bit does not change.



Bits	PIB	OCI	Field Mnemonic: Description
4	ROX	ROX	IDLE_SCOPE_12: 0 = Non-Power Off 1 = Power Off This bit is only valid if Chiplet 12 Idle Pending = 1. When Chiplet 12 Idle Pending becomes 0, this bit does not change.
5	ROX	ROX	ASSIST_MODE_12: 0 = No assist 1 = Assist This bit is only valid if Chiplet 12 Idle Pending = 1. When Chiplet 12 Idle Pending becomes 0, this bit does not change.
6:7	ROX	ROX	RESERVED_PIRR_12: reserved bits
8	ROX	ROX	IDLE_PENDING_13: 0 = Not Pending 1 = Pending See Chiplet 0 Idle Pending description though applicable to Chiplet 13
9:10	ROX	ROX	IDLE_OP_13: 00 = Run 01 = Nap 10 = Sleep 11 = Winkle See Chiplet 0 Idle Pending description though applicable to Chiplet 13
11	ROX	ROX	IDLE_TYPE_13: 0 = Entry 1 = Exit See Chiplet 0 Idle Pending description though applicable to Chiplet 13
12	ROX	ROX	IDLE_SCOPE_13: 0 = Non-Power Off 1 = Power Off See Chiplet 0 Idle Pending description though applicable to Chiplet 13
13	ROX	ROX	ASSIST_MODE_13: 0 = No assist 1 = Assist See Chiplet 12 Idle Pending description though applicable to Chiplet 13
14:15	ROX	ROX	RESERVED_PIRR_13: Reserved bits
16	ROX	ROX	IDLE_PENDING_14: 0 = Not Pending 1 = Pending See Chiplet 12 Idle Pending description though applicable to Chiplet 14
17:18	ROX	ROX	IDLE_OP_14: 00 = Run 01 = Nap 10 = Sleep 11 = Winkle See Chiplet 12 Idle Pending description though applicable to Chiplet 14
19	ROX	ROX	IDLE_TYPE_14: 0 = Entry 1 = Exit See Chiplet 12 Idle Pending description though applicable to Chiplet 14
20	ROX	ROX	IDLE_SCOPE_14: 0 = Non-Power Off 1 = Power Off See Chiplet 12 Idle Pending description though applicable to Chiplet 14

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Bits	PIB	OCI	Field Mnemonic: Description
21	ROX	ROX	ASSIST_MODE_14: 0 = No assist 1 = Assist See Chiplet 12 Idle Pending description though applicable to Chiplet 14
22:23	ROX	ROX	RESERVED_PIRR_14: Reserved bits
24	ROX	ROX	IDLE_PENDING_15: 0 = Not Pending 1 = Pending See Chiplet 12 Idle Pending description though applicable to Chiplet 15
25:26	ROX	ROX	IDLE_OP_15: 00 = Run 01 = Nap 10 = Sleep 15 = Winkle See Chiplet 12 Idle Pending description though applicable to Chiplet 15
27	ROX	ROX	IDLE_TYPE_15: 0 = Entry 1 = Exit See Chiplet 12 Idle Pending description though applicable to Chiplet 15
28	ROX	ROX	IDLE_SCOPE_15: 0 = Non-Power Off 1 = Power Off See Chiplet 12 Idle Pending description though applicable to Chiplet 15.
29	ROX	ROX	ASSIST_MODE_15: 0 = No assist 1 = Assist See Chiplet 12 Idle Pending description though applicable to Chiplet 15.
30:31	ROX	ROX	RESERVED_PIRR_15: reserved bits

Register Name	PMC PORE Request Register 0 (PORRR0)
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_PORE_REQ_REG0
Address	000000000006208E (PIB) 0000000040010470 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:7	ROX	ROX	PORRR_reserved0 Written with 0s
8:11	ROX	ROX	PORRR_START_VECTOR: Start_Vector. This field indicates the class of transition requested to the PORE, which is translated into an execution address vector. 0x0 - Fast Sleep Entry 0x1 - Deep Sleep Entry 0x2 - Fast Sleep Exit 0x3 - Deep Sleep Exit 0x4 - Fast Winkle Entry 0x5 - Deep Winkle Entry 0x6 - Fast Winkle Exit 0x7 - Deep Winkle Exit 0x8 - Nap Entry 0x9 - Nap Exit 0xA - 0xF Reserved

Bits	PIB	OCI	Field Mnemonic: Description
12:19	ROX	ROX	PORRR_reserved1 Not implemented.
20	ROX	ROX	PORRR_PORE_BUSY: Value of PORE_busy. 1- indicates that the request in PORRR is a valid outstanding one.
21	ROX	ROX	PORRR_PORE_SUSPENDED: Value of PORE_suspended. PORE_suspended due to PORE error indicated by PORRS write, timeout waiting for PORRS write, or pore_fatal_error signal is reflected in PORRR bit 21, and blocks writes of PORRS that do not have bit 21 (PORRS_recovery_write) value equal to 1. Recovery code reads PORRR and knows that request hit an error as reflected in the PORE_suspended bit, and thus deconfigures those cores/chiplets and writes PORRS with the value read from PORRR which includes a 1 value in bit 21 (from PORRR_PORE_suspended) for the PORRS_recovery_write indication so that this manual write of PORRS succeeds in clearing PORE_busy and PORE_suspended allowing another assist = 1 request to be serviced by the PMC. If recovery code reads PORRR and PORRR.PORE_suspended = 0, it knows that the request does not need recovering from.
22	ROX	ROX	PORRR_PORRTC_BUSY: Value of porrtc_busy (for debug). 1 - Indicates that the request in PORRR is currently not finished, PORRS has not been written, and the timeout counter waiting on the PORRS write is currently counting.

Register Name	PMC PORE Request Register 1 (PORRR1)
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_PORE_REQ_REG1
Address	00000000006208F (PIB) 0000000040010478 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0	ROX	ROX	PORRR_CHIPLET_ENABLE_0: When set, indicates that PMC is requesting PORE to perform the execution trigger for chiplet 0
1	ROX	ROX	PORRR_CHIPLET_ENABLE_1: When set, indicates that PMC is requesting PORE to perform the execution trigger for chiplet 1
2	ROX	ROX	PORRR_CHIPLET_ENABLE_2: When set, indicates that PMC is requesting PORE to perform the execution trigger for chiplet 2
3	ROX	ROX	PORRR_CHIPLET_ENABLE_3: When set, indicates that PMC is requesting PORE to perform the execution trigger for chiplet 3
4	ROX	ROX	PORRR_CHIPLET_ENABLE_4: When set, indicates that PMC is requesting PORE to perform the execution trigger for chiplet 4
5	ROX	ROX	PORRR_CHIPLET_ENABLE_5: When set, indicates that PMC is requesting PORE to perform the execution trigger for chiplet 5
6	ROX	ROX	PORRR_CHIPLET_ENABLE_6: When set, indicates that PMC is requesting PORE to perform the execution trigger for chiplet 6
7	ROX	ROX	PORRR_CHIPLET_ENABLE_7: When set, indicates that PMC is requesting PORE to perform the execution trigger for chiplet 7
8	ROX	ROX	PORRR_CHIPLET_ENABLE_8: When set, indicates that PMC is requesting PORE to perform the execution trigger for chiplet 8
9	ROX	ROX	PORRR_CHIPLET_ENABLE_9: When set, indicates that PMC is requesting PORE to perform the execution trigger for chiplet 9

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Bits	PIB	OCI	Field Mnemonic: Description
10	ROX	ROX	PORRR_CHIPLET_ENABLE_10: When set, indicates that PMC is requesting PORE to perform the execution trigger for chiplet 10
11	ROX	ROX	PORRR_CHIPLET_ENABLE_11: When set, indicates that PMC is requesting PORE to perform the execution trigger for chiplet 11
12	ROX	ROX	PORRR_CHIPLET_ENABLE_12: When set, indicates that PMC is requesting PORE to perform the execution trigger for chiplet 12
13	ROX	ROX	PORRR_CHIPLET_ENABLE_13: When set, indicates that PMC is requesting PORE to perform the execution trigger for chiplet 13
14	ROX	ROX	PORRR_CHIPLET_ENABLE_14: When set, indicates that PMC is requesting PORE to perform the execution trigger for chiplet 14
15	ROX	ROX	PORRR_CHIPLET_ENABLE_15: When set, indicates that PMC is requesting PORE to perform the execution trigger for chiplet 15

Register Name	PMC PORE Request Status Register (PORRS)
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_PORE_REQ_STAT_REG
Address	0000000000062090 (PIB) 0000000040010480 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:7	RWX	RWX	PORRS_RESERVED0: Written with 0s
8:11	RWX	RWX	PORRS_START_VECTOR: Start_Vector 0x0 - Fast Sleep Entry 0x1 - Deep Sleep Entry 0x2 - Fast Sleep Exit 0x3 - Deep Sleep Exit 0x4 - Fast Winkle Entry 0x5 - Deep Winkle Entry 0x6 - Fast Winkle Exit 0x7 - Deep Winkle Exit 0x8 - Nap Entry 0x9 - Nap Exit 0xA to 0xF Reserved This field indicates the class of transition requested to the PORE, which is translated into an execution address vector.
12:19	RWX	RWX	PORE_RC: PORE Return Code Any non zero return code triggers the error bit 19 in the PMC local FIR. Please reference bits 32:39 to see which chiplets were being processed by PORE when it last updated this register.
20	RWX	RWX	PORRS_RESERVED1: Unimplemented
21	RWX	RWX	PORRS_RECOVERY_WRITE: Write-only pulse bit indicating to allow PORRS write to override the PORE_suspended state. Once PORE_suspended is set, all writes to PORRS without bit 21 set are blocked. NOTE: That way unexpected writes to PORRS are blocked after an error (for example, especially by the PORE after a timeout) until a user does a write with bit 21 set. Because bit 21 in PORRR is really the state of PORE_suspended, this allows error recovery code to simply read PORRR and write that same value to PORRS to resume operation, but PORE code always writes PORRS with bit 21 = 0.



Register Name	<i>The PDEMR Register Masks The Ability For A Given Chiplet To Exit From Deep Sleep Or Winkle State</i>
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_DEEP_EXIT_MASK_REG
Address	0000000000062092 (PIB) 00000000000620A0 (PIB1) 00000000000620A1 (PIB2) 0000000040010490 (OCI) 0000000040010500 (OCI1) 0000000040010508 (OCI2)
Attributes	
Description	NOTE that this register is to be used by the OCC for implementing power shift algorithms

Bits	PIB	PIB1	PIB2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	RW
1	RW	WO_AND	WO_OR	RW
2	RW	WO_AND	WO_OR	RW
3	RW	WO_AND	WO_OR	RW
4	RW	WO_AND	WO_OR	RW
5	RW	WO_AND	WO_OR	RW
6	RW	WO_AND	WO_OR	RW
7	RW	WO_AND	WO_OR	RW
8	RW	WO_AND	WO_OR	RW
9	RW	WO_AND	WO_OR	RW
10	RW	WO_AND	WO_OR	RW
11	RW	WO_AND	WO_OR	RW
12	RW	WO_AND	WO_OR	RW
13	RW	WO_AND	WO_OR	RW
14	RW	WO_AND	WO_OR	RW
15	RW	WO_AND	WO_OR	RW

Register Name	<i>PMCICPR</i>			
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_INTCHP_PSTATE_REG			
Address	0000000000062017 (PIB) 00000000400100B8 (OCI)			
Attributes				
Description	Interchip Pstate request			
Bits	PIB	OCI	Field Mnemonic: Description	
0:7	RWX	RWX	PSTATE_INTERCHIP: Pstate Request of Slave Chip	

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Register Name	PMICCMR
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_INTCHP_COMMAND_REG
Address	0000000000062014 (PIB) 00000000400100A0 (OCI)
Attributes	
Description	Provides the Means to Gracefully Halt the Interchip FSM. This allows for seamless firmware enablement and disablement of the hardware FSM.

Bits	PIB	OCI	Field Mnemonic: Description
0	RWX	RWX	INTERCHIP_RESET_IF: If set to 1, this bit causes the send_fsm, recv_fsm and capture_enable_It of the interchip interface component to be reset. Firmware must write 1 to this to reset then 0 to remove reset.
1	RWX	RWX	INTERCHIP_HALT_MSG_FSM: If set to 1, this bit causes the Msg FSM to complete any on-going operation and then halt in the idle condition
2	RWX	RWX	INTERCHIP_CLEAR_STICKY_BITS: if set to 1 all sticky bits in PMC_INTCHP_STATUS_REG are cleared.

Register Name	PMICCSR Displays The Current Status About The Interchip Interface
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_INTCHP_STATUS_REG
Address	0000000000062013 (PIB) 0000000040010098 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0	ROX	ROX	INTERCHIP_GA_ONGOING: asserted if the Global Actual protocol on the interchip interface is ongoing or queued. Note that this bit can be used as a done indicator, in case FW performs the voltage regulation using the register PMC_Global_Actual_Voltage_Reg
1	ROX	ROX	INTERCHIP_ECC_UE: if this bit gets asserted, an uncorrectable ECC error was detected by the interchip interface (only valid, if interchip_ecc_check_en=1). This bit is non-sticky and does not cause a fatal error. When PMC_INTCHP_CTRL_REG4.interchip_ecc_check_en=0, the ecc_ue indication is made available in interchip_ecc_ue but does not cause a fatal error. This is to allow for a workaround for incorrect generation or checking of ECC, and use the transmitted value as is.
2	ROX	ROX	INTERCHIP_ECC_CE: if this bit gets asserted, a correctable ECC error was detected by the interchip interface (only valid, if interchip_ecc_check_en=1)
3	ROX	ROX	INTERCHIP_PING_DETECTED: if this bit gets asserted, a ping packet was detected (valid command decode and, if enabled, valid ECC). Note: the bit is not controlled by the setting of the interchip_mode
4	ROX	ROX	INTERCHIP_PING_ACK_DETECTED: if this bit gets asserted, a ping_ack packet was detected (valid command decode and, if enabled, valid ECC). Note: the bit is not controlled by the setting of the interchip_mode
5	ROX	ROX	INTERCHIP_MSG_SEND_ONGOING: asserted upon a write to PMICMWD to indicate a Msg transaction on the interchip interface is ongoing or queued. Note that this bit can be used as a done indicator. Hardware resets the bit when a Msg Ack packet is detected.
6	ROX	ROX	INTERCHIP_MSG_RECV_DETECTED: if this bit gets asserted, a msg packet was received (valid command decode and, if enabled, valid ECC) and the message frame is in PMICMRD,. Upon reading of PMICMRD, this bit is reset.

Bits	PIB	OCI	Field Mnemonic: Description
7	ROX	ROX	INTERCHIP_FSM_ERR: Indicates a catastrophic FSM error in the interchip control FSM. This bit is cleared when interchip_clear_sticky_bits = 1.
8:15	ROX	ROX	INTERCHIP_PING_DETECT_COUNT: Count of the number of ping type packets detected. This count wraps upon maximum value and reset only by setting interchip_ping_detect_clear. If interchip_mode = 0 (slave), this counts the number of ping packets detected
16:19	ROX	ROX	INTERCHIP_SLAVE_ERROR_CODE: Captures bits 4:7 (ErrCode) of a received Error packet. bit16: always 0 bit17: occ heartbeat timeout bit18: gpsa timeout bit19: ECC UE error This bits are cleared when interchip_clear_sticky_bits = 1.
20	ROX	ROX	INTERCHIP_MSG_SND_OVERFLOW_DETECTED: if this bit gets asserted, a write to PMC_INTCHP_MSG_WDATA_REG to start a send has occurred when a previous one was still in the queue. This bit is cleared when interchip_halt_msg_fsm = 1.
21	ROX	ROX	INTERCHIP_MSG_RCV_OVERFLOW_DETECTED: if this bit is 1, a msg frame is received while interchip_ping_detected is currently set. Enabled by interchip_msg_rcv_overflow_check_en in PMCIC4. This bit is cleared when interchip_halt_msg_fsm = 1.
22	ROX	ROX	INTERCHIP_ECC_UE_ERR: if this bit gets asserted, an uncorrectable ECC error was detected by the interchip interface (only gets set, if interchip_ecc_check_en=1). This bit is sticky and causes a fatal error. This bit is cleared when interchip_clear_sticky_bits = 1.

Register Name	<i>PMCIC1 Provides Control Bits for the Interchip Interface</i>
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_INTCHP_CTRL_REG1
Address	0000000000062010 (PIB) 0000000040010080 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0	RW	RW	INTERCHIP_GA_FSM_ENABLE: if 1, the PMC FSM that performs Pstate sequencing to produce interchip writes for voltage movement is enabled. Note that the bridge access and accesses by the Pstate sequencer to the interchip master are arbitrated. If 0, the PMC FSM is forced to the reset stage and will not perform any interchip operations. Note: if the FSM is presently active, the hard reset can truncate on-going operations and leave the interchip in an indeterminate state. See interchip_halt bit.
1	RW	RW	INTERCHIP_RECV_DONE_VALID_WITHOUT_IF_EN: CHKSW_HW226422 0 = interchip_recv_done only gets active when PMC_MODE_REG.enable_interchip_interface = 1 1 = interchip_recv_done does not require interface enabled
2	RW	RW	PMCIC1_RESERVED_2: Reserved for clock polarity. Only CPOL=0 is supported.
3	RW	RW	INTERCHIP_CPHA: interchip clock phase (CPHA=0 means to change/sample values of data signals on the first edge, otherwise on second edge)

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Bits	PIB	OCI	Field Mnemonic: Description
4:13	RW	RW	INTERCHIP_CLOCK_DIVIDER: Interchip clock speed divider to divide the nest_nclk/4 mesh clock, which results in a divider = (nest_freq/ (interchip_freq*8))-1 For a 2.4 GHz nest clock, this means that the interchip clk can be theoretically adjusted between 300 MHz and 0.29 MHz (cycle time 1.66 ns...3.41 us, in 1.66 ns steps). However, due to some constraints, a practical range is 0.5...75 MHz. Allowed values: 0x003...0x3FF Due to metastability constraints, only use values > 2 for interchip_clock_divider, otherwise data will not be sampled correctly!
14:17	RW	RW	PMICR1_RESERVED_14_17: Reserved for Number of Frames
18:20	RW	RW	PMICR1_RESERVED_18_20: Reserved for Port Enable

Register Name	PMIC4 Provides Control Bits for the Checking Behavior of the Interchip Interface
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_INTCHP_CTRL_REG4
Address	0000000000062012 (PIB) 0000000040010090 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0	RW	RW	INTERCHIP_ECC_GEN_EN: enable ECC generation. This will produce an 8-bit ECC of an assumed 64-bit payload using 64/72 SEC/DED encoding. If ECC generation is disabled, the contents of that byte depends on the command.
1	RW	RW	INTERCHIP_ECC_CHECK_EN: enable ECC checking of the 8-bit ECC of an assumed 64-bit payload using 64/72 SEC/DED encoding. If ECC checking is disabled, the check is reflected in the PMC_INTCHP_STATUS_REG.interchip_ecc_ue and .interchip_ecc_ce bits, but the raw uncorrected read data is used/available and it is not considered an error.
2	RW	RW	INTERCHIP_MSG_RCV_OVERFLOW_CHECK_EN: if this bit is 1, if a msg frame is received while interchip_ping_detected is currently set, then interchip_msg_overflow_detected will be set. if this bit is 0, the interchip_msg_rcv_overflow_detected is not set.
3	RW	RW	INTERCHIP_ECC_UE_BLOCK_EN: If this bit is 1, ECC UEs on interchip cmds received are not processed. If this bit is 0, even when a previous ECC_UE error occurred, a received cmd without ECC_UE is processed.
4	RW	RW	CHKSW_HW221732: Debug switch. Fixes a 1-cycle glitch on pmc_protocol_ongoing of slave when mps_fsm goes through its inactive state between global actual requests received back-to-back from the master. 0 = Fix enabled 1 = Fix disabled
5	RW	RW	SLAVE_OCC_TIMEOUT_FORCES_SAFE_MODE_DISABLE: Debug switch for HW221733. If this bit is 0, OccTimeout ErrorCmd from SlavePMC forces Pvsafe as GPST. If this bit is 1, OccTimeout is immediately a fatal error, GPST unchanged.
6	RW	RW	CHKSW_HW234213: Debug switch. Fixes problem when UnfreezePstate can cause interchip Arb hang. Because ErrorCmd send has its own grant, icp_err_grant = 1 must be responded to by either sending ErrorCmd or ICP_MSG_FSM_DONE releasing arb. 0 = Fix enabled (ICP_MSG_FSM_DONE branch active) 1 = Fix disabled

Bits	PIB	OCI	Field Mnemonic: Description
7	RW	RW	PMCIC4_RESERVED7: Implemented but not used.

Register Name	Basic Parameters Of Operation For PMC		
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_PARAMETER_REG0		
Address	0000000000062005 (PIB) 0000000040010028 (OCI)		
Attributes			
Description			

Bits	PIB	OCI	Field Mnemonic: Description
0:6	RW	RW	PSTATE_STEPSIZE: unsigned 7 bit (baby-) stepsize for Pstate transitions between the Global Pstate Actual and the Global Pstate Target. Only non-zero values are supported for this dial.
7:10	RW	RW	VRM_STEPDELAY_RANGE: Selects the resolution for the step delay count after a voltage change (decimal value N for this field divides the prv clock by $2^{(N+3)}$) A 4 bit field selects one of the the upper 16bit of a 19bit counter (16+3) incremented in the nest/4 domain
11:14	RW	RW	VRM_STEPDELAY_VALUE: Step delay after a voltage change in increments of vrm_stepdelay_range. Setting this dial to a value N causes a delay of N cycles of the divided nest clk (see dial vrm_stepdelay_range). The closed formula is as follows: Delay_seconds = vrm_stepdelay_value * ($2^{(3 + vrm_stepdelay\_range)}$) / (Nest_frequency_Hz/4))
15:20	RW	RW	HANGPULSE_PREDIVIDER: this dial divides the tp_occ_hang_pulse hang pulse for the OCC heartbeat counter in PMC. Note that this needs to be set according to the description of dial pmc_occ_heartbeat_time
21:28	RW	RW	GPSA_TIMEOUT_VALUE: Global Pstate Actual Acknowledge Timeout Time in which all Global Actual Acknowledges must be received tp_occ_hang_pulse_time = ~1us (853ns) Time is computed as: (value * tp_occ_hang_pulse_time) +0/-1 tp_occ_hang_pulse_time 0x00 - Timer disabled 0x01 - 0xFF: value = number of tp_occ_hang_pulses
29	RW	RW	GPSA_TIMEOUT_VALUE_SEL: When 1, use tp_occ_hang_pulse_time * 64 for gpsa timeout

Register Name	PMC O2PCSR Register Controls The Function of the PMC O2P Bridge And Provides Status Of It		
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_O2P_CTRL_STATUS_REG		
Address	0000000000062061 (PIB) 0000000040010308 (OCI)		
Attributes			
Description			

Bits	PIB	OCI	Field Mnemonic: Description
0	ROX	ROX	O2P_ONGOING: Indicates that a bridge transaction is in progress of being executed. This bit is set by hardware while an operation is in progress and will be be reset by hardware when the operation is complete.
1:3	ROX	ROX	O2P_SCRESP: Captured sc_resp Error Code from the PIB Transaction

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Bits	PIB	OCI	Field Mnemonic: Description
4	ROX	ROX	O2P_WRITE_WHILE_BRIDGE_BUSY_ERR: Indicates that firmware attempted to perform an OCI Write to either the PMC_O2P_ADDRESS_REG, PMC_SEND_DATA_HI_REG or PMC_SEND_DATA_LO_REG while the O2P bridge is busy causing undefined bridge behavior (data corruption). Sticky.
5	ROX	ROX	O2P_FSM_ERR: Indicates a catastrophic FSM error in the OCI2PIB control FSM. Sticky.
6	ROX	ROX	O2P_ABORT: Indicates an aborted bridge transaction
7	ROX	ROX	O2P_PARITY_ERROR: Indicates that a parity error has occurred on the O2P bridge
8	RWX	RWX	O2P_CLEAR_STICKY_BITS: if set to 1 all sticky bits in O2P_CTRL_STATUS_REG are cleared.

Register Name	<i>PMCSR0A Provides The Length Control Information for the First of the P2S Frames</i>
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_SPIV_CTRL_REG0A
Address	0000000000062040 (PIB) 0000000040010200 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:5	RW	RW	SPIVID_FRAME_SIZE: Number of data bits per individual SPI transaction (also referred to as frame) during chip select assertion Supported values: 0x20 (32d) Chip Select assertion duration is spi_frame_size + 2
6:11	RW	RW	SPIVID_OUT_COUNT1: Number of bits sent out MOSI in frame 1 of a 2 frame set (the arbitration unit) Supported values: 0x00 to spi_frame_size. Values beyond spi_frame_size are ignored.
12:17	RW	RW	SPIVID_IN_DELAY1: Number of SPI clocks after chip select to wait before capturing MISO input in frame 1 Supported values: 0x00 to spi_frame_size. Values beyond spi_frame_size result in the input never being captured
18:23	RW	RW	SPIVID_IN_COUNT1: Number of bits captured on MISO input in frame 1 Supported values: 0x00 to spi_frame_size. The actual number of bits captured is spi_frame_size - spi_in_delay

Register Name	<i>PMCSR0B Provides The Length Control Information for the Second of the P2S Frames</i>
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_SPIV_CTRL_REG0B
Address	0000000000062041 (PIB) 0000000040010208 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:5	RW	RW	SPIVID_OUT_COUNT2: Number of bits sent out MOSI in frame 2 of a 2 frame set (the arbitration unit) Supported values: 0x00 to spi_frame_size. Values beyond spi_frame_size are ignored.

Bits	PIB	OCI	Field Mnemonic: Description
6:11	RW	RW	SPIVID_IN_DELAY2: Number of SPI clocks after chip select to wait before capturing MISO input in frame 2 Supported values: 0x00 to spi_frame_size. Values beyond spi_frame_size result in the input never being captured
12:17	RW	RW	SPIVID_IN_COUNT2: Number of bits captured on MISO input in frame 2 Supported values: 0x00 to spi_frame_size. The actual number of bits captured is spi_frame_size - spi_in_delay

Register Name	<i>PMCSR1 Provides All Control Bits for the Redundant SPI Interface</i>
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_SPIV_CTRL_REG1
Address	0000000000062042 (PIB) 0000000040010210 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0	RW	RW	SPIVID_FSM_ENABLE: If 1, the PMC FSM that performs Pstate sequencing to produce SPIVID writes for voltage movement is enabled. Note that the bridge access and accesses by the Pstate sequencer to the SPI master are arbitrated. If 0, the PMC FSM is forced to the reset stage and does not perform any SPIVID operations. Note: if the FSM is presently active, the hard reset can truncate on-going operations and leave the SPIVID in an indeterminate state. See spivd_halt bit.
1	RW	RW	PMCSR1_RESERVED_1: Reserved for device control (up to 2 devices)
2	RW	RW	SPIVID_CPOL: SPI clock polarity (CPOL = 0 means that clk idle is deasserted, CPOL = 1 means that clk idle is asserted)
3	RW	RW	SPIVID_CPHA: SPI clock phase (CPHA = 0 means to change/sample values of data signals on the first edge; otherwise, on the second edge).
4:13	RW	RW	SPIVID_CLOCK_DIVIDER: SPI clock speed divider to divide the nest_nclk/4 mesh clock, which results in a divider = (nest_freq/ (SPI_freq*8))-1 For a 2.4GHz nest clock, this means that the SPI clk can be theoretically adjusted between 300MHz and 0.29MHz (cycle time 1.66ns...3.41us, in 1.66ns steps). However, due to some constraints, a practical range is 0.5...75MHz. Allowed values: 0x003...0x3FF Due to metastability constraints, only use values > 2 for spivd_clock_divider, otherwise data will not be sampled correctly!
14:17	RW	RW	PMCSR1_RESERVED_2: Reserved for Number of Frames
18:20	RW	RW	SPIVID_PORT_ENABLE: a 1 (0) in bit N (N=0,1,2) means that the SPI port N is configured to be used (not used) for redundant SPI operation. Note that at least one port needs to be enabled in order for the SPI function to work properly.

Register Name	<i>PMCSR2 Provides All Control Bits for the Redundant SPI Interface</i>
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_SPIV_CTRL_REG2
Address	0000000000062043 (PIB) 0000000040010218 (OCI)
Attributes	
Description	

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Bits	PIB	OCI	Field Mnemonic: Description
0:16	RW	RW	SPIVID_INTER_FRAME_DELAY_WRITE_STATUS: Delay between two frames of a Write command as measured from the end of the last bit of the first frame until the chip select of the second frame, which contains the status, is asserted. This delay allows for the checking and status data production in the SPIVID chip. Delay is computed as: (value * ~100ns_hang_pulse) +0/~100ns_hang_pulse time 0x00000: Wait 1 SPI Clock 0x00001 - 0x1FFFF: value = number of ~100ns_hang_pulses For values greater than 0x00000, the actual delay is 1 SPI Clock + the time delay designated by the value defined. Max. delay at 0x1FFFF: 13.1ms + 1 SPI clock cycle.

Register Name	<i>PMSCSR3 Provides All Control Bits for the Redundant SPI Interface</i>
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_SPIV_CTRL_REG3
Address	0000000000062044 (PIB) 0000000040010220 (OCI)
Attributes	
Description	Valid for O2S as well

Bits	PIB	OCI	Field Mnemonic: Description
0:16	RW	RW	SPIVID_INTER_RETRY_DELAY: Delay between command retry attempts. Delay is computed as: (value * ~100ns_hang_pulse) +0/~100ns_hang_pulse time 0x0000: Wait 1 SPI Clock 0x0001 - 0xFFFF: value = number of ~100ns_hang_pulses For values greater than 0x00000, the actual delay is 1 SPI Clock + the time delay designated by the value defined. Max. delay at 0x1FFFF: 13.1ms + 1 SPI clock cycle.
17:22	RW	RW	PMC_100NS_PLS_RANGE: The content of this register controls the period length of the 100ns pulse used for the inter_frame_delay and inter_retry_delay counters. The formula for the period is as follows: $pmc\_100ns\_pls\_ns = (pmc\_100ns\_pls\_range + 1) / (Nest\_frequency\_Hz/4)$ To maintain a period of exactly 100ns, set this register as follows: $pmc\_100ns\_pls\_range = (100ns * (Nest\_frequency\_Hz/4)) - 1$ Examples: for 1.6GHz nest freq.: 0d39 = 0b100111 for 2.4GHz nest freq.: 0d59 = 0b111011

Register Name	<i>PMSCSR4 Provides Control Bits for the Checking Behavior of the Redundant SPI Interface</i>
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_SPIV_CTRL_REG4
Address	0000000000062045 (PIB) 0000000040010228 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0	RW	RW	SPIVID_CRC_GEN_EN: enable CRC generation. This produces an 8-bit CRC per the enabled polynomial. If CRC generation is disabled, the full 32 bits at the data input of the SPI master are transmitted.
1	RW	RW	SPIVID_CRC_CHECK_EN: enable CRC check, NOTE that this is only supported, if spivd_frame_size is set correctly (to 32d)

Bits	PIB	OCI	Field Mnemonic: Description
2	RW	RW	SPIVID_MAJORITY_VOTE_EN: Enables a majority vote on the 3 bytes of status payload on a frame received by the master as each of these have a 1 byte status field replicated three (3) times by the slave.
3:7	RW	RW	SPIVID_MAX_RETRIES: Number retries upon detected errors. 0x00: No retry 0x01 - 0x1F: 1 - 31 respectively.
8:15	RW	RW	SPIVID_CRC_POLYNOMIAL_ENABLES: CRC8 polynomial enables. 8-bit mask vector to enable XORs in the CRC generation and checking LFSRs at the respective bit position. MSB (x ⁸) is omitted, because it is always enabled, so that the mask layout is (x ⁷ ,x ⁶ ,x ⁵ ,x ⁴ ,x ³ ,x ² ,x ¹ ,1) Planned CRC8 polynomial: x ⁸ + x ⁷ + x ⁶ + x ⁴ + x ² + 1 Value to enable planned polynomial: 0b1101_0101 (=0xD5)
16	RW	RW	SPIVID_CRC_CONST_GEN_ENABLE: When set to a 1, the hardware causes constant value 0x9B to be sent in Frame1 crc field instead of calculated crc when crc_gen_en = 1.
17	RW	RW	SPIVID_CRC_CONST_CHECK_ENABLE: When set to a 1, the hardware checks the crc field (that is, bits 24:31) of the received frame against constant 0xD6 when crc_check_en = 1.
18	RW	RW	SPIVID_FRAME_SYNC_WRONG_ENABLE: When set to a 1, the hardware checks for frames getting out of sync.
19	RW	RW	CHKSW_HW240494: Debug switch for HW240494. 0: crc_error latch in the spivid master is cleared when spivid_crc_check_en=0 or when PMC_MODE_REG.spivid_reset_if = 1 1: crc_error latch in the spivid master is not cleared

Register Name	<i>PMCSSR Displays The Current Status About SPI-related Activities</i>
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_SPIV_STATUS_REG
Address	0000000000062046 (PIB) 0000000040010230 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0	ROX	ROX	SPIVID_ONGOING: asserted if an outstanding transaction for the SPIVID interface is ongoing or queued. Note that this bit can be used as a done indicator, in case FW performs the voltage regulation using the register PMC_Global_Actual_Voltage_Reg
1	ROX	ROX	SPIVID_CRC_ERROR0: if this bit gets asserted, a crc error was detected by the SPI master interface for SPIVID link 0 (only valid, if spivid_crc_check_en=1)
2	ROX	ROX	SPIVID_CRC_ERROR1: if this bit gets asserted, a crc error was detected by the SPI master interface for SPIVID link 1 (only valid, if spivid_crc_check_en=1)
3	ROX	ROX	SPIVID_CRC_ERROR2: if this bit gets asserted, a crc error was detected by the SPI master interface for SPIVID link 2 (only valid, if spivid_crc_check_en=1)
4	ROX	ROX	SPIVID_RETRY_TIMEOUT: if this bit gets asserted, the number of unsuccessful retries has reached the value specified in spivid_max_retries.
5:6	ROX	ROX	PMCSSR_RESERVED_1: Implemented but not used
7	ROX	ROX	SPIVID_FSM_ERR: Indicates a catastrophic FSM error in the SPIVID control FSM
8	ROX	ROX	SPIVID_MAJORITY_DETECTED_A_MINORITY0: if this bit gets asserted, one or more bits across the checked bytes of link0 have a minority present

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Bits	PIB	OCI	Field Mnemonic: Description
9	ROX	ROX	SPIVID_MAJORITY_DETECTED_A_MINORITY1: If this bit gets asserted, one or more bits across the checked bytes of link1 have a minority present
10	ROX	ROX	SPIVID_MAJORITY_DETECTED_A_MINORITY2: If this bit gets asserted, one or more bits across the checked bytes of link2 have a minority present
11:14	ROX	ROX	SPIVID_MAJORITY_NR_OF_MINORITIES0: Number of bits across the checked bytes of link0 with a detected minority. Valid only if spivid_majority_vote_en = '1'.
15:18	ROX	ROX	SPIVID_MAJORITY_NR_OF_MINORITIES1: Number of bits across the checked bytes of link1 with a detected minority. Valid only if spivid_majority_vote_en = '1'.
19:22	ROX	ROX	SPIVID_MAJORITY_NR_OF_MINORITIES2: Number of bits across the checked bytes of link2 with a detected minority. Valid only if spivid_majority_vote_en = '1'.

Register Name	<i>PMCSCMR Provides The Means To Gracefully Halt The SPIVID FSM</i>
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_SPIV_COMMAND_REG
Address	0000000000062047 (PIB) 0000000040010238 (OCI)
Attributes	
Description	This allows for seamless firmware enablement and disablement of the hardware FSM.

Bits	PIB	OCI	Field Mnemonic: Description
0	RWX	RWX	SPIVID_HALT_FSM: If set to 1 and spivid_fsm_enable = 1, this bit causes the FSM to complete any on-going operation (frame set) and then is halted in the idle condition

Register Name	<i>PMCOCR0A Provides The Length Control Information for the First of the P2S Frames</i>
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_O2S_CTRL_REG0A
Address	0000000000062050 (PIB) 0000000040010280 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:5	RW	RW	O2S_FRAME_SIZE: Number of data bits per individual SPI transaction (also referred to as frame) during chip select assertion Supported values: 0x20 (32d) Chip Select assertion duration is spi_frame_size + 2
6:11	RW	RW	O2S_OUT_COUNT1: Number of bits sent out MOSI in frame 1 of a 2 frame set (the arbitration unit) Supported values: 0x00 to spi_frame_size. Values beyond spi_frame_size are ignored.
12:17	RW	RW	O2S_IN_DELAY1: Number of SPI clocks after chip select to wait before capturing MISO input in frame 1 Supported values: 0x00 to spi_frame_size. Values beyond spi_frame_size result in the input never being captured
18:23	RW	RW	O2S_IN_COUNT1: Number of bits captured on MISO input in frame 1 Supported values: 0x00 to spi_frame_size. The actual number of bits captured is spi_frame_size - spi_in_delay

Register Name	<i>PMCOCR0B Provides The Length Control Information for the Second of the P2S Frames</i>
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_O2S_CTRL_REG0B
Address	0000000000062051 (PIB) 0000000040010288 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:5	RW	RW	O2S_OUT_COUNT2: Number of bits sent out MOSI in frame 2 of a 2 frame set (the arbitration unit) Supported values: 0x00 to spi_frame_size. Values beyond spi_frame_size are ignored.
6:11	RW	RW	O2S_IN_DELAY2: Number of SPI clocks after chip select to wait before capturing MISO input in frame 2 Supported values: 0x00 to spi_frame_size. Values beyond spi_frame_size result in the input never being captured
12:17	RW	RW	O2S_IN_COUNT2: Number of bits captured on MISO input in frame 2 Supported values: 0x00 to spi_frame_size. The actual number of bits captured is spi_frame_size - spi_in_delay

Register Name	<i>PMCOCR1 Provides Control Bits for the P2S Bridge Interface (note That This Interface Does Not Support CRC)</i>
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_O2S_CTRL_REG1
Address	0000000000062052 (PIB) 0000000040010290 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0	RW	RW	O2S_BRIDGE_ENABLE: if 1 the OCI2SPI bridge can be used to control the SPI interface If 0, the OCI2SPI is forced to the reset state. Note: if the Bridge is presently active (os2_in_progress+E147 = 1, the hard reset can truncate on-going operations and leave the SPIVID in an indeterminate state.
1	RW	RW	PMCOCR1_RESERVED_1: Implemented but not used.
2	RW	RW	O2S_CPOL: SPI clock polarity (CPOL=0 means that clk idle is deasserted, CPOL=1 means that clk idle is asserted)
3	RW	RW	O2S_CPHA: SPI clock phase (CPHA=0 means to change/sample values of data signals on first edge; otherwise on the second edge).
4:13	RW	RW	O2S_CLOCK_DIVIDER: SPI clock speed divider to divide the nest_nclk/4 mesh clock, that results in a divider = (nest_freq/ (SPI_freq*8)) - 1 For a 2.4 GHz nest clock, this means that the SPI clk can be theoretically adjusted between 600 MHz and 0.29 MHz (cycle time 1.66 ns...3.41us, in 1.66 ns steps). However, a practical range is 0.5...25 MHz.
14:16	RW	RW	PMCOCR1_RESERVED_2: Reserved for Number of Frames.
17	RW	RW	O2S_NR_OF_FRAMES: Specifies the number of frames sent in the frame set (# of frames before the arbitration unit rearbiterates). 0: 1 frame 1: 2 frames

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Bits	PIB	OCI	Field Mnemonic: Description
18:20	RW	RW	O2S_PORT_ENABLE: enable vector for SPI port 0, 1, and 2. Note that the PMC_O2S_RCV_DATA registers are only valid, if this vector enables exactly one SPI port.

Register Name	PMCOCR2 Provides All Control Bits for the SPI ADC Interface (note: This Interface Does Not Support ECC)		
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_O2S_CTRL_REG2		
Address	0000000000062053 (PIB) 0000000040010298 (OCI)		
Attributes			
Description			

Bits	PIB	OCI	Field Mnemonic: Description
0:16	RW	RW	O2S_INTER_FRAME_DELAY: Delay between two frames of a two command set as measured from the end of the last bit of the first frame until the chip select of the second frame is asserted. Delay is computed as: (value * ~100ns_hang_pulse) +0/~100ns_hang_pulse time 0x00000: Wait 1 SPI Clock 0x00001 - 0x1FFFF: value = number of ~100ns_hang_pulses For values greater than 0x00000, the actual delay is 1 SPI Clock + the time delay designated by the value defined. Max. delay at 0x1FFFF: 13.1ms + 1 SPI clock cycle.

Register Name	PMCOCR4 Provides Control Bits for the Checking Behavior of the Redundant SPI Interface		
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_O2S_CTRL_REG4		
Address	0000000000062055 (PIB) 00000000400102A8 (OCI)		
Attributes			
Description	Valid for O2S as well.		

Bits	PIB	OCI	Field Mnemonic: Description
0	RW	RW	O2S_CRC_GEN_EN: enable CRC generation. This will produce an 8-bit CRC per the enabled polynomial. If CRC generation is disabled, the full 32 bits at the data input of the SPI master are transmitted.
1	RW	RW	O2S_CRC_CHECK_EN: enable CRC check, NOTE that this is only supported, if o2s_frame_size is set correctly (to 32d)
2	RW	RW	O2S_MAJORITY_VOTE_EN: enables the a majority vote on the 3B of payload on a frame received by the master (Write Command Status frame or Read State frame) as each of these have a 1 byte field replicated three (3) times by the slave.
3:7	RW	RW	O2S_MAX_RETRIES: Number retries upon detected errors. 0x00: No retry 0x01 to 0x1F: 1 to 31 respectively
8:15	RW	RW	PMCOCR4_RESERVED8_15: unused



Register Name	<i>PMCOSR Displays The Current Status About SPI-related Activities</i>
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_O2S_STATUS_REG
Address	0000000000062056 (PIB) 00000000400102B0 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0	ROX	ROX	O2S_ONGOING: Indicates that a bridge transaction is in progress of being executed. This bit is set by hardware while an operation is in progress and will be reset by hardware when the operation is complete.
1	ROX	ROX	O2S_CRC_ERROR0: if this bit gets asserted, a crc error was detected by the SPI master interface for SPIVID link 0 (only valid, if spivid_crc_check_en=1)
2	ROX	ROX	O2S_CRC_ERROR1: if this bit gets asserted, a crc error was detected by the SPI master interface for SPIVID link 1 (only valid, if spivid_crc_check_en=1)
3	ROX	ROX	O2S_CRC_ERROR2: if this bit gets asserted, a crc error was detected by the SPI master interface for SPIVID link 2 (only valid, if spivid_crc_check_en=1)
4	ROX	ROX	O2S_RETRY_TIMEOUT: if this bit gets asserted, the number of unsuccessful retries has reached the value specified in o2s_max_retries.
5	ROX	ROX	O2S_WRITE_WHILE_BRIDGE_BUSY_ERR: Indicates that firmware attempted to perform an PIB Write to either the PMC_O2S_R/WDATA_REG while the o2s bridge is busy, which will caused undefined bridge behavior.
6	ROX	ROX	PMCOSR_RESERVED_6: Implemented but not used
7	ROX	ROX	O2S_FSM_ERR: Indicates a catastrophic FSM error in the OCI2SPI control FSM
8	ROX	ROX	O2S_MAJORITY_DETECTED_A_MINORITY0: if this bit gets asserted, one or more bits across the checked bytes of link0 have a minority present
9	ROX	ROX	O2S_MAJORITY_DETECTED_A_MINORITY1: if this bit gets asserted, one or more bits across the checked bytes of link0 have a minority present
10	ROX	ROX	O2S_MAJORITY_DETECTED_A_MINORITY2: if this bit gets asserted, one or more bits across the checked bytes of link0 have a minority present
11:14	ROX	ROX	O2S_MAJORITY_NR_OF_MINORITIES0: Number of bits across the checked bytes of link0 with a detected minority. Valid only if spivid_majority_vote_en = '1'.
15:18	ROX	ROX	O2S_MAJORITY_NR_OF_MINORITIES1: Number of bits across the checked bytes of link0 with a detected minority. Valid only if spivid_majority_vote_en = '1'.
19:22	ROX	ROX	O2S_MAJORITY_NR_OF_MINORITIES2: Number of bits across the checked bytes of link0 with a detected minority. Valid only if spivid_majority_vote_en = '1'.

Register Name	<i>PMCOCMR Provides The Means To Control Retries of the O2S Bridge And Clear The Sticky Bits In PMCOSR</i>
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_O2S_COMMAND_REG
Address	0000000000062057 (PIB) 00000000400102B8 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0	RW	RW	O2S_HALT_RETRIES: if set to 1 no more retries will be done by the o2s bridge.

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Bits	PIB	OCI	Field Mnemonic: Description
1	RWX	RWX	O2S_CLEAR_STICKY_BITS: if set to 1 all sticky bits in O2S_STATUS_REG are cleared.

Register Name	<i>PO2SWR Register Is Used For Sending 3B Of Write Data Through The O2s Bridge</i>		
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_O2S_WDATA_REG		
Address	0000000000062058 (PIB) 00000000400102C0 (OCI)		
Attributes			
Description	Note that a write to this register starts the SPI transaction (read or write), if the switch enable_o2s_bridge is set.		

Bits	PIB	OCI	Field Mnemonic: Description
0:31	RW	RW	O2S_WDATA: Bits 0 to 23 are the SPI send data packet

Register Name	<i>PO2SRR Register Is Used for the Read Data of the O2s Bridge</i>		
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_O2S_RDATA_REG		
Address	0000000000062059 (PIB) 00000000400102C8 (OCI)		
Attributes			
Description	After the o2s_ongoing bit has dropped, the read values are available in PO2SRR.		

Bits	PIB	OCI	Field Mnemonic: Description
0:31	ROX	ROX	O2S_RDATA: 8 bit SPI receive data packet, duplicated in bits 8..15 and 16..23., plus 8 bit CRC. CRC is checked in SPI master if spivid_crc_check_en = 1. If spivid_majority_vote_en = 1, bits 0..7, contain the corrected result, duplicated in bits 8..15 and 16..23.

Register Name	<i>TP PMC FIR Error Register</i>		
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_LFIR_ERR_REG		
Address	0000000001010840 (SCOM) 0000000001010841 (SCOM1) 0000000001010842 (SCOM2)		
Attributes			
Description			

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	LFIR_PSTATE_OCI_MASTER_RDERR: OCI Read Error for Pstate operation A Global Pstate Read operation received a Read Error indication on the OCI.
1	RWX	WOX_AND	WOX_OR	LFIR_PSTATE_OCI_MASTER_RDDATA_PARITY_ERR: OCI Read Date Parity Error for Pstate operation A Global Pstate Read operation detected bad parity on the OCI data.



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
2	RWX	WOX_AND	WOX_OR	LFIR_PSTATE_GPST_CHECKBYTE_ERR: Global Pstate Table Check Byte Error The check byte in the Global Pstate Table indicates the contents are inconsistent and typically indicates an erroneous store has occurred to the table in SRAM.
3	RWX	WOX_AND	WOX_OR	LFIR_PSTATE_GACK_TO_ERR: Global Actual Acknowledge Timeout Error Indicates that not all Global Actual Acks were received in the time defined by dial gpsa_timeout_value
4	RWX	WOX_AND	WOX_OR	LFIR_PSTATE_PIB_MASTER_NONOFFLINE_ERR: PIB Master Non-Offline Error for Pstate operation Indicates that a PIB Master operation from the Pstate macro detected a non-offline error response on the PIB bus.
5	RWX	WOX_AND	WOX_OR	LFIR_PSTATE_PIB_MASTER_OFFLINE_ERR: PIB Master Offline Error for Pstate operation Indicates that a PIB Master operation from the Pstate macro detected an offline error response on the PIB bus.
6	RWX	WOX_AND	WOX_OR	LFIR_PSTATE_OCI_MASTER_TO_ERR: PIB OCI Master Timeout Error for Pstate operation Indicates that a PIB Master operation from the Pstate macro detected a timeout error response on the PIB bus.
7	RWX	WOX_AND	WOX_OR	LFIR_PSTATE_INTERCHIP_UE_ERR: Interchip Uncorrectable Error for Pstate operation Indicates that the interchip interface detected an uncorrectable error.
8	RWX	WOX_AND	WOX_OR	LFIR_PSTATE_INTERCHIP_ERRORFRAME_ERR: Interchip Error Frame Detect for Pstate operation Indicates that the interchip interface detected an error frame. This occurs when the other chip has detected an error in which it cannot be considered reliable.
9	RWX	WOX_AND	WOX_OR	LFIR_PSTATE_MS_FSM_ERR: Register Parity Error for ms component Indicates that a register in the mds component detected incorrect parity.
10	RWX	WOX_AND	WOX_OR	LFIR_MS_COMP_PARITY_ERR: Register Parity Error for ms component Indicates that a register in the mds component detected incorrect parity.
11	RWX	WOX_AND	WOX_OR	LFIR_IDLE_PORESW_FATAL_ERR: PORE-SW Fatal Error The PORE-SW engine detected a fatal error during processing of an assisted idle operation.
12	RWX	WOX_AND	WOX_OR	LFIR_IDLE_PORESW_STATUS_RC_ERR: PORE-SW Status Return Code Error The assisted idle operation program running on the PORE-SW wrote a non-zero return code in the PMC_PORE_REQ_STAT_REG register.
13	RWX	WOX_AND	WOX_OR	LFIR_IDLE_PORESW_STATUS_VALUE_ERR: PORE-SW Statue Value Error The value written back by the assisted idle operation program running on the PORE-SW to the in the PMC_PORE_REQ_STAT_REG register did not match the request in PMC_PORE_REQ_REG0.
14	RWX	WOX_AND	WOX_OR	LFIR_IDLE_PORESW_WRITE_WHILE_INACTIVE_ERR: PORE-SW Write While Inactive Error The assisted idle operation program that was to run on the PORE-SW engine has written back to the PMC_PORE_REQ_STAT_REG when no assisted idle operation was active in PMC

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
15	RWX	WOX_AND	WOX_OR	LFIR_IDLE_PORESW_TIMEOUT_ERR: PORE-SW Timeout Error The assisted idle operation program that was to run on the PORE-SW engine did not write back to the PMC_PORE_REQ_STAT_REG in the time defined by dial PORRTT_timeout_threshold
16	RWX	WOX_AND	WOX_OR	LFIR_IDLE_OCI_MASTER_WRITE_TIMEOUT_ERR: OCI Write Timeout Error An OCI Write received an OCI Timeout from the OCI arbiter.
17	RWX	WOX_AND	WOX_OR	LFIR_IDLE_INTERNAL_ERR: Idle Internal Error An error was detected in the Idle macro FSM.
18	RWX	WOX_AND	WOX_OR	LFIR_INT_COMP_PARITY_ERR: Register Parity Error for int component Indicates that a register in the int component detected incorrect parity.
19	RWX	WOX_AND	WOX_OR	LFIR_PMC_OCC_HEARTBEAT_TIMEOUT: PMC OCC Heartbeat Timeout Indicates that a read of the PMCSR was not done in the time defined by dial pmc_occ_heartbeat_time
20	RWX	WOX_AND	WOX_OR	LFIR_SPIVID_CRC_ERROR0: Voltage Change Sequencer OP: SPI Master CRC Error - Link 0 A crc error was detected by the SPI master interface for SPIVID link 0 during a data transfer from the voltage change sequencer
21	RWX	WOX_AND	WOX_OR	LFIR_SPIVID_CRC_ERROR1: Voltage Change Sequencer OP: SPI Master CRC Error - Link 1 A crc error was detected by the SPI master interface for SPIVID link 1 during a data transfer from the voltage change sequencer
22	RWX	WOX_AND	WOX_OR	LFIR_SPIVID_CRC_ERROR2: Voltage Change Sequencer OP: SPI Master CRC Error - Link 2 A crc error was detected by the SPI master interface for SPIVID link 2 during a data transfer from the voltage change sequencer
23	RWX	WOX_AND	WOX_OR	LFIR_SPIVID_RETRY_TIMEOUT: The number of unsuccessful retries of data transfers from the master sequencer has reached the value specified in spivid_max_retries.
24	RWX	WOX_AND	WOX_OR	LFIR_SPIVID_FSM_ERR: Fatal error of Voltage Change Sequencer Finite State Machine (svs_fsm)
25	RWX	WOX_AND	WOX_OR	LFIR_SPIVID_MAJORITY_DETECTED_A_MINORITY: One or more bits across the checked bytes of link0, 1, or 2 have a minority present
26	RWX	WOX_AND	WOX_OR	LFIR_O2S_CRC_ERROR0: O2S Bridge OP: SPI Master CRC Error - Link 0 A crc error was detected by the SPI master interface for SPIVID link 0 during a data transfer from the O2S bridge
27	RWX	WOX_AND	WOX_OR	LFIR_O2S_CRC_ERROR1: O2S Bridge OP: SPI Master CRC Error - Link 1 A crc error was detected by the SPI master interface for SPIVID link 0 during a data transfer from the O2S bridge
28	RWX	WOX_AND	WOX_OR	LFIR_O2S_CRC_ERROR2: O2S Bridge OP: SPI Master CRC Error - Link 2 A crc error was detected by the SPI master interface for SPIVID link 0 during a data transfer from the O2S bridge
29	RWX	WOX_AND	WOX_OR	LFIR_O2S_RETRY_TIMEOUT: The number of unsuccessful retries of data transfers from the O2S bridge has reached the value specified in o2s_max_retries.



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
30	RWX	WOX_AND	WOX_OR	LFIR_O2S_WRITE_WHILE_BRIDGE_BUSY_ERR: Indicates that firmware attempted to perform an PIB Write to either the PMC_O2S_R/WDATA_REG while the o2s bridge is busy, which will caused undefined bridge behavior.
31	RWX	WOX_AND	WOX_OR	LFIR_O2S_FSM_ERR: Fatal error of O2S Bridge Finite State Machine (o2s_fsm)
32	RWX	WOX_AND	WOX_OR	LFIR_O2S_MAJORITY_DETECTED_A_MINORITY: One or more bits across the checked bytes of link0, 1, or 2 have a minority present
33	RWX	WOX_AND	WOX_OR	LFIR_O2P_WRITE_WHILE_BRIDGE_BUSY_ERR: Indicates that firmware attempted to perform an OCI Write to either the PMC_O2P_ADDRESS_REG, PMC_SEND_DATA_HI_REG or PMC_SEND_DATA_LO_REG while the O2P bridge is busy causing undefined bridge behavior (data corruption). Sticky.
34	RWX	WOX_AND	WOX_OR	LFIR_O2P_FSM_ERR: Fatal error of O2P Bridge Finite State Machine (o2p_fsm)
35	RWX	WOX_AND	WOX_OR	LFIR_OCI_SLAVE_ERR: Error from OCI Slave I/F
36	RWX	WOX_AND	WOX_OR	LFIR_IF_COMP_PARITY_ERROR: Register Parity Error for if component Indicates that a register in the if component detected incorrect parity.
37	RWX	WOX_AND	WOX_OR	IDLE_RECOVERY_NOTIFY_PRD: Used by SLW recovery firmware to indicate that the host side actions are complete and that FFDC information is available for analysis toward subsequent garding and/or deconfiguration. Intended to produce a recoverable attention (via Action register settings) to the PRD component for such analysis.
38:46	RWX	WOX_AND	WOX_OR	SPARE_FIR:
47	RWX	WOX_AND	WOX_OR	FIR_PARITY_ERR_DUP:
48	RWX	WOX_AND	WOX_OR	FIR_PARITY_ERR:

Register Name	TP PMC FIR Mask Registers
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_LFIR_ERR_MASK_REG
Address	0000000001010843 (SCOM) 0000000001010844 (SCOM1) 0000000001010845 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	PMC_LFIR_MASK_0:
1	RW	WO_AND	WO_OR	PMC_LFIR_MASK_1:
2	RW	WO_AND	WO_OR	PMC_LFIR_MASK_2:
3	RW	WO_AND	WO_OR	PMC_LFIR_MASK_3:
4	RW	WO_AND	WO_OR	PMC_LFIR_MASK_4:
5	RW	WO_AND	WO_OR	PMC_LFIR_MASK_5:
6	RW	WO_AND	WO_OR	PMC_LFIR_MASK_6:
7	RW	WO_AND	WO_OR	PMC_LFIR_MASK_7:
8	RW	WO_AND	WO_OR	PMC_LFIR_MASK_8:
9	RW	WO_AND	WO_OR	PMC_LFIR_MASK_9:



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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
10	RW	WO_AND	WO_OR	PMC_LFIR_MASK_10:
11	RW	WO_AND	WO_OR	PMC_LFIR_MASK_11:
12	RW	WO_AND	WO_OR	PMC_LFIR_MASK_12:
13	RW	WO_AND	WO_OR	PMC_LFIR_MASK_13:
14	RW	WO_AND	WO_OR	PMC_LFIR_MASK_14:
15	RW	WO_AND	WO_OR	PMC_LFIR_MASK_15:
16	RW	WO_AND	WO_OR	PMC_LFIR_MASK_16:
17	RW	WO_AND	WO_OR	PMC_LFIR_MASK_17:
18	RW	WO_AND	WO_OR	PMC_LFIR_MASK_18:
19	RW	WO_AND	WO_OR	PMC_LFIR_MASK_19:
20	RW	WO_AND	WO_OR	PMC_LFIR_MASK_20:
21	RW	WO_AND	WO_OR	PMC_LFIR_MASK_21:
22	RW	WO_AND	WO_OR	PMC_LFIR_MASK_22:
23	RW	WO_AND	WO_OR	PMC_LFIR_MASK_23:
24	RW	WO_AND	WO_OR	PMC_LFIR_MASK_24:
25	RW	WO_AND	WO_OR	PMC_LFIR_MASK_25:
26	RW	WO_AND	WO_OR	PMC_LFIR_MASK_26:
27	RW	WO_AND	WO_OR	PMC_LFIR_MASK_27:
28	RW	WO_AND	WO_OR	PMC_LFIR_MASK_28:
29	RW	WO_AND	WO_OR	PMC_LFIR_MASK_29:
30	RW	WO_AND	WO_OR	PMC_LFIR_MASK_30:
31	RW	WO_AND	WO_OR	PMC_LFIR_MASK_31:
32	RW	WO_AND	WO_OR	PMC_LFIR_MASK_32:
33	RW	WO_AND	WO_OR	PMC_LFIR_MASK_33:
34	RW	WO_AND	WO_OR	PMC_LFIR_MASK_34:
35	RW	WO_AND	WO_OR	PMC_LFIR_MASK_35:
36	RW	WO_AND	WO_OR	PMC_LFIR_MASK_36:
37	RW	WO_AND	WO_OR	PMC_LFIR_MASK_37:
38:46	RW	WO_AND	WO_OR	PMC_LFIR_MASK1_38_46:
47	RW	WO_AND	WO_OR	PMC_LFIR_MASK1_47:
48	RW	WO_AND	WO_OR	PMC_LFIR_MASK1_48:

Register Name	TP PMC FIR Action 0 Reg
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_LFIR_ACTION0_REG
Address	0000000001010846 (SCOM)
Attributes	
Description	



Bits	SCOM	Field Mnemonic: Description
0	RW	PMC_LFIR_ACTION0_0: MSB of action select for corresponding bit in FIR (Action0, Action1, Mask) = Action Select (0,0,0) = Checkstop Error (0,1,0) = Recoverable Error (1,0,0) = Recoverable Interrupt (1,1,0) = Local Checkstop (x,x,1) = MASKED
1	RW	PMC_LFIR_ACTION0_1:
2	RW	PMC_LFIR_ACTION0_2:
3	RW	PMC_LFIR_ACTION0_3:
4	RW	PMC_LFIR_ACTION0_4:
5	RW	PMC_LFIR_ACTION0_5:
6	RW	PMC_LFIR_ACTION0_6:
7	RW	PMC_LFIR_ACTION0_7:
8	RW	PMC_LFIR_ACTION0_8:
9	RW	PMC_LFIR_ACTION0_9:
10	RW	PMC_LFIR_ACTION0_10:
11	RW	PMC_LFIR_ACTION0_11:
12	RW	PMC_LFIR_ACTION0_12:
13	RW	PMC_LFIR_ACTION0_13:
14	RW	PMC_LFIR_ACTION0_14:
15	RW	PMC_LFIR_ACTION0_15:
16	RW	PMC_LFIR_ACTION0_16:
17	RW	PMC_LFIR_ACTION0_17:
18	RW	PMC_LFIR_ACTION0_18:

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Bits	SCOM	Field Mnemonic: Description
19	RW	PMC_LFIR_ACTION0_19:
20	RW	PMC_LFIR_ACTION0_20:
21	RW	PMC_LFIR_ACTION0_21:
22	RW	PMC_LFIR_ACTION0_22:
23	RW	PMC_LFIR_ACTION0_23:
24	RW	PMC_LFIR_ACTION0_24:
25	RW	PMC_LFIR_ACTION0_25:
26	RW	PMC_LFIR_ACTION0_26:
27	RW	PMC_LFIR_ACTION0_27:
28	RW	PMC_LFIR_ACTION0_28:
29	RW	PMC_LFIR_ACTION0_29:
30	RW	PMC_LFIR_ACTION0_30:
31	RW	PMC_LFIR_ACTION0_31:
32	RW	PMC_LFIR_ACTION0_32:
33	RW	PMC_LFIR_ACTION0_33:
34	RW	PMC_LFIR_ACTION0_34:
35	RW	PMC_LFIR_ACTION0_35:
36	RW	PMC_LFIR_ACTION0_36:
37	RW	PMC_LFIR_ACTION0_37:
38:46	RW	PMC_LFIR_ACTION0_38_46:
47	RW	PMC_LFIR_ACTION0_47:
48	RW	PMC_LFIR_ACTION0_48:

Register Name	TP PMC FIR Action 1 Reg
Mnemonic	EH.TPCHIP.OCC.PMC.PMC_LFIR_ACTION1_REG
Address	0000000001010847 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	PMC_LFIR_ACTION1_0: LSB of action select for corresponding bit in FIR (Action0, Action1, Mask) = Action Select (0,0,0) = Checkstop Error (0,1,0) = Recoverable Error (1,0,0) = Recoverable Interrupt (1,1,0) = Local Checkstop (x,x,1) = MASKED
1	RW	PMC_LFIR_ACTION1_1:
2	RW	PMC_LFIR_ACTION1_2:
3	RW	PMC_LFIR_ACTION1_3:
4	RW	PMC_LFIR_ACTION1_4:
5	RW	PMC_LFIR_ACTION1_5:



Bits	SCOM	Field Mnemonic: Description
6	RW	PMC_LFIR_ACTION1_6:
7	RW	PMC_LFIR_ACTION1_7:
8	RW	PMC_LFIR_ACTION1_8:
9	RW	PMC_LFIR_ACTION1_9:
10	RW	PMC_LFIR_ACTION1_10:
11	RW	PMC_LFIR_ACTION1_11:
12	RW	PMC_LFIR_ACTION1_12:
13	RW	PMC_LFIR_ACTION1_13:
14	RW	PMC_LFIR_ACTION1_14:
15	RW	PMC_LFIR_ACTION1_15:
16	RW	PMC_LFIR_ACTION1_16:
17	RW	PMC_LFIR_ACTION1_17:
18	RW	PMC_LFIR_ACTION1_18:
19	RW	PMC_LFIR_ACTION1_19:
20	RW	PMC_LFIR_ACTION1_20:
21	RW	PMC_LFIR_ACTION1_21:
22	RW	PMC_LFIR_ACTION1_22:
23	RW	PMC_LFIR_ACTION1_23:
24	RW	PMC_LFIR_ACTION1_24:
25	RW	PMC_LFIR_ACTION1_25:
26	RW	PMC_LFIR_ACTION1_26:
27	RW	PMC_LFIR_ACTION1_27:
28	RW	PMC_LFIR_ACTION1_28:
29	RW	PMC_LFIR_ACTION1_29:
30	RW	PMC_LFIR_ACTION1_30:
31	RW	PMC_LFIR_ACTION1_31:
32	RW	PMC_LFIR_ACTION1_32:
33	RW	PMC_LFIR_ACTION1_33:
34	RW	PMC_LFIR_ACTION1_34:
35	RW	PMC_LFIR_ACTION1_35:
36	RW	PMC_LFIR_ACTION1_36:
37	RW	PMC_LFIR_ACTION1_37:
38:46	RW	PMC_LFIR_ACTION1_38_46:
47	RW	PMC_LFIR_ACTION1_47:
48	RW	PMC_LFIR_ACTION1_48:



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Register Name		<i>Hi Register Of Mask For Pmc_ocb_pmc_error OCC Interrupt</i>	
Mnemonic		EH.TPCHIP.OCC.PMC.PMC_ERROR_INT_MASK_HI_REG	
Address		0000000000062067 (PIB) 0000000040010338 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:31	RW	RW	PMC_ERROR_INT_MASK_HI: Most-significant half of mask for pmc_ocb_pmc_error

Register Name		<i>Lo Register Of Mask For Pmc_ocb_pmc_error OCC Interrupt</i>	
Mnemonic		EH.TPCHIP.OCC.PMC.PMC_ERROR_INT_MASK_LO_REG	
Address		0000000000062068 (PIB) 0000000040010340 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:31	RW	RW	PMC_ERROR_INT_MASK_LO: Least-significant half of mask for pmc_ocb_pmc_error

Register Name		<i>PMC PORE Scratch Register (PORSCR)</i>	
Mnemonic		EH.TPCHIP.OCC.PMC.PMC_PORE_SCRATCH_REG0	
Address		000000000006209D (PIB) 00000000400104E8 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:31	RW	RW	PORSCR_SCRATCH0: PORE scratch space to record things during the initial IPL that PORE needs when waking up a core (for example, SPURR base value)

Register Name		<i>PMC PORE Scratch Register (PORSCR)</i>	
Mnemonic		EH.TPCHIP.OCC.PMC.PMC_PORE_SCRATCH_REG1	
Address		000000000006209E (PIB) 00000000400104F0 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:31	RW	RW	PORSCR_SCRATCH1: PORE scratch space to record things during the initial IPL that PORE needs when waking up a core (for example, SPURR base value)



Register Name		<i>SSCR0 Provides The Length Control Information for the P2S Frames</i>
Mnemonic		EH.TPCHIP.PIB.SPIADC.SPIMPSS_ADC_CTRL_REG0
Address		0000000000070000 (PIB)
Attributes		
Description		
Bits	PIB	Field Mnemonic: Description
0:5	RWX	HWCTRL_FRAME_SIZE: Number of data bits per individual SPI transaction (also referred to as frame) during chip select assertion Supported values: 0x10 (16d), Chip Select assertion duration is spi_frame_size + 2
6:11	RWX	HWCTRL_OUT_COUNT: Number of bits sent out MOSI of the frame Supported values: 0x000 to spi_frame_size. Values beyond spi_frame_size are ignored.
12:17	RWX	HWCTRL_IN_DELAY: Number of SPI clocks after chip select to wait before capturing MISO input Supported values: 0x000 to spi_frame_size. Values beyond spi_frame_size result in the input never being captured
18:23	RWX	HWCTRL_IN_COUNT: Number of bits captured on MISO input Supported values: 0x000 to spi_frame_size. The actual number of bits captured is spi_frame_size - spi_in_delay

Register Name		<i>SSCR1 Provides All Control Bits for the SPI ADC Interface (note That This Interface Does Not Support CRC)</i>
Mnemonic		EH.TPCHIP.PIB.SPIADC.SPIPSS_ADC_CTRL_REG1
Address		0000000000070001 (PIB)
Attributes		
Description		
Bits	PIB	Field Mnemonic: Description
0	RWX	HWCTRL_FSM_ENABLE: if 1 the ADC FSM can be used to control the SPI interface
1	RWX	HWCTRL_DEVICE: Select the device on the ADC bus to target: 0: Chip Select 0 1: Chip Select 1
2	RWX	HWCTRL_CPOL: SPI clock polarity (CPOL=0 means that clk idle is deasserted, CPOL=1 means that clk idle is asserted)
3	RWX	HWCTRL_CPHA: SPI clock phase (CPHA=0 means to first edge --> sample , second_edge --> change) (CPHA=1 means first edge --> change , second_edge --> sample)
4:13	RWX	HWCTRL_CLOCK_DIVIDER: SPI clock speed divider to divide the nest_nclk/4 mesh clock, which results in a SPI frequency $SPI\_freq = nest\_freq / (8 * (clock\_divider + 1))$ For a 2.4GHz nest clock, this means that the interchip clk can be theoretically adjusted between 300MHz and 0.29MHz (cycle time 1.66ns...3.41us, in 1.66ns steps). However, due to some constraints, a practical range is 0.5...75MHz. Allowed values: 0x003...0x3FF Due to metastability constraints, only use values > 2 for interchip_clock_divider, otherwise data will not be sampled correctly!
14:17	RWX	HWCTRL_NR_OF_FRAMES: specifies the number of frames for each iteration of ADC sampling (legal values are 0,1, 2, ..., 15)
18	RWX	HWCTRL_WRITE_WHILE_BRIDGE_BUSY_SCRESP_EN: If this bit is '1' (enabled) then if somebody tries to write into the registers of HWCTRL in the middle of operation then it will send out the busy_response code which is given in the bit 19:21.
19:21	RWX	BUSY_RESPONSE_CODE: busy response code for the bit 18

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Register Name	<i>SSCR2 Provides All Control Bits for the SPI ADC Interface (note That This Interface Does Not Support ECC)</i>
Mnemonic	EH.TPCHIP.PIB.SPIADC.SPIPSS_ADC_CTRL_REG2
Address	0000000000070002 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:16	RWX	HWCTRL_INTER_FRAME_DELAY: Delay between two frames of a two command set as measured from the end of the last bit of the first frame until the chip select of the second frame, which contains the status, is asserted. This delay allows for the ADC chip to acquire the next value.. Delay is computed as: (value * ~100ns_hang_pulse) +0/~100ns_hang_pulse time 0x00000: Wait 1 SPI Clock 0x00001 - 0x1FFFF: value = number of ~100ns_hang_pulses Max. delay at 0x1FFFF: 131071*100ns = 13.1ms. Firmware has to make sure that the delay is at least one SPI clock. In the case of of APSS with Analog-to-Digital Converter (ADC), this delay allows for acquisition of the next reading when using a continuous acquisition mode. (TI specs indicate 325ns)

Register Name	<i>SSSR Displays The Current Status About SPI-related Activities</i>
Mnemonic	EH.TPCHIP.PIB.SPIADC.SPIPSS_ADC_STATUS_REG
Address	0000000000070003 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	ROX	HWCTRL_ONGOING: the SPI interface is in progress of shifting data. This bit is provided, as a wire, to the OCC interrupt controller. Note that FW can poll on this bit to wait for valid data.
1	ROX	ADC_RESERVED_1: Implemented but not used
2	ROX	ADC_RESERVED_2: Implemented but not used
3	ROX	ADC_RESERVED_3: Implemented but not used
4	ROX	HWCTRL_INVALID_NUMBER_OF_FRAMES: if this bit gets asserted, a non-supported number of frames was set in SPIPSS_ADC_CTRL_REG1. This bit is cleared upon the next enabled command that has a legal number of frames.
5	NCX	HWCTRL_WRITE_WHILE_FSM_BUSY_ERR: Indicates that firmware attempted to perform an PIB Write to the any writeable register while the adc FSM is busy (adc_ongoing=1), which will cause undefined bridge behavior. This bit can only be reset by doing proper reset operation using reset register
6	ROX	ADC_RESERVED_6: Implemented but not used
7	ROX	HWCTRL_FSM_ERR: Indicates a catastrophic FSM error in the PIB2SPI control FSM

Register Name	<i>SSCR Provided A Way To Start The ADC Sampling</i>
Mnemonic	EH.TPCHIP.PIB.SPIADC.SPIPSS_ADC_CMD_REG
Address	0000000000070004 (PIB)
Attributes	
Description	



Bits	PIB	Field Mnemonic: Description
0	RWX	HWCTRL_START_SAMPLING: if bit set to 1 this register immediately resets itself and starts the ADC sampling only if adc_fsm_enable is enabled otherwise it will not trigger the sampling

Register Name	<i>SSWDR Register Is Used To Configure The SPI Data That Are Shifted Out For Each Frame To The SPIADC</i>	
Mnemonic	EH.TPCHIP.PIB.SPIADC.SPIPSS_ADC_WDATA_REG	
Address	000000000070010 (PIB)	
Attributes		
Description		

Bits	PIB	Field Mnemonic: Description
0:15	RWX	HWCTRL_WDATA: These 16bits are shifted out of the SPI interface to the ADC every time a frame is read.

Register Name	<i>SRDR0 Displays The Read Data For Frames 0 To 3</i>	
Mnemonic	EH.TPCHIP.PIB.SPIADC.SPIPSS_ADC_RDATA_REG0	
Address	000000000070020 (PIB)	
Attributes		
Description	Note to FW: this register should be read last, if the dial 'enable_restart_ADC_sampling_after_last_read' is enabled	

Bits	PIB	Field Mnemonic: Description
0:63	ROX	HWCTRL_RDATA0: bits 0 to 15: frame 0 read data bits 16 to 31: frame 1 read data bits 32 to 47: frame 2 read data bits 48 to 63: frame 3 read data

Register Name	<i>SRDR1 Displays The Read Data For Frames 4 To 7</i>	
Mnemonic	EH.TPCHIP.PIB.SPIADC.SPIPSS_ADC_RDATA_REG1	
Address	000000000070021 (PIB)	
Attributes		
Description		

Bits	PIB	Field Mnemonic: Description
0:63	ROX	HWCTRL_RDATA1: bits 0 to 15: frame 4 read data bits 16 to 31: frame 5 read data bits 32 to 47: frame 6 read data bits 48 to 63: frame 7 read data

Register Name	<i>SRDR2 Displays The Read Data For Frames 8 To 11</i>	
Mnemonic	EH.TPCHIP.PIB.SPIADC.SPIPSS_ADC_RDATA_REG2	
Address	000000000070022 (PIB)	
Attributes		
Description		

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Bits	PIB	Field Mnemonic: Description
0:63	ROX	HWCTRL_RDATA2: bits 0 to 15: frame 8 read data bits 16 to 31: frame 9 read data bits 32 to 47: frame 10 read data bits 48 to 63: frame 11 read data

Register Name	<i>SRDR2 Displays The Read Data For Frames 8 To 11</i>
Mnemonic	EH.TPCHIP.PIB.SPIADC.SPIPSS_ADC_RDATA_REG3
Address	0000000000070023 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	ROX	HWCTRL_RDATA3: bits 0 to 15: frame 12 read data bits 16 to 31: frame 13 read data bits 32 to 47: frame 14 read data bits 48 to 63: frame 15 read data

Register Name	<i>S100R Register Defines The Number Of Nest/4 Cycles Approximates 100ns As Decrementer Is Reloaded With This Value Upon Reaching 0</i>
Mnemonic	EH.TPCHIP.PIB.SPIADC.SPIPSS_100NS_REG
Address	0000000000070028 (PIB)
Attributes	
Description	At the 0 value, a pulse is generated to represent an approximate 100ns interval.

Bits	PIB	Field Mnemonic: Description
0:31	RW	REG_100NS_OUT: value should be corresponding to 100ns

Register Name	<i>PPCR0A Provides The Length Control Information for the P2S Frames</i>
Mnemonic	EH.TPCHIP.PIB.SPIADC.SPIPSS_P2S_CTRL_REG0
Address	0000000000070040 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:5	RWX	P2S_FRAME_SIZE: Number of data bits per individual SPI transaction (also referred to as frame) during chip select assertion Supported values: 0x10 (16d), Chip Select assertion duration is spi_frame_size + 2
6:11	RWX	P2S_OUT_COUNT1: Number of bits sent out MOSI in frame 1 of a 2 frame set (the arbitration unit) Supported values: 0x000 to spi_frame_size. Values beyond spi_frame_size are ignored.
12:17	RWX	P2S_IN_DELAY1: Number of SPI clocks after chip select to wait before capturing MISO input in frame 1 Supported values: 0x000 to spi_frame_size. Values beyond spi_frame_size result in the input never being captured

Bits	PIB	Field Mnemonic: Description
18:23	RWX	P2S_IN_COUNT1: Number of bits captured on MISO input in frame 1 Supported values: 0x000 to spi_frame_size. The actual number of bits captured is spi_frame_size - spi_in_delay
24:29	RWX	P2S_OUT_COUNT2: Number of bits sent out MOSI in frame 2 of a 2 frame set (the arbitration unit) Supported values: 0x000 to spi_frame_size. Values beyond spi_frame_size are ignored.
30:35	RWX	P2S_IN_DELAY2: Number of SPI clocks after chip select to wait before capturing MISO input in frame 2 Supported values: 0x000 to spi_frame_size. Values beyond spi_frame_size result in the input never being captured
36:41	RWX	P2S_IN_COUNT2: Number of bits captured on MISO input in frame 2 Supported values: 0x000 to spi_frame_size. The actual number of bits captured is spi_frame_size - spi_in_delay

Register Name	<i>SSCR1 Provides Control Bits for the P2S Bridge Interface (note That This Interface Does Not Support CRC)</i>
Mnemonic	EH.TPCHIP.PIB.SPIADC.SPIPSS_P2S_CTRL_REG1
Address	0000000000070041 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	RWX	P2S_BRIDGE_ENABLE: if 1 the PIB2SPI bridge can be used to control the SPI interface if 0, the PIB2SPI bridge is disabled.
1	RWX	P2S_DEVICE: Select the device on the ADC bus to target: 0: Chip Select 0 1: Chip Select 1
2	RWX	P2S_CPOL: SPI clock polarity (CPOL = 0 means that clk idle is deasserted. CPOL = 1 means that clk idle is asserted).
3	RWX	P2S_CPHA: SPI clock phase (CPHA = 0 means to change/sample values of data signals on first edge; otherwise, on the second edge).
4:13	RWX	P2S_CLOCK_DIVIDER: SPI clock speed divider to divide the nest_nclk/4 mesh clock, which results in a SPI frequency $SPI\_freq = nest\_freq / (8 * (clock\_divider + 1))$ For a 2.4GHz nest clock, this means that the interchip clk can be theoretically adjusted between 300MHz and 0.29MHz (cycle time 1.66ns...3.41us, in 1.66ns steps). However, due to some constraints, a practical range is 0.5...75MHz. Allowed values: 0x003...0x3FF Due to metastability constraints, only use values > 2 for interchip_clock_divider, otherwise data will not be sampled correctly!
14:16	RWX	RESERVED: Implemented but not used
17	RWX	P2S_NR_OF_FRAMES: Specifies the number of frames sent in the frame set (# of frames before the arbitration unit rearbitrates). 0: 1 frame 1: 2 frames
18	RWX	P2S_WRITE_WHILE_BRIDGE_BUSY_SCRESP_EN: If this bit is '1' (enabled) then if somebody tries to write into the registers of P2S bridge in the middle of operation then it will send out the busy_response code which is given in the bit 19:21.
19:21	RWX	BUSY_RESPONSE_CODE_NO_1: busy response code for the bit 18

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Register Name	<i>SSCR2 Provides All Control Bits for the SPI ADC Interface (note That This Interface Does Not Support ECC)</i>
Mnemonic	EH.TPCHIP.PIB.SPIADC.SPIPSS_P2S_CTRL_REG2
Address	0000000000070042 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:16	RWX	P2S_INTER_FRAME_DELAY: Delay between two frames of a two command set as measured from the end of the last bit of the first frame until the chip select of the second frame, which contains the status, is asserted. This delay allows for the checking and status data the production in the addressed chip. Delay is computed as: (value * ~100ns_hang_pulse) + 0/~100ns_hang_pulse time 0x00000: Wait 1 SPI Clock 0x00001 - 0x1FFFF: value = number of ~100ns_hang_pulses Max. delay at 0x1FFFF: 131071*100ns = 13.1ms. Firmware has to make sure that the delay is at least one SPI clock.

Register Name	<i>SSSR Displays The Current Status About SPI-related Activities</i>
Mnemonic	EH.TPCHIP.PIB.SPIADC.SPIPSS_P2S_STATUS_REG
Address	0000000000070043 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	ROX	P2S_ONGOING: Indicates that a bridge transaction is queued or in progress of being executed. This bit is set by hardware while an operation is queued or in progress and will be reset by hardware when the operation is complete.
1	ROX	P2S_RESERVED_1: Implemented but not used
2	ROX	P2S_RESERVED_2: Implemented but not used
3	ROX	P2S_RESERVED_3: Implemented but not used
4	ROX	P2S_RESERVED_4: Implemented but not used
5	NCX	P2S_WRITE_WHILE_BRIDGE_BUSY_ERR: Indicates that firmware attempted to perform an PIB Write to the any register while the p2s bridge is busy, which will caused undefined bridge behavior. This bit can only be reset by doing proper reset operation using reset register
6	ROX	RESERVED6: Implemented but not used
7	ROX	P2S_FSM_ERR: Indicates a catastrophic FSM error in the PIB2SPI control FSM

Register Name	<i>SSCR Provides The Means To Start The P2S Bridge</i>
Mnemonic	EH.TPCHIP.PIB.SPIADC.SPIPSS_P2S_COMMAND_REG
Address	0000000000070044 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	RWX	P2S_START_COMMAND: if set to '1' and enable_pib2spi_bridge = '1', this register immediately resets itself and starts the P2S operation. If enable_pib2spi_bridge = '0', this register immediately resets itself but no operation is started.



Register Name	<i>SPW Register is Used for the Most Significant 4 Bytes of Write Data Through the P2s Bridge</i>
Mnemonic	EH.TPCHIP.PIB.SPIADC.SPIPSS_P2S_WDATA_REG
Address	0000000000070050 (PIB)
Attributes	
Description	Note that a write to this register starts the SPI transaction (read or write), if the switch enable_pib2p2s_bridge is set.

Bits	PIB	Field Mnemonic: Description
0:31	RWX	P2S_WDATA: Bits 0 to 31 of SPI data packet

Register Name	<i>SPR Register Is Used for the Most Significant 4 Bytes Of Read Data of the P2s Bridge</i>
Mnemonic	EH.TPCHIP.PIB.SPIADC.SPIPSS_P2S_RDATA_REG
Address	0000000000070060 (PIB)
Attributes	
Description	After the p2s_ongoing bit has dropped, the read values are available in SPR.

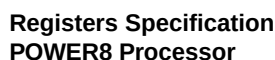
Bits	PIB	Field Mnemonic: Description
0:31	ROX	P2S_RDATA: Bits 0 to 31 of SPI data packet

Register Name	<i>Write Into This Register With Proper Value Will Reset Complete HWCTRL SPIPSS</i>
Mnemonic	EH.TPCHIP.PIB.SPIADC.SPIPSS_ADC_RESET_REGISTER
Address	0000000000070005 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:1	RW	HWCTRL_RESET: writing value 01 on this will reset

Register Name	<i>Write Into This Register With Proper Value Will Reset Complete P2S_ SPIPSS</i>
Mnemonic	EH.TPCHIP.PIB.SPIADC.SPIPSS_P2S_RESET_REGISTER
Address	0000000000070045 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:1	RW	P2S_RESET: writing value 01 on this will reset



Bits	PIB	Field Mnemonic: Description
0	RWX	AUTO_PRE_INCREMENT: If this bit is 1 : when Auto_increment_register is read/written, data will be read/written into array after the address pointer is incremented. If this bit is 0 : when Auto_increment_register is read/written, data will be read/written into array before address pointer is incremented. Default_value : 0
1	RWX	AUTO_POST_DECREMENT: If this bit is 1 : when Auto_decrement_register is read/written, data will be read/written into array before the address pointer is decremented. If this bit is 0 : when Auto_decrement_register is read/written, data will be read/written into array after address pointer is decremented. Default_value:0
2	RWX	DISABLE_ECC: If this bit is 1 : disables the ECC checking and calculating If this bit is 0 : sends ECC and checks the ECC for the array data

Bits	PIB	Field Mnemonic: Description
0:47	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000
48:63	RWX	ADDRESS_POINTER: If the value on this is 0x0000 = accesses zero location of the array 0x0001 = accesses first location of the array

Bits	PIB	Field Mnemonic: Description
0	ROX	ADDR_INVALID: Address which PIB is trying to access in PIBMEM is not valid one in PIBMEM
1	ROX	WRITE_INVALID: Address for which PIB is trying to write is not writable
2	ROX	READ_INVALID: Address for which PIB is trying to read is not readable
3	ROX	ECC_UNCORRECTED_ERROR: Uncorrectable error occurred while PIB memory read . This also go out as FIR error
4	ROX	ECC_CORRECTED_ERROR: Corrected error in PIB mem read . Data can still be considered as good. This is an error o/p of ECC CHECK CORRECTION block



Bits	PIB	Field Mnemonic: Description
5:9	ROX	RESERVED: Reserved as of now tiedown
10	RO	Constant = 0b0
11:17	ROX	FSM_PRESENT_STATE: State machines present state IDLE : Default state := 1000000; ECC_GEN : ECC generation happens for the write operation := 0100000; WRITE_ARRAY : Writes data into the array := 0010000; ACK : Gives out the ack to the PIB := 0001000; READ_SETUP : Checks for errors in this state := 0000100; READ_ARRAY : Performs read operation to array in this state := 0000010; ECC_CHK : Performs ECC checking in this state := 0000001;

Register Name	<i>Write Into This Register With Proper Value Will Reset Complete PIBMEM Controller Except Array</i>
Mnemonic	EH.TPCHIP.PIB.POREMEM.PIBMEM.CTRL.PIBMEM_RESET_REGISTER
Address	0000000000088006 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:1	RW	RESET: writing value 10 on this will reset PIBMEM

Register Name	<i>Holds Repair Data for the Array</i>
Mnemonic	EH.TPCHIP.PIB.POREMEM.PIBMEM.CTRL.PIBMEM_REPAIR_REGISTER_0
Address	0000000000088007 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RW	REPAIR_DATA_0: parallel register through which repair data can be loaded directly on to the repair chain of the array 0th bit : Enables the mux selecting repair data from this register 1:7 : Repair data for first array (that has the address from 0x0 to 0x7F) 8:14 : Repair data for second array (that has the address from 0x80 to 0xFF) 15:21 : Repair data for third array (that has the address from 0x100 to 0x17F) and so on 22:62 : Reserved 63 : Switch to disable the start_abist

Register Name	<i>Control Register PMC Mode 1</i>
Mnemonic	EH.TPCHIP.PIB.I2CM.CONTROL_REGISTER_1
Address	00000000000A0020 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	WOX	PIB_CNTR_REG_BIT_WITHSTART_1: for command register of i2c engine
1	WOX	PIB_CNTR_REG_BIT_WITHADDR_1: for command register of i2c engine
2	WOX	PIB_CNTR_REG_BIT_READCONT_1: for command register of i2c engine
3	WOX	PIB_CNTR_REG_BIT_WITHSTOP_1: for command register of i2c engine

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Bits	PIB	Field Mnemonic: Description
4:7	WOX	PIB_CNTR_REG_LENGTH_1: Maximum_write = 4 , Maximum_read = 8
8:14	WOX	PIB_CNTR_REG_ADDR_1: for command register of i2c engine
15	WOX	PIB_CNTR_REG_BIT_RNW_1: for command register of i2c engine
16:17	WOX	PIB_CNTR_REG_SPEED_1: 00=100K 01=400K 10=3400K 11=50K
18:22	WOX	PIB_CNTR_REG_PORT_NUMBER_1: for mode register of i2c engine
23:25	WOX	REG_ADDR_LEN_1: 00= No register address in FIFO 01= 1 Byte of FIFO's data is Register address 10= 2 Byte of FIFO's data are Register address 11= 3 Byte of FIFO's data are Register address
26	WOX	ENH_MODE_1: Enable enhanced mode in mode register of I2C engine
27:31	WOX	UNUSED_1:
32:39	WOX	PIB_CNTR_REG_DATA_1_1: data for i2c FIFO
40:47	WOX	PIB_CNTR_REG_DATA_2_1: data for i2c FIFO
48:55	WOX	PIB_CNTR_REG_DATA_3_1: data for i2c FIFO
56:63	WOX	PIB_CNTR_REG_DATA_4_1: data for i2c FIFO

Register Name		Reset Register PMC Mode
Mnemonic		EH.TPCHIP.PIB.I2CM.RESET_REGISTER_1
Address		0000000000A0021 (PIB)
Attributes		
Description		
Bits	PIB	Field Mnemonic: Description
0	WOX	overall_reset_1 one bit register resets all registers and I2C ENGINE

Register Name		Status Register PMC Mode
Mnemonic		EH.TPCHIP.PIB.I2CM.STATUS_REGISTER_1
Address		0000000000A0022 (PIB)
Attributes		
Description		
Bits	PIB	Field Mnemonic: Description
0	ROX	BUS_STATUS_ADDR_NVLD_1: Address invalid
1	ROX	BUS_STATUS_WRITE_NVLD_1: Write invalid
2	ROX	BUS_STATUS_READ_NVLD_1: Read invalid
3	ROX	BUS_STATUS_ADDR_P_ERR_1: Address parity error
4	ROX	BUS_STATUS_PAR_ERR_1: Data parity error
5	ROX	BUS_STATUS_LB_PARITY_ERROR_1: local bus parity error
6:13	ROX	PIB_REG_DATA_ACT_0_1: First byte of data
14:21	ROX	PIB_REG_DATA_ACT_1_1: Second byte of data
22:29	ROX	PIB_REG_DATA_ACT_2_1: Third byte of data
30:37	ROX	PIB_REG_DATA_ACT_3_1: Fourth byte of data



Bits	PIB	Field Mnemonic: Description
38:43	RO	Constant = 0b0000000
44	ROX	BUS_STATUS_BUSY_1: Local bus busy
45	ROX	BUS_STATUS_INVALID_COMMAND_1: invalid command
46	ROX	BUS_STATUS_PARITY_ERROR_1: parity error
47	ROX	BUS_STATUS_BACK_END_OVERRUN_ERROR_1: back end overrun error
48	ROX	BUS_STATUS_BACK_END_ACCESS_ERROR_1: back end access error
49	ROX	BUS_STATUS_ARBITRATION_LOST_ERROR_1: arbitration lost error
50	ROX	BUS_STATUS_NACK_RECEIVED_ERROR_1: nack received error
51	ROX	BUS_STATUS_DATA_REQUEST_1: data request
52	ROX	BUS_STATUS_COMMAND_COMPLETE_1: command complete
53	ROX	BUS_STATUS_STOP_ERROR_1: stop error
54	ROX	BUS_STATUS_I2C_PORT_BUSY_1: i2c port busy
55	ROX	BUS_STATUS_I2C_INTERFACE_BUSY_1: i2c interface busy
56:63	ROX	BUS_STATUS_FIFO_ENTRY_COUNT_1: fifo entry count

Register Name	<i>I2CS Configuration Register</i>
Mnemonic	EH.TPCHIP.PIB.I2CS.TP_I2CS_COMP.I2CSCONFIG
Address	00000000000D0000 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:6	RW	BASE_ADDRESS: I2C base address
7:10	RW	HW_VERSION: Hardware version control number set by FSP
11:20	RW	ONE_MICROSECOND_COUNTER: I2C one microsecond counter wraparound value
21	RW	I2CS_PORT_ENABLE: Enable I2CS port
22	RW	I2CS_PORT_RESET: Enable I2CS reset
23	RW	I2CS_ENABLE_ERROR_STATE: Enable I2CS error state
24	RW	I2CS_ENABLE_TIMEOUT: Enable I2CS timeout
25	RWX	I2CS_ERROR: I2CS error state
26	RW	I2CS_DISABLE_RETURN_ONES: Disable the return all ones mode
27	RW	I2C_ENABLE_PARITY_CHECK: Enable I2CS parity check
28	RW	I2C_SWITCH_ERRORCODE_4_5: Switch write condition of the error register
29	RW	I2C_DISABLE_23_ADDRESSING: Switch to select 23- and 32-bit addressing

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Register Name	<i>I2CS Status Register</i>
Mnemonic	EH.TPCHIP.PIB.I2CS.TP_I2CS_COMP.I2CSSTATUS
Address	0000000000D0001 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	RWX_WCLRR EG	CMD_IN_PROGRESS: I2CS command in progress
1	RWX_WCLRR EG	NO_ACK: I2CS No ACK
2	RWX_WCLRR EG	ANY_ERROR: I2CS any error
3	RWX_WCLRR EG	READ_NOT_WRITE: I2CS R/W
4:27	RWX_WCLRR EG	PCB_ADDRESS_TO_ACCESS: I2CS address
28:30	ROX	PCB_MASTER_ERRORS: PCB Master Error Code (scresp coming back to master)

Register Name	<i>I2CS Error Register</i>
Mnemonic	EH.TPCHIP.PIB.I2CS.TP_I2CS_COMP.I2CSERRORS
Address	0000000000D0002 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:2	RWX_WCLRR EG	SCRESP_TO_MASTER: Scresp coming back to master
3	RWX_WCLRR EG	READ_PARITY_ERR: Read data parity error
4	RWX_WCLRR EG	I2C_INTERFACE_PERR: I2C Interface Parity Error
5	RWX_WCLRR EG	INTERFACE_RESET_HANG: PIB reset while read or write operation -> Interface will hang
6	RWX_WCLRR EG	ADDR_NVLD: PIB slave: invalid address
7	RWX_WCLRR EG	WRITE_NVLD: PIB slave: invalid write access
8	RWX_WCLRR EG	READ_NVLD: PIB slave: invalid read access
9	RWX_WCLRR EG	ADDR_P_ERR: PIB slave: address parity error
10	RWX_WCLRR EG	DATA_P_ERR: PIB slave: data parity error
11	RWX_WCLRR EG	I2CS_TIME_OUT: I2C slave timeout



Bits	PIB	Field Mnemonic: Description
12	RWX_WCLRR EG	SCRESET_WHILE_WRITE: PIB reset while write
13	RWX_WCLRR EG	ABORT: Reset on PIB

Register Name	Data Register PMC Mode
Mnemonic	EH.TPCHIP.PIB.I2CM.DATA_REGISTER_1
Address	0000000000A0023 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:7	RWX	PIB_REG_DATA_ACT_0_1: First byte of data
8:15	RWX	PIB_REG_DATA_ACT_1_1: Second byte of data
16:23	RWX	PIB_REG_DATA_ACT_2_1: Third byte of data
24:31	RWX	PIB_REG_DATA_ACT_3_1: Fourth byte of data
32:39	RWX	PIB_REG_DATA_ACT_4_1: Fifth byte of data
40:47	RWX	PIB_REG_DATA_ACT_5_1: Sixth byte of data
48:55	RWX	PIB_REG_DATA_ACT_6_1: Seventh byte of data
56:63	RWX	PIB_REG_DATA_ACT_7_1: Eighth byte of data

Register Name	Command Register 1
Mnemonic	EH.TPCHIP.PIB.I2CM.COMMAND_REGISTER_1
Address	0000000000A0025 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	RWX	WITH_START_1: Decides start command to be issued or not during the beginning of the operation Decides start command to be issued or not during the beginning of the operation
1	RWX	WITH_ADDRESS_1: Decides Device address to be send or not during the beginning of the operation Decides Device address to be send or not during the beginning of the operation
2	RWX	READ_CONTINUE_1: Decides Next read operation is continuation of present operation or not Decides Next read operation is continuation of present operation or not
3	RWX	WITH_STOP_1: Decides stop command to be issued or not during the end of the operation Decides stop command to be issued or not during the end of the operation
4:7	RWX	NOT_USED_1: not used not used
8:14	RWX	DEVICE_ADDRESS_1: Device address of Slave on the I2C Bus Device address of Slave on the I2C Bus
15	RWX	READ_NOT_WRITE_1: I2C read or write I2C read or write
16:31	RWX	LENGTH_IN_BYTES_1: Length of Bytes to be accessed through the I2C Bus Length of Bytes to be accessed through the I2C Bus

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Bits	PIB	Field Mnemonic: Description
32:39	ROX	PEEK_DATA1_1: 0 : invalid command : Written with New command when Old command is still in progress 1: parity error: 2: back end overrun error: Writing/reading into full/empty fifo resply 3: back end access error: Writing/Reading more data than requested 4: arbitration lost error: I2C bus is held by some other master when trying to access 5: nack received error: Slave is not responding back with the ACK. 6: data request: FIFO needs to be accessed some more times to full fill the expectation 7: state m/c idle : I2C state machine is now in idle state ' 0 : invalid command' '1: parity error' '2: back end overrun error' '3: back end access error' '4: arbitration lost error' '5: nack received error' '6: data request' '7: state m/c idle '
40	ROX	LBUS_PARITY_ERR1_1: local bus parity error from the local bus to glue logic local bus parity error from the local bus to glue logic
41:63	RO	Constant = 0b000000000000000000000000

Register Name	ECCB : Control Register
Mnemonic	EH.TPCHIP.PIB.LPCM.ECCB.CONTROL_REG
Address	00000000000B0000 (PIB)
Attributes	Secure=true
Description	

Bits	PIB	Field Mnemonic: Description
0	WO	I2C_CNTL_WITHSTART: If the With Start bit is set to b1, then a Start Condition will precede any command for data transfer on the I2C bus
1	WO	I2C_CNTL_WITHADDR: When With Address is set to b1, it indicates that the address field in the Command Register (bits 8 to 14) contains an I2C slave device address
2	WO	I2C_CNTL_READCONT: Indicates this read will continue and more data will be requested on the I2C interface
3	WO	I2C_CNTL_WITHSTOP: When Stop is set to b1, it will generate a stop sequence on the I2C bus after the transfer is complete
4:7	WO	I2C_CNTL_DATA_LENGTH: Requested Data Length of Operation
8:14	WO	I2C_CNTL_DEV_ADDR: The Device Address field in the command register holds the device address to be sent to the I2C bus if the With Address bit is set to b1.
15	WO	I2C_CNTL_RNW: Read not Write Operation
16:17	WO	I2C_CNTL_SPEED: 00= No change , this will not change the bit rate divisor . Whatever value is already residing there will stay as it is. 01=400K 10=3400K 11=50K
18:22	WO	I2C_CNTL_PORT_NUMBER: The I2C engine provides 64 I2C interfaces (ports). One out of these four I2C ports is selected by setting Port Number (0 to 5)
23:25	WO	I2C_CNTL_ADDR_LENGTH: 000= No register address in data field 001= 1 Byte of the data field is Register address 010= 2 Byte of the data field are Register address 011= 3 Byte of the data field are Register address 100= 4 Byte of the data field are Register address others are not allowed



Bits	PIB	Field Mnemonic: Description
26	WO	I2C_CNTL_ENHANCED_MODE: Stop Only command sends immediately a Stop condition.
27:31	WO	I2C_CNTL_UNUSED: UNUSED Bits
32:63	WO	I2C_CNTL_DATA: When register address = 4 Byte this field contains only reg address. In case reg. Address < 4 the field contains reg address and data in the remaining bytes.

Register Name	<i>ECCB : Reset Register</i>
Mnemonic	EH.TPCHIP.PIB.LPCM.ECCB.RESET_REG
Address	0000000000B0001 (PIB)
Attributes	Secure=true
Description	

Bits	PIB	Field Mnemonic: Description
0	WOX	pib_reset_reg Reset active operation for register set 0x00 to 0x03
1	WO	lpc_fast_logic_reset Resets the fast lpc logic. Active by default at power on. Write to '0' is necessary before a read/write op via lpc is started.

Register Name	<i>ECCB : Status Register</i>
Mnemonic	EH.TPCHIP.PIB.LPCM.ECCB.STATUS_REG
Address	0000000000B0002 (PIB)
Attributes	Secure=true
Description	

Bits	PIB	Field Mnemonic: Description
0	ROX	PIB_BUS_ADDR_NVLD_ERR: Bits from I2C Macro. Only used if I2C connected
1	ROX	PIB_BUS_WRITE_NVLD_ERR: Bits from I2C Macro. Only used if I2C connected
2	ROX	PIB_BUS_READ_NVLD_ERR: Bits from I2C Macro. Only used if I2C connected
3	ROX	PIB_BUS_ADDR_PAR_ERR: Bits from I2C Macro. Only used if I2C connected
4	ROX	PIB_BUS_PAR_ERR: Bits from I2C Macro. (Parity error from PIB (signal from pib_slave_interface))
5	ROX	LOCAL_BUS_PAR_ERR: Bits from I2C Macro.
6:37	ROX	READ_DATA: Read data in case of a read operation
38:40	ROX	PIB_MASTER_RESP_INFO: Response Info of PIB Master in case any Slave is connected
41:43	ROX	ECCB_ERROR_INFO: 100 = pib_control_reg_data_lgt_err 101 = pib_control_reg_addr_lgt_err 110 = pib_control_reg_addr_bdy_err 111 = pib_eccaddr_reg_err 010 = eff_pibm_reset 011 = eff_pibs_reset 001 = uce_q
44	ROX	ECCB_OP_BUSY: Last Request has not finished. Data are available when bit is 0
45	ROX	PIB_INVALID_COMMAND: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected

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Bits	PIB	Field Mnemonic: Description
46	ROX	PIB_PARITY_ERR: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected
47	ROX	I2C_BACK_END_OVERRUN_ERR: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected
48	ROX	I2C_BACK_END_ACCESS_ERR: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected
49	ROX	I2C_ARBITRATION_LOST_ERR: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected
50	ROX	I2C_NACK_RECIEVED_ERR: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected
51	ROX	I2C_DATA_REQUEST: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected
52	ROX	I2C_COMMAND_COMPLETE: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected
53	ROX	I2C_STOP_ERR: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected
54	ROX	I2C_PORT_BUSY: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected
55	ROX	I2C_INTERFACE_BUSY: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected
56	ROX	PARITY_ERROR: I2C Address register or ECC Address Register Parity Error
57	ROX	CE_COUNTER_OVERFLOW: More than 128 correctable ecc errors detected.
58:63	ROX	READ_DATA_LENGTH: Read data length - right aligned

Register Name		<i>ECCB : Data Register</i>
Mnemonic		EH.TPCHIP.PIB.LPCM.ECCB.DATA_REG
Address		0000000000B0003 (PIB)
Attributes		Secure=true
Description		
Bits	PIB	Field Mnemonic: Description
0:63	RWX	DATA_REGISTER: Write data in case of write and data has not been complete transferred via control register. Complete read data in case of a read.

Register Name		<i>ECCB : ECC Address Register</i>
Mnemonic		EH.TPCHIP.PIB.LPCM.ECCB.ECC_ADDRESS_REG
Address		0000000000B0004 (PIB)
Attributes		Secure=true
Description		
Bits	PIB	Field Mnemonic: Description
0:31	WO	START_ADDR: Start of ECC range
32:63	WO	STOP_ADDR: End of ECC range

Register Name		<i>ECCB : FWControl Register</i>
Mnemonic		EH.TPCHIP.PIB.LPCM.ECCB.FWCONTROL_REG
Address		00000000000B0020 (PIB)
Attributes		Secure=true
Description		
Bits	PIB	Field Mnemonic: Description
0	WO	FW_I2C_CNTL_WITHSTART: If the With Start bit is set to b1, then a Start Condition will precede any command for data transfer on the I2C bus
1	WO	FW_I2C_CNTL_WITHADDR: When With Address is set to b1, it indicates that the address field in the Command Register (bits 8 to 14) contains an I2C slave device address
2	WO	FW_I2C_CNTL_READCONT: Indicates this read will continue and more data will be requested on the I2C interface
3	WO	FW_I2C_CNTL_WITHSTOP: When Stop is set to b1, it will generate a stop sequence on the I2C bus after the transfer is complete
4:7	WO	FW_I2C_CNTL_DATA_LENGTH: Requested Data Length of Operation
8:14	WO	FW_I2C_CNTL_DEV_ADDR: The device address field in the command register holds the device address to be sent to the I2C bus if the address bit is set to b1.
15	WO	FW_I2C_CNTL_RNW: Read not Write Operation
16:17	WO	FW_I2C_CNTL_SPEED: 00 = No change. This does not change the bit rate divisor. Whatever value is already residing there stays as is. 01 = 400K 10 = 3400K 11 = 50K
18:22	WO	FW_I2C_CNTL_PORT_NUMBER: The I2C engine provides 64 I2C interfaces (ports). One out of these four I2C ports is selected by setting Port Number (0 to 5)
23:25	WO	FW_I2C_CNTL_ADDR_LENGTH: 000 = No register address in data field 001 = 1 byte of the data field is the Register address 010 = 2 bytes of the data field are the Register address 011 = 3 bytes of the data field are the Register address 100 = 4 bytes of the data field are the Register address Others are not allowed
26	WO	FW_I2C_CNTL_ENHANCED_MODE: Stop Only command sends immediately a Stop condition.
27:31	WO	FW_I2C_CNTL_UNUSED: UNUSED Bits
32:63	WO	FW_I2C_CNTL_DATA: When register address = 4 Byte this field contains only reg address. In case reg. Address < 4 the field contains reg address and data in the remaining bytes.

Register Name		<i>ECCB : FWReset Register</i>
Mnemonic		EH.TPCHIP.PIB.LPCM.ECCB.FWRESET_REG
Address		00000000000B0021 (PIB)
Attributes		Secure=true
Description		

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Bits	PIB	Field Mnemonic: Description
0	WOX	pib_fwreset_reg Reset active operation for register set 0x20 to 0x23

Register Name	<i>ECCB : FWStatus Register</i>
Mnemonic	EH.TPCHIP.PIB.LPCM.ECCB.FWSTATUS_REG
Address	00000000000B0022 (PIB)
Attributes	Secure=true
Description	

Bits	PIB	Field Mnemonic: Description
0	ROX	FW_PIB_BUS_ADDR_NVLD_ERR: Bits from I2C Macro. Only used if I2C connected
1	ROX	FW_PIB_BUS_WRITE_NVLD_ERR: Bits from I2C Macro. Only used if I2C connected
2	ROX	FW_PIB_BUS_READ_NVLD_ERR: Bits from I2C Macro. Only used if I2C connected
3	ROX	FW_PIB_BUS_ADDR_PAR_ERR: Bits from I2C Macro. Only used if I2C connected
4	ROX	FW_PIB_BUS_PAR_ERR: Bits from I2C Macro. (Parity error from PIB (signal from pib_slave_interface))
5	ROX	FW_LOCAL_BUS_PAR_ERR: Bits from I2C Macro.
6:37	ROX	FW_READ_DATA: Read data in case of a read operation
38:40	ROX	PIB_MASTER_RESP_INFO_FOR_FW_ACTION: Response Info of PIB Master in case any Slave is connected
41:43	ROX	ECCB_ERROR_INFO_FOR_FW_ACTION: 100 = pib_control_reg_data_lgt_err 101 = pib_control_reg_addr_lgt_err 110 = pib_control_reg_addr_bdy_err 011 = eff_pibs_reset 010 = eff_pibm_reset
44	ROX	FW_ECCB_OP_BUSY: Last Request has not finished. Data are available when bit is 0
45	ROX	FW_PIB_INVALID_COMMAND: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected
46	ROX	FW_PIB_PARITY_ERR: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected
47	ROX	FW_I2C_BACK_END_OVERRUN_ERR: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected
48	ROX	FW_I2C_BACK_END_ACCESS_ERR: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected
49	ROX	FW_I2C_ARBITRATION_LOST_ERR: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected
50	ROX	FW_I2C_NACK_RECIEVED_ERR: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected
51	ROX	FW_I2C_DATA_REQUEST: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected
52	ROX	FW_I2C_COMMAND_COMPLETE: ECCB completed the command
53	ROX	FW_I2C_STOP_ERR: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected
54	ROX	FW_I2C_PORT_BUSY: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected



Bits	PIB	Field Mnemonic: Description
55	ROX	FW_I2C_INTERFACE_BUSY: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected
56	ROX	FW_PARITY_ERROR: I2C Address register or ECC Address Register Parity Error
57:63	ROX	FW_READ_DATA_LENGTH: Read data length - right aligned+E62

Register Name	<i>ECCB : FWDData Register</i>
Mnemonic	EH.TPCHIP.PIB.LPCM.ECCB.FWDATA_REG
Address	00000000000B0023 (PIB)
Attributes	Secure=true
Description	

Bits	PIB	Field Mnemonic: Description
0:31	RWX	FW_DATA_REGISTER: Write data in case of write and data has not been complete transferred via control register. Complete read data in case of a read.

Register Name	<i>ECCB : Control Register</i>
Mnemonic	EH.TPCHIP.PIB.ECCB.CONTROL_REG
Address	00000000000C0000 (PIB)
Attributes	Secure=true
Description	

Bits	PIB	Field Mnemonic: Description
0	WO	I2C_CNTL_WITHSTART: If the With Start bit is set to b1, then a Start Condition will precede any command for data transfer on the I2C bus
1	WO	I2C_CNTL_WITHADDR: When With Address is set to b1, it indicates that the address field in the Command Register (bits 8 to 14) contains an I2C slave device address
2	WO	I2C_CNTL_READCONT: Indicates this read will continue and more data will be requested on the I2C interface
3	WO	I2C_CNTL_WITHSTOP: When Stop is set to b1, it will generate a stop sequence on the I2C bus after the transfer is complete
4:7	WO	I2C_CNTL_DATA_LENGTH: Requested Data Length of Operation
8:14	WO	I2C_CNTL_DEV_ADDR: The Device Address field in the command register holds the device address to be sent to the I2C bus if the With Address bit is set to b1.
15	WO	I2C_CNTL_RNW: Read not Write Operation
16:17	WO	I2C_CNTL_SPEED: 00= No change , this will not change the bit rate divisor . Whatever value is already residing there will stay as it is. 01=400K 10=3400K 11=50K
18:22	WO	I2C_CNTL_PORT_NUMBER: The I2C engine provides 64 I2C interfaces (ports). One out of these four I2C ports is selected by setting Port Number (0 to 5)

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Bits	PIB	Field Mnemonic: Description
23:25	WO	I2C_CNTL_ADDR_LENGTH: 000= No register address in data field 001= 1 Byte of the data field is Register address 010= 2 Byte of the data field are Register address 011= 3 Byte of the data field are Register address 100= 4 Byte of the data field are Register address others are not allowed
26	WO	I2C_CNTL_ENHANCED_MODE: Stop Only command sends immediately a Stop condition.
27:31	WO	I2C_CNTL_UNUSED: UNUSED Bits
32:63	WO	I2C_CNTL_DATA: When register address = 4 Byte this field contains only reg address. In case reg. Address < 4 the field contains reg address and data in the remaining bytes.

Register Name	ECCB : Status Register
Mnemonic	EH.TPCHIP.PIB.ECCB.STATUS_REG
Address	00000000000C0002 (PIB)
Attributes	Secure=true
Description	

Bits	PIB	Field Mnemonic: Description
0	ROX	PIB_BUS_ADDR_NVLD_ERR: Bits from I2C Macro. Only used if I2C connected
1	ROX	PIB_BUS_WRITE_NVLD_ERR: Bits from I2C Macro. Only used if I2C connected
2	ROX	PIB_BUS_READ_NVLD_ERR: Bits from I2C Macro. Only used if I2C connected
3	ROX	PIB_BUS_ADDR_PAR_ERR: Bits from I2C Macro. Only used if I2C connected
4	ROX	PIB_BUS_PAR_ERR: Bits from I2C Macro. (Parity error from PIB (signal from pib_slave_interface))
5	ROX	LOCAL_BUS_PAR_ERR: Bits from I2C Macro.
6:37	ROX	READ_DATA: Read data in case of a read operation
38:40	ROX	PIB_MASTER_RESP_INFO: Response Info of PIB Master in case any Slave is connected
41:43	ROX	ECCB_ERROR_INFO: 100 = pib_control_reg_data_lgt_err 101 = pib_control_reg_addr_lgt_err 110 = pib_control_reg_addr_bdy_err 111 = pib_eccaddr_reg_err 011 = eff_pibs_reset 010 = eff_pibm_reset 001 = uce_q
44	ROX	ECCB_OP_BUSY: Last Request has not finished. Data are available when bit is 0
45	ROX	PIB_INVALID_COMMAND: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected
46	ROX	PIB_PARITY_ERR: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected
47	ROX	I2C_BACK_END_OVERRUN_ERR: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected
48	ROX	I2C_BACK_END_ACCESS_ERR: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected
49	ROX	I2C_ARBITRATION_LOST_ERR: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected
50	ROX	I2C_NACK_RECIEVED_ERR: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected



Bits	PIB	Field Mnemonic: Description
51	ROX	I2C_DATA_REQUEST: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected
52	ROX	I2C_COMMAND_COMPLETE: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected
53	ROX	I2C_STOP_ERR: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected
54	ROX	I2C_PORT_BUSY: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected
55	ROX	I2C_INTERFACE_BUSY: Bits from I2C Engine status register(refer I2C engine documentation for details). Only used if I2C is connected
56	ROX	PARITY_ERROR: I2C Address register or ECC Address Register Parity Error
57	ROX	CE_COUNTER_OVERFLOW: More than 128 correctable ecc errors detected.
58:63	ROX	READ_DATA_LENGTH: Read data length - right aligned

Register Name		<i>ECCB : Data Register</i>
Mnemonic		EH.TPCHIP.PIB.ECCB.DATA_REG
Address		00000000000C0003 (PIB)
Attributes		Secure=true
Description		

Bits	PIB	Field Mnemonic: Description
0:63	RWX	DATA_REGISTER: Write data in case of write and data has not been complete transferred via control register. Complete read data in case of a read.

Register Name		<i>SBE: Status Register</i>
Mnemonic		EH.TPCHIP.PIB.SBE.STATUS_REG
Address		00000000000E0000 (PIB)
Attributes		Secure=true
Description		

Bits	PIB	Field Mnemonic: Description
0:7	ROX	SM_STAT: Instruction engine State Machine State: 000 & state_vector(0:3) & bad_instruction_parity
8	ROX	FREEZE_PORE_ACTION_MASKED: Operation frozen due to SBE/PORE freeze action input (that is, system checkstop).
9	ROX	EXE_TRIGGER_WR_REQ_Q: Interrupt pending. 0 = No interrupt pending. 1 = An interrupt is pending.
10:11	RO	Constant = 0b00
12:15	ROX	PC_STACK_CURRENT_STATE: Stack Pointer, 0001 = empty, 0010 = filled up to level 1, 0100 = filled up to level 2, 0100 = filled up to level 3 (error handler only)
16:63	ROX	PC_Q: ProgramCounter is fetch-address for POR instructions in 48-bit representation, counting in bytes. Initial value is x8000000000000000.



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Register Name		SBE: Control and Debug Register
Mnemonic		EH.TPCHIP.PIB.SBE.CONTROL_REG
Address		00000000000E0001 (PIB)
Attributes		Secure=true
Description		
Bits	PIB	Field Mnemonic: Description
0	RWX	CTL_NO_LB: IE Stop/Run bit: 0-> Automatic run-mode. 1-> STOP/debug mode. This gets cleared (run mode) upon SCOM write or Write to EXE Trigger register. This gets set (STOP/debug mode) upon SCOM write or exec WAIT 0 or System Check Stop (when enabled) or Stop on error (when enabled) or PORE IE RESET from user (SCOM Operation).
1	NCX	CTL_POR_CONT: IE Continue bit (writing '1' makes pulse) when stopped at breakpoint or SCAND-CRC-error, Unaffected by Bit(3).
2	NCX	CTL_POR_SKIP: IE Skip instruction (writing '1' makes pulse), when stopped, PC<--PC+1, to skip a long instruction write into this bit 3 times, unaffected by Bit(3).
3	NCX	CTL_SETPC: IE Set-PC (writing '1' makes pulse): Set PC to value in bits 16:63.
4:6	RWX	CTL_SCAN_CLKDIV: IE Scanclk divider setting for SCAND instruction, default 000 = nclk/32.
7	RWX	CTL_EXE_LOCK: EXE register lock bit, not written when Bit(3)='1', Control register never gets locked.
8	RWX	CTL_FREEZE_PORE_ACTION_MASK: Mask bit to freeze action based on system xstop. '0' : Not masked(default), pore_freeze_action possible '1' : Masked
9	RWX	CTL_INSTR_PAR_EN: Instruction parity check enable, 0 = parity check disabled, 1 = parity check enabled
10	RWX	CTL_PIB_PAR_EN_B: PIB parity check disable, 0 = parity check enabled, 1 = parity check disabled
11	RWX	CTL_TRAP_EN: Trap enable, 0 = disabled, 1 = enabled
12	RWX	CTL_TRC_NARROW_EN: Trace Bus narrow mode, 0 = drive all 88 trace bus pins, 1 = drive only first 8 bit of trace bus (remaining 80 bits are forced to zero)
13	RWX	CTL_INT_ENABLE: PORE interruptible indication (only valid for interruptible PORE instances), 0 = PORE is not interruptible, 1 = PORE is interruptible
14	RWX	CTL_DONE_OVR: PORE done overwrite, 0 = no overwrite of PMC done indicator, 1 = force PMC done indicator to 1
15	RWX	CTL_INTERRUPT_CHKSW: Interruptible PORE feature on/off, 0 = This PORE instance is not interruptible, 1 = This PORE instance is interruptible
16:63	RWX	CTL_ABR: IE When written with Bit(3)='0':sets Program Counter break point address, When written with Bit(3)='1':Value is written into PC(breakpoint address unchanged), Upon a read the PC breakpoint address is always returned

Register Name		SBE: Reset Register
Mnemonic		EH.TPCHIP.PIB.SBE.RESET_REG
Address		00000000000E0002 (PIB)
Attributes		Secure=true
Description		
Bits	PIB	Field Mnemonic: Description
0	RWX	PORE_IE_RESET_TRIGGER: Trigger functional reset of PORE/SBE IE, clears all register include debug regs, but does not clear ERROR MASK register.
1	RWX	PORE_OCI_RESET_TRIGGER: Trigger PORE to OCI reset



Bits	PIB	Field Mnemonic: Description
2	RWX	SBE_RESTART_TRIGGER: Trigger functional and OCI reset and then restarts the SBE
3	RWX	CHKSW_HW215170: Debug switch for HW215170. 0b0 : Fix enabled (default) 0b1: Fix disabled
4	RWX	CHKSW_HW217012: Debug switch for HW217012. 0b0 : Fix enabled (default) 0b1: Fix disabled
5	RWX	CHKSW_HW237648: Debug switch for HW237648. 0b0 : Fix enabled (default) 0b1: Fix disabled

Register Name	SBE: Error Mask Register
Mnemonic	EH.TPCHIP.PIB.SBE.ERROR_MASK_REG
Address	00000000000E0003 (PIB)
Attributes	Secure=true
Description	

Bits	PIB	Field Mnemonic: Description
0:4	RW	ERROR_INTERRUPT_ENABLE: bit 0: error event 0 bit 1: error event 1 bit 2: error event 2 bit 3: error event 3 bit 4: spare bit set to 1 triggers corresponding error handler
5:9	RW	ERROR_FIR_ENABLE: bit 0: error event 0 bit 1: error event 1 bit 2: error event 2 bit 3: error event 3 bit 4: error event 4 bit set to 1 triggers pulse on PORE_error_out line
10:14	RW	ERROR_FATAL_ENABLE: bit 0: error event 0 bit 1: error event 1 bit 2: error event 2 bit 3: error event 3 bit 4: error event 4 bit set to 1 triggers pulse on PORE_fatal_error_out line
15:19	RW	STOP_PORE: bit 0: error event 0 bit 1: error event 1 bit 2: error event 2 bit 3: error event 3 bit 4: error event 4. Bit set to `1` stops PORE execution.
20	RW	GATE_PIB_CHIPLET_OFFLINE: Chiplet offline return code (010) triggers error event 0 if reset; otherwise, it does not trigger an error event.
21:24	RW	I2C_ERROR_MASK: bit 0: mask i2c errors type 1 (I2CM internal and parity) bit 1: mask i2c error type 2 (Bad PIB resp I2CM -> ECCAX) bit 2: mask i2c error type 3 (ECCAX internal) bit 3: mask i2c error type 4 (I2C bus errors)
25:29	RW	GROUP_PARITY_MASK: masks for parity error detection of registers bit 25 : debug,status,error mask,pc stack registers bit 26: control, exe trigger, exe t_mask, i2c param registers bit 27: perv/oci base addr, table base addr, memory reloc, bit 28: scr0, scr1, scr2, and data scr0 register bit 29: ibuf register

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Register Name		<i>SBE: Pervasive Base Address 0 Register</i>
Mnemonic		EH.TPCHIP.PIB.SBE.PERV_BASE_ADDRESS_0_REG
Address		00000000000E0004 (PIB)
Attributes		Secure=true
Description		
Bits	PIB	Field Mnemonic: Description
0:24	RO	Constant = 0b000000000000000000000000
25	RWX	MULTICAST_BIT_0: Multicast Bit for Base Address0 used for Pervasive accesses during execution phase of instructions.
26:31	RWX	CHIPLET_ID_0: Base Address0 used for Pervasive accesses during execution phase of instructions. Bits used as chiplet ID or Multicast Group part of the pervasive addresses leaving PRV PIBMS. This value can be incremented using the ADDI instruction from PORE instruction set

Register Name		<i>SBE: Pervasive Base Address 1 Register</i>
Mnemonic		EH.TPCHIP.PIB.SBE.PERV_BASE_ADDRESS_1_REG
Address		00000000000E0005 (PIB)
Attributes		Secure=true
Description		
Bits	PIB	Field Mnemonic: Description
0:24	RO	Constant = 0b000000000000000000000000
25	RWX	MULTICAST_BIT_1: Multicast Bit for Base Address1 used for Pervasive accesses during execution phase of instructions.
26:31	RWX	CHIPLET_ID_1: Base Address1 used for Pervasive accesses during execution phase of instructions. Bits used as chiplet ID part of the pervasive addresses leaving PRV PIBMS. This value can be incremented using the ADDI instruction from PORE instruction set

Register Name		<i>SBE: OCI Base Address 0 Register</i>
Mnemonic		EH.TPCHIP.PIB.SBE.OCI_BASE_ADDRESS_0_REG
Address		00000000000E0006 (PIB)
Attributes		Secure=true
Description		
Bits	PIB	Field Mnemonic: Description
0:17	RO	Constant = 0b00000000000000000000
18:23	RWX	SBE_FI2C_BASE_PCB_SLAVE_0: SBE Fast I2C Base 0 - PCB Slave ID: Used in SBE to identify the Fast I2C protocol memory space, unused in SLW/GPE
24:27	RWX	SBE_FI2C_BASE_PIB_ID_0: SBE Fast I2C Base 0 - PIB master ID: Used in SBE to identify the Fast I2C protocol memory space, unused in SLW/GPE
28:31	RWX	SBE_FI2C_BASE_PORT_ID_0: SBE Fast I2C Base 0 - Pervasive Port ID: Used in SBE to identify the Fast I2C protocol memory space, unused in SLW/GPE
32:63	RWX	OCI_BASE_ADDR_0: Base Address0 used for OCI/FI2C accesses during execution phase of instructions. Added to address parameter of instruction. This value can be incremented using the ADDI instruction from PORE instruction set



Register Name		SBE: OCI Base Address 1 Register
Mnemonic		EH.TPCHIP.PIB.SBE.OCI_BASE_ADDRESS_1_REG
Address		00000000000E0007 (PIB)
Attributes		Secure=true
Description		
Bits	PIB	Field Mnemonic: Description
0:17	RO	Constant = 0b000000000000000000
18:23	RWX	SBE_FI2C_BASE_PCB_SLAVE_1: SBE Fast I2C Base 1 - PCB Slave ID: Used in SBE to identify the Fast I2C protocol memory space, unused in SLW/GPE
24:27	RWX	SBE_FI2C_BASE_PIB_ID_1: SBE Fast I2C Base 1 - PIB master ID: Used in SBE to identify the Fast I2C protocol memory space, unused in SLW/GPE
28:31	RWX	SBE_FI2C_BASE_PORT_ID_1: SBE Fast I2C Base 1 - Pervasive Port ID: Used in SBE to identify the Fast I2C protocol memory space, unused in SLW/GPE
32:63	RWX	OCI_BASE_ADDR_1: Base Address1 used for OCI/FI2C accesses during execution phase of instructions. Added to address parameter of instruction. This value can be incremented using the ADDI instruction from PORE instruction set

Register Name		SBE: Table Base Address Register
Mnemonic		EH.TPCHIP.PIB.SBE.TABLE_BASE_ADDRESS_REG
Address		00000000000E0008 (PIB)
Attributes		Secure=true
Description		
Bits	PIB	Field Mnemonic: Description
0:15	RO	Constant = 0b0000000000000000
16	RWX	TABLE_BASE_ADDR_INTERFACE: Interface used to access the Base Table (used for Start Vectors and Error Handlers): 0 = PIB/PERV, 1 = OCI/FI2C
17	RWX	RESERVED: reserved
18:23	RWX	TABLE_BASE_ADDR_CHIPLET_ID: In case of PIB/PERV or FI2C interface, this field defines the pervasive chiplet ID, unused for OCI
24:27	RWX	TABLE_BASE_ADDR_PIB_ID: In case of PIB/PERV or FI2C interface, this field defines the PIB master ID, unused for OCI
28:31	RWX	TABLE_BASE_ADDR_PORT_ID: In case of PIB/PERV or FI2C interface, this field defines the pervasive port ID, unused for OCI
32:63	RWX	TABLE_BASE_ADDR: Table base address for jump table. This value can be incremented using the ADDI instruction from PORE instruction set

Register Name		SBE: EXE Trigger Register
Mnemonic		EH.TPCHIP.PIB.SBE.EXE_TRIGGER_REG
Address		00000000000E0009 (PIB)
Attributes		Secure=true
Description		
Bits	PIB	Field Mnemonic: Description
0:7	RO	Constant = 0b00000000

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Bits	PIB	Field Mnemonic: Description
8:11	RWX	START_VECTOR: Writing to start_vector causes PORE to enter run mode at the corresponding address given by (start_vector X 3) + 0x0018. This register is locked when CONTROL_REG bit(0) is '0'(in run mode) or if CONTROL_REG bit(7) is '1'(CTL_EXE_LOCK). The start vector is cleared upon PORE IE RESET
12:31	RO	Constant = 0b00000000000000000000
32:63	RWX	START_PARAMETER: One bit for each chiplet, bit(32 to 47) -> chiplets 0 to 15, which determines whether this chiplet is part of the mc accesses. This register is locked when CONTROL_REG bit(0) is '0'(in run mode) or if CONTROL_REG bit(7) is '1'(CTL_EXE_LOCK). The start_parameter is cleared upon PORE IE RESET

Register Name	SBE: Scratch0 Register, Address
Mnemonic	EH.TPCHIP.PIB.SBE.SCRATCH0_REG
Address	0000000000E000A (PIB)
Attributes	Secure=true
Description	

Bits	PIB	Field Mnemonic: Description
0:7	RO	Constant = 0b00000000
8:31	RWX	SCRATCH0: POR IE Scratch0 register, 24b, This register is locked upon CONTROL_REG bit(0) is '0'

Register Name	SBE: Scratch1 Register, Data
Mnemonic	EH.TPCHIP.PIB.SBE.SCRATCH1_REG
Address	0000000000E000B (PIB)
Attributes	Secure=true
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RWX	SCRATCH1: POR IE Scratch1 Register, 64-bit data buffer. This register is locked when CONTROL_REG bit(0) is '0'.

Register Name	SBE: Scratch2 Register, Data
Mnemonic	EH.TPCHIP.PIB.SBE.SCRATCH2_REG
Address	0000000000E000C (PIB)
Attributes	Secure=true
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RWX	SCRATCH2: POR IE Scratch2 Register, 64-bit data buffer. This register is locked when CONTROL_REG bit(0) is '0'.



Register Name		SBE: First 64 Bits of the Instruction Buffer
Mnemonic		EH.TPCHIP.PIB.SBE.IBUF_01_REG
Address		00000000000E000D (PIB)
Attributes		Secure=true
Description		
Bits	PIB	Field Mnemonic: Description
0:63	RWX	IBUF_LO: POR IE Instruction Buffer, bits 0-63. This register is locked when CONTROL_REG bit(0) is '0'.

Register Name		SBE: Last 32 Bits of the Instruction Buffer
Mnemonic		EH.TPCHIP.PIB.SBE.IBUF_2_REG
Address		00000000000E000E (PIB)
Attributes		Secure=true
Description		
Bits	PIB	Field Mnemonic: Description
0:31	RWX	IBUF_2: POR IE Instruction Buffer, bits 64 - 95. This register is locked when CONTROL_REG bit(0) is '0'.

Register Name		SBE: Debug 0 Register
Mnemonic		EH.TPCHIP.PIB.SBE.DBG0_REG
Address		00000000000E000F (PIB)
Attributes		Secure=true
Description		
Bits	PIB	Field Mnemonic: Description
0:31	RWX_WCLRR EG	LAST_PIBMS_ACCESS_ADDRESS: POR PIB Master: Address of last completed access. Register is cleared on PORE IE Reset.
32	RWX_WCLRR EG	PIB_DATA_READ_P_ERR: Parity error in read data from PRV PIB
33:35	RWX_WCLRR EG	LAST_PIBMS_ACCESS_RETURN_CODE: POR PIB Master: Last Return Code from PIB/PCB (SCRESP): For example: 000: OK 010: Chiplet offline 100: Invalid address 110: Parity error / unexpected/wrong packet 111: Timeout
36	RWX_WCLRR EG	I2C_BAD_STATUS_0: I2CM internal errors including parity errors
37	RWX_WCLRR EG	I2C_BAD_STATUS_1: bad PIB response code error for ECCAX to I2CM communication
38	RWX_WCLRR EG	I2C_BAD_STATUS_2: ECCAX internal errors (UCE or PIB master resets)
39	RWX_WCLRR EG	I2C_BAD_STATUS_3: I2C bus issues (I2C bus busy, NACK, stop bit error)
40	RWX_WCLRR EG	GROUP_PARITY_ERROR_0: parity error from debug or status or error mask or pc stack regs



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Bits	PIB	Field Mnemonic: Description
41	RWX_WCLRR EG	GROUP_PARITY_ERROR_1: parity error from control or exe trigger or exe t_mask or i2c param regs
42	RWX_WCLRR EG	GROUP_PARITY_ERROR_2: parity error from perv/oci base addr or table base addr or memory reloc
43	RWX_WCLRR EG	GROUP_PARITY_ERROR_3: parity error from scr0 or scr1 or scr2 or data scr0 reg
44	RWX_WCLRR EG	GROUP_PARITY_ERROR_4: parity error from ibuf reg
45:52	ROX	INTERRUPT_COUNTER_Q: Counter, which tracks the number of instructions executed after the exe trigger wr request is queued and interrupt enable is not set

Register Name	SBE: Debug 1 Register
Mnemonic	EH.TPCHIP.PIB.SBE.DBG1_REG
Address	00000000000E0010 (PIB)
Attributes	Secure=true
Description	

Bits	PIB	Field Mnemonic: Description
0:31	RWX_WCLRR EG	LAST_PC_ACCESS_ADDRESS_0_31: POR PC: Address of last completed PC access. Register is cleared on PORE IE Reset.
32:47	RWX_WCLRR EG	LAST_PC_ACCESS_ADDRESS_32_47: POR PC: Address of last completed PC access. Register is cleared on PORE IE Reset.
48	RWX_WCLRR EG	OCI_DATA_READ_P_ERR: Parity error in read data from OCI.
49:51	RWX_WCLRR EG	LAST_OCIMS_ACCESS_RETURN_CODE: POR OCI Master: Last Return Code from OCI (Error).
52	RWX_WCLRR EG	BAD_PAR: Bad instruction parity.
53	RWX_WCLRR EG	BAD_INSTRUCTION: Invalid instruction.
54	RWX_WCLRR EG	BAD_PC: PC Overflow/underflow.
55	RWX_WCLRR EG	SCAN_DATA_CRC: Scan data CRC error.
56	RWX_WCLRR EG	PC_STACK_ERR: PC stack PUSH error or POP error.
57	RWX_WCLRR EG	INSTR_FETCH_ERROR: Nonzero return code or read data parity error was received during fetch phase.
58	RWX_WCLRR EG	BAD_OPERAND: Invalid instruction operand
59	RWX_WCLRR EG	BAD_INSTRUCTION_PATH: Invalid instruction path (for example, FI2C parameter miss).
60	RWX_WCLRR EG	BAD_START_VECTOR_TRIGGER: Invalid start vector triggered.
61	RWX_WCLRR EG	FI2C_PROTOCOL_HANG: Fast I2C protocol hang detected - exceeded poll limit for FI2C engine.



Bits	PIB	Field Mnemonic: Description
62	RWX_WCLRR EG	ROL_INVALID: Rotate invalid.
63	RWX_WCLRR EG	PIBMS_DBG_LOCK: Lock debug0/1 registers on occurrence of error events 0-3. That is, when any one of PIBMS DBG0 Register(32:35) OR PIBMS DBG1 Register(48:55) is set.

Register Name	<i>SBE: Stack Level 0 Register</i>
Mnemonic	EH.TPCHIP.PIB.SBE.PC_STACK0_REG
Address	00000000000E0011 (PIB)
Attributes	Secure=true
Description	

Bits	PIB	Field Mnemonic: Description
0:47	RWX	STACK0_DATA: stack data level 0
48:58	RO	Constant = 0b000000000000
59	RWX	SET_STACK_POINTER: If set, the value in bits 60:63 is applied as a new stack pointer.
60:63	RWX	NEW_STACK_POINTER: If bit 59 is set, the Stack Pointer is overwritten: 0001 = Stack empty 0010 = Stack filled up to level 0 0100 = Stack filled up to level 1 1000 = Stack filled up to level 2

Register Name	<i>SBE: Stack Level 1 Register</i>
Mnemonic	EH.TPCHIP.PIB.SBE.PC_STACK1_REG
Address	00000000000E0012 (PIB)
Attributes	Secure=true
Description	

Bits	PIB	Field Mnemonic: Description
0:47	RWX	STACK1_DATA: Stack data level 1

Register Name	<i>SBE: Stack Level 2 Register</i>
Mnemonic	EH.TPCHIP.PIB.SBE.PC_STACK2_REG
Address	00000000000E0013 (PIB)
Attributes	Secure=true
Description	

Bits	PIB	Field Mnemonic: Description
0:47	RWX	STACK2_DATA: Stack data level 2

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Register Name		SBE: ID Flags Register
Mnemonic		EH.TPCHIP.PIB.SBE.ID_FLAGS_REG
Address		00000000000E0014 (PIB)
Attributes		Secure=true
Description		
Bits	PIB	Field Mnemonic: Description
0:31	RO	Constant = 0b00000000000000000000000000000000
32	ROX	PIB_EXECUTION_PARITY_FAIL: PIB execution phase parity error indicator. Holds the PIB parity error indicator bit for the last execution phase access.
33:35	ROX	PIB_EXECUTION_STATUS_FIELD: PIB execution phase status indicator. Holds the PIB response status of the last execution phase access.
36	ROX	OCI_EXECUTION_PARITY_FAIL: OCI execution phase parity error indicator. Holds the OCI parity error indication bit for the last execution phase access.
37:39	ROX	OCI_EXECUTION_STATUS_FIELD: OCI execution phase status indicator. Holds the OCI response status of the last execution phase access
40:47	RO	Constant = 0b00000000
48:55	RWX	ALU_FLAGS: ALU flags: UGT, ULT, SGT, SLT, C, O, N, Z
56:63	RO	Constant = 0b00000100

Register Name		SBE: Data0 Register
Mnemonic		EH.TPCHIP.PIB.SBE.DATA0_REG
Address		00000000000E0015 (PIB)
Attributes		Secure=true
Description		
Bits	PIB	Field Mnemonic: Description
0:31	RWX	DATA0: Scratch Data 0

Register Name		SBE: Memory Relocation Register
Mnemonic		EH.TPCHIP.PIB.SBE.MEMORY_RELOC_REG
Address		00000000000E0016 (PIB)
Attributes		Secure=true
Description		
Bits	PIB	Field Mnemonic: Description
0:29	RO	Constant = 0b00000000000000000000000000000000
30:31	RWX	MEM_RELOC_REGION: Memory Relocation Region
32:51	RWX	MEM_RELOC_BASE: Memory Relocation Base Address



Register Name		<i>SBE: Fast I2C Parameter Set 0 Register</i>
Mnemonic		EH.TPCHIP.PIB.SBE.I2C_E0_PARAM_REG
Address		00000000000E0017 (PIB)
Attributes		Secure=true
Description		
Bits	PIB	Field Mnemonic: Description
0:3	RWX	I2C_E0_ENGINE_ID: Fast I2C Parameter Set 0: Engine ID (equals to PIB ID of the addressed Fast I2C engine)
4	RWX	UNUSED1_I2C_E0_PARAM_REG: spare
5:7	RWX	I2C_E0_ADDRESS_RANGE: Fast I2C Parameter Set 0: Memory Device Local Address Range (001 = 8 bit local addressing, 010 = 16 bit local addressing, 011 = 24 bit local addressing, 100 = 32 bit local addressing)
8:10	RWX	UNUSED2_I2C_E0_PARAM_REG: spare
11:15	RWX	I2C_E0_ENGINE_PORT: Fast I2C Parameter Set 0: Engine Port (see Fast I2C document for details)
16	RWX	UNUSED3_I2C_E0_PARAM_REG: spare
17:23	RWX	I2C_E0_DEVICE_ID: Fast I2C Parameter Set 0: Target Device ID (see Fast I2C document for details)
24:25	RWX	UNUSED4_I2C_E0_PARAM_REG: spare
26:27	RWX	I2C_E0_ENGINE_SPEED: Fast I2C Parameter Set 0: Engine Speed Setting (see Fast I2C document for details)
28:31	RWX	I2C_POLL_THRESHOLD: Fast I2C poll threshold for DONE polling (0000 = disabled, 0001 = 2 ³ polls, 0010 = 2 ⁵ polls, ..., 1101 = 2 ²⁷ polls, 1110 and 1111 = 2 ²⁸ polls)

Register Name		<i>SBE: Fast I2C Parameter Set 1 Register</i>
Mnemonic		EH.TPCHIP.PIB.SBE.I2C_E1_PARAM_REG
Address		00000000000E0018 (PIB)
Attributes		Secure=true
Description		
Bits	PIB	Field Mnemonic: Description
0:3	RWX	I2C_E1_ENGINE_ID: Fast I2C Parameter Set 1: Engine ID (equals to PIB ID of the addressed Fast I2C engine)
4	RWX	UNUSED1_I2C_E1_PARAM_REG: spare
5:7	RWX	I2C_E1_ADDRESS_RANGE: Fast I2C Parameter Set 1: Memory Device Local Address Range (001 = 8 bit local addressing, 010 = 16 bit local addressing, 011 = 24 bit local addressing, 100 = 32 bit local addressing)
8:10	RWX	UNUSED2_I2C_E1_PARAM_REG: spare
11:15	RWX	I2C_E1_ENGINE_PORT: Fast I2C Parameter Set 1: Engine Port (see Fast I2C document for details)
16	RWX	UNUSED3_I2C_E1_PARAM_REG: spare
17:23	RWX	I2C_E1_DEVICE_ID: Fast I2C Parameter Set 1: Target Device ID (see Fast I2C document for details)
24:25	RWX	UNUSED4_I2C_E1_PARAM_REG: spare
26:27	RWX	I2C_E1_ENGINE_SPEED: Fast I2C Parameter Set 1: Engine Speed Setting (see Fast I2C document for details)
28:31	RWX	UNUSED5_I2C_E1_PARAM_REG: spare

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Register Name	SBE: Fast I2C Parameter Set 2 Register
Mnemonic	EH.TPCHIP.PIB.SBE.I2C_E2_PARAM_REG
Address	00000000000E0019 (PIB)
Attributes	Secure=true
Description	

Bits	PIB	Field Mnemonic: Description
0:3	RWX	I2C_E2_ENGINE_ID: Fast I2C Parameter Set 2: Engine ID (equals to PIB ID of the addressed Fast I2C engine)
4	RWX	UNUSED1_I2C_E2_PARAM_REG: spare
5:7	RWX	I2C_E2_ADDRESS_RANGE: Fast I2C Parameter Set 2: Memory Device Local Address Range (001 = 8 bit local addressing, 010 = 16 bit local addressing, 011 = 24 bit local addressing, 100 = 32 bit local addressing)
8:10	RWX	UNUSED2_I2C_E2_PARAM_REG: spare
11:15	RWX	I2C_E2_ENGINE_PORT: Fast I2C Parameter Set 2: Engine Port (see Fast I2C document for details)
16	RWX	UNUSED3_I2C_E2_PARAM_REG: spare
17:23	RWX	I2C_E2_DEVICE_ID: Fast I2C Parameter Set 2: Target Device ID (see Fast I2C document for details)
24:25	RWX	UNUSED4_I2C_E2_PARAM_REG: spare
26:27	RWX	I2C_E2_ENGINE_SPEED: Fast I2C Parameter Set 2: Engine Speed Setting (see Fast I2C document for details)
28:31	RWX	UNUSED5_I2C_E2_PARAM_REG: spare

Register Name	PBAM FIR Action0 Register
Mnemonic	EH.TPCHIP.PIB.LPCM.LPC.SYNC_FIR_ACTION0_REG
Address	0000000001010C06 (SCOM)
Attributes	
Description	Nest FIR Action0 Register Action select for corresponding bit in FIR (Action0,Action1) = Action Select (0,0) = No Error (0,1) = recoverable error (1,0) = Checkstop Error (1,1) = unused

Bits	SCOM	Field Mnemonic: Description
0	RO	INVALID_TRANSFER_SIZE_ACTION0: action0_for_invalid_transfer_size
1	RO	INVALID_COMMAND_ACTION0: action0_for_invalid_command
2	RO	INVALID_ADDRESS_ALIGNMENT_ACTION0: action0_for_invalid_address_alignment
3	RO	OPB_ERROR_ACTION0: action0_for_OPB_error
4	RO	OPB_TIMEOUT_ACTION0: action0_for_OPB_timeout
5	RO	OPB_MASTER_HANG_TIMEOUT_ACTION0: action0_for_OPB_master_hang_timeout
6	RO	CMD_BUFFER_PAR_ERR_ACTION0: action0_for_OPB_master_cmd_buffer_parity_error
7	RO	DAT_BUFFER_PAR_ERR_ACTION0: action0_for_OPB_master_dat_buffer_parity_error
8	RO	RETURNQ_ERR_ACTION0: reserved_bit_1
9	RO	RESERVED_ACTION0: action0_for_reserved0
10	RO	SYNC_SCOM_PARITY_ERR2_ACTION0: action0_for_Local FIR Parity Error RAS duplicate



Bits	SCOM	Field Mnemonic: Description
11	RO	SYNC_SCOM_PARITY_ERR_ACTION0: action0_for_Mask Local FIR Parity Error of ACTION/MASK registers
12:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	PBAM FIR Action1 Register
Mnemonic	EH.TPCHIP.PIB.LPCM.LPC.SYNC_FIR_ACTION1_REG
Address	0000000001010C07 (SCOM)
Attributes	
Description	Nest FIR action1 Register Action select for corresponding bit in FIR (Action0,Action1) = Action Select (0,0) = No Error (0,1) = recoverable error (1,0) = Checkstop Error (1,1) = unused

Bits	SCOM	Field Mnemonic: Description
0	RO	INVALID_TRANSFER_SIZE_ACTION1: action1_for_invalid_transfer_size
1	RO	INVALID_COMMAND_ACTION1: action1_for_invalid_command
2	RO	INVALID_ADDRESS_ALIGNMENT_ACTION1: action1_for_invalid_address_alignment
3	RO	OPB_ERROR_ACTION1: action1_for_OPB_error
4	RO	OPB_TIMEOUT_ACTION1: action1_for_OPB_timeout
5	RO	OPB_MASTER_HANG_TIMEOUT_ACTION1: action1_for_OPB_master_hang_timeout
6	RO	CMD_BUFFER_PAR_ERR_ACTION1: action1_for_OPB_master_cmd_buffer_parity_error
7	RO	DAT_BUFFER_PAR_ERR_ACTION1: action1_for_OPB_master_dat_buffer_parity_error
8	RO	RETURNQ_ERR_ACTION1: reserved_bit_1
9	RO	RESERVED_ACTION1: action1_for_reserved_bit_0
10	RO	SYNC_SCOM_PARITY_ERR2_ACTION1: action1_for_Local FIR Parity Error RAS duplicate
11	RO	SYNC_SCOM_PARITY_ERR_ACTION1: action1_for_Mask Local FIR Parity Error of ACTION/MASK registers
12:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	Trace Array High Data Register
Mnemonic	EH.TPC.TR1.SAMP.LEAF.COMP.TRACE_HI_DATA_REG
Address	0000000002010440 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63

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Register Name		<i>Trace Array Low Data Register</i>
Mnemonic		EH.TPC.TR1.SAMP.LEAF.COMP.TRACE_LO_DATA_REG
Address		0000000002010441 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95
32:41	ROX	TRACE_ADDRESS: Trace Address
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank
51	ROX	TRACE_LAST_BANK_VALID: Trace Last Bank Valid
52	ROX	TRACE_WRITE_ON_RUN: Trace Write-On-Run indicator
53	ROX	TRACE_RUNNING: Trace Run indicator
54:63	ROX	TRACE_HOLD_ADDRESS: Trace Hold Address (pointing to last entry)

Register Name		<i>Trace Array High Data Register</i>
Mnemonic		EH.TPC.TR2.SAMP.LEAF.COMP.TRACE_HI_DATA_REG
Address		0000000002010480 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63

Register Name		<i>Trace Array Low Data Register</i>
Mnemonic		EH.TPC.TR2.SAMP.LEAF.COMP.TRACE_LO_DATA_REG
Address		0000000002010481 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95
32:41	ROX	TRACE_ADDRESS: Trace Address
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank
51	ROX	TRACE_LAST_BANK_VALID: Trace Last Bank Valid
52	ROX	TRACE_WRITE_ON_RUN: Trace Write-On-Run indicator
53	ROX	TRACE_RUNNING: Trace Run indicator
54:63	ROX	TRACE_HOLD_ADDRESS: Trace Hold Address (pointing to last entry)



Register Name		<i>Trace Array High Data Register</i>
Mnemonic		EH.TPC.TR3.SAMP.LEAF.COMP.TRACE_HI_DATA_REG
Address		00000000020104C0 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63

Register Name		<i>Trace Array Low Data Register</i>
Mnemonic		EH.TPC.TR3.SAMP.LEAF.COMP.TRACE_LO_DATA_REG
Address		00000000020104C1 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95
32:41	ROX	TRACE_ADDRESS: Trace Address
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank
51	ROX	TRACE_LAST_BANK_VALID: Trace Last Bank Valid
52	ROX	TRACE_WRITE_ON_RUN: Trace Write-On-Run indicator
53	ROX	TRACE_RUNNING: Trace Run indicator
54:63	ROX	TRACE_HOLD_ADDRESS: Trace Hold Address (pointing to last entry)

Register Name		<i>Trace Array High Data Register</i>
Mnemonic		EH.TPC.TR4.SAMP.LEAF.COMP.TRACE_HI_DATA_REG
Address		0000000002010500 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63

Register Name		<i>Trace Array Low Data Register</i>
Mnemonic		EH.TPC.TR4.SAMP.LEAF.COMP.TRACE_LO_DATA_REG
Address		0000000002010501 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95
32:41	ROX	TRACE_ADDRESS: Trace Address
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank



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Bits	SCOM	Field Mnemonic: Description
51	ROX	TRACE_LAST_BANK_VALID: Trace Last Bank Valid
52	ROX	TRACE_WRITE_ON_RUN: Trace Write-On-Run indicator
53	ROX	TRACE_RUNNING: Trace Run indicator
54:63	ROX	TRACE_HOLD_ADDRESS: Trace Hold Address (pointing to last entry)

Register Name	<i>Trace Array High Data Register</i>
Mnemonic	EH.TPC.TR5.SAMP.LEAF.COMP.TRACE_HI_DATA_REG
Address	0000000002010540 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63

Register Name	<i>Trace Array Low Data Register</i>
Mnemonic	EH.TPC.TR5.SAMP.LEAF.COMP.TRACE_LO_DATA_REG
Address	0000000002010541 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95
32:41	ROX	TRACE_ADDRESS: Trace Address
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank
51	ROX	TRACE_LAST_BANK_VALID: Trace Last Bank Valid
52	ROX	TRACE_WRITE_ON_RUN: Trace Write-On-Run indicator
53	ROX	TRACE_RUNNING: Trace Run indicator
54:63	ROX	TRACE_HOLD_ADDRESS: Trace Hold Address (pointing to last entry)

Register Name	<i>Trace Array High Data Register</i>
Mnemonic	EH.TPC.TR6.SAMP.LEAF.COMP.TRACE_HI_DATA_REG
Address	0000000002010580 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63



Register Name		<i>Trace Array Low Data Register</i>
Mnemonic		EH.TPC.TR6.SAMP.LEAF.COMP.TRACE_LO_DATA_REG
Address		0000000002010581 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95
32:41	ROX	TRACE_ADDRESS: Trace Address
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank
51	ROX	TRACE_LAST_BANK_VALID: Trace Last Bank Valid
52	ROX	TRACE_WRITE_ON_RUN: Trace Write-On-Run indicator
53	ROX	TRACE_RUNNING: Trace Run indicator
54:63	ROX	TRACE_HOLD_ADDRESS: Trace Hold Address (pointing to last entry)

Register Name		<i>Trace Array High Data Register</i>
Mnemonic		EH.TPC.TR7.SAMP.LEAF.COMP.TRACE_HI_DATA_REG
Address		00000000020105C0 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63

Register Name		<i>Trace Array Low Data Register</i>
Mnemonic		EH.TPC.TR7.SAMP.LEAF.COMP.TRACE_LO_DATA_REG
Address		00000000020105C1 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95
32:41	ROX	TRACE_ADDRESS: Trace Address
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank
51	ROX	TRACE_LAST_BANK_VALID: Trace Last Bank Valid
52	ROX	TRACE_WRITE_ON_RUN: Trace Write-On-Run indicator
53	ROX	TRACE_RUNNING: Trace Run indicator
54:63	ROX	TRACE_HOLD_ADDRESS: Trace Hold Address (pointing to last entry)



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Register Name		<i>Trace Array High Data Register</i>
Mnemonic		EH.TPC.TR8.SAMP.LEAF.COMP.TRACE_HI_DATA_REG
Address		0000000002010600 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63

Register Name		<i>Trace Array Low Data Register</i>
Mnemonic		EH.TPC.TR8.SAMP.LEAF.COMP.TRACE_LO_DATA_REG
Address		0000000002010601 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95
32:41	ROX	TRACE_ADDRESS: Trace Address
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank
51	ROX	TRACE_LAST_BANK_VALID: Trace Last Bank Valid
52	ROX	TRACE_WRITE_ON_RUN: Trace Write-On-Run indicator
53	ROX	TRACE_RUNNING: Trace Run indicator
54:63	ROX	TRACE_HOLD_ADDRESS: Trace Hold Address (pointing to last entry)

Register Name		<i>Trace Array High Data Register</i>
Mnemonic		EH.TPC.TR9.SAMP.LEAF.COMP.TRACE_HI_DATA_REG
Address		0000000002010640 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63

Register Name		<i>Trace Array Low Data Register</i>
Mnemonic		EH.TPC.TR9.SAMP.LEAF.COMP.TRACE_LO_DATA_REG
Address		0000000002010641 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95
32:41	ROX	TRACE_ADDRESS: Trace Address
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank



Bits	SCOM	Field Mnemonic: Description
51	ROX	TRACE_LAST_BANK_VALID: Trace Last Bank Valid
52	ROX	TRACE_WRITE_ON_RUN: Trace Write-On-Run indicator
53	ROX	TRACE_RUNNING: Trace Run indicator
54:63	ROX	TRACE_HOLD_ADDRESS: Trace Hold Address (pointing to last entry)

Register Name	<i>Trace Array High Data Register</i>
Mnemonic	EN.TPC.TR1.SAMP.LEAF.COMP.TRACE_HI_DATA_REG
Address	0000000002010A00 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63

Register Name	<i>Trace Array Low Data Register</i>
Mnemonic	EN.TPC.TR1.SAMP.LEAF.COMP.TRACE_LO_DATA_REG
Address	0000000002010A01 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95
32:41	ROX	TRACE_ADDRESS: Trace Address
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank
51	ROX	TRACE_LAST_BANK_VALID: Trace Last Bank Valid
52	ROX	TRACE_WRITE_ON_RUN: Trace Write-On-Run indicator
53	ROX	TRACE_RUNNING: Trace Run indicator
54:63	ROX	TRACE_HOLD_ADDRESS: Trace Hold Address (pointing to last entry)

Register Name	<i>Configuration Of CC Counters</i>
Mnemonic	EH.TPC.SYNC_CONFIG
Address	0000000002030000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	ISLE_XSTOP_MASK_B: mask for clockstop of all island clocks on xstop from chiplet
1	RW	PCB_XSTOP_MASK_B: mask for clockstop of all island clocks on xstop from pcb
2	RW	CLKSTP_SYNC_EN: stop clocks aligned to sync pulse
3	RW	EDRAM_XSTOP_MASK_B: mask for clockstop of edram clock on any xstop
4	RW	PLL_XSTOP_MASK_B: mask for clockstop of pll clock on any xstop

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Bits	PCB	Field Mnemonic: Description
5	RW	LOCAL_XSTOP_MASK_B: mask for clockstop of all island clocks on local xstop from chiplet
6	RW	DISABLE_PCB_ITR: disable interrupt generation within CC
7	RW	USE_SYNC_FOR_SCAN: if set, use opcg initial alignment for scan requests
8	RW	KEEP_EDRAM_ON_XSTOP: keep edram enabled when a checkstop occurs
9	RW	TRIGGER_OPCG_ON_XSTOP: trigger opcg on xstop instead of performing clockstop
10	RW	SEL_EXT_OPCG_TRIGGER: select external OPCG trigger (set OPCG in slave mode)
11	RW	LISTEN_TO_SYNC_PULSE: enable phase counter synchronization by sync_pulse signal
12	RW	SYNC_CLK_START_ENABLE: enable clk start driven by tc_sync_clk_stop (falling edge)
13	RW	SYNC_CLK_STOP_ENABLE: enable clk stop driven by tc_sync_clk_stop (rising edge)
14	RWX_WOR	CHIP_PROTECTION_ENABLE: POWER8 Memory Buffer only - can only be set, but not cleared via PCB. When this bit is SET, no clock starts are possible. Only two scan0's will clear this bit
15	RW	SPARE15: spare
16	RW	SPARE16: spare
17	RW	SPARE17: spare
18	RW	SPARE18: spare
19	RW	SPARE19: spare
20	RW	SPARE20: spare

Register Name		PBA Local Fault Isolation Register		
Mnemonic		EN.TPC.PBA.PBAFIR		
Address		0000000002010840 (SCOM) 0000000002010841 (SCOM1) 0000000002010842 (SCOM2)		
Attributes				
Description				
Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PBAFIR_OCI_APAR_ERR: OCI Address Parity Error Det Address parity error detected by PBA OCI Slave logic for any valid address. OCI operation is ignored.
1	RWX	WOX_AND	WOX_OR	PBAFIR_PB_RDADRERR_FW: PB CRESP Addr Error Received for Forwarded Read Request. Processor bus request by PBA for a forwarded OCI read request received a CRESP error response. See PBAERRRPT0 for per-queue information. The buffer allocated for this request continues unless PBACFG[chsw_hang_on_adrerror] = 1. addr_error combined response
2	RWX	WOX_AND	WOX_OR	PBAFIR_PB_RDDATATO_FW: PB Read Data Timeout for Forwarded Request. Processor bus read request for a forwarded OCI request timed out waiting for data. PBA is reporting a data hang condition to the processor bus. The Buffer allocated for this request is hung and may be reset by following the PBA Slave Reset Sequence. See PBAERRRPT0 for per-queue information.
3	RWX	WOX_AND	WOX_OR	PBAFIR_PB_SUE_FW: PB Read Data SUE Error for Forwarded Request. Processor bus read data for a forwarded OCI Request contained SUE error.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
4	RWX	WOX_AND	WOX_OR	PBAFIR_PB_UE_FW: PB Read Data UE Error for Forwarded Request. Processor bus read data for a forwarded OCI request contained UE error.
5	RWX	WOX_AND	WOX_OR	PBAFIR_PB_CE_FW: PB Read Data CE Error for Forwarded Request. Processor bus read data for a forwarded OCI request contained CE error.
6	RWX	WOX_AND	WOX_OR	PBAFIR_OCI_SLAVE_INIT: PBA OCI Slave Initialization Error This is asserted when the upper two OCI address bits indicate they target the PBA Slave but the PBA slave is not setup properly. : No buffer allocated in targeted PBASLVCTLn PBASLVCTLn not enabled for master_id Multiple PBASLVCTLn are enabled for a master_id
7	RWX	WOX_AND	WOX_OR	PBAFIR_OCI_WRPAR_ERR: OCI Write Data Parity Error Detected Data parity error detected by PBA OCI Slave logic. This write and any previous gathered writes are not forwarded.
8	RWX	WOX_AND	WOX_OR	PBAFIR_OCI_REREQTO: OCI Re-Request Timeout PBA OCI Slave timeout on forwarded request that was re-arbitrated. OCI request was deasserted before any data was returned on a read request. The request may have been aborted so this is really not an error. See PBAERRRPT1 for per-queue information. Only 405 will abort requests for prefetched instructions.
9	RWX	WOX_AND	WOX_OR	PBAFIR_PB_UNEXPCRESP: PB Unexpected CRESP. Processor bus combined response was received unexpectedly with PBA transfer tag. Response is ignored. See PBAERRRPT0 for per-queue information.
10	RWX	WOX_AND	WOX_OR	PBAFIR_PB_UNEXPDATA: PB Unexpected Data. Processor bus data received for transaction ID that was not expecting data. Data is ignored. This does not check for duplicate OW_ID. See PBAERRRPT0 for per-queue information.
11	RWX	WOX_AND	WOX_OR	PBAFIR_PB_PARITY_ERR: PB Tag parity Error Detected. Processor bus CRESP TTAG, ATAG, or DPX RTAG parity error detected. FIR set only.
12	RWX	WOX_AND	WOX_OR	PBAFIR_PB_WRADRRERR_FW: PB CRESP Addr Error Received for Forwarded Write Request. Processor bus request by PBA for a forwarded OCI write request received a CRESP error response. See PBAERRRPT0 for per-queue information. addr_error combined response
13	RWX	WOX_AND	WOX_OR	PBAFIR_PB_BADCRESP: PB Invalid CRESP. An invalid CRESP was received for a pending request. PBA will retry the request unless PBACFG[chsw_hang_on_invalid_cresp] = 1. See PBAERRRPT1 for per-queue information.
14	RWX	WOX_AND	WOX_OR	PBAFIR_PB_ACKDEAD_FW_RD: PB CRESP ACK Dead response received for Forwarded Read request to a foreign link. The Buffer allocated for this request will continue unless PBACFG[chsw_hang_on_adrerror] = 1. See PBAERRRPT0 for per-queue information.
15	RWX	WOX_AND	WOX_OR	PBAFIR_PB_CRESPTO: PB CRESPTIMEOUT detected waiting for valid CRESP. Hang detected using processor bus report hang Data_Poll decode. The PBA is reporting an operational hang to the processor bus. See PBAERRRPT1 for per queue information.
16	RWX	WOX_AND	WOX_OR	PBAFIR_BCUE_SETUP_ERR: BCUE Setup Error Block Copy Unload Engine Setup Errors. See PBAERRRPT1. Unexpected 'Start' received while running Timeout Response for OCI Request
17	RWX	WOX_AND	WOX_OR	PBAFIR_BCUE_PB_ACK_DEAD: BCUE Processor Bus Link Dead. ack_dead combined response for processor bus write.
18	RWX	WOX_AND	WOX_OR	PBAFIR_BCUE_PB_ADRERR: PB CRESP Addr Error Received for BCUE Write Request addr_error combined response.

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
19	RWX	WOX_AND	WOX_OR	PBAFIR_BCUE_OCI_DATERR: BCUE Read Data Parity Error OR MRDERR Asserted Block Copy Unload Engine detected parity error on read data from the OCI.
20	RWX	WOX_AND	WOX_OR	PBAFIR_BCDE_SETUP_ERR: BCDE Setup Error Block Copy Download Engine Setup Errors. See PBAERRRPT1. Unexpected 'Start' received while running timeout response for OCI request (OCI address error)
21	RWX	WOX_AND	WOX_OR	PBAFIR_BCDE_PB_ACK_DEAD: BCDE Processor Bus Link Dead ack_dead combined response for Processor Bus Read
22	RWX	WOX_AND	WOX_OR	PBAFIR_BCDE_PB_ADRERR: PB CRESP Addr Error Received for BCDE Read Request addr_error combined response
23	RWX	WOX_AND	WOX_OR	PBAFIR_BCDE_RDDATATO_ERR: PB Read Data Timeout for BCDE Request. Processor bus read request for a BCDE request timed out waiting for data. Timer is based on the hang pulse.
24	RWX	WOX_AND	WOX_OR	PBAFIR_BCDE_SUE_ERR: PB Read Data SUE Error for BCDE Request. Processor bus read data for a BCDE request contained SUE error.
25	RWX	WOX_AND	WOX_OR	PBAFIR_BCDE_UE_ERR: PB Read Data UE Error for BCDE Request. Processor bus read data for a BCDE request contained UE error.
26	RWX	WOX_AND	WOX_OR	PBAFIR_BCDE_CE: PB Read Data CE Error for BCDE Request. Processor bus read data for a BCDE request contained CE error.
27	RWX	WOX_AND	WOX_OR	PBAFIR_BCDE_OCI_DATERR: BCDE Write Data error indicated by OCI Slave Block Copy Download Engine received WRDERR indication from OCI Slave.
28	RWX	WOX_AND	WOX_OR	PBAFIR_INTERNAL_ERR: Internal Logic Error. See PBAERRRPT2 for more detailed information.
29	RWX	WOX_AND	WOX_OR	PBAFIR_ILLEGAL_CACHE_OP: Byte count is less than full cache line: Write operation did not start gathering on a cache line boundary OR the write address was not contiguous before writing the full cache line.
30	RWX	WOX_AND	WOX_OR	PBAFIR_OCI_BAD_REG_ADDR: Illegal access to OCI Register. Invalid address, read to write-only, write to read-only.
31	RWX	WOX_AND	WOX_OR	PBAFIR_AXPUSH_WRERR: Push Write Error. Push queue did not get OCI ADDRACK for push write request. Either the address is invalid or the targeted detected and address parity error. See PBAERRRPT2 for per queue information.
32	RWX	WOX_AND	WOX_OR	PBAFIR_AXRCV_DLO_ERR: PBAXRCV Low data before High Data. See PBAXRCVSTAT[rcv_capture] for more information.
33	RWX	WOX_AND	WOX_OR	PBAFIR_AXRCV_DLO_TO: PBAXRCV Low data timeout. See PBAXRCVSTAT[rcv_capture] for more information.
34	RWX	WOX_AND	WOX_OR	PBAFIR_AXRCV_RSVDATA_TO: PBAXRCV reservation data timeout. Reservation acquired but phase1 data never seen. This could happen if PBAXSND is unable to get access to the processor bus. See PBAXRCVSTAT[rcv_capture] for more information.
35	RWX	WOX_AND	WOX_OR	PBAFIR_AXFLOW_ERR: Illegal PBAX Flow. See PBAERRRPT2 for more info. Write to PBAXSNDTX when PBAXSNDSTAT[snd_in_progress]=1 OR PBAXCFG[pbax_en] = 0 Per queue Push queue underflow: Store to PBAXSHINC when PBAXSHCS[push_empty]. Per queue Push queue overflow: PBAXRCV decode but Push Q is full
36	RWX	WOX_AND	WOX_OR	PBAFIR_AXSND_DHI_RTYTO: PBAXSND engine retry threshold reached sending Phase 1
37	RWX	WOX_AND	WOX_OR	PBAFIR_AXSND_DLO_RTYTO: PBAXSND engine retry threshold reached sending Phase 2



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
38	RWX	WOX_AND	WOX_OR	PBAFIR_AXSND_RSVTO: PBAXSND Reservation Timeout
39	RWX	WOX_AND	WOX_OR	PBAFIR_AXSND_RSVERR: PBAXSND Reservation Error. Reservation request and Reservations not enabled, push queue not enabled, or push queue is full.
40	RWX	WOX_AND	WOX_OR	PBAFIR_PB_ACKDEAD_FW_WR: PB CRESP ACK Dead response received for Forwarded Write request to a foreign link. The Buffer allocated for this request will continue unless PBACFG[chsw_hang_on_adrerror] = 1. See PBAERRRPT0 for per-queue information.
41	RWX	WOX_AND	WOX_OR	PBAFIR_RESERVED_41: Spare
42	RWX	WOX_AND	WOX_OR	PBAFIR_RESERVED_42: Spare
43	RWX	WOX_AND	WOX_OR	PBAFIR_RESERVED_43: Spare
44	RWX	WOX_AND	WOX_OR	PBAFIR_FIR_PARITY_ERR2: Internal fir parity error duplicate
45	RWX	WOX_AND	WOX_OR	PBAFIR_FIR_PARITY_ERR: Internal fir parity error
46:63	RO	N/A	N/A	Constant = 0b000000000000000000

Register Name	<i>PBA Local Fault Isolation Mask Register</i>
Mnemonic	EN.TPC.PBA.PBAFIRMASK
Address	0000000002010843 (SCOM) 0000000002010844 (SCOM1) 0000000002010845 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	PBAFIRMASK_OCI_APAR_ERR_MASK: oci_apar_err_mask
1	RW	WO_AND	WO_OR	PBAFIRMASK_PB_RDADRERR_FW_MASK: pb_rdadrerr_fw_mask
2	RW	WO_AND	WO_OR	PBAFIRMASK_PB_RDDATATO_FW_MASK: pb_rddatato_fw_mask
3	RW	WO_AND	WO_OR	PBAFIRMASK_PB_SUE_FW_MASK: pb_sue_fw_mask
4	RW	WO_AND	WO_OR	PBAFIRMASK_PB_UE_FW_MASK: pb_ue_fw_mask
5	RW	WO_AND	WO_OR	PBAFIRMASK_PB_CE_FW_MASK: pb_ce_fw_mask
6	RW	WO_AND	WO_OR	PBAFIRMASK_OCI_SLAVE_INIT_MASK: oci_slave_init_mask
7	RW	WO_AND	WO_OR	PBAFIRMASK_OCI_WRPAR_ERR_MASK: oci_wrpar_err_mask
8	RW	WO_AND	WO_OR	PBAFIRMASK_OCI_REREQTO_MASK: oci_rereqto_mask
9	RW	WO_AND	WO_OR	PBAFIRMASK_PB_UNEXPCRESP_MASK: pb_unexpcrep_mask
10	RW	WO_AND	WO_OR	PBAFIRMASK_PB_UNEXPDATA_MASK: pb_unexpdata_mask
11	RW	WO_AND	WO_OR	PBAFIRMASK_PB_PARITY_ERR_MASK: pb_parity_err_mask
12	RW	WO_AND	WO_OR	PBAFIRMASK_PB_WRADRERR_FW_MASK: pb_wradrerr_fw_mask
13	RW	WO_AND	WO_OR	PBAFIRMASK_PB_BADCRESP_MASK: pb_badcrep_mask
14	RW	WO_AND	WO_OR	PBAFIRMASK_PB_ACKDEAD_FW_RD_MASK: pb_ackdead_fw_rd_mask
15	RW	WO_AND	WO_OR	PBAFIRMASK_PB_CRESPTO_MASK: pb_crespto_mask
16	RW	WO_AND	WO_OR	PBAFIRMASK_BCUE_SETUP_ERR_MASK: bcue_setup_err_mask



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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
17	RW	WO_AND	WO_OR	PBAFIRMASK_BCUE_PB_ACK_DEAD_MASK: bcue_pb_ack_dead_mask
18	RW	WO_AND	WO_OR	PBAFIRMASK_BCUE_PB_ADRERR_MASK: bcue_pb_adrerr_mask
19	RW	WO_AND	WO_OR	PBAFIRMASK_BCUE_OCI_DATERR_MASK: bcue_oci_daterr_mask
20	RW	WO_AND	WO_OR	PBAFIRMASK_BCDE_SETUP_ERR_MASK: bcde_setup_err_mask
21	RW	WO_AND	WO_OR	PBAFIRMASK_BCDE_PB_ACK_DEAD_MASK: bcde_pb_ack_dead_mask
22	RW	WO_AND	WO_OR	PBAFIRMASK_BCDE_PB_ADRERR_MASK: bcde_pb_adrerr_mask
23	RW	WO_AND	WO_OR	PBAFIRMASK_BCDE_RDDATATO_ERR_MASK: bcde_rddatato_err_mask
24	RW	WO_AND	WO_OR	PBAFIRMASK_BCDE_SUE_ERR_MASK: bcde_sue_err_mask
25	RW	WO_AND	WO_OR	PBAFIRMASK_BCDE_UE_ERR_MASK: bcde_ue_err_mask
26	RW	WO_AND	WO_OR	PBAFIRMASK_BCDE_CE_MASK: bcde_ce_mask
27	RW	WO_AND	WO_OR	PBAFIRMASK_BCDE_OCI_DATERR_MASK: bcde_oci_daterr_mask
28	RW	WO_AND	WO_OR	PBAFIRMASK_INTERNAL_ERR_MASK: internal_err_mask
29	RW	WO_AND	WO_OR	PBAFIRMASK_ILLEGAL_CACHE_OP_MASK: illegal_cache_op_mask
30	RW	WO_AND	WO_OR	PBAFIRMASK_OCI_BAD_REG_ADDR_MASK: oci_bad_reg_addr_mask
31	RW	WO_AND	WO_OR	PBAFIRMASK_AXPUSH_WRERR_MASK: axpush_wrerr_mask
32	RW	WO_AND	WO_OR	PBAFIRMASK_AXRCV_DLO_ERR_MASK: axrcv_dlo_err_mask
33	RW	WO_AND	WO_OR	PBAFIRMASK_AXRCV_DLO_TO_MASK: axrcv_dlo_to_mask
34	RW	WO_AND	WO_OR	PBAFIRMASK_AXRCV_RSVDATA_TO_MASK: axrcv_rsvdata_to_mask
35	RW	WO_AND	WO_OR	PBAFIRMASK_AXFLOW_ERR_MASK: axflow_err_mask
36	RW	WO_AND	WO_OR	PBAFIRMASK_AXSND_DHI_RTYTO_MASK: axsnd_dhi_rtyto_mask
37	RW	WO_AND	WO_OR	PBAFIRMASK_AXSND_DLO_RTYTO_MASK: axsnd_dlo_rtyto_mask
38	RW	WO_AND	WO_OR	PBAFIRMASK_AXSND_RSUTO_MASK: axsnd_rsvto_mask
39	RW	WO_AND	WO_OR	PBAFIRMASK_AXSND_RSVERR_MASK: axsnd_rsverr_mask
40	RW	WO_AND	WO_OR	PBAFIRMASK_PB_ACKDEAD_FW_WR_MASK: pb_ackdead_fw_wr_mask
41:43	RW	WO_AND	WO_OR	PBAFIRMASK_RESERVED_41_43: Reserved
44	RW	WO_AND	WO_OR	PBAFIRMASK_FIR_PARITY_ERR2_MASK: fir_parity_err2_mask
45	RW	WO_AND	WO_OR	PBAFIRMASK_FIR_PARITY_ERR_MASK: fir_parity_err_mask
46:63	RO	N/A	N/A	Constant = 0b00000000000000000000

Register Name	PBA FIR Action0	
Mnemonic	EN.TPC.PBA.PBAFIRACT0	
Address	0000000002010846 (SCOM)	
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:45	RW	PBAFIRACT0_FIR_ACTION0: MSB of action select for corresponding bit in FIR (Action0, Action1, Mask) = Action Select (0,0,x) = No Error reported (0,1,0) = Recoverable Error (PBA_TC_RECOV) (1,0,0) = Checkstop Error (PBA_TC_XSTOP) (1,1,0) = No Error reported (x,x,1) = MASKED
46:63	RO	Constant = 0b00000000000000000000

Register Name		<i>PBA FIR Action1</i>
Mnemonic		EN.TPC.PBA.PBAFIRACT1
Address		0000000002010847 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:45	RW	PBAFIRACT1_FIR_ACTION1: MSB of action select for corresponding bit in FIR (Action0, Action1, Mask) = Action Select (0,0,x) = No Error reported (0,1,0) = Recoverable Error (PBA_TC_RECOV) (1,0,0) = Checkstop Error (PBA_TC_XSTOP) (1,1,0) = No Error reported (x,x,1) = MASKED
46:63	RO	Constant = 0b00000000000000000000

Register Name		<i>PBA OCC Action</i>
Mnemonic		EN.TPC.PBA.PBAOCCACT
Address		000000000201084A (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:43	RW	PBAOCCACT_OCC_ACTION_SET: OCC Action Set 0 - FIR Input does not cause pba_occ_error to be pulsed. 1 - FIR input causes pba_occ_error to be pulsed.
44:63	RO	Constant = 0b00000000000000000000

Register Name		<i>PBA Configuration Register</i>
Mnemonic		EN.TPC.PBA.PBACFG
Address		000000000201084B (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:1	RW	PBACFG_PBREQ_SLVFW_MAX_PRIORITY: Max Processor Bus Drop Priority for forwarded requests. These bits control the maximum processor bus drop priority that can be used to forward OCI requests. It should be set to 'HI'. LOW=>0b00 MED=>0b01 HI=>0b10
2:3	RW	PBACFG_PBREQ_BCE_MAX_PRIORITY: Max Processor Bus Drop Priority for Block Copy Engine Requests. These bits control the maximum processor bus drop priority that can be used by the Block copy Engine. It should be set to 'HI'. LOW=>0b00 MED=>0b01 HI=>0b10
4:8	RW	PBACFG_PBREQ_DATA_HANG_DIV: Processor Bus Data Hang Timeout Divider. Initializes when clocks are started. Divides the processor bus data hang pulse to control the read data timeout.

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Bits	SCOM	Field Mnemonic: Description
9:13	RW	PBACFG_PBREQ_OPER_HANG_DIV: Processor Bus Operational Hang Timeout Divider. Initializes when clocks are started. Divides the processor bus operational hang pulse to control the Livelockhang rty_other response to the processor bus hang check command.
14:19	RW	PBACFG_PBREQ_DROP_PRIORITY_MASK: Processor Bus Drop Priority Mask. Mask to control the probability that a request that received a rty_drop cresp should increase its priority. Mask bits control probability from 1:1 (all ones) to 64:1 (all zeroes).
20:23	RW	PBACFG_RESERVED_20_23: Spare.
24	RW	PBACFG_CHSW_HANG_ON_ADRERROR: Enable PBA OCI Slave Hang on Processor Bus Address Error. 0 - Address error on processor bus request will self-recover (Default) 1 - Address error on processor bus request will need SLVRST to recover otherwise it will hang.
25	RW	PBACFG_CHSW_DIS_OCIABUSPAR_CHECK: Disable OCI Address Parity Checking and Generation OFF - PBA OCI Slave uses oci_pba_s_addrparen to control whether address parity is checked. PBA OCI Master asserts pba_oci_m_addrparen. ON - PBA OCI Slave does not check address parity. PBA OCI Master does not assert pba_oci_m_addrparen.
26	RW	PBACFG_CHSW_DIS_OCIBEPAR_CHECK: Disable OCI BE Parity Checking and Generation OFF - PBA OCI Slave uses oci_pba_s_beparen to control whether BE parity is checked. PBA OCI Master asserts pba_oci_m_beparen. ON - PBA OCI Slave does not check BE parity. PBA OCI Master does not assert pba_oci_m_beparen.
27	RW	PBACFG_CHSW_HANG_ON_DERROR: Enable PBA OCI Slave hang on Processor Bus Data Error. 0 - Processor bus data error self-recovers after sending RDDACK with an error response to the OCI master (Default) 1 - Processor bus data error causes hang after sending RDDACK with an error response. Buffer FSM cannot be reset.
28	RW	PBACFG_CHSW_HANG_ON_REREQ_TIMEOUT: Enable PBA OCI Slave hang on OCI ReRequest Timeout. 0 - Rdbuffsm goes to empty state after timeout (Default). 1 - Rdbuffsm hangs in the timeout state if the OCI master stops re-requesting the read.
29	RW	PBACFG_CHSW_DIS_WRITE_MATCH_REARB: Disable PBA OCI Slave Write Ordering Match. Disable Rearb for incoming write that matches in the same cache line as a pending write. This will allow sequential, non-gathered writes to get queued. This will allow overlapping writes to get out of order if the pending write is retried by the Memory Controller.
30	RW	PBACFG_CHSW_DIS_OCIDATAPAR_GEN: Disable OCI Data Parity Generation This bit is used to control data parity generate by the PBA OCI Master and OCI Slave. OFF - PBA OCI Slave assert pba_oci_s_rdbusparen with valid read data. PBA OCI Master assert pba_oci_m_wrbusparen with valid write data. ON - PBA OCI Slave does not assert pba_oci_s_rdbusparen with valid read data. PBA OCI Master does not assert pba_oci_m_wrbusparen with valid write data.
31	RW	PBACFG_CHSW_DIS_OCIDATAPAR_CHECK: Disable OCI Data Parity Checking OFF - PBA OCI Slave uses oci_pba_s_wrbusparen to control whether the write data parity is checked. PBA OCI Master uses pba_oci_m_rdbusparen to control whether the read data parity is checked. ON - PBA OCI Slave does not check write data parity. PBA OCI Master does not check read data parity.
32	RW	PBACFG_CHSW_DIS_OPER_HANG: Disable operational hang pulse preventing processor bus livelock warning.
33	RW	PBACFG_CHSW_DIS_DATA_HANG: Disable data hang pulse preventing processor bus timeout.
34	RW	PBACFG_CHSW_DIS_ECC_CHECK: Disable ECC checking on inbound processor bus data.
35	RW	PBACFG_CHSW_DIS_RETRY_BACKOFF: Disable retry backoff on processor bus.
36	RW	PBACFG_CHSW_HANG_ON_INVALID_CRESP: Enable hang on invalid processor bus CRESP, (otherwise it will retry).
37	RW	PBACFG_CHSW_EN_SCOPEINC_ON_BKILL_INC: Enable processor bus scope increase on bkill_inc like retry_inc.

Bits	SCOM	Field Mnemonic: Description
38	RW	PBACFG_CHSW_DIS_GROUP_SCOPE: Disable forcing group scope on writes when scope is programmed to nodal. Set only if group class MCD is disabled. Group scope will be 'skipped' on a rty_inc. If BAR is set to group scope, request uses system scope.
39	RW	PBACFG_CHSW_DIS_RTAG_PARITY_CHK: Disable processor bus parity check on dpx_rtag. Only used in designer simulation.
40	RW	PBACFG_CHSW_DIS_PB_PARITY_CHK: Disable processor bus parity check on rcmd0 addr, cresp atag and ttag. Only used in designer simulation.
41:47	RW	PBACFG_RESERVED_41_47: Spare.
48:63	RO	Constant = 0b000000000000000000.

Register Name	<i>PBA Error Report 0 Register</i>
Mnemonic	EN.TPC.PBA.PBAERRRPT0
Address	000000000201084C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	RWX_WCLRP ART	PBAERRRPT0_CERR_PB_RDDATATO_FW: CERR_OBS: PBAFIR(2) PB Read Data Timeout for Forwarded Request 0:5 - Per Read queue(0:5).
6:11	RWX_WCLRP ART	PBAERRRPT0_CERR_PB_RDADRERR_FW: CERR_OBS: PBAFIR(1) PB CRESP Addr Error Received for Forwarded Read Request 0:5 - Per Read queue (0:5)
12:15	RWX_WCLRP ART	PBAERRRPT0_CERR_PB_WRADRERR_FW: CERR_OBS: PBAFIR(12) PB CRESP Addr Error Received for Forwarded Write Request 0:1 - Per Write queue (0:1), f 2 - PBAXSND, 3 - PBAXRCV
16:21	RWX_WCLRP ART	PBAERRRPT0_CERR_PB_ACKDEAD_FW_RD: CERR_OBS: PBAFIR(14) Ackdead response received for forwarded read request 0:5 - Per Read queue(0:5),
22:23	RWX_WCLRP ART	PBAERRRPT0_CERR_PB_ACKDEAD_FW_WR: CERR_OBS: PBAFIR(40) Ackdead response received for forwarded write request 0:1 - Per Write queue.(0:1)
24:34	RWX_WCLRP ART	PBAERRRPT0_CERR_PB_UNEXPCRESP: CERR_OBS: PBAFIR(9) Unexp CRESP received for request. 0:5 - Per Read queue.(0:5), 6:7 - Per Write queue(0:1), 8:9 - Per BCUE write queue, 10 - PBAXSND,
35:40	RWX_WCLRP ART	PBAERRRPT0_CERR_PB_UNEXPDATA: CERR_OBS: PBAFIR(10) Unexpected Data response received 0:5 - Per Read queue(0:5)
41:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>PBA Error Report 1 Register</i>
Mnemonic	EN.TPC.PBA.PBAERRRPT1
Address	000000000201084D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:11	ROX	PBAERRRPT1_CERR_PB_BADCRESP: CERR_OBS: PBAFIR(13) Invalid CRESP received. 0:5 - Per Read queue(0:5) 6:9 - Per Write queue(0:3) 10 - PBAXSND 11 - PBAXRCV

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Bits	SCOM	Field Mnemonic: Description
12:23	ROX	PBAERRRPT1_CERR_PB_CRESPTO: CERR_OBS: PBAFIR(15) Valid CRESP never received. 0:5 - Per Read queue(0:5) 6:9 - Per Write queue(0:3) 10 - PBAXSND 11 - PBAXRCV
24:29	ROX	PBAERRRPT1_CERR_OCI_REREQTO: CERR_OBS: PBAFIR(8) PBA OCI Slave detected Read Re-Request Timeout. Request was aborted. 0:5 - Per Read queue(0:5)
30:31	ROX	PBAERRRPT1_CERR_BCDE_SETUP_ERR: CERR_OBS: PBAFIR(20) BCDE Setup Error 0 - Unexpected start when already running. 1 - Processor bus address error.
32:33	ROX	PBAERRRPT1_CERR_BCUE_SETUP_ERR: CERR_OBS: PBAFIR(16) BCUE Setup Error 0 - Unexpected start when already running. 1 - Processor bus address error.
34:35	ROX	PBAERRRPT1_CERR_BCUE_OCI_DATAERR: CERR_OBS: PBAFIR(19) 0 - BCUE received MRDERR. 1 - BCUE read parity error.
36:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>PBA Error Report 2 Register</i>
Mnemonic	EN.TPC.PBA.PBAERRRPT2
Address	000000000201084E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	PBAERRRPT2_CERR_SLV_INTERNAL_ERR: CERR_OBS: PBAFIR(28) PBA Internal Error (OCI Slave) 0 - Multi address match 1 - Multip rdbuf start 2 - Unexp rdbuf start 3 - Cancel rdbuf start 4 - Bad Region or Marker Address in PBAMODE register 5 - RDBUFFSM illegal State 6 - WRBUFFSM illegal State 7 - not defined.
8:11	ROX	PBAERRRPT2_CERR_BCDE_INTERNAL_ERR: CERR_OBS: PBAFIR(28) PBA Internal Error (BCDE) 0 - Unexp addrack 1 - Unexp dataack 2 - wrfsm illegal state 3 - bcefsm illegal state
12:15	ROX	PBAERRRPT2_CERR_BCUE_INTERNAL_ERR: CERR_OBS: PBAFIR(28) PBA Internal Error (BCDE) 0 - Unexp addrack 1 - Unexp dataack 2 - Not defined. 3 - bcefsm illegal state
16	ROX	PBAERRRPT2_CERR_BAR_PARITY_ERR: CERR_OBS: PBAFIR(28) PBA Internal Error - BAR Parity Error
17	ROX	PBAERRRPT2_CERR_SCOMTB_ERR: CERR_OBS: PBAFIR(28) PBA Internal Error - Trusted SCOM FSM error.
18:19	ROX	PBAERRRPT2_CERR_SPARE: CERR_OBS: PBAFIR(28) PBA Internal Error - Unused.



Bits	SCOM	Field Mnemonic: Description
20	ROX	PBAERRRPT2_CERR_PBDOUT_PARITY_ERR: CERR_OBS: PBAFIR(28) PBA Internal Error - Parity error detected on outbound write data. Forced bad ECC.
21:23	ROX	PBAERRRPT2_CERR_PB_PARITY_ERR: CERR_OBS: PBAFIR(11) processor bus parity error detected 0 - CRESP TTAG or ATAG parity error 1 - DPX_RTAG parity error 2 - RCMD0 ADDR parity error
24:28	ROX	PBAERRRPT2_CERR_AXFLOW_ERR: CERR_OBS.PBAFIR(35) PBAX Flow error 0 - axflow Setup 1:2 - axflow underflow per qid. 3:4 - axflow overflow per qid.
29:30	ROX	PBAERRRPT2_CERR_AXPUSH_WRERR: CERR_OBS.PBAFIR(31) PBAX Push Write Error 0 - push queue 0 1 - push queue 1
31:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	PBA Read Buffer Valid Status 0
Mnemonic	EN.TPC.PBA.PBARBUFVAL0
Address	0000000002010850 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:1	ROX	PBARBUFVAL0_RD_SLVNUM: Rd_slvnum. This is the pbaslvctl that defines the the master_id and buffer controls for this OCI address. It is set by the OCI Slave Control logic when the buffer is selected. SLVCTL0=>0b00 SLVCTL1=>0b01 SLVCTL2=>0b10 SLVCTL3=>0b11
2:24	ROX	PBARBUFVAL0_CUR_RD_ADDR: Current Rd Address 128-byte cache line address for the current buffer. It is set by the OCI slave control logic when the buffer is selected.
25:27	RO	Constant = 0b000
28	ROX	PBARBUFVAL0_PREFETCH: Prefetch status. This bit is set when the next cache line is prefetched and is used as extra information to decide if the buffer can be reused for another operation and forced to the timeout state when the buffer is in the valid, PB CRESP Error, or PB data error state. This bit is cleared when an OCI Request matches the address or when the Rd Buffer Status goes to the Empty State. OFF - OCI Read Address requested this buffered address ON - processor bus Read request kicked off for next cache line prefetch
29:30	RO	Constant = 0b00
31	ROX	PBARBUFVAL0_ABORT: Abort Status This bit is set when the OCI Master has aborted the request or the PBASLVRST[SLV Reset] was written while the read data is being fetched. This bit clears when the Rd Buffer Status goes to the Empty State. OFF - Request has not been aborted ON - Request has been aborted
32	RO	Constant = 0b0

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Bits	SCOM	Field Mnemonic: Description
33:39	ROX	PBARBUFVAL0_BUFFER_STATUS: Rd Buffer Status These bits indicate which bit is set in the one-hot Read in Progress state machine. Zero is not a valid state after clocks have started. EMPTY=>0b0000001 FETCHING=>0b0000010 VALID=>0b0000100 VALIDWFP=>0b0001000 DATAERR=>0b0010000 CRESPERR=>0b0100000 RREQ_TO=>0b1000000
40	RO	Constant = 0b0 EMPTY=>0b0000001 FETCHING=>0b0000010 VALID=>0b0000100 VALIDWFP=>0b0001000 DATAERR=>0b0010000 CRESPERR=>0b0100000 RREQ_TO=>0b1000000
41:43	ROX	PBARBUFVAL0_MASTERID: Master Id These bits indicate the Master Id that requested the read operation.
44:63	RO	Constant = 0b00000000000000000000

Register Name	PBA Read Buffer Valid Status 1
Mnemonic	EN.TPC.PBA.PBARBUFVAL1
Address	0000000002010851 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:1	ROX	PBARBUFVAL1_RD_SLVNUM: Rd_slvnum. This is the pbaslvctl that defines the the master_id, and buffer controls for this OCI address. It is set by the OCI slave control logic when the buffer is selected. SLVCTL0=>0b00 SLVCTL1=>0b01 SLVCTL2=>0b10 SLVCTL3=>0b11
2:24	ROX	PBARBUFVAL1_CUR_RD_ADDR: Current read address 128-byte cache line address for the current buffer. It is set by the OCI slave control logic when the buffer is selected.
25:27	RO	Constant = 0b000
28	ROX	PBARBUFVAL1_PREFETCH: Prefetch status. This bit is set when the next cache line is prefetched and is used as extra info to decide if the buffer can be reused for another operation and forced to the timeout state when the buffer is in the valid, PB CRESP Error, or PB data error state. This bit is cleared when an OCI request matches the address or when the read buffer status goes to the empty state. OFF - OCI read address requested this buffered address. ON – Processor bus read request kicked off for next cache line prefetch.
29:30	RO	Constant = 0b00
31	ROX	PBARBUFVAL1_ABORT: Abort status. This bit is set when the OCI master has aborted the request or the PBASLVRST[SLV Reset] was written while the read data is being fetched. This bit clears when the Rd Buffer Status goes to the Empty State. OFF - Request has not been aborted. ON - Request has been aborted.



Bits	SCOM	Field Mnemonic: Description
32	RO	Constant = 0b0
33:39	ROX	PBARBUFVAL1_BUFFER_STATUS: Rd Buffer Status These bits indicate which bit is set in the one-hot Read in Progress state machine. Zero is not a valid state after clocks have started. EMPTY=>0b0000001 FETCHING=>0b0000010 VALID=>0b0000100 VALIDWFP=>0b0001000 DATAERR=>0b0010000 CRESPERR=>0b0100000 REREQ_TO=>0b1000000
40	RO	Constant = 0b0 EMPTY=>0b0000001 FETCHING=>0b0000010 VALID=>0b0000100 VALIDWFP=>0b0001000 DATAERR=>0b0010000 CRESPERR=>0b0100000 REREQ_TO=>0b1000000
41:43	ROX	PBARBUFVAL1_MASTERID: Master Id These bits indicate the Master Id that requested the read operation.
44:63	RO	Constant = 0b00000000000000000000

Register Name	PBA Read Buffer Valid Status 2
Mnemonic	EN.TPC.PBA.PBARBUFVAL2
Address	0000000002010852 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:1	ROX	PBARBUFVAL2_RD_SLVNUM: Rd_slvnum This is the pbaslvctl that defines the the master_id, and buffer controls for this OCI address. It is set by the OCI slave control logic when the buffer is selected. SLVCTL0=>0b00 SLVCTL1=>0b01 SLVCTL2=>0b10 SLVCTL3=>0b11
2:24	ROX	PBARBUFVAL2_CUR_RD_ADDR: Current read address. 128-byte cache line address for the current buffer. It is set by the OCI slave control logic when the buffer is selected.
25:27	RO	Constant = 0b000
28	ROX	PBARBUFVAL2_PREFETCH: Prefetch status. This bit is set when the next cache line is prefetched and is used as extra information to decide if the buffer can be reused for another operation and forced to the timeout state when the buffer is in the valid, PB CRESP error, or PB data error state. This bit is cleared when an OCI request matches the address or when the Rd Buffer status goes to the empty state. OFF - OCI read address requested this buffered address. ON - Processor bus read request kicked off for next cache line prefetch.
29:30	RO	Constant = 0b00

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Bits	SCOM	Field Mnemonic: Description
31	ROX	PBARBUFVAL2_ABORT: Abort status. This bit is set when the OCI master has aborted the request or the PBASLVRST[SLV Reset] was written while the read data is being fetched. This bit clears when the read buffer status goes to the empty state. OFF - Request has not been aborted. ON - Request has been aborted.
32	RO	Constant = 0b0
33:39	ROX	PBARBUFVAL2_BUFFER_STATUS: Rd Buffer Status These bits indicate which bit is set in the one-hot Read in Progress state machine. Zero is not a valid state after clocks have started. EMPTY=>0b0000001 FETCHING=>0b0000010 VALID=>0b0000100 VALIDWFP=>0b0001000 DATAERR=>0b0010000 CRESPERR=>0b0100000 REREQ_TO=>0b1000000
40	RO	Constant = 0b0 EMPTY=>0b0000001 FETCHING=>0b0000010 VALID=>0b0000100 VALIDWFP=>0b0001000 DATAERR=>0b0010000 CRESPERR=>0b0100000 REREQ_TO=>0b1000000
41:43	ROX	PBARBUFVAL2_MASTERID: Master Id These bits indicate the Master Id that requested the read operation.
44:63	RO	Constant = 0b000000000000000000000000

Register Name	PBA Read Buffer Valid Status 3
Mnemonic	EN.TPC.PBA.PBARBUFVAL3
Address	0000000002010853 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:1	ROX	PBARBUFVAL3_RD_SLVNUM: Rd_slvnum This is the pbaslvctl that defines the the master_id, and buffer controls for this OCI address. It is set by the OCI Slave Control logic when the buffer is selected. SLVCTL0=>0b00 SLVCTL1=>0b01 SLVCTL2=>0b10 SLVCTL3=>0b11
2:24	ROX	PBARBUFVAL3_CUR_RD_ADDR: Current Rd Address 128-byte cache line address for the current buffer. It is set by the OCI Slave Control logic when the buffer is selected.
25:27	RO	Constant = 0b000
28	ROX	PBARBUFVAL3_PREFETCH: Prefetch Status This bit is set when the next cache line is prefetched and is used as extra info to decide if the buffer can be reused for another operation and forced to the timeout state when the buffer is in the valid, PB CRESPE error, or PB data error state. This bit is cleared when an OCI request matches the address or when the read buffer status goes to the empty state. OFF - OCI read address requested this buffered address. ON – Processor bus read request kicked off for next cache line prefetch.



Bits	SCOM	Field Mnemonic: Description
29:30	RO	Constant = 0b00.
31	ROX	PBARBUFVAL3_ABORT: Abort status. This bit is set when the OCI master has aborted the request or the PBASLVRST[SLV Reset] was written while the read data is being fetched. This bit clears when the read buffer status goes to the empty state. OFF - Request has not been aborted. ON - Request has been aborted.
32	RO	Constant = 0b0
33:39	ROX	PBARBUFVAL3_BUFFER_STATUS: Rd Buffer Status These bits indicate which bit is set in the one-hot Read in Progress state machine. Zero is not a valid state after clocks have started. EMPTY=>0b0000001 FETCHING=>0b0000010 VALID=>0b0000100 VALIDWFP=>0b0001000 DATAERR=>0b0010000 CRESPERR=>0b0100000 REREQ_TO=>0b1000000
40	RO	Constant = 0b0 EMPTY=>0b0000001 FETCHING=>0b0000010 VALID=>0b0000100 VALIDWFP=>0b0001000 DATAERR=>0b0010000 CRESPERR=>0b0100000 REREQ_TO=>0b1000000
41:43	ROX	PBARBUFVAL3_MASTERID: Master ID. These bits indicate the Master ID that requested the read operation.
44:63	RO	Constant = 0b00000000000000000000

Register Name	<i>PBA Read Buffer Valid Status 4</i>
Mnemonic	EN.TPC.PBA.PBARBUFVAL4
Address	0000000002010854 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:1	ROX	PBARBUFVAL4_RD_SLVNUM: Rd_slvnum. This is the pbaslvctl that defines the the master_id and buffer controls for this OCI address. It is set by the OCI slave control logic when the buffer is selected. SLVCTL0=>0b00 SLVCTL1=>0b01 SLVCTL2=>0b10 SLVCTL3=>0b11
2:24	ROX	PBARBUFVAL4_CUR_RD_ADDR: Current read address. 128-byte cache line address for the current buffer. It is set by the OCI slave control logic when the buffer is selected.
25:27	RO	Constant = 0b000.

Registers Specification

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Bits	SCOM	Field Mnemonic: Description
28	ROX	PBARBUFVAL4_PREFETCH: Prefetch status. This bit is set when the next cache line is prefetched and is used as extra information to decide if the buffer can be reused for another operation and forced to the timeout state when the buffer is in the valid, PB CRESP error, or PB data error state. This bit is cleared when an OCI request matches the address or when the read buffer status goes to the empty state. OFF - OCI read address requested this buffered address. ON - Processor bus read request kicked off for next cache line prefetch.
29:30	RO	Constant = 0b00
31	ROX	PBARBUFVAL4_ABORT: Abort status. This bit is set when the OCI master has aborted the request or the PBASLVRST[SLV Reset] was written while the read data is being fetched. This bit clears when the read buffer status goes to the empty state. OFF - Request has not been aborted. ON - Request has been aborted.
32	RO	Constant = 0b0
33:39	ROX	PBARBUFVAL4_BUFFER_STATUS: Rd Buffer Status These bits indicate which bit is set in the one-hot Read in Progress state machine. Zero is not a valid state after clocks have started. EMPTY=>0b00000001 FETCHING=>0b00000010 VALID=>0b00000100 VALIDWFP=>0b00001000 DATAERR=>0b00010000 CRESPERR=>0b00100000 REREQ_TO=>0b01000000
40	RO	Constant = 0b0 EMPTY=>0b00000001 FETCHING=>0b00000010 VALID=>0b00000100 VALIDWFP=>0b00001000 DATAERR=>0b00010000 CRESPERR=>0b00100000 REREQ_TO=>0b01000000
41:43	ROX	PBARBUFVAL4_MASTERID: Master Id These bits indicate the Master Id that requested the read operation.
44:63	RO	Constant = 0b00000000000000000000

Register Name	PBA Read Buffer Valid Status 5
Mnemonic	EN.TPC.PBA.PBARBUFVAL5
Address	0000000002010855 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:1	ROX	PBARBUFVAL5_RD_SLVNUM: Rd_slvnum. This is the pbaslvctl that defines the the master_id, and buffer controls for this OCI address. It is set by the OCI slave control logic when the buffer is selected. SLVCTL0=>0b00 SLVCTL1=>0b01 SLVCTL2=>0b10 SLVCTL3=>0b11
2:24	ROX	PBARBUFVAL5_CUR_RD_ADDR: Current read address. 128-byte cache line address for the current buffer. It is set by the OCI slave control logic when the buffer is selected.



Bits	SCOM	Field Mnemonic: Description
25:27	RO	Constant = 0b000
28	ROX	PBARBUFVAL5_PREFETCH: Prefetch status. This bit is set when the next cache line is prefetched and is used as extra information to decide if the buffer can be reused for another operation and forced to the timeout state when the buffer is in the valid, PB CRESP error, or PB data error state. This bit is cleared when an OCI Request matches the address or when the read buffer status goes to the empty state. OFF - OCI read address requested this buffered address. ON - Processor bus read request kicked off for next cache line prefetch.
29:30	RO	Constant = 0b00.
31	ROX	PBARBUFVAL5_ABORT: Abort status. This bit is set when the OCI master has aborted the request or the PBASLVRST[SLV Reset] was written while the read data is being fetched. This bit clears when the read buffer status goes to the empty state. OFF - Request has not been aborted. ON - Request has been aborted.
32	RO	Constant = 0b0.
33:39	ROX	PBARBUFVAL5_BUFFER_STATUS: Read buffer status. These bits indicate which bit is set in the one-hot read-in-progress state machine. Zero is not a valid state after clocks have started. EMPTY=>0b0000001 FETCHING=>0b0000010 VALID=>0b0000100 VALIDWFP=>0b0001000 DATAERR=>0b0010000 CRESPERR=>0b0100000 REREQ_TO=>0b1000000
40	RO	Constant = 0b0 EMPTY=>0b0000001 FETCHING=>0b0000010 VALID=>0b0000100 VALIDWFP=>0b0001000 DATAERR=>0b0010000 CRESPERR=>0b0100000 REREQ_TO=>0b1000000
41:43	ROX	PBARBUFVAL5_MASTERID: Master Id. These bits indicate the Master Id that requested the read operation.
44:63	RO	Constant = 0b00000000000000000000

Register Name	<i>PBA Write Buffer Valid Status 0</i>
Mnemonic	EN.TPC.PBA.PBAWBUFVAL0
Address	0000000002010858 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:1	ROX	PBAWBUFVAL0_WR_SLVNUM: Wr_slvnum This is the pbaslvctl that defines the the master_id, and buffer controls for this OCI address. It is set by the OCI Slave Control logic when the buffer is selected. SLVCTL0=>0b00 SLVCTL1=>0b01 SLVCTL2=>0b10 SLVCTL3=>0b11

Registers Specification

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Bits	SCOM	Field Mnemonic: Description
2:31	ROX	PBAWBUFVAL0_START_WR_ADDR: Starting write address. These bits save the starting OCI address for the gathered write operation and are valid only if the write buffer status is not EMPTY.
32:34	RO	Constant = 0b000
35:39	ROX	PBAWBUFVAL0_WR_BUFFER_STATUS: Write buffer status. These bits indicate which bit is set in the one-hot write-in-progress state machine. Zero is not a valid state after clocks have started. EMPTY=>0b00001 GATHERING=>0b00010 WAIT=>0b00100 WRITING=>0b01000 CRESPERR=>0b10000
40	RO	Constant = 0b0. EMPTY=>0b00001 GATHERING=>0b00010 WAIT=>0b00100 WRITING=>0b01000 CRESPERR=>0b10000
41:47	ROX	PBAWBUFVAL0_WR_BYTE_COUNT: Write byte count. These bits are the number of bytes in the gathered write operation. Starting write address plus write byte count is the next write address from the same master required to continue gathering. 0000000 - 128 bytes 0000001 - 1 byte 0000010 - 2 bytes 0000011 - 3 bytes ... 1111111 - 127 bytes
48:63	RO	Constant = 0b000000000000000000.

Register Name	PBA Write Buffer Valid Status 1
Mnemonic	EN.TPC.PBA.PBAWBUFVAL1
Address	0000000002010859 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:1	ROX	PBAWBUFVAL1_WR_SLVNUM: Wr_slvnum This is the pbaslvctl that defines the the master_id, and buffer controls for this OCI address. It is set by the OCI Slave Control logic when the buffer is selected. SLVCTL0=>0b00 SLVCTL1=>0b01 SLVCTL2=>0b10 SLVCTL3=>0b11
2:31	ROX	PBAWBUFVAL1_START_WR_ADDR: Starting Write Address These bits save the starting OCI address for the gathered write operation and are valid only If the write buffer status is not EMPTY.
32:34	RO	Constant = 0b000

Bits	SCOM	Field Mnemonic: Description
35:39	ROX	PBAWBUFVAL1_WR_BUFFER_STATUS: Write Buffer Status These bits indicate which bit is set in the one-hot Write in Progress state machine. Zero is not a valid state after clocks have started. EMPTY=>0b00001 GATHERING=>0b00010 WAIT=>0b00100 WRITING=>0b01000 CRESPERR=>0b10000
40	RO	Constant = 0b0 EMPTY=>0b00001 GATHERING=>0b00010 WAIT=>0b00100 WRITING=>0b01000 CRESPERR=>0b10000
41:47	ROX	PBAWBUFVAL1_WR_BYTE_COUNT: Write Byte Count These bits are the number of bytes in the gathered write operation. Starting Write Address plus Write Byte Count is the Next Write Address from the same master required to continue gathering. 0000000 - 128 bytes 0000001 - 1 byte 0000010 - 2 bytes 0000011 - 3 bytes . . . 1111111 - 127 bytes
48:63	RO	Constant = 0b0000000000000000

Register Name	<i>PBA Mode And Control Register</i>
Mnemonic	EN.TPC.PBA.PBAMODE
Address	0000000000064000 (PIB) 0000000040020000 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:3	RW	RW	PBAMODE_RESERVED_0_3: These bits are spare
4	RW	RW	PBAMODE_DIS_REARB: Disable OCI Rearbitration This debug bit controls whether the PBA OCI slave supports 'delayed read' mode'. If this bit is set, the PBA will still assert pba_oci_s_rearbitrate for a write request if a write buffer is unavailable. OFF - Assert pba_oci_s_rearbitrate when requested read data is not valid in Buffer. This will free the bus for other operations while the data is fetched from system memory and is the expected default mode. ON - Assert pba_oci_s_wait when requested read data is not valid in the buffer. The arbiter will continue to assert oci_pba_s_pavalid and no other operations can proceed until the PBA responds. The PBA will assert pba_oci_s_addrAck for one cycle and deassert pba_oci_s_wait when the data has been fetched into the buffer. NOTE, IF THIS MODE IS ENABLED, PBASLVCTLn[Read Prefetch Control] must be set to 'No Prefetch'. Additionally, Secondary read operations (SAVALID) are ignored so Pipeline support MUST BE DISABLED in the OCI Arbiter.
5	RW	RW	PBAMODE_DIS_MSTID_MATCH_PREF_INV: Disable Master ID Match for Prefetch Invalidate. Controls if a buffer can be invalidated when it contains valid data prefetched by another master. This bit MUST be set if prefetching is enabled for buffers shared with multiple masters. OFF - (default) Only the original master can cause its prefetch to be invalidated when a buffer is needed. ON - Any master can cause a prefetched buffer to be invalidated when a buffer is needed.

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Bits	PIB	OCI	Field Mnemonic: Description
6	RW	RW	PBAMODE_DIS_SLAVE_RDPIPE: Disable PBA slave read pipeline support. This debug bit controls whether pipelined read requests are supported by the PBA OCI slave for operations that target the processor bus. OFF - Monitor oci_pba_s_savlid for secondary read requests (2-level Pipelined support). ON - Do not respond (no AddrAck or ReArbitrate) for oci_pba_s_savlid for read requests. Requests will be qualified with oci_pba_s_pavalid only. (No pipeline support.)
7	RW	RW	PBAMODE_DIS_SLAVE_WRPIPE: Disable PBA slave write pipeline support. This debug bit controls whether pipeline write requests are supported by the PBA OCI slave for operations that target the processor bus. OFF - Monitor oci_pba_s_savlid for secondary write requests (2-level Pipeline support). ON - Do not respond (no AddrAck or ReArbitrate) for oci_pba_s_savlid for write requests. Requests are qualified with oci_pba_s_pavalid only. (no pipeline support).
8	RW	RW	PBAMODE_EN_MARKER_ACK: Enable PBA slave acknowledge of OCC HTM marker operations. This bit controls whether the PBA OCI slave will AACK and then WRDACK the OCI transactions that target the OCC HTM marker space. The PBAMODE [OCI Marker Space] bits must be initialized before setting this bit. Read operations to the marker space are not recommended. OFF - Ignore OCC HTM Marker writes.
9	RW	RW	PBAMODE_DIS_SLVMATCH_ORDER: Disable PBA SLVCTL match for ordering. This bit controls if read/write ordering is maintained for OCI address matches sent from different masters that use different SLVCTL s and may get remapped to different processor bus addresses. OFF - OCI read/write ordering for OCI transactions only if using the same SLVCTL. ON - OCI read/write ordering for OCI transactions using any SLVCTL.
10	RW	RW	PBAMODE_EN_SECOND_WRBUF: Enable second write buffer. This bit controls whether the allocated write buffers for the PBA OCI slave are treated as a pair or if just one is used. ON - Write buffers are used as a ping-pong pair. One buffer can be writing the forwarded data to the processor bus, while the other is receiving more data from the OCI OFF - Only one write buffer is used. (Default mode and expected mode to use during IPL.)
11	RW	RW	PBAMODE_DIS_REREQUEST_TO: Disable re-request timeout. This debug bit disables the time that controls how long a read machine will wait for a re-presentation of the read request after the read from the processor bus has completed. This must not be set if the 405 is doing reads from the PBA for its ICACHE because it will abort requests. OFF - The length of the re-request timeout is controlled in PBACFG[ocisl_v_rereq_hang_div]. (expected default) ON - Re-request timeout is disabled.
12:13	RW	RW	PBAMODE_INJECT_TYPE: Configure error injection type. These bits can be written at any time to setup the error injection type on the processor bus inbound read data. CE=>0b00 UE=>0b01 SUE=>0b10

Bits	PIB	OCI	Field Mnemonic: Description
14:15	RWX	RWX	PBAMODE_INJECT_MODE: Configure error injection mode. These bits can be written at any time to setup the error injection mode for the processor bus inbound read data. When doing single-error inject, the CEUESUE error bits in the FIR must be cleared before another error can be injected. Additionally, the bits are cleared when the CEUESUE bits in FIR are set NONE=>0b00 SOLID=>0b01 SINGLE=>0b10 NOT_VALID=>0b11
16:17	RO	RO	PBAMODE_PBA_REGION: PBA Region These bits define the PBA region decoded by the PBA OCI Slave in the upper two bits of the OCI address and are scan only. They are also visible through this register. They are initialized to '00'.
18:20	RW	RW	PBAMODE_OCI_MARKER_SPACE: OCI Marker Space. These bits define the register region used for OCC markers and correspond to address(13:15) when address(0:1) = '01'. The PBA OCI slave always acknowledges writes to this register space and acknowledges and drops the data on the floor if PBAMODE[Enable PBA Acknowledge of OCC HTM Marker Operations] = 1. This must not conflict with the defined register space of other OCI slaves including PBA's own register space. Only '110' or '111' avoids conflict.
21:22	RW	RW	PBAMODE_BCDE_OCITRANS: BCDE OCI transaction control. These bits define how efficiently the data is written to the SRAM by the Block Copy Download Engine. These bits should be changed only when the BCDE is not running. 00 - Data is written to the SRAM in 32-byte transactions. (4 beats) 01 - Data is written to the SRAM in 64-byte transactions (8 beats) 10 - Data is written to the SRAM in 8-Byte transactions (1 beat) 11 - Not defined
23:24	RW	RW	PBAMODE_BCUE_OCITRANS: BCUE OCI transaction control. These bits define how efficiently the data is read from the SRAM by the Block Copy Upload Engine. These bits should be changed only when the BCUE is not running. 00 - Data is read from the SRAM in 32-byte transactions. (4 beats) 01 - Data is read from the SRAM in 64-byte transactions (8 beats) 10 - Data is read from the SRAM in 8-byte transactions (1 beat) 11 - Not defined
25	RW	RW	PBAMODE_DIS_MASTER_RD_PIPE: Disable PBA master read pipeline support. This bit controls whether pipeline read requests are supported by the PBA Block Copy Upload Engine. OFF - Assert pba_oci_m_request for a pending read request immediately after oci_pba_m_addrAck is received to allow for read pipelining on the OCI. (Expected default) ON - Do not assert pba_oci_m_request for a pending read request until all expected oci_pba_m_rddack have been received for the previous request.
26	RW	RW	PBAMODE_DIS_MASTER_WR_PIPE: Disable PBA master write pipeline support. This bit controls whether pipeline write requests are supported by the PBA Block Copy Download Engine and should be changed only when the BCDE is stopped. OFF - Assert pba_oci_m_request for a pending write request immediately after oci_pba_m_addrAck is received to allow for write pipelining on the OCI. ON - Do not assert pba_oci_m_request for a pending write request until all expected oci_pba_m_wrdack have been received for the previous request.
27	RW	RW	PBAMODE_EN_SLV_FAIRNESS: Enable PBA slave fairness support. This bit controls whether the fairness protocol is engaged for the PBA slave. It should be set if multiple OCI masters are often sharing the same read and write buffers in the PBA. Mask bits can be configured in the PBACFG [ocisl_v_fairness_mask] to increase the probability that the PBA will engage the fairness. OFF - Do not engage Fairness protocol. ON - Engage the PBA slave fairness protocol based on the probability of the Fairness Mask.

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Bits	PIB	OCI	Field Mnemonic: Description
28	RW	RW	PBAMODE_EN_EVENT_COUNT: Enable event count. This bit enables the first four PBAPBOCRn counters to be re-purposed as event counters. The PBAMODE[dis_chgrate_count] must also be set.
29	RW	RW	PBAMODE_PB_NOCI_EVENT_SEL: Processor busOCI event select. This bit is valid when the PBAMODE[en_event_count] is set and controls whether PBA Slave OCI Events or PBA Processor bus events are counted. OFF - OCI events ON – Processor bus events
30:31	RW	RW	PBAMODE_SLV_EVENT_MUX: OCI event select. These bits control which PBA Slave Buffer OCI events are muxed to the event counters. '00' - Buffer A (Busy Rearb, Accept Rearb, Clr Prefetch, Drop Prefetch) '01' - Buffer B '10' - Buffer C '11' - not defined
32	RW	RW	PBAMODE_ENABLE_DEBUG_BUS: Enable PBA debug outputs. This bit enables the clock gating and allows the PBA to drive the debug outputs to the trace array.
33	RW	RW	PBAMODE_DEBUG_PB_NOT_OCI: Debug processor bus or OCI logic. This bit controls the muxing of the OCI logic or processor bus logic to the debug outputs. OFF - OCI logic debug ON – Processor bus logic debug
34:38	RW	RW	PBAMODE_DEBUG_OCI_MODE: Debug Mux selects for OCI logic. These bit control the muxing of trace information for the OCI logic debug. See the tpmiscpba.template for detailed info.
39	RW	RW	PBAMODE_RESERVED_39: Spare.
40:44	RW	RW	PBAMODE_OCISLV_FAIRNESS_MASK: PBA Slave fairness mask. Mask to control the probability that the PBA slave randomly ReArbs a write or takes no action on a read that it could otherwise handle. All 1s provides a 2:1 probability, All 0s provides 64:1 probability.
45:49	RW	RW	PBAMODE_OCISLV_REREQ_HANG_DIV: OCI ReRequest Hang Timeout Divider. Initializes when clocks are started. Divides a pulse that asserts every 64 cycles. Used to control the Re-request timeout for read requests that have been aborted without PBA seeing the abort.
50	RW	RW	PBAMODE_DIS_CHGRATE_COUNT: Disable CHGRATE Counters OFF - (default) CHGRATE Counters are Enabled. PBAMODE[en_event_count] must also be zero. ON - Freeze the CHGRATE Counters. If PBAMODE[en_event_count] = 1, the counters are repurposed as event counters.
51:52	RW	RW	PBAMODE_PBREQ_EVENT_MUX: PB event select. These bits control which processor bus events are muxed to the event counters. Only Counters 0 and 1 are used. 00 - Count rty_inc CRESP and rty_drp CRESP 01 - Count cycles waiting for CMD Grant and Data Write Grant 10 - Count PBAX RCV Asserting rty_other for reservationnot reservation 11 - Not defined
53:63	RW	RW	PBAMODE_RESERVED_53_63: Spare



Register Name	PBA Slave Reset Register
Mnemonic	EN.TPC.PBA.PBASLVRST
Address	0000000000064001 (PIB) 0000000040020008 (OCI)
Attributes	
Description	

[illegible]

Register Name	PBA Slave Control 0 Register
Mnemonic	EN.TPC.PBA.PBASLVCTL0
Address	0000000000064004 (PIB) 0000000040020020 (OCI)
Attributes	Magic=true
Description	

Registers Specification

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Bits	PIB	OCI	Field Mnemonic: Description
0	RW	RW	PBASLVCTL0_ENABLE: OCI_Base_Address_Range_Enabled. This bit must be set by software for the PBA to respond to an OCI request that targets the processor bus and matches the OCI MasterID Match Value. OFF - Ignore OCI operations ON - Accept OCI operations
1:3	RW	RW	PBASLVCTL0_MID_MATCH_VALUE: OCI Masterid Match Value. These bits must be initialized by software to indicate the OCI master ID that will use this set of Base Address Registers when the OCI request targets the processor bus region. Only ONE PBASLVCTLn may match any Master ID.
4	RW	RW	PBASLVCTL0_RESERVED_4: Spare
5:7	RW	RW	PBASLVCTL0_MID_CARE_MASK: OCI Masterid Care Mask. These bits must be initialized by software to indicate which OCI Masterid bits must match the OCI Master ID Match Value. If only one OCI Master is using this PBASLVCTL, these bits must be set to '111'.
8:10	RW	RW	PBASLVCTL0_WRITE_TTYPE: Write Ttype. Forwarded write requests that target this PBASLVCTL register use the specified write ttype on the processor bus. DMA uses a DMA_PR_W to write 1 - 127 bytes or a CL_DMA_W_I to write the gathered 128 bytes. LCO_M is a Lateral Castout M that is used only at IPL time. Cache_Inj is a cache line DMA cache inject ttype that is used only at IPL time to write an L3 line that has already been initialized. CI_PR_WR is a cache inhibited partial write ttype implemented to write to the POWER8 Memory Buffer register space. It forwards the write exactly as it was asked for in the OCI operation. Atomic is an Atomic RMW operation that should only be done as an 8-byte write. DMA=>0b000 LCO_M=>0b001 ATOMIC=>0b010 CACHE_INJ=>0b011 CI_PR_W=>0b100

Bits	PIB	OCI	Field Mnemonic: Description
11:14	RW	RW	PBASLVCTL0_RESERVED_11_14: Spare
15	RW	RW	PBASLVCTL0_READ_TTYPE: Read Ttype. Forwarded read requests that target this PBASLVCTL register use the specified ttype on the processor bus. CL_RD_NC is a cache line DMA read with no intent to cache. It always reads 128 bytes from system memory. CI_PR_RD is a cache-inhibited partial read. It forwards the read exactly as it was asked for in the OCI operation. This mode is required when accessing the POWER8 Memory Buffer register space. CL_RD_NC=>0b0 CI_PR_RD=>0b1
16:17	RW	RW	PBASLVCTL0_READ_PREFETCH_CTL: Read Prefetch Control. Auto Early Prefetch Ahead - Prefetch current and next 128-byte cache line on first read. Buffers are used in pairs. This mode should not be used if two or more masters need to share a buffer pair. No Prefetch Ahead - fetch only current requested 128-byte cache line. This mode may be used if two or more masters are allocated to the same buffer pair. Auto Late Prefetch Ahead - Prefetch next cache line after last read data returned for current cache line. This mode may also be used if two masters need to share a buffer pair but the PBAMODE [dis_mstid_match_pref_inv] mode bit must be set to avoid a hang condition. AUTO_EARLY=>0b00 NONE=>0b01 AUTO_LATE=>0b10
18	RW	RW	PBASLVCTL0_BUF_INVALIDATE_CTL: Read Buffer Invalidate Control 0 - Do not invalidate read buffer data automatically
19	RW	RW	PBASLVCTL0_BUF_ALLOC_W: Write Buffer Pair Allocation. The Master ID that uses this PBASLVCTL can use only the allocated buffers. Buffer allocation is for a buffer pair. Multiple buffer pairs can be assigned. This bit must be set for the PBA to respond to write operations through this PBASLVCTL Register.
20	RW	RW	PBASLVCTL0_BUF_ALLOC_A: Read Buffer Pair A Allocation. The Master ID that uses this PBASLVCTL can use only the allocated buffers. Buffer allocation is for a buffer pair. Multiple buffer pairs can be assigned. At least one read buffer must be allocated for the PBA to respond to read operations through this PBASLVCTL Register.
21	RW	RW	PBASLVCTL0_BUF_ALLOC_B: Read Buffer Pair B Allocation. The Master ID that uses this PBASLVCTL can use only the allocated buffers. Buffer allocation is for a buffer pair. Multiple buffer pairs can be assigned.
22	RW	RW	PBASLVCTL0_BUF_ALLOC_C: Read Buffer Pair C Allocation. The Master ID that uses this PBASLVCTL can use only the allocated buffers. Buffer allocation is for a buffer pair. Multiple buffer pairs can be assigned.
23	RW	RW	PBASLVCTL0_RESERVED_23: Spare buffer allocation bit.
24	RW	RW	PBASLVCTL0_DIS_WRITE_GATHER: Disable Write Gather. This bit disables gathering of write data in the buffer. This mode bit used only when PBASLVCTL[Write ttype] = DMA_PR_W. Otherwise it is ignored. OFF - Gather writes into the write buffer. ON - Do not gather. Writes forwarded to processor bus as written from OCI.

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Bits	PIB	OCI	Field Mnemonic: Description
25:27	RW	RW	PBASLVCTL0_WR_GATHER_TIMEOUT: Write Gather Timeout Control. These bits control how long the PBA should wait to gather write operations. This mode bit is used only when PBASLVCTL[Write ttype] = DMA_PR_W. Otherwise it is ignored. The PBA counts write gather timeout pulses that arrive every 64 OCI cycles. Write gather timeouts must not be disabled if multiple masters are enabled to write through the PBA. 000 - Disable Write Gather Timeout. Write will be flushed under the following conditions: Need another write by the same master to a nonsequential address, Gathered data to cache line boundary. Read by a master that uses this same SLVCTL register to the same address, or a PBASLVRST[SLV Reset(n)] for this PBASLVCTL. 100 - 2 Pulses (64 to 128 OCI cycles) 101 - 4 Pulses (192 to 256 OCI cycles) 110 - 8 Pulses (448 to 512 OCI cycles) 111 - 16 Pulses (960 to 1024 OCI cycles)
28:34	RW	RW	PBASLVCTL0_WRITE_TSIZE: When PBASLVCTL[Write Ttype] = Atomic RNW no fetch, these bits provide a secondary encoding for the atomic operation defined as 'FFF0011'. The 'FFF' specify the function to be applied to the operand. Only 8-byte operations are supported. Supported 'FFF' values: 000 - armw_add 001 - armw_and 010 - armw_or 011 - armw_xor
35:48	RW	RW	PBASLVCTL0_EXTADDR: PB Extaddr. This bits are the processor bus address bits (23:36) that can be used when forwarding the operation if the selected PBABARMSK bits are one.
49:50	RW	RW	PBASLVCTL0_RESERVED_49_50: Spare
51:63	RO	RO	Constant = 0b00000000000000.

Register Name		PBA Slave Control 1 Register	
Mnemonic		EN.TPC.PBA.PBASLVCTL1	
Address		0000000000064005 (PIB) 0000000040020028 (OCI)	
Attributes		Magic=true	
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0	RW	RW	PBASLVCTL1_ENABLE: OCI_Base_Address_Range_Enabled. This bit must be set by software for the PBA to respond to an OCI request that targets the processor bus and matches the OCI MasterID match value. OFF - Ignore OCI operations ON - Accept OCI operations
1:3	RW	RW	PBASLVCTL1_MID_MATCH_VALUE: OCI Masterid Match Value. These bits must be initialized by software to indicate the OCI master ID that will use this set of Base Address Registers when the OCI request targets the processor bus region. Only one PBASLVCTLn may match any Master ID.
4	RW	RW	PBASLVCTL1_RESERVED_4: Spare
5:7	RW	RW	PBASLVCTL1_MID_CARE_MASK: OCI Masterid Care Mask. These bits must be initialized by software to indicate which OCI Masterid bits must match the OCI Master ID match value. If only one OCI master is using this PBASLVCTL, these bits must be set to '111'.

Bits	PIB	OCI	Field Mnemonic: Description
8:10	RW	RW	PBASLVCTL1_WRITE_TTYPE: Write Ttype. Forwarded write requests that target this PBASLVCTL Register use the specified write ttype on the processor bus. DMA uses a DMA_PR_W to write 1 - 127 bytes or a CL_DMA_W_I to write the gathered 128 bytes. LCO_M is a Lateral Castout M that is used only at IPL time. Cache_Inj is a cache line DMA cache inject ttype that is used only at IPL time to write an L3 line that has already been initialized. CI_PR_WR is a cache inhibited partial write ttype implemented to write to the POWER8 Memory Buffer register space. It forwards the write exactly as it was asked for in the OCI operation. Atomic is an Atomic RMW operation that should only be done as an 8-byte write. DMA=>0b000 LCO_M=>0b001 ATOMIC=>0b010 CACHE_INJ=>0b011 CI_PR_W=>0b100
11:14	RW	RW	PBASLVCTL1_RESERVED_11_14: Spare
15	RW	RW	PBASLVCTL1_READ_TTYPE: Read Ttype. Forwarded read request that targets this PBASLVCTL Register uses the specified ttype on the processor bus. CL_RD_NC is a cache line DMA read with no intent to cache. It always reads 128 bytes from system memory. CI_PR_RD is a cache-inhibited partial read. It forwards the read exactly as it was asked for in the OCI operation. This mode is required when accessing the POWER8 Memory Buffer register space. CL_RD_NC=>0b0 CI_PR_RD=>0b1
16:17	RW	RW	PBASLVCTL1_READ_PREFETCH_CTL: Read Prefetch Control. Auto Early Prefetch Ahead - Prefetch current and next 128-byte cache line on first read. Buffers are used in pairs. This mode should not be used if two or more masters need to share a buffer pair. No Prefetch Ahead - Fetch only current requested 128-byte cache line. This mode can be used if two or more masters are allocated to the same buffer pair. Auto Late Prefetch Ahead - Prefetch next cache line after last read data returned for current cache line. This mode can also be used if two masters need to share a buffer pair but the PBAMODE [dis_mstid_match_pref_inv] mode bit must be set to avoid a hang condition. AUTO_EARLY=>0b00 NONE=>0b01 AUTO_LATE=>0b10
18	RW	RW	PBASLVCTL1_BUF_INVALIDATE_CTL: Read Buffer Invalidate Control 0 - Do not invalidate read buffer data automatically.
19	RW	RW	PBASLVCTL1_BUF_ALLOC_W: Write Buffer Pair Allocation The Master ID that uses this PBASLVCTL may use only the allocated buffers. Buffer allocation is for a buffer pair. Multiple buffer pairs may be assigned. This bit must be set for the PBA to respond to Write operations through this PBASLVCTL register.
20	RW	RW	PBASLVCTL1_BUF_ALLOC_A: Read Buffer Pair A Allocation The Master ID that uses this PBASLVCTL may use only the allocated buffers. Buffer allocation is for a buffer pair. Multiple buffer pairs may be assigned. At least one read buffer must be allocated for the PBA to respond to Read operations through this PBASLVCTL register.
21	RW	RW	PBASLVCTL1_BUF_ALLOC_B: Read Buffer Pair B Allocation The Master ID that uses this PBASLVCTL may use only the allocated buffers. Buffer allocation is for a buffer pair. Multiple buffer pairs may be assigned.
22	RW	RW	PBASLVCTL1_BUF_ALLOC_C: Read Buffer Pair C Allocation The Master ID that uses this PBASLVCTL may use only the allocated buffers. Buffer allocation is for a buffer pair. Multiple buffer pairs may be assigned.

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Bits	PIB	OCI	Field Mnemonic: Description
23	RW	RW	PBASLVCTL1_RESERVED_23: Spare buffer allocation bit.
24	RW	RW	PBASLVCTL1_DIS_WRITE_GATHER: Disable Write Gather This bit disables gathering of write data in the buffer. This mode bit used only when PBASLVCTL[Write ttype] = DMA_PR_W. Otherwise it is ignored. OFF - Gather writes into the write buffer. ON - Do not gather. Writes forwarded to the processor bus as written from OCI.
25:27	RW	RW	PBASLVCTL1_WR_GATHER_TIMEOUT: Write Gather Timeout Control These bits control how long the PBA should wait to gather write operations. This mode bit used only when PBASLVCTL[Write ttype] = DMA_PR_W. Otherwise it is ignored. The PBA counts Write Gather Timeout Pulses that arrive every 64 OCI cycles. Write gather timeouts must NOT be disabled if multiple masters are enabled to write through the PBA. 000 - Disable Write Gather Timeout. Write will be flushed under the following conditions: Need another write by the same master to a non-sequential address, Gathered data to cache line boundary, Read by a master that uses this same SLVCTL register to the same address, or a PBASLVRST[SLV Reset(n)] for this PBASLVCTL. 100 - 2 Pulses (64 to 128 OCI cycles) 101 - 4 Pulses (192 to 256 OCI cycles) 110 - 8 Pulses (448 to 512 OCI cycles) 111 - 16 Pulses (960 to 1024 OCI cycles)
28:34	RW	RW	PBASLVCTL1_WRITE_TSIZE: When PBASLVCTL[Write Ttype] = Atomic RNW no fetch, these bits provide a secondary encoding for the atomic operation defined as 'fff0011'. The 'fff' specify the function to be applied to the operand. Only 8-byte operations are supported. Supported 'fff' values: 000 - armw_add 001 - armw_and 010 - armw_or 011 - armw_xor
35:48	RW	RW	PBASLVCTL1_EXTADDR: PB Extaddr. These bits are the processor bus address bits (23:36) that can be used when forwarding the operation if the selected PBABARMSK bits are one.
49:50	RW	RW	PBASLVCTL1_RESERVED_49_50: Spare
51:63	RO	RO	Constant = 0b00000000000000

Register Name	PBA Slave Control 2 Register
Mnemonic	EN.TPC.PBA.PBASLVCTL2
Address	0000000000064006 (PIB) 0000000040020030 (OCI)
Attributes	Magic=true
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0	RW	RW	PBASLVCTL2_ENABLE: OCI_Base_Address_Range_Enabled. This bit must be set by software for the PBA to respond to an OCI request that targets the processor bus and matches the OCI MasterID Match Value. OFF - Ignore OCI operations ON - Accept OCI operations
1:3	RW	RW	PBASLVCTL2_MID_MATCH_VALUE: OCI Masterid Match Value. These bits must be initialized by software to indicate the OCI master ID that uses this set of Base Address Registers when the OCI request targets the processor bus region. Only one PBASLVCTLn may match any Master ID.
4	RW	RW	PBASLVCTL2_RESERVED_4: Spare
5:7	RW	RW	PBASLVCTL2_MID_CARE_MASK: OCI Masterid Care Mask. These bits must be initialized by software to indicate which OCI Masterid bits must match the OCI Master ID Match Value. If only one OCI Master is using this PBASLVCTL, these bits must be set to '111'.

Bits	PIB	OCI	Field Mnemonic: Description
8:10	RW	RW	PBASLVCTL2_WRITE_TTYPE: Write Ttype. Forwarded write requests that target this PBASLVCTL register use the specified write ttype on the processor bus. DMA uses a DMA_PR_W to write 1 - 127 bytes or a CL_DMA_W_I to write the gathered 128 bytes. LCO_M is a Lateral Castout M that is used only at IPL time. Cache_Inj is a cache-line DMA cache inject ttype that is used only at IPL time to write an L3 line that has already been initialized. CI_PR_WR is a cache-inhibited partial write ttype implemented to write to the POWER8 Memory Buffer register space. It forwards the write exactly as it was asked for in the OCI operation. Atomic is an Atomic RMW operation that should only be done as an 8-byte write. DMA=>0b000 LCO_M=>0b001 ATOMIC=>0b010 CACHE_INJ=>0b011 CI_PR_W=>0b100
11:14	RW	RW	PBASLVCTL2_RESERVED_11_14: Spare
15	RW	RW	PBASLVCTL2_READ_TTYPE: Read Ttype. Forwarded read request that targets this PBASLVCTL Register uses the specified ttype on the processor bus. CL_RD_NC is a cache-line DMA read with no intent to cache. It always reads 128 bytes from system memory. CI_PR_RD is a cache-inhibited partial read. It forwards the read exactly as it was asked for in the OCI operation. This mode is required when accessing the POWER8 Memory Buffer register space. CL_RD_NC=>0b0 CI_PR_RD=>0b1
16:17	RW	RW	PBASLVCTL2_READ_PREFETCH_CTL: Read Prefetch Control. Auto Early Prefetch Ahead - Prefetch current and next 128-byte cache line on first read. Buffers are used in pairs. This mode should not be used if two or more masters need to share a buffer pair. No Prefetch Ahead - Fetch only current requested 128-byte cache line. This mode may be used if two or more masters are allocated to the same buffer pair. Auto Late Prefetch Ahead - Prefetch next cache line after last read data returned for current cache line. This mode can also be used if two masters need to share a buffer pair but the PBAMODE [dis_mstid_match_pref_inv] mode bit must be set to avoid a hang condition. AUTO_EARLY=>0b00 NONE=>0b01 AUTO_LATE=>0b10
18	RW	RW	PBASLVCTL2_BUF_INVALIDATE_CTL: Read Buffer Invalidate Control. 0 : Do not invalidate read buffer data automatically.
19	RW	RW	PBASLVCTL2_BUF_ALLOC_W: Write Buffer Pair Allocation. The Master ID that uses this PBASLVCTL may use only the allocated buffers. Buffer allocation is for a buffer pair. Multiple buffer pairs may be assigned. This bit must be set for the PBA to respond to Write operations through this PBASLVCTL register.
20	RW	RW	PBASLVCTL2_BUF_ALLOC_A: Read Buffer Pair A Allocation The Master ID that uses this PBASLVCTL may use only the allocated buffers. Buffer allocation is for a buffer pair. Multiple buffer pairs may be assigned. At least one read buffer must be allocated for the PBA to respond to Read operations through this PBASLVCTL register.
21	RW	RW	PBASLVCTL2_BUF_ALLOC_B: Read Buffer Pair B Allocation The Master ID that uses this PBASLVCTL may use only the allocated buffers. Buffer allocation is for a buffer pair. Multiple buffer pairs may be assigned.
22	RW	RW	PBASLVCTL2_BUF_ALLOC_C: Read Buffer Pair C Allocation The Master ID that uses this PBASLVCTL may use only the allocated buffers. Buffer allocation is for a buffer pair. Multiple buffer pairs may be assigned.

Registers Specification

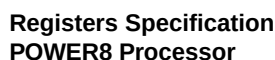
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Bits	PIB	OCI	Field Mnemonic: Description
23	RW	RW	PBASLVCTL2_RESERVED_23: Spare buffer allocation bit.
24	RW	RW	PBASLVCTL2_DIS_WRITE_GATHER: Disable Write Gather. This bit disables gathering of write data in the buffer. This mode bit is used only when PBASLVCTL[Write ttype] = DMA_PR_W. Otherwise it is ignored. OFF - Gather writes into the write buffer ON - Do not gather. Writes are forwarded to the processor bus as written from the OCI.
25:27	RW	RW	PBASLVCTL2_WR_GATHER_TIMEOUT: Write Gather Timeout Control. These bits control how long the PBA should wait to gather write operations. This mode bit is used only when PBASLVCTL[Write ttype] = DMA_PR_W. Otherwise it is ignored. The PBA counts Write Gather Timeout Pulses that arrive every 64 OCI cycles. Write gather timeouts must NOT be disabled if multiple masters are enabled to write through the PBA. 000 - Disable Write Gather Timeout. Write will be flushed under the following conditions: Need another write by the same master to a non-sequential address, Gathered data to cache line boundary, Read by a master that uses this same SLVCTL register to the same address, or a PBASLVRST[SLV Reset(n)] for this PBASLVCTL. 100 - 2 Pulses (64 to 128 OCI cycles) 101 - 4 Pulses (192 to 256 OCI cycles) 110 - 8 Pulses (448 to 512 OCI cycles) 111 - 16 Pulses (960 to 1024 OCI cycles)
28:34	RW	RW	PBASLVCTL2_WRITE_TSIZE: When PBASLVCTL[Write Ttype] = Atomic RNW no fetch, these bits provide a secondary encoding for the atomic operation defined as 'fff011'. The 'fff' specify the function to be applied to the operand. Only 8-byte operations are supported. Supported 'fff' values: 000 - armw_add 001 - armw_and 010 - armw_or 011 - armw_xor
35:48	RW	RW	PBASLVCTL2_EXTADDR: PB Extaddr This bits are the processor bus address bits (23:36) that may be used when forwarding the operation if the selected PBABARMSK bits are one.
49:50	RW	RW	PBASLVCTL2_RESERVED_49_50: Spare
51:63	RO	RO	Constant = 0b00000000000000

Register Name	PBA Slave Control 3 Register
Mnemonic	EN.TPC.PBA.PBASLVCTL3
Address	0000000000064007 (PIB) 0000000040020038 (OCI)
Attributes	Magic=true
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0	RW	RW	PBASLVCTL3_ENABLE: OCI_Base_Address_Range_Enabled This bit must be set by software for the PBA to respond to an OCI request that targets the processor bus and matches the OCI MasterID Match Value. OFF - Ignore OCI operations ON - Accept OCI operations
1:3	RW	RW	PBASLVCTL3_MID_MATCH_VALUE: OCI Masterid Match Value These bits must be initialized by software to indicate the OCI master ID that will use this set of Base Address Registers when the OCI request targets the processor bus region. Only ONE PBASLVCTLn may match any Master ID.
4	RW	RW	PBASLVCTL3_RESERVED_4: Spare
5:7	RW	RW	PBASLVCTL3_MID_CARE_MASK: OCI Masterid Care Mask These bits must be initialized by software to indicate which OCI Masterid bits must match the OCI Master ID Match Value. If only one OCI Master is using this PBASLVCTL , these bits must be set to '111'.

Bits	PIB	OCI	Field Mnemonic: Description
8:10	RW	RW	PBASLVCTL3_WRITE_TTYPE: Write Ttype. Forwarded write requests that target this PBASLVCTL Register use the specified write ttype on the processor bus. DMA uses a DMA_PR_W to write 1 - 127 bytes or a CL_DMA_W_I to write the gathered 128 bytes. LCO_M is a Lateral Castout M that is used only at IPL time. Cache_Inj is a cache-line DMA cache inject ttype that is used only at IPL time to write an L3 line that has already been initialized. CI_PR_WR is a cache inhibited partial write ttype implemented to write to the POWER8 Memory Buffer register space. It forwards the write exactly as it was asked for in the OCI operation. Atomic is an Atomic RMW operation that should only be done as an 8-byte write. DMA=>0b000 LCO_M=>0b001 ATOMIC=>0b010 CACHE_INJ=>0b011 CI_PR_W=>0b100
11:14	RW	RW	PBASLVCTL3_RESERVED_11_14: Spare
15	RW	RW	PBASLVCTL3_READ_TTYPE: Read Ttype. Forwarded read request that targets this PBASLVCTL Register uses the specified ttype on the processor bus. CL_RD_NC is a Cache Line DMA Read with no intent to cache. It will always read 128 bytes from system memory. CI_PR_RD is a Cache Inhibited Partial Read. It will forward the read exactly as it was asked for in the OCI operation. This mode is required when accessing the POWER8 Memory Buffer register space. CL_RD_NC=>0b0 CI_PR_RD=>0b1
16:17	RW	RW	PBASLVCTL3_READ_PREFETCH_CTL: Read Prefetch Control. Auto Early Prefetch Ahead - Prefetch current and next 128-byte cache line on first read. Buffers are used in pairs. This mode should not be used if two or more masters need to share a buffer pair. No Prefetch Ahead - Fetch only current requested 128-byte cache line. This mode can be used if two or more masters are allocated to the same buffer pair. Auto Late Prefetch Ahead - Prefetch next cache line after last read data returned for current cache line. This mode can also be used if two masters need to share a buffer pair but the PBAMODE [dis_mstid_match_pref_inv] mode bit must be set to avoid a hang condition. AUTO_EARLY=>0b00 NONE=>0b01 AUTO_LATE=>0b10
18	RW	RW	PBASLVCTL3_BUF_INVALIDATE_CTL: Read Buffer Invalidate Control. 0 - Do not invalidate read buffer data automatically.
19	RW	RW	PBASLVCTL3_BUF_ALLOC_W: Write Buffer Pair Allocation. The Master ID that uses this PBASLVCTL can use only the allocated buffers. Buffer allocation is for a buffer pair. Multiple buffer pairs can be assigned. This bit must be set for the PBA to respond to write operations through this PBASLVCTL Register.
20	RW	RW	PBASLVCTL3_BUF_ALLOC_A: Read Buffer Pair A Allocation. The Master ID that uses this PBASLVCTL can use only the allocated buffers. Buffer allocation is for a buffer pair. Multiple buffer pairs can be assigned. At least one read buffer must be allocated for the PBA to respond to read operations through this PBASLVCTL Register.
21	RW	RW	PBASLVCTL3_BUF_ALLOC_B: Read Buffer Pair B Allocation. The Master ID that uses this PBASLVCTL can use only the allocated buffers. Buffer allocation is for a buffer pair. Multiple buffer pairs can be assigned.
22	RW	RW	PBASLVCTL3_BUF_ALLOC_C: Read Buffer Pair C Allocation. The Master ID that uses this PBASLVCTL can use only the allocated buffers. Buffer allocation is for a buffer pair. Multiple buffer pairs may be assigned.



Register Name	PBA Block Copy Download Engine Control Register
Mnemonic	EN.TPC.PBA.BCDE_CTL
Address	0000000000064010 (PIB) 0000000040020080 (OCI)
Attributes	
Description	

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Register Name	<i>PBA Block Copy Download Engine Setup Register</i>
Mnemonic	EN.TPC.PBA.BCDE_SET
Address	0000000000064011 (PIB) 0000000040020088 (OCI)
Attributes	
Description	

[illegible]

Register Name	PBA Block Copy Download Engine Status Register
Mnemonic	EN.TPC.PBA.BCDE_STAT
Address	0000000000064012 (PIB) 0000000040020090 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0	ROX	ROX	BCDE_STAT_RUNNING: BCDE Running This bit is set after the BCDE_CTL[Start] is set to '1'. It is cleared when the BCDE_STAT[Done] , [Stopped] , or [Error] bit is set.
1	ROX	ROX	BCDE_STAT_WAITING: BCDE Waiting This bit is set after the BCDE_CTL[Start] is set to '1' and BCDE is waiting to gain ownership of Buffer 'C' or BCDE_CTL[Stop] is set to '1' and BCDE is waiting for pending operations to complete.
2:7	ROX	ROX	BCDE_STAT_WRCMP: BCDE Copy Write Complete These bits are valid only when the 'Running', 'Stopped', or 'Done' bits are set in this register. These bits define the number of bytes worth of data that have been transferred to the SRAM without an error. 0x00 - No bytes transferred 0x01 - 128 bytes transferred 0x02 - 256 bytes transferred . . . 0x1F - 3968 bytes transferred 0x20 - 4096 bytes transferred
8:13	RO	RO	Constant = 0b000000
14:19	ROX	ROX	BCDE_STAT_RDCMP: 0x00 - No bytes read 0x01 - 128-byte read 0x02 - 256 bytes read . . . 0x1F - 3968 bytes read 0x20 - 4096 bytes read
20:28	ROX	ROX	BCDE_STAT_DEBUG: BCDE Debug Status These bits are a glimpse into the Block Copy Engine other state machine bits for debug purposes only. bit 0: rdtrans0 bit 1: wrtrans0 bit 2: waitfor0 bit 3: rdtrans1 bit 4: wrtrans1 bit 5: waitfor1 bit 6: finish bits 7:8 Reserved

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Bits	PIB	OCI	Field Mnemonic: Description
29	ROX	ROX	BCDE_STAT_STOPPED: BCDE Stopped This bit is set and pba_occ_bcde_attn is asserted when the BCDE has been stopped cleanly by a write to BCDE_CTL[Stop]=1 and the originally defined byte transfer has not completed. This bit is reset by hardware when the BCDE_CTL register is written.
30	ROX	ROX	BCDE_STAT_ERROR: BCDE Error This bit is set and pba_occ_error is asserted when the BCDE has detected an error. It may also be set if an error was detected while stopping the BCDE. The PBAFIR indicates the detected error. This bit is reset by hardware when the BCDE_CTL register is written.
31	ROX	ROX	BCDE_STAT_DONE: BCDE Done This bit is set to '1' and pba_occ_bcde_attn is asserted when the Block Copy Engine has completed the transfer. It is reset by hardware when the BCDE_CTL register is written.
32:63	RO	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>PBA Block Copy Download Engine Processor Bus Address Register</i>
Mnemonic	EN.TPC.PBA.BCDE_PBADR
Address	0000000000064013 (PIB) 0000000040020098 (OCI)
Attributes	
Description	

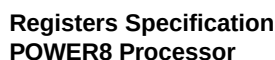
Bits	PIB	OCI	Field Mnemonic: Description
0:1	RW	RW	BCDE_PBADR_RESERVED_0_1: Spare
2:24	RW	RW	BCDE_PBADR_PB_OFFSET: Processor bus offset. These bits define the starting processor bus cache line address to read for the Block Copy Download Engine transfer. This address is used to select the PBABARBARMSK pair and is remapped to the real processor bus address. See 'Block Copy Engine Processor Bus Address Map'.
25:26	RW	RW	BCDE_PBADR_RESERVED_25_26: Spare
27:40	RW	RW	BCDE_PBADR_EXTADDR: Extended address. These bits define bits (23:36) of the processor bus cache line address to use to read for the Block Copy Download Engine transfer.
41:42	RW	RW	BCDE_PBADR_RESERVED_41_42: Spare
43:63	RO	RO	Constant = 0b000000000000000000000000

Register Name	<i>PBA Block Copy Download Engine OCI Address Register</i>
Mnemonic	EN.TPC.PBA.BCDE_OCIBAR
Address	0000000000064014 (PIB) 00000000400200A0 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:24	RW	RW	BCDE_OCIBAR_ADDR: OCI_Base_Address These bits define the starting OCI 128-byte aligned address to Write for the Block Copy Download Engine transfer. 0:24 - Starting OCI Address.
25:63	RO	RO	Constant = 0b00000000000000000000000000000000

[illegible][illegible]

Register Name	PBA Block Copy Upload Engine Status Register
Mnemonic	EN.TPC.PBA.BCUE_STAT
Address	0000000000064017 (PIB) 00000000400200B8 (OCI)
Attributes	
Description	



Register Name	PBA Block Copy Upload Engine Processor Bus Address Register
Mnemonic	EN.TPC.PBA.BCUE_PBADR
Address	0000000000064018 (PIB) 00000000400200C0 (OCI)
Attributes	
Description	

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Bits	PIB	OCI	Field Mnemonic: Description
41:42	RW	RW	BCUE_PBADR_RESERVED_41_42: Spare
43:63	RO	RO	Constant = 0b000000000000000000000000

Register Name	<i>PBA Block Copy Upload Engine OCI Address Register</i>
Mnemonic	EN.TPC.PBA.BCUE_OCIBAR
Address	0000000000064019 (PIB) 00000000400200C8 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:24	RW	RW	BCUE_OCIBAR_ADDR: OCI_Base_Address These bits define the starting OCI 128-byte aligned address to Read for the Block Copy Upload Engine transfer. 0:24 - Starting OCI Address.
25:63	RO	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>PBA PBAX Send Transaction Register</i>
Mnemonic	EN.TPC.PBA.PBAXSNDTX
Address	0000000000064020 (PIB) 0000000040020100 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:2	RW	RW	PBAXSNDTX_SND_SCOPE: Note: Reserved fields are for Nodal, Remote Group Pump and Foreign scopes. However, these are not supported and cannot be programmed as such. The Default is SYSTEM scope. GROUP=>0b001 SYSTEM=>0b010
3	RW	RW	PBAXSNDTX_SND_QID: PBAX Queue Id This bit controls which push queue is the target at the PBAX Receive. 0 : Sync Queue 1 : Doorbell Queue
4	RW	RW	PBAXSNDTX_SND_TYPE: 0 - Unicast 1 - Broadcast
5	RW	RW	PBAXSNDTX_SND_RESERVATION: Note: A reservation is necessary for real-time broadcasts.
6:7	RW	RW	PBAXSNDTX_RESERVED_6_7: Spare
8:10	RW	RW	PBAXSNDTX_SND_NODEID: PBAX Send Nodeid(0:2) Value used by PBAX Send engine to indicate target(s) for PMISC message.
11:13	RW	RW	PBAXSNDTX_SND_CHIPID: PBAX Send Chipid(0:2) Value used by PBAX Send engine to indicate target(s) for PMISC message
14:15	RW	RW	PBAXSNDTX_RESERVED_14_15: Spare
16:63	RO	RO	Constant = 0b00000000000000000000000000000000

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Register Name	PBA PBAX Configuration Register		
Mnemonic	EN.TPC.PBA.PBAXCFG		
Address	0000000000064021 (PIB) 0000000040020108 (OCI)		
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0	RW	RW	PBAXCFG_PBAX_EN: 0 - Disabled: writes to the PBAX DataHi Register occur but the processor bus PMISC operations do not take place. 1 - Enabled: writes to the PBAX DataHi Register cause the atomic processor bus PMISC Hi Data/Lo Data phases to occur.
1	RW	RW	PBAXCFG_RESERVATION_EN: Architectural Note. This bit is intended to be set (enabled) in the chip that is the power domain OCC Master that is performing the real-time power measurement distribution and reset (disabled) in all other chips in the power domain. This keeps any other OCCs (including Voltage Masters) from producing reservation broadcasts that can lead to PBAX livelocks.
2	WOX	WOX	PBAXCFG_SND_RESET: PBAX Send Reset. Setting this bit to a '1' on a register write clears the snd_error condition in the PBAXSNDSTAT Register.
3	WOX	WOX	PBAXCFG_RCV_RESET: PBAX Receive Reset Setting this bit to a '1' on a register write clears the rcv_error condition in the PBAXRCVSTAT register.
4:6	RW	RW	PBAXCFG_RCV_NODEID: Receive PBAX Nodeid Value that indicates this PBA's PBAX Node affinity. This is matched to pbax_nodeid of the PMISC Address phase.
7:9	RW	RW	PBAXCFG_RCV_CHIPID: Receive PBAX Chipid Value that indicates this PBA's PBAX Chipid within the PBAX node. Is matched to pbax_chipid of the Address phase if pbax_type=unicast.
10:11	RW	RW	PBAXCFG_RESERVED_10_11: Spare
12:19	RW	RW	PBAXCFG_RCV_BRDCST_GROUP: Receive PBAX Broadcast Group Vector that is indexed when decoded PMISC pbax_type=broadcast with the decoded PMISC pbax_chipid value. If the bit in this vector at the decoded bit location is a 1, then this receive engine will participate in the broadcast operation.
20:24	RW	RW	PBAXCFG_RCV_DATATO_DIV: 00000 - Data Timeout is Disabled 00001 - divided hang pulse = PBAX hang pulse 00010 - divided hang pulse = PBAX hang pulse2 00011 - divided hang pulse = PBAX hang pulse3 . . . 11111 - divided hang pulse = PBAX hang pulse31
25:26	RW	RW	PBAXCFG_RESERVED_25_26: Spare
27	RW	RW	PBAXCFG_SND_RETRY_COUNT_OVERCOM: PBAX Send Retry count overcommit. Mode bit to count overcommit retries for the send retry threshold when sending PBAX commands on the processor bus.
28:35	RW	RW	PBAXCFG_SND_RETRY_THRESH: 0x00 : No Timeout 0x01 : 1 attempt 0x02 : 2 attempts ... 0xFF : 255 attempts
36:40	RW	RW	PBAXCFG_SND_RSVTO_DIV: 00000 - Send Reservation Timeout is Disabled 00001 - divided hang pulse = PBAX hang pulse 00010 - divided hang pulse = PBAX hang pulse2 00011 - divided hang pulse = PBAX hang pulse3 ... 11111 - divided hang pulse = PBAX hang pulse31



Bits	PIB	OCI	Field Mnemonic: Description
41:63	RO	RO	Constant = 0b000000000000000000000000

Register Name	<i>PBA PBAX Send Status Register</i>
Mnemonic	EN.TPC.PBA.PBAXSNDSTAT
Address	0000000000064022 (PIB) 0000000040020110 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0	ROX	ROX	PBAXSNDSTAT_SND_IN_PROGRESS: If PBAXCFG[pbax_en=0] (disabled), this bit is not set and the PBAX PMISC is not forwarded.
1	ROX	ROX	PBAXSNDSTAT_SND_ERROR: PBAX Send Error This bit is set when an error is detected while sending a PBAX request. The detailed reasons for setting this error bit are defined in the PBAFIR(bits tbd). If the correspond bit is set in the PBAOCCACT register, the pba_occ_error output pin is asserted. This bit is cleared by writing PBAXCFG[snd_reset] = 1.
2:7	ROX	ROX	PBAXSNDSTAT_SND_STATUS: TBD.
8:15	ROX	ROX	PBAXSNDSTAT_SND_RETRY_COUNT: Reset to 0, on the successful write of the PBAX Send DataHi Register.
16:63	RO	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000

Register Name	<i>PBA PBAX Send Data Register</i>
Mnemonic	EN.TPC.PBA.PBAXSNDDAT
Address	0000000000064023 (PIB) 0000000040020118 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:31	RW	RW	PBAXSNDDAT_PBAX_DATAHI: If PBAX Control1.pbax_en = 1 AND PBAX Status.pbax_send_in_progress = 1, this register is not updated and an error indication is set in the LFIR.
32:63	RW	RW	PBAXSNDDAT_PBAX_DATALO: If this written with an odd 4-byte address (using the PPC405), the data is stored in the PBAX Send Engine, but no processor bus operation is started.

Register Name	<i>PBAX Receive Status Register</i>
Mnemonic	EN.TPC.PBA.PBAXRCVSTAT
Address	0000000000064024 (PIB) 0000000040020120 (OCI)
Attributes	
Description	



Register Name		<i>PBA Base Address Range Mask Register 0</i>
Mnemonic		EN.TPC.PBA.SCOMTRUST.PBABARMSK0
Address		0000000002013F04 (SCOM)
Attributes		Secure=true, Magic=true
Description		
Bits	SCOM	Field Mnemonic: Description
0:22	RO	Constant = 0b000000000000000000000000
23:43	RW	PBABARMSK0_MSK: Processor Bus Base Address Mask. When set to a '1', the OCI Address (5:11) and PBASLVCTL[ExtAddr(23:36)] is used instead of the PB Base Address in that bit position. See the diagram of the OCI Address Mapping to processor bus. Default to allow access to first 8M of memory.
44:63	RO	Constant = 0b000000000000000000000000

Register Name		<i>PBA Base Address Range Register 1</i>
Mnemonic		EN.TPC.PBA.SCOMTRUST.PBABAR1
Address		0000000002013F01 (SCOM)
Attributes		Secure=true, Magic=true
Description		
Bits	SCOM	Field Mnemonic: Description
0:2	RW	PBABAR1_CMD_SCOPE: NODAL=>0b000 GROUP=>0b001 SYSTEM=>0b010 RGP=>0b011 FOREIGN0=>0b100 FOREIGN1=>0b101
3	RW	PBABAR1_RESERVED_3: Spare
4:13	RO	Constant = 0b000000000000
14:43	RW	PBABAR1_ADDR: Processor Bus Base Address. These bits and the PBA Base Address Mask Register define how the OCI address is mapped to the processor bus by the PBA slave and how the processor bus address offset is mapped by the Block Copy Engine. 14:22 - PB Base Address bit not maskable. Used as-is on the processor bus. 23:43 - PB Base Address bits maskable with PBABARMSK0
44:63	RO	Constant = 0b000000000000000000000000

Register Name		<i>PBA Base Address Range Mask Register 1</i>
Mnemonic		EN.TPC.PBA.SCOMTRUST.PBABARMSK1
Address		0000000002013F05 (SCOM)
Attributes		Secure=true, Magic=true
Description		
Bits	SCOM	Field Mnemonic: Description
0:22	RO	Constant = 0b000000000000000000000000
23:43	RW	PBABARMSK1_MSK: Processor Bus Base Address Mask. When set to a '1', the OCI Address (5:11) and PBASLVCTL[ExtAddr(23:36)] is used instead of the PB Base Address in that bit position. See the diagram of the OCI Address Mapping to Processor Bus. Default to allow access to first 8M of memory.

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Bits	SCOM	Field Mnemonic: Description
44:63	RO	Constant = 0b00000000000000000000

Register Name	<i>PBA Base Address Range Register 2</i>
Mnemonic	EN.TPC.PBA.SCOMTRUST.PBABAR2
Address	0000000002013F02 (SCOM)
Attributes	Secure=true, Magic=true
Description	

Bits	SCOM	Field Mnemonic: Description
0:2	RW	PBABAR2_CMD_SCOPE: NODAL=>0b000 GROUP=>0b001 SYSTEM=>0b010 RGP=>0b011 FOREIGN0=>0b100 FOREIGN1=>0b101
3	RW	PBABAR2_RESERVED_3: Spare
4:13	RO	Constant = 0b0000000000
14:43	RW	PBABAR2_ADDR: Processor Bus Base Address. These bits and the PBA Base Address Mask register define how the OCI address is mapped to the Processor bus by the PBA slave and how the Processor bus address offset is mapped by the Block Copy Engine. 14:22 - PB Base Address bit not maskable. Used as-is on the processor bus. 23:43 - PB Base Address bits maskable with PBABARMSK _n
44:63	RO	Constant = 0b00000000000000000000

Register Name	<i>PBA Base Address Range Mask Register 2</i>
Mnemonic	EN.TPC.PBA.SCOMTRUST.PBABARMSK2
Address	0000000002013F06 (SCOM)
Attributes	Secure=true, Magic=true
Description	

Bits	SCOM	Field Mnemonic: Description
0:22	RO	Constant = 0b000000000000000000000000
23:43	RW	PBABARMSK2_MSK: Processor Bus Base Address Mask. When set to a '1', the OCI address (5:11) and PBASLVCTL[ExtAddr(23:36)] is used instead of the PB Base Address in that bit position. See the diagram of the OCI Address Mapping to processor bus. Default to allow access to first 8M of memory.
44:63	RO	Constant = 0b000000000000000000000000

Register Name	<i>PBA Base Address Range Register 3</i>
Mnemonic	EN.TPC.PBA.SCOMTRUST.PBABAR3
Address	0000000002013F03 (SCOM)
Attributes	Secure=true, Magic=true
Description	



Bits	SCOM	Field Mnemonic: Description
0:2	RW	PBABAR3_CMD_SCOPE: NODAL=>0b000 GROUP=>0b001 SYSTEM=>0b010 RGP=>0b011 FOREIGN0=>0b100 FOREIGN1=>0b101
3	RW	PBABAR3_RESERVED_3: Spare
4:13	RO	Constant = 0b0000000000
14:43	RW	PBABAR3_ADDR: Processor Bus Base Address. These bits and the PBA Base Address Mask register define how the OCI address is mapped to the processor bus by the PBA slave and how the processor bus address offset is mapped by the Block Copy Engine. 14:22 - PB Base Address bit not maskable. Used as-is on the processor bus. 23:43 - PB Base Address bits maskable with PBABARMSK _n
44:63	RO	Constant = 0b00000000000000000000

Register Name	<i>PBA Base Address Range Mask Register 3</i>
Mnemonic	EN.TPC.PBA.SCOMTRUST.PBABARMSK3
Address	0000000002013F07 (SCOM)
Attributes	Secure=true, Magic=true
Description	

Bits	SCOM	Field Mnemonic: Description
0:22	RO	Constant = 0b000000000000000000000000
23:43	RW	PBABARMSK3_MSK: Processor Bus Base Address Mask. When set to a '1', the OCI address (5:11) and PBASLVCTL[ExtAddr(23:36)] is used instead of the PB Base Address in that bit position. See the diagram of the OCI Address Mapping to the processor bus. Default to allow access to first 8M of memory.
44:63	RO	Constant = 0b000000000000000000000000

Register Name	<i>PBAX Push Base 0 Register</i>
Mnemonic	EN.TPC.PBA.PBAXSHBR0
Address	0000000000064026 (PIB) 0000000040020130 (OCI)
Attributes	
Description	

Bits	PIB	OCI	Field Mnemonic: Description
0:28	RW	RW	PBAXSHBR0_PUSH_START: PBAX Push Queue Start. Starting address of Push queue (aligned to the length of the queue 8 bytes – 256 bytes). Bits(0:1) of this address should be set to '11' to target the SRAM.
29:63	RO	RO	Constant = 0b00000000000000000000000000000000

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Register Name		PBAX Push Control/Status 0 Register	
Mnemonic		EN.TPC.PBA.PBAXSHCS0	
Address		0000000000064027 (PIB) 0000000040020138 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0	RWX_WCLRP ART	RWX_WCLRPART	PBAXSHCS0_PUSH_FULL: Any write to this register clears this indicator and clears push_write_ptr and push_read_ptr to 0s. (this is a means for resetting the queue hardware) NOT_FULL=>0b0 FULL=>0b1
1	RWX_WSETP ART	RWX_WSETPART	PBAXSHCS0_PUSH_EMPTY: Any write to this register sets this indicator and clears push_write_ptr and push_read_ptr to 0s. (this is a means for resetting the queue hardware) NOT_EMPTY=>0b0 EMPTY=>0b1
2:3	RW	RW	PBAXSHCS0_RESERVED_2_3: Spare
4:5	RW	RW	PBAXSHCS0_PUSH_INTR_ACTION_0_1: b00 - Full (default on hardware initialization) b01 - Not full b10 - Empty b11 - Not empty (doorbell queue setting)
6:10	RW	RW	PBAXSHCS0_PUSH_LENGTH: Push queue length. These bits define the depth of the Push queue. (push_length +1) * 8 bytes. Value mapping: 0b00000: 8 bytes (1 entry) 0b00001: 16 bytes (2 entry) 0b00010: 24 bytes (3 entry) 0b00011: 32 bytes (4 entry) ... 0b11111: 256 bytes (32 entry)
11:12	RO	RO	Constant = 0b00
13:17	RWX_WCLRP ART	RWX_WCLRPART	PBAXSHCS0_PUSH_WRITE_PTR: Writes to this field are ignored. Hardware performs all modifications. This field is cleared upon a write to this register.
18:20	RO	RO	Constant = 0b000
21:25	RWX_WCLRP ART	RWX_WCLRPART	PBAXSHCS0_PUSH_READ_PTR: This field is cleared upon a write to this register.
26:30	RO	RO	Constant = 0b00000
31	RW	RW	PBAXSHCS0_PUSH_ENABLE: If disabled, PMISC PBAX commands are ignored and an error indication is set. Note: OCI writes to PBAX Push Increment [n] Register to cause incrementation and any side effects are unaffected by the setting of this bit. DISABLED=>0b0 ENABLED=>0b1
32:63	RO	RO	Constant = 0b00000000000000000000000000000000 DISABLED=>0b0 ENABLED=>0b1



Register Name		PBAX Push Base 1 Register	
Mnemonic		EN.TPC.PBA.PBAXSHBR1	
Address		000000000006402A (PIB) 0000000040020150 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0:28	RW	RW	PBAXSHBR1_PUSH_START: PBAX Push Queue Start. Starting address of Push queue (aligned to the length of the queue 8 - 256 bytes). Bits(0:1) of this address should be set to '11' to target the SRAM.
29:63	RO	RO	Constant = 0b00000000000000000000000000000000

Register Name		PBAX Push Control/Status 1 Register	
Mnemonic		EN.TPC.PBA.PBAXSHCS1	
Address		000000000006402B (PIB) 0000000040020158 (OCI)	
Attributes			
Description			
Bits	PIB	OCI	Field Mnemonic: Description
0	RWX_WCLRPART	RWX_WCLRPART	PBAXSHCS1_PUSH_FULL: Any write to this register clears this indicator and clears push_write_ptr and push_read_ptr to 0s. (This is a means for resetting the queue hardware.) NOT_FULL=>0b0 FULL=>0b1
1	RWX_WSETPART	RWX_WSETPART	PBAXSHCS1_PUSH_EMPTY: Any write to this register sets this indicator and clears push_write_ptr and push_read_ptr to 0s. (This is a means for resetting the queue hardware.) NOT_EMPTY=>0b0 EMPTY=>0b1
2:3	RW	RW	PBAXSHCS1_RESERVED_2_3: Spare
4:5	RW	RW	PBAXSHCS1_PUSH_INTR_ACTION_0_1: b00 - Full (default upon hardware initialization) b01 - Not full b10 - Empty b11 - Not empty (doorbell queue setting)
6:10	RW	RW	PBAXSHCS1_PUSH_LENGTH: Push queue length. These bits define the depth of the Push queue. (push_length +1) * 8 bytes. Value mapping: 0b00000: 8 bytes (1 entry) 0b00001: 16 bytes (2 entry) 0b00010: 24 bytes (3 entry) 0b00011: 32 bytes (4 entry) ... 0b11111: 256 bytes (32 entry)
11:12	RO	RO	Constant = 0b00
13:17	RWX_WCLRPART	RWX_WCLRPART	PBAXSHCS1_PUSH_WRITE_PTR: Writes to this field are ignored. Hardware performs all modifications. This field is cleared on a write to this register.
18:20	RO	RO	Constant = 0b000

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Bits	PIB	OCI	Field Mnemonic: Description
21:25	RWX_WCLRPART	RWX_WCLRPART	PBAXSHCS1_PUSH_READ_PTR: This field is cleared on a write to this register.
26:30	RO	RO	Constant = 0b00000
31	RW	RW	PBAXSHCS1_PUSH_ENABLE: If Disabled, PMISC PBAX commands are ignored and an error indication is set. Note: OCI Writes to PBAX Push Increment [n] Register to cause incrementation and any side effects are unaffected by the setting of this bit. DISABLED=>0b0 ENABLED=>0b1
32:63	RO	RO	Constant = 0b00000000000000000000000000000000 DISABLED=>0b0 ENABLED=>0b1

Register Name	<i>TX And Common Control Status Register</i>
Mnemonic	EN.TPC.PSI.PSI_WRAP.TX_CTRL_STAT_REG
Address	0000000002010800 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	ENABLE_SCWR_TO_TXRF: OFF: Disable SCOM write to TX RF ON: Enable SCOM write to TX RF
1	RW	DISABLE_ECC_COR_GXC_PSI: OFF: Enable ECC Correction GXC PSI ON: Disable ECC Correction GXC PSI
2	RW	DISABLE_ECC_COR_TXRF_PSI: OFF: Enable ECC Correction TXRF PSI ON: Disable ECC Correction TXRF PSI
3	RW	TX_CRC_MODE: OFF: TX_CRC-16 Mode ON: TX_CRC-32 Mode
4	RW	TX_CHIP_PERSONALISATION: OFF: TX Processor Chip ON: TX FSP-1 Chip
5	RW	TX_ENABLE_STREAMING_MODE: OFF: TX Disable Streaming Mode ON: TX Enable Streaming Mode
6	RW	TX_CHIP_INTERFACEMODE: ON: Processor Chip ON: FSP-1 Chip
7	RW	DISABLE_TIMEOUT_AND_RETRY: OFF: Enable Timeout and Retry Function ON: Disable Timeout and Retry Function
8	RW	FENCE_IO_INTERFACE: OFF: no fence I/O interface ON: fence I/O interface
9	RO	Reserved
10	RO	Reserved
11	RW	Reserved field. (Access type is txsc)
12:31	RO	Constant = 0b000000000000000000000000



Register Name	<i>TX Error Register</i>
Mnemonic	EN.TPC.PSI.PSI_WRAP.TX_ERROR_REG
Address	0000000002010802 (PCB) 0000000002010804 (PCB1)
Attributes	
Description	

Bits	PCB	PCB1	Field Mnemonic: Description
0	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c1_psitxins_data_pck)
1	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c1_psitxins_tzrtmp_pck)
2	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c1_psitxei_shift_pck)
3	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c1_psitxei_transmit_pck)
4	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c1_psitxins_parity)
5	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c1_psitxins_underrun)
6	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c2_psitxbff_data_pck)
7	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c1_psitxbff_tdo_pck)
8	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c2_psitxbff_tfc_pck)
9	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c2_psitxlc_fsm_pck)
10	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c3_psitxlc_data_buff_pck)
11	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c2_psitxlc_tdo_pck)
12	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c2_psitxlc_taddr_pck)
13	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c2_psitxlc_tctrl_pck)
14	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c2_psitxlc_ue_rf)
15	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c0_psitxlc_ce_rf)
16	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c3_psitxlc_ue_gx_2n)
17	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c0_psitxlc_ce_gx_2n)
18	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c3_psitxlc_data_gxst2_pck_2n)
19	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c3_psitxlc_data_gxst3_pck_2n)

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Bits	PCB	PCB1	Field Mnemonic: Description
20	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c3_psirfacc_taddr_pck)
21	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c3_psirfacc_tctrl_pck)
22	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c3_psirfacc_tdl_cmd_ctrl_pck)
23	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c3_psirfacc_tdl_rsp_ctrl_pck)
24	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c3_psirfacc_tfsm_pck)
25	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c3_psirfacc_tdl_fsm_pck)
26	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c4_psirfacc_txsc_pck)
27	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c3_psirfacc_tdl_retry_err)
28:31	RO	N/A	Constant = 0b0000

Register Name	<i>TX Data Flow FSM</i>
Mnemonic	EN.TPC.PSI.PSI_WRAP.TX_DF_FSM_REG
Address	0000000002010806 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RWX	Reserved field. (Access type is tx_df_fsm)
4:31	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>RX Control Status Register</i>
Mnemonic	EN.TPC.PSI.PSI_WRAP.RX_CTRL_STAT_REG
Address	0000000002010808 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	ENABLE_SCWR_TO_RXRF: OFF: Disable SCOM write to RX RF ON: Enable SCOM write to RX RF
1	RW	Reserved field. (Access type is rxsc)
2	RW	DISABLE_ECC_COR_RXRF_PSI: OFF: Enable ECC Correction RXRF PSI ON: Disable ECC Correction RXRF PSI
3	RW	RX_CRC_MODE: OFF: RX_CRC-16 Mode ON: RX_CRC-32 Mode
4	RW	ENABLE_SCRD_FR_RXRF: OFF: Disable SCOM read from RX RF ON: Enable SCOM read from RX RF



Bits	PCB	Field Mnemonic: Description
5	RW	RX_ENABLE_STREAMING_MODE: OFF: RX Disable Streaming Mode ON: RX Enable Streaming Mode
6	RW	RX_CHIP_INTERFACEMODE: ON: RX Processor Chip ON: RX FSP-1 Chip
7	RW	RX_CHIP_PERSONALISATION: OFF: RX Processor Chip ON: RX FSP-1 Chip
8:31	RO	Constant = 0b000000000000000000000000

Register Name	<i>RX Error Register</i>
Mnemonic	EN.TPC.PSI.PSI_WRAP.RX_ERROR_REG
Address	000000000201080A (PCB) 000000000201080C (PCB1)
Attributes	
Description	

Bits	PCB	PCB1	Field Mnemonic: Description
0	RWX_WCLEA R	WOX_OR	Reserved field. (Access type is c1_psirxins_rfgshift_pck)
1	RWX_WCLEA R	WOX_OR	Reserved field. (Access type is c1_psirxins_rzrtmp_pck)
2	RWX_WCLEA R	WOX_OR	Reserved field. (Access type is c1_psirxins_data_pck)
3	RWX_WCLEA R	WOX_OR	Reserved field. (Access type is c1_psirxei_shift_pck)
4	RWX_WCLEA R	WOX_OR	Reserved field. (Access type is c1_psirxei_transmit_pck)
5	RWX_WCLEA R	WOX_OR	Reserved field. (Access type is c1_psirxins_overrun)
6	RWX_WCLEA R	WOX_OR	Reserved field. (Access type is c1_psirxbff_data_pck)
7	RWX_WCLEA R	WOX_OR	Reserved field. (Access type is c2_psirxbff_datao_pck)
8	RWX_WCLEA R	WOX_OR	Reserved field. (Access type is c2_psirxbff_rfc_pck)
9	RWX_WCLEA R	WOX_OR	Reserved field. (Access type is c2_psirxlc_fsm_pck)
10	RWX_WCLEA R	WOX_OR	Reserved field. (Access type is c3_psirxlc_data_buff_pck)
11	RWX_WCLEA R	WOX_OR	Reserved field. (Access type is c2_psirxlc_data_pck)
12	RWX_WCLEA R	WOX_OR	Reserved field. (Access type is c2_psirxlc_raddr_pck)
13	RWX_WCLEA R	WOX_OR	Reserved field. (Access type is c2_psirxlc_rctrl_pck)
14	RWX_WCLEA R	WOX_OR	Reserved field. (Access type is c3_psirxlc_ue_rf)

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Bits	PCB	PCB1	Field Mnemonic: Description
15	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c0_psirxlc_ce_rf)
16	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c2_psirxlc_data_gxst1_pck_2n)
17	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c2_psirfacc_raddr_pck)
18	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c2_psirfacc_rctrl_pck)
19	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c3_psirfacc_rfsm_pck)
20	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c3_psirfacc_rdl_fsm_pck)
21	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c4_psirfacc_rxsc_pck)
22	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c0_psirfacc_rlink_state_lt_02)
23	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c0_psirfacc_c_rxdata_rdy_err)
24	RWX_WCLEAR	WOX_OR	Reserved field. (Access type is c0_errack_rise)
25:31	RO	N/A	Constant = 0b00000000

Register Name	<i>RX Data Flow FSM</i>
Mnemonic	EN.TPC.PSI.PSI_WRAP.RX_DF_FSM_REG
Address	000000000201080E (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RWX	Reserved field. (Access type is rx_df_fsm)
4:31	RO	Constant = 0b000000000000000000000000

Register Name	<i>TX Channel Internal Address Register</i>
Mnemonic	EN.TPC.PSI.PSI_WRAP.TX_CH_INTADDR_REG
Address	0000000002010810 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	Reserved field. (Access type is scom_mode_0)
1	RW	Reserved field. (Access type is scom_mode_1)
2	RW	Reserved field. (Access type is scom_mode_2)
3	RW	Reserved field. (Access type is scom_mode_3)
4	RW	Reserved field. (Access type is scom_mode_4)



Bits	PCB	Field Mnemonic: Description
5	RW	Reserved field. (Access type is scom_mode_5)
6	RW	Reserved field. (Access type is scom_mode_6)
7	RW	Reserved field. (Access type is scom_mode_7)
8:31	RO	Constant = 0b000000000000000000000000

Register Name	<i>TX Channel Misc Register</i>
Mnemonic	EN.TPC.PSI.PSI_WRAP.TX_CH_MISC_REG
Address	0000000002010813 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RWX	Reserved field. (Access type is fsm)
4:6	RO	Constant = 0b000
7:11	RWX	Reserved field. (Access type is tframesize)
12	RWX	Reserved field. (Access type is wen0)
13	RWX	Reserved field. (Access type is wen1)
14	RWX	Reserved field. (Access type is wen2)
15	RWX	Reserved field. (Access type is data_req)
16	RWX	Reserved field. (Access type is start_trans)
17	RWX	Reserved field. (Access type is gxdataavail_q)
18:31	RO	Constant = 0b0000000000000000

Register Name	<i>RX Channel Internal Address Register</i>
Mnemonic	EN.TPC.PSI.PSI_WRAP.RX_CH_INTADDR_REG
Address	0000000002010818 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	Reserved field. (Access type is scom_mode_0)
1	RW	Reserved field. (Access type is scom_mode_1)
2	RW	Reserved field. (Access type is scom_mode_2)
3	RW	Reserved field. (Access type is scom_mode_3)
4	RW	Reserved field. (Access type is scom_mode_4)
5	RW	Reserved field. (Access type is scom_mode_5)
6	RW	Reserved field. (Access type is scom_mode_6)
7	RW	Reserved field. (Access type is scom_mode_7)
8:31	RO	Constant = 0b000000000000000000000000

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Register Name		<i>RX Channel Misc Register</i>
Mnemonic		EN.TPC.PSI.PSI_WRAP.RX_CH_MISC_REG
Address		000000000201081B (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:2	RWX	Reserved field. (Access type is fsm0)
3:6	RWX	Reserved field. (Access type is fsm1)
7:11	RWX	Reserved field. (Access type is tframesize)
12	RWX	Reserved field. (Access type is wen0)
13	RWX	Reserved field. (Access type is wen1)
14	RWX	Reserved field. (Access type is wen2)
15	RWX	Reserved field. (Access type is en_scrd)
16	RWX	Reserved field. (Access type is strtogx)
17:31	RO	Constant = 0b0000000000000000

Register Name		<i>HCA EN FIR Register</i>		
Mnemonic		EN.TPC.BRIDGE.HCA.ENHCA_FIR_REG		
Address		0000000002010940 (SCOM) 0000000002010941 (SCOM1) 0000000002010942 (SCOM2)		
Attributes				
Description		HCA EN FIR Register		
Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	DPX0_DAT_UE: PB0 data UE
1	RWX	WOX_AND	WOX_OR	DPX0_DAT_SUE: PB0 data UE
2	RWX	WOX_AND	WOX_OR	DPX0_DAT_CE: PB0 data ue
3	RWX	WOX_AND	WOX_OR	
4	RWX	WOX_AND	WOX_OR	CO_DROP_COUNTER_FULL: Castout Drop Counter Full
5	RWX	WOX_AND	WOX_OR	DATA_HANG_DETECT: Castout Drop Counter Full
6	RWX	WOX_AND	WOX_OR	UNEXPECTED_DATA_OR_CRESP: Castout Drop Counter Full
7	RWX	WOX_AND	WOX_OR	INTERNAL_ERROR: Castout Drop Counter Full
8	RWX	WOX_AND	WOX_OR	SCOM_ERROR: Internal Error
9	RWX	WOX_AND	WOX_OR	FIR_PARITY_ERROR: Internal Error



Register Name		HCA EN FIR MASK Register		
Mnemonic		EN.TPC.BRIDGE.HCA.ENHCA_FIR_MASK_REG		
Address		0000000002010943 (SCOM) 0000000002010944 (SCOM1) 0000000002010945 (SCOM2)		
Attributes				
Description		HCA EN FIR MASK Register		
Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	DPX0_DAT_UE_MASK: PB0 data UE
1	RW	WO_AND	WO_OR	DPX0_DAT_SUE_MASK: PB0 data UE
2	RW	WO_AND	WO_OR	DPX0_DAT_CE_MASK: PB0 data ue
3	RW	WO_AND	WO_OR	
4	RW	WO_AND	WO_OR	CO_DROP_COUNTER_FULL_MASK: Castout Drop Counter Full
5	RW	WO_AND	WO_OR	DATA_HANG_DETECT_MASK: Castout Drop Counter Full
6	RW	WO_AND	WO_OR	UNEXPECTED_DATA_OR_CRESP_MASK: Castout Drop Counter Full
7	RW	WO_AND	WO_OR	INTERNAL_ERROR_MASK: Castout Drop Counter Full
8	RW	WO_AND	WO_OR	SCOM_ERROR_MASK: Internal Error
9	RW	WO_AND	WO_OR	FIR_PARITY_ERROR_MASK: Internal Error

Register Name		HCA BAR and Range Register	
Mnemonic		EN.TPC.BRIDGE.HCA.HCA_BAR	
Address		000000000201094A (SCOM)	
Attributes			
Description			
Bits	SCOM	Field Mnemonic: Description	
0:13	RO	Constant = 0b0000000000000000	
14:31	RW	HCA_BAR_ADDR: HCA Base Address These bits and the hca_bar_range bits define how the address is mapped to the processor bus Bits(14:23) - Used as is on the processor bus. Bits(24:32) - Maskable with hca_bar_range	
32:40	RW	HCA_BAR_RANGE: Memory size These bits indicate memory size behind the MC. It is used to define the Bar address M4GB=>0b000000000 M8GB=>0b000000001 M16GB=>0b000000011 M32GB=>0b000000111 M64GB=>0b000001111 M128GB=>0b000011111 M256GB=>0b000111111 M512GB=>0b001111111 M1TB=>0b011111111 M2TB=>0b111111111	

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Bits	SCOM	Field Mnemonic: Description
41:61	RO	Constant = 0b000000000000000000000000 M4GB=>0b000000000 M8GB=>0b000000001 M16GB=>0b000000011 M32GB=>0b000000111 M64GB=>0b000001111 M128GB=>0b000011111 M256GB=>0b000111111 M512GB=>0b001111111 M1TB=>0b011111111 M2TB=>0b111111111
62	RW	PAGE_SIZE_64K: Page size 64K enable
63	RW	HCA_BAR_VALID: Bar valid Indicates that the BAR is valid

Register Name	HCA COUNT BAR Register
Mnemonic	EN.TPC.BRIDGE.HCA.HCA_COUNT_BAR
Address	000000000201094B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:22	RO	Constant = 0b000000000000000000000000
23:44	RW	HCA_COUNT_BAR_ADDR: HCA Counter Base Address These bits and the hca_count_bar_range bits define how the address is mapped to the processor bus Bits(23:31) - Maskable with hca_bar_range Bits(32) - Used as is on the processor bus - 4K page mode Bits(33:40) - Maskable with hca_bar_range - 4K page mode Bits(32:36) - Used as is on the processor bus - 64K page mode Bits(37:44) - Maskable with hca_bar_range - 64K page mode
45:62	RO	Constant = 0b000000000000000000000000
63	RW	HCA_COUNT_BAR_VALID: Count Bar valid Indicates that the COUNT BAR is valid

Register Name	HCA DECAY1 Register
Mnemonic	EN.TPC.BRIDGE.HCA.HCA_DECAY1
Address	000000000201094C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	HCA_DECAY_SCOM_VALID: HCA Start DECAY command. This starts a sequencer that issues decay commands based on the decay_scom_addr and by how many decay_scom_count.
1:31	RO	Constant = 0b00000000000000000000000000000000
32:63	RW	HCA_DECAY_SCOM_COUNT: HCA DECAY count. This specifies how many decay commands are issued after decay_scom_valid is set.

Register Name	<i>HCA DECAY2 Register</i>
Mnemonic	EN.TPC.BRIDGE.HCA.HCA_DECAY2
Address	000000000201094D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	RWX	HCA_DECAY_SCOM_DELAY: HCA DECAY delay counter. This counter specifies number of cycles x256 in between decay commands.
32	RO	Constant = 0b0
33:40	RWX	HCA_DECAY_ADDR_COND: HCA DECAY address. This specifies bits 33:40 of the starting address of the decay commands which is conditionally loaded based on range. The upper bits 24:32 use the mcount_bar or the count_bar based on hca_decay_mirror switch.
41:56	RWX	HCA_DECAY_ADDR: HCA DECAY address. This specifies bits 41:56 of the starting address of the decay commands. The upper bits 24:32 use the mcount_bar or the count_bar based on hca_decay_mirror switch.
57:63	RO	Constant = 0b00000000

Register Name	<i>HCA REF BAR Register</i>
Mnemonic	EN.TPC.BRIDGE.HCA.HCA_REF_BAR
Address	000000000201094E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:22	RO	Constant = 0b000000000000000000000000
23:45	RW	HCA_REF_BAR_ADDR: HCA ref base address These bits and the hca_bar_range bits define how the address is mapped to the processor bus. Bits(23:31) - Maskable with hca_bar_range Bits(32:33) - Used as is on the processor bus - 4K page mode Bits(34:41) - Maskable with hca_bar_range - 4K page mode Bits(32:37) - Used as is on the processor bus - 64K page mode Bits(38:45) - Maskable with hca_bar_range - 64K page mode
46:62	RO	Constant = 0b000000000000000000000000
63	RW	HCA_REF_BAR_VALID: ref Bar valid. Indicates that the ref BAR is valid.

Register Name	<i>HCA MODE Register</i>
Mnemonic	EN.TPC.BRIDGE.HCA.HCA_MODES
Address	000000000201094F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:2	RO	Constant = 0b000
3	RW	HCA_PB_32_1: 32:1 castout mode - HCA only sends one out of 32 castouts.

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Bits	SCOM	Field Mnemonic: Description
4	RW	HCA_PB_16_1: 16:1 castout mode - HCA only sends one out of 16 castouts.
5:12	RW	TRACE_SELECT: Trace array select bits.
13:15	RO	Constant = 0b000
16:20	RW	HANG_DIVIDER_CMD: Command hang divider.
21:29	RW	EPSILON_COUNT: Epsilon count.
30:34	RW	HANG_DIVIDER_DATA: Data hang divider.
35:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>HCA RESET Register</i>
Mnemonic	EN.TPC.BRIDGE.HCA.HCA_RESET
Address	0000000002010952 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	N/A	Not implemented.

Register Name	<i>HCA Mirror BAR and Range Register</i>
Mnemonic	EN.TPC.BRIDGE.HCA.HCA_MIRROR_BAR
Address	0000000002010953 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:13	RO	Constant = 0b0000000000000000
14:32	RW	HCA_MIRROR_BAR_ADDR: HCA mirror_Base Address These bits and the hca_mirror_bar_range bits define how the address is mapped to the processor bus. Bits(14:24) - Used as is on the processor bus. Bits(25:32) - Maskable with hca_mirror_bar_range.
33:62	RO	Constant = 0b00000000000000000000000000000000
63	RW	HCA_MIRROR_BAR_VALID: Bar valid. Indicates that the BAR is valid.

Register Name	<i>HCA EH FIR Register</i>
Mnemonic	EH.TPC.HCA.EHHCA_FIR_REG
Address	0000000002010980 (SCOM) 0000000002010981 (SCOM1) 0000000002010982 (SCOM2)
Attributes	
Description	HCA EH FIR Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	CE1_0_OUT: array0_a CE



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
1	RWX	WOX_AND	WOX_OR	CE2_0_OUT: array0_b CE
2	RWX	WOX_AND	WOX_OR	UE1_0_OUT: array0_a ue
3	RWX	WOX_AND	WOX_OR	UE2_0_OUT: array0_b ue
4	RWX	WOX_AND	WOX_OR	CE1_1_OUT: array1_a CE
5	RWX	WOX_AND	WOX_OR	CE2_1_OUT: array1_b CE
6	RWX	WOX_AND	WOX_OR	UE1_1_OUT: array1_a ue
7	RWX	WOX_AND	WOX_OR	UE2_1_OUT: array1_b ue
8	RWX	WOX_AND	WOX_OR	CE1_2_OUT: array2_a CE
9	RWX	WOX_AND	WOX_OR	CE2_2_OUT: array2_b CE
10	RWX	WOX_AND	WOX_OR	UE1_2_OUT: array2_a ue
11	RWX	WOX_AND	WOX_OR	UE2_2_OUT: array2_b ue
12	RWX	WOX_AND	WOX_OR	CE1_3_OUT: array3_a CE
13	RWX	WOX_AND	WOX_OR	CE2_3_OUT: array3_b CE
14	RWX	WOX_AND	WOX_OR	UE1_3_OUT: array3_a ue
15	RWX	WOX_AND	WOX_OR	UE2_3_OUT: array3_b ue
16	RWX	WOX_AND	WOX_OR	CE1_4_OUT: array4_a CE
17	RWX	WOX_AND	WOX_OR	CE2_4_OUT: array4_b CE
18	RWX	WOX_AND	WOX_OR	UE1_4_OUT: array4_a ue
19	RWX	WOX_AND	WOX_OR	UE2_4_OUT: array4_b ue
20	RWX	WOX_AND	WOX_OR	CE1_5_OUT: array5_a CE
21	RWX	WOX_AND	WOX_OR	CE2_5_OUT: array5_b CE
22	RWX	WOX_AND	WOX_OR	UE1_5_OUT: array5_a ue
23	RWX	WOX_AND	WOX_OR	UE2_5_OUT: array5_b ue
24	RWX	WOX_AND	WOX_OR	CE1_6_OUT: array6_a CE
25	RWX	WOX_AND	WOX_OR	CE2_6_OUT: array6_b CE
26	RWX	WOX_AND	WOX_OR	UE1_6_OUT: array6_a ue
27	RWX	WOX_AND	WOX_OR	UE2_6_OUT: array6_b ue
28	RWX	WOX_AND	WOX_OR	CE1_7_OUT: array7_a CE
29	RWX	WOX_AND	WOX_OR	CE2_7_OUT: array7_b CE
30	RWX	WOX_AND	WOX_OR	UE1_7_OUT: array7_a ue
31	RWX	WOX_AND	WOX_OR	UE2_7_OUT: array7_b ue
32	RWX	WOX_AND	WOX_OR	DROP_COUNTER_FULL: Drop Counter Full
33	RWX	WOX_AND	WOX_OR	INTERNAL_ERROR: Internal Error
34	RWX	WOX_AND	WOX_OR	SCOM_ERROR: Internal Error
35	RWX	WOX_AND	WOX_OR	FIR_PARITY_ERROR: Internal Error



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Register Name		HCA EN FIR MASK Register		
Mnemonic		EH.TPC.HCA.EHHCA_FIR_MASK_REG		
Address		0000000002010983 (SCOM) 0000000002010984 (SCOM1) 0000000002010985 (SCOM2)		
Attributes				
Description		HCA EN FIR MASK Register		
Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	CE1_0_OUT_MASK: array0_a CE
1	RW	WO_AND	WO_OR	CE2_0_OUT_MASK: array0_b CE
2	RW	WO_AND	WO_OR	UE1_0_OUT_MASK: array0_a ue
3	RW	WO_AND	WO_OR	UE2_0_OUT_MASK: array0_b ue
4	RW	WO_AND	WO_OR	CE1_1_OUT_MASK: array1_a CE
5	RW	WO_AND	WO_OR	CE2_1_OUT_MASK: array1_b CE
6	RW	WO_AND	WO_OR	UE1_1_OUT_MASK: array1_a ue
7	RW	WO_AND	WO_OR	UE2_1_OUT_MASK: array1_b ue
8	RW	WO_AND	WO_OR	CE1_2_OUT_MASK: array2_a CE
9	RW	WO_AND	WO_OR	CE2_2_OUT_MASK: array2_b CE
10	RW	WO_AND	WO_OR	UE1_2_OUT_MASK: array2_a ue
11	RW	WO_AND	WO_OR	UE2_2_OUT_MASK: array2_b ue
12	RW	WO_AND	WO_OR	CE1_3_OUT_MASK: array3_a CE
13	RW	WO_AND	WO_OR	CE2_3_OUT_MASK: array3_b CE
14	RW	WO_AND	WO_OR	UE1_3_OUT_MASK: array3_a ue
15	RW	WO_AND	WO_OR	UE2_3_OUT_MASK: array3_b ue
16	RW	WO_AND	WO_OR	CE1_4_OUT_MASK: array4_a CE
17	RW	WO_AND	WO_OR	CE2_4_OUT_MASK: array4_b CE
18	RW	WO_AND	WO_OR	UE1_4_OUT_MASK: array4_a ue
19	RW	WO_AND	WO_OR	UE2_4_OUT_MASK: array4_b ue
20	RW	WO_AND	WO_OR	CE1_5_OUT_MASK: array5_a CE
21	RW	WO_AND	WO_OR	CE2_5_OUT_MASK: array5_b CE
22	RW	WO_AND	WO_OR	UE1_5_OUT_MASK: array5_a ue
23	RW	WO_AND	WO_OR	UE2_5_OUT_MASK: array5_b ue
24	RW	WO_AND	WO_OR	CE1_6_OUT_MASK: array6_a CE
25	RW	WO_AND	WO_OR	CE2_6_OUT_MASK: array6_b CE
26	RW	WO_AND	WO_OR	UE1_6_OUT_MASK: array6_a ue
27	RW	WO_AND	WO_OR	UE2_6_OUT_MASK: array6_b ue
28	RW	WO_AND	WO_OR	CE1_7_OUT_MASK: array7_a CE
29	RW	WO_AND	WO_OR	CE2_7_OUT_MASK: array7_b CE
30	RW	WO_AND	WO_OR	UE1_7_OUT_MASK: array7_a ue
31	RW	WO_AND	WO_OR	UE2_7_OUT_MASK: array7_b ue
32	RW	WO_AND	WO_OR	DROP_COUNTER_FULL_MASK: Drop Counter Full



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
33	RW	WO_AND	WO_OR	INTERNAL_ERROR_MASK: Internal Error
34	RW	WO_AND	WO_OR	SCOM_ERROR_MASK: Internal Error
35	RW	WO_AND	WO_OR	FIR_PARITY_ERROR_MASK: Internal Error

Register Name	HCA BAR and Range Register
Mnemonic	EH.TPC.HCA.HCA_BAR
Address	000000000201098A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:13	RO	Constant = 0b0000000000000000
14:31	RW	HCA_BAR_ADDR: HCA base address. These bits and the hca_bar_range bits define how the address is mapped to the processor bus. Bits(14:22) - Used as is on the processor bus. Bits(23:32) - Maskable with hca_bar_range.
32:40	RW	HCA_BAR_RANGE: Memory size. These bits indicate memory size behind the MC. It is used to define the Bar address. M4GB=>0b000000000 M8GB=>0b000000001 M16GB=>0b000000011 M32GB=>0b000000111 M64GB=>0b000001111 M128GB=>0b000011111 M256GB=>0b000111111 M512GB=>0b001111111 M1TB=>0b011111111 M2TB=>0b111111111
41:61	RO	Constant = 0b00000000000000000000 M4GB=>0b000000000 M8GB=>0b000000001 M16GB=>0b000000011 M32GB=>0b000000111 M64GB=>0b000001111 M128GB=>0b000011111 M256GB=>0b000111111 M512GB=>0b001111111 M1TB=>0b011111111 M2TB=>0b111111111
62	RW	PAGE_SIZE_64K: Page size 64K enable.
63	RW	HCA_BAR_VALID: Bar valid. Indicates that the BAR is valid.

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Register Name		HCA COUNT BAR Register
Mnemonic		EH.TPC.HCA.HCA_COUNT_BAR
Address		000000000201098B (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:22	RO	Constant = 0b000000000000000000000000
23:44	RW	HCA_COUNT_BAR_ADDR: HCA Counter Base Address. These bits and the hca_count_bar_range bits define how the address is mapped to the processor bus. Bits(23:31) - Maskable with hca_bar_range Bits(32) - Used as is on the processor bus - 4K page mode Bits(33:40) - Maskable with hca_bar_range - 4K page mode Bits(32:36) - Used as is on the processor bus - 64K page mode Bits(37:44) - Maskable with hca_bar_range - 64K page mode
45:62	RO	Constant = 0b000000000000000000000000
63	RW	HCA_COUNT_BAR_VALID: Count Bar valid. Indicates that the COUNT BAR is valid.

Register Name		HCA REF BAR Register
Mnemonic		EH.TPC.HCA.HCA_REF_BAR
Address		000000000201098E (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:22	RO	Constant = 0b000000000000000000000000
23:45	RW	HCA_REF_BAR_ADDR: HCA ref base address. These bits and the hca_bar_range bits define how the address is mapped to the processor bus. Bits(23:31) - Maskable with hca_bar_range Bits(32:33) - Used as is on the processor bus - 4K page mode Bits(34:41) - Maskable with hca_bar_range - 4K page mode Bits(32:37) - Used as is on the processor bus - 64K page mode Bits(38:45) - Maskable with hca_bar_range - 64K page mode
46:62	RO	Constant = 0b000000000000000000000000
63	RW	HCA_REF_BAR_VALID: REF Bar valid. Indicates that the REF BAR is valid.

Register Name		HCA MODE Register
Mnemonic		EH.TPC.HCA.HCA_MODES
Address		000000000201098F (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:4	RO	Constant = 0b000000

[illegible]

Register Name	HCA FLUSH Register
Mnemonic	EH.TPC.HCA.HCA_FLUSH
Address	000000002010990 (SCOM)
Attributes	
Description	

[illegible]

Register Name	HCA RESET Register
Mnemonic	EH.TPC.HCA.HCA_RESET
Address	0000000002010992 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	N/A	Not implemented.



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Register Name	HCA Mirror BAR and Range Register	
Mnemonic	EH.TPC.HCA.HCA_MIRROR_BAR	
Address	0000000002010993 (SCOM)	
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0:13	RO	Constant = 0b0000000000000000
14:32	RW	HCA_MIRROR_BAR_ADDR: HCA mirror_Base Address These bits and the hca_mirror_bar_range bits define how the address is mapped to the processor bus Bits(14:24) - Used as is on the processor bus. Bits(25:32) - Maskable with hca_mirror_bar_range
33:62	RO	Constant = 0b00000000000000000000000000000000
63	RW	HCA_MIRROR_BAR_VALID: Bar valid Indicates that the BAR is valid

Register Name	ICP BAR Register	
Mnemonic	EN.TPC.INTP.SYNC_BAR_REG	
Address	00000000020109CA (SCOM)	
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0:29	RW	ICP_BAR: Set to compare against bits 14 to 43 of address to define 1 MB region, all bits compared
30	RW	ICP_BAR_EN: Set to 1 to enable ICP to receive loads/stores against its BAR region
31:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	ICP Mode Register 0	
Mnemonic	EN.TPC.INTP.SYNC_MODE_REG0	
Address	00000000020109CB (SCOM)	
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0:7	RW	PRIORITY: priority field used
8	RW	
9:11	RW	SCOPE_INITIAL: scope field used for command
12	RW	
13	RW	NO_HANG2STATUS: do not report hang via rty_other status
14	RW	OPER_DISABLE_HANG: disable operational hang detect
15:19	RW	OPER_HANG_DIV: operational hang detect divider
20	RW	UE_SUE_DD1: DD1 mode for UE/SUE see HW247016
21	RW	
22	RW	DATA_DISABLE_HANG: disable data hang detect



Bits	SCOM	Field Mnemonic: Description
23:27	RW	DATA_HANG_DIV: data hang detect divider
28	RW	BACKOFF_DISABLE: disable backoff for eoi fwd and return queue
29	RW	FWD_QUE_FWD_CONV_DISABLE: disable conversion forward to return after retry limit
30	RW	DISA_WAIT4CRESP_MODE4RIS: Disable wait for cresp upon start for ris cmds
31	RW	DISA_AUTO_NO_RETRY4RIS: Disable automatic force mode, when unfairness is detected (due to request dropping during retry) for ris cmds
32	RW	DISA_RETRY_MODE4RIS: Disable retry mode for ris cmds
33	RW	HANG_ON_ADDR_ERR: Hang when Cresp addr_err received
34:35	RW	EOI_CORRECTION: binary number, that stops accepting eoi cmds earlier that needed (to fix a potential bug)
36:39	RW	MAX_LOAD_COUNT: binary number, that denotes the maximum number of loads allowed to be queued -1
40:43	RW	MAX_STORE_COUNT: binary number, that denotes the maximum number of stores allowed to be queued -1
44	RW	EOI_CREDIT_DD1: DD1 mode for eoi credits see HW240848
45	RW	UNSOL_DATA_DD1: DD1 mode for unsolicited data checker see HW243661
46	RW	US_OW0_WCR_DD1: DD1 mode for unsolicited data checker OW0 see HW246839
47	RW	ENABLE_INJECT: enable interrupt inject via intr_inject_reg

Register Name	<i>ICP Interrupt Inject Register</i>
Mnemonic	EN.TPC.INTP.INTR_INJECT_REG
Address	00000000020109CC (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	INJECT_TARGET_CORE: multy hot selection of core to be target of interrupt inject
16:23	RW	INJECT_TARGET_THREAD: multi hot selection of thread to be target of interrupt inject
24:31	RW	
32:35	RW	INJECT_LEVEL: level to be used for interrupt inject (updates xirr 28:31)
36:39	RW	
40:47	RW	INJECT_PRIORITY: priority to be used for interrupt inject (updated mfr(0:7)
48:63	RO	Constant = 0b0000000000000000

Register Name	<i>ICP Nest FIR Register</i>
Mnemonic	EN.TPC.INTP.SYNC_FIR_REG
Address	00000000020109C0 (SCOM) 00000000020109C1 (SCOM1) 00000000020109C2 (SCOM2)
Attributes	
Description	ICP Nest FIR Register



Registers Specification

POWER8 Processor

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	INT_HW_ERROR_EOI_Q: internal hardware error eoi queue
1	RWX	WOX_AND	WOX_OR	INT_HW_ERROR_FWD_Q: internal hardware error fwd queue
2	RWX	WOX_AND	WOX_OR	INT_HW_ERROR_IR_QU: internal hardware error ir queue
3	RWX	WOX_AND	WOX_OR	INT_HW_ERROR_RET_Q: internal hardware error return queue
4	RWX	WOX_AND	WOX_OR	INT_HW_ERROR_ADDRI: internal hardware error address in
5	RWX	WOX_AND	WOX_OR	INT_HW_ERROR_DATAI: internal hardware error data in
6	RWX	WOX_AND	WOX_OR	INT_HW_ERROR_ADDRO: internal hardware error address out
7	RWX	WOX_AND	WOX_OR	INT_HW_ERROR_DATAO: internal hardware error data out



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
8	RWX	WOX_AND	WOX_OR	INT_HW_ERROR_LDSTQ: internal hardware error load store queue
9	RWX	WOX_AND	WOX_OR	INT_HW_ERROR_REQQ: internal hardware error request queue
10	RWX	WOX_AND	WOX_OR	SCOM_REG_CHECK: parity check withing scom register
11	RWX	WOX_AND	WOX_OR	INVALID_FORWARD_SETUP: invalid forward setup (either loop or invalid core ID)
12	RWX	WOX_AND	WOX_OR	ADDRESS_CORE_FIELD: core field > 11 for inter.req. or fwd.interr
13	RWX	WOX_AND	WOX_OR	ADDRESS_CORE_FIELD_MMIO: core field > 11 for mmio
14	RWX	WOX_AND	WOX_OR	UNSOLICITED_CRESP: unsolicited cresp (master)
15	RWX	WOX_AND	WOX_OR	UNSOLICITED_DATA: unsolicited data (store snooper)
16	RWX	WOX_AND	WOX_OR	INVALID_CMD: unexpected cmd
17	RWX	WOX_AND	WOX_OR	INVALID_CRESPZ: ris_cresp_addr_err_inv_rc cresp address error
18	RWX	WOX_AND	WOX_OR	INVALID_CRESP: ris_cresp_addr_err_inv_rc cresp invalid
19	RWX	WOX_AND	WOX_OR	Reserved field. (Access type is reserved)
20	RWX	WOX_AND	WOX_OR	ECC_CE_ON_DATA: ecc ce off of inbound processor bus
21	RWX	WOX_AND	WOX_OR	ECC_UE_ON_DATA: ecc ue off of inbound processor bus
22	RWX	WOX_AND	WOX_OR	ECC_SUE_ON_DATA: ecc sue off of inbound processor bus
23	RWX	WOX_AND	WOX_OR	PARITY_CHK_ADDRESS: parity error PB address
24	RWX	WOX_AND	WOX_OR	PARITY_CHK_TAG: parity error PB tag
25	RWX	WOX_AND	WOX_OR	TIMEOUT_LD_STQ: (data) timeout load/store (ldstq) queue
26	RWX	WOX_AND	WOX_OR	TIMEOUT_RETURNQ: timeout return interrupt queue
27	RWX	WOX_AND	WOX_OR	TIMEOUT_FWDQ: timeout forward interrupt queue
28	RWX	WOX_AND	WOX_OR	TIMEOUT_LDSTQ: timeout end of interrupt queue
29	RWX	WOX_AND	WOX_OR	TIMEOUT_REQQ: (operational) timeout load/store (ldstq) queue
30	RWX	WOX_AND	WOX_OR	TIMEOUT_EOIQ: timeout interrupt request queue
31	RWX	WOX_AND	WOX_OR	Reserved field. (Access type is reserved_31)
32	RWX	WOX_AND	WOX_OR	EXT_TRACE_0: trace error 0
33	RWX	WOX_AND	WOX_OR	EXT_TRACE_1: trace error 1
34	RWX	WOX_AND	WOX_OR	ADU_RECOV: ADU recoverable error
35	RWX	WOX_AND	WOX_OR	EXT_XSTOP: ADU xstop error
36	RWX	WOX_AND	WOX_OR	Reserved field. (Access type is fir_parity_err2)
37	RWX	WOX_AND	WOX_OR	Reserved field. (Access type is fir_parity_err)
38:63	RO	N/A	N/A	Constant = 0b000000000000000000000000

Register Name	<i>ICP Nest FIR Mask Register</i>
Mnemonic	EN.TPC.INTP.SYNC_FIR_MASK_REG
Address	00000000020109C3 (SCOM) 00000000020109C4 (SCOM1) 00000000020109C5 (SCOM2)
Attributes	
Description	ICP Nest FIR Mask Register

Registers Specification

POWER8 Processor

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	INT_HW_ERROR_EOI_Q_MASK: mask for internal hardware error eoi queue
1	RW	WO_AND	WO_OR	INT_HW_ERROR_FWD_Q_MASK: mask for internal hardware error fwd queue
2	RW	WO_AND	WO_OR	INT_HW_ERROR_IR_QU_MASK: mask for internal hardware error ir queue
3	RW	WO_AND	WO_OR	INT_HW_ERROR_RET_Q_MASK: mask for internal hardware error return queue
4	RW	WO_AND	WO_OR	INT_HW_ERROR_ADDRI_MASK: mask for internal hardware error address in
5	RW	WO_AND	WO_OR	INT_HW_ERROR_DATAI_MASK: mask for internal hardware error data in
6	RW	WO_AND	WO_OR	INT_HW_ERROR_ADDRO_MASK: mask for internal hardware error address out
7	RW	WO_AND	WO_OR	INT_HW_ERROR_DATAO_MASK: mask for internal hardware error data out
8	RW	WO_AND	WO_OR	INT_HW_ERROR_LDSTQ_MASK: mask for internal hardware error load store queue
9	RW	WO_AND	WO_OR	INT_HW_ERROR_REQQ_MASK: mask for internal hardware error request queue
10	RW	WO_AND	WO_OR	SCOM_REG_CHECK_MASK: mask for parity check withing scom register
11	RW	WO_AND	WO_OR	INVAL_FWD_SETUP_MASK: mask for parity check withing scom register
12	RW	WO_AND	WO_OR	ADDRESS_CORE_FIELD_MASK: mask for core field > 11 for inter.req. or fwd.interr
13	RW	WO_AND	WO_OR	ADDRESS_CORE_FIELD_MMIO_MASK: mask for core field > 11 for mmio
14	RW	WO_AND	WO_OR	UNSOLICITED_CRESP_MASK: mask for unsolicited cresp (master)
15	RW	WO_AND	WO_OR	UNSOLICITED_DATA_MASK: mask for unsolicited data (store snoop)
16	RW	WO_AND	WO_OR	INVALID_CMD_MASK: mask for unexpected cmd
17	RW	WO_AND	WO_OR	INVALID_CRESPZ_MASK: mask for ris_cresp_addr_err_inv_rc cresp address error
18	RW	WO_AND	WO_OR	INVALID_CRESP_MASK: mask for ris_cresp_addr_err_inv_rc cresp invalid
19	RW	WO_AND	WO_OR	Reserved field. (Access type is reserved_mask)
20	RW	WO_AND	WO_OR	ECC_CE_ON_DATA_MASK: mask for ecc ce off of inbound processor bus
21	RW	WO_AND	WO_OR	ECC_UE_ON_DATA_MASK: mask for ecc ue off of inbound processor bus
22	RW	WO_AND	WO_OR	ECC_SUE_ON_DATA_MASK: mask for ecc sue off of inbound processor bus
23	RW	WO_AND	WO_OR	PARITY_CHK_ADDRESS_MASK: mask for parity error PB address
24	RW	WO_AND	WO_OR	PARITY_CHK_TAG_MASK: mask for parity error PB tag
25	RW	WO_AND	WO_OR	TIMEOUT_LD_STQ_MASK: mask for timeout load store queue
26	RW	WO_AND	WO_OR	TIMEOUT_RETURNQ_MASK: mask for timeout return queue
27	RW	WO_AND	WO_OR	TIMEOUT_FWDQ_MASK: mask for timeout forward interrupt queue
28	RW	WO_AND	WO_OR	TIMEOUT_EOIQ_MASK: mask for timeout end of interrupt queue
29	RW	WO_AND	WO_OR	Reserved field. (Access type is reserved_29_mask)



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
30	RW	WO_AND	WO_OR	Reserved field. (Access type is reserved_30_mask)
31	RW	WO_AND	WO_OR	Reserved field. (Access type is reserved_31_mask)
32	RW	WO_AND	WO_OR	EXT_TRACE_0_MASK: mask for trace error 0
33	RW	WO_AND	WO_OR	EXT_TRACE_1_MASK: mask for trace error 1
34	RW	WO_AND	WO_OR	ADU_RECOV_MASK: mask for ADU recoverable error
35	RW	WO_AND	WO_OR	EXT_XSTOP_MASK: mask for ADU xstop error
36	RW	WO_AND	WO_OR	Reserved field. (Access type is fir_parity_err2)
37	RW	WO_AND	WO_OR	Reserved field. (Access type is fir_parity_err)
38:63	RO	N/A	N/A	Constant = 0b000000000000000000000000

Register Name	Processor Bus PB WEST Mode Configuration Register
Mnemonic	EH.PB.MISC.PB_WEST_MODE
Address	0000000002010C0A (SCOM)
Attributes	
Description	00 pb_west_pbixxx_init 01:03 spare 04 pb_cfg_west_chip_is_system 05:06 pb_cfg_west_avp_mode(0:1) 07 spare 08 pb_cfg_west_hng_chk_disable 09 pb_cfg_west_dbg_clr_max_hang_stage 10:11 spare 12:15 pb_cfg_west_sw_ab_wait(0:3) 16:21 pb_cfg_west_sp_hw_mark(0:5) 22:27 pb_cfg_west_gp_hw_mark(0:5) 28:33 pb_cfg_west_lcl_hw_mark(0:5) 34:40 pb_cfg_west_e2e_hw_mark(0:6) 41:46 pb_cfg_west_fp_hw_mark(0:5) 47 pb_cfg_west_reset_error_capture 48:58 spare 59 pb_cfg_west_switch_option_ab 60:62 pb_cfg_west_cpu_ratio_override(0:2) 63 reserved

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is pb_west_pbixxx_init)
1:3	RO	Constant = 0b000
4	RWX	PB_CFG_CHIP_IS_SYSTEM: configures whether there are other Processors in the system. ON=>0b111 OFF=>0b000
5:6	RWX	PB_CFG_AVP_MODE: configures command snoop and cresp arbiter for AVP test mode. Disables AHASH checks, tlb checks; 00=AVP disabled, 10=chip AVP, 11=card AVP OFF=>0b000000 CHIP_AVP=>0b101010 CARD_AVP=>0b111111
7	RW	OFF=>0b000000 CHIP_AVP=>0b101010 CARD_AVP=>0b111111
8	RWX	PB_CFG_HNG_CHK_DISABLE: Hang Check Disable. ON=>0b111 OFF=>0b000

Registers Specification

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Bits	SCOM	Field Mnemonic: Description
9	RWX	PB_DBG_CLR_MAX_HANG_STAGE: Resets the maximum hang state level (pb_hang_level) ON=>0b111 OFF=>0b000
10:11	RW	ON=>0b111 OFF=>0b000
12:15	RWX	PB_CFG_SW_AB_WAIT: Adds delay to tc_pb_switch_ab input from TPC during hot plug sequence CNT_0=>0b0000000000000 CNT_1=>0b000100010001 CNT_2=>0b001000100010 CNT_3=>0b001100110011 CNT_4=>0b010001000100 CNT_5=>0b010101010101 CNT_6=>0b011001100110 CNT_7=>0b011101110111 CNT_8=>0b100010001000 CNT_9=>0b100110011001 CNT_10=>0b101010101010 CNT_11=>0b101110111011 CNT_12=>0b110011001100 CNT_13=>0b110111011101 CNT_14=>0b111011101110 CNT_15=>0b111111111111



Bits	SCOM	Field Mnemonic: Description
16:21	RWX	PB_CFG_SP_HW_MARK: Configures the maximum system pumps an I/O unit can issue. CNT_0=>0b00000000000000000000 CNT_1=>0b000001000001000001 CNT_2=>0b000010000010000010 CNT_3=>0b000011000011000011 CNT_4=>0b000100000100000100 CNT_5=>0b000101000101000101 CNT_6=>0b000110000110000110 CNT_7=>0b000111000111000111 CNT_8=>0b001000001000001000 CNT_9=>0b001001001001001001 CNT_10=>0b001010001010001010 CNT_11=>0b001011001011001011 CNT_12=>0b001100001100001100 CNT_13=>0b001101001101001101 CNT_14=>0b001110001110001110 CNT_15=>0b001111001111001111 CNT_16=>0b010000010000010000 CNT_17=>0b010001010001010001 CNT_18=>0b010010010010010010 CNT_19=>0b010011010011010011 CNT_20=>0b010100010100010100 CNT_21=>0b010101010101010101 CNT_22=>0b010110010110010110 CNT_23=>0b010111010111010111 CNT_24=>0b011000011000011000 CNT_25=>0b011001011001011001 CNT_26=>0b011010011010011010 CNT_27=>0b011011011011011011 CNT_28=>0b011100011100011100 CNT_29=>0b011101011101011101 CNT_30=>0b011110011110011110 CNT_31=>0b011111011111011111 CNT_32=>0b100000100000100000

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
22:27	RWX	PB_CFG_GP_HW_MARK: configures the maximum group pumps this chip may issue CNT_0=>0b000000000000000000 CNT_1=>0b000001000001000001 CNT_2=>0b000010000010000010 CNT_3=>0b000011000011000011 CNT_4=>0b000100000100000100 CNT_5=>0b000101000101000101 CNT_6=>0b000110000110000110 CNT_7=>0b000111000111000111 CNT_8=>0b001000001000001000 CNT_9=>0b001001001001001001 CNT_10=>0b001010001010001010 CNT_11=>0b001011001011001011 CNT_12=>0b001100001100001100 CNT_13=>0b001101001101001101 CNT_14=>0b001110001110001110 CNT_15=>0b001111001111001111 CNT_16=>0b010000010000010000 CNT_17=>0b010001010001010001 CNT_18=>0b010010010010010010 CNT_19=>0b010011010011010011 CNT_20=>0b010100010100010100 CNT_21=>0b010101010101010101 CNT_22=>0b010110010110010110 CNT_23=>0b010111010111010111 CNT_24=>0b011000011000011000 CNT_25=>0b011001011001011001 CNT_26=>0b011010011010011010 CNT_27=>0b011011011011011011 CNT_28=>0b011100011100011100 CNT_29=>0b011101011101011101 CNT_30=>0b011110011110011110 CNT_31=>0b011111011111011111 CNT_32=>0b100000100000100000



Bits	SCOM	Field Mnemonic: Description
28:33	RWX	PB_CFG_LCL_HW_MARK: configures the maximum local pumps this chip may issue CNT_0=>0b00000000000000000000 CNT_1=>0b0000001000001000001 CNT_2=>0b0000010000010000010 CNT_3=>0b0000011000011000011 CNT_4=>0b0000100000100000100 CNT_5=>0b0000101000101000101 CNT_6=>0b0000110000110000110 CNT_7=>0b0000111000111000111 CNT_8=>0b0001000001000001000 CNT_9=>0b0001001001001001001 CNT_10=>0b0001010001010001010 CNT_11=>0b0001011001011001011 CNT_12=>0b0001100001100001100 CNT_13=>0b0001101001101001101 CNT_14=>0b0001110001110001110 CNT_15=>0b0001111001111001111 CNT_16=>0b010000010000010000 CNT_17=>0b0100001010001010001 CNT_18=>0b0100100100100100100 CNT_19=>0b010011010011010011 CNT_20=>0b010100010100010100 CNT_21=>0b010101010101010101 CNT_22=>0b010110010110010110 CNT_23=>0b010111010111010111 CNT_24=>0b011000011000011000 CNT_25=>0b011001011001011001 CNT_26=>0b011010011010011010 CNT_27=>0b011011011011011011 CNT_28=>0b011100011100011100 CNT_29=>0b011101011101011101 CNT_30=>0b011110011110011110 CNT_31=>0b011111011111011111 CNT_32=>0b100000100000100000

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
34:40	RWX	PB_CFG_E2E_HW_MARK: configures the maximum local pumps this chip may issue CNT_0=>0b000000000000000000000000 CNT_1=>0b000000010000000100000001 CNT_2=>0b000000100000001000000010 CNT_3=>0b000000110000001100000011 CNT_4=>0b000001000000010000000100 CNT_5=>0b000001010000010100000101 CNT_6=>0b000001100000011000000110 CNT_7=>0b000001110000011100000111 CNT_8=>0b000010000000100000001000 CNT_9=>0b000010010000100100001001 CNT_10=>0b00001010000010100001010 CNT_11=>0b000010110000101100001011 CNT_12=>0b000011000000110000001100 CNT_13=>0b000011010000110100001101 CNT_14=>0b000011100000111000001110 CNT_15=>0b000011110000111100001111 CNT_16=>0b0010000000100000010000 CNT_17=>0b00100001001000010010001 CNT_18=>0b0010001000100100010010 CNT_19=>0b0010001100100110010011 CNT_20=>0b00100100000101000010100 CNT_21=>0b00100101000101010010101 CNT_22=>0b00100110000101100010110 CNT_23=>0b00100111000101110010111 CNT_24=>0b00110000001100000011000 CNT_25=>0b0011001000110010011001 CNT_26=>0b00110100001101000011010 CNT_27=>0b00110110001101100011011 CNT_28=>0b00111000001110000011100 CNT_29=>0b00111010001110100011101 CNT_30=>0b00111100001111000011110 CNT_31=>0b00111110001111100011111 CNT_32=>0b0100000010000001000000 CNT_33=>0b0100001010000101000001 CNT_34=>0b01000010010000100100010 CNT_35=>0b01000011010000110100001 CNT_36=>0b0100100010010000100100100 CNT_37=>0b01001010100101010100101 CNT_38=>0b01001100100110010010110 CNT_39=>0b01001110100111010011111 CNT_40=>0b01010000010100000101000 CNT_41=>0b01010001010100010101001 CNT_42=>0b010101000101010010101010 CNT_43=>0b01010110101010110101011 CNT_44=>0b01011000010110000101100 CNT_45=>0b010110100101101010101101 CNT_46=>0b01011100010111001011110 CNT_47=>0b01011110010111101011111 CNT_48=>0b0110000011000000110000 CNT_49=>0b01100001011000010110001 CNT_50=>0b011001000110010011001010 CNT_51=>0b01100110011001101100111 CNT_52=>0b01101000011010000110100 CNT_53=>0b01101010011010101010101 CNT_54=>0b01101100011011001011010 CNT_55=>0b01101110011011101011011 CNT_56=>0b01110000011100000111000 CNT_57=>0b0111001001110010111001 CNT_58=>0b01110100011101001110101



Bits	SCOM	Field Mnemonic: Description
41:46	RWX	PB_CFG_FP_HW_MARK: configures the maximum foreign pumps this chip may issue CNT_0=>0b000000000000000000 CNT_1=>0b000001000001000001 CNT_2=>0b000010000010000010 CNT_3=>0b000011000011000011 CNT_4=>0b000100000100000100 CNT_5=>0b000101000101000101 CNT_6=>0b000110000110000110 CNT_7=>0b000111000111000111 CNT_8=>0b001000001000001000 CNT_9=>0b001001001001001001 CNT_10=>0b001010001010001010 CNT_11=>0b001011001011001011 CNT_12=>0b001100001100001100 CNT_13=>0b001101001101001101 CNT_14=>0b001110001110001110 CNT_15=>0b001111001111001111 CNT_16=>0b010000010000010000 CNT_17=>0b010001010001010001 CNT_18=>0b010010010010010010 CNT_19=>0b010011010011010011 CNT_20=>0b010100010100010100 CNT_21=>0b010101010101010101 CNT_22=>0b010110010110010110 CNT_23=>0b010111010111010111 CNT_24=>0b011000011000011000 CNT_25=>0b011001011001011001 CNT_26=>0b011010011010011010 CNT_27=>0b011011011011011011 CNT_28=>0b011100011100011100 CNT_29=>0b011101011101011101 CNT_30=>0b011110011110011110 CNT_31=>0b011111011111011111 CNT_32=>0b100000100000100000

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
47	RWX	Reserved field. (Access type is pb_cfg_west_reset_error_capture) CNT_0=>0b00000000000000000000 CNT_1=>0b00000010000010000001 CNT_2=>0b000010000010000010 CNT_3=>0b000011000011000011 CNT_4=>0b0000100000100000100 CNT_5=>0b0000101000101000101 CNT_6=>0b0000110000110000110 CNT_7=>0b0000111000111000111 CNT_8=>0b001000001000001000 CNT_9=>0b001001001001001001 CNT_10=>0b001010001010001010 CNT_11=>0b001011001011001011 CNT_12=>0b001100001100001100 CNT_13=>0b001101001101001101 CNT_14=>0b001110001110001110 CNT_15=>0b001111001111001111 CNT_16=>0b010000010000010000 CNT_17=>0b010001010001010001 CNT_18=>0b010010010010010010 CNT_19=>0b010011010011010011 CNT_20=>0b010100010100010100 CNT_21=>0b010101010101010101 CNT_22=>0b010110010110010110 CNT_23=>0b010111010111010111 CNT_24=>0b011000011000011000 CNT_25=>0b011001011001011001 CNT_26=>0b011010011010011010 CNT_27=>0b011011011011011011 CNT_28=>0b011100011100011100 CNT_29=>0b011101011101011101 CNT_30=>0b011110011110011110 CNT_31=>0b011111011111011111 CNT_32=>0b100000100000100000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	CNT_0=>0b000000000000000000 CNT_1=>0b0000001000001000001 CNT_2=>0b0000010000010000010 CNT_3=>0b0000011000011000011 CNT_4=>0b0000100000100000100 CNT_5=>0b0000101000101000101 CNT_6=>0b0000110000110000110 CNT_7=>0b0000111000111000111 CNT_8=>0b0001000001000001000 CNT_9=>0b0001001001001001001 CNT_10=>0b0001010001010001010 CNT_11=>0b0001011001011001011 CNT_12=>0b0001100001100001100 CNT_13=>0b0001101001101001101 CNT_14=>0b0001110001110001110 CNT_15=>0b0001111001111001111 CNT_16=>0b0100000100000100000 CNT_17=>0b010001010001010001 CNT_18=>0b010010010010010010 CNT_19=>0b010011010011010011 CNT_20=>0b010100010100010100 CNT_21=>0b010101010101010101 CNT_22=>0b010110010110010110 CNT_23=>0b010111010111010111 CNT_24=>0b011000011000011000 CNT_25=>0b011001011001011001 CNT_26=>0b011010011010011010 CNT_27=>0b011011011011011011 CNT_28=>0b011100011100011100 CNT_29=>0b011101011101011101 CNT_30=>0b011110011110011110 CNT_31=>0b011111011111011111 CNT_32=>0b100000100000100000
58	RW	PB_CFG_SWITCH_CD_PULSE: Controls switch_cd pulse width. Uses pb_cfg_sw_ab_wait to extend pulse. Default=long pulse. Requires pb_cfg_sw_ab_wait > cnt_5 for 6 cycle pulse. SHORT=>0b111 LONG=>0b000
59	RWX	PB_CFG_SWITCH_OPTION_AB: SCOM access to determine what signal drives pb_cfg_switch_cd. on=tc_pb_switch_ab, off=tc_pb_switch_cd. ON=>0b111 OFF=>0b000
60:62	RWX	PB_CFG_CPU_RATIO_OVERRIDE: Sets rcmd high water mark. 000=16:max hw, 001=12:75% hw, 01x=8:50% hw, 1xx=4:25% hw LVL_0=>0b000000000 LVL_1=>0b001001001 LVL_2=>0b010010010 LVL_3=>0b011011011 LVL_4=>0b100100100 LVL_5=>0b101101101 LVL_6=>0b110110110 LVL_7=>0b111111111

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
63	RW	LVL_0=>0b000000000 LVL_1=>0b001001001 LVL_2=>0b010010010 LVL_3=>0b011011011 LVL_4=>0b100100100 LVL_5=>0b101101101 LVL_6=>0b110110110 LVL_7=>0b111111111

Register Name	Processor Bus PB WEST HP Mode Configuration Register
Mnemonic	EH.PB.MISC.PB_WEST_HP_MODE_NEXT
Address	0000000002010C0B (SCOM)
Attributes	
Description	00 pb_cfg_west_master_chip 01 pb_cfg_west_link_a0_en 02 pb_cfg_west_link_a1_en 03 pb_cfg_west_link_a2_en 04 pb_cfg_west_na0_addr_dis 05 pb_cfg_west_na1_addr_dis 06 pb_cfg_west_na2_addr_dis 07:09 pb_cfg_west_link_a0_nodeid(0:2) 10:12 pb_cfg_west_link_a1_nodeid(0:2) 13:15 pb_cfg_west_link_a2_nodeid(0:2) 16 pb_cfg_west_a_aggregate 17 pb_cfg_west_tm_grp_master 18 pb_cfg_west_chg_rate_gp_master 19 pb_cfg_west_chg_rate_sp_master 20 pb_cfg_west_pump_mode 21 pb_cfg_west_single_mc 22:23 spare 24:31 pb_cfg_west_a_cmd_rate(0:7) 32 pb_cfg_west_a_gather_enable 33:37 pb_cfg_west_a_dly_cnt(0:4) 38 pb_cfg_west_p0_x8tok 39 pb_cfg_west_p2_x8tok 40 pb_cfg_west_req_gather_enable 41 spare 42 pb_cfg_west_f0_link_master 43 pb_cfg_west_f1_link_master 44 pb_cfg_west_link_f0_en 45 pb_cfg_west_link_f1_en 46 pb_cfg_west_nf0_addr_dis 47 pb_cfg_west_nf1_addr_dis 48:50 pb_cfg_west_link_f0_nodeid(0:2) 51:53 pb_cfg_west_link_f1_nodeid(0:2) 54 spare 55 pb_cfg_west_f_aggregate 56:63 pb_cfg_west_f_cmd_rate(0:7)

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_MASTER_CHIP_NEXT: Processor bus master. ON=>0b111 OFF=>0b000
1	RWX	PB_CFG_LINK_A0_EN_NEXT: Link A0 enabled. ON=>0b111 OFF=>0b000
2	RWX	PB_CFG_LINK_A1_EN_NEXT: Link A1 enabled. ON=>0b111 OFF=>0b000
3	RWX	PB_CFG_LINK_A2_EN_NEXT: Link A2 enabled. ON=>0b111 OFF=>0b000
4	RWX	PB_CFG_LINK_NA0_ADDR_DIS_NEXT: Link A0 address broadcast disabled ON=>0b111 OFF=>0b000
5	RWX	PB_CFG_LINK_NA1_ADDR_DIS_NEXT: Link A1 address broadcast disabled ON=>0b111 OFF=>0b000

Bits	SCOM	Field Mnemonic: Description
6	RWX	PB_CFG_LINK_NA2_ADDR_DIS_NEXT: Link A2 address broadcast disabled ON=>0b111 OFF=>0b000
7:9	RWX	PB_CFG_LINK_A0_NODEID_NEXT: Node ID of chip connected to A0 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
10:12	RWX	PB_CFG_LINK_A1_NODEID_NEXT: Node ID of chip connected to A1 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
13:15	RWX	PB_CFG_LINK_A2_NODEID_NEXT: Node ID of chip connected to A2 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
16	RWX	PB_CFG_A_AGGREGATE_NEXT: Processor bus A links are configured as parallel buses to same chip. ON=>0b111 OFF=>0b000
17	RWX	PB_CFG_TM_MASTER_NEXT: configure Chip as PB TM Master. ON=>0b111 OFF=>0b000
18	RWX	PB_CFG_CHG_RATE_GP_MASTER_NEXT: Sets the Group pump change rate master. This master gathers all GP chg_rate.reqs and issues a chg_rate.gnt ON=>0b111 OFF=>0b000
19	RWX	PB_CFG_CHG_RATE_SP_MASTER_NEXT: Sets the System pump change rate master. This master gathers all SP chg_rate.reqs and issues a chg_rate.gnt ON=>0b111 OFF=>0b000

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
20	RWX	PB_CFG_PUMP_MODE_NEXT: configures whether there are other Processors in the system and if they are part of this node NODAL_IS_CHIP_GROUP_IS_GROUP=>0b000 NODAL_AND_GROUP_IS_GROUP=>0b111
21	RWX	PB_CFG_SINGLE_MC_NEXT: Enables Single MC mode. ON=>0b111 OFF=>0b000
22	RW	PB_CFG_DCACHE_CAPP_MODE_NEXT: Dcache CAPP mode. Combines MC/L4 dcache codepoint for Beyond5Chip locality. ON=>0b111 OFF=>0b000
23	RW	 ON=>0b111 OFF=>0b000
24:31	RWX	PB_CFG_A_CMD_RATE_WEST_NEXT: configures the paced command rate to not overrun the A link
32	RWX	PB_CFG_A_GATHER_ENABLE_NEXT: Enable Data OW gathering on A links. ON=>0b111 OFF=>0b000
33:37	RWX	Reserved field. (Access type is pb_cfg_west_a_dly_cnt) ON=>0b111 OFF=>0b000
38	RWX	PB_CFG_P0_X8TOK_NEXT: Configures PHB0 as an 8 token data ramp. 0=PHB0/F0:4OW, 1=P0:8OW and F0:0OW ON=>0b111 OFF=>0b000
39	RWX	PB_CFG_P2_X8TOK_NEXT: Configures PHB2 as an 8 token data ramp. 0=PHB2/F1:4OW, 1=P2:8OW and F1:0OW ON=>0b111 OFF=>0b000
40	RWX	PB_CFG_REQ_GATHER_ENABLE_NEXT: Enable Data OW gathering on all chiplet/link requests. ON=>0b111 OFF=>0b000
41	RW	 ON=>0b111 OFF=>0b000
42	RWX	PB_CFG_F0_LINK_MASTER_EN_NEXT: Link f0 command master enabled. ON=>0b111 OFF=>0b000
43	RWX	PB_CFG_F1_LINK_MASTER_EN_NEXT: Link f1 command master enabled. ON=>0b111 OFF=>0b000

Bits	SCOM	Field Mnemonic: Description
44	RWX	PB_CFG_LINK_F0_EN_NEXT: Link f0 enabled. ON=>0b111 OFF=>0b000
45	RWX	PB_CFG_LINK_F1_EN_NEXT: Link f1 enabled. ON=>0b111 OFF=>0b000
46	RWX	PB_CFG_LINK_F0_ADDR_DIS_NEXT: Link f0 address broadcast disabled ON=>0b111 OFF=>0b000
47	RWX	PB_CFG_LINK_F1_ADDR_DIS_NEXT: Link f1 address broadcast disabled ON=>0b111 OFF=>0b000
48:50	RWX	PB_CFG_LINK_F0_NODEID_NEXT: Node ID of chip connected to f0 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
51:53	RWX	PB_CFG_LINK_F1_NODEID_NEXT: Node ID of chip connected to f1 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
54	RW	 ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
55	RWX	PB_CFG_F_AGGREGATE_NEXT: Processor bus F links are configured as parallel buses to same chip. ON=>0b111 OFF=>0b000
56:63	RWX	PB_CFG_F_CMD_RATE_WEST_NEXT: configures the paced command rate to not overrun the F link

Registers Specification

POWER8 Processor

Register Name		Processor Bus PB WEST HP Mode Configuration Register
Mnemonic		EH.PB.MISC.PB_WEST_HP_MODE_CURR
Address		0000000002010C0C (SCOM)
Attributes		
Description		00 pb_cfg_west_master_chip 01 pb_cfg_west_link_a0_en 02 pb_cfg_west_link_a1_en 03 pb_cfg_west_link_a2_en 04 pb_cfg_west_na0_addr_dis 05 pb_cfg_west_na1_addr_dis 06 pb_cfg_west_na2_addr_dis 07:09 pb_cfg_west_link_a0_nodeid(0:2) 10:12 pb_cfg_west_link_a1_nodeid(0:2) 13:15 pb_cfg_west_link_a2_nodeid(0:2) 16 pb_cfg_west_a_aggregate 17 pb_cfg_west_tm_grp_master 18 pb_cfg_west_chg_rate_gp_master 19 pb_cfg_west_chg_rate_sp_master 20 pb_cfg_west_pump_mode 21 pb_cfg_west_single_mc 22:23 spare 24:31 pb_cfg_west_a_cmd_rate(0:7) 32 pb_cfg_west_a_gather_enable 33:37 pb_cfg_west_a_dly_cnt(0:4) 38 pb_cfg_west_p0_x8tok 39 pb_cfg_west_p2_x8tok 40 pb_cfg_west_req_gather_enable 41 spare 42 pb_cfg_west_f0_link_master 43 pb_cfg_west_f1_link_master 44 pb_cfg_west_link_f0_en 45 pb_cfg_west_link_f1_en 46 pb_cfg_west_nf0_addr_dis 47 pb_cfg_west_nf1_addr_dis 48:50 pb_cfg_west_link_f0_nodeid(0:2) 51:53 pb_cfg_west_link_f1_nodeid(0:2) 54 spare 55 pb_cfg_west_f_aggregate 56:63 pb_cfg_west_f_cmd_rate(0:7)
Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_MASTER_CHIP_CURR: Processor bus master. ON=>0b111 OFF=>0b000
1	RWX	PB_CFG_LINK_A0_EN_CURR: Link A0 enabled. ON=>0b111 OFF=>0b000
2	RWX	PB_CFG_LINK_A1_EN_CURR: Link A1 enabled. ON=>0b111 OFF=>0b000
3	RWX	PB_CFG_LINK_A2_EN_CURR: Link A2 enabled. ON=>0b111 OFF=>0b000
4	RWX	PB_CFG_LINK_NA0_ADDR_DIS_CURR: Link A0 address broadcast disabled ON=>0b111 OFF=>0b000
5	RWX	PB_CFG_LINK_NA1_ADDR_DIS_CURR: Link A1 address broadcast disabled ON=>0b111 OFF=>0b000
6	RWX	PB_CFG_LINK_NA2_ADDR_DIS_CURR: Link A2 address broadcast disabled ON=>0b111 OFF=>0b000

Bits	SCOM	Field Mnemonic: Description
7:9	RWX	PB_CFG_LINK_A0_NODEID_CURR: Node ID of chip connected to A0 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
10:12	RWX	PB_CFG_LINK_A1_NODEID_CURR: Node ID of chip connected to A1 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
13:15	RWX	PB_CFG_LINK_A2_NODEID_CURR: Node ID of chip connected to A2 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
16	RWX	PB_CFG_A_AGGREGATE_CURR: Processor bus A links are configured as parallel buses to same chip. ON=>0b111 OFF=>0b000
17	RWX	PB_CFG_TM_MASTER_CURR: Configure chip as PB TM Master. ON=>0b111 OFF=>0b000
18	RWX	PB_CFG_CHG_RATE_GP_MASTER_CURR: Sets the Group pump change rate master. This master gathers all GP chg_rate.reqs and issues a chg_rate.gnt ON=>0b111 OFF=>0b000
19	RWX	PB_CFG_CHG_RATE_SP_MASTER_CURR: Sets the system pump change rate master. This master gathers all SP chg_rate.reqs and issues a chg_rate.gnt ON=>0b111 OFF=>0b000

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
20	RWX	PB_CFG_PUMP_MODE_CURR: configures whether there are other Processors in the system and if they are part of this node NODAL_IS_CHIP_GROUP_IS_GROUP=>0b000 NODAL_AND_GROUP_IS_GROUP=>0b111
21	RWX	PB_CFG_SINGLE_MC_CURR: Enables Single MC mode. ON=>0b111 OFF=>0b000
22	RW	PB_CFG_DCACHE_CAPP_MODE_CURR: Dcache CAPP mode. Combines MC/L4 dcache codepoint for Beyond5Chip locality. ON=>0b111 OFF=>0b000
23	RW	ON=>0b111 OFF=>0b000
24:31	RWX	PB_CFG_A_CMD_RATE_WEST_CURR: configures the paced command rate to not overrun the A link
32	RWX	PB_CFG_A_GATHER_ENABLE_CURR: Enable Data OW gathering on A links. ON=>0b111 OFF=>0b000
33:37	RWX	Reserved field. (Access type is pb_cfg_west_a_dly_cnt) ON=>0b111 OFF=>0b000
38	RWX	PB_CFG_P0_X8TOK_CURR: Configures PHB0 as an 8 token data ramp. 0=PHB0/F0:4OW, 1=P0:8OW and F0:0OW ON=>0b111 OFF=>0b000
39	RWX	PB_CFG_P2_X8TOK_CURR: Configures PHB2 as an 8 token data ramp. 0=PHB2/F1:4OW, 1=P2:8OW and F1:0OW ON=>0b111 OFF=>0b000
40	RWX	PB_CFG_REQ_GATHER_ENABLE_CURR: Enable Data OW gathering on all chiplet/link requests. ON=>0b111 OFF=>0b000
41	RW	ON=>0b111 OFF=>0b000



Bits	SCOM	Field Mnemonic: Description
42	RWX	PB_CFG_F0_LINK_MASTER_EN_CURR: Link f0 command master enabled. ON=>0b111 OFF=>0b000
43	RWX	PB_CFG_F1_LINK_MASTER_EN_CURR: Link f1 command master enabled. ON=>0b111 OFF=>0b000
44	RWX	PB_CFG_LINK_F0_EN_CURR: Link f0 enabled. ON=>0b111 OFF=>0b000
45	RWX	PB_CFG_LINK_F1_EN_CURR: Link f1 enabled. ON=>0b111 OFF=>0b000
46	RWX	PB_CFG_LINK_NF0_ADDR_DIS_CURR: Link f0 address broadcast disabled ON=>0b111 OFF=>0b000
47	RWX	PB_CFG_LINK_NF1_ADDR_DIS_CURR: Link f1 address broadcast disabled ON=>0b111 OFF=>0b000
48:50	RWX	PB_CFG_LINK_F0_NODEID_CURR: Node ID of chip connected to f0 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
51:53	RWX	PB_CFG_LINK_F1_NODEID_CURR: Node ID of chip connected to f1 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
54	RW	ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
55	RWX	PB_CFG_F_AGGREGATE_CURR: Processor bus F links are configured as parallel buses to same chip. ON=>0b111 OFF=>0b000
56:63	RWX	PB_CFG_F_CMD_RATE_WEST_CURR: configures the paced command rate to not overrun the F link

Register Name	Processor Bus PB WEST HP Mode Configuration Register
Mnemonic	EH.PB.MISC.PB_WEST_HPX_MODE_NEXT
Address	0000000002010C0D (SCOM)
Attributes	
Description	00 pb_cfg_west_link_x0_en 01 pb_cfg_west_link_x1_en 02 pb_cfg_west_link_x2_en 03 pb_cfg_west_link_x3_en 04 spare 05 pb_cfg_west_nx0_addr_dis 06 pb_cfg_west_nx1_addr_dis 07 pb_cfg_west_nx2_addr_dis 08 pb_cfg_west_nx3_addr_dis 09 spare 10:12 pb_cfg_west_link_x0_chipid(0:2) 13:15 pb_cfg_west_link_x1_chipid(0:2) 16:18 pb_cfg_west_link_x2_chipid(0:2) 19:21 pb_cfg_west_link_x3_chipid(0:2) 22:24 spare 25 pb_cfg_west_x_aggregate 26 pb_cfg_west_x_indirect_en 27 pb_cfg_west_x_fp_disabled 28:31 spare 32 pb_cfg_west_x_gather_enable 33:37 pb_cfg_west_x_dly_cnt(0:4) 38 pb_cfg_west_x_onnode_12ques 39 spare 40 pb_cfg_west_a0_ind_a1_en 41 pb_cfg_west_a0_ind_a2_en 42 pb_cfg_west_a1_ind_a0_en 43 pb_cfg_west_a1_ind_a2_en 44 pb_cfg_west_a2_ind_a0_en 45 pb_cfg_west_a2_ind_a1_en 46:55 spare 56:63 pb_cfg_west_x_cmd_rate(0:7)

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_LINK_X0_EN_NEXT: Link X0 enabled. ON=>0b111 OFF=>0b000
1	RWX	PB_CFG_LINK_X1_EN_NEXT: Link X1 enabled. ON=>0b111 OFF=>0b000
2	RWX	PB_CFG_LINK_X2_EN_NEXT: Link X2 enabled. ON=>0b111 OFF=>0b000
3	RWX	PB_CFG_LINK_X3_EN_NEXT: Link X3 enabled. ON=>0b111 OFF=>0b000



Bits	SCOM	Field Mnemonic: Description
4	RW	ON=>0b111 OFF=>0b000
5	RWX	PB_CFG_LINK_NX0_ADDR_DIS_NEXT: Link X0 address broadcast disabled ON=>0b111 OFF=>0b000
6	RWX	PB_CFG_LINK_NX1_ADDR_DIS_NEXT: Link X1 address broadcast disabled ON=>0b111 OFF=>0b000
7	RWX	PB_CFG_LINK_NX2_ADDR_DIS_NEXT: Link X2 address broadcast disabled ON=>0b111 OFF=>0b000
8	RWX	PB_CFG_LINK_NX3_ADDR_DIS_NEXT: Link X3 address broadcast disabled ON=>0b111 OFF=>0b000
9	RW	ON=>0b111 OFF=>0b000
10:12	RWX	PB_CFG_LINK_X0_CHIPID_NEXT: Chip ID of chip connected to X0 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
13:15	RWX	PB_CFG_LINK_X1_CHIPID_NEXT: Chip ID of chip connected to X1 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
16:18	RWX	PB_CFG_LINK_X2_CHIPID_NEXT: Chip ID of chip connected to X2 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
19:21	RWX	PB_CFG_LINK_X3_CHIPID_NEXT: Chip ID of chip connected to X3 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
22:24	RW	ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
25	RWX	PB_CFG_X_AGGREGATE_NEXT: Processor bus X links are configured as parallel buses to same chip. ON=>0b111 OFF=>0b000
26	RWX	PB_CFG_X_INDIRECT_EN_NEXT: Processor bus X links are configured for indirect data routing. ON=>0b111 OFF=>0b000
27	RWX	PB_CFG_X_FP_DISABLED_NEXT: Processor bus X link rtag fastpath disable. ON=>0b111 OFF=>0b000
28:31	RW	ON=>0b111 OFF=>0b000
32	RWX	PB_CFG_X_GATHER_ENABLE_NEXT: Enable Data OW gathering on X links. ON=>0b111 OFF=>0b000



Bits	SCOM	Field Mnemonic: Description
33:37	RWX	Reserved field. (Access type is pb_cfg_west_x_dly_cnt) ON=>0b111 OFF=>0b000
38	RWX	PB_CFG_X_ONNODE_12QUES_NEXT: Configures X on group queue depth to 12 OW. 1=12on/4off. 0=8on/8off. ON=>0b111 OFF=>0b000
39	RW	 ON=>0b111 OFF=>0b000
40	RWX	PB_CFG_A0_IND_A1_EN_NEXT: Enable Indirect Data routing on secondary A1 link. A0 is primary. ON=>0b111 OFF=>0b000
41	RWX	PB_CFG_A0_IND_A2_EN_NEXT: Enable Indirect Data routing on secondary A2 link. A0 is primary. ON=>0b111 OFF=>0b000
42	RWX	PB_CFG_A1_IND_A0_EN_NEXT: Enable Indirect Data routing on secondary A0 link. A1 is primary. ON=>0b111 OFF=>0b000
43	RWX	PB_CFG_A1_IND_A2_EN_NEXT: Enable Indirect Data routing on secondary A2 link. A1 is primary. ON=>0b111 OFF=>0b000
44	RWX	PB_CFG_A2_IND_A0_EN_NEXT: Enable Indirect Data routing on secondary A0 link. A2 is primary. ON=>0b111 OFF=>0b000
45	RWX	PB_CFG_A2_IND_A1_EN_NEXT: Enable Indirect Data routing on secondary A1 link. A2 is primary. ON=>0b111 OFF=>0b000
46:55	RW	 ON=>0b111 OFF=>0b000
56:63	RWX	PB_CFG_X_CMD_RATE_WEST_NEXT: configures the paced command rate to not overrun the X link

Registers Specification

POWER8 Processor

Register Name	Processor Bus PB WEST HP Mode Configuration Register
Mnemonic	EH.PB.MISC.PB_WEST_HPX_MODE_CURR
Address	0000000002010C0E (SCOM)
Attributes	
Description	00 pb_cfg_west_link_x0_en 01 pb_cfg_west_link_x1_en 02 pb_cfg_west_link_x2_en 03 pb_cfg_west_link_x3_en 04 spare 05 pb_cfg_west_nx0_addr_dis 06 pb_cfg_west_nx1_addr_dis 07 pb_cfg_west_nx2_addr_dis 08 pb_cfg_west_nx3_addr_dis 09 spare 10:12 pb_cfg_west_link_x0_chipid(0:2) 13:15 pb_cfg_west_link_x1_chipid(0:2) 16:18 pb_cfg_west_link_x2_chipid(0:2) 19:21 pb_cfg_west_link_x3_chipid(0:2) 22:24 spare 25 pb_cfg_west_x_aggregate 26 pb_cfg_west_x_indirect_en 27 pb_cfg_west_x_fp_disabled 28:31 spare 32 pb_cfg_west_x_gather_enable 33:37 pb_cfg_west_x_dly_cnt(0:4) 38 pb_cfg_west_x_onnode_12ques 39 spare 40 pb_cfg_west_a0_ind_a1_en 41 pb_cfg_west_a0_ind_a2_en 42 pb_cfg_west_a1_ind_a0_en 43 pb_cfg_west_a1_ind_a2_en 44 pb_cfg_west_a2_ind_a0_en 45 pb_cfg_west_a2_ind_a1_en 46:55 spare 56:63 pb_cfg_west_x_cmd_rate(0:7)

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_LINK_X0_EN_CURR: Link X0 enabled. ON=>0b111 OFF=>0b000
1	RWX	PB_CFG_LINK_X1_EN_CURR: Link X1 enabled. ON=>0b111 OFF=>0b000
2	RWX	PB_CFG_LINK_X2_EN_CURR: Link X2 enabled. ON=>0b111 OFF=>0b000
3	RWX	PB_CFG_LINK_X3_EN_CURR: Link X3 enabled. ON=>0b111 OFF=>0b000
4	RW	ON=>0b111 OFF=>0b000
5	RWX	PB_CFG_LINK_NX0_ADDR_DIS_CURR: Link X0 address broadcast disabled ON=>0b111 OFF=>0b000
6	RWX	PB_CFG_LINK_NX1_ADDR_DIS_CURR: Link X1 address broadcast disabled ON=>0b111 OFF=>0b000
7	RWX	PB_CFG_LINK_NX2_ADDR_DIS_CURR: Link X2 address broadcast disabled ON=>0b111 OFF=>0b000



Bits	SCOM	Field Mnemonic: Description
8	RWX	PB_CFG_LINK_NX3_ADDR_DIS_CURR: Link X3 address broadcast disabled ON=>0b111 OFF=>0b000
9	RW	ON=>0b111 OFF=>0b000
10:12	RWX	PB_CFG_LINK_X0_CHIPID_CURR: Chip ID of chip connected to X0 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
13:15	RWX	PB_CFG_LINK_X1_CHIPID_CURR: Chip ID of chip connected to X1 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
16:18	RWX	PB_CFG_LINK_X2_CHIPID_CURR: Chip ID of chip connected to X2 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
19:21	RWX	PB_CFG_LINK_X3_CHIPID_CURR: Chip ID of chip connected to X3 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
22:24	RW	ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
25	RWX	PB_CFG_X_AGGREGATE_CURR: Processor bus X links are configured as parallel buses to same chip. ON=>0b111 OFF=>0b000
26	RWX	PB_CFG_X_INDIRECT_EN_CURR: Processor bus X links are configured for indirect data routing. ON=>0b111 OFF=>0b000
27	RWX	PB_CFG_X_FP_DISABLED_CURR: Processor bus X link rtag fastpath disable. ON=>0b111 OFF=>0b000
28:31	RW	ON=>0b111 OFF=>0b000
32	RWX	PB_CFG_X_GATHER_ENABLE_CURR: Enable Data OW gathering on X links. ON=>0b111 OFF=>0b000
33:37	RWX	Reserved field. (Access type is pb_cfg_west_x_dly_cnt) ON=>0b111 OFF=>0b000
38	RWX	PB_CFG_X_ONNODE_12QUES_CURR: Configures X on group queue depth to 12 OW. 1=12on/4off. 0=8on/8off. ON=>0b111 OFF=>0b000
39	RW	ON=>0b111 OFF=>0b000
40	RWX	PB_CFG_A0_IND_A1_EN_CURR: Enable Indirect Data routing on secondary A1 link. A0 is primary. ON=>0b111 OFF=>0b000
41	RWX	PB_CFG_A0_IND_A2_EN_CURR: Enable Indirect Data routing on secondary A2 link. A0 is primary. ON=>0b111 OFF=>0b000



Bits	SCOM	Field Mnemonic: Description
42	RWX	PB_CFG_A1_IND_A0_EN_CURR: Enable Indirect Data routing on secondary A0 link. A1 is primary. ON=>0b111 OFF=>0b000
43	RWX	PB_CFG_A1_IND_A2_EN_CURR: Enable Indirect Data routing on secondary A2 link. A1 is primary. ON=>0b111 OFF=>0b000
44	RWX	PB_CFG_A2_IND_A0_EN_CURR: Enable Indirect Data routing on secondary A0 link. A2 is primary. ON=>0b111 OFF=>0b000
45	RWX	PB_CFG_A2_IND_A1_EN_CURR: Enable Indirect Data routing on secondary A1 link. A2 is primary. ON=>0b111 OFF=>0b000
46:55	RW	ON=>0b111 OFF=>0b000
56:63	RWX	PB_CFG_X_CMD_RATE_WEST_CURR: configures the paced command rate to not overrun the X link

Register Name	<i>Processor Bus PB WEST FLMCFG0 Register</i>
Mnemonic	EH.PB.MISC.PB_WEST_FLMCFG0
Address	0000000002010C12 (SCOM)
Attributes	
Description	00 = pb_cfg_flmcfg0_valid 01:19 = pb_cfg_flmcfg0_group_size 20:45 = pb_cfg_flmcfg0_base_addr 46:47 = spare

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_FLMCFG0_VALID: configures the Foreign Local Memory BAR for link F0 as valid ON=>0b111 OFF=>0b000

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
1:19	RWX	PB_CFG_FLMCFG0_GROUP_SIZE_WEST: configures the group size for Foreign Local Memory BAR for link F0 16MB=>0b00000000000000000000 32MB=>0b00000000000000000001 64MB=>0b00000000000000000011 128MB=>0b00000000000000000111 256MB=>0b00000000000000001111 512MB=>0b00000000000000011111 1GB=>0b00000000000001111111 2GB=>0b00000000000011111111 4GB=>0b00000000001111111111 8GB=>0b00000000111111111111 16GB=>0b00000001111111111111 32GB=>0b00000011111111111111 64GB=>0b00000111111111111111 128GB=>0b00001111111111111111 256GB=>0b00011111111111111111 512GB=>0b00111111111111111111 1TB=>0b00111111111111111111 2TB=>0b01111111111111111111 4TB=>0b11111111111111111111 8TB=>0b11111111111111111111
20:45	RWX	PB_CFG_FLMCFG0_BASE_WEST: configures the base address of Foreign Local Memory BAR for link F0
46:47	RW	Reserved field. (Access type is spare)
48:63	RO	Constant = 0b0000000000000000

Register Name	<i>Processor Bus PB WEST FLMCFG1 Register</i>
Mnemonic	EH.PB.MISC.PB_WEST_FLMCFG1
Address	000000002010C13 (SCOM)
Attributes	
Description	00 = pb_cfg_flmcfg1_valid 01:19 = pb_cfg_flmcfg1_group_size 20:45 = pb_cfg_flmcfg1_base_addr 46:47 = spare

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_FLMCFG1_VALID: configures the Foreign Local Memory BAR for link F1 as valid ON=>0b111 OFF=>0b000



Bits	SCOM	Field Mnemonic: Description
1:19	RWX	PB_CFG_FLMCFG1_GROUP_SIZE_WEST: configures the group size for Foreign Local Memory BAR for link F1 16MB=>0b00000000000000000000 32MB=>0b00000000000000000001 64MB=>0b00000000000000000011 128MB=>0b00000000000000000111 256MB=>0b00000000000000001111 512MB=>0b00000000000000011111 1GB=>0b00000000000001111111 2GB=>0b00000000000011111111 4GB=>0b00000000001111111111 8GB=>0b00000000111111111111 16GB=>0b00000001111111111111 32GB=>0b00000011111111111111 64GB=>0b00000111111111111111 128GB=>0b00001111111111111111 256GB=>0b00011111111111111111 512GB=>0b00111111111111111111 1TB=>0b00111111111111111111 2TB=>0b01111111111111111111 4TB=>0b11111111111111111111 8TB=>0b11111111111111111111
20:45	RWX	PB_CFG_FLMCFG1_BASE_WEST: configures the base address of Foreign Local Memory BAR for link F1
46:47	RW	Reserved field. (Access type is spare)
48:63	RO	Constant = 0b0000000000000000

Register Name	Processor Bus PB WEST FLMCFG0 Register
Mnemonic	EH.PB.MISC.PB_WEST_FLMCFG0
Address	000000002010C14 (SCOM)
Attributes	
Description	00 = pb_cfg_flmcfgm0_valid 01:19 = pb_cfg_flmcfgm0_group_size 20:45 = pb_cfg_flmcfgm0_base_addr 46:47 = spare

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_FFMCFG0_VALID: configures the Foreign Far Memory BAR for link F0 as valid ON=>0b111 OFF=>0b000

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
1:19	RWX	PB_CFG_FFMCFG0_GROUP_SIZE_WEST: configures the group size for Foreign Far Memory BAR for link F0 16MB=>0b00000000000000000000 32MB=>0b00000000000000000001 64MB=>0b00000000000000000011 128MB=>0b00000000000000000111 256MB=>0b00000000000000001111 512MB=>0b00000000000000011111 1GB=>0b00000000000001111111 2GB=>0b00000000000011111111 4GB=>0b00000000001111111111 8GB=>0b00000000111111111111 16GB=>0b00000001111111111111 32GB=>0b00000011111111111111 64GB=>0b00000111111111111111 128GB=>0b00001111111111111111 256GB=>0b00011111111111111111 512GB=>0b01111111111111111111 1TB=>0b00111111111111111111 2TB=>0b01111111111111111111 4TB=>0b11111111111111111111 8TB=>0b11111111111111111111
20:45	RWX	PB_CFG_FFMCFG0_BASE_WEST: configures the base address of Foreign Far Memory BAR for link F0
46:47	RW	Reserved field. (Access type is spare)
48:63	RO	Constant = 0b0000000000000000

Register Name	<i>Processor Bus PB WEST FLMCFG1 Register</i>	
Mnemonic	EH.PB.MISC.PB_WEST_FLMCFG1	
Address	000000002010C15 (SCOM)	
Attributes		
Description	00 = pb_cfg_flmcfgm1_valid 01:19 = pb_cfg_flmcfgm1_group_size 20:45 = pb_cfg_flmcfgm1_base_addr 46:47 = spare	

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_FFMCFG1_VALID: configures the Foreign Far Memory BAR for link F1 as valid ON=>0b111 OFF=>0b000



Bits	SCOM	Field Mnemonic: Description
1:19	RWX	PB_CFG_FFMCFG1_GROUP_SIZE_WEST: configures the group size for Foreign Far Memory BAR for link F1 16MB=>0b00000000000000000000 32MB=>0b00000000000000000001 64MB=>0b00000000000000000011 128MB=>0b00000000000000000111 256MB=>0b00000000000000001111 512MB=>0b00000000000000011111 1GB=>0b00000000000001111111 2GB=>0b00000000000011111111 4GB=>0b00000000001111111111 8GB=>0b00000000111111111111 16GB=>0b00000001111111111111 32GB=>0b00000011111111111111 64GB=>0b00000111111111111111 128GB=>0b00001111111111111111 256GB=>0b00011111111111111111 512GB=>0b00111111111111111111 1TB=>0b00111111111111111111 2TB=>0b01111111111111111111 4TB=>0b11111111111111111111 8TB=>0b11111111111111111111
20:45	RWX	PB_CFG_FFMCFG1_BASE_WEST: configures the base address of Foreign Far Memory BAR for link F1
46:47	RW	Reserved field. (Access type is spare)
48:63	RO	Constant = 0b0000000000000000

Register Name	<i>Processor Bus PB WEST EVENT COMPB Register</i>
Mnemonic	EH.PB.MISC.PB_WEST_SCONFIG_LOAD
Address	000000002010C16 (SCOM)
Attributes	
Description	00 = pb_cfg_sconfig_load 01 = pb_cfg_sconfig_slow 02:07 = pb_cfg_sconfig_shift_count 08:11 = pb_cfg_sconfig_select 12:63 = pb_cfg_sconfig_shift_data

Bits	SCOM	Field Mnemonic: Description
0	WOX	PB_CFG_WEST_SCONFIG_LOAD: Load Serial Mode Registers
1	RWX	PB_CFG_WEST_SCONFIG_SLOW: Set Load of Serial Mode Registers to 16:1 slow clock
2:7	WOX	PB_CFG_WEST_SCONFIG_SHIFT_COUNT: Configures length of Serial Mode Register

Registers Specification

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Bits	SCOM	Field Mnemonic: Description
8:11	RWX	PB_CFG_WEST_SCONFIG_SELECT: Select Serial Mode register: 0000=pbh_pbiex_eh, 0001=pbh_pbiex_ex, 0010=pbh_dat_ex_req_pmac, 0011=pbh_dat_em_req_pmac, 0100=pbh_dat_arb_ex_pmac, 0101=pbh_dat_arb_em_pmac SEL_0=>0b0000 SEL_1=>0b0001 SEL_2=>0b0010 SEL_3=>0b0011 SEL_4=>0b0100 SEL_5=>0b0101 SEL_6=>0b0110 SEL_7=>0b0111 SEL_8=>0b1000 SEL_9=>0b1001 SEL_10=>0b1010 SEL_11=>0b1011 SEL_12=>0b1100 SEL_13=>0b1101 SEL_14=>0b1110 SEL_15=>0b1111
12:63	RWX	PB_CFG_WEST_SCONFIG_SHIFT_DATA: Serial Mode Register Data

Register Name	Processor Bus PB CENT Mode Configuration Register
Mnemonic	EH.PB.MISC.PB_CENT_MODE
Address	0000000002010C4A (SCOM)
Attributes	
Description	00 pb_cent_pbixxx_init 01:03 pb_cent_dbg_max_hang_stage_reached 04 pb_cfg_cent_chip_is_system 05:06 pb_cfg_cent_avp_mode(0:1) 07 spare 08 pb_cfg_cent_hng_chk_disable 09 pb_cfg_cent_dbg_clr_max_hang_stage 10:11 spare 12:15 pb_cfg_cent_sw_ab_wait(0:3) 16:21 pb_cfg_cent_sp_hw_mark(0:5) 22:27 pb_cfg_cent_gp_hw_mark(0:5) 28:33 pb_cfg_cent_lcl_hw_mark(0:5) 34:40 pb_cfg_cent_e2e_hw_mark(0:6) 41:46 pb_cfg_cent_fp_hw_mark(0:5) 47 pb_cfg_cent_reset_error_capture 48:58 spare 59 pb_cfg_cent_switch_option_ab 60:62 pb_cfg_cent_cpu_ratio_override(0:2) 63 reserved

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is pb_cent_pbixxx_init)
1:3	ROX	Reserved field. (Access type is pb_cent_dbg_max_hang_stage_reached)
4	RWX	PB_CFG_CHIP_IS_SYSTEM: configures whether there are other Processors in the system. ON=>0b111 OFF=>0b000
5:6	RWX	PB_CFG_AVP_MODE: configures command snoop and cresp arbiter for AVP test mode. Disables AHASH checks, tlb checks; 00=AVP disabled, 10=chip AVP, 11=card AVP OFF=>0b000000 CHIP_AVP=>0b101010 CARD_AVP=>0b111111
7	RW	OFF=>0b000000 CHIP_AVP=>0b101010 CARD_AVP=>0b111111



Bits	SCOM	Field Mnemonic: Description
8	RWX	PB_CFG_HNG_CHK_DISABLE: Hang Check Disable. ON=>0b111 OFF=>0b000
9	RWX	PB_DBG_CLR_MAX_HANG_STAGE: Resets the maximum hang state level (pb_hang_level) ON=>0b111 OFF=>0b000
10:11	RW	 ON=>0b111 OFF=>0b000
12:15	RWX	PB_CFG_SW_AB_WAIT: Adds delay to tc_pb_switch_ab input from TPC during hot plug sequence CNT_0=>0b0000000000000 CNT_1=>0b000100010001 CNT_2=>0b001000100010 CNT_3=>0b001100110011 CNT_4=>0b010001000100 CNT_5=>0b010101010101 CNT_6=>0b011001100110 CNT_7=>0b011101110111 CNT_8=>0b100010001000 CNT_9=>0b100110011001 CNT_10=>0b101010101010 CNT_11=>0b101110111011 CNT_12=>0b110011001100 CNT_13=>0b110111011101 CNT_14=>0b111011101110 CNT_15=>0b111111111111

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
16:21	RWX	PB_CFG_SP_HW_MARK: Configures the maximum system pumps an I/O unit can issue. CNT_0=>0b000000000000000000 CNT_1=>0b000001000001000001 CNT_2=>0b000010000010000010 CNT_3=>0b000011000011000011 CNT_4=>0b000100000100000100 CNT_5=>0b000101000101000101 CNT_6=>0b000110000110000110 CNT_7=>0b000111000111000111 CNT_8=>0b001000001000001000 CNT_9=>0b001001001001001001 CNT_10=>0b001010001010001010 CNT_11=>0b001011001011001011 CNT_12=>0b001100001100001100 CNT_13=>0b001101001101001101 CNT_14=>0b001110001110001110 CNT_15=>0b001111001111001111 CNT_16=>0b010000010000010000 CNT_17=>0b010001010001010001 CNT_18=>0b010010010010010010 CNT_19=>0b010011010011010011 CNT_20=>0b010100010100010100 CNT_21=>0b010101010101010101 CNT_22=>0b010110010110010110 CNT_23=>0b010111010111010111 CNT_24=>0b011000011000011000 CNT_25=>0b011001011001011001 CNT_26=>0b011010011010011010 CNT_27=>0b011011011011011011 CNT_28=>0b011100011100011100 CNT_29=>0b011101011101011101 CNT_30=>0b011110011110011110 CNT_31=>0b011111011111011111 CNT_32=>0b100000100000100000



Bits	SCOM	Field Mnemonic: Description
22:27	RWX	PB_CFG_GP_HW_MARK: configures the maximum group pumps this chip may issue CNT_0=>0b00000000000000000000 CNT_1=>0b000001000001000001 CNT_2=>0b000010000010000010 CNT_3=>0b000011000011000011 CNT_4=>0b000100000100000100 CNT_5=>0b000101000101000101 CNT_6=>0b000110000110000110 CNT_7=>0b000111000111000111 CNT_8=>0b001000001000001000 CNT_9=>0b001001001001001001 CNT_10=>0b001010001010001010 CNT_11=>0b001011001011001011 CNT_12=>0b001100001100001100 CNT_13=>0b001101001101001101 CNT_14=>0b001110001110001110 CNT_15=>0b001111001111001111 CNT_16=>0b010000010000010000 CNT_17=>0b010001010001010001 CNT_18=>0b010010010010010010 CNT_19=>0b010011010011010011 CNT_20=>0b010100010100010100 CNT_21=>0b010101010101010101 CNT_22=>0b010110010110010110 CNT_23=>0b010111010111010111 CNT_24=>0b011000011000011000 CNT_25=>0b011001011001011001 CNT_26=>0b011010011010011010 CNT_27=>0b011011011011011011 CNT_28=>0b011100011100011100 CNT_29=>0b011101011101011101 CNT_30=>0b011110011110011110 CNT_31=>0b011111011111011111 CNT_32=>0b100000100000100000

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
28:33	RWX	PB_CFG_LCL_HW_MARK: configures the maximum local pumps this chip may issue CNT_0=>0b000000000000000000 CNT_1=>0b000001000001000001 CNT_2=>0b000010000010000010 CNT_3=>0b000011000011000011 CNT_4=>0b000100000100000100 CNT_5=>0b000101000101000101 CNT_6=>0b000110000110000110 CNT_7=>0b000111000111000111 CNT_8=>0b001000001000001000 CNT_9=>0b001001001001001001 CNT_10=>0b001010001010001010 CNT_11=>0b001011001011001011 CNT_12=>0b001100001100001100 CNT_13=>0b001101001101001101 CNT_14=>0b001110001110001110 CNT_15=>0b001111001111001111 CNT_16=>0b010000010000010000 CNT_17=>0b010001010001010001 CNT_18=>0b010010010010010010 CNT_19=>0b010011010011010011 CNT_20=>0b010100010100010100 CNT_21=>0b010101010101010101 CNT_22=>0b010110010110010110 CNT_23=>0b010111010111010111 CNT_24=>0b011000011000011000 CNT_25=>0b011001011001011001 CNT_26=>0b011010011010011010 CNT_27=>0b011011011011011011 CNT_28=>0b011100011100011100 CNT_29=>0b011101011101011101 CNT_30=>0b011110011110011110 CNT_31=>0b011111011111011111 CNT_32=>0b100000100000100000

Bits	SCOM	Field Mnemonic: Description
34:40	RWX	PB_CFG_E2E_HW_MARK: configures the maximum local pumps this chip may issue CNT_0=>0b000000000000000000000000 CNT_1=>0b000000010000000100000001 CNT_2=>0b000000100000001000000010 CNT_3=>0b000000110000001100000011 CNT_4=>0b000001000000010000000100 CNT_5=>0b000001010000010100000101 CNT_6=>0b000001100000011000000110 CNT_7=>0b000001110000011100000111 CNT_8=>0b000010000000100000001000 CNT_9=>0b000010010000100100001001 CNT_10=>0b000010100000101000001010 CNT_11=>0b000010110000101100001011 CNT_12=>0b000011000000110000001100 CNT_13=>0b000011010000110100001101 CNT_14=>0b000011100000111000001110 CNT_15=>0b000011110000111100001111 CNT_16=>0b00100000001000000010000 CNT_17=>0b001000010001000010010001 CNT_18=>0b00100100001001000010010 CNT_19=>0b0010011000100110010010 CNT_20=>0b00101000001010000010100 CNT_21=>0b00101010001010100010101 CNT_22=>0b00101100001011000010110 CNT_23=>0b00101110001011100010111 CNT_24=>0b00110000001100000011000 CNT_25=>0b00110010001100100011001 CNT_26=>0b00110100001101000011010 CNT_27=>0b00110110001101100011011 CNT_28=>0b00111000001110000011100 CNT_29=>0b00111010001110100011101 CNT_30=>0b00111100001111000011110 CNT_31=>0b00111110001111100011111 CNT_32=>0b01000000010000000100000 CNT_33=>0b01000001010000010100001 CNT_34=>0b010000100100000100100010 CNT_35=>0b010000110100001101000011 CNT_36=>0b010010000010010000100100 CNT_37=>0b010010100010010100100101 CNT_38=>0b010011000010011001001010 CNT_39=>0b010011100010011101001011 CNT_40=>0b01010000010100000101000 CNT_41=>0b01010001010100001010001 CNT_42=>0b01010100001010001010010 CNT_43=>0b010101010001010101010101 CNT_44=>0b010110000010110000101100 CNT_45=>0b010110100010110100101101 CNT_46=>0b01011100001011100101110 CNT_47=>0b01011110001011110101111 CNT_48=>0b01100000011000000110000 CNT_49=>0b011000010110000010110001 CNT_50=>0b01100100001001000010010 CNT_51=>0b011001010000100101000101 CNT_52=>0b01101000001010000010100 CNT_53=>0b011010010000101001001001 CNT_54=>0b01101100001011000010110 CNT_55=>0b01101110001011100010111 CNT_56=>0b01110000001100000011000 CNT_57=>0b011100010000100100001001 CNT_58=>0b01110100001001000010010

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
41:46	RWX	PB_CFG_FP_HW_MARK: configures the maximum foreign pumps this chip may issue CNT_0=>0b00000000000000000000 CNT_1=>0b000001000001000001 CNT_2=>0b000010000010000010 CNT_3=>0b000011000011000011 CNT_4=>0b000100000100000100 CNT_5=>0b000101000101000101 CNT_6=>0b000110000110000110 CNT_7=>0b000111000111000111 CNT_8=>0b001000001000001000 CNT_9=>0b001001001001001001 CNT_10=>0b001010001010001010 CNT_11=>0b001011001011001011 CNT_12=>0b001100001100001100 CNT_13=>0b001101001101001101 CNT_14=>0b001110001110001110 CNT_15=>0b001111001111001111 CNT_16=>0b010000010000010000 CNT_17=>0b010001010001010001 CNT_18=>0b010010010010010010 CNT_19=>0b010011010011010011 CNT_20=>0b010100010100010100 CNT_21=>0b010101010101010101 CNT_22=>0b010110010110010110 CNT_23=>0b010111010111010111 CNT_24=>0b011000011000011000 CNT_25=>0b011001011001011001 CNT_26=>0b011010011010011010 CNT_27=>0b011011011011011011 CNT_28=>0b011100011100011100 CNT_29=>0b011101011101011101 CNT_30=>0b011110011110011110 CNT_31=>0b011111011111011111 CNT_32=>0b100000100000100000
47	RWX	PB_CFG_RESET_ERROR_CAPTURE: Reset cresp error capture latches
48:57	RW	
58	RW	PB_CFG_SWITCH_CD_PULSE: Controls switch_cd pulse width. Uses pb_cfg_sw_ab_wait to extend pulse. Default=long pulse. Requires pb_cfg_sw_ab_wait > cnt_5 for 6 cycle pulse. SHORT=>0b111 LONG=>0b000
59	RWX	PB_CFG_SWITCH_OPTION_AB: SCOM access to determine what signal drives pb_cfg_switch_cd. on=tc_pb_switch_ab, off=tc_pb_switch_cd. ON=>0b111 OFF=>0b000



Bits	SCOM	Field Mnemonic: Description
60:62	RWX	PB_CFG_CPU_RATIO_OVERRIDE: Sets rcmd high water mark. 000=16:max hw, 001=12:75% hw, 01x=8:50% hw, 1xx=4:25% hw LVL_0=>0b000000000 LVL_1=>0b001001001 LVL_2=>0b010010010 LVL_3=>0b011011011 LVL_4=>0b100100100 LVL_5=>0b101101101 LVL_6=>0b110110110 LVL_7=>0b111111111
63	RW	LVL_0=>0b000000000 LVL_1=>0b001001001 LVL_2=>0b010010010 LVL_3=>0b011011011 LVL_4=>0b100100100 LVL_5=>0b101101101 LVL_6=>0b110110110 LVL_7=>0b111111111

Register Name	Processor Bus PB CENT HP Mode Configuration Register
Mnemonic	EH.PB.MISC.PB_CENT_HP_MODE_NEXT
Address	0000000002010C4B (SCOM)
Attributes	
Description	00 pb_cfg_cent_master_chip 01 pb_cfg_cent_link_a0_en 02 pb_cfg_cent_link_a1_en 03 pb_cfg_cent_link_a2_en 04 pb_cfg_cent_na0_addr_dis 05 pb_cfg_cent_na1_addr_dis 06 pb_cfg_cent_na2_addr_dis 07:09 pb_cfg_cent_link_a0_nodeid(0:2) 10:12 pb_cfg_cent_link_a1_nodeid(0:2) 13:15 pb_cfg_cent_link_a2_nodeid(0:2) 16 pb_cfg_cent_a_aggregate 17 pb_cfg_cent_tm_grp_master 18 pb_cfg_cent_chg_rate_gp_master 19 pb_cfg_cent_chg_rate_sp_master 20 pb_cfg_cent_pump_mode 21 pb_cfg_cent_single_mc 22:23 spare 24:31 pb_cfg_cent_a_cmd_rate(0:7) 32 pb_cfg_cent_a_gather_enable 33:37 pb_cfg_cent_a_dly_cnt(0:4) 38 pb_cfg_cent_p0_x8tok 39 pb_cfg_cent_p2_x8tok 40 pb_cfg_cent_req_gather_enable 41 spare 42 pb_cfg_cent_f0_link_master 43 pb_cfg_cent_f1_link_master 44 pb_cfg_cent_link_f0_en 45 pb_cfg_cent_link_f1_en 46 pb_cfg_cent_nf0_addr_dis 47 pb_cfg_cent_nf1_addr_dis 48:50 pb_cfg_cent_link_f0_nodeid(0:2) 51:53 pb_cfg_cent_link_f1_nodeid(0:2) 54 spare 55 pb_cfg_cent_f_aggregate 56:63 pb_cfg_cent_f_cmd_rate(0:7)

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_MASTER_CHIP_NEXT: Processor bus master. ON=>0b111 OFF=>0b000
1	RWX	PB_CFG_LINK_A0_EN_NEXT: Link A0 enabled. ON=>0b111 OFF=>0b000
2	RWX	PB_CFG_LINK_A1_EN_NEXT: Link A1 enabled. ON=>0b111 OFF=>0b000

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
3	RWX	PB_CFG_LINK_A2_EN_NEXT: Link A2 enabled. ON=>0b111 OFF=>0b000
4	RWX	PB_CFG_LINK_NA0_ADDR_DIS_NEXT: Link A0 address broadcast disabled ON=>0b111 OFF=>0b000
5	RWX	PB_CFG_LINK_NA1_ADDR_DIS_NEXT: Link A1 address broadcast disabled ON=>0b111 OFF=>0b000
6	RWX	PB_CFG_LINK_NA2_ADDR_DIS_NEXT: Link A2 address broadcast disabled ON=>0b111 OFF=>0b000
7:9	RWX	PB_CFG_LINK_A0_NODEID_NEXT: Node ID of chip connected to A0 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
10:12	RWX	PB_CFG_LINK_A1_NODEID_NEXT: Node ID of chip connected to A1 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
13:15	RWX	PB_CFG_LINK_A2_NODEID_NEXT: Node ID of chip connected to A2 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111

Bits	SCOM	Field Mnemonic: Description
16	RWX	PB_CFG_A_AGGREGATE_NEXT: Processor bus A links are configured as parallel buses to same chip. ON=>0b111 OFF=>0b000
17	RWX	PB_CFG_TM_MASTER_NEXT: configure Chip as PB TM Master. ON=>0b111 OFF=>0b000
18	RWX	PB_CFG_CHG_RATE_GP_MASTER_NEXT: Sets the Group pump change rate master. This master gathers all GP chg_rate.reqs and issues a chg_rate.gnt ON=>0b111 OFF=>0b000
19	RWX	PB_CFG_CHG_RATE_SP_MASTER_NEXT: Sets the System pump change rate master. This master gathers all SP chg_rate.reqs and issues a chg_rate.gnt ON=>0b111 OFF=>0b000
20	RWX	PB_CFG_PUMP_MODE_NEXT: configures whether there are other Processors in the system and if they are part of this node NODAL_IS_CHIP_GROUP_IS_GROUP=>0b000 NODAL_AND_GROUP_IS_GROUP=>0b111
21	RWX	PB_CFG_SINGLE_MC_NEXT: Enables Single MC mode. ON=>0b111 OFF=>0b000
22	RW	PB_CFG_DCACHE_CAPP_MODE_NEXT: Dcache CAPP mode. Combines MC/L4 dcache codepoint for Beyond5Chip locality. ON=>0b111 OFF=>0b000
23	RW	ON=>0b111 OFF=>0b000
24:31	RWX	PB_CFG_A_CMD_RATE_CENT_NEXT: configures the paced command rate to not overrun the A link
32	RWX	PB_CFG_A_GATHER_ENABLE_NEXT: Enable Data OW gathering on A links. ON=>0b111 OFF=>0b000
33:37	RWX	PB_CFG_A_DLY_CNT_CENT_NEXT: configures the OW gathering delay count on A links

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Bits	SCOM	Field Mnemonic: Description
38	RWX	PB_CFG_P0_X8TOK_NEXT: Configures PHB0 as an 8 token data ramp. 0=PHB0/F0:4OW, 1=P0:8OW and F0:0OW ON=>0b111 OFF=>0b000
39	RWX	PB_CFG_P2_X8TOK_NEXT: Configures PHB2 as an 8 token data ramp. 0=PHB2/F1:4OW, 1=P2:8OW and F1:0OW ON=>0b111 OFF=>0b000
40	RWX	PB_CFG_REQ_GATHER_ENABLE_NEXT: Enable Data OW gathering on all chiplet/link requests. ON=>0b111 OFF=>0b000
41	RW	ON=>0b111 OFF=>0b000
42	RWX	PB_CFG_F0_LINK_MASTER_EN_NEXT: Link f0 command master enabled. ON=>0b111 OFF=>0b000
43	RWX	PB_CFG_F1_LINK_MASTER_EN_NEXT: Link f1 command master enabled. ON=>0b111 OFF=>0b000
44	RWX	PB_CFG_LINK_F0_EN_NEXT: Link f0 enabled. ON=>0b111 OFF=>0b000
45	RWX	PB_CFG_LINK_F1_EN_NEXT: Link f1 enabled. ON=>0b111 OFF=>0b000
46	RWX	PB_CFG_LINK_NF0_ADDR_DIS_NEXT: Link f0 address broadcast disabled ON=>0b111 OFF=>0b000
47	RWX	PB_CFG_LINK_NF1_ADDR_DIS_NEXT: Link f1 address broadcast disabled ON=>0b111 OFF=>0b000



Bits	SCOM	Field Mnemonic: Description
48:50	RWX	PB_CFG_LINK_F0_NODEID_NEXT: Node ID of chip connected to f0 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
51:53	RWX	PB_CFG_LINK_F1_NODEID_NEXT: Node ID of chip connected to f1 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
54	RW	ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
55	RWX	PB_CFG_F_AGGREGATE_NEXT: Processor bus F links are configured as parallel buses to same chip. ON=>0b111 OFF=>0b000
56:63	RWX	PB_CFG_F_CMD_RATE_CENT_NEXT: configures the paced command rate to not overrun the F link

Register Name	Processor Bus PB CENT HP Mode Configuration Register
Mnemonic	EH.PB.MISC.PB_CENT_HP_MODE_CURR
Address	0000000002010C4C (SCOM)
Attributes	
Description	00 pb_cfg_cent_master_chip 01 pb_cfg_cent_link_a0_en 02 pb_cfg_cent_link_a1_en 03 pb_cfg_cent_link_a2_en 04 pb_cfg_cent_na0_addr_dis 05 pb_cfg_cent_na1_addr_dis 06 pb_cfg_cent_na2_addr_dis 07:09 pb_cfg_cent_link_a0_nodeid(0:2) 10:12 pb_cfg_cent_link_a1_nodeid(0:2) 13:15 pb_cfg_cent_link_a2_nodeid(0:2) 16 pb_cfg_cent_a_aggregate 17 pb_cfg_cent_tm_grp_master 18 pb_cfg_cent_chg_rate_gp_master 19 pb_cfg_cent_chg_rate_sp_master 20 pb_cfg_cent_pump_mode 21 pb_cfg_cent_single_mc 22:23 spare 24:31 pb_cfg_cent_a_cmd_rate(0:7) 32 pb_cfg_cent_a_gather_enable 33:37 pb_cfg_cent_a_dly_cnt(0:4) 38 pb_cfg_cent_p0_x8tok 39 pb_cfg_cent_p2_x8tok 40 pb_cfg_cent_req_gather_enable 41 spare 42 pb_cfg_cent_f0_link_master 43 pb_cfg_cent_f1_link_master 44 pb_cfg_cent_link_f0_en 45 pb_cfg_cent_link_f1_en 46 pb_cfg_cent_nf0_addr_dis 47 pb_cfg_cent_nf1_addr_dis 48:50 pb_cfg_cent_link_f0_nodeid(0:2) 51:53 pb_cfg_cent_link_f1_nodeid(0:2) 54 spare 55 pb_cfg_cent_f_aggregate 56:63 pb_cfg_cent_f_cmd_rate(0:7)

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_MASTER_CHIP_CURR: Processor bus master. ON=>0b111 OFF=>0b000
1	RWX	PB_CFG_LINK_A0_EN_CURR: Link A0 enabled. ON=>0b111 OFF=>0b000
2	RWX	PB_CFG_LINK_A1_EN_CURR: Link A1 enabled. ON=>0b111 OFF=>0b000
3	RWX	PB_CFG_LINK_A2_EN_CURR: Link A2 enabled. ON=>0b111 OFF=>0b000
4	RWX	PB_CFG_LINK_NA0_ADDR_DIS_CURR: Link A0 address broadcast disabled ON=>0b111 OFF=>0b000
5	RWX	PB_CFG_LINK_NA1_ADDR_DIS_CURR: Link A1 address broadcast disabled ON=>0b111 OFF=>0b000
6	RWX	PB_CFG_LINK_NA2_ADDR_DIS_CURR: Link A2 address broadcast disabled ON=>0b111 OFF=>0b000
7:9	RWX	PB_CFG_LINK_A0_NODEID_CURR: Node ID of chip connected to A0 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111

Bits	SCOM	Field Mnemonic: Description
10:12	RWX	PB_CFG_LINK_A1_NODEID_CURR: Node ID of chip connected to A1 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
13:15	RWX	PB_CFG_LINK_A2_NODEID_CURR: Node ID of chip connected to A2 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
16	RWX	PB_CFG_A_AGGREGATE_CURR: Processor bus A links are configured as parallel buses to same chip. ON=>0b111 OFF=>0b000
17	RWX	PB_CFG_TM_MASTER_CURR: configure Chip as PB TM Master. ON=>0b111 OFF=>0b000
18	RWX	PB_CFG_CHG_RATE_GP_MASTER_CURR: Sets the Group pump change rate master. This master gathers all GP chg_rate.reqs and issues a chg_rate.gnt ON=>0b111 OFF=>0b000
19	RWX	PB_CFG_CHG_RATE_SP_MASTER_CURR: Sets the System pump change rate master. This master gathers all SP chg_rate.reqs and issues a chg_rate.gnt ON=>0b111 OFF=>0b000
20	RWX	PB_CFG_PUMP_MODE_CURR: configures whether there are other Processors in the system and if they are part of this node NODAL_IS_CHIP_GROUP_IS_GROUP=>0b000 NODAL_AND_GROUP_IS_GROUP=>0b111
21	RWX	PB_CFG_SINGLE_MC_CURR: Enables Single MC mode. ON=>0b111 OFF=>0b000

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
22	RW	PB_CFG_DCACHE_CAPP_MODE_CURR: Dcache CAPP mode. Combines MC/L4 dcache codepoint for Beyond5Chip locality. ON=>0b111 OFF=>0b000
23	RW	 ON=>0b111 OFF=>0b000
24:31	RWX	PB_CFG_A_CMD_RATE_CENT_CURR: configures the paced command rate to not overrun the A link
32	RWX	PB_CFG_A_GATHER_ENABLE_CURR: Enable Data OW gathering on A links. ON=>0b111 OFF=>0b000
33:37	RWX	PB_CFG_A_DLY_CNT_CENT_CURR: configures the OW gathering delay count on A links
38	RWX	PB_CFG_P0_X8TOK_CURR: Configures PHB0 as an 8 token data ramp. 0=PHB0/F0:4OW, 1=P0:8OW and F0:0OW ON=>0b111 OFF=>0b000
39	RWX	PB_CFG_P2_X8TOK_CURR: Configures PHB2 as an 8 token data ramp. 0=PHB2/F1:4OW, 1=P2:8OW and F1:0OW ON=>0b111 OFF=>0b000
40	RWX	PB_CFG_REQ_GATHER_ENABLE_CURR: Enable Data OW gathering on all chiplet/link requests. ON=>0b111 OFF=>0b000
41	RW	 ON=>0b111 OFF=>0b000
42	RWX	PB_CFG_F0_LINK_MASTER_EN_CURR: Link f0 command master enabled. ON=>0b111 OFF=>0b000
43	RWX	PB_CFG_F1_LINK_MASTER_EN_CURR: Link f1 command master enabled. ON=>0b111 OFF=>0b000
44	RWX	PB_CFG_LINK_F0_EN_CURR: Link f0 enabled. ON=>0b111 OFF=>0b000



Bits	SCOM	Field Mnemonic: Description
45	RWX	PB_CFG_LINK_F1_EN_CURR: Link f1 enabled. ON=>0b111 OFF=>0b000
46	RWX	PB_CFG_LINK_F0_ADDR_DIS_CURR: Link f0 address broadcast disabled ON=>0b111 OFF=>0b000
47	RWX	PB_CFG_LINK_F1_ADDR_DIS_CURR: Link f1 address broadcast disabled ON=>0b111 OFF=>0b000
48:50	RWX	PB_CFG_LINK_F0_NODEID_CURR: Node ID of chip connected to f0 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
51:53	RWX	PB_CFG_LINK_F1_NODEID_CURR: Node ID of chip connected to f1 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
54	RW	ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
55	RWX	PB_CFG_F_AGGREGATE_CURR: Processor bus F links are configured as parallel buses to same chip. ON=>0b111 OFF=>0b000
56:63	RWX	PB_CFG_F_CMD_RATE_CENT_CURR: configures the paced command rate to not overrun the F link

Registers Specification

POWER8 Processor

Register Name	Processor Bus PB CENT HP Mode Configuration Register
Mnemonic	EH.PB.MISC.PB_CENT_HPX_MODE_NEXT
Address	0000000002010C4D (SCOM)
Attributes	
Description	00 pb_cfg_cent_link_x0_en 01 pb_cfg_cent_link_x1_en 02 pb_cfg_cent_link_x2_en 03 pb_cfg_cent_link_x3_en 04 spare 05 pb_cfg_cent_nx0_addr_dis 06 pb_cfg_cent_nx1_addr_dis 07 pb_cfg_cent_nx2_addr_dis 08 pb_cfg_cent_nx3_addr_dis 09 spare 10:12 pb_cfg_cent_link_x0_chipid(0:2) 13:15 pb_cfg_cent_link_x1_chipid(0:2) 16:18 pb_cfg_cent_link_x2_chipid(0:2) 19:21 pb_cfg_cent_link_x3_chipid(0:2) 22:24 spare 25 pb_cfg_cent_x_aggregate 26 pb_cfg_cent_x_indirect_en 27 pb_cfg_cent_x_fp_disabled 28:31 spare 32 pb_cfg_cent_x_gather_enable 33:37 pb_cfg_cent_x_dly_cnt(0:4) 38 pb_cfg_cent_x_onnode_12ques 39 spare 40 pb_cfg_cent_a0_ind_a1_en 41 pb_cfg_cent_a0_ind_a2_en 42 pb_cfg_cent_a1_ind_a0_en 43 pb_cfg_cent_a1_ind_a2_en 44 pb_cfg_cent_a2_ind_a0_en 45 pb_cfg_cent_a2_ind_a1_en 46:55 spare 56:63 pb_cfg_cent_x_cmd_rate(0:7)

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_LINK_X0_EN_NEXT: Link X0 enabled. ON=>0b111 OFF=>0b000
1	RWX	PB_CFG_LINK_X1_EN_NEXT: Link X1 enabled. ON=>0b111 OFF=>0b000
2	RWX	PB_CFG_LINK_X2_EN_NEXT: Link X2 enabled. ON=>0b111 OFF=>0b000
3	RWX	PB_CFG_LINK_X3_EN_NEXT: Link X3 enabled. ON=>0b111 OFF=>0b000
4	RW	ON=>0b111 OFF=>0b000
5	RWX	PB_CFG_LINK_NX0_ADDR_DIS_NEXT: Link X0 address broadcast disabled ON=>0b111 OFF=>0b000
6	RWX	PB_CFG_LINK_NX1_ADDR_DIS_NEXT: Link X1 address broadcast disabled ON=>0b111 OFF=>0b000
7	RWX	PB_CFG_LINK_NX2_ADDR_DIS_NEXT: Link X2 address broadcast disabled ON=>0b111 OFF=>0b000



Bits	SCOM	Field Mnemonic: Description
8	RWX	PB_CFG_LINK_NX3_ADDR_DIS_NEXT: Link X3 address broadcast disabled ON=>0b111 OFF=>0b000
9	RW	ON=>0b111 OFF=>0b000
10:12	RWX	PB_CFG_LINK_X0_CHIPID_NEXT: Chip ID of chip connected to X0 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
13:15	RWX	PB_CFG_LINK_X1_CHIPID_NEXT: Chip ID of chip connected to X1 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
16:18	RWX	PB_CFG_LINK_X2_CHIPID_NEXT: Chip ID of chip connected to X2 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
19:21	RWX	PB_CFG_LINK_X3_CHIPID_NEXT: Chip ID of chip connected to X3 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
22:24	RW	ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
25	RWX	PB_CFG_X_AGGREGATE_NEXT: Processor bus X links are configured as parallel buses to same chip. ON=>0b111 OFF=>0b000
26	RWX	PB_CFG_X_INDIRECT_EN_NEXT: Processor bus X links are configured for indirect data routing. ON=>0b111 OFF=>0b000
27	RWX	PB_CFG_X_FP_DISABLED_NEXT: Processor bus X link rtag fastpath disable. ON=>0b111 OFF=>0b000
28:31	RW	ON=>0b111 OFF=>0b000
32	RWX	PB_CFG_X_GATHER_ENABLE_NEXT: Enable Data OW gathering on X links. ON=>0b111 OFF=>0b000
33:37	RWX	PB_CFG_X_DLY_CNT_CENT_NEXT: configures the OW gathering delay count on X links
38	RWX	PB_CFG_X_ONNODE_12QUES_NEXT: Configures X on group queue depth to 12 OW. 1=12on/4off. 0=8on/8off. ON=>0b111 OFF=>0b000
39	RW	ON=>0b111 OFF=>0b000
40	RWX	PB_CFG_A0_IND_A1_EN_NEXT: Enable Indirect Data routing on secondary A1 link. A0 is primary. ON=>0b111 OFF=>0b000
41	RWX	PB_CFG_A0_IND_A2_EN_NEXT: Enable Indirect Data routing on secondary A2 link. A0 is primary. ON=>0b111 OFF=>0b000



Bits	SCOM	Field Mnemonic: Description
42	RWX	PB_CFG_A1_IND_A0_EN_NEXT: Enable Indirect Data routing on secondary A0 link. A1 is primary. ON=>0b111 OFF=>0b000
43	RWX	PB_CFG_A1_IND_A2_EN_NEXT: Enable Indirect Data routing on secondary A2 link. A1 is primary. ON=>0b111 OFF=>0b000
44	RWX	PB_CFG_A2_IND_A0_EN_NEXT: Enable Indirect Data routing on secondary A0 link. A2 is primary. ON=>0b111 OFF=>0b000
45	RWX	PB_CFG_A2_IND_A1_EN_NEXT: Enable Indirect Data routing on secondary A1 link. A2 is primary. ON=>0b111 OFF=>0b000
46:55	RW	ON=>0b111 OFF=>0b000
56:63	RWX	PB_CFG_X_CMD_RATE_CENT_NEXT: configures the paced command rate to not overrun the X link

Register Name	Processor Bus PB CENT HP Mode Configuration Register
Mnemonic	EH.PB.MISC.PB_CENT_HP_X_MODE_CURR
Address	0000000002010C4E (SCOM)
Attributes	
Description	00 pb_cfg_cent_link_x0_en 01 pb_cfg_cent_link_x1_en 02 pb_cfg_cent_link_x2_en 03 pb_cfg_cent_link_x3_en 04 spare 05 pb_cfg_cent_nx0_addr_dis 06 pb_cfg_cent_nx1_addr_dis 07 pb_cfg_cent_nx2_addr_dis 08 pb_cfg_cent_nx3_addr_dis 09 spare 10:12 pb_cfg_cent_link_x0_chipid(0:2) 13:15 pb_cfg_cent_link_x1_chipid(0:2) 16:18 pb_cfg_cent_link_x2_chipid(0:2) 19:21 pb_cfg_cent_link_x3_chipid(0:2) 22:24 spare 25 pb_cfg_cent_x_aggregate 26 pb_cfg_cent_x_indirect_en 27 pb_cfg_cent_x_fp_disabled 28:31 spare 32 pb_cfg_cent_x_gather_enable 33:37 pb_cfg_cent_x_dly_cnt(0:4) 38 pb_cfg_cent_x_onnode_12ques 39 spare 40 pb_cfg_cent_a0_ind_a1_en 41 pb_cfg_cent_a0_ind_a2_en 42 pb_cfg_cent_a1_ind_a0_en 43 pb_cfg_cent_a1_ind_a2_en 44 pb_cfg_cent_a2_ind_a0_en 45 pb_cfg_cent_a2_ind_a1_en 46:55 spare 56:63 pb_cfg_cent_x_cmd_rate(0:7)

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_LINK_X0_EN_CURR: Link X0 enabled. ON=>0b111 OFF=>0b000
1	RWX	PB_CFG_LINK_X1_EN_CURR: Link X1 enabled. ON=>0b111 OFF=>0b000

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Bits	SCOM	Field Mnemonic: Description
2	RWX	PB_CFG_LINK_X2_EN_CURR: Link X2 enabled. ON=>0b111 OFF=>0b000
3	RWX	PB_CFG_LINK_X3_EN_CURR: Link X3 enabled. ON=>0b111 OFF=>0b000
4	RW	 ON=>0b111 OFF=>0b000
5	RWX	PB_CFG_LINK_NX0_ADDR_DIS_CURR: Link X0 address broadcast disabled ON=>0b111 OFF=>0b000
6	RWX	PB_CFG_LINK_NX1_ADDR_DIS_CURR: Link X1 address broadcast disabled ON=>0b111 OFF=>0b000
7	RWX	PB_CFG_LINK_NX2_ADDR_DIS_CURR: Link X2 address broadcast disabled ON=>0b111 OFF=>0b000
8	RWX	PB_CFG_LINK_NX3_ADDR_DIS_CURR: Link X3 address broadcast disabled ON=>0b111 OFF=>0b000
9	RW	 ON=>0b111 OFF=>0b000
10:12	RWX	PB_CFG_LINK_X0_CHIPID_CURR: Chip ID of chip connected to X0 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111

Bits	SCOM	Field Mnemonic: Description
13:15	RWX	PB_CFG_LINK_X1_CHIPID_CURR: Chip ID of chip connected to X1 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
16:18	RWX	PB_CFG_LINK_X2_CHIPID_CURR: Chip ID of chip connected to X2 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
19:21	RWX	PB_CFG_LINK_X3_CHIPID_CURR: Chip ID of chip connected to X3 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
22:24	RW	ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
25	RWX	PB_CFG_X_AGGREGATE_CURR: Processor bus X links are configured as parallel buses to same chip. ON=>0b111 OFF=>0b000
26	RWX	PB_CFG_X_INDIRECT_EN_CURR: Processor bus X links are configured for indirect data routing. ON=>0b111 OFF=>0b000
27	RWX	PB_CFG_X_FP_DISABLED_CURR: Processor bus X link rtag fastpath disable. ON=>0b111 OFF=>0b000

Registers Specification

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Bits	SCOM	Field Mnemonic: Description
28:31	RW	ON=>0b111 OFF=>0b000
32	RWX	PB_CFG_X_GATHER_ENABLE_CURR: Enable Data OW gathering on X links. ON=>0b111 OFF=>0b000
33:37	RWX	PB_CFG_X_DLY_CNT_CENT_CURR: configures the OW gathering delay count on X links
38	RWX	PB_CFG_X_ONNODE_12QUES_CURR: Configures X on group queue depth to 12 OW. 1=12on/4off. 0=8on/8off. ON=>0b111 OFF=>0b000
39	RW	ON=>0b111 OFF=>0b000
40	RWX	PB_CFG_A0_IND_A1_EN_CURR: Enable Indirect Data routing on secondary A1 link. A0 is primary. ON=>0b111 OFF=>0b000
41	RWX	PB_CFG_A0_IND_A2_EN_CURR: Enable Indirect Data routing on secondary A2 link. A0 is primary. ON=>0b111 OFF=>0b000
42	RWX	PB_CFG_A1_IND_A0_EN_CURR: Enable Indirect Data routing on secondary A0 link. A1 is primary. ON=>0b111 OFF=>0b000
43	RWX	PB_CFG_A1_IND_A2_EN_CURR: Enable Indirect Data routing on secondary A2 link. A1 is primary. ON=>0b111 OFF=>0b000
44	RWX	PB_CFG_A2_IND_A0_EN_CURR: Enable Indirect Data routing on secondary A0 link. A2 is primary. ON=>0b111 OFF=>0b000
45	RWX	PB_CFG_A2_IND_A1_EN_CURR: Enable Indirect Data routing on secondary A1 link. A2 is primary. ON=>0b111 OFF=>0b000
46:55	RW	ON=>0b111 OFF=>0b000
56:63	RWX	PB_CFG_X_CMD_RATE_CENT_CURR: configures the paced command rate to not overrun the X link



Register Name	<i>Processor Bus PB CENT FLMCFG0 Register</i>
Mnemonic	EH.PB.MISC.PB_CENT_FLMCFG0
Address	0000000002010C5E (SCOM)
Attributes	
Description	00 = pb_cfg_flmcfg0_valid 01:19 = pb_cfg_flmcfg0_group_size 20:45 = pb_cfg_flmcfg0_base_addr 46:47 = spare

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_FLMCFG0_VALID: configures the Foreign Local Memory BAR for link F0 as valid ON=>0b111 OFF=>0b000
1:19	RWX	PB_CFG_FLMCFG0_GROUP_SIZE_CENT: configures the group size for Foreign Local Memory BAR for link F0 16MB=>0b00000000000000000000 32MB=>0b00000000000000000001 64MB=>0b00000000000000000011 128MB=>0b00000000000000000111 256MB=>0b00000000000000001111 512MB=>0b00000000000000011111 1GB=>0b00000000000001111111 2GB=>0b00000000000011111111 4GB=>0b00000000000111111111 8GB=>0b00000000011111111111 16GB=>0b00000000111111111111 32GB=>0b00000001111111111111 64GB=>0b00000011111111111111 128GB=>0b00000111111111111111 256GB=>0b00001111111111111111 512GB=>0b00011111111111111111 1TB=>0b00111111111111111111 2TB=>0b01111111111111111111 4TB=>0b11111111111111111111 8TB=>0b11111111111111111111
20:45	RWX	PB_CFG_FLMCFG0_BASE_CENT: configures the base address of Foreign Local Memory BAR for link F0
46:47	RW	Reserved field. (Access type is spare)
48:63	RO	Constant = 0b0000000000000000

Register Name	<i>Processor Bus PB CENT FLMCFG1 Register</i>
Mnemonic	EH.PB.MISC.PB_CENT_FLMCFG1
Address	0000000002010C5F (SCOM)
Attributes	
Description	00 = pb_cfg_flmcfg1_valid 01:19 = pb_cfg_flmcfg1_group_size 20:45 = pb_cfg_flmcfg1_base_addr 46:47 = spare

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_FLMCFG1_VALID: configures the Foreign Local Memory BAR for link F1 as valid ON=>0b111 OFF=>0b000
1:19	RWX	PB_CFG_FLMCFG1_GROUP_SIZE_CENT: configures the group size for Foreign Local Memory BAR for link F1 16MB=>0b00000000000000000000 32MB=>0b00000000000000000001 64MB=>0b00000000000000000011 128MB=>0b00000000000000000111 256MB=>0b00000000000000001111 512MB=>0b00000000000000011111 1GB=>0b00000000000001111111 2GB=>0b00000000000011111111 4GB=>0b00000000000111111111 8GB=>0b00000000011111111111 16GB=>0b00000000111111111111 32GB=>0b00000001111111111111 64GB=>0b00000011111111111111 128GB=>0b00000111111111111111 256GB=>0b00001111111111111111 512GB=>0b00011111111111111111 1TB=>0b00111111111111111111 2TB=>0b01111111111111111111 4TB=>0b11111111111111111111 8TB=>0b11111111111111111111
20:45	RWX	PB_CFG_FLMCFG1_BASE_CENT: configures the base address of Foreign Local Memory BAR for link F1
46:47	RW	Reserved field. (Access type is spare)
48:63	RO	Constant = 0b0000000000000000

Register Name	<i>Processor Bus PB CENT FLMCFG0 Register</i>
Mnemonic	EH.PB.MISC.PB_CENT_FLMCFG0
Address	000000002010C60 (SCOM)
Attributes	
Description	00 = pb_cfg_flmcfgm0_valid 01:19 = pb_cfg_flmcfgm0_group_size 20:45 = pb_cfg_flmcfgm0_base_addr 46:47 = spare

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_FFMCFG0_VALID: configures the Foreign Far Memory BAR for link F0 as valid ON=>0b111 OFF=>0b000



Bits	SCOM	Field Mnemonic: Description
1:19	RWX	PB_CFG_FFMCFG0_GROUP_SIZE_CENT: configures the group size for Foreign Far Memory BAR for link F0 16MB=>0b00000000000000000000 32MB=>0b00000000000000000001 64MB=>0b00000000000000000011 128MB=>0b00000000000000000111 256MB=>0b00000000000000001111 512MB=>0b00000000000000011111 1GB=>0b00000000000001111111 2GB=>0b00000000000011111111 4GB=>0b00000000001111111111 8GB=>0b00000000111111111111 16GB=>0b00000001111111111111 32GB=>0b00000011111111111111 64GB=>0b00000111111111111111 128GB=>0b00001111111111111111 256GB=>0b00011111111111111111 512GB=>0b00111111111111111111 1TB=>0b00111111111111111111 2TB=>0b01111111111111111111 4TB=>0b11111111111111111111 8TB=>0b11111111111111111111
20:45	RWX	PB_CFG_FFMCFG0_BASE_CENT: configures the base address of Foreign Far Memory BAR for link F0
46:47	RW	Reserved field. (Access type is spare)
48:63	RO	Constant = 0b0000000000000000

Register Name	Processor Bus PB CENT FLMCFG0 Register
Mnemonic	EH.PB.MISC.PB_CENT_FLMCFG0
Address	000000002010C61 (SCOM)
Attributes	
Description	00 = pb_cfg_flmcfg0_valid 01:19 = pb_cfg_flmcfg0_group_size 20:45 = pb_cfg_flmcfg0_base_addr 46:47 = spare

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_FFMCFG1_VALID: configures the Foreign Far Memory BAR for link F1 as valid ON=>0b111 OFF=>0b000

Registers Specification

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Bits	SCOM	Field Mnemonic: Description
1:19	RWX	PB_CFG_FFMCFG1_GROUP_SIZE_CENT: configures the group size for Foreign Far Memory BAR for link F1 16MB=>0b00000000000000000000 32MB=>0b00000000000000000001 64MB=>0b00000000000000000011 128MB=>0b00000000000000000111 256MB=>0b00000000000000001111 512MB=>0b00000000000000011111 1GB=>0b00000000000001111111 2GB=>0b00000000000011111111 4GB=>0b00000000001111111111 8GB=>0b00000000111111111111 16GB=>0b00000001111111111111 32GB=>0b00000011111111111111 64GB=>0b00000111111111111111 128GB=>0b00001111111111111111 256GB=>0b00011111111111111111 512GB=>0b00111111111111111111 1TB=>0b00111111111111111111 2TB=>0b01111111111111111111 4TB=>0b11111111111111111111 8TB=>0b11111111111111111111
20:45	RWX	PB_CFG_FFMCFG1_BASE_CENT: configures the base address of Foreign Far Memory BAR for link F1
46:47	RW	Reserved field. (Access type is spare)
48:63	RO	Constant = 0b0000000000000000

Register Name	<i>Processor Bus PB CENT Event COMPB Register</i>
Mnemonic	EH.PB.MISC.PB_CENT_SCONFIG_LOAD
Address	000000002010C6D (SCOM)
Attributes	
Description	00 = pb_cfg_sconfig_load 01 = pb_cfg_sconfig_slow 02:07 = pb_cfg_sconfig_shift_count 08:11 = pb_cfg_sconfig_select 12:63 = pb_cfg_sconfig_shift_data

Bits	SCOM	Field Mnemonic: Description
0	WOX	PB_CFG_CENT_SCONFIG_LOAD: Load Serial Mode Registers
1	RWX	PB_CFG_CENT_SCONFIG_SLOW: Set Load of Serial Mode Registers to 16:1 slow clock
2:7	WOX	PB_CFG_CENT_SCONFIG_SHIFT_COUNT: Configures length of Serial Mode Register

Bits	SCOM	Field Mnemonic: Description
8:11	RWX	PB_CFG_CENT_SCONFIG_SELECT: Select Serial Mode register: 0000=pbh_pbien, 0001=pbh_pbies, 0010=pbh_dat_ex_req_pmac, 0011=pbh_dat_arb_enes_pmac, 01xx=pbh_cmd_snooper_pmac, SEL_0=>0b0000 SEL_1=>0b0001 SEL_2=>0b0010 SEL_3=>0b0011 SEL_4=>0b0100 SEL_5=>0b0101 SEL_6=>0b0110 SEL_7=>0b0111 SEL_8=>0b1000 SEL_9=>0b1001 SEL_10=>0b1010 SEL_11=>0b1011 SEL_12=>0b1100 SEL_13=>0b1101 SEL_14=>0b1110 SEL_15=>0b1111
12:63	RWX	PB_CFG_CENT_SCONFIG_SHIFT_DATA: Serial Mode Register Data

Register Name	Processor Bus PB East Mode Register
Mnemonic	EH.PB.MISC.PB_EAST_MODE
Address	0000000002010C8A (SCOM)
Attributes	
Description	00 pb_east_pbixxx_init 01:03 spare 04 pb_cfg_east_chip_is_system 05:06 pb_cfg_east_avp_mode(0:1) 07 spare 08 pb_cfg_east_hng_chk_disable 09 pb_cfg_east_dbg_clr_max_hang_stage 10:11 spare 12:15 pb_cfg_east_sw_ab_wait(0:3) 16:21 pb_cfg_east_sp_hw_mark(0:5) 22:27 pb_cfg_east_gp_hw_mark(0:5) 28:33 pb_cfg_east_lcl_hw_mark(0:5) 34:40 pb_cfg_east_e2e_hw_mark(0:6) 41:46 pb_cfg_east_fp_hw_mark(0:5) 47 pb_cfg_east_reset_error_capture 48:58 spare 59 pb_cfg_east_switch_option_ab 60:62 pb_cfg_east_cpu_ratio_override(0:2) 63 reserved

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is pb_east_pbixxx_init)
1:3	RO	Constant = 0b000
4	RWX	PB_CFG_CHIP_IS_SYSTEM: configures whether there are other Processors in the system. ON=>0b111 OFF=>0b000
5:6	RWX	PB_CFG_AVP_MODE: configures command snooper and cresp arbiter for AVP test mode. Disables AHASH checks, tlbi checks; 00=AVP disabled, 10=chip AVP, 11=card AVP OFF=>0b000000 CHIP_AVP=>0b101010 CARD_AVP=>0b111111
7	RW	OFF=>0b000000 CHIP_AVP=>0b101010 CARD_AVP=>0b111111

Registers Specification

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Bits	SCOM	Field Mnemonic: Description
8	RWX	PB_CFG_HNG_CHK_DISABLE: Hang Check Disable. ON=>0b111 OFF=>0b000
9	RWX	PB_DBG_CLR_MAX_HANG_STAGE: Resets the maximum hang state level (pb_hang_level) ON=>0b111 OFF=>0b000
10:11	RW	ON=>0b111 OFF=>0b000
12:15	RWX	PB_CFG_SW_AB_WAIT: Adds delay to tc_pb_switch_ab input from TPC during hot plug sequence CNT_0=>0b0000000000000 CNT_1=>0b000100010001 CNT_2=>0b001000100010 CNT_3=>0b001100110011 CNT_4=>0b010001000100 CNT_5=>0b010101010101 CNT_6=>0b011001100110 CNT_7=>0b011101110111 CNT_8=>0b100010001000 CNT_9=>0b100110011001 CNT_10=>0b101010101010 CNT_11=>0b101110111011 CNT_12=>0b110011001100 CNT_13=>0b110111011101 CNT_14=>0b111011101110 CNT_15=>0b111111111111



Bits	SCOM	Field Mnemonic: Description
16:21	RWX	PB_CFG_SP_HW_MARK: Configures the maximum system pumps an I/O unit can issue. CNT_0=>0b00000000000000000000 CNT_1=>0b000001000001000001 CNT_2=>0b000010000010000010 CNT_3=>0b000011000011000011 CNT_4=>0b000100000100000100 CNT_5=>0b000101000101000101 CNT_6=>0b000110000110000110 CNT_7=>0b000111000111000111 CNT_8=>0b001000001000001000 CNT_9=>0b001001001001001001 CNT_10=>0b001010001010001010 CNT_11=>0b001011001011001011 CNT_12=>0b001100001100001100 CNT_13=>0b001101001101001101 CNT_14=>0b001110001110001110 CNT_15=>0b001111001111001111 CNT_16=>0b010000010000010000 CNT_17=>0b010001010001010001 CNT_18=>0b010010010010010010 CNT_19=>0b010011010011010011 CNT_20=>0b010100010100010100 CNT_21=>0b010101010101010101 CNT_22=>0b010110010110010110 CNT_23=>0b010111010111010111 CNT_24=>0b011000011000011000 CNT_25=>0b011001011001011001 CNT_26=>0b011010011010011010 CNT_27=>0b011011011011011011 CNT_28=>0b011100011100011100 CNT_29=>0b011101011101011101 CNT_30=>0b011110011110011110 CNT_31=>0b011111011111011111 CNT_32=>0b100000100000100000

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Bits	SCOM	Field Mnemonic: Description
22:27	RWX	PB_CFG_GP_HW_MARK: configures the maximum group pumps this chip may issue CNT_0=>0b000000000000000000 CNT_1=>0b000001000001000001 CNT_2=>0b000010000010000010 CNT_3=>0b000011000011000011 CNT_4=>0b000100000100000100 CNT_5=>0b000101000101000101 CNT_6=>0b000110000110000110 CNT_7=>0b000111000111000111 CNT_8=>0b001000001000001000 CNT_9=>0b001001001001001001 CNT_10=>0b001010001010001010 CNT_11=>0b001011001011001011 CNT_12=>0b001100001100001100 CNT_13=>0b001101001101001101 CNT_14=>0b001110001110001110 CNT_15=>0b001111001111001111 CNT_16=>0b010000010000010000 CNT_17=>0b010001010001010001 CNT_18=>0b010010010010010010 CNT_19=>0b010011010011010011 CNT_20=>0b010100010100010100 CNT_21=>0b010101010101010101 CNT_22=>0b010110010110010110 CNT_23=>0b010111010111010111 CNT_24=>0b011000011000011000 CNT_25=>0b011001011001011001 CNT_26=>0b011010011010011010 CNT_27=>0b011011011011011011 CNT_28=>0b011100011100011100 CNT_29=>0b011101011101011101 CNT_30=>0b011110011110011110 CNT_31=>0b011111011111011111 CNT_32=>0b100000100000100000



Bits	SCOM	Field Mnemonic: Description
28:33	RWX	PB_CFG_LCL_HW_MARK: configures the maximum local pumps this chip may issue CNT_0=>0b00000000000000000000 CNT_1=>0b000001000001000001 CNT_2=>0b000010000010000010 CNT_3=>0b000011000011000011 CNT_4=>0b000100000100000100 CNT_5=>0b000101000101000101 CNT_6=>0b000110000110000110 CNT_7=>0b000111000111000111 CNT_8=>0b001000001000001000 CNT_9=>0b001001001001001001 CNT_10=>0b001010001010001010 CNT_11=>0b001011001011001011 CNT_12=>0b001100001100001100 CNT_13=>0b001101001101001101 CNT_14=>0b001110001110001110 CNT_15=>0b001111001111001111 CNT_16=>0b010000010000010000 CNT_17=>0b010001010001010001 CNT_18=>0b010010010010010010 CNT_19=>0b010011010011010011 CNT_20=>0b010100010100010100 CNT_21=>0b010101010101010101 CNT_22=>0b010110010110010110 CNT_23=>0b010111010111010111 CNT_24=>0b011000011000011000 CNT_25=>0b011001011001011001 CNT_26=>0b011010011010011010 CNT_27=>0b011011011011011011 CNT_28=>0b011100011100011100 CNT_29=>0b011101011101011101 CNT_30=>0b011110011110011110 CNT_31=>0b011111011111011111 CNT_32=>0b100000100000100000

Registers Specification

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Bits	SCOM	Field Mnemonic: Description
34:40	RWX	PB_CFG_E2E_HW_MARK: configures the maximum local pumps this chip may issue CNT_0=>0b000000000000000000000000 CNT_1=>0b0000001000000100000001 CNT_2=>0b000001000000100000010 CNT_3=>0b000001100000110000011 CNT_4=>0b000010000001000000100 CNT_5=>0b000010100001010000101 CNT_6=>0b000011000001100000110 CNT_7=>0b000011100001110000111 CNT_8=>0b000100000010000001000 CNT_9=>0b000100100010010001001 CNT_10=>0b000101000010100001010 CNT_11=>0b000101100010110001011 CNT_12=>0b000110000011000001100 CNT_13=>0b000110100011010001101 CNT_14=>0b000111000011100001110 CNT_15=>0b000111100011110001111 CNT_16=>0b001000000100000010000 CNT_17=>0b001000100100010010001 CNT_18=>0b001001000100100010010 CNT_19=>0b001001100100110010011 CNT_20=>0b001010000101000010100 CNT_21=>0b001010100101010010101 CNT_22=>0b001011000101100010110 CNT_23=>0b001011100101110010111 CNT_24=>0b001100000110000011000 CNT_25=>0b001100100110010011001 CNT_26=>0b001101000110100011010 CNT_27=>0b001101100110110011011 CNT_28=>0b001110000111000011100 CNT_29=>0b001110100111010011101 CNT_30=>0b001111000111100011110 CNT_31=>0b001111100111110011111 CNT_32=>0b010000001000000100000 CNT_33=>0b010000101000010100001 CNT_34=>0b010001001000100100010 CNT_35=>0b010001101000110100011 CNT_36=>0b010010001001000100100 CNT_37=>0b010010101001010100101 CNT_38=>0b010011001001100100110 CNT_39=>0b010011101001110100111 CNT_40=>0b010100001010000101000 CNT_41=>0b010100010100010101001 CNT_42=>0b0101010001010100101010 CNT_43=>0b0101011010101011010101 CNT_44=>0b010110001011000101100 CNT_45=>0b010110101011010101101 CNT_46=>0b010111001011100101110 CNT_47=>0b010111101011110101111 CNT_48=>0b011000001100000110000 CNT_49=>0b011000101100010110001 CNT_50=>0b011001001100100110010 CNT_51=>0b011001101100110110011 CNT_52=>0b011010001101000110100 CNT_53=>0b011010101101010110101 CNT_54=>0b011011001101100110110 CNT_55=>0b011011101101110110111 CNT_56=>0b011100001110000111000 CNT_57=>0b011100101110010111001 CNT_58=>0b011101001110100111010



Bits	SCOM	Field Mnemonic: Description
41:46	RWX	PB_CFG_FP_HW_MARK: configures the maximum foreign pumps this chip may issue CNT_0=>0b000000000000000000 CNT_1=>0b000001000001000001 CNT_2=>0b000010000010000010 CNT_3=>0b000011000011000011 CNT_4=>0b000100000100000100 CNT_5=>0b000101000101000101 CNT_6=>0b000110000110000110 CNT_7=>0b000111000111000111 CNT_8=>0b001000001000001000 CNT_9=>0b001001001001001001 CNT_10=>0b001010001010001010 CNT_11=>0b001011001011001011 CNT_12=>0b001100001100001100 CNT_13=>0b001101001101001101 CNT_14=>0b001110001110001110 CNT_15=>0b001111001111001111 CNT_16=>0b010000010000010000 CNT_17=>0b010001010001010001 CNT_18=>0b010010010010010010 CNT_19=>0b010011010011010011 CNT_20=>0b010100010100010100 CNT_21=>0b010101010101010101 CNT_22=>0b010110010110010110 CNT_23=>0b010111010111010111 CNT_24=>0b011000011000011000 CNT_25=>0b011001011001011001 CNT_26=>0b011010011010011010 CNT_27=>0b011011011011011011 CNT_28=>0b011100011100011100 CNT_29=>0b011101011101011101 CNT_30=>0b011110011110011110 CNT_31=>0b011111011111011111 CNT_32=>0b100000100000100000

Registers Specification

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Bits	SCOM	Field Mnemonic: Description
47	RWX	Reserved field. (Access type is pb_cfg_east_reset_error_capture) CNT_0=>0b00000000000000000000 CNT_1=>0b00000010000010000001 CNT_2=>0b000010000010000010 CNT_3=>0b000011000011000011 CNT_4=>0b000100000100000100 CNT_5=>0b000101000101000101 CNT_6=>0b000110000110000110 CNT_7=>0b000111000111000111 CNT_8=>0b001000001000001000 CNT_9=>0b001001001001001001 CNT_10=>0b001010001010001010 CNT_11=>0b001011001011001011 CNT_12=>0b001100001100001100 CNT_13=>0b001101001101001101 CNT_14=>0b001110001110001110 CNT_15=>0b001111001111001111 CNT_16=>0b010000010000010000 CNT_17=>0b010001010001010001 CNT_18=>0b010010010010010010 CNT_19=>0b010011010011010011 CNT_20=>0b010100010100010100 CNT_21=>0b010101010101010101 CNT_22=>0b010110010110010110 CNT_23=>0b010111010111010111 CNT_24=>0b011000011000011000 CNT_25=>0b011001011001011001 CNT_26=>0b011010011010011010 CNT_27=>0b011011011011011011 CNT_28=>0b011100011100011100 CNT_29=>0b011101011101011101 CNT_30=>0b011110011110011110 CNT_31=>0b011111011111011111 CNT_32=>0b100000100000100000

Bits	SCOM	Field Mnemonic: Description
48:57	RW	CNT_0=>0b000000000000000000 CNT_1=>0b0000001000001000001 CNT_2=>0b0000010000010000010 CNT_3=>0b0000011000011000011 CNT_4=>0b0000100000100000100 CNT_5=>0b0000101000101000101 CNT_6=>0b0000110000110000110 CNT_7=>0b0000111000111000111 CNT_8=>0b0001000001000001000 CNT_9=>0b0001001001001001001 CNT_10=>0b0001010001010001010 CNT_11=>0b0001011001011001011 CNT_12=>0b0001100001100001100 CNT_13=>0b0001101001101001101 CNT_14=>0b0001110001110001110 CNT_15=>0b0001111001111001111 CNT_16=>0b010000010000010000 CNT_17=>0b010001010001010001 CNT_18=>0b010010010010010010 CNT_19=>0b010011010011010011 CNT_20=>0b010100010100010100 CNT_21=>0b010101010101010101 CNT_22=>0b010110010110010110 CNT_23=>0b010111010111010111 CNT_24=>0b011000011000011000 CNT_25=>0b011001011001011001 CNT_26=>0b011010011010011010 CNT_27=>0b011011011011011011 CNT_28=>0b011100011100011100 CNT_29=>0b011101011101011101 CNT_30=>0b011110011110011110 CNT_31=>0b011111011111011111 CNT_32=>0b100000100000100000
58	RW	PB_CFG_SWITCH_CD_PULSE: Controls switch_cd pulse width. Uses pb_cfg_sw_ab_wait to extend pulse. Default=long pulse. Requires pb_cfg_sw_ab_wait > cnt_5 for 6 cycle pulse. SHORT=>0b111 LONG=>0b000
59	RWX	PB_CFG_SWITCH_OPTION_AB: SCOM access to determine what signal drives pb_cfg_switch_cd. on=tc_pb_switch_ab, off=tc_pb_switch_cd. ON=>0b111 OFF=>0b000
60:62	RWX	PB_CFG_CPU_RATIO_OVERRIDE: Sets rcmd high water mark. 000=16:max hw, 001=12:75% hw, 01x=8:50% hw, 1xx=4:25% hw LVL_0=>0b000000000 LVL_1=>0b001001001 LVL_2=>0b010010010 LVL_3=>0b011011011 LVL_4=>0b100100100 LVL_5=>0b101101101 LVL_6=>0b110110110 LVL_7=>0b111111111

Registers Specification

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Bits	SCOM	Field Mnemonic: Description
63	RW	LVL_0=>0b000000000 LVL_1=>0b001001001 LVL_2=>0b010010010 LVL_3=>0b011011011 LVL_4=>0b100100100 LVL_5=>0b101101101 LVL_6=>0b110110110 LVL_7=>0b111111111

Register Name	<i>Processor Bus PB East HP Mode Configuration Register</i>
Mnemonic	EH.PB.MISC.PB_EAST_HP_MODE_NEXT
Address	0000000002010C8B (SCOM)
Attributes	
Description	00 pb_cfg_east_master_chip 01 pb_cfg_east_link_a0_en 02 pb_cfg_east_link_a1_en 03 pb_cfg_east_link_a2_en 04 pb_cfg_east_na0_addr_dis 05 pb_cfg_east_na1_addr_dis 06 pb_cfg_east_na2_addr_dis 07:09 pb_cfg_east_link_a0_nodeid(0:2) 10:12 pb_cfg_east_link_a1_nodeid(0:2) 13:15 pb_cfg_east_link_a2_nodeid(0:2) 16 pb_cfg_east_a_aggregate 17 pb_cfg_east_tm_grp_master 18 pb_cfg_east_chg_rate_gp_master 19 pb_cfg_east_chg_rate_sp_master 20 pb_cfg_east_pump_mode 21 pb_cfg_east_single_mc 22:23 spare 24:31 pb_cfg_east_a_cmd_rate(0:7) 32 pb_cfg_east_a_gather_enable 33:37 pb_cfg_east_a_dly_cnt(0:4) 38 pb_cfg_east_p0_x8tok 39 pb_cfg_east_p2_x8tok 40 pb_cfg_east_req_gather_enable 41 spare 42 pb_cfg_east_f0_link_master 43 pb_cfg_east_f1_link_master 44 pb_cfg_east_link_f0_en 45 pb_cfg_east_link_f1_en 46 pb_cfg_east_nf0_addr_dis 47 pb_cfg_east_nf1_addr_dis 48:50 pb_cfg_east_link_f0_nodeid(0:2) 51:53 pb_cfg_east_link_f1_nodeid(0:2) 54 spare 55 pb_cfg_east_f_aggregate 56:63 pb_cfg_east_f_cmd_rate(0:7)

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_MASTER_CHIP_NEXT: Processor bus master. ON=>0b111 OFF=>0b000
1	RWX	PB_CFG_LINK_A0_EN_NEXT: Link A0 enabled. ON=>0b111 OFF=>0b000
2	RWX	PB_CFG_LINK_A1_EN_NEXT: Link A1 enabled. ON=>0b111 OFF=>0b000
3	RWX	PB_CFG_LINK_A2_EN_NEXT: Link A2 enabled. ON=>0b111 OFF=>0b000
4	RWX	PB_CFG_LINK_NA0_ADDR_DIS_NEXT: Link A0 address broadcast disabled ON=>0b111 OFF=>0b000



Bits	SCOM	Field Mnemonic: Description
5	RWX	PB_CFG_LINK_NA1_ADDR_DIS_NEXT: Link A1 address broadcast disabled ON=>0b111 OFF=>0b000
6	RWX	PB_CFG_LINK_NA2_ADDR_DIS_NEXT: Link A2 address broadcast disabled ON=>0b111 OFF=>0b000
7:9	RWX	PB_CFG_LINK_A0_NODEID_NEXT: Node ID of chip connected to A0 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
10:12	RWX	PB_CFG_LINK_A1_NODEID_NEXT: Node ID of chip connected to A1 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
13:15	RWX	PB_CFG_LINK_A2_NODEID_NEXT: Node ID of chip connected to A2 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
16	RWX	PB_CFG_A_AGGREGATE_NEXT: Processor bus A links are configured as parallel buses to same chip. ON=>0b111 OFF=>0b000
17	RWX	PB_CFG_TM_MASTER_NEXT: configure Chip as PB TM Master. ON=>0b111 OFF=>0b000

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
18	RWX	PB_CFG_CHG_RATE_GP_MASTER_NEXT: Sets the Group pump change rate master. This master gathers all GP chg_rate.reqs and issues a chg_rate.gnt ON=>0b111 OFF=>0b000
19	RWX	PB_CFG_CHG_RATE_SP_MASTER_NEXT: Sets the System pump change rate master. This master gathers all SP chg_rate.reqs and issues a chg_rate.gnt ON=>0b111 OFF=>0b000
20	RWX	PB_CFG_PUMP_MODE_NEXT: configures whether there are other Processors in the system and if they are part of this node NODAL_IS_CHIP_GROUP_IS_GROUP=>0b000 NODAL_AND_GROUP_IS_GROUP=>0b111
21	RWX	PB_CFG_SINGLE_MC_NEXT: Enables Single MC mode. ON=>0b111 OFF=>0b000
22	RW	PB_CFG_DCACHE_CAPP_MODE_NEXT: Dcache CAPP mode. Combines MC/L4 dcache codepoint for Beyond5Chip locality. ON=>0b111 OFF=>0b000
23	RW	ON=>0b111 OFF=>0b000
24:31	RWX	PB_CFG_A_CMD_RATE_EAST_NEXT: configures the paced command rate to not overrun the A link
32	RWX	PB_CFG_A_GATHER_ENABLE_NEXT: Enable Data OW gathering on A links. ON=>0b111 OFF=>0b000
33:37	RWX	Reserved field. (Access type is pb_cfg_east_a_dly_cnt) ON=>0b111 OFF=>0b000
38	RWX	PB_CFG_P0_X8TOK_NEXT: Configures PHB0 as an 8 token data ramp. 0=PHB0/F0:4OW, 1=P0:8OW and F0:0OW ON=>0b111 OFF=>0b000
39	RWX	PB_CFG_P2_X8TOK_NEXT: Configures PHB2 as an 8 token data ramp. 0=PHB2/F1:4OW, 1=P2:8OW and F1:0OW ON=>0b111 OFF=>0b000



Bits	SCOM	Field Mnemonic: Description
40	RWX	PB_CFG_REQ_GATHER_ENABLE_NEXT: Enable Data OW gathering on all chiplet/link requests. ON=>0b111 OFF=>0b000
41	RW	 ON=>0b111 OFF=>0b000
42	RWX	PB_CFG_F0_LINK_MASTER_EN_NEXT: Link f0 command master enabled. ON=>0b111 OFF=>0b000
43	RWX	PB_CFG_F1_LINK_MASTER_EN_NEXT: Link f1 command master enabled. ON=>0b111 OFF=>0b000
44	RWX	PB_CFG_LINK_F0_EN_NEXT: Link f0 enabled. ON=>0b111 OFF=>0b000
45	RWX	PB_CFG_LINK_F1_EN_NEXT: Link f1 enabled. ON=>0b111 OFF=>0b000
46	RWX	PB_CFG_LINK_NF0_ADDR_DIS_NEXT: Link f0 address broadcast disabled ON=>0b111 OFF=>0b000
47	RWX	PB_CFG_LINK_NF1_ADDR_DIS_NEXT: Link f1 address broadcast disabled ON=>0b111 OFF=>0b000
48:50	RWX	PB_CFG_LINK_F0_NODEID_NEXT: Node ID of chip connected to f0 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
51:53	RWX	PB_CFG_LINK_F1_NODEID_NEXT: Node ID of chip connected to f1 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
54	RW	ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
55	RWX	PB_CFG_F_AGGREGATE_NEXT: Processor bus F links are configured as parallel buses to same chip. ON=>0b111 OFF=>0b000
56:63	RWX	PB_CFG_F_CMD_RATE_EAST_NEXT: configures the paced command rate to not overrun the F link

Register Name	Processor Bus PB EAST HP Mode Configuration Register
Mnemonic	EH.PB.MISC.PB_EAST_HP_MODE_CURR
Address	0000000002010C8C (SCOM)
Attributes	
Description	00 pb_cfg_east_master_chip 01 pb_cfg_east_link_a0_en 02 pb_cfg_east_link_a1_en 03 pb_cfg_east_link_a2_en 04 pb_cfg_east_na0_addr_dis 05 pb_cfg_east_na1_addr_dis 06 pb_cfg_east_na2_addr_dis 07:09 pb_cfg_east_link_a0_nodeid(0:2) 10:12 pb_cfg_east_link_a1_nodeid(0:2) 13:15 pb_cfg_east_link_a2_nodeid(0:2) 16 pb_cfg_east_a_aggregate 17 pb_cfg_east_tm_grp_master 18 pb_cfg_east_chg_rate_gp_master 19 pb_cfg_east_chg_rate_sp_master 20 pb_cfg_east_pump_mode 21 pb_cfg_east_single_mc 22:23 spare 24:31 pb_cfg_east_a_cmd_rate(0:7) 32 pb_cfg_east_a_gather_enable 33:37 pb_cfg_east_a_dly_cnt(0:4) 38 pb_cfg_east_p0_x8tok 39 pb_cfg_east_p2_x8tok 40 pb_cfg_east_req_gather_enable 41 spare 42 pb_cfg_east_f0_link_master 43 pb_cfg_east_f1_link_master 44 pb_cfg_east_link_f0_en 45 pb_cfg_east_link_f1_en 46 pb_cfg_east_nf0_addr_dis 47 pb_cfg_east_nf1_addr_dis 48:50 pb_cfg_east_link_f0_nodeid(0:2) 51:53 pb_cfg_east_link_f1_nodeid(0:2) 54 spare 55 pb_cfg_east_f_aggregate 56:63 pb_cfg_east_f_cmd_rate(0:7)

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_MASTER_CHIP_CURR: Processor bus master. ON=>0b111 OFF=>0b000
1	RWX	PB_CFG_LINK_A0_EN_CURR: Link A0 enabled. ON=>0b111 OFF=>0b000



Bits	SCOM	Field Mnemonic: Description
2	RWX	PB_CFG_LINK_A1_EN_CURR: Link A1 enabled. ON=>0b111 OFF=>0b000
3	RWX	PB_CFG_LINK_A2_EN_CURR: Link A2 enabled. ON=>0b111 OFF=>0b000
4	RWX	PB_CFG_LINK_NA0_ADDR_DIS_CURR: Link A0 address broadcast disabled ON=>0b111 OFF=>0b000
5	RWX	PB_CFG_LINK_NA1_ADDR_DIS_CURR: Link A1 address broadcast disabled ON=>0b111 OFF=>0b000
6	RWX	PB_CFG_LINK_NA2_ADDR_DIS_CURR: Link A2 address broadcast disabled ON=>0b111 OFF=>0b000
7:9	RWX	PB_CFG_LINK_A0_NODEID_CURR: Node ID of chip connected to A0 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
10:12	RWX	PB_CFG_LINK_A1_NODEID_CURR: Node ID of chip connected to A1 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
13:15	RWX	PB_CFG_LINK_A2_NODEID_CURR: Node ID of chip connected to A2 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
16	RWX	PB_CFG_A_AGGREGATE_CURR: Processor bus A links are configured as parallel buses to same chip. ON=>0b111 OFF=>0b000
17	RWX	PB_CFG_TM_MASTER_CURR: configure Chip as PB TM Master. ON=>0b111 OFF=>0b000
18	RWX	PB_CFG_CHG_RATE_GP_MASTER_CURR: Sets the Group pump change rate master. This master gathers all GP chg_rate.reqs and issues a chg_rate.gnt ON=>0b111 OFF=>0b000
19	RWX	PB_CFG_CHG_RATE_SP_MASTER_CURR: Sets the System pump change rate master. This master gathers all SP chg_rate.reqs and issues a chg_rate.gnt ON=>0b111 OFF=>0b000
20	RWX	PB_CFG_PUMP_MODE_CURR: configures whether there are other Processors in the system and if they are part of this node NODAL_IS_CHIP_GROUP_IS_GROUP=>0b000 NODAL_AND_GROUP_IS_GROUP=>0b111
21	RWX	PB_CFG_SINGLE_MC_CURR: Enables Single MC mode. ON=>0b111 OFF=>0b000
22	RW	PB_CFG_DCACHE_CAPP_MODE_CURR: Dcache CAPP mode. Combines MC/L4 dcache codepoint for Beyond5Chip locality. ON=>0b111 OFF=>0b000
23	RW	ON=>0b111 OFF=>0b000
24:31	RWX	PB_CFG_A_CMD_RATE_EAST_CURR: configures the paced command rate to not overrun the A link

Bits	SCOM	Field Mnemonic: Description
32	RWX	PB_CFG_A_GATHER_ENABLE_CURR: Enable Data OW gathering on A links. ON=>0b111 OFF=>0b000
33:37	RWX	Reserved field. (Access type is pb_cfg_east_a_dly_cnt) ON=>0b111 OFF=>0b000
38	RWX	PB_CFG_P0_X8TOK_CURR: Configures PHB0 as an 8 token data ramp. 0=PHB0/F0:4OW, 1=P0:8OW and F0:0OW ON=>0b111 OFF=>0b000
39	RWX	PB_CFG_P2_X8TOK_CURR: Configures PHB2 as an 8 token data ramp. 0=PHB2/F1:4OW, 1=P2:8OW and F1:0OW ON=>0b111 OFF=>0b000
40	RWX	PB_CFG_REQ_GATHER_ENABLE_CURR: Enable Data OW gathering on all chiplet/link requests. ON=>0b111 OFF=>0b000
41	RW	 ON=>0b111 OFF=>0b000
42	RWX	PB_CFG_F0_LINK_MASTER_EN_CURR: Link f0 command master enabled. ON=>0b111 OFF=>0b000
43	RWX	PB_CFG_F1_LINK_MASTER_EN_CURR: Link f1 command master enabled. ON=>0b111 OFF=>0b000
44	RWX	PB_CFG_LINK_F0_EN_CURR: Link f0 enabled. ON=>0b111 OFF=>0b000
45	RWX	PB_CFG_LINK_F1_EN_CURR: Link f1 enabled. ON=>0b111 OFF=>0b000
46	RWX	PB_CFG_LINK_NF0_ADDR_DIS_CURR: Link f0 address broadcast disabled ON=>0b111 OFF=>0b000

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
47	RWX	PB_CFG_LINK_NF1_ADDR_DIS_CURR: Link f1 address broadcast disabled ON=>0b111 OFF=>0b000
48:50	RWX	PB_CFG_LINK_F0_NODEID_CURR: Node ID of chip connected to f0 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
51:53	RWX	PB_CFG_LINK_F1_NODEID_CURR: Node ID of chip connected to f1 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
54	RW	ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
55	RWX	PB_CFG_F_AGGREGATE_CURR: Processor bus F links are configured as parallel buses to same chip. ON=>0b111 OFF=>0b000
56:63	RWX	PB_CFG_F_CMD_RATE_EAST_CURR: Configures the paced command rate to not overrun the F link.



Register Name	Processor Bus PB EAST HP Mode Configuration Register
Mnemonic	EH.PB.MISC.PB_EAST_HPX_MODE_NEXT
Address	0000000002010C8D (SCOM)
Attributes	
Description	00 pb_cfg_east_link_x0_en 01 pb_cfg_east_link_x1_en 02 pb_cfg_east_link_x2_en 03 pb_cfg_east_link_x3_en 04 spare 05 pb_cfg_east_nx0_addr_dis 06 pb_cfg_east_nx1_addr_dis 07 pb_cfg_east_nx2_addr_dis 08 pb_cfg_east_nx3_addr_dis 09 spare 10:12 pb_cfg_east_link_x0_chipid(0:2) 13:15 pb_cfg_east_link_x1_chipid(0:2) 16:18 pb_cfg_east_link_x2_chipid(0:2) 19:21 pb_cfg_east_link_x3_chipid(0:2) 22:24 spare 25 pb_cfg_east_x_aggregate 26 pb_cfg_east_x_indirect_en 27 pb_cfg_east_x_fp_disabled 28:31 spare 32 pb_cfg_east_x_gather_enable 33:37 pb_cfg_east_x_dly_cnt(0:4) 38 pb_cfg_east_x_onnode_12ques 39 spare 40 pb_cfg_east_a0_ind_a1_en 41 pb_cfg_east_a0_ind_a2_en 42 pb_cfg_east_a1_ind_a0_en 43 pb_cfg_east_a1_ind_a2_en 44 pb_cfg_east_a2_ind_a0_en 45 pb_cfg_east_a2_ind_a1_en 46:55 spare 56:63 pb_cfg_east_x_cmd_rate(0:7)

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_LINK_X0_EN_NEXT: Link X0 enabled. ON=>0b111 OFF=>0b000
1	RWX	PB_CFG_LINK_X1_EN_NEXT: Link X1 enabled. ON=>0b111 OFF=>0b000
2	RWX	PB_CFG_LINK_X2_EN_NEXT: Link X2 enabled. ON=>0b111 OFF=>0b000
3	RWX	PB_CFG_LINK_X3_EN_NEXT: Link X3 enabled. ON=>0b111 OFF=>0b000
4	RW	ON=>0b111 OFF=>0b000
5	RWX	PB_CFG_LINK_NX0_ADDR_DIS_NEXT: Link X0 address broadcast disabled ON=>0b111 OFF=>0b000
6	RWX	PB_CFG_LINK_NX1_ADDR_DIS_NEXT: Link X1 address broadcast disabled ON=>0b111 OFF=>0b000
7	RWX	PB_CFG_LINK_NX2_ADDR_DIS_NEXT: Link X2 address broadcast disabled ON=>0b111 OFF=>0b000

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
8	RWX	PB_CFG_LINK_NX3_ADDR_DIS_NEXT: Link X3 address broadcast disabled ON=>0b111 OFF=>0b000
9	RW	ON=>0b111 OFF=>0b000
10:12	RWX	PB_CFG_LINK_X0_CHIPID_NEXT: Chip ID of chip connected to X0 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
13:15	RWX	PB_CFG_LINK_X1_CHIPID_NEXT: Chip ID of chip connected to X1 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
16:18	RWX	PB_CFG_LINK_X2_CHIPID_NEXT: Chip ID of chip connected to X2 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
19:21	RWX	PB_CFG_LINK_X3_CHIPID_NEXT: Chip ID of chip connected to X3 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111



Bits	SCOM	Field Mnemonic: Description
22:24	RW	ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
25	RWX	PB_CFG_X_AGGREGATE_NEXT: Processor bus X links are configured as parallel buses to same chip. ON=>0b111 OFF=>0b000
26	RWX	PB_CFG_X_INDIRECT_EN_NEXT: Processor bus X links are configured for indirect data routing. ON=>0b111 OFF=>0b000
27	RWX	PB_CFG_X_FP_DISABLED_NEXT: Processor bus X link rtag fastpath disable. ON=>0b111 OFF=>0b000
28:31	RW	ON=>0b111 OFF=>0b000
32	RWX	PB_CFG_X_GATHER_ENABLE_NEXT: Enable Data OW gathering on X links. ON=>0b111 OFF=>0b000
33:37	RWX	Reserved field. (Access type is pb_cfg_east_x_dly_cnt) ON=>0b111 OFF=>0b000
38	RWX	PB_CFG_X_ONNODE_12QUES_NEXT: Configures X on group queue depth to 12 OW. 1=12on/4off. 0=8on/8off. ON=>0b111 OFF=>0b000
39	RW	ON=>0b111 OFF=>0b000
40	RWX	PB_CFG_A0_IND_A1_EN_NEXT: Enable Indirect Data routing on secondary A1 link. A0 is primary. ON=>0b111 OFF=>0b000
41	RWX	PB_CFG_A0_IND_A2_EN_NEXT: Enable Indirect Data routing on secondary A2 link. A0 is primary. ON=>0b111 OFF=>0b000

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
42	RWX	PB_CFG_A1_IND_A0_EN_NEXT: Enable Indirect Data routing on secondary A0 link. A1 is primary. ON=>0b111 OFF=>0b000
43	RWX	PB_CFG_A1_IND_A2_EN_NEXT: Enable Indirect Data routing on secondary A2 link. A1 is primary. ON=>0b111 OFF=>0b000
44	RWX	PB_CFG_A2_IND_A0_EN_NEXT: Enable Indirect Data routing on secondary A0 link. A2 is primary. ON=>0b111 OFF=>0b000
45	RWX	PB_CFG_A2_IND_A1_EN_NEXT: Enable Indirect Data routing on secondary A1 link. A2 is primary. ON=>0b111 OFF=>0b000
46:55	RW	ON=>0b111 OFF=>0b000
56:63	RWX	PB_CFG_X_CMD_RATE_EAST_NEXT: configures the paced command rate to not overrun the X link

Register Name	Processor Bus PB EAST HP Mode Configuration Register
Mnemonic	EH.PB.MISC.PB_EAST_HPX_MODE_CURR
Address	0000000002010C8E (SCOM)
Attributes	
Description	00 pb_cfg_east_link_x0_en 01 pb_cfg_east_link_x1_en 02 pb_cfg_east_link_x2_en 03 pb_cfg_east_link_x3_en 04 spare 05 pb_cfg_east_nx0_addr_dis 06 pb_cfg_east_nx1_addr_dis 07 pb_cfg_east_nx2_addr_dis 08 pb_cfg_east_nx3_addr_dis 09 spare 10:12 pb_cfg_east_link_x0_chipid(0:2) 13:15 pb_cfg_east_link_x1_chipid(0:2) 16:18 pb_cfg_east_link_x2_chipid(0:2) 19:21 pb_cfg_east_link_x3_chipid(0:2) 22:24 spare 25 pb_cfg_east_x_aggregate 26 pb_cfg_east_x_indirect_en 27 pb_cfg_east_x_fp_disabled 28:31 spare 32 pb_cfg_east_x_gather_enable 33:37 pb_cfg_east_x_dly_cnt(0:4) 38 pb_cfg_east_x_onnode_12ques 39 spare 40 pb_cfg_east_a0_ind_a1_en 41 pb_cfg_east_a0_ind_a2_en 42 pb_cfg_east_a1_ind_a0_en 43 pb_cfg_east_a1_ind_a2_en 44 pb_cfg_east_a2_ind_a0_en 45 pb_cfg_east_a2_ind_a1_en 46:55 spare 56:63 pb_cfg_east_x_cmd_rate(0:7)

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_LINK_X0_EN_CURR: Link X0 enabled. ON=>0b111 OFF=>0b000
1	RWX	PB_CFG_LINK_X1_EN_CURR: Link X1 enabled. ON=>0b111 OFF=>0b000

Bits	SCOM	Field Mnemonic: Description
2	RWX	PB_CFG_LINK_X2_EN_CURR: Link X2 enabled. ON=>0b111 OFF=>0b000
3	RWX	PB_CFG_LINK_X3_EN_CURR: Link X3 enabled. ON=>0b111 OFF=>0b000
4	RW	 ON=>0b111 OFF=>0b000
5	RWX	PB_CFG_LINK_NX0_ADDR_DIS_CURR: Link X0 address broadcast disabled ON=>0b111 OFF=>0b000
6	RWX	PB_CFG_LINK_NX1_ADDR_DIS_CURR: Link X1 address broadcast disabled ON=>0b111 OFF=>0b000
7	RWX	PB_CFG_LINK_NX2_ADDR_DIS_CURR: Link X2 address broadcast disabled ON=>0b111 OFF=>0b000
8	RWX	PB_CFG_LINK_NX3_ADDR_DIS_CURR: Link X3 address broadcast disabled ON=>0b111 OFF=>0b000
9	RW	 ON=>0b111 OFF=>0b000
10:12	RWX	PB_CFG_LINK_X0_CHIPID_CURR: Chip ID of chip connected to X0 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
13:15	RWX	PB_CFG_LINK_X1_CHIPID_CURR: Chip ID of chip connected to X1 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
16:18	RWX	PB_CFG_LINK_X2_CHIPID_CURR: Chip ID of chip connected to X2 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
19:21	RWX	PB_CFG_LINK_X3_CHIPID_CURR: Chip ID of chip connected to X3 link ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
22:24	RW	ID_0=>0b000000000 ID_1=>0b001001001 ID_2=>0b010010010 ID_3=>0b011011011 ID_4=>0b100100100 ID_5=>0b101101101 ID_6=>0b110110110 ID_7=>0b111111111
25	RWX	PB_CFG_X_AGGREGATE_CURR: Processor bus X links are configured as parallel buses to same chip. ON=>0b111 OFF=>0b000
26	RWX	PB_CFG_X_INDIRECT_EN_CURR: Processor bus X links are configured for indirect data routing. ON=>0b111 OFF=>0b000
27	RWX	PB_CFG_X_FP_DISABLED_CURR: Processor bus X link rtag fastpath disable. ON=>0b111 OFF=>0b000

Bits	SCOM	Field Mnemonic: Description
28:31	RW	ON=>0b111 OFF=>0b000
32	RWX	PB_CFG_X_GATHER_ENABLE_CURR: Enable Data OW gathering on X links. ON=>0b111 OFF=>0b000
33:37	RWX	Reserved field. (Access type is pb_cfg_east_x_dly_cnt) ON=>0b111 OFF=>0b000
38	RWX	PB_CFG_X_ONNODE_12QUES_CURR: Configures X on group queue depth to 12 OW. 1=12on/4off. 0=8on/8off. ON=>0b111 OFF=>0b000
39	RW	ON=>0b111 OFF=>0b000
40	RWX	PB_CFG_A0_IND_A1_EN_CURR: Enable Indirect Data routing on secondary A1 link. A0 is primary. ON=>0b111 OFF=>0b000
41	RWX	PB_CFG_A0_IND_A2_EN_CURR: Enable Indirect Data routing on secondary A2 link. A0 is primary. ON=>0b111 OFF=>0b000
42	RWX	PB_CFG_A1_IND_A0_EN_CURR: Enable Indirect Data routing on secondary A0 link. A1 is primary. ON=>0b111 OFF=>0b000
43	RWX	PB_CFG_A1_IND_A2_EN_CURR: Enable Indirect Data routing on secondary A2 link. A1 is primary. ON=>0b111 OFF=>0b000
44	RWX	PB_CFG_A2_IND_A0_EN_CURR: Enable Indirect Data routing on secondary A0 link. A2 is primary. ON=>0b111 OFF=>0b000
45	RWX	PB_CFG_A2_IND_A1_EN_CURR: Enable Indirect Data routing on secondary A1 link. A2 is primary. ON=>0b111 OFF=>0b000
46:55	RW	ON=>0b111 OFF=>0b000

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Bits	SCOM	Field Mnemonic: Description
56:63	RWX	PB_CFG_X_CMD_RATE_EAST_CURR: configures the paced command rate to not overrun the X link

Register Name	<i>Processor Bus PB EAST FLMCFG0 Register</i>
Mnemonic	EH.PB.MISC.PB_EAST_FLMCFG0
Address	0000000002010C92 (SCOM)
Attributes	
Description	00 = pb_cfg_flmcfg0_valid 01:19 = pb_cfg_flmcfg0_group_size 20:45 = pb_cfg_flmcfg0_base_addr 46:47 = spare

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_FLMCFG0_VALID: configures the Foreign Local Memory BAR for link F0 as valid ON=>0b111 OFF=>0b000
1:19	RWX	PB_CFG_FLMCFG0_GROUP_SIZE_EAST: configures the group size for Foreign Local Memory BAR for link F0 16MB=>0b00000000000000000000 32MB=>0b00000000000000000001 64MB=>0b00000000000000000011 128MB=>0b00000000000000000111 256MB=>0b00000000000000001111 512MB=>0b00000000000000011111 1GB=>0b00000000000000111111 2GB=>0b00000000000001111111 4GB=>0b00000000000011111111 8GB=>0b00000000000111111111 16GB=>0b00000000011111111111 32GB=>0b00000000111111111111 64GB=>0b00000001111111111111 128GB=>0b00000011111111111111 256GB=>0b00000111111111111111 512GB=>0b00001111111111111111 1TB=>0b00011111111111111111 2TB=>0b00111111111111111111 4TB=>0b01111111111111111111 8TB=>0b11111111111111111111
20:45	RWX	PB_CFG_FLMCFG0_BASE_EAST: configures the base address of Foreign Local Memory BAR for link F0
46:47	RW	Reserved field. (Access type is spare)
48:63	RO	Constant = 0b0000000000000000

Register Name	<i>Processor Bus PB EAST FLMCFG1 Register</i>
Mnemonic	EH.PB.MISC.PB_EAST_FLMCFG1
Address	0000000002010C93 (SCOM)
Attributes	
Description	00 = pb_cfg_flmcfg1_valid 01:19 = pb_cfg_flmcfg1_group_size 20:45 = pb_cfg_flmcfg1_base_addr 46:47 = spare



Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_FLMCFG1_VALID: configures the Foreign Local Memory BAR for link F1 as valid ON=>0b111 OFF=>0b000
1:19	RWX	PB_CFG_FLMCFG1_GROUP_SIZE_EAST: configures the group size for Foreign Local Memory BAR for link F1 16MB=>0b00000000000000000000 32MB=>0b00000000000000000001 64MB=>0b00000000000000000011 128MB=>0b00000000000000000111 256MB=>0b00000000000000001111 512MB=>0b00000000000000011111 1GB=>0b00000000000001111111 2GB=>0b00000000000011111111 4GB=>0b00000000000111111111 8GB=>0b00000000011111111111 16GB=>0b00000000111111111111 32GB=>0b00000001111111111111 64GB=>0b00000011111111111111 128GB=>0b00000111111111111111 256GB=>0b00001111111111111111 512GB=>0b00011111111111111111 1TB=>0b00111111111111111111 2TB=>0b01111111111111111111 4TB=>0b11111111111111111111 8TB=>0b11111111111111111111
20:45	RWX	PB_CFG_FLMCFG1_BASE_EAST: configures the base address of Foreign Local Memory BAR for link F1
46:47	RW	Reserved field. (Access type is spare)
48:63	RO	Constant = 0b0000000000000000

Register Name	<i>Processor Bus PB EAST FLMCFGM0 Register</i>
Mnemonic	EH.PB.MISC.PB_EAST_FLMCFGM0
Address	000000002010C94 (SCOM)
Attributes	
Description	00 = pb_cfg_flmcfgm0_valid 01:19 = pb_cfg_flmcfgm0_group_size 20:45 = pb_cfg_flmcfgm0_base_addr 46:47 = spare

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_FFMCFG0_VALID: configures the Foreign Far Memory BAR for link F0 as valid ON=>0b111 OFF=>0b000

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Bits	SCOM	Field Mnemonic: Description
1:19	RWX	PB_CFG_FFMCFG0_GROUP_SIZE_EAST: configures the group size for Foreign Far Memory BAR for link F0 16MB=>0b00000000000000000000 32MB=>0b00000000000000000001 64MB=>0b00000000000000000011 128MB=>0b00000000000000000111 256MB=>0b00000000000000001111 512MB=>0b00000000000000011111 1GB=>0b00000000000001111111 2GB=>0b00000000000011111111 4GB=>0b00000000001111111111 8GB=>0b00000000111111111111 16GB=>0b00000001111111111111 32GB=>0b00000011111111111111 64GB=>0b00000111111111111111 128GB=>0b00001111111111111111 256GB=>0b00011111111111111111 512GB=>0b00111111111111111111 1TB=>0b00111111111111111111 2TB=>0b01111111111111111111 4TB=>0b11111111111111111111 8TB=>0b11111111111111111111
20:45	RWX	PB_CFG_FFMCFG0_BASE_EAST: configures the base address of Foreign Far Memory BAR for link F0
46:47	RW	Reserved field. (Access type is spare)
48:63	RO	Constant = 0b0000000000000000

Register Name	<i>Processor Bus PB EAST FLMCFG1 Register</i>
Mnemonic	EH.PB.MISC.PB_EAST_FLMCFG1
Address	000000002010C95 (SCOM)
Attributes	
Description	00 = pb_cfg_flmcfgm1_valid 01:19 = pb_cfg_flmcfgm1_group_size 20:45 = pb_cfg_flmcfgm1_base_addr 46:47 = spare

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_FFMCFG1_VALID: configures the Foreign Far Memory BAR for link F1 as valid ON=>0b111 OFF=>0b000



Bits	SCOM	Field Mnemonic: Description
1:19	RWX	PB_CFG_FFMCFG1_GROUP_SIZE_EAST: configures the group size for Foreign Far Memory BAR for link F1 16MB=>0b00000000000000000000 32MB=>0b00000000000000000001 64MB=>0b00000000000000000011 128MB=>0b00000000000000000111 256MB=>0b00000000000000001111 512MB=>0b00000000000000011111 1GB=>0b00000000000001111111 2GB=>0b00000000000011111111 4GB=>0b00000000001111111111 8GB=>0b00000000111111111111 16GB=>0b00000001111111111111 32GB=>0b00000011111111111111 64GB=>0b00000111111111111111 128GB=>0b00001111111111111111 256GB=>0b00011111111111111111 512GB=>0b00111111111111111111 1TB=>0b00111111111111111111 2TB=>0b01111111111111111111 4TB=>0b11111111111111111111 8TB=>0b11111111111111111111
20:45	RWX	PB_CFG_FFMCFG1_BASE_EAST: configures the base address of Foreign Far Memory BAR for link F1
46:47	RW	Reserved field. (Access type is spare)
48:63	RO	Constant = 0b0000000000000000

Register Name	<i>Processor Bus PB EAST EVENT COMPB Register</i>
Mnemonic	EH.PB.MISC.PB_EAST_SCONFIG_LOAD
Address	000000002010C96 (SCOM)
Attributes	
Description	00 = pb_cfg_sconfig_load 01 = pb_cfg_sconfig_slow 02:07 = pb_cfg_sconfig_shift_count 08:11 = pb_cfg_sconfig_select 12:63 = pb_cfg_sconfig_shift_data

Bits	SCOM	Field Mnemonic: Description
0	WOX	PB_CFG_EAST_SCONFIG_LOAD: Load Serial Mode Registers
1	RWX	PB_CFG_EAST_SCONFIG_SLOW: Set Load of Serial Mode Registers to 16:1 slow clock
2:7	WOX	PB_CFG_EAST_SCONFIG_SHIFT_COUNT: Configures length of Serial Mode Register

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Bits	SCOM	Field Mnemonic: Description
8:11	RWX	PB_CFG_EAST_SCONFIG_SELECT: Select Serial Mode register: 0000=pbh_pbiex_ah, 0001=pbh_pbiex_ex, 0010=pbh_dat_ex_req_pmac, 0011=pbh_dat_em_req_pmac, 0100=pbh_dat_arb_ex_pmac, 0101=pbh_dat_arb_em_pmac SEL_0=>0b0000 SEL_1=>0b0001 SEL_2=>0b0010 SEL_3=>0b0011 SEL_4=>0b0100 SEL_5=>0b0101 SEL_6=>0b0110 SEL_7=>0b0111 SEL_8=>0b1000 SEL_9=>0b1001 SEL_10=>0b1010 SEL_11=>0b1011 SEL_12=>0b1100 SEL_13=>0b1101 SEL_14=>0b1110 SEL_15=>0b1111
12:63	RWX	PB_CFG_EAST_SCONFIG_SHIFT_DATA: Serial Mode Register Data

Register Name	Processor Bus PB CENT Trace Config Register
Mnemonic	EH.PB.MISC.PB_CENT_TRACE
Address	0000000002010C4F (SCOM)
Attributes	
Description	00:01 pb_cfg_trace_sel0(0:1) 02:03 pb_cfg_trace_sel1(0:1) 04:05 pb_cfg_trace_sel2(0:1) 06:07 pb_cfg_trace_sel3(0:1) 08:09 pb_cfg_trace_sel4(0:1) 10:12 pb_cfg_trace_sel5(0:2) 13:18 pb_cfg_trace_sel6(0:5) 19:31 spare 32 = Enable perfttrace mode and enable the perfttrace trigger function to send a trigger to EH, EN and ES. (trigger can be ignored at the trace arrays) 33 = 1=perfttrace trigger has fired. Resets to 0 when the PMU counter is reset. Can also be written to 1 to induce a trigger. 34:35 = Perfttrace counter select. PMU_group0_counter# will be compared against the pb_cfg_perfttrace_counter_match field to generate a perfttrace trigger. 36:51 = Perfttrace counter match. When the selected counter matches these bits, a perfttrace trigger is generated. 52 = Enable_perfttrace_prescale - wide-angle view - perftcounts are prescaled by 128 53 = perfttrace fixed window mode - take a perfttrace sample every 255 or 255x128 cycles 54 = 0=event_bus(8:11) routed to perfttrace counters 0:3 1=event_bus(12:15) routed to perfttrace counters 0:3 55 = 0=event_bus(16:19) routed to perfttrace counters 4:7 1=event_bus(20:23) routed to perfttrace counters 4:7 56:58 = PMU event compare A - scope mask 59:61 = PMU event compare B - scope mask 62:63 spare

Bits	SCOM	Field Mnemonic: Description
0:1	RW	PB_CFG_TRACE_SEL0: configures PB Trace SN0 inputs; 10=rcmd0{por}, 01=rsvd, 00=none PB_TRACE_SN0_NONE_SEL=>0b00 PB_TRACE_SN0_B_SEL=>0b01 PB_TRACE_SN0_A_SEL=>0b10
2:3	RW	PB_CFG_TRACE_SEL1: configures PB Trace SN1 inputs; 10=rcmd1{por}, 01=rsvd, 00=none PB_TRACE_SN1_NONE_SEL=>0b00 PB_TRACE_SN1_B_SEL=>0b01 PB_TRACE_SN1_A_SEL=>0b10

Bits	SCOM	Field Mnemonic: Description
4:5	RW	PB_CFG_TRACE_SELCR0: configures PB Trace CR0 inputs; 10=crsp0{por}, 01=atag/data, 00=none PB_TRACE_CR0_NONE_SEL=>0b00 PB_TRACE_CR0_B_SEL=>0b01 PB_TRACE_CR0_A_SEL=>0b10
6:7	RW	PB_CFG_TRACE_SELCR1: configures PB Trace CR1 inputs; 10=crsp1{por}, 01=atag, 00=none PB_TRACE_CR1_NONE_SEL=>0b00 PB_TRACE_CR1_B_SEL=>0b01 PB_TRACE_CR1_A_SEL=>0b10
8:9	RW	PB_CFG_TRACE_SELRT0: configures PB Trace RT0 inputs; 10=busn0{por}, 01=buss0, 00=none PB_TRACE_RT0_NONE_SEL=>0b00 PB_TRACE_RT0_B_SEL=>0b01 PB_TRACE_RT0_A_SEL=>0b10
10:12	RW	PB_CFG_TRACE_SELRT1: configures PB Trace RT1 inputs; 100=busn1, 010=buss1, 001=MCD {por}, 000=none PB_TRACE_RT1_NONE_SEL=>0b000 PB_TRACE_RT1_C_SEL=>0b001 PB_TRACE_RT1_B_SEL=>0b010 PB_TRACE_RT1_A_SEL=>0b100
13:18	RW	PB_CFG_TRACE_SELD: configures PB Trace CR0 data inputs; default=none PB_TRACE_D_NONE_SEL=>0b000000 PB_TRACE_D_X0_SEL=>0b100000 PB_TRACE_D_X1_SEL=>0b100001 PB_TRACE_D_X2_SEL=>0b100010 PB_TRACE_D_X3_SEL=>0b100011 PB_TRACE_D_TP_SEL=>0b100100 PB_TRACE_D_NX_SEL=>0b100101 PB_TRACE_D_X3ON_SEL=>0b100110 PB_TRACE_D_X0NX_SEL=>0b101000 PB_TRACE_D_X1X3_SEL=>0b101001 PB_TRACE_D_X2TP_SEL=>0b101010 PB_TRACE_D_X0ON_SEL=>0b101100 PB_TRACE_D_X1ON_SEL=>0b101101 PB_TRACE_D_X2ON_SEL=>0b101110 PB_TRACE_D_A_SEL=>0b110000 PB_TRACE_D_F0_SEL=>0b110010 PB_TRACE_D_F1_SEL=>0b110011 PB_TRACE_D_P0_SEL=>0b110100 PB_TRACE_D_P1_SEL=>0b110101 PB_TRACE_D_P2_SEL=>0b110110 PB_TRACE_D_A0P2_SEL=>0b111000 PB_TRACE_D_A1P1_SEL=>0b111001 PB_TRACE_D_A2P0_SEL=>0b111010 PB_TRACE_D_A0ON_SEL=>0b111100 PB_TRACE_D_A1ON_SEL=>0b111101 PB_TRACE_D_A2ON_SEL=>0b111110

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Bits	SCOM	Field Mnemonic: Description
19:31	RW	PB_TRACE_D_NONE_SEL=>0b000000 PB_TRACE_D_X0_SEL=>0b100000 PB_TRACE_D_X1_SEL=>0b100001 PB_TRACE_D_X2_SEL=>0b100010 PB_TRACE_D_X3_SEL=>0b100011 PB_TRACE_D_TP_SEL=>0b100100 PB_TRACE_D_NX_SEL=>0b100101 PB_TRACE_D_X3ON_SEL=>0b100110 PB_TRACE_D_X0NX_SEL=>0b101000 PB_TRACE_D_X1X3_SEL=>0b101001 PB_TRACE_D_X2TP_SEL=>0b101010 PB_TRACE_D_X0ON_SEL=>0b101100 PB_TRACE_D_X1ON_SEL=>0b101101 PB_TRACE_D_X2ON_SEL=>0b101110 PB_TRACE_D_A_SEL=>0b110000 PB_TRACE_D_F0_SEL=>0b110010 PB_TRACE_D_F1_SEL=>0b110011 PB_TRACE_D_P0_SEL=>0b110100 PB_TRACE_D_P1_SEL=>0b110101 PB_TRACE_D_P2_SEL=>0b110110 PB_TRACE_D_A0P2_SEL=>0b111000 PB_TRACE_D_A1P1_SEL=>0b111001 PB_TRACE_D_A2P0_SEL=>0b111010 PB_TRACE_D_A0ON_SEL=>0b111100 PB_TRACE_D_A1ON_SEL=>0b111101 PB_TRACE_D_A2ON_SEL=>0b111110
32	RW	PB_CFG_PERFTRACE_EN: Enable the perftrace trigger function to send a trigger to EN and ES.
33	RWX	PB_CFG_PERFTRACE_TRIG: 1=perftrace trigger has fired. Resets to 0 when the PMU counter is reset. Can also be written to 1 to induce a trigger.
34:35	RW	PB_CFG_PERFTRACE_COUNTER_SEL: Perftrace counter select. PMU_group0_counter# will be compared against the pb_cfg_perftrace_counter_match field to generate a perftrace trigger.
36:51	RW	PB_CFG_PERFTRACE_COUNTER_MATCH: Perftrace counter match. When the selected counter matches these bits, a perftrace trigger is generated.
52	RW	PB_CFG_ENABLE_PERFTRACE_PRESCALE: Enable_perftrace_prescale - wide-angle view - perfcunts are prescaled by 128
53	RW	PB_CFG_ENABLE_PERFTRACE_FIXED_WIN: perftrace fixed window mode - take a perftrace sample every 255 or 255x128 cycles
54	RW	PB_CFG_PERFTRACE_GRP1_SEL: 0=event_bus(8:11) routed to pertrace counters 0:3. 1=event_bus(12:15) routed to pertrace counters 0:3
55	RW	PB_CFG_PERFTRACE_GRP2_SEL: 0=event_bus(16:19) routed to pertrace counters 4:7. 1=event_bus(20:23) routed to pertrace counters 4:7
56:58	RW	PB_CFG_EVENT_COMPA_SCOPE_MASK: PMU event compare A - scope mask
59:61	RW	PB_CFG_EVENT_COMPB_SCOPE_MASK: PMU event compare B - scope mask
62:63	RW	



Register Name	Processor Bus PB CENT NMPM Counter Register
Mnemonic	EH.PB.MISC.PB_CENT_NMPM_COUNTER
Address	0000000002010C50 (SCOM)
Attributes	
Description	00 pb_cfg_apm_en 01:02 pb_cfg_sample_sel(0:1) 03 pb_cfg_pmucnt_en 04:05 pb_cfg_pmucnt_sel(0:1) 06 pb_cfg_nm_hi_comp_lsb 07 pb_cfg_nm_lo_comp_lsb 08:11 pb_cfg_nm_hi_comp(0:3) 12:15 pb_cfg_nm_lo_comp(0:3) 16:39 pb_apm_nm_lo_cnt(0:23) 40:63 pb_apm_nm_hi_cnt(0:23)

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_APM_ENABLE: Enable Advanced Power Management Counters
1:2	RWX	PB_CFG_APM_SAMPLE_SEL: configures APM sample period SEL_0=>0b00 SEL_1=>0b01 SEL_2=>0b10 SEL_3=>0b11
3	RWX	PB_CFG_PMUCNT_EN: Enable Performance Monitor Counters
4:5	RWX	PB_CFG_PMUCNT_SEL: configures Performance Monitor inputs. SEL_0=>0b00 SEL_1=>0b01 SEL_2=>0b10 SEL_3=>0b11
6	RWX	PB_CFG_APM_NM_HI_COMP: configures APM NM hi compare SEL_0=>0b00000 SEL_0_1=>0b00001 SEL_1=>0b00010 SEL_1_1=>0b00011 SEL_2=>0b00100 SEL_2_1=>0b00101 SEL_3=>0b00110 SEL_3_1=>0b00111 SEL_4=>0b01000 SEL_4_1=>0b01001 SEL_5=>0b01010 SEL_5_1=>0b01011 SEL_6=>0b01100 SEL_6_1=>0b01101 SEL_7=>0b01110 SEL_7_1=>0b01111 SEL_8=>0b10000 SEL_8_1=>0b10001 SEL_9=>0b10010 SEL_9_1=>0b10011 SEL_10=>0b10100 SEL_10_1=>0b10101 SEL_11=>0b10110 SEL_11_1=>0b10111 SEL_12=>0b11000 SEL_12_1=>0b11001 SEL_13=>0b11010 SEL_13_1=>0b11011 SEL_14=>0b11100 SEL_14_1=>0b11101 SEL_15=>0b11110 SEL_15_1=>0b11111

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Bits	SCOM	Field Mnemonic: Description
7	RWX	PB_CFG_APM_NM_LO_COMP: configures APM NM lo compare SEL_0=>0b00000 SEL_0_1=>0b00001 SEL_1=>0b00010 SEL_1_1=>0b00011 SEL_2=>0b00100 SEL_2_1=>0b00101 SEL_3=>0b00110 SEL_3_1=>0b00111 SEL_4=>0b01000 SEL_4_1=>0b01001 SEL_5=>0b01010 SEL_5_1=>0b01011 SEL_6=>0b01100 SEL_6_1=>0b01101 SEL_7=>0b01110 SEL_7_1=>0b01111 SEL_8=>0b10000 SEL_8_1=>0b10001 SEL_9=>0b10010 SEL_9_1=>0b10011 SEL_10=>0b10100 SEL_10_1=>0b10101 SEL_11=>0b10110 SEL_11_1=>0b10111 SEL_12=>0b11000 SEL_12_1=>0b11001 SEL_13=>0b11010 SEL_13_1=>0b11011 SEL_14=>0b11100 SEL_14_1=>0b11101 SEL_15=>0b11110 SEL_15_1=>0b11111



Bits	SCOM	Field Mnemonic: Description
8:11	RWX	PB_CFG_APM_NM_HI_COMP: configures APM NM hi compare SEL_0=>0b00000 SEL_0_1=>0b00001 SEL_1=>0b00010 SEL_1_1=>0b00011 SEL_2=>0b00100 SEL_2_1=>0b00101 SEL_3=>0b00110 SEL_3_1=>0b00111 SEL_4=>0b01000 SEL_4_1=>0b01001 SEL_5=>0b01010 SEL_5_1=>0b01011 SEL_6=>0b01100 SEL_6_1=>0b01101 SEL_7=>0b01110 SEL_7_1=>0b01111 SEL_8=>0b10000 SEL_8_1=>0b10001 SEL_9=>0b10010 SEL_9_1=>0b10011 SEL_10=>0b10100 SEL_10_1=>0b10101 SEL_11=>0b10110 SEL_11_1=>0b10111 SEL_12=>0b11000 SEL_12_1=>0b11001 SEL_13=>0b11010 SEL_13_1=>0b11011 SEL_14=>0b11100 SEL_14_1=>0b11101 SEL_15=>0b11110 SEL_15_1=>0b11111

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Bits	SCOM	Field Mnemonic: Description
12:15	RWX	PB_CFG_APM_NM_LO_COMP: configures APM NM lo compare SEL_0=>0b00000 SEL_0_1=>0b00001 SEL_1=>0b00010 SEL_1_1=>0b00011 SEL_2=>0b00100 SEL_2_1=>0b00101 SEL_3=>0b00110 SEL_3_1=>0b00111 SEL_4=>0b01000 SEL_4_1=>0b01001 SEL_5=>0b01010 SEL_5_1=>0b01011 SEL_6=>0b01100 SEL_6_1=>0b01101 SEL_7=>0b01110 SEL_7_1=>0b01111 SEL_8=>0b10000 SEL_8_1=>0b10001 SEL_9=>0b10010 SEL_9_1=>0b10011 SEL_10=>0b10100 SEL_10_1=>0b10101 SEL_11=>0b10110 SEL_11_1=>0b10111 SEL_12=>0b11000 SEL_12_1=>0b11001 SEL_13=>0b11010 SEL_13_1=>0b11011 SEL_14=>0b11100 SEL_14_1=>0b11101 SEL_15=>0b11110 SEL_15_1=>0b11111



Bits	SCOM	Field Mnemonic: Description
16:39	ROX	Reserved field. (Access type is pb_apm_nm_lo_cnt) SEL_0=>0b00000 SEL_0_1=>0b00001 SEL_1=>0b00010 SEL_1_1=>0b00011 SEL_2=>0b00100 SEL_2_1=>0b00101 SEL_3=>0b00110 SEL_3_1=>0b00111 SEL_4=>0b01000 SEL_4_1=>0b01001 SEL_5=>0b01010 SEL_5_1=>0b01011 SEL_6=>0b01100 SEL_6_1=>0b01101 SEL_7=>0b01110 SEL_7_1=>0b01111 SEL_8=>0b10000 SEL_8_1=>0b10001 SEL_9=>0b10010 SEL_9_1=>0b10011 SEL_10=>0b10100 SEL_10_1=>0b10101 SEL_11=>0b10110 SEL_11_1=>0b10111 SEL_12=>0b11000 SEL_12_1=>0b11001 SEL_13=>0b11010 SEL_13_1=>0b11011 SEL_14=>0b11100 SEL_14_1=>0b11101 SEL_15=>0b11110 SEL_15_1=>0b11111

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Bits	SCOM	Field Mnemonic: Description
40:63	ROX	Reserved field. (Access type is pb_apm_nm_hi_cnt) SEL_0=>0b00000 SEL_0_1=>0b00001 SEL_1=>0b00010 SEL_1_1=>0b00011 SEL_2=>0b00100 SEL_2_1=>0b00101 SEL_3=>0b00110 SEL_3_1=>0b00111 SEL_4=>0b01000 SEL_4_1=>0b01001 SEL_5=>0b01010 SEL_5_1=>0b01011 SEL_6=>0b01100 SEL_6_1=>0b01101 SEL_7=>0b01110 SEL_7_1=>0b01111 SEL_8=>0b10000 SEL_8_1=>0b10001 SEL_9=>0b10010 SEL_9_1=>0b10011 SEL_10=>0b10100 SEL_10_1=>0b10101 SEL_11=>0b10110 SEL_11_1=>0b10111 SEL_12=>0b11000 SEL_12_1=>0b11001 SEL_13=>0b11010 SEL_13_1=>0b11011 SEL_14=>0b11100 SEL_14_1=>0b11101 SEL_15=>0b11110 SEL_15_1=>0b11111

Register Name	<i>Processor Bus PB CENT LMPM Counter Register</i>
Mnemonic	EH.PB.MISC.PB_CENT_LMPM_COUNTER
Address	0000000002010C51 (SCOM)
Attributes	
Description	00:05 spare 06 pb_cfg_lm_hi_comp_lsb 07 pb_cfg_lm_lo_comp_lsb 08:11 pb_cfg_lm_hi_comp(0:3) 12:15 pb_cfg_lm_lo_comp(0:3) 16:39 pb_apm_lm_lo_cnt(0:23) 40:63 pb_apm_lm_hi_cnt(0:23)

Bits	SCOM	Field Mnemonic: Description
0	RW	PB_CFG_APM_DD1_MODE: configures APM counters for DD1 mode
1:2	RW	PB_CFG_APM_SEL: configures APM scopes SEL_0=>0b00 SEL_1=>0b01 SEL_2=>0b10 SEL_3=>0b11



Bits	SCOM	Field Mnemonic: Description
3:5	RW	SEL_0=>0b00 SEL_1=>0b01 SEL_2=>0b10 SEL_3=>0b11
6	RWX	PB_CFG_APM_LM_HI_COMP: configures APM LM hi compare SEL_0=>0b00000 SEL_0_1=>0b00001 SEL_1=>0b00010 SEL_1_1=>0b00011 SEL_2=>0b00100 SEL_2_1=>0b00101 SEL_3=>0b00110 SEL_3_1=>0b00111 SEL_4=>0b01000 SEL_4_1=>0b01001 SEL_5=>0b01010 SEL_5_1=>0b01011 SEL_6=>0b01100 SEL_6_1=>0b01101 SEL_7=>0b01110 SEL_7_1=>0b01111 SEL_8=>0b10000 SEL_8_1=>0b10001 SEL_9=>0b10010 SEL_9_1=>0b10011 SEL_10=>0b10100 SEL_10_1=>0b10101 SEL_11=>0b10110 SEL_11_1=>0b10111 SEL_12=>0b11000 SEL_12_1=>0b11001 SEL_13=>0b11010 SEL_13_1=>0b11011 SEL_14=>0b11100 SEL_14_1=>0b11101 SEL_15=>0b11110 SEL_15_1=>0b11111

Registers Specification

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Bits	SCOM	Field Mnemonic: Description
7	RWX	PB_CFG_APM_LM_LO_COMP: configures APM LM lo compare SEL_0=>0b00000 SEL_0_1=>0b00001 SEL_1=>0b00010 SEL_1_1=>0b00011 SEL_2=>0b00100 SEL_2_1=>0b00101 SEL_3=>0b00110 SEL_3_1=>0b00111 SEL_4=>0b01000 SEL_4_1=>0b01001 SEL_5=>0b01010 SEL_5_1=>0b01011 SEL_6=>0b01100 SEL_6_1=>0b01101 SEL_7=>0b01110 SEL_7_1=>0b01111 SEL_8=>0b10000 SEL_8_1=>0b10001 SEL_9=>0b10010 SEL_9_1=>0b10011 SEL_10=>0b10100 SEL_10_1=>0b10101 SEL_11=>0b10110 SEL_11_1=>0b10111 SEL_12=>0b11000 SEL_12_1=>0b11001 SEL_13=>0b11010 SEL_13_1=>0b11011 SEL_14=>0b11100 SEL_14_1=>0b11101 SEL_15=>0b11110 SEL_15_1=>0b11111



Bits	SCOM	Field Mnemonic: Description
8:11	RWX	PB_CFG_APM_LM_HI_COMP: configures APM LM hi compare SEL_0=>0b00000 SEL_0_1=>0b00001 SEL_1=>0b00010 SEL_1_1=>0b00011 SEL_2=>0b00100 SEL_2_1=>0b00101 SEL_3=>0b00110 SEL_3_1=>0b00111 SEL_4=>0b01000 SEL_4_1=>0b01001 SEL_5=>0b01010 SEL_5_1=>0b01011 SEL_6=>0b01100 SEL_6_1=>0b01101 SEL_7=>0b01110 SEL_7_1=>0b01111 SEL_8=>0b10000 SEL_8_1=>0b10001 SEL_9=>0b10010 SEL_9_1=>0b10011 SEL_10=>0b10100 SEL_10_1=>0b10101 SEL_11=>0b10110 SEL_11_1=>0b10111 SEL_12=>0b11000 SEL_12_1=>0b11001 SEL_13=>0b11010 SEL_13_1=>0b11011 SEL_14=>0b11100 SEL_14_1=>0b11101 SEL_15=>0b11110 SEL_15_1=>0b11111

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
12:15	RWX	PB_CFG_APM_LM_LO_COMP: configures APM LM lo compare SEL_0=>0b00000 SEL_0_1=>0b00001 SEL_1=>0b00010 SEL_1_1=>0b00011 SEL_2=>0b00100 SEL_2_1=>0b00101 SEL_3=>0b00110 SEL_3_1=>0b00111 SEL_4=>0b01000 SEL_4_1=>0b01001 SEL_5=>0b01010 SEL_5_1=>0b01011 SEL_6=>0b01100 SEL_6_1=>0b01101 SEL_7=>0b01110 SEL_7_1=>0b01111 SEL_8=>0b10000 SEL_8_1=>0b10001 SEL_9=>0b10010 SEL_9_1=>0b10011 SEL_10=>0b10100 SEL_10_1=>0b10101 SEL_11=>0b10110 SEL_11_1=>0b10111 SEL_12=>0b11000 SEL_12_1=>0b11001 SEL_13=>0b11010 SEL_13_1=>0b11011 SEL_14=>0b11100 SEL_14_1=>0b11101 SEL_15=>0b11110 SEL_15_1=>0b11111



Bits	SCOM	Field Mnemonic: Description
16:39	ROX	Reserved field. (Access type is pb_apm_lm_lo_cnt) SEL_0=>0b00000 SEL_0_1=>0b00001 SEL_1=>0b00010 SEL_1_1=>0b00011 SEL_2=>0b00100 SEL_2_1=>0b00101 SEL_3=>0b00110 SEL_3_1=>0b00111 SEL_4=>0b01000 SEL_4_1=>0b01001 SEL_5=>0b01010 SEL_5_1=>0b01011 SEL_6=>0b01100 SEL_6_1=>0b01101 SEL_7=>0b01110 SEL_7_1=>0b01111 SEL_8=>0b10000 SEL_8_1=>0b10001 SEL_9=>0b10010 SEL_9_1=>0b10011 SEL_10=>0b10100 SEL_10_1=>0b10101 SEL_11=>0b10110 SEL_11_1=>0b10111 SEL_12=>0b11000 SEL_12_1=>0b11001 SEL_13=>0b11010 SEL_13_1=>0b11011 SEL_14=>0b11100 SEL_14_1=>0b11101 SEL_15=>0b11110 SEL_15_1=>0b11111

Registers Specification

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Bits	SCOM	Field Mnemonic: Description
40:63	ROX	Reserved field. (Access type is pb_apm_lm_hi_cnt) SEL_0=>0b00000 SEL_0_1=>0b00001 SEL_1=>0b00010 SEL_1_1=>0b00011 SEL_2=>0b00100 SEL_2_1=>0b00101 SEL_3=>0b00110 SEL_3_1=>0b00111 SEL_4=>0b01000 SEL_4_1=>0b01001 SEL_5=>0b01010 SEL_5_1=>0b01011 SEL_6=>0b01100 SEL_6_1=>0b01101 SEL_7=>0b01110 SEL_7_1=>0b01111 SEL_8=>0b10000 SEL_8_1=>0b10001 SEL_9=>0b10010 SEL_9_1=>0b10011 SEL_10=>0b10100 SEL_10_1=>0b10101 SEL_11=>0b10110 SEL_11_1=>0b10111 SEL_12=>0b11000 SEL_12_1=>0b11001 SEL_13=>0b11010 SEL_13_1=>0b11011 SEL_14=>0b11100 SEL_14_1=>0b11101 SEL_15=>0b11110 SEL_15_1=>0b11111

Register Name		Processor Bus PB CENT RCMD INTDAT Counter Register
Mnemonic		EH.PB.MISC.PB_CENT_RCMD_INTDAT_COUNTER
Address		0000000002010C52 (SCOM)
Attributes		
Description		00:31 pb_apm_rcmd_cnt(0:31) 32:63 pb_apm_intdata_cnt(0:31)
Bits	SCOM	Field Mnemonic: Description
0:31	RWX_WCLRR EG	Reserved field. (Access type is pb_apm_rcmd_cnt)
32:63	RWX_WCLRR EG	Reserved field. (Access type is pb_apm_intdata_cnt)

Register Name		Processor Bus PB CENT EXTDAT Counter Register
Mnemonic		EH.PB.MISC.PB_CENT_EXTDAT_COUNTER
Address		0000000002010C53 (SCOM)
Attributes		
Description		00:31 pb_apm_extdatasnd_cnt(0:31) 32:63 pb_apm_extdatarcv_cnt(0:31)



Bits	SCOM	Field Mnemonic: Description
0:31	RWX_WCLRR EG	Reserved field. (Access type is pb_apm_extdatasnd_cnt)
32:63	RWX_WCLRR EG	Reserved field. (Access type is pb_apm_extdatarcv_cnt)

Register Name	<i>Processor Bus PB CENT PMU0 Counter Register</i>
Mnemonic	EH.PB.PB_CENT_PMU0_COUNTER
Address	0000000002010C54 (SCOM)
Attributes	
Description	00:15 pbh_event_grp0_counter0(0:15) 16:31 pbh_event_grp0_counter1(0:15) 32:47 pbh_event_grp0_counter2(0:15) 48:63 pbh_event_grp0_counter3(0:31)

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRR EG	Reserved field. (Access type is pbh_event_grp0_counter0)
16:31	RWX_WCLRR EG	Reserved field. (Access type is pbh_event_grp0_counter1)
32:47	RWX_WCLRR EG	Reserved field. (Access type is pbh_event_grp0_counter2)
48:63	RWX_WCLRR EG	Reserved field. (Access type is pbh_event_grp0_counter3)

Register Name	<i>Processor Bus PB CENT PMU1 Counter Register</i>
Mnemonic	EH.PB.PB_CENT_PMU1_COUNTER
Address	0000000002010C55 (SCOM)
Attributes	
Description	00:15 pbh_event_grp1_counter0(0:15) 16:31 pbh_event_grp1_counter1(0:15) 32:47 pbh_event_grp1_counter2(0:15) 48:63 pbh_event_grp1_counter3(0:31)

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRR EG	Reserved field. (Access type is pbh_event_grp1_counter0)
16:31	RWX_WCLRR EG	Reserved field. (Access type is pbh_event_grp1_counter1)
32:47	RWX_WCLRR EG	Reserved field. (Access type is pbh_event_grp1_counter2)
48:63	RWX_WCLRR EG	Reserved field. (Access type is pbh_event_grp1_counter3)

Register Name	<i>Processor Bus PB CENT PMU2 Counter Register</i>
Mnemonic	EH.PB.PB_CENT_PMU2_COUNTER
Address	0000000002010C56 (SCOM)
Attributes	
Description	00:15 pbh_event_grp2_counter0(0:15) 16:31 pbh_event_grp2_counter1(0:15) 32:47 pbh_event_grp2_counter2(0:15) 48:63 pbh_event_grp2_counter3(0:31)

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Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRR EG	Reserved field. (Access type is pbh_event_grp2_counter0)
16:31	RWX_WCLRR EG	Reserved field. (Access type is pbh_event_grp2_counter1)
32:47	RWX_WCLRR EG	Reserved field. (Access type is pbh_event_grp2_counter2)
48:63	RWX_WCLRR EG	Reserved field. (Access type is pbh_event_grp2_counter3)

Register Name	<i>Processor Bus PB CENT PMU3 Counter Register</i>
Mnemonic	EH.PB.PB_CENT_PMU3_COUNTER
Address	0000000002010C57 (SCOM)
Attributes	
Description	00:15 pbh_event_grp3_counter0(0:15) 16:31 pbh_event_grp3_counter1(0:15) 32:47 pbh_event_grp3_counter2(0:15) 48:63 pbh_event_grp3_counter3(0:31)

Bits	SCOM	Field Mnemonic: Description
0:15	RWX_WCLRR EG	Reserved field. (Access type is pbh_event_grp3_counter0)
16:31	RWX_WCLRR EG	Reserved field. (Access type is pbh_event_grp3_counter1)
32:47	RWX_WCLRR EG	Reserved field. (Access type is pbh_event_grp3_counter2)
48:63	RWX_WCLRR EG	Reserved field. (Access type is pbh_event_grp3_counter3)

Register Name	<i>Processor Bus PB CENT RGMCFG00 Register</i>
Mnemonic	EH.PB.MISC.PB_CENT_RGMCFG00
Address	0000000002010C58 (SCOM)
Attributes	
Description	00 = pb_cfg_rgmcfg00_valid 01:14 = pb_cfg_rgmcfg00_group_size 15:32 = pb_cfg_rgmcfg00_base_addr 33:35 = spare

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_RGMCFG00_VALID: configures the Remote Group Memory BAR 00 for link A0 as valid



Bits	SCOM	Field Mnemonic: Description
1:14	RWX	PB_CFG_RGMCFG00_GROUP_SIZE: configures the group size for Remote Group Memory BAR 00 for link A0 4GB=>0b0000000000000000 8GB=>0b0000000000000001 16GB=>0b0000000000000011 32GB=>0b0000000000000111 64GB=>0b0000000000001111 128GB=>0b0000000000011111 256GB=>0b0000000001111111 512GB=>0b0000000011111111 1TB=>0b0000000111111111 2TB=>0b0000001111111111 4TB=>0b0000011111111111 8TB=>0b0000111111111111 16TB=>0b0001111111111111 32TB=>0b0011111111111111 64TB=>0b0111111111111111
15:32	RWX	PB_CFG_RGMCFG00_BASE: configures the base address of Remote Group Memory BAR 00 for link A0
33:35	RW	Reserved field. (Access type is spare)
36:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Processor Bus PB CENT RGMCFG01 Register
Mnemonic	EH.PB.MISC.PB_CENT_RGMCFG01
Address	0000000002010C59 (SCOM)
Attributes	
Description	00 = pb_cfg_rgmcfg01_valid 01:14 = pb_cfg_rgmcfg01_group_size 15:32 = pb_cfg_rgmcfg01_base_addr 33:35 = spare

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_RGMCFG01_VALID: configures the Remote Group Memory BAR 00 for link A1 as valid
1:14	RWX	PB_CFG_RGMCFG01_GROUP_SIZE: configures the group size for Remote Group Memory BAR 00 for link A1 4GB=>0b0000000000000000 8GB=>0b0000000000000001 16GB=>0b0000000000000011 32GB=>0b0000000000000111 64GB=>0b0000000000001111 128GB=>0b0000000000011111 256GB=>0b0000000001111111 512GB=>0b0000000011111111 1TB=>0b0000000111111111 2TB=>0b0000001111111111 4TB=>0b0000011111111111 8TB=>0b0000111111111111 16TB=>0b0001111111111111 32TB=>0b0011111111111111 64TB=>0b0111111111111111
15:32	RWX	PB_CFG_RGMCFG01_BASE: configures the base address of Remote Group Memory BAR 00 for link A1
33:35	RW	Reserved field. (Access type is spare)

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Bits	SCOM	Field Mnemonic: Description
36:63	RO	Constant = 0b000000000000000000000000

Register Name	<i>Processor Bus PB CENT RGMCFG10 Register</i>
Mnemonic	EH.PB.MISC.PB_CENT_RGMCFG10
Address	0000000002010C5A (SCOM)
Attributes	
Description	00 = pb_cfg_rgmcfg10_valid 01:14 = pb_cfg_rgmcfg10_group_size 15:32 = pb_cfg_rgmcfg10_base_addr 33:35 = spare

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_RGMCFG02_VALID: configures the Remote Group Memory BAR 00 for link A2 as valid
1:14	RWX	PB_CFG_RGMCFG02_GROUP_SIZE: configures the group size for Remote Group Memory BAR 00 for link A2 4GB=>0b0000000000000000 8GB=>0b0000000000000001 16GB=>0b0000000000000011 32GB=>0b0000000000000111 64GB=>0b0000000000001111 128GB=>0b0000000000011111 256GB=>0b0000000000111111 512GB=>0b0000000011111111 1TB=>0b0000000111111111 2TB=>0b0000001111111111 4TB=>0b0000011111111111 8TB=>0b0000111111111111 16TB=>0b0001111111111111 32TB=>0b0011111111111111 64TB=>0b0111111111111111
15:32	RWX	PB_CFG_RGMCFG02_BASE: configures the base address of Remote Group Memory BAR 00 for link A2
33:35	RW	Reserved field. (Access type is spare)
36:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>Processor Bus PB CENT RGMCFG00 Register</i>
Mnemonic	EH.PB.MISC.PB_CENT_RGMCFG00
Address	0000000002010C5B (SCOM)
Attributes	
Description	00 = pb_cfg_rgmcfgm00_valid 01:14 = pb_cfg_rgmcfgm00_group_size 15:32 = pb_cfg_rgmcfgm00_base_addr 33:35 = spare

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_RGMCFG00_VALID: configures the mirrored Remote Group Memory BAR 00 for link A0 as valid



Bits	SCOM	Field Mnemonic: Description
1:14	RWX	PB_CFG_RGMCFGM00_GROUP_SIZE: configures the group size for mirrored Remote Group Memory BAR 00 for link A0 4GB=>0b0000000000000000 8GB=>0b0000000000000001 16GB=>0b0000000000000011 32GB=>0b0000000000000111 64GB=>0b0000000000001111 128GB=>0b0000000000011111 256GB=>0b0000000001111111 512GB=>0b0000000111111111 1TB=>0b0000001111111111 2TB=>0b0000011111111111 4TB=>0b0000111111111111 8TB=>0b0001111111111111 16TB=>0b0011111111111111 32TB=>0b0111111111111111 64TB=>0b1111111111111111
15:32	RWX	PB_CFG_RGMCFGM00_BASE: configures the base address of Mirrored Remote Group Memory BAR 00 for link A0
33:35	RW	Reserved field. (Access type is spare)
36:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Processor Bus PB CENT RGMCFGM01 Register
Mnemonic	EH.PB.MISC.PB_CENT_RGMCFGM01
Address	0000000002010C5C (SCOM)
Attributes	
Description	00 = pb_cfg_rgmcfgm01_valid 01:14 = pb_cfg_rgmcfgm01_group_size 15:32 = pb_cfg_rgmcfgm01_base_addr 33:35 = spare

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_RGMCFGM01_VALID: configures the Mirrored Remote Group Memory BAR 00 for link A1 as valid
1:14	RWX	PB_CFG_RGMCFGM01_GROUP_SIZE: configures the group size for Mirrored Remote Group Memory BAR 00 for link A1 4GB=>0b0000000000000000 8GB=>0b0000000000000001 16GB=>0b0000000000000011 32GB=>0b0000000000000111 64GB=>0b0000000000001111 128GB=>0b0000000000011111 256GB=>0b0000000001111111 512GB=>0b0000000111111111 1TB=>0b0000001111111111 2TB=>0b0000011111111111 4TB=>0b0000111111111111 8TB=>0b0001111111111111 16TB=>0b0011111111111111 32TB=>0b0111111111111111 64TB=>0b1111111111111111

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Bits	SCOM	Field Mnemonic: Description
15:32	RWX	PB_CFG_RGMCFG01_BASE: configures the base address of Mirrored Remote Group Memory BAR 00 for link A1
33:35	RW	Reserved field. (Access type is spare)
36:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Processor Bus PB CENT RGMCFG01 Register
Mnemonic	EH.PB.MISC.PB_CENT_RGMCFG01
Address	0000000002010C5D (SCOM)
Attributes	
Description	00 = pb_cfg_rgmcfg01_valid 01:14 = pb_cfg_rgmcfg01_group_size 15:32 = pb_cfg_rgmcfg01_base_addr 33:35 = spare

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_RGMCFG02_VALID: configures the Mirrored Remote Group Memory BAR 00 for link A2 as valid
1:14	RWX	PB_CFG_RGMCFG02_GROUP_SIZE: configures the group size for Mirrored Remote Group Memory BAR 00 for link A2 4GB=>0b0000000000000000 8GB=>0b0000000000000001 16GB=>0b0000000000000011 32GB=>0b0000000000000111 64GB=>0b0000000000001111 128GB=>0b0000000000011111 256GB=>0b0000000000111111 512GB=>0b0000000001111111 1TB=>0b0000000111111111 2TB=>0b0000011111111111 4TB=>0b0000111111111111 8TB=>0b0001111111111111 16TB=>0b0011111111111111 32TB=>0b0111111111111111 64TB=>0b1111111111111111
15:32	RWX	PB_CFG_RGMCFG02_BASE: configures the base address of Mirrored Remote Group Memory BAR 00 for link A2
33:35	RW	Reserved field. (Access type is spare)
36:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Processor Bus PB CENT GP CMD RATE DP0 Register
Mnemonic	EH.PB.MISC.PB_CENT_GP_CMD_RATE_DP0
Address	0000000002010C62 (SCOM)
Attributes	
Description	00:07 = pb_gp_cmd_rate_dp0_lvl0 08:15 = pb_gp_cmd_rate_dp0_lvl1 16:23 = pb_gp_cmd_rate_dp0_lvl2 24:31 = pb_gp_cmd_rate_dp0_lvl3 32:39 = pb_gp_cmd_rate_dp0_lvl4 40:47 = pb_gp_cmd_rate_dp0_lvl5 48:55 = pb_gp_cmd_rate_dp0_lvl6 56:63 = pb_gp_cmd_rate_dp0_lvl7

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	PB_CFG_GP_CMD_RATE_DP0_LVL0: configures the command rate for group pump drop priority 0 at level 0
8:15	RWX	PB_CFG_GP_CMD_RATE_DP0_LVL1: configures the command rate for group pump drop priority 0 at level 1
16:23	RWX	PB_CFG_GP_CMD_RATE_DP0_LVL2: configures the command rate for group pump drop priority 0 at level 2
24:31	RWX	PB_CFG_GP_CMD_RATE_DP0_LVL3: configures the command rate for group pump drop priority 0 at level 3
32:39	RWX	PB_CFG_GP_CMD_RATE_DP0_LVL4: configures the command rate for group pump drop priority 0 at level 4
40:47	RWX	PB_CFG_GP_CMD_RATE_DP0_LVL5: configures the command rate for group pump drop priority 0 at level 5
48:55	RWX	PB_CFG_GP_CMD_RATE_DP0_LVL6: configures the command rate for group pump drop priority 0 at level 6
56:63	RWX	PB_CFG_GP_CMD_RATE_DP0_LVL7: configures the command rate for group pump drop priority 0 at level 7

Register Name	<i>Processor Bus PB CENT GP CMD RATE DP1 Register</i>
Mnemonic	EH.PB.MISC.PB_CENT_GP_CMD_RATE_DP1
Address	0000000002010C63 (SCOM)
Attributes	
Description	00:07 = pb_gp_cmd_rate_dp1_lv0 08:15 = pb_gp_cmd_rate_dp1_lv1 16:23 = pb_gp_cmd_rate_dp1_lv2 24:31 = pb_gp_cmd_rate_dp1_lv3 32:39 = pb_gp_cmd_rate_dp1_lv4 40:47 = pb_gp_cmd_rate_dp1_lv5 48:55 = pb_gp_cmd_rate_dp1_lv6 56:63 = pb_gp_cmd_rate_dp1_lv7

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	PB_CFG_GP_CMD_RATE_DP1_LVL0: configures the command rate for group pump drop priority 1 at level 0
8:15	RWX	PB_CFG_GP_CMD_RATE_DP1_LVL1: configures the command rate for group pump drop priority 1 at level 1
16:23	RWX	PB_CFG_GP_CMD_RATE_DP1_LVL2: configures the command rate for group pump drop priority 1 at level 2
24:31	RWX	PB_CFG_GP_CMD_RATE_DP1_LVL3: configures the command rate for group pump drop priority 1 at level 3
32:39	RWX	PB_CFG_GP_CMD_RATE_DP1_LVL4: configures the command rate for group pump drop priority 1 at level 4
40:47	RWX	PB_CFG_GP_CMD_RATE_DP1_LVL5: configures the command rate for group pump drop priority 1 at level 5
48:55	RWX	PB_CFG_GP_CMD_RATE_DP1_LVL6: configures the command rate for group pump drop priority 1 at level 6
56:63	RWX	PB_CFG_GP_CMD_RATE_DP1_LVL7: configures the command rate for group pump drop priority 1 at level 7

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Register Name	Processor Bus PB CENT RGP CMD RATE DP0 Register
Mnemonic	EH.PB.MISC.PB_CENT_RGP_CMD_RATE_DP0
Address	0000000002010C64 (SCOM)
Attributes	
Description	00:07 = pb_rgp_cmd_rate_dp0_lvl0 08:15 = pb_rgp_cmd_rate_dp0_lvl1 16:23 = pb_rgp_cmd_rate_dp0_lvl2 24:31 = pb_rgp_cmd_rate_dp0_lvl3 32:39 = pb_rgp_cmd_rate_dp0_lvl4 40:47 = pb_rgp_cmd_rate_dp0_lvl5 48:55 = pb_rgp_cmd_rate_dp0_lvl6 56:63 = pb_rgp_cmd_rate_dp0_lvl7

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	PB_CFG_RGP_CMD_RATE_DP0_LVL0: configures the command rate for remote group pump drop priority 0 at level 0
8:15	RWX	PB_CFG_RGP_CMD_RATE_DP0_LVL1: configures the command rate for remote group pump drop priority 0 at level 1
16:23	RWX	PB_CFG_RGP_CMD_RATE_DP0_LVL2: configures the command rate for remote group pump drop priority 0 at level 2
24:31	RWX	PB_CFG_RGP_CMD_RATE_DP0_LVL3: configures the command rate for remote group pump drop priority 0 at level 3
32:39	RWX	PB_CFG_RGP_CMD_RATE_DP0_LVL4: configures the command rate for remote group pump drop priority 0 at level 4
40:47	RWX	PB_CFG_RGP_CMD_RATE_DP0_LVL5: configures the command rate for remote group pump drop priority 0 at level 5
48:55	RWX	PB_CFG_RGP_CMD_RATE_DP0_LVL6: configures the command rate for remote group pump drop priority 0 at level 6
56:63	RWX	PB_CFG_RGP_CMD_RATE_DP0_LVL7: configures the command rate for remote group pump drop priority 0 at level 7

Register Name	Processor Bus PB CENT RGP CMD RATE DP1 Register
Mnemonic	EH.PB.MISC.PB_CENT_RGP_CMD_RATE_DP1
Address	0000000002010C65 (SCOM)
Attributes	
Description	00:07 = pb_rgp_cmd_rate_dp1_lvl0 08:15 = pb_rgp_cmd_rate_dp1_lvl1 16:23 = pb_rgp_cmd_rate_dp1_lvl2 24:31 = pb_rgp_cmd_rate_dp1_lvl3 32:39 = pb_rgp_cmd_rate_dp1_lvl4 40:47 = pb_rgp_cmd_rate_dp1_lvl5 48:55 = pb_rgp_cmd_rate_dp1_lvl6 56:63 = pb_rgp_cmd_rate_dp1_lvl7

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	PB_CFG_RGP_CMD_RATE_DP1_LVL0: configures the command rate for remote group pump drop priority 1 at level 0
8:15	RWX	PB_CFG_RGP_CMD_RATE_DP1_LVL1: configures the command rate for remote group pump drop priority 1 at level 1
16:23	RWX	PB_CFG_RGP_CMD_RATE_DP1_LVL2: configures the command rate for remote group pump drop priority 1 at level 2
24:31	RWX	PB_CFG_RGP_CMD_RATE_DP1_LVL3: configures the command rate for remote group pump drop priority 1 at level 3
32:39	RWX	PB_CFG_RGP_CMD_RATE_DP1_LVL4: configures the command rate for remote group pump drop priority 1 at level 4
40:47	RWX	PB_CFG_RGP_CMD_RATE_DP1_LVL5: configures the command rate for remote group pump drop priority 1 at level 5
48:55	RWX	PB_CFG_RGP_CMD_RATE_DP1_LVL6: configures the command rate for remote group pump drop priority 1 at level 6

Bits	SCOM	Field Mnemonic: Description
56:63	RWX	PB_CFG_RGP_CMD_RATE_DP1_LVL7: configures the command rate for remote group pump drop priority 1 at level 7

Register Name	<i>Processor Bus PB CENT SP CMD RATE DP0 Register</i>
Mnemonic	EH.PB.MISC.PB_CENT_SP_CMD_RATE_DP0
Address	0000000002010C66 (SCOM)
Attributes	
Description	00:07 = pb_sp_cmd_rate_dp0_lvl0 08:15 = pb_sp_cmd_rate_dp0_lvl1 16:23 = pb_sp_cmd_rate_dp0_lvl2 24:31 = pb_sp_cmd_rate_dp0_lvl3 32:39 = pb_sp_cmd_rate_dp0_lvl4 40:47 = pb_sp_cmd_rate_dp0_lvl5 48:55 = pb_sp_cmd_rate_dp0_lvl6 56:63 = pb_sp_cmd_rate_dp0_lvl7

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	PB_CFG_SP_CMD_RATE_DP0_LVL0: configures the command rate for system pump drop priority 0 at level 0
8:15	RWX	PB_CFG_SP_CMD_RATE_DP0_LVL1: configures the command rate for system pump drop priority 0 at level 1
16:23	RWX	PB_CFG_SP_CMD_RATE_DP0_LVL2: configures the command rate for system pump drop priority 0 at level 2
24:31	RWX	PB_CFG_SP_CMD_RATE_DP0_LVL3: configures the command rate for system pump drop priority 0 at level 3
32:39	RWX	PB_CFG_SP_CMD_RATE_DP0_LVL4: configures the command rate for system pump drop priority 0 at level 4
40:47	RWX	PB_CFG_SP_CMD_RATE_DP0_LVL5: configures the command rate for system pump drop priority 0 at level 5
48:55	RWX	PB_CFG_SP_CMD_RATE_DP0_LVL6: configures the command rate for system pump drop priority 0 at level 6
56:63	RWX	PB_CFG_SP_CMD_RATE_DP0_LVL7: configures the command rate for system pump drop priority 0 at level 7

Register Name	<i>Processor Bus PB CENT SP CMD RATE DP1 Register</i>
Mnemonic	EH.PB.MISC.PB_CENT_SP_CMD_RATE_DP1
Address	0000000002010C67 (SCOM)
Attributes	
Description	00:07 = pb_sp_cmd_rate_dp1_lvl0 08:15 = pb_sp_cmd_rate_dp1_lvl1 16:23 = pb_sp_cmd_rate_dp1_lvl2 24:31 = pb_sp_cmd_rate_dp1_lvl3 32:39 = pb_sp_cmd_rate_dp1_lvl4 40:47 = pb_sp_cmd_rate_dp1_lvl5 48:55 = pb_sp_cmd_rate_dp1_lvl6 56:63 = pb_sp_cmd_rate_dp1_lvl7

Bits	SCOM	Field Mnemonic: Description
0:7	RWX	PB_CFG_SP_CMD_RATE_DP1_LVL0: configures the command rate for system pump drop priority 1 at level 0
8:15	RWX	PB_CFG_SP_CMD_RATE_DP1_LVL1: configures the command rate for system pump drop priority 1 at level 1
16:23	RWX	PB_CFG_SP_CMD_RATE_DP1_LVL2: configures the command rate for system pump drop priority 1 at level 2
24:31	RWX	PB_CFG_SP_CMD_RATE_DP1_LVL3: configures the command rate for system pump drop priority 1 at level 3

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Bits	SCOM	Field Mnemonic: Description
32:39	RWX	PB_CFG_SP_CMD_RATE_DP1_LVL4: configures the command rate for system pump drop priority 1 at level 4
40:47	RWX	PB_CFG_SP_CMD_RATE_DP1_LVL5: configures the command rate for system pump drop priority 1 at level 5
48:55	RWX	PB_CFG_SP_CMD_RATE_DP1_LVL6: configures the command rate for system pump drop priority 1 at level 6
56:63	RWX	PB_CFG_SP_CMD_RATE_DP1_LVL7: configures the command rate for system pump drop priority 1 at level 7

Register Name	Processor Bus PB CENT PMU Register
Mnemonic	EH.PB.MISC.PB_CENT_PMU
Address	0000000002010C68 (SCOM)
Attributes	
Description	00 = pb_cfg_pmu_en 01 = pb_cfg_pmu_prescaler_mode 02:03 = spare 04 = pb_cfg_pmu_counter_mode 05 = spare 06 = pb_cfg_pmu_reset_mode 07 = pb_cfg_apm_enhanced_mode 08:09 = pb_cfg_pmu_prescaler_grp0 10:11 = pb_cfg_pmu_prescaler_grp1 12:13 = pb_cfg_pmu_prescaler_grp2 14:15 = pb_cfg_pmu_prescaler_grp3 16:17 = pb_cfg_pmu_op_0 18:19 = pb_cfg_pmu_op_1 20:21 = pb_cfg_pmu_op_2 22:23 = pb_cfg_pmu_op_3 24:25 = pb_cfg_pmu_op_4 26:27 = pb_cfg_pmu_op_5 28:29 = pb_cfg_pmu_op_6 30:31 = pb_cfg_pmu_op_7 32:33 = pb_cfg_pmu_op_8 34:35 = pb_cfg_pmu_op_9 36:37 = pb_cfg_pmu_op_10 38:39 = pb_cfg_pmu_op_11 40:41 = pb_cfg_pmu_op_12 42:43 = pb_cfg_pmu_op_13 44:45 = pb_cfg_pmu_op_14 46:47 = pb_cfg_pmu_op_15 48:63 = pb_cfg_pmu_edge

Bits	SCOM	Field Mnemonic: Description
0	RWX	PB_CFG_PMU_ENABLE: Enable Performance Monitor
1	RWX	PB_CFG_PMU_PRESCALER_MODE: 1 = Enable prescale level control of PMU counter3 0 = Default to group prescaler. The default is 0.
2:3	RW	
4	RWX	PB_CFG_PMU_COUNTER_MODE: 0 = Freeze on counter max 1 = Free running
5	RW	PB_CFG_PMU_RESET_MODE: Performance Monitor Reset Mode. 00 = Reset on read 01 = Reset on write RESET_ON_RD=>0b00 RESET_ON_WR=>0b01
6	RWX	PB_CFG_PMU_RESET_MODE: Performance Monitor Reset Mode. 00 = Reset on read 01 = Reset on write RESET_ON_RD=>0b00 RESET_ON_WR=>0b01
7	RWX	PB_CFG_APM_ENHANCED_MODE: 1 = Freeze APM counter on PMU counter maximum 0 = Free running (default = 0)



Bits	SCOM	Field Mnemonic: Description
8:9	RWX	PB_CFG_PMU_PRESCALER_GRP0: Performance Monitor Prescaler Select. 00 = 20 bit 01 = 16 bit 10 = 8 bit 11 = 4 bit P20=>0b00 P16=>0b01 Processor=>0b10 P4=>0b11
10:11	RWX	PB_CFG_PMU_PRESCALER_GRP1: Performance Monitor Prescaler Select. 00 = 20 bit 01 = 16 bit 10 = 8 bit 11 = 4 bit P20=>0b00 P16=>0b01 Processor=>0b10 P4=>0b11
12:13	RWX	PB_CFG_PMU_PRESCALER_GRP2: Performance Monitor Prescaler Select. 00 = 20 bit 01 = 16 bit 10 = 8 bit 11 = 4 bit P20=>0b00 P16=>0b01 Processor=>0b10 P4=>0b11
14:15	RWX	PB_CFG_PMU_PRESCALER_GRP3: Performance Monitor Prescaler Select. 00 = 20 bit 01 = 16 bit 10 = 8 bit 11 = 4 bit P20=>0b00 P16=>0b01 Processor=>0b10 P4=>0b11
16:17	RWX	PB_CFG_PMU_0_1_OP: Performance Monitor Bit 0/1 Select. 00 = sel_a 01 = sel_b 10 = add_ab 11 = cycles SEL_A=>0b00 SEL_B=>0b01 ADD_AB=>0b10 CYCLES=>0b11

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Bits	SCOM	Field Mnemonic: Description
18:19	RWX	PB_CFG_PMU_2_3_OP: Performance Monitor Bit 2/3 Select. 00 = sel_a, 01 = sel_b 10 = add_ab 11 = cycles SEL_A=>0b00 SEL_B=>0b01 ADD_AB=>0b10 CYCLES=>0b11
20:21	RWX	PB_CFG_PMU_4_5_OP: Performance Monitor Bit 4/5 Select. 00 = sel_a 01 = sel_b 10 = add_ab 11 = cycles SEL_A=>0b00 SEL_B=>0b01 ADD_AB=>0b10 CYCLES=>0b11
22:23	RWX	PB_CFG_PMU_6_7_OP: Performance Monitor Bit 6/7 Select. 00 = sel_a 01 = sel_b 10 = add_ab 11 = cycles SEL_A=>0b00 SEL_B=>0b01 ADD_AB=>0b10 CYCLES=>0b11
24:25	RWX	PB_CFG_PMU_8_9_OP: Performance Monitor Bit 8/9 Select. 00 = sel_a 01 = sel_b 10 = add_ab 11 = cycles SEL_A=>0b00 SEL_B=>0b01 ADD_AB=>0b10 CYCLES=>0b11
26:27	RWX	PB_CFG_PMU_10_11_OP: Performance Monitor Bit 10/11 Select. 00 = sel_a 01 = sel_b 10 = add_ab 11 = cycles SEL_A=>0b00 SEL_B=>0b01 ADD_AB=>0b10 CYCLES=>0b11



Bits	SCOM	Field Mnemonic: Description
28:29	RWX	PB_CFG_PMU_12_13_OP: Performance Monitor Bit 12/13 Select. 00 = sel_a 01 = sel_b 10 = add_ab 11 = cycles SEL_A=>0b00 SEL_B=>0b01 ADD_AB=>0b10 CYCLES=>0b11
30:31	RWX	PB_CFG_PMU_14_15_OP: Performance Monitor Bit 14/15 Select. 00 = sel_a 01 = sel_b 10 = add_ab 11 = cycles SEL_A=>0b00 SEL_B=>0b01 ADD_AB=>0b10 CYCLES=>0b11
32:33	RWX	PB_CFG_PMU_16_17_OP: Performance Monitor Bit 16/17 Select. 00 = sel_a 01 = sel_b 10 = add_ab 11 = cycles SEL_A=>0b00 SEL_B=>0b01 ADD_AB=>0b10 CYCLES=>0b11
34:35	RWX	PB_CFG_PMU_18_19_OP: Performance Monitor Bit 18/19 Select. 00 = sel_a 01 = sel_b 10 = add_ab 11 = cycles SEL_A=>0b00 SEL_B=>0b01 ADD_AB=>0b10 CYCLES=>0b11
36:37	RWX	PB_CFG_PMU_20_21_OP: Performance Monitor Bit 20/21 Select. 00 = sel_a 01 = sel_b 10 = add_ab 11 = cycles SEL_A=>0b00 SEL_B=>0b01 ADD_AB=>0b10 CYCLES=>0b11

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Bits	SCOM	Field Mnemonic: Description
38:39	RWX	PB_CFG_PMU_22_23_OP: Performance Monitor Bit 22/23 Select. 00 = sel_a 01 = sel_b 10 = add_ab 11 = cycles SEL_A=>0b00 SEL_B=>0b01 ADD_AB=>0b10 CYCLES=>0b11
40:41	RWX	PB_CFG_PMU_24_25_OP: Performance Monitor Bit 24/25 Select. 00 = sel_a 01 = sel_b 10 = add_ab 11 = cycles SEL_A=>0b00 SEL_B=>0b01 ADD_AB=>0b10 CYCLES=>0b11
42:43	RWX	PB_CFG_PMU_26_27_OP: Performance Monitor Bit 26/27 Select. 00 = sel_a 01 = sel_b 10 = add_ab 11 = cycles SEL_A=>0b00 SEL_B=>0b01 ADD_AB=>0b10 CYCLES=>0b11
44:45	RWX	PB_CFG_PMU_28_29_OP: Performance Monitor Bit 28/29 Select. 00 = sel_a 01 = sel_b 10 = add_ab 11 = cycles SEL_A=>0b00 SEL_B=>0b01 ADD_AB=>0b10 CYCLES=>0b11
46:47	RWX	PB_CFG_PMU_30_31_OP: Performance Monitor Bit 30/31 Select. 00 = sel_a 01 = sel_b 10 = add_ab 11 = cycles SEL_A=>0b00 SEL_B=>0b01 ADD_AB=>0b10 CYCLES=>0b11
48	RWX	PB_CFG_PMU_0_1_EDGE: 0 = Count level 1 = Count edge
49	RWX	PB_CFG_PMU_2_3_EDGE: 0 = Count level 1 = Count edge



Bits	SCOM	Field Mnemonic: Description
50	RWX	PB_CFG_PMU_4_5_EDGE: 0 = Count level 1 = Count edge
51	RWX	PB_CFG_PMU_6_7_EDGE: 0 = Count level 1 = Count edge
52	RWX	PB_CFG_PMU_8_9_EDGE: 0 = Count level 1 = Count edge
53	RWX	PB_CFG_PMU_10_11_EDGE: 0 = Count level 1 = Count edge
54	RWX	PB_CFG_PMU_12_13_EDGE: 0 = Count level 1 = Count edge
55	RWX	PB_CFG_PMU_14_15_EDGE: 0 = Count level 1 = Count edge
56	RWX	PB_CFG_PMU_16_17_EDGE: 0 = Count level 1 = Count edge
57	RWX	PB_CFG_PMU_18_19_EDGE: 0 = Count level 1 = Count edge
58	RWX	PB_CFG_PMU_20_21_EDGE: 0 = Count level 1 = Count edge
59	RWX	PB_CFG_PMU_22_23_EDGE: 0 = Count level 1 = Count edge
60	RWX	PB_CFG_PMU_24_25_EDGE: 0 = Count level 1 = Count edge
61	RWX	PB_CFG_PMU_26_27_EDGE: 0 = Count level 1 = Count edge
62	RWX	PB_CFG_PMU_28_29_EDGE: 0 = Count level 1 = Count edge
63	RWX	PB_CFG_PMU_30_31_EDGE: 0 = Count level 1 = Count edge

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Register Name	<i>Processor Bus PB CENT EVENT SEL Register</i>
Mnemonic	EH.PB.MISC.PB_CENT_EVENT_SEL
Address	0000000002010C69 (SCOM)
Attributes	
Description	00:02 = pb_cfg_event_sel0 03:05 = pb_cfg_event_sel1 06:08 = pb_cfg_event_sel2 09:11 = pb_cfg_event_sel3 12 = pb_cfg_mc0_mask 13 = pb_cfg_mc1_mask 14 = pb_cfg_mc2_mask 15 = pb_cfg_mc3_mask 16 = pb_cfg_mcd_mask 17 = pb_cfg_nx_mask 18 = pb_cfg_pb_mask 19 = pb_cfg_es_mask 20 = pb_cfg_pmu_grp0_prescale_level 21 = pb_cfg_pmu_grp1_prescale_level 22 = pb_cfg_pmu_grp2_prescale_level 23 = pb_cfg_pmu_grp3_prescale_level 24:31 = spare 32:63 = pbh_ebus_en

Bits	SCOM	Field Mnemonic: Description
0:1	RWX	PB_CFG_PMU_SEL0: Performance Monitor Group0 Select; 00 = A 01 = B 10 = C 11 = D SEL_A=>0b00 SEL_B=>0b01 SEL_C=>0b10 SEL_D=>0b11
2	RWX	Reserved field. (Access type is pb_cfg_event_sel0.) SEL_A=>0b00 SEL_B=>0b01 SEL_C=>0b10 SEL_D=>0b11
3:4	RWX	PB_CFG_PMU_SEL1: Performance Monitor Group1 Select. 00 = A 01 = B 10 = C 11 = D SEL_A=>0b00 SEL_B=>0b01 SEL_C=>0b10 SEL_D=>0b11
5	RWX	Reserved field. (Access type is pb_cfg_event_sel1.) SEL_A=>0b00 SEL_B=>0b01 SEL_C=>0b10 SEL_D=>0b11

Bits	SCOM	Field Mnemonic: Description
6:7	RWX	PB_CFG_PMU_SEL2: Performance Monitor Group2 Select. 00 = A 01 = B 10 = C 11 = D SEL_A=>0b00 SEL_B=>0b01 SEL_C=>0b10 SEL_D=>0b11
8	RWX	Reserved field. (Access type is pb_cfg_event_sel2.) SEL_A=>0b00 SEL_B=>0b01 SEL_C=>0b10 SEL_D=>0b11
9:10	RWX	PB_CFG_PMU_SEL3: Performance Monitor Group3 Select. 00 = A 01 = B 10 = C 11 = D SEL_A=>0b00 SEL_B=>0b01 SEL_C=>0b10 SEL_D=>0b11
11	RWX	Reserved field. (Access type is pb_cfg_event_sel3.) SEL_A=>0b00 SEL_B=>0b01 SEL_C=>0b10 SEL_D=>0b11
12	RWX	PB_CFG_MC0_MASK: MC0 unit event bus mask. When set, unit event bus inputs are disabled. The default is 0.
13	RWX	PB_CFG_MC1_MASK: MC1 unit event bus mask. When set, unit event bus inputs are disabled. The default is 0.
14	RWX	PB_CFG_MC2_MASK: MC2 unit event bus mask. When set, unit event bus inputs are disabled. The default is 0.
15	RWX	PB_CFG_MC3_MASK: MC3 unit event bus mask. When set, unit event bus inputs are disabled. The default is 0.
16	RWX	PB_CFG_MCD_MASK: MCD unit event bus mask. When set, unit event bus inputs are disabled. The default is 0.
17	RWX	PB_CFG_NX_MASK: NX unit event bus mask. When set, unit event bus inputs are disabled. The default is 0.
18	RWX	PB_CFG_PB_MASK: PB unit event bus mask. When set, unit event bus inputs are disabled. The default is 0.
19	RWX	PB_CFG_ES_MASK: PE unit event bus mask. When set, unit event bus inputs are disabled. The default is 0.
20	RWX	PB_CFG_PMU_GRP0_PRESCALE_LEVEL: 0=Group0 prescaler-1, 1=Group0 prescaler+1. Requires pb_cfg_pmu_prescaler_mode=1. The default is 0.
21	RWX	PB_CFG_PMU_GRP1_PRESCALE_LEVEL: 0=Group1 prescaler-1, 1=Group1 prescaler+1. Requires pb_cfg_pmu_prescaler_mode=1. The default is 0.

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Bits	SCOM	Field Mnemonic: Description
22	RWX	PB_CFG_PMU_GRP2_PRESCALE_LEVEL: 0=Group2 prescaler-1, 1=Group2 prescaler+1. Requires pb_cfg_pmu_prescaler_mode=1. The default is 0.
23	RWX	PB_CFG_PMU_GRP3_PRESCALE_LEVEL: 0=Group3 prescaler-1, 1=Group3 prescaler+1. Requires pb_cfg_pmu_prescaler_mode=1. The default is 0.
24:31	RW	
32:63	RWX	PB_CFG_PMU_BITWISE_ENABLE: Individual enable of PB events asserted on event bus.

Register Name	<i>Processor Bus PB CENT EVENT COMPA Register</i>
Mnemonic	EH.PB.MISC.PB_CENT_EVENT_COMPA
Address	0000000002010C6A (SCOM)
Attributes	
Description	00:05 = pb_cfg_event_compa_ttype 06:11 = pb_cfg_event_compa_ttype_mask 12:18 = pb_cfg_event_compa_tsize 19:25 = pb_cfg_event_compa_tsize_mask 26:28 = pb_cfg_event_compa_scope 29:40 = pb_cfg_event_compa_presp 41:52 = pb_cfg_event_compa_presp_mask 53:57 = pb_cfg_event_compa_cresp 58:62 = pb_cfg_event_compa_cresp_mask 63 = pb_cfg_event_compa_cresp_polarity

Bits	SCOM	Field Mnemonic: Description
0:5	RWX	PB_CFG_EVENT_COMPA_TTYPE: PMU event compare A - Ttype
6:11	RWX	PB_CFG_EVENT_COMPA_TTYPE_MASK: PMU event compare A - Ttype mask
12:18	RWX	PB_CFG_EVENT_COMPA_TSIZE: PMU event compare A - tsize
19:25	RWX	PB_CFG_EVENT_COMPA_TSIZE_MASK: PMU event compare A - tsize mask
26:28	RWX	PB_CFG_EVENT_COMPA_SCOPE: PMU event compare A - scope
29:40	RWX	PB_CFG_EVENT_COMPA_PRESP: PMU event compare A - presp
41:52	RWX	PB_CFG_EVENT_COMPA_PRESP_MASK: PMU event compare A - presp mask
53:57	RWX	PB_CFG_EVENT_COMPA_CRESP: PMU event compare A - cresp
58:62	RWX	PB_CFG_EVENT_COMPA_CRESP_MASK: PMU event compare A - cresp mask
63	RWX	PB_CFG_EVENT_COMPA_CRESP_POLARITY: PMU event compare A - cresp polarity

Register Name	Processor Bus PB CENT EVENT COMPB Register
Mnemonic	EH.PB.MISC.PB_CENT_EVENT_COMPB
Address	0000000002010C6B (SCOM)
Attributes	
Description	00:05 = pb_cfg_event_compb_ttype 06:11 = pb_cfg_event_compb_ttype_mask 12:18 = pb_cfg_event_compb_tsize 19:25 = pb_cfg_event_compb_tsize_mask 26:28 = pb_cfg_event_compb_scope 29:40 = pb_cfg_event_compb_presp 41:52 = pb_cfg_event_compb_presp_mask 53:57 = pb_cfg_event_compb_cresp 58:62 = pb_cfg_event_compb_cresp_mask 63 = pb_cfg_event_compb_cresp_polarity

Bits	SCOM	Field Mnemonic: Description
0:5	RWX	PB_CFG_EVENT_COMPB_TTYPE: PMU event compare B - Ttype
6:11	RWX	PB_CFG_EVENT_COMPB_TTYPE_MASK: PMU event compare B - Ttype mask
12:18	RWX	PB_CFG_EVENT_COMPB_TSIZE: PMU event compare B - tsize
19:25	RWX	PB_CFG_EVENT_COMPB_TSIZE_MASK: PMU event compare B - tsize mask
26:28	RWX	PB_CFG_EVENT_COMPB_SCOPE: PMU event compare B - scope
29:40	RWX	PB_CFG_EVENT_COMPB_PRESP: PMU event compare B - presp
41:52	RWX	PB_CFG_EVENT_COMPB_PRESP_MASK: PMU event compare B - presp mask
53:57	RWX	PB_CFG_EVENT_COMPB_CRESP: PMU event compare B - cresp
58:62	RWX	PB_CFG_EVENT_COMPB_CRESP_MASK: PMU event compare B - cresp mask
63	RWX	PB_CFG_EVENT_COMPB_CRESP_POLARITY: PMU event compare B - cresp polarity

Register Name	Processor Bus PB CENT CR ERROR Register
Mnemonic	EH.PB.MISC.PB_CENT_CR_ERROR
Address	0000000002010C6C (SCOM)
Attributes	
Description	00 = pb_cresp_error 01 = pb_cresp_addr_error 02 = pb_cfg_cresp_error_other 03:08 = pb_cfg_cresp_ttype 09:15 = pb_cfg_cresp_tsize 16:34 = pb_cfg_cresp_ttag 35:37 = pb_cfg_cresp_scope 38:42 = pb_cfg_cresp 43:54 = pb_cfg_presp

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is pb_cresp_error)
1	ROX	Reserved field. (Access type is pb_cresp_addr_error)
2	ROX	Reserved field. (Access type is pb_cfg_cresp_error_other)
3:8	ROX	Reserved field. (Access type is pb_cfg_cresp_ttype)
9:15	ROX	Reserved field. (Access type is pb_cfg_cresp_tsize)
16:34	ROX	Reserved field. (Access type is pb_cfg_cresp_ttag)



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Bits	SCOM	Field Mnemonic: Description
35:37	ROX	Reserved field. (Access type is pb_cfg_cresp_scope)
38:42	ROX	Reserved field. (Access type is pb_cfg_cresp)
43:54	ROX	Reserved field. (Access type is pb_cfg_presp)
55:63	RO	Constant = 0b000000000

Register Name	Processor Bus PBEH WEST Nest Domain FIR0 Register
Mnemonic	EH.PB.MISC.PB_WEST_FIR_REG
Address	0000000002010C00 (SCOM) 0000000002010C01 (SCOM1) 0000000002010C02 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX01_PBH_HW1_ERROR: pbiex01_pbh_hw1_error
1	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX01_PBH_HW2_ERROR: pbiex01_pbh_hw2_error
2	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX01_PBH_PROTOCOL_ERROR: pbiex01_pbh_protocol_error
3	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX01_PBH_OVERFLOW_ERROR: pbiex01_pbh_overflow_error
4	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX02_PBH_HW1_ERROR: pbiex02_pbh_hw1_error
5	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX02_PBH_HW2_ERROR: pbiex02_pbh_hw2_error
6	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX02_PBH_PROTOCOL_ERROR: pbiex02_pbh_protocol_error
7	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX02_PBH_OVERFLOW_ERROR: pbiex02_pbh_overflow_error
8	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX03_PBH_HW1_ERROR: pbiex03_pbh_hw1_error
9	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX03_PBH_HW2_ERROR: pbiex03_pbh_hw2_error
10	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX03_PBH_PROTOCOL_ERROR: pbiex03_pbh_protocol_error
11	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX03_PBH_OVERFLOW_ERROR: pbiex03_pbh_overflow_error
12	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX09_PBH_HW1_ERROR: pbiex09_pbh_hw1_error
13	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX09_PBH_HW2_ERROR: pbiex09_pbh_hw2_error
14	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX09_PBH_PROTOCOL_ERROR: pbiex09_pbh_protocol_error
15	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX09_PBH_OVERFLOW_ERROR: pbiex09_pbh_overflow_error
16	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX10_PBH_HW1_ERROR: pbiex10_pbh_hw1_error
17	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX10_PBH_HW2_ERROR: pbiex10_pbh_hw2_error
18	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX10_PBH_PROTOCOL_ERROR: pbiex10_pbh_protocol_error
19	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX10_PBH_OVERFLOW_ERROR: pbiex10_pbh_overflow_error



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
20	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX11_PBH_HW1_ERROR: pbiex11_pbh_hw1_error
21	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX11_PBH_HW2_ERROR: pbiex11_pbh_hw2_error
22	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX11_PBH_PROTOCOL_ERROR: pbiex11_pbh_protocol_error
23	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX11_PBH_OVERFLOW_ERROR: pbiex11_pbh_overflow_error
24	RWX	WOX_AND	WOX_OR	PB_WEST_DATA_OVERFLOW_ERROR: data_overflow_error
25	RWX	WOX_AND	WOX_OR	PB_WEST_DATA_PROTOCOL_ERROR: data_protocol_error
26	RWX	WOX_AND	WOX_OR	PB_WEST_DATA_ROUTE_ERROR: data_route_error
27	RWX	WOX_AND	WOX_OR	PB_WEST_CMD_OVERFLOW_ERROR: cmd_overflow_error
28	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_ERROR: fir_spare_error
29	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_0_ERROR: fir_spare_0_error
30	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_1_ERROR: fir_spare_1_error
31	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_2_ERROR: fir_spare_2_error
32	RWX	WOX_AND	WOX_OR	FIR_SCOM_WEST_ERR: PBEH WEST FIR_SCOM_err
33	RWX	WOX_AND	WOX_OR	FIR_SCOM_WEST_ERR_DUP: PBEH WEST FIR_SCOM_err
34:63	RO	N/A	N/A	Constant = 0b00000000000000000000000000000000

Register Name	Processor Bus PBEH WEST Nest Domain FIR MASK Register
Mnemonic	EH.PB.MISC.PB_WEST_FIR_MASK_REG
Address	0000000002010C03 (SCOM) 0000000002010C04 (SCOM1) 0000000002010C05 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX01_PBH_HW1_ERROR_MASK: pbiex01_pbh_hw1_error_mask
1	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX01_PBH_HW2_ERROR_MASK: pbiex01_pbh_hw2_error_mask
2	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX01_PBH_PROTOCOL_ERROR_MASK: pbiex01_pbh_protocol_error_mask
3	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX01_PBH_OVERFLOW_ERROR_MASK: pbiex01_pbh_overflow_error_mask
4	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX02_PBH_HW1_ERROR_MASK: pbiex02_pbh_hw1_error_mask
5	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX02_PBH_HW2_ERROR_MASK: pbiex02_pbh_hw2_error_mask
6	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX02_PBH_PROTOCOL_ERROR_MASK: pbiex02_pbh_protocol_error_mask
7	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX02_PBH_OVERFLOW_ERROR_MASK: pbiex02_pbh_overflow_error_mask

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
8	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX03_PBH_HW1_ERROR_MASK: pbiex03_pbh_hw1_error_mask
9	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX03_PBH_HW2_ERROR_MASK: pbiex03_pbh_hw2_error_mask
10	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX03_PBH_PROTOCOL_ERROR_MASK: pbiex03_pbh_protocol_error_mask
11	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX03_PBH_OVERFLOW_ERROR_MASK: pbiex03_pbh_overflow_error_mask
12	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX09_PBH_HW1_ERROR_MASK: pbiex09_pbh_hw1_error_mask
13	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX09_PBH_HW2_ERROR_MASK: pbiex09_pbh_hw2_error_mask
14	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX09_PBH_PROTOCOL_ERROR_MASK: pbiex09_pbh_protocol_error_mask
15	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX09_PBH_OVERFLOW_ERROR_MASK: pbiex09_pbh_overflow_error_mask
16	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX10_PBH_HW1_ERROR_MASK: pbiex10_pbh_hw1_error_mask
17	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX10_PBH_HW2_ERROR_MASK: pbiex10_pbh_hw2_error_mask
18	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX10_PBH_PROTOCOL_ERROR_MASK: pbiex10_pbh_protocol_error_mask
19	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX10_PBH_OVERFLOW_ERROR_MASK: pbiex10_pbh_overflow_error_mask
20	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX11_PBH_HW1_ERROR_MASK: pbiex11_pbh_hw1_error_mask
21	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX11_PBH_HW2_ERROR_MASK: pbiex11_pbh_hw2_error_mask
22	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX11_PBH_PROTOCOL_ERROR_MASK: pbiex11_pbh_protocol_error_mask
23	RWX	WOX_AND	WOX_OR	PB_WEST_PBIEX11_PBH_OVERFLOW_ERROR_MASK: pbiex11_pbh_overflow_error_mask
24	RWX	WOX_AND	WOX_OR	PB_WEST_DATA_OVERFLOW_ERROR_MASK: data_overflow_error_mask
25	RWX	WOX_AND	WOX_OR	PB_WEST_DATA_PROTOCOL_ERROR_MASK: data_protocol_error_mask
26	RWX	WOX_AND	WOX_OR	PB_WEST_DATA_ROUTE_ERROR_MASK: data_route_error_mask
27	RWX	WOX_AND	WOX_OR	PB_WEST_CMD_OVERFLOW_ERROR_MASK: cmd_overflow_error_mask
28	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_ERROR_MASK: fir_spare_error_mask
29	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_0_ERROR_MASK: fir_spare_0_error_mask
30	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_1_ERROR_MASK: fir_spare_1_error_mask
31	RWX	WOX_AND	WOX_OR	PB_WEST_FIR_SPARE_2_ERROR_MASK: fir_spare_2_error_mask
32	RWX	WOX_AND	WOX_OR	FIR_SCOM_WEST_ERR_MASK: PBEH WEST FIR_SCOM_err_mask
33	RWX	WOX_AND	WOX_OR	FIR_SCOM_WEST_ERR_MASK_DUP: PBEH WEST FIR_SCOM_err_mask



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
34:63	RO	N/A	N/A	Constant = 0b00000000000000000000000000000000

Register Name	<i>Processor Bus PBEH WEST Nest Domain FIR Action 0 Register</i>
Mnemonic	EH.PB.MISC.PB_WEST_FIR_ACTION0_REG
Address	0000000002010C06 (SCOM)
Attributes	
Description	

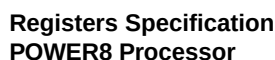
Bits	SCOM	Field Mnemonic: Description
0:33	RW	PB_WEST_FIR_ACTION0: Processor bus PBEH WEST nest domain FIR LSB of action select for corresponding bit in FIR. (Action0,Action1) = Action Select (0,0) = Checkstop (0,1) = Recoverable Error to Service Processor (1,0) = Recoverable Interrupt to Processor (1,1) = Invalid
34:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>Processor Bus PBEH WEST Nest Domain FIR Action 1 Register</i>
Mnemonic	EH.PB.MISC.PB_WEST_FIR_ACTION1_REG
Address	0000000002010C07 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:33	RW	PB_WEST_FIR_ACTION1: Processor bus PBEH WEST nest domain FIR LSB of action select for corresponding bit in FIR (Action0,Action1) = Action Select (0,0) = Checkstop (0,1) = Recoverable Error to Service Processor (1,0) = Recoverable Interrupt to Processor (1,1) = Invalid
34:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>Processor Bus PBEH CENT Nest Domain FIR0 Register</i>
Mnemonic	EH.PB.MISC.PB_CENT_FIR_REG
Address	0000000002010C40 (SCOM) 0000000002010C41 (SCOM1) 0000000002010C42 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PB_CENT_PROTOCOL_ERROR: protocol_error
1	RWX	WOX_AND	WOX_OR	PB_CENT_OVERFLOW_ERROR: overflow_error
2	RWX	WOX_AND	WOX_OR	PB_CENT_HW_PARITY_ERROR: hw_parity_error

[illegible]

Register Name	Processor Bus PBEH CENT Nest Domain FIR MASK Register
Mnemonic	EH.PB.MISC.PB_CENT_FIR_MASK_REG
Address	0000000002010C43 (SCOM) 0000000002010C44 (SCOM1) 0000000002010C45 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PB_CENT_PROTOCOL_ERROR_MASK: protocol_error_mask
1	RWX	WOX_AND	WOX_OR	PB_CENT_OVERFLOW_ERROR_MASK: overflow_error_mask
2	RWX	WOX_AND	WOX_OR	PB_CENT_HW_PARITY_ERROR_MASK: hw_parity_error_mask
3	RWX	WOX_AND	WOX_OR	PB_CENT_TLBIE_TM_TIMEOUT_ERROR_MASK: tlbie_tm_timeout_error_mask
4	RWX	WOX_AND	WOX_OR	PB_CENT_COHERENCY_ERROR_MASK: coherency_error_mask
5	RWX	WOX_AND	WOX_OR	PB_CENT_CRESP_ADDR_ERROR_MASK: cresp_addr_error_mask
6	RWX	WOX_AND	WOX_OR	PB_CENT_CRESP_ERROR_MASK: cresp_error_mask
7	RWX	WOX_AND	WOX_OR	PB_CENT_HANG_RECOVERY_LIMIT_ERROR_MASK: hang_recovery_limit_error_mask
8	RWX	WOX_AND	WOX_OR	PB_CENT_DATA_ROUTE_ERROR_MASK: data_route_error_mask
9	RWX	WOX_AND	WOX_OR	PB_CENT_HANG_RECOVERY_GTE_LEVEL1_MASK: hang_recovery_gte_level1_mask
10	RWX	WOX_AND	WOX_OR	PB_CENT_FORCE_MP_IPL_MASK: force_mp_ipl_mask
11	RWX	WOX_AND	WOX_OR	PB_CENT_FIR_SPARE_0_MASK: fir_spare_0_mask

[illegible]

Register Name	Processor Bus PBEH CENT Nest Domain FIR Action 0 Register
Mnemonic	EH.PB.MISC.PB_CENT_FIR_ACTION0_REG
Address	0000000002010C46 (SCOM)
Attributes	
Description	

[illegible]

Register Name	<i>Processor Bus PBEH CENT Nest Domain FIR Action 1 Register</i>
Mnemonic	EH.PB.MISC.PB_CENT_FIR_ACTION1_REG
Address	0000000002010C47 (SCOM)
Attributes	
Description	

[illegible]



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Register Name		Processor Bus PBEH East Nest Domain FIR0 Register		
Mnemonic		EH.PB.MISC.PB_EAST_FIR_REG		
Address		0000000002010C80 (SCOM) 0000000002010C81 (SCOM1) 0000000002010C82 (SCOM2)		
Attributes				
Description				
Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX04_PBH_HW1_ERROR: pbiex04_pbh_hw1_error
1	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX04_PBH_HW2_ERROR: pbiex04_pbh_hw2_error
2	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX04_PBH_PROTOCOL_ERROR: pbiex04_pbh_protocol_error
3	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX04_PBH_OVERFLOW_ERROR: pbiex04_pbh_overflow_error
4	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX05_PBH_HW1_ERROR: pbiex05_pbh_hw1_error
5	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX05_PBH_HW2_ERROR: pbiex05_pbh_hw2_error
6	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX05_PBH_PROTOCOL_ERROR: pbiex05_pbh_protocol_error
7	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX05_PBH_OVERFLOW_ERROR: pbiex05_pbh_overflow_error
8	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX06_PBH_HW1_ERROR: pbiex06_pbh_hw1_error
9	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX06_PBH_HW2_ERROR: pbiex06_pbh_hw2_error
10	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX06_PBH_PROTOCOL_ERROR: pbiex06_pbh_protocol_error
11	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX06_PBH_OVERFLOW_ERROR: pbiex06_pbh_overflow_error
12	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX12_PBH_HW1_ERROR: pbiex12_pbh_hw1_error
13	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX12_PBH_HW2_ERROR: pbiex12_pbh_hw2_error
14	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX12_PBH_PROTOCOL_ERROR: pbiex12_pbh_protocol_error
15	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX12_PBH_OVERFLOW_ERROR: pbiex12_pbh_overflow_error
16	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX13_PBH_HW1_ERROR: pbiex13_pbh_hw1_error
17	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX13_PBH_HW2_ERROR: pbiex13_pbh_hw2_error
18	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX13_PBH_PROTOCOL_ERROR: pbiex13_pbh_protocol_error
19	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX13_PBH_OVERFLOW_ERROR: pbiex13_pbh_overflow_error
20	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX14_PBH_HW1_ERROR: pbiex14_pbh_hw1_error
21	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX14_PBH_HW2_ERROR: pbiex14_pbh_hw2_error
22	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX14_PBH_PROTOCOL_ERROR: pbiex14_pbh_protocol_error
23	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX14_PBH_OVERFLOW_ERROR: pbiex14_pbh_overflow_error
24	RWX	WOX_AND	WOX_OR	PB_EAST_DATA_OVERFLOW_ERROR: data_overflow_error



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
25	RWX	WOX_AND	WOX_OR	PB_EAST_DATA_PROTOCOL_ERROR: data_protocol_error
26	RWX	WOX_AND	WOX_OR	PB_EAST_DATA_ROUTE_ERROR: data_route_error
27	RWX	WOX_AND	WOX_OR	PB_EAST_CMD_OVERFLOW_ERROR: cmd_overflow_error
28	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_ERROR: fir_spare_error
29	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_0_ERROR: fir_spare_0_error
30	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_1_ERROR: fir_spare_1_error
31	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_2_ERROR: fir_spare_2_error
32	RWX	WOX_AND	WOX_OR	FIR_SCOM_EAST_ERR: PBEH EAST FIR_SCOM_err
33	RWX	WOX_AND	WOX_OR	FIR_SCOM_EAST_ERR_DUP: PBEH EAST FIR_SCOM_err duplicate
34:63	RO	N/A	N/A	Constant = 0b00000000000000000000000000000000

Register Name	<i>Processor Bus PBEH EAST Nest Domain FIR MASK Register</i>
Mnemonic	EH.PB.MISC.PB_EAST_FIR_MASK_REG
Address	0000000002010C83 (SCOM) 0000000002010C84 (SCOM1) 0000000002010C85 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX04_PBH_HW1_ERROR_MASK: pbiex04_pbh_hw1_error_mask
1	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX04_PBH_HW2_ERROR_MASK: pbiex04_pbh_hw2_error_mask
2	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX04_PBH_PROTOCOL_ERROR_MASK: pbiex04_pbh_protocol_error_mask
3	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX04_PBH_OVERFLOW_ERROR_MASK: pbiex04_pbh_overflow_error_mask
4	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX05_PBH_HW1_ERROR_MASK: pbiex05_pbh_hw1_error_mask
5	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX05_PBH_HW2_ERROR_MASK: pbiex05_pbh_hw2_error_mask
6	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX05_PBH_PROTOCOL_ERROR_MASK: pbiex05_pbh_protocol_error_mask
7	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX05_PBH_OVERFLOW_ERROR_MASK: pbiex05_pbh_overflow_error_mask
8	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX06_PBH_HW1_ERROR_MASK: pbiex06_pbh_hw1_error_mask
9	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX06_PBH_HW2_ERROR_MASK: pbiex06_pbh_hw2_error_mask
10	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX06_PBH_PROTOCOL_ERROR_MASK: pbiex06_pbh_protocol_error_mask
11	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX06_PBH_OVERFLOW_ERROR_MASK: pbiex06_pbh_overflow_error_mask

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
12	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX12_PBH_HW1_ERROR_MASK: pbiex12_pbh_hw1_error_mask
13	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX12_PBH_HW2_ERROR_MASK: pbiex12_pbh_hw2_error_mask
14	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX12_PBH_PROTOCOL_ERROR_MASK: pbiex12_pbh_protocol_error_mask
15	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX12_PBH_OVERFLOW_ERROR_MASK: pbiex12_pbh_overflow_error_mask
16	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX13_PBH_HW1_ERROR_MASK: pbiex13_pbh_hw1_error_mask
17	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX13_PBH_HW2_ERROR_MASK: pbiex13_pbh_hw2_error_mask
18	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX13_PBH_PROTOCOL_ERROR_MASK: pbiex13_pbh_protocol_error_mask
19	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX13_PBH_OVERFLOW_ERROR_MASK: pbiex13_pbh_overflow_error_mask
20	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX14_PBH_HW1_ERROR_MASK: pbiex14_pbh_hw1_error_mask
21	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX14_PBH_HW2_ERROR_MASK: pbiex14_pbh_hw2_error_mask
22	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX14_PBH_PROTOCOL_ERROR_MASK: pbiex14_pbh_protocol_error_mask
23	RWX	WOX_AND	WOX_OR	PB_EAST_PBIEX14_PBH_OVERFLOW_ERROR_MASK: pbiex14_pbh_overflow_error_mask
24	RWX	WOX_AND	WOX_OR	PB_EAST_DATA_OVERFLOW_ERROR_MASK: data_overflow_error_mask
25	RWX	WOX_AND	WOX_OR	PB_EAST_DATA_PROTOCOL_ERROR_MASK: data_protocol_error_mask
26	RWX	WOX_AND	WOX_OR	PB_EAST_DATA_ROUTE_ERROR_MASK: data_route_error_mask
27	RWX	WOX_AND	WOX_OR	PB_EAST_CMD_OVERFLOW_ERROR_MASK: cmd_overflow_error_mask
28	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_ERROR_MASK: fir_spare_error_mask
29	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_0_ERROR_MASK: fir_spare_0_error_mask
30	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_1_ERROR_MASK: fir_spare_1_error_mask
31	RWX	WOX_AND	WOX_OR	PB_EAST_FIR_SPARE_2_ERROR_MASK: fir_spare_2_error_mask
32	RWX	WOX_AND	WOX_OR	FIR_SCOM_EAST_ERR_MASK: PBEH EAST FIR_SCOM_err_mask
33	RWX	WOX_AND	WOX_OR	FIR_SCOM_EAST_ERR_MASK_DUP: PBEH EAST FIR_SCOM_err_mask duplicate
34:63	RO	N/A	N/A	Constant = 0b00000000000000000000000000000000

Register Name	<i>Processor Bus PBEH EAST Nest Domain FIR Action 0 Register</i>
Mnemonic	EH.PB.MISC.PB_EAST_FIR_ACTION0_REG
Address	0000000002010C86 (SCOM)
Attributes	
Description	



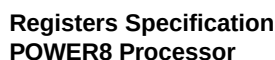
Bits	SCOM	Field Mnemonic: Description
0:33	RW	PB_EAST_FIR_ACTION0: Processor bus PBEH EAST nest domain FIR LSB of action select for corresponding bit in FIR. (Action0,Action1) = Action Select (0,0) = Checkstop (0,1) = Recoverable Error to Service Processor (1,0) = Recoverable Interrupt to Processor (1,1) = Invalid
34:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Processor Bus PBEH EAST Nest Domain FIR Action 1 Register
Mnemonic	EH.PB.MISC.PB_EAST_FIR_ACTION1_REG
Address	0000000002010C87 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:33	RW	PB_EAST_FIR_ACTION1: Processor bus PBEH EAST nest domain FIR LSB of action select for corresponding bit in FIR. (Action0,Action1) = Action Select (0,0) = Checkstop (0,1) = Recoverable Error to Service Processor (1,0) = Recoverable Interrupt to Processor (1,1) = Invalid
34:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Processor Bus EH EXTFIR Register
Mnemonic	EH.PB.MISC.EXTFIR_REG
Address	0000000002010C6E (SCOM) 0000000002010C6F (SCOM1) 0000000002010C70 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PB_X0_FIR_ERR: pb_x0_fir_err
1	RWX	WOX_AND	WOX_OR	PB_X1_FIR_ERR: pb_x1_fir_err
2	RWX	WOX_AND	WOX_OR	PB_X2_FIR_ERR: pb_x2_fir_err
3	RWX	WOX_AND	WOX_OR	PB_X3_FIR_ERR: pb_x3_fir_err
4	RWX	WOX_AND	WOX_OR	PB_A0_FIR_ERR: pb_a0_fir_err
5	RWX	WOX_AND	WOX_OR	PB_A1_FIR_ERR: pb_a1_fir_err
6	RWX	WOX_AND	WOX_OR	PB_A2_FIR_ERR: pb_a2_fir_err
7	RWX	WOX_AND	WOX_OR	EXTFIR_SCOM_ERROR: Processor bus EXTFIR SCOM error
8:63	RO	N/A	N/A	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000



Register Name	Processor Bus EXT FIR Mask Registers
Mnemonic	EH.PB.MISC.EXT FIR_MASK_REG
Address	0000000002010C71 (SCOM) 0000000002010C72 (SCOM1) 0000000002010C73 (SCOM2)
Attributes	
Description	

[illegible]

Register Name	Processor Bus EXT FIR Action 0 Register
Mnemonic	EH.PB.MISC.EXTFIR_ACTION0_REG
Address	000000002010C74 (SCOM)
Attributes	
Description	

[illegible]

Register Name	Processor Bus EXT FIR Action 1 Register
Mnemonic	EH.PB.MISC.EXTFIR_ACTION1_REG
Address	000000002010C75 (SCOM)
Attributes	
Description	

[illegible]

Register Name	Lock Indications From PLLs
Mnemonic	EH.TPCHIP.NET.PCBSLNEST.PLL_LOCK_REG
Address	0000000020F0019 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	ROX	Reserved field. (Access type is lock.)

Register Name	APC Master Processor Bus Control Register
Mnemonic	EN.NX.CXA.CXA_APC1.APCTL
Address	000000002013018 (SCOM)
Attributes	
Description	Controls processor bus operations.

Bits	SCOM	Field Mnemonic: Description
0:2	RO	Constant = 0b000
3	RW	APCCTL_ENB_CRESP_EXAM: Enables APC master examining cResps for it. When disabled, prevents false assertion of unexpected cresp FIR when cResps for PHB are seen. (APC RD FSM spoofs PHB unit ID).
4	RW	APCCTL_UNLIM_SCOPE: Unlimited Scope Only
5	RW	APCCTL_DIS_GRP_SCOPE: Disable Group Scope
6	RW	APCCTL_DIS_RGS: Disable Remote Group Scope
7	RW	APCCTL_HANG_ARE: Hang on Address Error
8	RW	APCCTL_HANG_DEAD: Hang on Ack_*dead
9	RW	APCCTL_CFG_BKILL_INC: cfg bkill inc
10:11	RW	RDBUFF_ALLOC: read buffer allocation when PHBs are enabled. 00 = CAPP owns all PHB read buffers. 01 = CAPP owns PHB read buffers 0,8,16,24. ignore cresps for others. 10 = CAPP owns no read buffers. ignore cresps for all. 11 = reserved.
12:13	RW	Reserved field. (Access type is spare)
14:38	RO	Constant = 0b000000000000000000000000
39:45	RW	WR_EPSILON_VALUE: write epsilon value
46:55	RO	Constant = 0b0000000000
56:63	RW	APCCTL_MAX_RETRY: Max Retry count. 0=retry forever.



Register Name		<i>MC Primary Memory Configuration Register (MCFGP)</i>
Mnemonic		MC0.MCS0.LEFT.LEFT.MCFGPQ
Address		0000000002011800 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0	RW	MCFGPQ_VALID: When set, MCFGP facility values are valid. If none of the MCS address configuration valid bits are set, no physical memory resides behind this MC, and the MC will ignore all reflected commands (that is, will not respond with lpc_ack).
1:3	RW	MCFGPQ_MCS_UNITS_PER_GROUP: The group size field below is the size of the entire group. For example, if the group size is 16 GB, and the chips per group is 4, then each memory controller in the group must have 4 GB of memory behind it. 1=>0b000 2=>0b001 3=>0b011 4=>0b010 6=>0b110 8=>0b100
4:8	RW	MCFGPQ_GROUP_MEMBER_IDENTIFICATION: Each MCS within a group must have a unique Group Member Identification (that is, no two MCS units within a defined group may have the same Group Member Identification setting). Also, all members of a unique group must have the same group_size and base_address settings.
9	RW	MCFGPQ_ENABLE_RCMD0: When set, the MCS will respond to reflected commands on RCMD0. When reset, the MCS will ignore reflected commands on RCMD0.
10	RW	MCFGPQ_ENABLE_RCMD1: When set, the MCS will respond to reflected commands on RCMD1. When reset, the MCS will ignore reflected commands on RCMD1.
11:23	RW	MCFGPQ_GROUP_SIZE: Because the minimum amount of memory behind any single memory controller is 4 GB, the 4 GB size setting must be accompanied by a memory controllers per group setting of 1.
24	RW	MCFGPQ_RESERVED_24: Reserved, must be set to 1.
25	RW	MCFGPQ_ENABLE_FASTPATH: When set, the MCS responds to fastpath commands. When reset, the MCS ignores fastpath commands.
26:43	RW	MCFGPQ_BASE_ADDRESS_OF_GROUP: MCFGPQ(0) must be set to zero when this field is modified.
44:63	RO	Constant = 0b00000000000000000000

Register Name		<i>MCS Primary Memory Configuration Register, Mirrored (MCFGPM)</i>
Mnemonic		MC0.MCS0.LEFT.LEFT.MCFGPMQ
Address		0000000002011801 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0	RW	MCFGPMQ_VALID: When set, MCFGPM facility values are valid. If none of the MCS address configuration valid bits are set, no physical memory resides behind this MC, and the MC will ignore all reflected commands (that is, will not respond with lpc_ack).
1:3	RW	MCFGPMQ_RESERVED_1_3: Reserved
4:8	RW	MCFGPMQ_RESERVED_4_8: Reserved



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Bits	SCOM	Field Mnemonic: Description
9:10	RW	MCFGPMQ_SPARE2: Reserved
11:23	RW	MCFGPMQ_GROUP_SIZE: Because the minimum amount of memory behind any single memory controller is 4 GB, the 4 GB size setting must be accompanied by a memory controllers per group setting of 1.
24:25	RW	MCFGPMQ_SPARE3: Reserved
26:43	RW	MCFGPMQ_BASE_ADDRESS_OF_GROUP: MCFGPMQ(0) must be set to zero when this field is modified.
44:63	RO	Constant = 0b000000000000000000000000

Register Name	<i>MCS Primary Memory Configuration Register, Register (MCFGPR)</i>
Mnemonic	MC0.MCS0.LEFT.LEFT.MCFGPRQ
Address	0000000002011802 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MCFGPRQ_VALID: When set, MCFGPR facility values are valid. If none of the MCS address configuration valid bits are set, no physical memory resides behind this MC, and the MC will ignore all reflected commands (that is, will not respond with lpc_ack).
1:5	RW	MCFGPRQ_SPARE0: Reserved.
6:19	RW	MCFGPRQ_BASE_ADDRESS: This 14-bit field is set to the starting real memory address of this Memory group. This value is compared to reflected address bits 14:27. Reflected command bits 28:60 (33 bits) are passed to the POWER8 Memory Buffer as an inband configuration address. Note that only one POWER8 Memory Buffer configuration register access can be in flight at a time. If MCMODE0(36) is set, only MCFGPR(6:18) are compared to reflected address bits 14:26, and reflected address bit 27 is sent to the POWER8 Memory Buffer as the HostOCC bit.
20:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>MCS Mode0 Register (MCSMODE0)</i>
Mnemonic	MC0.MCS0.LEFT.LEFT.MCMODE0Q
Address	0000000002011807 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MCMODE0Q_ENABLE_CMD_BYP_STUTTER: When set, MCS command bypass stutter is enabled.
1	RW	MCMODE0Q_RESERVED_1: Reserved
2	RW	MCMODE0Q_ENABLE_NS_RD_AO_SFU_FOR_DCBZ: When set, a DCBZ command to the POWER8 Memory Buffer is changed to a NS_RD_AO_SFU command, if the DCBZ secondary encode tt bits are non zero.
3	RW	MCMODE0Q_ENABLE_CENTAUR_LOCAL_CHECKSTOP_COMMAND: When set, enable the POWER8 Memory Buffer local checkstop command.
4:7	RW	MCMODE0Q_L3_PREFETCH_RETRY_THRESHOLD: If the MCS receives a pref_go_m, pref_go_s, cl_dma_rd, or cl_rd_nc ttype, and the allocate (a) bit is set, and the number of active read command list entries is greater than MCSMODE0(4:7) & 0 (where & = concatenated with), retry the operation (rty_lpc). This value must be greater than zero. SETU(1-10#10:11-14#40:15-15#50) SETN(10-14#25:15-15#75) SETS(10-14#25:15-15#75)



Bits	SCOM	Field Mnemonic: Description
8:11	RW	MCMODE0Q_NUMBER_OF_CL_ENTRIES_RESERVED_FOR_READ: Reserve 0 - 15 CL entries for read operations.
12:15	RW	MCMODE0Q_NUMBER_OF_CL_ENTRIES_RESERVED_FOR_MIRRORED_OPS: Reserve 0 - 15 CL entries for secondary mirror operations.
16:19	RW	MCMODE0Q_NUMBER_OF_CL_ENTRIES_RESERVED_FOR_WRITES: Reserve 0 - 15 CL entries for write operations.
20:23	RW	MCMODE0Q_NUMBER_OF_CL_ENTRIES_RESERVED_FOR_CP_WRITES: Reserve 0 - 15 CL entries for CP write operations.
24:27	RW	MCMODE0Q_NUMBER_OF_CL_ENTRIES_RESERVED_FOR_CP_IG: Reserve 0 - 15 CL entries for CP_ig write operations, fabric ttype = cp_ig.
28:31	RW	MCMODE0Q_NUMBER_OF_CL_ENTRIES_RESERVED_FOR_HTM_OPS: Reserve 0 to 15 CL entries for HTM operations, fabric ttype = htm_cl_w.
32:35	RW	MCMODE0Q_NUMBER_OF_CL_ENTRIES_RESERVED_FOR_HA_ASSIST: Reserve 0 to 15 CL entries for HA Assist fabric ttype, cl_dma_wr_hp.
36	RW	MCMODE0Q_MCFGPR_19_IS_HO_BIT: When set, MCFGPR(19) is not used for address decoding, and is passed to the POWER8 Memory Buffer as the HostOCC bit for error logging.
37	RW	MCMODE0Q_CL_CHANNEL_TIMEOUT_FORCES_CHANNEL_FAIL: When set, a command list channel timeout causes a channel fail. This forced channel fail action has the same affect on MCS logic as the mci_mcs_channel_fail input signal.
38	RW	MCMODE0Q_ENABLE_FAULT_LINE_FOR_GLOBAL_CHECKSTOP: When set, the fault line is driven for a global checkstop
39:40	RW	MCMODE0Q_RESERVED_39_40: Reserved
41:43	RW	MCMODE0Q_CHANNEL_ARB_SPEC_READ_HP_THRESHOLD: Number of read cresp commands sent on channel before spec read commands are made high priority
44:52	RW	MCMODE0Q_ADDRESS_COLLISION_MODES: When set, enables alternate address collision modes. To set all collision actions to 'retry', regardless of snoop or command list operation type, set this field to x1FE. 44: retry snoop hpc_wrCL rrto before cresp (ack if zero) 45: retry snoop hpc_wrCL wrto before cresp (ack if zero) 46: do not set error if snoop hpc_wrCL hpc_wr before cresp (set error if zero, always retry) 47: do not set error if snoop hpc_wrCL hpc_wr after cresp (set error if zero, always retry) 48: retry snoop ig_wr CL rrto before cresp (ack if zero) 49: retry snoop ig_wr CL wrto before cresp (ack if zero) 50: retry snoop ig_wr CL wrto after cresp (abort if zero) 51: retry snoop ig_wr CL hpc_wr after cresp (abort if zero, set only for test mode, can cause deadlock 52: abort snoop ig_wr CL ig_wr after cresp (retry if zero). SETU(Randomize#25:00000000#75, for retry all set to 111111110) SETN(000000000) SETS(000000000)
53	RW	MCMODE0Q_INCLUDE_CP_IG_IN_CP_WRITE_FULLNESS_GROUP: When set, CP_ig ops are included in the CP Write Fullness Group
54	RW	MCMODE0Q_ENABLE_DMAWR_CMD_BIT: When set, command bit 8 will be set for DMA write ops (for processor bus ttypes cl_dma_wr and dma_pr_w), regardless of the state of MCMODE2(60), Drive BC4 Write Command .
55	RW	MCMODE0Q_ENABLE_READ_LFSR_DATA: When set, LFSR data is substituted for memory read data, and the 65th bit is always zero. Good ECC is sent to the processor bus (unless ECC error injection is enabled). Sfstat is forced to a one for nodal scope operations. When this mode is set, MCMODE0(56), Force Channel Fail, must also be set before any memory accesses.
56	RW	MCMODE0Q_FORCE_CHANNEL_FAIL: When set, channel fail is forced. This forced channel fail action has the same affect on MCS logic as the mci_mcs_channel_fail input signal.
57	RW	MCMODE0Q_DISABLE_READ_CRC_ECC_BYPASS_TAKEN: When set, read CRCECC Bypass Taken mode is disabled (he upstream bypass bit from the POWER8 Memory Buffer is assumed to be zero). SIM ONLY, must not be set for lab testing!



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Bits	SCOM	Field Mnemonic: Description
58	RW	MCMODE0Q_DISABLE_CL_AO_QUEUES: When set, address protection only command list entries are disabled.
59:60	RW	MCMODE0Q_ADDRESS_SELECT_LFSR_VALUE: Selects address arb lfsr setting 4K=>0b00 2K=>0b01 1K=>0b10 256=>0b11
61	RW	MCMODE0Q_ENABLE_CENTAUR_SYNC: When set, this MCS is enabled to generate the POWER8 Memory Buffer Sync commands. Note that this bit should only be set in one MCS unit per POWER8 chip.
62	RW	MCMODE0Q_WRITE_DATA_BUFFER_ECC_CHECK_DISABLE: When set, ecc check is disabled for the write data buffer
63	RW	MCMODE0Q_WRITE_DATA_BUFFER_ECC_CORRECT_DISABLE: When set, ecc correct is disabled for the write data buffer

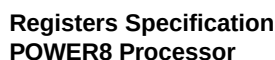
Register Name	MCS Mode1 Register (MCSMODE1)
Mnemonic	MC0.MCS0.LEFT.LEFT.MCMODE1Q
Address	0000000002011808 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MCMODE1Q_DISABLE_ADDRESS_SELECT_LFSR_MODE: When set, the LFSR that forces an arb cycle for mirror ops (into the snoop pipeline) is disabled.
1	RW	MCMODE1Q_NODAL_SCOPE_MCD_VALID: When set, the system contains a nodal scope MCD. Used for DCBZ and dclaim presp generation. Note that the presence of a group scope MCD does not alter MC behavior, so a configuration bit to specify the presence of a group scope MCD is not required.
2:6	RW	MCMODE1Q_DISABLE_HIGH_PRIORITY: When set, disable the high priority bit to the POWER8 Memory Buffer for rcmd ttypes: 2: rd_go_m 3: rd_go_s 4: rwitm 5: dclaim 6: dcbz This field disables the Qos bit in the processor bus type secondary encode, This field does not affect fastpath ops.
7:9	RW	MCMODE1Q_DISABLE_CRC_ECC_BYPASS: When set, disable the bypass bit to the POWER8 Memory Buffer for ttypes: 7 rd_go_m 8 rd_go_s 9 rwitm
10:15	RW	MCMODE1Q_DISABLE_READ_ALLOCATION_TO_CACHE: When set, do not allocate read data to the POWER8 Memory Buffer cache for ttypes: 10 rd_go_m 11 rd_go_s 12 pref_go_m 13 pref_go_s 14 cl_dma_rd 15 rwitm
16	RW	MCMODE1Q_DISABLE_READ_ALLOCATION_TO_CACHE_FOR_FASTPATH_OP: When set, do not allocate read data to the POWER8 Memory Buffer cache for fastpath ttypes
17	RW	MCMODE1Q_ENABLE_CRC_ECC_BYPASS_NODAL_SCOPE_ONLY: When set, CRCECC bypass is allowed only for nodal scope operations (if Disable CRCECC Bypass is not set). This bit affects rcmd dispatched ops only, does not affect fastpath dispatched ops.
18:26	RW	MCMODE1Q_DISABLE_SPEC_OPS_BY_SOURCE_AND_OR_SCOPE: When set, disable spec ops for: 18: source local 19: source near 20: source remote 21: source far 22: scope nodal 23: scope group 24: scope system 25: scope rgp 26: scope foreign
27:30	RW	MCMODE1Q_DISABLE_PREFETCH: When set, disable the prefetch to the POWER8 Memory Buffer for ttypes: 27: pref_go_m 28: pref_go_s 29: cl_dma_rd 30: cl_rd_nc
31	RW	MCMODE1Q_DISABLE_ALL_SPEC_OPS: When set, all speculative operations are disabled. Note that fastpath spec read ops are not disabled by this bit.

Bits	SCOM	Field Mnemonic: Description
32:48	RW	MCMODE1Q_DISABLE_SPEC_OP: When set, disable speculative ops for ttypes: 32: cl_rd_nc 33: rd_go_m 34: rd_go_s 35: cl_dma_rd 36: pref_go_m 37: pref_go_s 38: rwitm 39: dcbz 40: cp_ig 41: dma_pr_wr 42: dcbf* 43: armw* (include hca and pte_updt operations) 44: armwf* 45: dma_pr_rd 46: ci_pr_w 47: ci_pr_ooo_w 48: ci_pr_rd
49	RW	MCMODE1Q_DISABLE_OP_SOURCE_AND_SCOPE: When reset, disable spec ops for the (source(s) specified in MCSMODE1Q(18:21) OR the scope(s) specified in MCSMODE1Q(22:26)). When set, disable spec ops for the (source(s) specified in MCSMODE1Q(18:21) AND the scope(s) specified in MCSMODE1Q(22:26))
50:51	RW	MCMODE1Q_DISABLE_CACHE_INHIBITED: When set, a cache inhibited op allocates read data to the POWER8 Memory Buffer cache for ttypes: 50: cl_rd_nc 51: ci_pr_rd
52	RW	MCMODE1Q_DISABLE_ALL_MCS_COMMAND_BYPASS: When set, MCS bypass is disabled for all spec read ttypes
53:59	RW	MCMODE1Q_DISABLE_MCS_COMMAND_BYPASS: When set, MCS bypass is disabled for ttypes: 53: cl_rd_nc 54: rd_go_m 55: rd_go_s 56: cl_dma_rd 57: pref_go_m 58: pref_go_s 59: rwitm
60	RW	MCMODE1Q_ENABLE_DISABLE_SPEC_READ_FOR_NONDMA_GROUP_PUMP_LOCAL_READ: When set, spec reads are disabled for ttype rd_go_m, rd_go_s, pref_go_m, pref_go_s, and rwitm with scope = group and source = local.
61	RW	MCMODE1Q_ENABLE_DISABLE_SPEC_READ_FOR_NONDMA_SYSTEM_PUMP_LOCAL_READ: When set, spec reads are disabled for ttype rd_go_m, rd_go_s, pref_go_m, pref_go_s, and rwitm with scope = system and source = local.
62	RW	MCMODE1Q_DISABLE_FASTPATH_MCS_COMMAND_BYPASS: When set, MCS command bypass is disabled for fastpath reads
63	RW	MCMODE1Q_DISABLE_FASTPATH_CRC_ECC_BYPASS: When set, CRCECC bypass is disabled for fastpath reads

Register Name	<i>MCS Sync Command Register (MCSYNC)</i>	
Mnemonic	MC0.MCS0.LEFT.LEFT.MCSYNQC	
Address	00000000201180B (SCOM)	
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0:7	RW	MCSYNQC_MCS_SELECT: Selects which MCS unit generates sync commands specified by MCSYNC(8:15). Bit 0 is MCS0, Bit 1 is MCS1, and so on
8	RW	MCSYNQC_REFRESH_SYNC: When set, a refresh sync command is generated when MCMODE3(0) is set.
9	RW	MCSYNQC_CAL1_SYNC: When set, a calibration 1 timer sync command is generated when MCMODE3(0) is set.
10	RW	MCSYNQC_CAL2_SYNC: When set, a calibration 2 timer sync command is generated when MCMODE3(0) is set.
11	RW	MCSYNQC_CAL3_SYNC: When set, a calibration 3 timer sync command is generated when MCMODE3(0) is set.
12	RW	MCSYNQC_N_M_SYNC: When set, a NM Throttle counter sync command is generated when MCMODE3(0) is set.
13	RW	MCSYNQC_MB_TIMEBASE_SYNC: When set, a MB Timerbase sync command is generated when MCMODE3(0) is set.
14	RW	MCSYNQC_SUPER_SYNC: When set, a Super Sync command is generated when MCMODE3(0) is set.



Bits	SCOM	Field Mnemonic: Description
0	RW	MCMODE3Q_GENERATE_SYNC_GO_COMMAND: When set, a POWER8 Memory Buffer Sync command is generated. Must be reset and set again to generate another POWER8 Memory Buffer Sync command.
1:7	RW	MCMODE3Q_SYNC_REPLAY_TIMER_VALUE: Timer value, in units to 4 MCS clocks, used to determine if a replay event occurred during the sync command. The minimum value for this field is 2. If this field is set to 0 or 1, read sync status is not captured.
8	RW	MCMODE3Q_ALTERNATE_LOCAL_TIMER_TIMEBASE_SELECT: Used with MCSMODE3(24) and MCSMODE4(19) to set the timeout interval.
9:11	RW	MCMODE3Q_MIRROR_CONTROL_MODE: In default mode, MCS0 decodes even mirrored pair addresses, MCS1 decodes odd mirrored pair addresses. In inverse default mode, MCS0 decodes odd mirrored pair addresses, MCS1 decodes even mirrored pair addresses. Note that this field is defined only in MCS0, and is reserved in MCS1. DEFAULT_MODE=>0b000 RESEVED=>0b001 CL_AVAIL_MODE=>0b010 FAIL_MCS0=>0b100 FAIL_MCS1=>0b101 INVERSE_DEFAULT_MODE=>0b110
12:16	RW	MCMODE3Q_MIRROR_CL_AVAIL_MODE_THRESHOLD: Mirror CL Avail Mode Threshold. Note that this field is defined only in MCS0, and is reserved in MCS1.
17:19	RW	MCMODE3Q_MIRROR_TOGGLE_CONTROL_MODE: Control for mirror toggle mode. Note that this field is defined only in MCS0, and is reserved in MCS1.
20	RW	MCMODE3Q_USE_ALT_CRESP_BUS_SELECT: When set, bits 21 and 22 control which cresp bus is enabled
21	RW	MCMODE3Q_ENABLE_CRESP_BUS_0: When set, and bit 20 is set, enable cresp bus 0
22	RW	MCMODE3Q_ENABLE_CRESP_BUS_1: When set, and bit 20 is set, enable cresp bus 1
23	RW	MCMODE3Q_MPIPL_CL_RESET: When set, a MPIPL CL reset operation is started. This bit must be reset and set again to generate another MPIPL CL reset.
24	RW	MCMODE3Q_ENABLE_LOCAL_TIMEOUT_TIMEBASE: Used with MCSMODE3(8) and MCSMODE4(19) to set the timeout interval.
25:30	RW	MCMODE3Q_LOCAL_TIMEOUT_TIMEBASE_THRESHOLD: Local Timeout Timebase Threshold. Timebase value is (this field +1) times 2^16 nest clocks.
31	RW	MCMODE3Q_RESERVED_31: Reserved.
32:47	RW	MCMODE3Q_ALTERNATE_TIMEBASE_SELECTS: Alternate timeout timebase selects.
48:52	RW	MCMODE3Q_READ_RAMP_PERF_TRESHOLD: Read ramp performance threshold value.
53:63	RW	MCMODE3Q_RESERVED_53_63: Reserved.

Register Name		<i>MCS Mode4 Register (MCSCODE4)</i>
Mnemonic		MC0.MCS0.LEFT.LEFT.MCSCODE4Q
Address		000000000201181A (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0	RW	MCSCODE4Q_MCS_RESET_KEEPER: When set, c_err_rpt latches associated with MCERPT0 are held reset.
1	RW	MCSCODE4Q_DISABLE_FORCE_COMMAND_TAKEN_INACTIVE_DURING_CHECKSTOP: When set, an active checkstop signal (mcsx.right.mci_tc_fir_xstop, or tc_mc_fir_xstop) does not block all downstream commands (except checkstop).
2	RW	MCSCODE4Q_DISABLE_FORCE_CL_FULL_DURING_CHECKSTOP: When set, an active checkstop signal (mcsx.right.mci_tc_fir_xstop, or tc_mc_fir_xstop) does not force command list full.
3	RW	MCSCODE4Q_DISABLE_INHIBIT_MIRROR_REQ_AND_DONE_DURING_CHECKSTOP: When set, an active checkstop signal (mcsx.right.mci_tc_fir_xstop, or tc_mc_fir_xstop) does not disable the mirror req and done interfaces.
4:5	RW	MCSCODE4Q_CL_FULL_LFSR_SELECT: CL Full LFSR Select NO_LFSR=>0b00 LFSR_CL_FULL_EVERY_4K_CYCLES=>0b01 LFSR_CL_FULL_EVERY_16K_CYCLES=>0b10 LFSR_CL_FULL_EVERY_64K_CYCLES=>0b11
6	RW	MCSCODE4Q_ENABLE_CHANNEL_ARB_DISABLE_HP_OP_LFSR: When set, Channel Arb Disable HP Op LFSR is enabled (disable once every 64 cycles)
7	RW	MCSCODE4Q_ENABLE_CHANNEL_ARB_FORCE_WR_HP_LFSR: When set, Channel Arb Force Wr HP LFSR is enabled (force once every 256 cycles)
8	RW	MCSCODE4Q_MCS_WAT_CONTROL_0: WAT Control bit 0
9	RW	MCSCODE4Q_MCS_WAT_CONTROL_1: WAT Control bit 1
10	RW	MCSCODE4Q_MCS_WAT_CONTROL_2: WAT Control bit 2
11	RW	MCSCODE4Q_RESERVED_11: Reserved
12	RW	MCSCODE4Q_ENABLE_FIR_SPEC_ATTN: When set, MCS FIR recov_int output drives MCS spec_attn output.
13	RW	MCSCODE4Q_ENABLE_FIR_HOST_ATTN: When set, MCS FIR recov_int output drives MCS host_attn output
14	RW	MCSCODE4Q_ENABLE_PTE_UPDATE_OPS: pte_update operations are always enabled, and this bit is reserved.
15	RW	MCSCODE4Q_ENABLE_ALT_ADDR_SHIFT1: Valid only when number of MCS units per group is one.
16	RW	MCSCODE4Q_ENABLE_ALT_ADDR_SHIFT2: Valid only when number of MCS units per group is two.
17:18	RW	MCSCODE4Q_SELECT_RPTHANG_DECODE: Selects processor bus RPTHANG secondary encode field SEC_ENCODE_DATA_2_SEC_INTERVAL=>0b00 SEC_ENCODE_POLL_40_MS_INTERVAL=>0b01 SEC_ENCODE_CHECK_4_MS_INTERVAL=>0b10 IGNORE_RPTHANG_COMMAND=>0b11
19	RW	MCSCODE4Q_LOCAL_TIMEBASE_SELECT: Used with MCSCODE3(8) and MCSCODE3(24) to set the timeout interval.



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Bits	SCOM	Field Mnemonic: Description
20	RW	MCMODE4Q_DISABLE_RETRY_OTHER_CL_FULL: When set, retry_other is not driven for non-paam retry cl full cases.
21	RW	MCMODE4Q_DISABLE_POWERBUS_READ_AND_WRITE_RAMPS_DURING_CHECKSTOP: When set, an active checkstop signal (mcsx.right.mci_tc_fir_xstop, or tc_mc_fir_xstop) does not disable the processor bus read and write data ramp interfaces.
22	RW	MCMODE4Q_DISABLE_MDI01_UPDATE_INTERFACE: When set, the MDI01 update interface from the POWER8 Memory Buffer is disabled.
23	RW	MCMODE4Q_FLR_ACTIVE_FOR_FAR_SOURCE_ONLY: When set, Foreign Link Recovery is active only for foreign scope command with far source.
24	RW	MCMODE4Q_FIR45_SET_FOR_MPIPL_AND_FLR: When reset, FIR(45) is set only during MPIPL cleanup. When set, FIR(45) can be set for MPIPL cleanup or Foreign Link Recovery.
25	RW	MCMODE4Q_ENABLE_DISABLE_PREFETCH_FOR_MIRROR_READS: When set, prefetch commands to the POWER8 Memory Buffer are changed to non-prefetch commands for mirror reads.
26	RW	MCMODE4Q_FORCE_NONINBAND_CL_FULL: When set, force cl full for non-inband operations.
27	RW	MCMODE4Q_ENABLE_READ_RAMP_VENDD1_PERFORMANCE_IMPROVEMENT: When set, enables POWER8 read ramp performance improvement.
28	RW	MCMODE4Q_RETRY_DATA_CHECK_UNTIL_FP_RCMD: When set, enables retry of data check until all rcmds associated with fastpath ops are received.
29	RW	MCMODE4Q_ENABLE_CP_M_WRITE_MDI0_ALL_SOURCES: When set, cp_m writes of all source types write the mdi bit to zero.
30:31	RW	MCMODE4Q_RESERVED_30_31: Reserved
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	MC Primary Memory Configuration Alternate Register (MCFGPA)
Mnemonic	MC0.MCS0.LEFT.LEFT.MCFGPAQ
Address	0000000002011814 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MCFGPAQ_VALID: When set, MCFGPA facility values are valid.
1:3	RW	MCFGPAQ_RESERVED_1_3: Reserved
4:8	RW	MCFGPAQ_RESERVED_4_8: Reserved
9:10	RW	MCFGPAQ_RESERVED_9_10: Reserved
11:23	RW	MCFGPAQ_GROUP_SIZE: Because the minimum amount of memory behind any single memory controller is 4 GB, the 4 GB size setting must be accompanied by a memory controllers per group setting of 1.
24:25	RW	MCFGPAQ_RESERVED_24_25: Reserved
26:43	RW	MCFGPAQ_BASE_ADDRESS_OF_GROUP: For example, a 16 GB group must have MCFGPA(42:43) set to b00. A 32 GB group must have MCFGPA(41:43) set to b000. A 64 GB group must have MCFGPA(40:43) set to b0000.
44:63	RO	Constant = 0b000000000000000000000000



Register Name		<i>MCS Primary Memory Configuration Register, Mirrored Alternate (MCFGPMA)</i>
Mnemonic		MC0.MCS0.LEFT.LEFT.MCFGPMAQ
Address		0000000002011815 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0	RW	MCFGPMAQ_VALID: When set, MCFGPMA facility values are valid.
1:3	RW	MCFGPMAQ_RESERVED_1_3: Reserved
4:8	RW	MCFGPMAQ_RESERVED_4_8: Reserved
9:10	RW	MCFGPMAQ_RESERVED_9_10: Reserved
11:23	RW	MCFGPMAQ_GROUP_SIZE: Because the minimum amount of memory behind any single memory controller is 4 GB, the 4 GB size setting must be accompanied by a memory controllers per group setting of 1.
24:25	RW	MCFGPMAQ_RESERVED_24_25: Reserved
26:43	RW	MCFGPMAQ_BASE_ADDRESS_OF_GROUP: A 16 GB group must have MCFGPMA(42:43) set to b00. A 32 GB group must have MCFGPMA(41:43) set to b000. A 64 GB group must have MCFGPMA(40:43) set to b0000.
44:63	RO	Constant = 0b000000000000000000000000

Register Name		<i>MCS Epsilon Register (MCEPS)</i>
Mnemonic		MC0.MCS0.LEFT.LEFT.MCEPSQ
Address		0000000002011816 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:7	RW	MCEPSQ_JITTER_EPSILON: Epsilon value for ops not requiring epsilon protection SETU(Randomize) SETN(tbd) SETS(tbd)
8:15	RW	MCEPSQ_NODAL_EPSILON: Epsilon value for nodal scope ops requiring epsilon protection SETU(Randomize) SETN(tbd) SETS(tbd)
16:23	RW	MCEPSQ_GROUP_EPSILON: Epsilon value for group scope ops requiring epsilon protection SETU(Randomize) SETN(tbd) SETS(tbd)
24:31	RW	MCEPSQ_SYSTEM_OR_RGP_EPSILON: Epsilon value for system or RGP scope ops requiring epsilon protection SETU(Randomize) SETN(tbd) SETS(tbd)
32:39	RW	MCEPSQ_FOREIGN_EPSILON: Epsilon value for foreign scope ops requiring epsilon protection SETU(Randomize) SETN(tbd) SETS(tbd)
40:63	RO	Constant = 0b000000000000000000000000

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Register Name		MCI Fault Isolation Register (MCIFIR)		
Mnemonic		MC0.MCS0.RIGHT.MCIFIRQ		
Address		0000000002011840 (SCOM) 0000000002011841 (SCOM1) 0000000002011842 (SCOM2)		
Attributes				
Description				
Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	MCIFIRQ_REPLAY_TIMEOUT: If 0 EDI channel is operational. If 1 Too many EDI replays due to CRC error. There's no forward progress.
1	RWX	WOX_AND	WOX_OR	MCIFIRQ_CHANNEL_FAIL: NOTE: Look at the EDI FIR for details. NOTE: This bit must be reset in the EDI phy.
2	RWX	WOX_AND	WOX_OR	MCIFIRQ_CRC_ERROR: If 0 No CRC errors detected. If 1 A CRC error is detected by receiver.
3	RWX	WOX_AND	WOX_OR	MCIFIRQ_FRAME_NOACK: If 0 All transmitted frames have been acknowledged If 1 A transmitted frame did not get a Positive Acknowledge.
4	RWX	WOX_AND	WOX_OR	MCIFIRQ_SEQID_OUT_OF_ORDER: If 0 All received frames ID are in sequential order during non-replay transfer. If 1 Received frames ID are not in sequential order during non-replay transfer.
5	RWX	WOX_AND	WOX_OR	MCIFIRQ_REPLAY_BUFFER_ECC_CE: If 0 No ECC Correctable Error detected. If 1 An ECC Correctable Error was detected in the replay buffer.
6	RWX	WOX_AND	WOX_OR	MCIFIRQ_REPLAY_BUFFER_ECC_UE: If 0 No ECC UnCorrectable Error detected. If 1 An ECC UnCorrectable Error was detected in the replay buffer.
7	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCI_CHINIT_STATE_MACHINE_TIMEOUT: If 1 An internal MCI state machine did not get a response within a programmable time interval.
8	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCI_INTERNAL_CONTROL_PARITY_ERROR: If 1 An internal MCI state machine parity error was detected.
9	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCI_DATA_FLOW_PARITY_ERROR: If '1', a parity error was detected on the downstream data flow.
10	RWX	WOX_AND	WOX_OR	MCIFIRQ_CRC_PERFORMANCE_DEGRADATION: If '1' the EDI bus performance has degraded by 1% of the channel bandwidth.
11	RWX	WOX_AND	WOX_OR	MCIFIRQ_CHANNEL_INTERLOCK_FAIL: If '1', an error condition was detected during the channel interlock window
12	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_CHECKSTOP: If '1', an active POWER8 Memory Buffer checkstop bit was detected in an upstream attention packet
13	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_TRACESTOP: If '1', an active POWER8 Memory Buffer tracestop bit was detected in an upstream attention packet
14	RWX	WOX_AND	WOX_OR	MCIFIRQ_FPGA_INTERRUPT: If '1' an active FPGA interrupt bit was detected in an upstream attention packet
15	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_RECOVERABLE_ERROR: If '1', an active POWER8 Memory Buffer recoverable error bit was detected in an upstream attention packet
16	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_SPECIAL_ATTENTION: If '1', an active POWER8 Memory Buffer special attention bit was detected in an upstream attention packet
17	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_MAINTENANCE_COMPLETE: If '1', an active POWER8 Memory Buffer maintenance complete bit was detected in an upstream attention packet



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
18	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_INBAND_PIB_ERROR: If '1', an active POWER8 Memory Buffer inband PIB error bit was detected in an upstream attention packet
19	RWX	WOX_AND	WOX_OR	MCIFIRQ_FRTL_COUNTER_OVERFLOW: If '1' the FRTL counter has overflowed or wrapped around
20	RWX	WOX_AND	WOX_OR	MCIFIRQ_SCOM_WR_PERR: If '1', a SCOM register parity error has been detected. This error does not include parity errors on mcicfgq.
21	RWX	WOX_AND	WOX_OR	MCIFIRQ_MULTIPLE_REPLAY: A replay event was detected while the transmitter was in replay.
22	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCICFG_WR_PERR: If '1', a parity error has been detected on mcicfgq.
23	RWX	WOX_AND	WOX_OR	MCIFIRQ_REPLAY_BUFFER_OVERRUN: If '1', a new frame taken when all replay buffers are in use.
24	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_RECOVERABLE_ERROR: If '1', a MCS recoverable error was detected. See the MCERPT0 register description for a list of errors that cause this FIR to be set.
25	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_INTERNAL_NONRECOVERABLE_ERROR: If '1', an internal MCS nonrecoverable error was detected. See the MCERPT0 register description for a list of errors that cause this FIR to be set.
26	RWX	WOX_AND	WOX_OR	MCIFIRQ_POWERBUS_PROTOCOL_ERROR: If '1', a processor bus protocol error was detected. (for example, a HPC_WR is snooped when a HPC_WR to the same address is active)
27	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_COMMAND_LIST_TIMEOUT: If '1', a command list state machine has timed out
28	RWX	WOX_AND	WOX_OR	MCIFIRQ_MULTIPLE_RCMD_OR_CRESP_ACTIVE: If '1', a cresp command is active on cresp bus0 and bus1 in the same cycle, or a valid non-inband command is active on rcmd0 and a valid non-inband command is active on rcmd1 in the same cycle. Note the rcmd validity for this check does not include alternate, foreign hole, or HA BAR checking. Note that cresp portion of this checker is enabled only if MCFGPM(0) or MCFGPM(0) is set.
29	RWX	WOX_AND	WOX_OR	MCIFIRQ_INBAND_BAR_HIT_WITH_INCORRECT_TTYPE: If '1', a command was issued to inband address space using a ttype the MCS responds to, but other than ttypes: (8-byte CI_PR_W, 8-byte CI_PR_RD, CL_RD_NC, CHGRATE, RPTHANG, or LINK_CHK)
30	RWX	WOX_AND	WOX_OR	MCIFIRQ_MULTIPLE_BAR_HIT: If '1', an address match on more than one Memory BAR was detected
31	RWX	WOX_AND	WOX_OR	MCIFIRQ_CHANNEL_FAIL_SIGNAL_ACTIVE: If '1', the MCS logic is in the channel fail state
32	RWX	WOX_AND	WOX_OR	MCIFIRQ_MIRROR_ACTION_OCCURRED: If '1', a channel fail or read SUE was detected on a primary mirror read access, causing a secondary mirror request. This FIR is set when secondary mirror commands with types of 000 (ns_rd), 001 (ns_rd_sfu), or 111 (ns_rmw_f)
33	RWX	WOX_AND	WOX_OR	MCIFIRQ_INVALID_FOREIGN_BAR_ACCESS: If '1', an invalid foreign BAR access has occurred.
34	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_SYNC_COMMAND_DETECTED: If '1', a POWER8 Memory Buffer Sync Command was detected in the MCS car1 cycle, because of a processor bus 8-byte ci_pr_w sync command.
35	RWX	WOX_AND	WOX_OR	MCIFIRQ_POWERBUS_WRITE_DATA_BUFFER_CE: If '1', a CE was detected on a read of the processor bus write data buffer.

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
36	RWX	WOX_AND	WOX_OR	MCIFIRQ_POWERBUS_WRITE_DATA_BUFFER_UE: If '1', a UE was detected on a read of the processor bus write data buffer.
37	RWX	WOX_AND	WOX_OR	MCIFIRQ_POWERBUS_WRITE_DATA_BUFFER_SUE: If '1', a SUE was detected on a read of the processor bus write data buffer.
38	RWX	WOX_AND	WOX_OR	MCIFIRQ_HA_ILLEGAL_CONSUMER_ACCESS_ERROR: If '1', a HA Illegal Consumer Access Error was detected.
39	RWX	WOX_AND	WOX_OR	MCIFIRQ_HA_ILLEGAL_PRODUCER_ACCESS_ERROR: If '1', a HA Illegal Producer Access Error was detected.
40	RWX	WOX_AND	WOX_OR	MCIFIRQ_CHANNEL_TIMEOUT_ERROR: If '1', a Channel Timeout Error was detected. If MCMODE0(37) is set to force a channel fail if a channel timeout error is detected, this FIR should be set to recoverable. If MCMODE0(37) is not set, so a channel timeout does not force a channel fail, this FIR should be set to non-recoverable. If a channel fail occurs, the conditions causing this FIR bit to be set are blocked.
41	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_FAULT_LINE: If '1', the POWER8 Memory Buffer fault line input has gone active (low)
42	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_WAT: If '1', a MCS WAT event has occurred, an has been programmed to set this FIR
43	RWX	WOX_AND	WOX_OR	MCIFIRQ_INVALID_ADDRESS: If '1', the MCS has received an address in the high half of MCFGPMCFGPM, that is not defined by MCFGPAMCFGPMA
44	RWX	WOX_AND	WOX_OR	MCIFIRQ_COMMAND_LIST_TIMEOUT_RCMD_TO_CRESP_WRITE_DATA_AVAILABLE: If '1', a MCS command list has timed out between the dispatch (due to fastpath or rcmd) and combined response for a read operation, or between dispatch and combined response and write data arrival for a write operation.
45	RWX	WOX_AND	WOX_OR	MCIFIRQ_MPIPL_OR_FLR_WRITE_SUE: If '1', a SCOM MPIPL cleanup or Foreign Link Recovery (FLR) operation has caused a SUE to be written to memory. MCMODE4(24) controls the setting of this FIR. This FIR is set once for each cache line written to memory with a SUE.
46	RWX	WOX_AND	WOX_OR	MCIFIRQ_INVALID_CENTAUR_BYPASS: If '1', the POWER8 Memory Buffer returns an op marked as bypass that is unexpected by the MCS (command not bypassable). The upstream bypass bit evaluated for this check is crc qualified.
47	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_WRITE_DATAFLOW_SUE: If '1', a SUE error was detected in the MCS write dataflow, due to a write buffer UE or SUE, or a MPIPL or foreign link recovery write operation.
48	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_EXTRA_FIR_0: If '1', Extra_FIR_0 was detected in the MCS.
49	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_EXTRA_FIR_1: If '1', Extra_FIR_1 was detected in the MCS.
50	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_EXTRA_FIR_2: If '1', Extra_FIR_2 was detected in the MCS.
51	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_EXTRA_FIR_3: If '1', Extra_FIR_3 was detected in the MCS.
52	RWX	WOX_AND	WOX_OR	MCIFIRQ_INTERNAL_SCOM_ERROR: Internal SCOM Error
53	RWX	WOX_AND	WOX_OR	MCIFIRQ_INTERNAL_SCOM_ERROR_CLONE: Internal SCOM Error Clone
54:63	RO	N/A	N/A	Constant = 0b0000000000



Register Name		<i>MC I Fault Isolation Mask Register (MCIFIRMASK)</i>		
Mnemonic		MC0.MCS0.RIGHT.MCIFIRMASK		
Address		0000000002011843 (SCOM) 0000000002011844 (SCOM1) 0000000002011845 (SCOM2)		
Attributes				
Description				
Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	MCIFIRMASK_REPLAY_TIMEOUT_MASK: Masks FIR(0)
1	RW	WO_AND	WO_OR	MCIFIRMASK_CHANNEL_FAIL_MASK: Masks FIR(1)
2	RW	WO_AND	WO_OR	MCIFIRMASK_CRC_ERROR_MASK: Masks FIR(2)
3	RW	WO_AND	WO_OR	MCIFIRMASK_FRAME_NOACK_MASK: Masks FIR(3)
4	RW	WO_AND	WO_OR	MCIFIRMASK_SEQID_OUT_OF_ORDER_MASK: Masks FIR(4)
5	RW	WO_AND	WO_OR	MCIFIRMASK_REPLAY_BUFFER_ECC_CE_MASK: Masks FIR(5)
6	RW	WO_AND	WO_OR	MCIFIRMASK_REPLAY_BUFFER_ECC_UE_MASK: Masks FIR(6)
7	RW	WO_AND	WO_OR	MCIFIRMASK_MCI_CHINIT_STATE_MACHINE_TIMEOUT: Masks FIR(7)
8	RW	WO_AND	WO_OR	MCIFIRMASK_MCI_INTERNAL_CONTROL_PARITY_ERROR: Masks FIR(8)
9	RW	WO_AND	WO_OR	MCIFIRMASK_MCI_DATA_FLOW_PARITY_ERROR: Masks FIR(9)
10	RW	WO_AND	WO_OR	MCIFIRMASK_CRC_PERFORMANCE_DEGRADATION: Masks FIR(10)
11	RW	WO_AND	WO_OR	MCIFIRMASK_SPARE0: Reserved
12	RW	WO_AND	WO_OR	MCIFIRMASK_CENTAUR_CHECKSTOP: Masks FIR(12)
13	RW	WO_AND	WO_OR	MCIFIRMASK_CENTAUR_TRACESTOP: Masks FIR(13)
14	RW	WO_AND	WO_OR	MCIFIRMASK_FPGA_INTERRUPT: Masks FIR(14)
15	RW	WO_AND	WO_OR	MCIFIRMASK_CENTAUR_RECOVERABLE_ERROR: Masks FIR(15)
16	RW	WO_AND	WO_OR	MCIFIRMASK_CENTAUR_SPECIAL_ATTENTION: Masks FIR(16)
17	RW	WO_AND	WO_OR	MCIFIRMASK_CENTAUR_MAINTENANCE_COMPLETE: Masks FIR(17)
18	RW	WO_AND	WO_OR	MCIFIRMASK_CENTAUR_INBAND_PIB_ERROR: Masks FIR(18)
19	RW	WO_AND	WO_OR	MCIFIRMASK_FRTL_COUNTER_OVERFLOW: Masks FIR(19)
20	RW	WO_AND	WO_OR	MCIFIRMASK_SCOM_WR_PERR: Masks FIR(20)
21	RW	WO_AND	WO_OR	MCIFIRMASK_MULTIPLE_REPLAY: Masks FIR(21)
22	RW	WO_AND	WO_OR	MCIFIRMASK_MCICFG_WR_PERR: Masks FIR(22)
23	RW	WO_AND	WO_OR	MCIFIRMASK_REPLAY_BUFFER_OVERRUN: Masks FIR(23)
24	RW	WO_AND	WO_OR	MCIFIRMASK_MCS_RECOVERABLE_ERROR: Masks FIR(24)
25	RW	WO_AND	WO_OR	MCIFIRMASK_MCS_INTERNAL_NONRECOVERABLE_ERROR: Masks FIR(25)
26	RW	WO_AND	WO_OR	MCIFIRMASK_POWERBUS_PROTOCOL_ERROR: Masks FIR(26)
27	RW	WO_AND	WO_OR	MCIFIRMASK_MCS_COMMAND_LIST_TIMEOUT_DUE_TO_POWERBUS: Masks FIR(27)
28	RW	WO_AND	WO_OR	MCIFIRMASK_MULTIPLE_RCMD_OR_CRESP_ACTIVE: Masks FIR(28)
29	RW	WO_AND	WO_OR	MCIFIRMASK_INBAND_BAR_HIT_WITH_INCORRECT_TTYPE: Masks FIR(29)

Registers Specification

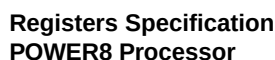
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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
30	RW	WO_AND	WO_OR	MCIFIRMASK_MULTIPLE_BAR_HIT: Masks FIR(30)
31	RW	WO_AND	WO_OR	MCIFIRMASK_CHANNEL_FAIL_SIGNAL_ACTIVE: Masks FIR(31)
32	RW	WO_AND	WO_OR	MCIFIRMASK_MIRROR_ACTION_OCCURRED: Masks FIR(32)
33	RW	WO_AND	WO_OR	MCIFIRMASK_NONFOREIGN_ACCESS_TO_FOREIGN_BAR: Masks FIR(33)
34	RW	WO_AND	WO_OR	MCIFIRMASK_CENTAUR_SYNC_COMMAND_DETECTED: Masks FIR(34)
35	RW	WO_AND	WO_OR	MCIFIRMASK_POWERBUS_WRITE_DATA_BUFFER_CE: Masks FIR(35)
36	RW	WO_AND	WO_OR	MCIFIRMASK_POWERBUS_WRITE_DATA_BUFFER_UE: Masks FIR(36)
37	RW	WO_AND	WO_OR	MCIFIRMASK_POWERBUS_WRITE_DATA_BUFFER_SUE: Masks FIR(37)
38	RW	WO_AND	WO_OR	MCIFIRMASK_HA_ILLEGAL_CONSUMER_ACCESS_ERROR: Masks FIR(38)
39	RW	WO_AND	WO_OR	MCIFIRMASK_HA_ILLEGAL_PRODUCER_ACCESS_ERROR: Masks FIR(39)
40	RW	WO_AND	WO_OR	MCIFIRMASK_CHANNEL_TIMEOUT_ERROR: Masks FIR(40)
41	RW	WO_AND	WO_OR	MCIFIRMASK_CENTAUR_FAULT_LINE: Masks FIR(41)
42	RW	WO_AND	WO_OR	MCIFIRMASK_MCS_WAT: Masks FIR(42)
43	RW	WO_AND	WO_OR	MCIFIRMASK_INVALID_ADDRESS: Masks FIR(43)
44	RW	WO_AND	WO_OR	MCIFIRMASK_COMMAND_LIST_TIMEOUT_RCMD_TO_CRESP_WRITE_DATA_AVAILABLE: Masks FIR(44)
45	RW	WO_AND	WO_OR	MCIFIRMASK_MPIPL_OR_FLR_WRITE_SUE: Masks FIR(45)
46	RW	WO_AND	WO_OR	MCIFIRMASK_INVALID_CENTAUR_BYPASS: Masks FIR(46)
47	RW	WO_AND	WO_OR	MCIFIRMASK_MCS_WRITE_DATAFLOW_SUE: Masks FIR(47)
48	RW	WO_AND	WO_OR	MCIFIRMASK_MCS_EXTRA_FIR_0: Masks FIR(48)
49	RW	WO_AND	WO_OR	MCIFIRMASK_MCS_EXTRA_FIR_1: Masks FIR(49)
50	RW	WO_AND	WO_OR	MCIFIRMASK_MCS_EXTRA_FIR_2: Masks FIR(50)
51	RW	WO_AND	WO_OR	MCIFIRMASK_MCS_EXTRA_FIR_3: Masks FIR(51)
52	RW	WO_AND	WO_OR	MCIFIRMASK_INTERNAL_SCOM_ERROR: Masks FIR(52)
53	RW	WO_AND	WO_OR	MCIFIRMASK_INTERNAL_SCOM_ERROR_CLONE: Mask FIR(53)
54:63	RO	N/A	N/A	Constant = 0b0000000000

Register Name	<i>MCI Fault Isolation Action0 Register (MCIFIRACT0)</i>		
Mnemonic	MC0.MCS0.RIGHT.MCIFIRACT0		
Address	0000000002011846 (SCOM)		
Attributes			
Description			
Bits	SCOM	Field Mnemonic: Description	
0:53	RW	MCIFIRACT0_ACTION_0: Action 0 for FIR(0:53)	
54:63	RO	Constant = 0b0000000000	

Register Name		<i>MCI Fault Isolation Action1 Register (MCIFIRACT1)</i>
Mnemonic		MC0.MCS0.RIGHT.MCIFIRACT1
Address		0000000002011847 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:53	RW	MCIFIRACT1_ACTION_0: Action 0 for FIR(0:53)
54:63	RO	Constant = 0b0000000000

Register Name		<i>MCI Configuration Register (MCICFGQ)</i>
Mnemonic		MC0.MCS0.RIGHT.MCICFGQ
Address		000000000201184A (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0	RW	MCICFGQ_FORCE_CHANNEL_FAIL: If 1 the MCI will enter the channel fail state
1	RW	MCICFGQ_REPLAY_CRC_DISABLE: If 0 EDI frames will be replayed, by the transmitter, when a frame crc error is detected. If 1 EDI frames will not be replayed, by the transmitter, when a frame crc error occurs.
2	RW	MCICFGQ_REPLAY_NOACK_DISABLE: If 0 EDI frames will be replayed, by the transmitter, when the frame does not get acknowledged when the FRTL timer expires. If 1 EDI frames will not be replayed, by the transmitter, when the frame does not get acknowledged when the FRTL timer expires.
3	RW	MCICFGQ_REPLAY_OUTOFORDER_DISABLE: If 0 EDI frames will be replayed, by the transmitter, when an out of order Sequence ID is detected. If 1 EDI frames will not be replayed, by the transmitter, when an out-of-order Sequence ID is detected.
4	RWX	MCICFGQ_FORCE_LFSR_REPLAY: If 1 EDI frames are replayed from the replay buffer when an LFSR pulse is detected by the replay controller. Setting this bit will result in multiple frame replays.
5	RW	MCICFGQ_CRC_CHECK_DISABLE: If 0 EDI frames will be checked for CRC errors. If 1 EDI frames will not be checked for CRC errors.
6	RW	MCICFGQ_ECC_CHECK_DISABLE: If 0 EDI frames from the replay buffer will be checked for ECC errors. If 1 EDI frames from the replay buffer will not be checked for ECC errors.
7	RWX	MCICFGQ_START_FRAME_LOCK: If 1 Start EDI frame start generation. Sixteen 9.6GHz (or 4 2.4 GHz) beats of all ones, except the crc bits, is transmitted for the receiver to determine the incoming EDI frame boundaries.
8	RWX	MCICFGQ_START_FRTL: If 1 Start EDI Frame Round Trip Latency calculation. The transmitter sends a null frame and the receiver response with an acknowledge frame. The FRTL is the time the transmitter sends the first block of data for the null frame to the time the transmitter receives the first block of data for the acknowledge frame.
9	RW	MCICFGQ_AUTO_FRTL_DISABLE: If 0 Frame Round Trip Latency of EDI frames will automatically be generated by hardware. If 1 Disable the automatic calculation of EDI Frame Round Trip Latency by hardware. This bit should be set when the FRTL value is set manually in bits 10 to16.
10:16	RW	MCICFGQ_MANUAL_FRTL_VALUE: Note: This value is used only when bit 9 of mci_cfg is a 1. Note: Both the POWER8 Memory Buffer and the host MC must be set up similarly in either auto or manual mode.
17	RW	MCICFGQ_MANUAL_FRTL_DONE: If 1 the manual Frame Round Trip Latency (FRTL) value has been set by software. Note: This bit must be set, when in manual FRTL mode, to complete channel initialization.



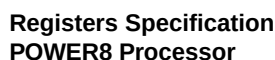
Bits	SCOM	Field Mnemonic: Description
18	RW	MCICFGQ_ECC_CORRECT_DISABLE: If 0 EDI frames, from the replay buffer, will be corrected for ECC Correctable Errors. If 1 EDI frames, from the replay buffer, will not be corrected for ECC Correctable Errors.
19	RW	MCICFGQ_SPARE1: Reserved
20	RW	MCICFGQ_LANE_VOTING_BYPASS: If 0 Bad lane vote is automatically generated by hardware when a cro error is detected. If 1 Force a one shot bad lane vote. Allows firmware to bypass the hardware lane voting algorithm.
21:25	RW	MCICFGQ_BAD_LANE_VALUE: Note: POWER8 Memory Buffer attached chips have 14 downstream lanes and 21 upstream lanes.
26	RW	MCICFGQ_BAD_LANE_VOTING_DISABLE: If 1 the automatic bad lane voting by the hardware algorithm is disabled.
27:32	RW	MCICFGQ_NO_FORWARD_PROGRESS_TIMEOUT_VALUE: Formula: Timeout = 0.109 * DEC(Value) The Timeout term above is in milliseconds. The smallest timeout value is 109 microseconds.
33:34	RW	MCICFGQ_PERFORMANCE_DEGRADATION_PERCENT_SELECT: Value Timeout 00 1% 01 2% 10 3% 11 4%
35:36	RW	MCICFGQ_CHANNEL_INITIALIZATION_STATE_MACHINE_TIMEOUT_VALUE: Value Timeout 00 No Timeout 01 3us 10 7us 11 14us
37	RW	MCICFGQ_RESET_KEEPER: Writing this bit to a 1 will pulse the reset of the hold latches in the MCI c_err_rpt macros
38:41	RW	MCICFGQ_REPLAY_DELAY_VALUE: This is the delay between a replay error event and the start of the replay.
42	RW	MCICFGQ_DEASSERT_MCS_CHANNEL_FAIL: If 1 the MCI_MCS_Channel_Fail is deasserted.
43	RW	MCICFGQ_SPARE3: Reserved
44:63	RO	Constant = 0b000000000000000000000000

Register Name	MCI Status Register (MCISTAT)
Mnemonic	MC0.MCS0.RIGHT.MCISTATQ
Address	00000000201184B (SCOM)
Attributes	
Description	

[illegible]

Register Name		<i>MCI CRC Syndromes Register (MCICRCSYN)</i>
Mnemonic		MC0.MCS0.RIGHT.MCICRCSYNQ
Address		000000000201184C (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0	RWX	MCICRCSYNQ_VALID: If 1 the CRC syndrome is valid.
1	RWX	MCICRCSYNQ_FIRST: If 0, continuously capture the crc syndrome when a crc error occurs. If 1, only capture the crc syndrome for the first crc error.
2	RWX	MCICRCSYNQ_AUTO_RESET_DISABLE: If 0, reset the crc syndrome register when MCICRCSYNQ is read. If 1, do not clear the crc syndrome register when MCICRCSYNQ is read.
3	RWX	MCICRCSYNQ_SPARE0: Reserved
4:35	RWX	MCICRCSYNQ_US_SYNDROME: 32-bit Upstream CRC syndrome logged when a crc error is detected.
36:63	RO	Constant = 0b00000000000000000000000000000000

Register Name		<i>Normal SCOM Mode Reg</i>
Mnemonic		IOMC0.BUSCTL.SCOM.SCOM_MODE_PB
Address		0000000002011A20 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0	RWX	GCR_TEST_MODE: GCR Test Mode. Put register logic into GCR test mode, which allows all RW registers to be read and written by diagnostic code to verify all register accesses. This mode gates off both logic inputs to the registers, as well as the outputs from the logic. The outputs are gated to their scanflush value.
1	RWX	ENABLE_GCR_OFL_BUFF: Enables second GCR overflow buffer, one is used by default.
2:7	RWX	IORESET_HARD_BUS0: I/O Hard Reset Per-Bus and GCR Reset. Enables a hard reset on bus 0-5 (this is application dependent and bus 1-5 might not be present). A GCR reset affects all buses because any of them might be corrupted. 0b000000 = Functional (default) 0b100000 = Reset Bus 0 0b010000 = Reset Bus 1 0b001000 = Reset Bus 2 0b000100 = Reset Bus 3 0b000010 = Reset Bus 4 0b000001 = Reset Bus 5 0b111111 = Reset all local buses and perform a GCR reset.jfg FUNCTIONAL=>0b000000 RESET0=>0b100000 RESET1=>0b010000 RESET2=>0b001000 RESET3=>0b000100 RESET4=>0b000010 RESET5=>0b000001 RESETGCR=>0b111111
8:10	RWX	GCR_HANG_DET_SEL: GCR hang detect threshold Select



Register Name	<i>Pervasive FIR Register</i>
Mnemonic	IOMC0.BUSCTL.SCOM.FIR_REG
Address	0000000002011A00 (SCOM) 0000000002011A01 (SCOM1) 0000000002011A02 (SCOM2)
Attributes	
Description	Local FIR register for the chip pervasive logic

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
24	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_TRAINING_ERROR: FIR Register - An Initialization Training error has occurred on Bus2.
25	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_SPARE_DEPLOYED: FIR Register - A Spare lane has been deployed to repair another lane on Bus2.
26	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_MAX_SPARES_EXCEEDED: FIR Register - The maximum number of spare lanes has been exceeded on Bus2. The bus is no longer capable of transferring data.
27	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_RECAL_OR_DYN_REPAIR_ERROR: FIR Register - A bus recal or dynamic repair error has occurred on Bus2.
28	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_TOO_MANY_BUS_ERRORS: FIR Register - A bus has experienced too many random lane errors on Bus2.
29:31	RWX	WOX_AND	WOX_OR	RESERVED29_31: FIR Register - Reserved.
32	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_TRAINING_ERROR: FIR Register - An Initialization Training error has occurred on Bus3.
33	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_SPARE_DEPLOYED: FIR Register - A Spare lane has been deployed to repair another lane on Bus3.
34	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_MAX_SPARES_EXCEEDED: FIR Register - The maximum number of spare lanes has been exceeded on Bus3. The bus is no longer capable of transferring data.
35	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_RECAL_OR_DYN_REPAIR_ERROR: FIR Register - A bus recal or dynamic repair error has occurred on Bus3.
36	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_TOO_MANY_BUS_ERRORS: FIR Register - A bus has experienced too many random lane errors on Bus3.
37:39	RWX	WOX_AND	WOX_OR	RESERVED37_39: FIR Register - Reserved.
40	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_TRAINING_ERROR: FIR Register - An Initialization Training error has occurred on Bus4.
41	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_SPARE_DEPLOYED: FIR Register - A Spare lane has been deployed to repair another lane on Bus4.
42	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_MAX_SPARES_EXCEEDED: FIR Register - The maximum number of spare lanes has been exceeded on Bus4. The bus is no longer capable of transferring data.
43	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_RECAL_OR_DYN_REPAIR_ERROR: FIR Register - A bus recal or dynamic repair error has occurred on Bus4.
44	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_TOO_MANY_BUS_ERRORS: FIR Register - A bus has experienced too many random lane errors on Bus4.
45:47	RWX	WOX_AND	WOX_OR	RESERVED45_47: FIR Register - Reserved.
48	RWX	WOX_AND	WOX_OR	FIR_SCOMFIR_ERROR: FIR Register- A SCOM FSM or FIR register parity error has occurred.
49	RWX	WOX_AND	WOX_OR	FIR_SCOMFIR_ERROR_CLONE: FIR Register- A SCOM FSM or FIR register parity error has occurred.
50:63	RO	N/A	N/A	Constant = 0b0000000000000000

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Register Name		<i>Pervasive FIR Mask Register</i>		
Mnemonic		IOMC0.BUSCTL.SCOM.FIR_MASK_REG		
Address		0000000002011A03 (SCOM) 0000000002011A04 (SCOM1) 0000000002011A05 (SCOM2)		
Attributes				
Description		Error mask register (Action0,Mask) = Action Select (0,0) = Recoverable Error (0,1) = Masked		
Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_RX_INVALID_STATE_OR_PARITY_ERROR_MASK: FIR Register Mask - Mask RX state machine parity or mode register parity error.
1	RWX	WOX_AND	WOX_OR	FIR_TX_INVALID_STATE_OR_PARITY_ERROR_MASK: FIR Register Mask - Mask TX state machine parity or mode register parity error.
2	RWX	WOX_AND	WOX_OR	FIR_GCR_HANG_ERROR_MASK: FIR Register Mask - Mask GCR ring hang detector error.
3:7	RWX	WOX_AND	WOX_OR	RESERVED3_7_MASK: FIR Register - Reserved.
8	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_TRAINING_ERROR_MASK: FIR Register Mask - Mask Initialization Training error on Bus0.
9	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_SPARE_DEPLOYED_MASK: FIR Register Mask - Mask Spare lane has been deployed indication on Bus0.
10	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_MAX_SPARES_EXCEEDED_MASK: FIR Register Mask - Mask maximum number of spare lanes has been exceeded error on Bus0.
11	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_RECAL_OR_DYN_REPAIR_ERROR_MASK: FIR Register Mask - Mask bus recal or dynamic repair error on Bus0.
12	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_TOO_MANY_BUS_ERRORS_MASK: FIR Register Mask - Mask too many random lane error on Bus0.
13:15	RWX	WOX_AND	WOX_OR	RESERVED13_15_MASK: FIR Register - Reserved.
16	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_TRAINING_ERROR_MASK: FIR Register Mask - Mask Initialization Training error on Bus1.
17	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_SPARE_DEPLOYED_MASK: FIR Register Mask - Mask Spare lane has been deployed indication on Bus1.
18	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_MAX_SPARES_EXCEEDED_MASK: FIR Register Mask - Mask maximum number of spare lanes has been exceeded error on Bus1.
19	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_RECAL_OR_DYN_REPAIR_ERROR_MASK: FIR Register Mask - Mask bus recal or dynamic repair error on Bus1.
20	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_TOO_MANY_BUS_ERRORS_MASK: FIR Register Mask - Mask too many random lane error on Bus1.
21:23	RWX	WOX_AND	WOX_OR	RESERVED21_23_MASK: FIR Register - Reserved.
24	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_TRAINING_ERROR_MASK: FIR Register Mask - Mask Initialization Training error on Bus2.
25	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_SPARE_DEPLOYED_MASK: FIR Register Mask - Mask Spare lane has been deployed indication on Bus2.
26	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_MAX_SPARES_EXCEEDED_MASK: FIR Register Mask - Mask maximum number of spare lanes has been exceeded error on Bus2.
27	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_RECAL_OR_DYN_REPAIR_ERROR_MASK: FIR Register Mask - Mask bus recal or dynamic repair error on Bus2.
28	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_TOO_MANY_BUS_ERRORS_MASK: FIR Register Mask - Mask too many random lane error on Bus2.



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
29:31	RWX	WOX_AND	WOX_OR	RESERVED29_31_MASK: FIR Register - Reserved.
32	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_TRAINING_ERROR_MASK: FIR Register Mask - Mask Initialization Training error on Bus3.
33	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_SPARE_DEPLOYED_MASK: FIR Register Mask - Mask Spare lane has been deployed indication on Bus3.
34	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_MAX_SPARES_EXCEEDED_MASK: FIR Register Mask - Mask maximum number of spare lanes has been exceeded error on Bus3.
35	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_RECAL_OR_DYN_REPAIR_ERROR_MASK: FIR Register Mask - Mask bus recal or dynamic repair error on Bus3.
36	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_TOO_MANY_BUS_ERRORS_MASK: FIR Register Mask - Mask too many random lane error on Bus3.
37:39	RWX	WOX_AND	WOX_OR	RESERVED37_39_MASK: FIR Register - Reserved.
40	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_TRAINING_ERROR_MASK: FIR Register Mask - Mask Initialization Training error on Bus4.
41	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_SPARE_DEPLOYED_MASK: FIR Register Mask - Mask Spare lane has been deployed indication on Bus4.
42	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_MAX_SPARES_EXCEEDED_MASK: FIR Register Mask - Mask maximum number of spare lanes has been exceeded error on Bus4.
43	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_RECAL_OR_DYN_REPAIR_ERROR_MASK: FIR Register Mask - Mask bus recal or dynamic repair error on Bus4.
44	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_TOO_MANY_BUS_ERRORS_MASK: FIR Register Mask - Mask too many random lane error on Bus4.
45:47	RWX	WOX_AND	WOX_OR	RESERVED45_47_MASK: FIR Register - Reserved.
48	RWX	WOX_AND	WOX_OR	INTERNAL_SCOM_ERROR_MASK: Internal SCOM Error Mask
49	RWX	WOX_AND	WOX_OR	INTERNAL_SCOM_ERROR_MASK_CLONE: Internal SCOM Error Mask Clone
50:63	RO	N/A	N/A	Constant = 0b0000000000000000

Register Name	<i>Pervasive FIR Register</i>
Mnemonic	IOMC1.BUSCTL.SCOM.FIR_REG
Address	0000000002011E00 (SCOM) 0000000002011E01 (SCOM1) 0000000002011E02 (SCOM2)
Attributes	
Description	Local FIR register for the chip pervasive logic

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_RX_INVALID_STATE_OR_PARITY_ERROR: FIR Register - A RX state machine parity or mode register parity error has occurred.
1	RWX	WOX_AND	WOX_OR	FIR_TX_INVALID_STATE_OR_PARITY_ERROR: FIR Register - A TX state machine parity or mode register parity error has occurred.
2	RWX	WOX_AND	WOX_OR	FIR_GCR_HANG_ERROR: FIR Register - The per-bus GCR ring hang detector error has occurred.
3:7	RWX	WOX_AND	WOX_OR	RESERVED3_7: FIR Register - Reserved.
8	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_TRAINING_ERROR: FIR Register - An Initialization Training error has occurred on Bus0.

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
9	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_SPARE_DEPLOYED: FIR Register - A Spare lane has been deployed to repair another lane on Bus0.
10	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_MAX_SPARES_EXCEEDED: FIR Register - The maximum number of spare lanes has been exceeded on Bus0. The bus is no longer capable of transferring data.
11	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_RECAL_OR_DYN_REPAIR_ERROR: FIR Register - A bus recal or dynamic repair error has occurred on Bus0.
12	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_TOO_MANY_BUS_ERRORS: FIR Register - A bus has experienced too many random lane errors on Bus0.
13:15	RWX	WOX_AND	WOX_OR	RESERVED13_15: FIR Register - Reserved.
16	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_TRAINING_ERROR: FIR Register - An Initialization Training error has occurred on Bus1.
17	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_SPARE_DEPLOYED: FIR Register - A Spare lane has been deployed to repair another lane on Bus1.
18	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_MAX_SPARES_EXCEEDED: FIR Register - The maximum number of spare lanes has been exceeded on Bus1. The bus is no longer capable of transferring data.
19	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_RECAL_OR_DYN_REPAIR_ERROR: FIR Register - A bus recal or dynamic repair error has occurred on Bus1.
20	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_TOO_MANY_BUS_ERRORS: FIR Register - A bus has experienced too many random lane errors on Bus1.
21:23	RWX	WOX_AND	WOX_OR	RESERVED21_23: FIR Register - Reserved.
24	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_TRAINING_ERROR: FIR Register - An Initialization Training error has occurred on Bus2.
25	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_SPARE_DEPLOYED: FIR Register - A Spare lane has been deployed to repair another lane on Bus2.
26	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_MAX_SPARES_EXCEEDED: FIR Register - The maximum number of spare lanes has been exceeded on Bus2. The bus is no longer capable of transferring data.
27	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_RECAL_OR_DYN_REPAIR_ERROR: FIR Register - A bus recal or dynamic repair error has occurred on Bus2.
28	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_TOO_MANY_BUS_ERRORS: FIR Register - A bus has experienced too many random lane errors on Bus2.
29:31	RWX	WOX_AND	WOX_OR	RESERVED29_31: FIR Register - Reserved.
32	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_TRAINING_ERROR: FIR Register - An Initialization Training error has occurred on Bus3.
33	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_SPARE_DEPLOYED: FIR Register - A Spare lane has been deployed to repair another lane on Bus3.
34	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_MAX_SPARES_EXCEEDED: FIR Register - The maximum number of spare lanes has been exceeded on Bus3. The bus is no longer capable of transferring data.
35	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_RECAL_OR_DYN_REPAIR_ERROR: FIR Register - A bus recal or dynamic repair error has occurred on Bus3.
36	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_TOO_MANY_BUS_ERRORS: FIR Register - A bus has experienced too many random lane errors on Bus3.
37:39	RWX	WOX_AND	WOX_OR	RESERVED37_39: FIR Register - Reserved.
40	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_TRAINING_ERROR: FIR Register - An Initialization Training error has occurred on Bus4.



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
41	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_SPARE_DEPLOYED: FIR Register - A Spare lane has been deployed to repair another lane on Bus4.
42	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_MAX_SPARES_EXCEEDED: FIR Register - The maximum number of spare lanes has been exceeded on Bus4. The bus is no longer capable of transferring data.
43	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_RECAL_OR_DYN_REPAIR_ERROR: FIR Register - A bus recal or dynamic repair error has occurred on Bus4.
44	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_TOO_MANY_BUS_ERRORS: FIR Register - A bus has experienced too many random lane errors on Bus4.
45:47	RWX	WOX_AND	WOX_OR	RESERVED45_47: FIR Register - Reserved.
48	RWX	WOX_AND	WOX_OR	FIR_SCOMFIR_ERROR: FIR Register- A SCOM FSM or FIR register parity error has occurred.
49	RWX	WOX_AND	WOX_OR	FIR_SCOMFIR_ERROR_CLONE: FIR Register- A SCOM FSM or FIR register parity error has occurred.
50:63	RO	N/A	N/A	Constant = 0b0000000000000000

Register Name	MCI Fault Isolation Register (MCIFIR)
Mnemonic	MC2.MCS0.RIGHT.MCIFIRQ
Address	0000000002011C40 (SCOM) 0000000002011C41 (SCOM1) 0000000002011C42 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	MCIFIRQ_REPLAY_TIMEOUT: If 0 EDI channel is operational. If 1 Too many EDI replays due to CRC error. There's no forward progress.
1	RWX	WOX_AND	WOX_OR	MCIFIRQ_CHANNEL_FAIL: NOTE: Look at the EDI FIR for details. NOTE: This bit must be reset in the EDI phy.
2	RWX	WOX_AND	WOX_OR	MCIFIRQ_CRC_ERROR: If 0 No CRC errors detected. If 1 A CRC error is detected by receiver.
3	RWX	WOX_AND	WOX_OR	MCIFIRQ_FRAME_NOACK: If 0 All transmitted frames have been acknowledged If 1 A transmitted frame did not get a Positive Acknowledge.
4	RWX	WOX_AND	WOX_OR	MCIFIRQ_SEQID_OUT_OF_ORDER: If 0 All received frames ID are in sequential order during non-replay transfer. If 1 Received frames ID are not in sequential order during non-replay transfer.
5	RWX	WOX_AND	WOX_OR	MCIFIRQ_REPLAY_BUFFER_ECC_CE: If 0 No ECC Correctable Error detected. If 1 An ECC Correctable Error was detected in the replay buffer.
6	RWX	WOX_AND	WOX_OR	MCIFIRQ_REPLAY_BUFFER_ECC_UE: If 0 No ECC UnCorrectable Error detected. If 1 An ECC UnCorrectable Error was detected in the replay buffer.
7	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCI_CHINIT_STATE_MACHINE_TIMEOUT: If 1 An internal MCI state machine did not get a response within a programmable time interval.
8	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCI_INTERNAL_CONTROL_PARITY_ERROR: If 1 An internal MCI state machine parity error was detected.
9	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCI_DATA_FLOW_PARITY_ERROR: If '1', a parity error was detected on the downstream data flow.

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
10	RWX	WOX_AND	WOX_OR	MCIFIRQ_CRC_PERFORMANCE_DEGRADATION: If '1' the EDI bus performance has degraded by 1% of the channel bandwidth.
11	RWX	WOX_AND	WOX_OR	MCIFIRQ_CHANNEL_INTERLOCK_FAIL: If '1', an error condition was detected during the channel interlock window
12	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_CHECKSTOP: If '1', an active POWER8 Memory Buffer checkstop bit was detected in an upstream attention packet
13	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_TRACESTOP: If '1', an active POWER8 Memory Buffer tracestop bit was detected in an upstream attention packet
14	RWX	WOX_AND	WOX_OR	MCIFIRQ_FPGA_INTERRUPT: If '1' an active FPGA interrupt bit was detected in an upstream attention packet
15	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_RECOVERABLE_ERROR: If '1', an active POWER8 Memory Buffer recoverable error bit was detected in an upstream attention packet
16	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_SPECIAL_ATTENTION: If '1', an active POWER8 Memory Buffer special attention bit was detected in an upstream attention packet
17	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_MAINTENANCE_COMPLETE: If '1', an active POWER8 Memory Buffer maintenance complete bit was detected in an upstream attention packet
18	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_INBAND_PIB_ERROR: If '1', an active POWER8 Memory Buffer inband PIB error bit was detected in an upstream attention packet
19	RWX	WOX_AND	WOX_OR	MCIFIRQ_FRTL_COUNTER_OVERFLOW: If '1' the FRTL counter has overflowed or wrapped around
20	RWX	WOX_AND	WOX_OR	MCIFIRQ_SCOM_WR_PERR: If '1', a SCOM register parity error has been detected. This error does not include parity errors on mcicfgq.
21	RWX	WOX_AND	WOX_OR	MCIFIRQ_MULTIPLE_REPLAY: A replay event was detected while the transmitter was in replay.
22	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCICFG_WR_PERR: If '1', a parity error has been detected on mcicfgq.
23	RWX	WOX_AND	WOX_OR	MCIFIRQ_REPLAY_BUFFER_OVERRUN: If '1', a new frame taken when all replay buffers are in use.
24	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_RECOVERABLE_ERROR: If '1', a MCS recoverable error was detected. See the MCERPT0 register description for a list of errors that cause this FIR to be set.
25	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_INTERNAL_NONRECOVERABLE_ERROR: If '1', an internal MCS nonrecoverable error was detected. See the MCERPT0 register description for a list of errors that cause this FIR to be set.
26	RWX	WOX_AND	WOX_OR	MCIFIRQ_POWERBUS_PROTOCOL_ERROR: If '1', a processor bus protocol error was detected. (for example, a HPC_WR is snooped when a HPC_WR to the same address is active).
27	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_COMMAND_LIST_TIMEOUT: If '1', a command list state machine has timed out.
28	RWX	WOX_AND	WOX_OR	MCIFIRQ_MULTIPLE_RCMD_OR_CRESP_ACTIVE: If '1', a cresp command is active on cresp bus0 and bus1 in the same cycle, or a valid non-inband command is active on rcmd0 and a valid non-inband command is active on rcmd1 in the same cycle. Note the rcmd validity for this check does not include alternate, foreign hole, or HA BAR checking. Note that cresp portion of this checker is enabled only if MCFGPM(0) or MCFGPM(0) is set.



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
29	RWX	WOX_AND	WOX_OR	MCIFIRQ_INBAND_BAR_HIT_WITH_INCORRECT_TTYPE: If '1', a command was issued to inband address space using a ttype the MCS responds to, but other than ttypes: (8-byte CI_PR_W, 8-byte CI_PR_RD, CL_RD_NC, CHGRATE, RPTHANG, or LINK_CHK)
30	RWX	WOX_AND	WOX_OR	MCIFIRQ_MULTIPLE_BAR_HIT: If '1', an address match on more than one Memory BAR was detected
31	RWX	WOX_AND	WOX_OR	MCIFIRQ_CHANNEL_FAIL_SIGNAL_ACTIVE: If '1', the MCS logic is in the channel fail state
32	RWX	WOX_AND	WOX_OR	MCIFIRQ_MIRROR_ACTION_OCCURRED: If '1', a channel fail or read SUE was detected on a primary mirror read access, causing a secondary mirror request. This FIR is set when secondary mirror commands with types of 000 (ns_rd), 001 (ns_rd_sfu), or 111 (ns_rmw_f)
33	RWX	WOX_AND	WOX_OR	MCIFIRQ_INVALID_FOREIGN_BAR_ACCESS: If '1', an invalid foreign BAR access has occurred.
34	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_SYNC_COMMAND_DETECTED: If '1', a POWER8 Memory Buffer Sync Command was detected in the MCS car1 cycle, because of a processor bus 8-byte ci_pr_w sync command.
35	RWX	WOX_AND	WOX_OR	MCIFIRQ_POWERBUS_WRITE_DATA_BUFFER_CE: If '1', a CE was detected on a read of the processor bus write data buffer.
36	RWX	WOX_AND	WOX_OR	MCIFIRQ_POWERBUS_WRITE_DATA_BUFFER_UE: If '1', a UE was detected on a read of the processor bus write data buffer.
37	RWX	WOX_AND	WOX_OR	MCIFIRQ_POWERBUS_WRITE_DATA_BUFFER_SUE: If '1', a SUE was detected on a read of the processor bus write data buffer.
38	RWX	WOX_AND	WOX_OR	MCIFIRQ_HA_ILLEGAL_CONSUMER_ACCESS_ERROR: If '1', a HA Illegal Consumer Access Error was detected.
39	RWX	WOX_AND	WOX_OR	MCIFIRQ_HA_ILLEGAL_PRODUCER_ACCESS_ERROR: If '1', a HA Illegal Producer Access Error was detected.
40	RWX	WOX_AND	WOX_OR	MCIFIRQ_CHANNEL_TIMEOUT_ERROR: If '1', a Channel Timeout Error was detected. If MCMODE0(37) is set to force a channel fail if a channel timeout error is detected, this FIR should be set to recoverable. If MCMODE0(37) is not set, so a channel timeout does not force a channel fail, this FIR should be set to non-recoverable. If a channel fail occurs, the conditions causing this FIR bit to be set are blocked.
41	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_FAULT_LINE: If '1', the POWER8 Memory Buffer fault line input has gone active (low)
42	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_WAT: If '1', a MCS WAT event has occurred, and has been programmed to set this FIR
43	RWX	WOX_AND	WOX_OR	MCIFIRQ_INVALID_ADDRESS: If '1', the MCS has received an address in the high half of MCFGPMCFGPM, that is not defined by MCFGPAMCFGPMA
44	RWX	WOX_AND	WOX_OR	MCIFIRQ_COMMAND_LIST_TIMEOUT_RCMD_TO_CRESP_WRITE_DATA_AVAILABLE: If '1', a MCS command list has timed out between the dispatch (due to fastpath or rcmd) and combined response for a read operation, or between dispatch and combined response and write data arrival for a write operation.
45	RWX	WOX_AND	WOX_OR	MCIFIRQ_MPIPL_OR_FLR_WRITE_SUE: If '1', a SCOM MPIPL cleanup or Foreign Link Recovery (FLR) operation has caused a SUE to be written to memory. MCMODE4(24) controls the setting of this FIR. This FIR is set once for each cache line written to memory with a SUE.

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
46	RWX	WOX_AND	WOX_OR	MCIFIRQ_INVALID_CENTAUR_BYPASS: If '1', the POWER8 Memory Buffer returns an op marked as bypass that is unexpected by the MCS (command not bypassable). The upstream bypass bit evaluated for this check is crc qualified.
47	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_WRITE_DATAFLOW_SUE: If '1', a SUE error was detected in the MCS write dataflow, due to a write buffer UE or SUE, or a MPIPL or foreign link recovery write operation.
48	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_EXTRA_FIR_0: If '1', Extra_FIR_0 was detected in the MCS.
49	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_EXTRA_FIR_1: If '1', Extra_FIR_1 was detected in the MCS.
50	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_EXTRA_FIR_2: If '1', Extra_FIR_2 was detected in the MCS.
51	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_EXTRA_FIR_3: If '1', Extra_FIR_3 was detected in the MCS.
52	RWX	WOX_AND	WOX_OR	MCIFIRQ_INTERNAL_SCOM_ERROR: Internal SCOM Error
53	RWX	WOX_AND	WOX_OR	MCIFIRQ_INTERNAL_SCOM_ERROR_CLONE: Internal SCOM Error Clone
54:63	RO	N/A	N/A	Constant = 0b0000000000

Register Name	<i>MC Fault Isolation Register (MCIFIR)</i>
Mnemonic	MC2.MCS1.RIGHT.MCIFIRQ
Address	0000000002011CC0 (SCOM) 0000000002011CC1 (SCOM1) 0000000002011CC2 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	MCIFIRQ_REPLAY_TIMEOUT: If 0 EDI channel is operational. If 1 Too many EDI replays due to CRC error. There's no forward progress.
1	RWX	WOX_AND	WOX_OR	MCIFIRQ_CHANNEL_FAIL: NOTE: Look at the EDI FIR for details. NOTE: This bit must be reset in the EDI phy.
2	RWX	WOX_AND	WOX_OR	MCIFIRQ_CRC_ERROR: If 0 No CRC errors detected. If 1 A CRC error is detected by receiver.
3	RWX	WOX_AND	WOX_OR	MCIFIRQ_FRAME_NOACK: If 0 All transmitted frames have been acknowledged If 1 A transmitted frame did not get a Positive Acknowledge.
4	RWX	WOX_AND	WOX_OR	MCIFIRQ_SEQID_OUT_OF_ORDER: If 0 All received frames ID are in sequential order during non-replay transfer. If 1 Received frames ID are not in sequential order during non-replay transfer.
5	RWX	WOX_AND	WOX_OR	MCIFIRQ_REPLAY_BUFFER_ECC_CE: If 0 No ECC Correctable Error detected. If 1 An ECC Correctable Error was detected in the replay buffer.
6	RWX	WOX_AND	WOX_OR	MCIFIRQ_REPLAY_BUFFER_ECC_UE: If 0 No ECC UnCorrectable Error detected. If 1 An ECC UnCorrectable Error was detected in the replay buffer.
7	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCI_CHINIT_STATE_MACHINE_TIMEOUT: If 1 An internal MCI state machine did not get a response within a programmable time interval.



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
8	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCI_INTERNAL_CONTROL_PARITY_ERROR: If '1' An internal MCI state machine parity error was detected.
9	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCI_DATA_FLOW_PARITY_ERROR: If '1', a parity error was detected on the downstream data flow.
10	RWX	WOX_AND	WOX_OR	MCIFIRQ_CRC_PERFORMANCE_DEGRADATION: If '1' the EDI bus performance has degraded by 1% of the channel bandwidth.
11	RWX	WOX_AND	WOX_OR	MCIFIRQ_CHANNEL_INTERLOCK_FAIL: If '1', an error condition was detected during the channel interlock window
12	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_CHECKSTOP: If '1', an active POWER8 Memory Buffer checkstop bit was detected in an upstream attention packet
13	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_TRACESTOP: If '1', an active POWER8 Memory Buffer tracestop bit was detected in an upstream attention packet
14	RWX	WOX_AND	WOX_OR	MCIFIRQ_FPGA_INTERRUPT: If '1' an active FPGA interrupt bit was detected in an upstream attention packet
15	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_RECOVERABLE_ERROR: If '1', an active POWER8 Memory Buffer recoverable error bit was detected in an upstream attention packet
16	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_SPECIAL_ATTENTION: If '1', an active POWER8 Memory Buffer special attention bit was detected in an upstream attention packet
17	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_MAINTENANCE_COMPLETE: If '1', an active POWER8 Memory Buffer maintenance complete bit was detected in an upstream attention packet
18	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_INBAND_PIB_ERROR: If '1', an active POWER8 Memory Buffer inband PIB error bit was detected in an upstream attention packet
19	RWX	WOX_AND	WOX_OR	MCIFIRQ_FRTL_COUNTER_OVERFLOW: If '1' the FRTL counter has overflowed or wrapped around
20	RWX	WOX_AND	WOX_OR	MCIFIRQ_SCOM_WR_PERR: If '1', a SCOM register parity error has been detected. This error does not include parity errors on mcicfgq.
21	RWX	WOX_AND	WOX_OR	MCIFIRQ_MULTIPLE_REPLAY: A replay event was detected while the transmitter was in replay.
22	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCICFG_WR_PERR: If '1', a parity error has been detected on mcicfgq.
23	RWX	WOX_AND	WOX_OR	MCIFIRQ_REPLAY_BUFFER_OVERRUN: If '1', a new frame taken when all replay buffers are in use.
24	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_RECOVERABLE_ERROR: If '1', a MCS recoverable error was detected. See the MCERPT0 register description for a list of errors that cause this FIR to be set.
25	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_INTERNAL_NONRECOVERABLE_ERROR: If '1', an internal MCS nonrecoverable error was detected. See the MCERPT0 register description for a list of errors that cause this FIR to be set.
26	RWX	WOX_AND	WOX_OR	MCIFIRQ_POWERBUS_PROTOCOL_ERROR: If '1', a processor bus protocol error was detected. (for example, a HPC_WR is snooped when a HPC_WR to the same address is active).
27	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_COMMAND_LIST_TIMEOUT: If '1', a command list state machine has timed out.

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
28	RWX	WOX_AND	WOX_OR	MCIFIRQ_MULTIPLE_RCMD_OR_CRESP_ACTIVE: If '1', a cresp command is active on cresp bus0 and bus1 in the same cycle, or a valid non-inband command is active on rcmd0 and a valid non-inband command is active on rcmd1 in the same cycle. Note the rcmd validity for this check does not include alternate, foreign hole, or HA BAR checking. Note that cresp portion of this checker is enabled only if MCFGPM(0) is set.
29	RWX	WOX_AND	WOX_OR	MCIFIRQ_INBAND_BAR_HIT_WITH_INCORRECT_TTYPE: If '1', a command was issued to inband address space using a ttype the MCS responds to, but other than ttypes: (8-byte CI_PR_W, 8-byte CI_PR_RD, CL_RD_NC, CHGRATE, RPTHANG, or LINK_CHK)
30	RWX	WOX_AND	WOX_OR	MCIFIRQ_MULTIPLE_BAR_HIT: If '1', an address match on more than one Memory BAR was detected
31	RWX	WOX_AND	WOX_OR	MCIFIRQ_CHANNEL_FAIL_SIGNAL_ACTIVE: If '1', the MCS logic is in the channel fail state
32	RWX	WOX_AND	WOX_OR	MCIFIRQ_MIRROR_ACTION_OCCURRED: If '1', a channel fail or read SUE was detected on a primary mirror read access, causing a secondary mirror request. This FIR is set when secondary mirror commands with types of 000 (ns_rd), 001 (ns_rd_sfu), or 111 (ns_rmw_f)
33	RWX	WOX_AND	WOX_OR	MCIFIRQ_INVALID_FOREIGN_BAR_ACCESS: If '1', an invalid foreign BAR access has occurred.
34	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_SYNC_COMMAND_DETECTED: If '1', a POWER8 Memory Buffer Sync Command was detected in the MCS car1 cycle, because of a processor bus 8-byte ci_pr_w sync command.
35	RWX	WOX_AND	WOX_OR	MCIFIRQ_POWERBUS_WRITE_DATA_BUFFER_CE: If '1', a CE was detected on a read of the processor bus write data buffer.
36	RWX	WOX_AND	WOX_OR	MCIFIRQ_POWERBUS_WRITE_DATA_BUFFER_UE: If '1', a UE was detected on a read of the processor bus write data buffer.
37	RWX	WOX_AND	WOX_OR	MCIFIRQ_POWERBUS_WRITE_DATA_BUFFER_SUE: If '1', a SUE was detected on a read of the processor bus write data buffer.
38	RWX	WOX_AND	WOX_OR	MCIFIRQ_HA_ILLEGAL_CONSUMER_ACCESS_ERROR: If '1', a HA Illegal Consumer Access Error was detected.
39	RWX	WOX_AND	WOX_OR	MCIFIRQ_HA_ILLEGAL_PRODUCER_ACCESS_ERROR: If '1', a HA Illegal Producer Access Error was detected.
40	RWX	WOX_AND	WOX_OR	MCIFIRQ_CHANNEL_TIMEOUT_ERROR: If '1', a Channel Timeout Error was detected. If MCMODE0(37) is set to force a channel fail if a channel timeout error is detected, this FIR should be set to recoverable. If MCMODE0(37) is not set, so a channel timeout does not force a channel fail, this FIR should be set to non-recoverable. If a channel fail occurs, the conditions causing this FIR bit to be set are blocked.
41	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_FAULT_LINE: If '1', the POWER8 Memory Buffer fault line input has gone active (low)
42	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_WAT: If '1', a MCS WAT event has occurred, an has been programmed to set this FIR
43	RWX	WOX_AND	WOX_OR	MCIFIRQ_INVALID_ADDRESS: If '1', the MCS has received an address in the high half of MCFGPMCFGPM, that is not defined by MCFGPAMCFGPMA
44	RWX	WOX_AND	WOX_OR	MCIFIRQ_COMMAND_LIST_TIMEOUT_RCMD_TO_CRESP_WRITE_DATA_AVAILABLE: If '1', a MCS command list has timed out between the dispatch (due to fastpath or rcmd) and combined response for a read operation, or between dispatch and combined response and write data arrival for a write operation.



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
45	RWX	WOX_AND	WOX_OR	MCIFIRQ_MPIPL_OR_FLR_WRITE_SUE: If '1', a SCOM MPIPL cleanup or Foreign Link Recovery (FLR) operation has caused a SUE to be written to memory. MCMODE4(24) controls the setting of this FIR. This FIR is set once for each cache line written to memory with a SUE.
46	RWX	WOX_AND	WOX_OR	MCIFIRQ_INVALID_CENTAUR_BYPASS: If '1', the POWER8 Memory Buffer returns an op marked as bypass that is unexpected by the MCS (command not bypassable). The upstream bypass bit evaluated for this check is crc qualified.
47	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_WRITE_DATAFLOW_SUE: If '1', a SUE error was detected in the MCS write dataflow, due to a write buffer UE or SUE, or a MPIPL or foreign link recovery write operation.
48	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_EXTRA_FIR_0: If '1', Extra_FIR_0 was detected in the MCS.
49	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_EXTRA_FIR_1: If '1', Extra_FIR_1 was detected in the MCS.
50	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_EXTRA_FIR_2: If '1', Extra_FIR_2 was detected in the MCS.
51	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_EXTRA_FIR_3: If '1', Extra_FIR_3 was detected in the MCS.
52	RWX	WOX_AND	WOX_OR	MCIFIRQ_INTERNAL_SCOM_ERROR: Internal SCOM Error
53	RWX	WOX_AND	WOX_OR	MCIFIRQ_INTERNAL_SCOM_ERROR_CLONE: Internal SCOM Error Clone
54:63	RO	N/A	N/A	Constant = 0b0000000000

Register Name	MCI Fault Isolation Register (MCIFIR)
Mnemonic	MC3.MCS0.RIGHT.MCIFIRQ
Address	0000000002011D40 (SCOM) 0000000002011D41 (SCOM1) 0000000002011D42 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	MCIFIRQ_REPLAY_TIMEOUT: If 0 EDI channel is operational. If 1 Too many EDI replays due to CRC error. There's no forward progress.
1	RWX	WOX_AND	WOX_OR	MCIFIRQ_CHANNEL_FAIL: NOTE: Look at the EDI FIR for details. NOTE: This bit must be reset in the EDI phy.
2	RWX	WOX_AND	WOX_OR	MCIFIRQ_CRC_ERROR: If 0 No CRC errors detected. If 1 A CRC error is detected by receiver.
3	RWX	WOX_AND	WOX_OR	MCIFIRQ_FRAME_NOACK: If 0 All transmitted frames have been acknowledged If 1 A transmitted frame did not get a Positive Acknowledge.
4	RWX	WOX_AND	WOX_OR	MCIFIRQ_SEQID_OUT_OF_ORDER: If 0 All received frames ID are in sequential order during non-replay transfer. If 1 Received frames ID are not in sequential order during non-replay transfer.
5	RWX	WOX_AND	WOX_OR	MCIFIRQ_REPLAY_BUFFER_ECC_CE: If 0 No ECC Correctable Error detected. If 1 An ECC Correctable Error was detected in the replay buffer.

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
6	RWX	WOX_AND	WOX_OR	MCIFIRQ_REPLAY_BUFFER_ECC_UE: If 0 No ECC UnCorrectable Error detected. If 1 An ECC UnCorrectable Error was detected in the replay buffer.
7	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCI_CHINIT_STATE_MACHINE_TIMEOUT: If 1 An internal MCI state machine did not get a response within a programmable time interval.
8	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCI_INTERNAL_CONTROL_PARITY_ERROR: If 1 An internal MCI state machine parity error was detected.
9	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCI_DATA_FLOW_PARITY_ERROR: If '1', a parity error was detected on the downstream data flow.
10	RWX	WOX_AND	WOX_OR	MCIFIRQ_CRC_PERFORMANCE_DEGRADATION: If '1' the EDI bus performance has degraded by 1% of the channel bandwidth.
11	RWX	WOX_AND	WOX_OR	MCIFIRQ_CHANNEL_INTERLOCK_FAIL: If '1', an error condition was detected during the channel interlock window
12	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_CHECKSTOP: If '1', an active POWER8 Memory Buffer checkstop bit was detected in an upstream attention packet
13	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_TRACESTOP: If '1', an active POWER8 Memory Buffer tracestop bit was detected in an upstream attention packet
14	RWX	WOX_AND	WOX_OR	MCIFIRQ_FPGA_INTERRUPT: If '1' an active FPGA interrupt bit was detected in an upstream attention packet
15	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_RECOVERABLE_ERROR: If '1', an active POWER8 Memory Buffer recoverable error bit was detected in an upstream attention packet
16	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_SPECIAL_ATTENTION: If '1', an active POWER8 Memory Buffer special attention bit was detected in an upstream attention packet
17	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_MAINTENANCE_COMPLETE: If '1' an active Centaur maintenance complete bit was detected in an upstream attention packet
18	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_INBAND_PIB_ERROR: If '1', an active POWER8 Memory Buffer inband PIB error bit was detected in an upstream attention packet
19	RWX	WOX_AND	WOX_OR	MCIFIRQ_FRTL_COUNTER_OVERFLOW: If '1' the FRTL counter has overflowed or wrapped around
20	RWX	WOX_AND	WOX_OR	MCIFIRQ_SCOM_WR_PERR: If '1', a SCOM register parity error has been detected. This error does not include parity errors on mcicfgq.
21	RWX	WOX_AND	WOX_OR	MCIFIRQ_MULTIPLE_REPLAY: A replay event was detected while the transmitter was in replay.
22	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCICFG_WR_PERR: If '1', a parity error has been detected on mcicfgq.
23	RWX	WOX_AND	WOX_OR	MCIFIRQ_REPLAY_BUFFER_OVERRUN: If '1', a new frame taken when all replay buffers are in use.
24	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_RECOVERABLE_ERROR: If '1', a MCS recoverable error was detected. See the MCERPT0 register description for a list of errors that cause this FIR to be set.
25	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_INTERNAL_NONRECOVERABLE_ERROR: If '1', an internal MCS nonrecoverable error was detected. See the MCERPT0 register description for a list of errors that cause this FIR to be set.



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
26	RWX	WOX_AND	WOX_OR	MCIFIRQ_POWERBUS_PROTOCOL_ERROR: If '1', a processor bus protocol error was detected. (for example, a HPC_WR is snooped when a HPC_WR to the same address is active).
27	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_COMMAND_LIST_TIMEOUT: If '1', a command list state machine has timed out.
28	RWX	WOX_AND	WOX_OR	MCIFIRQ_MULTIPLE_RCMD_OR_CRESP_ACTIVE: If '1', a cresp command is active on cresp bus0 and bus1 in the same cycle, or a valid non-inband command is active on rcmd0 and a valid non-inband command is active on rcmd1 in the same cycle. Note the rcmd validity for this check does not include alternate, foreign hole, or HA BAR checking. Note that cresp portion of this checker is enabled only if MCFGPM(0) or MCFGPM(0) is set.
29	RWX	WOX_AND	WOX_OR	MCIFIRQ_INBAND_BAR_HIT_WITH_INCORRECT_TTYPE: If '1', a command was issued to inband address space using a ttype the MCS responds to, but other than ttypes: (8-byte CI_PR_W, 8-byte CI_PR_RD, CL_RD_NC, CHGRATE, RPTHANG, or LINK_CHK).
30	RWX	WOX_AND	WOX_OR	MCIFIRQ_MULTIPLE_BAR_HIT: If '1', an address match on more than one Memory BAR was detected
31	RWX	WOX_AND	WOX_OR	MCIFIRQ_CHANNEL_FAIL_SIGNAL_ACTIVE: If '1', the MCS logic is in the channel fail state
32	RWX	WOX_AND	WOX_OR	MCIFIRQ_MIRROR_ACTION_OCCURRED: If '1', a channel fail or read SUE was detected on a primary mirror read access, causing a secondary mirror request. This FIR is set when secondary mirror commands with types of 000 (ns_rd), 001 (ns_rd_sfu), or 111 (ns_rmw_f)
33	RWX	WOX_AND	WOX_OR	MCIFIRQ_INVALID_FOREIGN_BAR_ACCESS: If '1', an invalid foreign BAR access has occurred.
34	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_SYNC_COMMAND_DETECTED: If '1', a POWER8 Memory Buffer Sync Command was detected in the MCS car1 cycle, because of a processor bus 8-byte ci_pr_w sync command.
35	RWX	WOX_AND	WOX_OR	MCIFIRQ_POWERBUS_WRITE_DATA_BUFFER_CE: If '1', a CE was detected on a read of the processor bus write data buffer.
36	RWX	WOX_AND	WOX_OR	MCIFIRQ_POWERBUS_WRITE_DATA_BUFFER_UE: If '1', a UE was detected on a read of the processor bus write data buffer.
37	RWX	WOX_AND	WOX_OR	MCIFIRQ_POWERBUS_WRITE_DATA_BUFFER_SUE: If '1', a SUE was detected on a read of the processor bus write data buffer.
38	RWX	WOX_AND	WOX_OR	MCIFIRQ_HA_ILLEGAL_CONSUMER_ACCESS_ERROR: If '1', a HA Illegal Consumer Access Error was detected.
39	RWX	WOX_AND	WOX_OR	MCIFIRQ_HA_ILLEGAL_PRODUCER_ACCESS_ERROR: If '1', a HA Illegal Producer Access Error was detected.
40	RWX	WOX_AND	WOX_OR	MCIFIRQ_CHANNEL_TIMEOUT__ERROR: If '1', a Channel Timeout Error was detected. If MCMODE0(37) is set to force a channel fail if a channel timeout error is detected, this FIR should be set to recoverable. If MCMODE0(37) is not set, so a channel timeout does not force a channel fail, this FIR should be set to non-recoverable. If a channel fail occurs, the conditions causing this FIR bit to be set are blocked.
41	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_FAULT_LINE: If '1', the POWER8 Memory Buffer fault line input has gone active (low)
42	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_WAT: If '1', a MCS WAT event has occurred, an has been programmed to set this FIR

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
43	RWX	WOX_AND	WOX_OR	MCIFIRQ_INVALID_ADDRESS: If '1', the MCS has received an address in the high half of MCFGPMCFGPM, that is not defined by MCFGPAMCFGPMA
44	RWX	WOX_AND	WOX_OR	MCIFIRQ_COMMAND_LIST_TIMEOUT_RCMD_TO_CRESP_WRITE_DATA_AVAILABLE: If '1', a MCS command list has timed out between the dispatch (due to fastpath or rcmd) and combined response for a read operation, or between dispatch and combined response and write data arrival for a write operation.
45	RWX	WOX_AND	WOX_OR	MCIFIRQ_MPIPL_OR_FLR_WRITE_SUE: If '1', a SCOM MPIPL cleanup or Foreign Link Recovery (FLR) operation has caused a SUE to be written to memory. MCMODE4(24) controls the setting of this FIR. This FIR is set once for each cache line written to memory with a SUE.
46	RWX	WOX_AND	WOX_OR	MCIFIRQ_INVALID_CENTAUR_BYPASS: If '1', the POWER8 Memory Buffer returns an operation marked as bypass that is unexpected by the MCS (command not bypassable). The upstream bypass bit evaluated for this check is crc qualified.
47	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_WRITE_DATAFLOW_SUE: If '1', a SUE error was detected in the MCS write dataflow, due to a write buffer UE or SUE, or a MPIPL or foreign link recovery write operation.
48	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_EXTRA_FIR_0: If '1', Extra_FIR_0 was detected in the MCS.
49	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_EXTRA_FIR_1: If '1', Extra_FIR_1 was detected in the MCS.
50	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_EXTRA_FIR_2: If '1', Extra_FIR_2 was detected in the MCS.
51	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_EXTRA_FIR_3: If '1', Extra_FIR_3 was detected in the MCS.
52	RWX	WOX_AND	WOX_OR	MCIFIRQ_INTERNAL_SCOM_ERROR: Internal SCOM Error
53	RWX	WOX_AND	WOX_OR	MCIFIRQ_INTERNAL_SCOM_ERROR_CLONE: Internal SCOM Error Clone
54:63	RO	N/A	N/A	Constant = 0b0000000000

Register Name	MCI Fault Isolation Register (MCIFIR)
Mnemonic	MC3.MCS1.RIGHT.MCIFIRQ
Address	0000000002011DC0 (SCOM) 0000000002011DC1 (SCOM1) 0000000002011DC2 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	MCIFIRQ_REPLAY_TIMEOUT: If 0 EDI channel is operational. If 1 Too many EDI replays due to CRC error. There's no forward progress.
1	RWX	WOX_AND	WOX_OR	MCIFIRQ_CHANNEL_FAIL: NOTE: Look at the EDI FIR for details. NOTE: This bit must be reset in the EDI phy.
2	RWX	WOX_AND	WOX_OR	MCIFIRQ_CRC_ERROR: If 0 No CRC errors detected. If 1 A CRC error is detected by receiver.
3	RWX	WOX_AND	WOX_OR	MCIFIRQ_FRAME_NOACK: If 0 All transmitted frames have been acknowledged If 1 A transmitted frame did not get a Positive Acknowledge.



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
4	RWX	WOX_AND	WOX_OR	MCIFIRQ_SEQID_OUT_OF_ORDER: If 0 All received frames ID are in sequential order during non-replay transfer. If 1 Received frames ID are not in sequential order during non-replay transfer.
5	RWX	WOX_AND	WOX_OR	MCIFIRQ_REPLAY_BUFFER_ECC_CE: If 0 No ECC Correctable Error detected. If 1 An ECC Correctable Error was detected in the replay buffer.
6	RWX	WOX_AND	WOX_OR	MCIFIRQ_REPLAY_BUFFER_ECC_UE: If 0 No ECC UnCorrectable Error detected. If 1 An ECC UnCorrectable Error was detected in the replay buffer.
7	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCI_CHINIT_STATE_MACHINE_TIMEOUT: If 1 An internal MCI state machine did not get a response within a programmable time interval.
8	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCI_INTERNAL_CONTROL_PARITY_ERROR: If 1 An internal MCI state machine parity error was detected.
9	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCI_DATA_FLOW_PARITY_ERROR: If '1', a parity error was detected on the downstream data flow.
10	RWX	WOX_AND	WOX_OR	MCIFIRQ_CRC_PERFORMANCE_DEGRADATION: If '1' the EDI bus performance has degraded by 1% of the channel bandwidth.
11	RWX	WOX_AND	WOX_OR	MCIFIRQ_CHANNEL_INTERLOCK_FAIL: If '1', an error condition was detected during the channel interlock window
12	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_CHECKSTOP: If '1', an active POWER8 Memory Buffer checkstop bit was detected in an upstream attention packet
13	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_TRACESTOP: If '1', an active POWER8 Memory Buffer tracestop bit was detected in an upstream attention packet
14	RWX	WOX_AND	WOX_OR	MCIFIRQ_FPGA_INTERRUPT: If '1' an active FPGA interrupt bit was detected in an upstream attention packet
15	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_RECOVERABLE_ERROR: If '1', an active POWER8 Memory Buffer recoverable error bit was detected in an upstream attention packet
16	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_SPECIAL_ATTENTION: If '1', an active POWER8 Memory Buffer special attention bit was detected in an upstream attention packet
17	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_MAINTENANCE_COMPLETE: If '1', an active POWER8 Memory Buffer maintenance complete bit was detected in an upstream attention packet
18	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_INBAND_PIB_ERROR: If '1', an active POWER8 Memory Buffer inband PIB error bit was detected in an upstream attention packet
19	RWX	WOX_AND	WOX_OR	MCIFIRQ_FRTL_COUNTER_OVERFLOW: If '1' the FRTL counter has overflowed or wrapped around
20	RWX	WOX_AND	WOX_OR	MCIFIRQ_SCOM_WR_PERR: If '1', a SCOM register parity error has been detected. This error does not include parity errors on mcicfgq.
21	RWX	WOX_AND	WOX_OR	MCIFIRQ_MULTIPLE_REPLAY: A replay event was detected while the transmitter was in replay.
22	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCICFG_WR_PERR: If '1', a parity error has been detected on mcicfgq.
23	RWX	WOX_AND	WOX_OR	MCIFIRQ_REPLAY_BUFFER_OVERRUN: If '1', a new frame taken when all replay buffers are in use.

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
24	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_RECOVERABLE_ERROR: If '1', a MCS recoverable error was detected. See the MCERPT0 register description for a list of errors that cause this FIR to be set.
25	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_INTERNAL_NONRECOVERABLE_ERROR: If '1', an internal MCS nonrecoverable error was detected. See the MCERPT0 register description for a list of errors that cause this FIR to be set.
26	RWX	WOX_AND	WOX_OR	MCIFIRQ_POWERBUS_PROTOCOL_ERROR: If '1', a processor bus protocol error was detected. (for example, a HPC_WR is snooped when a HPC_WR to the same address is active).
27	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_COMMAND_LIST_TIMEOUT: If '1', a command list state machine has timed out.
28	RWX	WOX_AND	WOX_OR	MCIFIRQ_MULTIPLE_RCMD_OR_CRESP_ACTIVE: If '1', a cresp command is active on cresp bus0 and bus1 in the same cycle, or a valid non-inband command is active on rcmd0 and a valid non-inband command is active on rcmd1 in the same cycle. Note the rcmd validity for this check does not include alternate, foreign hole, or HA BAR checking. Note that cresp portion of this checker is enabled only if MCFGPM(0) or MCFGPM(0) is set.
29	RWX	WOX_AND	WOX_OR	MCIFIRQ_INBAND_BAR_HIT_WITH_INCORRECT_TTYPE: If '1', a command was issued to inband address space using a ttype the MCS responds to, but other than ttypes: (8-byte CI_PR_W, 8-byte CI_PR_RD, CL_RD_NC, CHGRATE, RPTHANG, or LINK_CHK)
30	RWX	WOX_AND	WOX_OR	MCIFIRQ_MULTIPLE_BAR_HIT: If '1', an address match on more than one Memory BAR was detected
31	RWX	WOX_AND	WOX_OR	MCIFIRQ_CHANNEL_FAIL_SIGNAL_ACTIVE: If '1', the MCS logic is in the channel fail state
32	RWX	WOX_AND	WOX_OR	MCIFIRQ_MIRROR_ACTION_OCCURRED: If '1', a channel fail or read SUE was detected on a primary mirror read access, causing a secondary mirror request. This FIR is set when secondary mirror commands with types of 000 (ns_rd), 001 (ns_rd_sfu), or 111 (ns_rmw_f)
33	RWX	WOX_AND	WOX_OR	MCIFIRQ_INVALID_FOREIGN_BAR_ACCESS: If '1', an invalid foreign BAR access has occurred.
34	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_SYNC_COMMAND_DETECTED: If '1', a POWER8 Memory Buffer Sync Command was detected in the MCS car1 cycle, because of a processor bus 8-byte ci_pr_w sync command.
35	RWX	WOX_AND	WOX_OR	MCIFIRQ_POWERBUS_WRITE_DATA_BUFFER_CE: If '1', a CE was detected on a read of the processor bus write data buffer.
36	RWX	WOX_AND	WOX_OR	MCIFIRQ_POWERBUS_WRITE_DATA_BUFFER_UE: If '1', a UE was detected on a read of the processor bus write data buffer.
37	RWX	WOX_AND	WOX_OR	MCIFIRQ_POWERBUS_WRITE_DATA_BUFFER_SUE: If '1', a SUE was detected on a read of the processor bus write data buffer.
38	RWX	WOX_AND	WOX_OR	MCIFIRQ_HA_ILLEGAL_CONSUMER_ACCESS_ERROR: If '1', a HA Illegal Consumer Access Error was detected.
39	RWX	WOX_AND	WOX_OR	MCIFIRQ_HA_ILLEGAL_PRODUCER_ACCESS_ERROR: If '1', a HA Illegal Producer Access Error was detected.
40	RWX	WOX_AND	WOX_OR	MCIFIRQ_CHANNEL_TIMEOUT_ERROR: If '1', a Channel Timeout Error was detected. If MCMODE0(37) is set to force a channel fail if a channel timeout error is detected, this FIR should be set to recoverable. If MCMODE0(37) is not set, so a channel timeout does not force a channel fail, this FIR should be set to non-recoverable. If a channel fail occurs, the conditions causing this FIR bit to be set are blocked.



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
41	RWX	WOX_AND	WOX_OR	MCIFIRQ_CENTAUR_FAULT_LINE: If '1', the POWER8 Memory Buffer fault line input has gone active (low).
42	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_WAT: If '1', a MCS WAT event has occurred and has been programmed to set this FIR.
43	RWX	WOX_AND	WOX_OR	MCIFIRQ_INVALID_ADDRESS: If '1', the MCS has received an address in the high half of MCFGPMCFGPM, that is not defined by MCFGPAMCFGPMA.
44	RWX	WOX_AND	WOX_OR	MCIFIRQ_COMMAND_LIST_TIMEOUT_RCMD_TO_CRESP_WRITE_DATA_AVAILABLE: If '1', a MCS command list has timed out between the dispatch (due to fastpath or rcmd) and combined response for a read operation, or between dispatch and combined response and write data arrival for a write operation..
45	RWX	WOX_AND	WOX_OR	MCIFIRQ_MPIPL_OR_FLR_WRITE_SUE: If '1', a SCOM MPIPL cleanup or Foreign Link Recovery (FLR) operation has caused a SUE to be written to memory. MCMODE4(24) controls the setting of this FIR. This FIR is set once for each cache line written to memory with a SUE.
46	RWX	WOX_AND	WOX_OR	MCIFIRQ_INVALID_CENTAUR_BYPASS: If '1', the POWER8 Memory Buffer returns an operation marked as bypass that is unexpected by the MCS (command not bypassable). The upstream bypass bit evaluated for this check is crc qualified.
47	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_WRITE_DATAFLOW_SUE: If '1', a SUE error was detected in the MCS write dataflow, due to a write buffer UE or SUE, or a MPIPL or foreign link recovery write operation.
48	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_EXTRA_FIR_0: If '1', Extra_FIR_0 was detected in the MCS.
49	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_EXTRA_FIR_1: If '1', Extra_FIR_1 was detected in the MCS.
50	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_EXTRA_FIR_2: If '1', Extra_FIR_2 was detected in the MCS.
51	RWX	WOX_AND	WOX_OR	MCIFIRQ_MCS_EXTRA_FIR_3: If '1', Extra_FIR_3 was detected in the MCS.
52	RWX	WOX_AND	WOX_OR	MCIFIRQ_INTERNAL_SCOM_ERROR: Internal SCOM Error
53	RWX	WOX_AND	WOX_OR	MCIFIRQ_INTERNAL_SCOM_ERROR_CLONE: Internal SCOM Error Clone
54:63	RO	N/A	N/A	Constant = 0b0000000000

Register Name	<i>Alter/Display Control Register</i>
Mnemonic	EN.TPC.AD.ALTD_CONTROL_REG
Address	0000000002020000 (PCB)
Attributes	
Description	

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Bits	PCB	Field Mnemonic: Description
0:5	RW	FBC_ALTD_TTYPE: The TTYPE used in the Alter/Display command Official Supported values: CI Partial Write DMA Partial Write CI Partial Read DMA Partial Read PB Operation (axtype) CI_PARTIAL_WRITE=>0b110111 CI_PARTIAL_OOO_WRITE=>0b110110 DMA_PARTIAL_WRITE=>0b100110 CI_PARTIAL_READ=>0b110100 DMA_PARTIAL_READ=>0b110101 PBOPERATION=>0b111111
6	RW	FBC_ALTD_RNW: The Read or Write control for the Alter/Display command Read = 1; must match TTYPE operation Write = 0; must match TTYPE operation READ=>0b1 WRITE=>0b0
7:13	RW	FBC_ALTD_TSIZE: The Tsize used in the Alter/Display command Supported values: 1, 2, 4 and 8 bytes
14:63	RWX	FBC_ALTD_ADDRESS: The Address bits 14:63 to use with the Alter/Display command

Register Name	<i>Alter/Display Command Register</i>
Mnemonic	EN.TPC.AD.ALTD_CMD_REG
Address	0000000002020001 (PCB)
Attributes	Secure=true
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RO	Constant = 0b00
2	NCX	FBC_ALTD_START_OP: Start the Alter/Display PCB Operation (latch resets after arbitration passed)
3	NCX	FBC_ALTD_CLEAR_STATUS: Clear the Alter/Display Status Register
4	NCX	FBC_ALTD_RESET_AD_PCB: Reset the Alter/Display State Machine and Status Registers
5	RO	Constant = 0b0
6	RWX	FBC_ALTD_AXTYPE: Address Only type command no data transfer will be done
7	RW	FBC_ALTD_DATA_ONLY: Skip the cmd-cresp part and only send a data packet with FBC_altd_address(0:13) as ttag. The Address bits 57:59 are send to the HT-Data ramp, too
8:9	RW	FBC_ALTD_DROP_PRIORITY_MAX: Maximal value the Command drop priority can increase to (if not already bigger) LOW=>0b00 MEDIUM=>0b01 HIGH=>0b10 RESERVED=>0b11

Bits	PCB	Field Mnemonic: Description
10	NCX	Reserved field. (Access type is FBC_lock_pick) LOW=>0b00 MEDIUM=>0b01 HIGH=>0b10 RESERVED=>0b11
11	RWX	FBC_LOCKED: set when the locked the ALTD_CMD_REG, ALTD_CONTROL_REG and ALTD_DATA_REG
12:15	ROX	FBC_LOCK_ID: Reading current lock owner (only valid when locked). Writing current owner when overwrite the lock
16:18	RWX	FBC_ALTD_SCOPE: The broadcast scope of the command NODAL=>0b000 GROUP=>0b001 SYSTEM=>0b010 REMOTE=>0b011 FOREIGN0=>0b100 FOREIGN1=>0b101 FOREIGN2=>0b110 FOREIGN3=>0b111
19	RW	FBC_ALTD_AUTO_INC: The Alter/Display will Auto Increment the address and issue the next command Auto Increment = 1; Address will increment by 8 and next command will be issued after current command is completed Regular = 0; Alter/Display will issue one command and stop AUTO_INC=>0b1 REGULAR=>0b0
20:21	RWX	FBC_ALTD_DROP_PRIORITY: Initial command drop priority: specifying which commands are dropped due to PB congestion first LOW=>0b00 MEDIUM=>0b01 HIGH=>0b10 RESERVED=>0b11
22	RO	Constant = 0b0 LOW=>0b00 MEDIUM=>0b01 HIGH=>0b10 RESERVED=>0b11
23	RW	FBC_ALTD_OVERWRITE_PBINIT: start this command even when pbinit is low
24	RWX	FBC_ALTD_WITH_PIB_DIRECT: copy ALTD_CONTROL_REG to OCA_PIB_DIRECT_CMD and ALTD_DATA_REG to OCA_PIB_DIRECT_DATA register inst
25	RWX	FBC_ALTD_WITH_PBINIT_LOW_WAIT: Wait for the pbinit signal to be dropped before continuing
26	RWX	FBC_ALTD_WITH_TM QUIESCE: Set and wait for the local token manager quiesce before the processor bus quiesce or altd command
27	RWX	FBC_ALTD_WITH_PRE QUIESCE: Sent out a processor bus quiesce command before executing the altd command
28:47	RWX	FBC_ALTD_AFTER QUIESCE_WAIT_COUNT: time to wait between quiesce and altd command
48:49	RO	Constant = 0b00
50:59	RWX	FBC_ALTD_BEFORE_INIT_WAIT_COUNT: time to wait between altd command and init

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Bits	PCB	Field Mnemonic: Description
60:62	RO	Constant = 0b000
63	RWX	FBC_ALTD_WITH_POST_INIT: Sent out a processor bus init command after executing the command

Register Name	<i>Alter/Display Status Register</i>
Mnemonic	EN.TPC.AD.ALTD_STATUS_REG
Address	0000000002020002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is FBC_altd_busy)
1	ROX	FBC_ALTD_WAIT_CMD_ARBIT: Waiting for arbiter to send the command out
2	ROX	FBC_ALTD_ADDR_DONE: The Address portion of the Alter/Display PCB Operation is complete
3	ROX	FBC_ALTD_DATA_DONE: The Data portion of the Alter/Display PCB Operation is complete
4	ROX	FBC_ALTD_WAIT_RESP: Waiting on a Clean Combined Resp to the Alter/Display PCB operation
5	RWX_WCLRR EG	FBC_ALTD_OVERRUN_ERROR: Overrun Error indicates new data was written before the previous data was used or a read was performed without new data arrived
6	RWX_WCLRR EG	FBC_ALTD_AUTOINC_ERROR: AutoInc Error indicates internal address counter rolled over the 0.5M boundary
7	RWX_WCLRR EG	FBC_ALTD_COMMAND_ERROR: Command Error indicates new command was issued before the previous one finished
8	RWX_WCLRR EG	FBC_ALTD_ADDRESS_ERROR: Invalid Address Error: PB respond with Address Error cresp
9	RWX_WCLRR EG	FBC_ALTD_PB_OP_HANG_ERR: PB Timeout while waiting for cresp
10	RWX_WCLRR EG	FBC_ALTD_PB_DATA_HANG_ERR: PB Timeout while waiting for data
11	RWX_WCLRR EG	FBC_ALTD_PB_UNEXPECT_CRESP_ERR: Combined response from PB received at a time it is not expected by FSM
12	RWX_WCLRR EG	FBC_ALTD_PB_UNEXPECT_DATA_ERR: Data from PB received at a time it is not expected by FSM
13:15	RO	Constant = 0b000
16	ROX	FBC_ALTD_WAIT_PIB_DIRECT: waiting on xscom state machine to complete direct oca (write) command
17	ROX	FBC_ALTD_PIB_DIRECT_DONE: completed a direct to pib (write) command
18	ROX	FBC_ALTD_PBINIT_MISSING: attempt to start a command without pb_init active detected, which was blocked, except when using overwrite bit
19	ROX	FBC_ALTD_UNTRUSTED_DENIED: attempt to start a untrusted command from untrusted pib master
20:31	RO	Constant = 0b000000000000
32	RWX_WCLRR EG	FBC_ALTD_PCB_ERROR_FIR: PCB Endpoint FIR indicates some error has occurred in the Alter/Display PCB endpoint
33:39	ROX	FBC_ALTD_PCB_ERROR: PCB Endpoint Error indicates what kind of PCB endpoint error
40:47	RO	Constant = 0b00000000



Bits	PCB	Field Mnemonic: Description
48	RWX_WCLRR EG	FBC_ALTD_ECC_CE: correctable ecc error detected and corrected during FBC_altd transaction (read)
49	RWX_WCLRR EG	FBC_ALTD_ECC_UE: uncorrectable ecc error detected during FBC_altd transaction (read)
50	RWX_WCLRR EG	FBC_ALTD_ECC_SUE: special uncorrectable ecc error detected during FBC_altd transaction (read)
51:58	RO	Constant = 0b00000000
59:63	ROX	FBC_ALTD_CRESP_VALUE: The cresp value

Register Name	<i>Alter/Display Data Register</i>
Mnemonic	EN.TPC.AD.ALTD_DATA_REG
Address	0000000002020003 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:63	RWX	FBC_ALTD_DATA: The Data to use with the Alter/Display command

Register Name	<i>Alter/Display XSCOM Base Address Register</i>
Mnemonic	EN.TPC.AD.ALTD_XSCOM_BASE_REG
Address	0000000002020005 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:13	RO	Constant = 0b0000000000000000
14:22	RW	FBC_ALTD_XSCOM_BASE: Base Address for XSCOM logic in Alter/Display
23:27	RO	Constant = 0b000000
28	WOX	FBC_ALTD_XSCOM_RESET: Used to reset the XSCOM State Machine logic in Alter/Display
29	RW	FBC_ALTD_XSCOM_DISABLE: Used to disable the XSCOM State Machine logic in Alter/Display
30	RW	FBC_ALTD_XSCOM_DISABLE_LOCAL_SHORTCUT: Used to disable the shortcut for local ADU internal registers
31:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>Force ECC Register</i>
Mnemonic	EN.TPC.AD.FORCE_ECC_REG
Address	0000000002020010 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	PCB_DATA_ITAG: 64th Bit the itag of a pcb operation

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Bits	PCB	Field Mnemonic: Description
1:16	RWX	PCB_DATA_TX_ECC: The two ECC values of a pcb/xscom/tbrom -> pb data transfer
17	RWX	PCB_DATA_TX_ECC_OVERWRITE: Override(=suppress update of) ECC value of a pcb -> pb operation data transfer. Be careful! There MUST BE NO xscom neither tbrom -> pb data transfer. In Example a XSCOM read will modify the ECC value

Register Name	<i>pMisc Receive Malfunction Alert Register</i>
Mnemonic	EN.TPC.AD.RCV_ERRLOG_REG
Address	0000000002020011 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW_WAND	MALF_ERR_FROM_NODE0: There was a malf error from node 0 (one bit for each chip)
8:15	RW_WAND	MALF_ERR_FROM_NODE1: There was a malf error from node 1 (one bit for each chip)
16:23	RW_WAND	MALF_ERR_FROM_NODE2: There was a malf error from node 2 (one bit for each chip)
24:31	RW_WAND	MALF_ERR_FROM_NODE3: There was a malf error from node 3 (one bit for each chip)
32:39	RW_WAND	MALF_ERR_FROM_NODE4: There was a malf error from node 4 (one bit for each chip)
40:47	RW_WAND	MALF_ERR_FROM_NODE5: There was a malf error from node 5 (one bit for each chip)
48:55	RW_WAND	MALF_ERR_FROM_NODE6: There was a malf error from node 6 (one bit for each chip)
56:63	RW_WAND	MALF_ERR_FROM_NODE7: There was a malf error from node 7 (one bit for each chip)

Register Name	<i>pMisc Mode Register</i>
Mnemonic	EN.TPC.AD.SND_MODE_REG
Address	000000000202000B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	ENABLE_TRC_GLB_TRIG0: Enable broadcast of Trace Global Trigger 0
1	RW	ENABLE_TRC_GLB_TRIG1: Enable broadcast of Trace Global Trigger 1
2	RW	ENABLE_GLB_PULSE_MODE: On rising edge, send a Trace Global Trigger toggle cmd.
3	RW	SINGLE_OUTSTANDING_CMD: Wait for the clean cresp on every command before the next can be posted. This can cause big delays if a command gets retried for a long time. DO NOT use TOGETHER with ENABLE_RECEIVE_OWN_TOD to prevent DEADLOCK. This is because the receive part depends on xscom-result-pmisc going out, before xcsn accepts the next TOD command. The deadlock would be tod retrying forever and xscom fsm can not finish sending the result pmisc.
4:7	RW	PROG_REQ_DELAY: Program amount of delay between Fabric address requests Matches 4 MSB of 12 bit counter, allows delay from 0 cycles to 3840 cycles in steps of 256 cycles. Defaulted to no delay (0000) in design.
8	RW	DISABLE_ERR_CMD: Block error commands from being broadcast (malf rising edge only).
9	RW	DISABLE_HTM_CMD: Block htm commands from being broadcast
10	RW	DISABLE_TRACE_CMD: Block trace commands from being broadcast



Bits	PCB	Field Mnemonic: Description
11	RW	DISABLE_TOD_CMD: Block freqchng commands from being broadcast
12	RW	DISABLE_XSCOM_CMD: Block XSCOM commands from being broadcast
13	RW	ENABLE_CLR_ERR_CMD: Enable sending of err reset when a malf goes away EXPERIMENTAL - DO NOT USE (sequence ordering can not be guaranteed)
14	RW	OVERRIDE_PBINIT_ERR_CMD: Allow error commands to being broadcast on quiesced PB
15	RW	OVERRIDE_PBINIT_HTM_CMD: Allow htm commands to being broadcast on quiesced PB
16	RW	OVERRIDE_PBINIT_TRACE_CMD: Allow trace commands to being broadcast on quiesced PB
17	RW	OVERRIDE_PBINIT_TOD_CMD: Allow freqchng commands to being broadcast on quiesced PB
18	RW	OVERRIDE_PBINIT_XSCOM_CMD: Allow XSCOM commands to being broadcast on quiesced PB
19	RW	DISABLE_CHECKSTOP: Disable forwarding checkstop to stop processor bus
20	WOX	MANUAL_SET_PB_STOP: Manual set and overwrite state of stop the processor bus signal (requires disabling forwarding first)
21	WOX	MANUAL_CLR_PB_STOP: Manual clr and overwrite state of stop the processor bus signal (requires disabling forwarding first).
22	ROX	PB_STOP: State of the processor bus pb_stop signal.
23:24	RO	Constant = 0b00
25	WOX	MANUAL_PB_SWITCH_ABCD: Force a local (not broadcast) processor bus AB or CD Register switch.
26:27	RW	ENABLE_RECEIVE_OWN_TRIGGER: Enables receiving debug trigger pmisc from same adu (with same nodeid, chipid).
28	RW	ENABLE_RECEIVE_OWN_TOD: Enables receiving tod pmisc from same adu (with same nodeid, chipid) DO NOT use TOGETHER with SINGLE_OUTSTANDING_CMD to prevent DEADLOCK.
29	WOX	RESET_TOD_STATE: Reset state machine of incomplete tod pmisc receive.
30	RW	ENABLE_PB_SWITCH_AB: Enable generation of a Processor Bus AB Register Switch event pulse.
31	RW	ENABLE_PB_SWITCH_CD: Enable generation of a Processor Bus CD Register Switch event pulse.

Register Name	<i>The Untrusted Memory Base Address Which Fsi Can Access</i>
Mnemonic	EN.TPC.AD.ALTD_UNTRUSTED_BAR_ADDR_REG
Address	0000000002020015 (PCB)
Attributes	Secure=true, Magic=true
Description	

Bits	PCB	Field Mnemonic: Description
0:13	RO	Constant = 0b0000000000000000
14:43	RWX	ALTD_UNTRUSTED_BAR: address bits used for compare when corresponding mask bit is 1, else this bit must be 0 otherwise fsi access is disabled
44:63	RO	Constant = 0b00000000000000000000

Register Name	<i>Untrusted Memory Base Address That FSI Can Access</i>
Mnemonic	EN.TPC.AD.ALTD_UNTRUSTED_BAR_MASK_ADDR_REG
Address	0000000002020016 (PCB)
Attributes	Secure=true, Magic=true
Description	

[illegible]

Register Name	PCI Nest FIR Register
Mnemonic	ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.FIR_REG
Address	0000000002012000 (SCOM) 0000000002012001 (SCOM1) 0000000002012002 (SCOM2)
Attributes	
Description	PCI Nest FIR Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	BAR_PE: One of the BARS or BAR Masks register parity error
1	RWX	WOX_AND	WOX_OR	NONBAR_PE: Any non-Bar register parity error
2	RWX	WOX_AND	WOX_OR	PB_TO_PEC_CE: ECC Correctable error off of outbound processor bus
3	RWX	WOX_AND	WOX_OR	PB_TO_PEC_UE: ECC Uncorrectable error off of outbound processor bus
4	RWX	WOX_AND	WOX_OR	PB_TO_PEC_SUE: ECC Special Uncorrectable error off of outbound processor bus
5	RWX	WOX_AND	WOX_OR	ARY_ECC_CE: ECC Correctable error on an internal array
6	RWX	WOX_AND	WOX_OR	ARY_ECC_UE: ECC Uncorrectable error on an internal array
7	RWX	WOX_AND	WOX_OR	ARY_ECC_SUE: ECC Special Uncorrectable error on an internal array
8	RWX	WOX_AND	WOX_OR	REGISTER_ARRAY_PE: Parity error on an internal register file
9	RWX	WOX_AND	WOX_OR	PB_INTERFACE_PE: Parity Error on PB interface(Address/ATag/RTAG/RTAG)
10	RWX	WOX_AND	WOX_OR	PB_DATA_HANG_ERRORS: Any processor bus data hang poll error. (Only checked for CI stores.)
11	RWX	WOX_AND	WOX_OR	PB_HANG_ERRORS: Any processor bus command hang error (in the domestic address range)
12	RWX	WOX_AND	WOX_OR	RD_ARE_ERRORS: Processor bus ARE detected by DMA read or Atomic engines
13	RWX	WOX_AND	WOX_OR	NONRD_ARE_ERRORS: Processor bus ARE detected by DMA write or Interrupt engines
14	RWX	WOX_AND	WOX_OR	PCI_HANG_ERROR: PBCQ detected that PCI load, store, EOI or dma read response did not make forward progress
15	RWX	WOX_AND	WOX_OR	PCI_CLOCK_ERROR: PBCQ has detected that the PCI clock has stopped
16	RWX	WOX_AND	WOX_OR	AIB_FENCE: The PHB had a severe error and has fenced the AIB
17	RWX	WOX_AND	WOX_OR	HW_ERRORS: Any misc hardware error
18	RWX	WOX_AND	WOX_OR	UNSOLICITEDPBDATA: PEC received data with an RTAG matching a Queue that was not expecting data, or too much data was received.
19	RWX	WOX_AND	WOX_OR	UNEXPECTEDCRESP: PEC received an unexpected Combined Response
20	RWX	WOX_AND	WOX_OR	INVALIDCRESP: PEC received an Invalid Combined Response
21	RWX	WOX_AND	WOX_OR	PBUNSUPPORTEDSIZE: PEC Receive a CI Command that matches one of our Bars but is an unsupported size or address alignment CI Loads Size != 1,2,4,8,16,32 with address naturally aligned CI Store Size != 1,2,4,16,32,64,128 with address naturally aligned

Registers Specification

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
22	RWX	WOX_AND	WOX_OR	PBUNSUPPORTEDCMD: PEC Receive a CI Command that matches one of our Bars but is an unsupported Ttype. Supported Ttypes are ci_pr_rd, ci_pr_ooo_w, ci_pr_w, ris.
23	RWX	WOX_AND	WOX_OR	AIB_PE: The internal AIB had a control or credit parity error.
24	RWX	WOX_AND	WOX_OR	ASB_ERROR: The internal SCOM to ASB bridge has an error
25	RWX	WOX_AND	WOX_OR	FOREIGN_LINK_FAIL: A command received ack_dead or link_chk.abort_op indicating the foreign link is down
26	RWX	WOX_AND	WOX_OR	FOREIGN_PB_HANG: Any processor bus command hang error (in the foreign address range)
27	RWX	WOX_AND	WOX_OR	CAPP_ERROR: Error from CAPP Unit for Freezing PHB
28	RWX	WOX_AND	WOX_OR	SYNC_SCOM_ERR: Error bit from SCOM engines, Nest domain
29	RWX	WOX_AND	WOX_OR	Reserved field. (Access type is local_err0)
30	RWX	WOX_AND	WOX_OR	Reserved field. (Access type is local_err1)
31:63	RO	N/A	N/A	Constant = 0b00000000000000000000000000000000

Register Name	PCI Nest FIR Mask Register
Mnemonic	ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.FIR_MASK_REG
Address	0000000002012003 (SCOM) 0000000002012004 (SCOM1) 0000000002012005 (SCOM2)
Attributes	
Description	PCI Nest FIR Mask Register 0 = No Mask 1 = Mask Error

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	BAR_PE_MASK: One of the BARS or BAR Masks register parity error
1	RW	WO_AND	WO_OR	NONBAR_PE_MASK: Any Non Bar register parity error
2	RW	WO_AND	WO_OR	PB_TO_PEC_CE_MASK: ECC Correctable error off of outbound processor bus
3	RW	WO_AND	WO_OR	PB_TO_PEC_UE_MASK: ECC Uncorrectable error off of outbound processor bus
4	RW	WO_AND	WO_OR	PB_TO_PEC_SUE_MASK: ECC Special Uncorrectable error off of outbound processor bus
5	RW	WO_AND	WO_OR	ARY_ECC_CE_MASK: ECC Correctable error on an internal array
6	RW	WO_AND	WO_OR	ARY_ECC_UE_MASK: ECC Uncorrectable error on an internal array
7	RW	WO_AND	WO_OR	ARY_ECC_SUE_MASK: ECC Special Uncorrectable error on an internal array
8	RW	WO_AND	WO_OR	REGISTER_ARRAY_PE_MASK: Parity error on an internal register file
9	RW	WO_AND	WO_OR	PB_INTERFACE_PE_MASK: Parity Error on PB interface(Address/ATag/TTag/RTAG)
10	RW	WO_AND	WO_OR	PB_DATA_HANG_ERRORS_MASK: Any processor bus data hang poll error(Only checked for CI Stores)
11	RW	WO_AND	WO_OR	PB_HANG_ERRORS_MASK: Any processor bus command hang error



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
12	RW	WO_AND	WO_OR	RD_ARE_ERRORS_MASK: Processor Bus ARE detected by DMA read or Atomic engines
13	RW	WO_AND	WO_OR	NONRD_ARE_ERRORS_MASK: Processor Bus ARE detected by DMA write or Interrupt engines
14	RW	WO_AND	WO_OR	PCI_HANG_ERROR_MASK: PBCQ detected that PCI load, store, EOI or dma read response did not make forward progress
15	RW	WO_AND	WO_OR	PCI_CLOCK_ERROR_MASK: PBCQ has detected that the PCI clock has stopped
16	RW	WO_AND	WO_OR	AIB_FENCE_MASK: The PHB had a severe error and has fenced the AIB
17	RW	WO_AND	WO_OR	HW_ERRORS_MASK: Any misc hardware error
18	RW	WO_AND	WO_OR	UNSOLICITEDPBDATA_MASK: PEC received data with an RTAG matching a Queue that was not expecting data, or too much data was received.
19	RW	WO_AND	WO_OR	UNEXPECTEDCRESP_MASK: PEC received an unexpected Combined Response
20	RW	WO_AND	WO_OR	INVALIDCRESP_MASK: PEC received an Invalid Combined Response
21	RW	WO_AND	WO_OR	PBUNSUPPORTEDSIZE_MASK: PEC Receive a CI Command that matches one of our Bars but is an unsupported size or address alignment CI Loads Size != 1,2,4,8,16,32 with address naturally aligned CI Store Size != 1,2,4,16,32,64,128 with address naturally aligned
22	RW	WO_AND	WO_OR	PBUNSUPPORTEDCMD_MASK: PEC Receive a CI Command that matches one of our Bars but is an unsupported Ttype. Supported Ttypes are ci_pr_rd, ci_pr_ooo_w, ci_pr_w, ris.
23	RW	WO_AND	WO_OR	AIB_PE_MASK: The internal AIB had a control or credit parity error.
24	RW	WO_AND	WO_OR	ASB_ERROR_MASK: The internal SCOM to ASB bridge has an error
25	RW	WO_AND	WO_OR	FOREIGN_LINK_FAIL_MASK: A command received ack_dead or data hang from the foreign interface
26	RW	WO_AND	WO_OR	FOREIGN_PB_HANG_MASK: Any processor bus command hang error (in the foreign address range)
27	RW	WO_AND	WO_OR	CAPP_ERROR_MASK: Error from CAPP Unit for Freezing PHB
28	RW	WO_AND	WO_OR	SYNC_SCOM_ERR_MASK: Error bit from SCOM engines, Nest domain
29	RW	WO_AND	WO_OR	Reserved field. (Access type is local_err0)
30	RW	WO_AND	WO_OR	Reserved field. (Access type is local_err1)
31:63	RO	N/A	N/A	Constant = 0b00000000000000000000000000000000

Register Name	PCI Nest FIR Action0 Register
Mnemonic	ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.FIR_ACTION0_REG
Address	0000000002012006 (SCOM)
Attributes	
Description	PCI Nest FIR Action0 Register

Registers Specification

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Bits	SCOM	Field Mnemonic: Description
0:30	RW	FIR_ACTION0: Action0 select for corresponding bit in FIR (Action0,Mask) = Action Select (0,0) = Checkstop Error (0,1) = Recoverable Error (1,0) = No Action (1,1) = Freeze
31:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>PCI Nest FIR Action1 Register</i>
Mnemonic	ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.FIR_ACTION1_REG
Address	0000000002012007 (SCOM)
Attributes	
Description	PCI Nest FIR Action1 Register

Bits	SCOM	Field Mnemonic: Description
0:30	RW	FIR_ACTION1: Action1 select for corresponding bit in FIR (Action1,Mask) = Action Select (0,0) = Checkstop Error (0,1) = Recoverable Error (1,0) = No Action (1,1) = Freeze
31:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>Pci Nest Fir Wof Register</i>
Mnemonic	ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.FIR_WOF_REG
Address	0000000002012008 (SCOM)
Attributes	
Description	pci nest fir wof register

Bits	SCOM	Field Mnemonic: Description
0:30	RWX_WCLRR EG	
31:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>Nodal Base Address/Mask Register 0</i>
Mnemonic	ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.PEPBREGS.NODALBAR0_REG
Address	0000000002012010 (SCOM)
Attributes	
Description	Nodal Base Address/Mask Register 0

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_BUS_NODAL_BAR0_EN: PE bus Nodal Base Address Register 0 Enable Each BAR/Mask set has 1 enable bit



Bits	SCOM	Field Mnemonic: Description
1:14	RW	PE_BUS_NODAL_MASK0: pe bus Nodal Base Address Register Mask 0 This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 4GB up to 64TB. 64_TB=>0b11111111111111 32_TB=>0b01111111111111 16_TB=>0b00111111111111 8_TB=>0b00011111111111 4_TB=>0b00001111111111 2_TB=>0b00000111111111 1_TB=>0b00000011111111 512_GB=>0b00000001111111 256_GB=>0b00000000111111 128_GB=>0b00000000011111 64_GB=>0b00000000001111 32_GB=>0b00000000000011 16_GB=>0b00000000000001 8_GB=>0b000000000000001 4_GB=>0b000000000000000
15:32	RW	PE_BUS_NODAL_BAR0: pe bus Nodal Base Address Register 0 Bits 14 to 31 of the Nodal Base Address 0 range are specified with this IDial. Bits 14 to 31 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 31 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Nodal address range specified by the BAR/Mask pair.
33:63	RO	Constant = 0b00000000000000000000000000000000

Register Name		Nodal Base Address/Mask Register 1
Mnemonic		ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.PEPBREGS.NODALBAR1_REG
Address		0000000002012011 (SCOM)
Attributes		
Description		Nodal Base Address/Mask Register 1
Bits	SCOM	Field Mnemonic: Description
0	RW	PE_BUS_NODAL_BAR1_EN: PE bus Nodal Base Address Register 1 Enable Each BAR/Mask set has 1 enable bit

Registers Specification

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Bits	SCOM	Field Mnemonic: Description
1:14	RW	PE_BUS_NODAL_MASK1: pe bus Nodal Base Address Register Mask 1 This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 4GB up to 64TB. 64_TB=>0b1111111111111111 32_TB=>0b0111111111111111 16_TB=>0b0011111111111111 8_TB=>0b0001111111111111 4_TB=>0b0000111111111111 2_TB=>0b0000011111111111 1_TB=>0b0000001111111111 512_GB=>0b0000000111111111 256_GB=>0b0000000011111111 128_GB=>0b0000000001111111 64_GB=>0b0000000000111111 32_GB=>0b0000000000001111 16_GB=>0b0000000000000111 8_GB=>0b0000000000000011 4_GB=>0b0000000000000001
15:32	RW	PE_BUS_NODAL_BAR1: pe bus Nodal Base Address Register 1 Bits 14 to 31 of the Nodal Base Address 1 range are specified with this IDial. Bits 14 to 31 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 31 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Nodal address range specified by the BAR/Mask pair.
33:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Group Base Address/Mask Register 0	
Mnemonic	ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.PEPBREGS.GROUPBAR0_REG	
Address	0000000002012012 (SCOM)	
Attributes		
Description	Group Base Address/Mask Register 0	

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_BUS_GROUP_BAR0_EN: PE bus Group Base Address Register 0 Enable Each BAR/Mask set has 1 enable bit



Bits	SCOM	Field Mnemonic: Description
1:14	RW	PE_BUS_GROUP_MASK0: pe bus Group Base Address Register Mask 0 This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 4GB up to 64TB. 64_TB=>0b11111111111111 32_TB=>0b01111111111111 16_TB=>0b00111111111111 8_TB=>0b00011111111111 4_TB=>0b00001111111111 2_TB=>0b00000111111111 1_TB=>0b00000011111111 512_GB=>0b00000001111111 256_GB=>0b00000000111111 128_GB=>0b00000000011111 64_GB=>0b00000000001111 32_GB=>0b00000000000111 16_GB=>0b00000000000011 8_GB=>0b00000000000001 4_GB=>0b00000000000000
15:32	RW	PE_BUS_GROUP_BAR0: pe bus Group Base Address Register 0 Bits 14 to 31 of the Group Base Address 0 range are specified with this IDial. Bits 14 to 31 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 31 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Group address range specified by the BAR/Mask pair.
33:63	RO	Constant = 0b00000000000000000000000000000000

Register Name		Group Base Address/Mask Register 1
Mnemonic		ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.PEPBREGS.GROUPBAR1_REG
Address		0000000002012013 (SCOM)
Attributes		
Description		Group Base Address/Mask Register 1
Bits	SCOM	Field Mnemonic: Description
0	RW	PE_BUS_GROUP_BAR1_EN: PE bus Group Base Address Register 1 Enable Each BAR/Mask set has 1 enable bit

Registers Specification

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Bits	SCOM	Field Mnemonic: Description
1:14	RW	PE_BUS_GROUP_MASK1: pe bus Group Base Address Register Mask 1 This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 4GB up to 64TB. 64_TB=>0b1111111111111111 32_TB=>0b0111111111111111 16_TB=>0b0011111111111111 8_TB=>0b0001111111111111 4_TB=>0b0000111111111111 2_TB=>0b0000011111111111 1_TB=>0b0000001111111111 512_GB=>0b0000000111111111 256_GB=>0b0000000011111111 128_GB=>0b0000000001111111 64_GB=>0b0000000000111111 32_GB=>0b0000000000001111 16_GB=>0b0000000000000111 8_GB=>0b0000000000000011 4_GB=>0b0000000000000001
15:32	RW	PE_BUS_GROUP_BAR1: pe bus Group Base Address Register 1 Bits 14 to 31 of the Group Base Address 1 range are specified with this IDial. Bits 14 to 31 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 31 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Group address range specified by the BAR/Mask pair.
33:63	RO	Constant = 0b00000000000000000000000000000000

Register Name		Foreign Local Base Address/Mask Register 0
Mnemonic		ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.PEPBREGS.FORL0BAR_REG
Address		0000000002012014 (SCOM)
Attributes		
Description		Foreign Local Base Address/Mask Register 0
Bits	SCOM	Field Mnemonic: Description
0	RW	PE_BUS_FORL0_BAR_EN: PE bus Foreign Link Local 0 Base Address Register Enable Each BAR/Mask set has 1 enable bit



Bits	SCOM	Field Mnemonic: Description
1:19	RW	PE_BUS_FORL0_MASK: pe bus Foreign Link Local 0 Base Address Register Mask This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 16MB up to 8TB. 16_MB=>0b00000000000000000000 32_MB=>0b00000000000000000001 64_MB=>0b00000000000000000011 128_MB=>0b00000000000000000111 256_MB=>0b00000000000000001111 512_MB=>0b00000000000000011111 1_GB=>0b00000000000001111111 2_GB=>0b00000000000011111111 4_GB=>0b00000000000111111111 8_GB=>0b00000000011111111111 16_GB=>0b00000000111111111111 32_GB=>0b00000001111111111111 64_GB=>0b00000011111111111111 128_GB=>0b00000111111111111111 256_GB=>0b00001111111111111111 512_GB=>0b00011111111111111111 1_TB=>0b00111111111111111111 2_TB=>0b01111111111111111111 4_TB=>0b11111111111111111111 8_TB=>0b11111111111111111111
20:45	RW	PE_BUS_FORL0_BAR: pe bus Foreign Link Local 0 Base Address Register Bits 14 to 39 of the Foreign Link Local 0 Base Address range are specified with this IDial. Bits 14 to 39 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 39 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Foreign Link Local 0 address range specified by the BAR/Mask pair.
46:63	RO	Constant = 0b00000000000000000000

Register Name	Foreign Far Base Address/Mask Register 0	
Mnemonic	ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.PEPBREGS.FORF0BAR_REG	
Address	0000000002012015 (SCOM)	
Attributes		
Description	Foreign Far Base Address/Mask Register 0	

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_BUS_FORF0_BAR_EN: PE bus Foreign Link Far 0 Base Address Register Enable Each BAR/Mask set has 1 enable bit

Registers Specification

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Bits	SCOM	Field Mnemonic: Description
1:19	RW	PE_BUS_FORF0_MASK: pe bus Foreign Link Far 0 Base Address Register Mask This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 16 MB up to 8 TB. 16_MB=>0b000000000000000000000000 32_MB=>0b000000000000000000000001 64_MB=>0b000000000000000000000011 128_MB=>0b000000000000000000000111 256_MB=>0b000000000000000000001111 512_MB=>0b000000000000000000011111 1_GB=>0b000000000000000001111111 2_GB=>0b000000000000000011111111 4_GB=>0b000000000000000011111111 8_GB=>0b000000000000000011111111 16_GB=>0b000000000000000011111111 32_GB=>0b000000000000000011111111 64_GB=>0b000000000000000011111111 128_GB=>0b000000000000000011111111 256_GB=>0b000000000000000011111111 512_GB=>0b000000000000000011111111 1_TB=>0b000011111111111111111111 2_TB=>0b001111111111111111111111 4_TB=>0b011111111111111111111111 8_TB=>0b111111111111111111111111
20:45	RW	PE_BUS_FORF0_BAR: pe bus Foreign Link Far 0 Base Address Register Bits 14 to 39 of the Foreign Link Far 0 Base Address range are specified with this IDial. Bits 14 to 39 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 39 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Foreign Link Far 0 address range specified by the BAR/Mask pair.
46:63	RO	Constant = 0b000000000000000000000000

Register Name	Foreign Local Base Address/Mask Register 1	
Mnemonic	ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.PEPBREGS.FORL1BAR_REG	
Address	0000000002012016 (SCOM)	
Attributes		
Description	Foreign Local Base Address/Mask Register 1	

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_BUS_FORL1_BAR_EN: PE bus Foreign Link Local 1 Base Address Register Enable Each BAR/Mask set has 1 enable bit



Bits	SCOM	Field Mnemonic: Description
1:19	RW	PE_BUS_FORL1_MASK: pe bus Foreign Link Local 1 Base Address Register Mask This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 16 MB up to 8 TB. 16_MB=>0b000000000000000000000000 32_MB=>0b000000000000000000000001 64_MB=>0b000000000000000000000011 128_MB=>0b000000000000000000000111 256_MB=>0b000000000000000000001111 512_MB=>0b000000000000000000011111 1_GB=>0b000000000000000001111111 2_GB=>0b000000000000000011111111 4_GB=>0b000000000000000011111111 8_GB=>0b000000000000000011111111 16_GB=>0b000000000000000011111111 32_GB=>0b000000000000000011111111 64_GB=>0b000000001111111111111111 128_GB=>0b000000011111111111111111 256_GB=>0b000000111111111111111111 512_GB=>0b000011111111111111111111 1_TB=>0b000111111111111111111111 2_TB=>0b001111111111111111111111 4_TB=>0b011111111111111111111111 8_TB=>0b111111111111111111111111
20:45	RW	PE_BUS_FORL1_BAR: pe bus Foreign Link Local 1 Base Address Register Bits 14 to 39 of the Foreign Link Local 1 Base Address range are specified with this IDial. Bits 14 to 39 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 39 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Foreign Link Local 1 address range specified by the BAR/Mask pair.
46:63	RO	Constant = 0b000000000000000000000000

Register Name	Foreign Far Base Address/Mask Register 0
Mnemonic	ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.PEPBREGS.FORF1BAR_REG
Address	0000000002012017 (SCOM)
Attributes	
Description	Foreign Far Base Address/Mask Register 0

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_BUS_FORF1_BAR_EN: PE bus Foreign Link Far 1 Base Address Register Enable Each BAR/Mask set has 1 enable bit

Registers Specification

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Bits	SCOM	Field Mnemonic: Description
1:19	RW	PE_BUS_FORF1_MASK: pe bus Foreign Link Far 1 Base Address Register Mask This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 16 MB up to 8 TB. 16_MB=>0b000000000000000000000000 32_MB=>0b000000000000000000000001 64_MB=>0b000000000000000000000011 128_MB=>0b000000000000000000000111 256_MB=>0b000000000000000000001111 512_MB=>0b000000000000000000011111 1_GB=>0b000000000000000001111111 2_GB=>0b000000000000000011111111 4_GB=>0b000000000000000011111111 8_GB=>0b000000000000000011111111 16_GB=>0b000000000000000011111111 32_GB=>0b000000000000000011111111 64_GB=>0b000000000000000011111111 128_GB=>0b000000000000000011111111 256_GB=>0b000000000000000011111111 512_GB=>0b000000000000000011111111 1_TB=>0b000011111111111111111111 2_TB=>0b001111111111111111111111 4_TB=>0b011111111111111111111111 8_TB=>0b111111111111111111111111
20:45	RW	PE_BUS_FORF1_BAR: pe bus Foreign Link Far 1 Base Address Register Bits 14 to 39 of the Foreign Link Far 1 Base Address range are specified with this IDial. Bits 14 to 39 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 39 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Foreign Link Far 1 address range specified by the BAR/Mask pair.
46:63	RO	Constant = 0b000000000000000000000000

Register Name	PE Bus I/O Base Address Register 0
Mnemonic	ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.PEBARS.PE_BUS_IO_BAR0_REG
Address	0000000002012040 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:33	RW	PE_BUS_IO_BAR0: pe bus I/O Base Address Register 0 Bits 14 - 47 of the Base Address range are specified with this IDial. Bits 14 - 47 of a snoop address are compared with this Base Address after ANDing bits 14 - 47 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the address range specified by the BAR/Mask pair.
34:37	RW	Reserved field. (Access type is pe_bus_io_bar0.)
38:63	RO	Constant = 0b000000000000000000000000



Register Name		PE Bus I/O Base Address Register 1
Mnemonic		ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.PEBARS.PE_BUS_IO_BAR1_REG
Address		0000000002012041 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:33	RW	PE_BUS_IO_BAR1: pe bus I/O Base Address Register 1 Bits 14 - 47 of the Base Address range are specified with this IDial. Bits 14 - 47 of a snoop address are compared with this Base Address after ANDing bits 14 - 47 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the address range specified by the BAR/Mask pair.
34:37	RW	Reserved field. (Access type is pe_bus_io_bar1.)
38:63	RO	Constant = 0b000000000000000000000000

Register Name		PE Bus I/O Base Address Register 2
Mnemonic		ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.PEBARS.PE_BUS_IO_BAR2_REG
Address		0000000002012042 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:37	RW	PE_BUS_IO_BAR2: pe bus I/O Base Address Register 2 Bits 14 - 51 of the Base Address range are specified with this IDial. Bits 14 - 51 of a snoop address are compared with this Base Address. If the compare is TRUE, the snoop address falls within the address range specified by the BAR. This BAR is intended for PHB MMIO space that is fixed at 4K; therefore, there is no Mask.
38:63	RO	Constant = 0b000000000000000000000000

Register Name		PE Bus I/O Mask Register 0
Mnemonic		ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.PEBARS.PE_BUS_IO_MASK0_REG
Address		0000000002012043 (SCOM)
Attributes		
Description		

[illegible]



Bits	SCOM	Field Mnemonic: Description
34:63	RO	Constant = 0b00000000000000000000000000000000 1_PB=>0b00000000000000000000000000000000 512_TB=>0b10000000000000000000000000000000 256_TB=>0b11000000000000000000000000000000 128_TB=>0b11100000000000000000000000000000 64_TB=>0b11110000000000000000000000000000 32_TB=>0b11111000000000000000000000000000 16_TB=>0b11111100000000000000000000000000 8_TB=>0b11111110000000000000000000000000 4_TB=>0b11111111000000000000000000000000 2_TB=>0b11111111100000000000000000000000 1_TB=>0b11111111110000000000000000000000 512_GB=>0b11111111111000000000000000000000 256_GB=>0b11111111111100000000000000000000 128_GB=>0b11111111111110000000000000000000 64_GB=>0b11111111111111000000000000000000 32_GB=>0b11111111111111100000000000000000 16_GB=>0b11111111111111110000000000000000 8_GB=>0b11111111111111111000000000000000 4_GB=>0b11111111111111111100000000000000 2_GB=>0b11111111111111111110000000000000 1_GB=>0b11111111111111111111000000000000 512_MB=>0b11111111111111111111100000000000 256_MB=>0b11111111111111111111110000000000 128_MB=>0b11111111111111111111111000000000 64_MB=>0b11111111111111111111111100000000 32_MB=>0b11111111111111111111111110000000 16_MB=>0b11111111111111111111111111000000 8_MB=>0b11111111111111111111111111100000 4_MB=>0b11111111111111111111111111110000 2_MB=>0b11111111111111111111111111111000 1_MB=>0b11111111111111111111111111111000 512_KB=>0b11111111111111111111111111111000 256_KB=>0b11111111111111111111111111111100 128_KB=>0b11111111111111111111111111111110 64_KB=>0b11111111111111111111111111111111

Register Name	PE Bus I/O Mask Register 1
Mnemonic	ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.PEBARS.PE_BUS_IO_MASK1_REG
Address	000000002012044 (SCOM)
Attributes	
Description	

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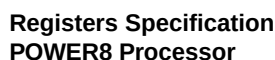
Bits	SCOM	Field Mnemonic: Description
0:33	RW	PE_BUS_IO_MASK1: pe bus I/O Base Address Register Mask 1. This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 16 MB up to 512 GB. 1_PB=>0b00000000000000000000000000000000 512_TB=>0b10000000000000000000000000000000 256_TB=>0b11000000000000000000000000000000 128_TB=>0b11100000000000000000000000000000 64_TB=>0b11110000000000000000000000000000 32_TB=>0b11111000000000000000000000000000 16_TB=>0b11111100000000000000000000000000 8_TB=>0b11111110000000000000000000000000 4_TB=>0b11111111000000000000000000000000 2_TB=>0b11111111100000000000000000000000 1_TB=>0b11111111110000000000000000000000 512_GB=>0b11111111111000000000000000000000 256_GB=>0b11111111111100000000000000000000 128_GB=>0b11111111111110000000000000000000 64_GB=>0b11111111111111000000000000000000 32_GB=>0b11111111111111100000000000000000 16_GB=>0b11111111111111110000000000000000 8_GB=>0b11111111111111111000000000000000 4_GB=>0b11111111111111111100000000000000 2_GB=>0b11111111111111111110000000000000 1_GB=>0b11111111111111111111000000000000 512_MB=>0b11111111111111111111100000000000 256_MB=>0b11111111111111111111110000000000 128_MB=>0b11111111111111111111111000000000 64_MB=>0b11111111111111111111111100000000 32_MB=>0b11111111111111111111111110000000 16_MB=>0b11111111111111111111111111000000 8_MB=>0b11111111111111111111111111100000 4_MB=>0b11111111111111111111111111110000 2_MB=>0b11111111111111111111111111111000 1_MB=>0b11111111111111111111111111111000 512_KB=>0b11111111111111111111111111111000 256_KB=>0b11111111111111111111111111111100 128_KB=>0b11111111111111111111111111111110 64_KB=>0b11111111111111111111111111111111



Bits	SCOM	Field Mnemonic: Description
34:63	RO	Constant = 0b00000000000000000000000000000000 1_PB=>0b00000000000000000000000000000000 512_TB=>0b10000000000000000000000000000000 256_TB=>0b11000000000000000000000000000000 128_TB=>0b11100000000000000000000000000000 64_TB=>0b11110000000000000000000000000000 32_TB=>0b11111000000000000000000000000000 16_TB=>0b11111100000000000000000000000000 8_TB=>0b11111110000000000000000000000000 4_TB=>0b11111111000000000000000000000000 2_TB=>0b11111111100000000000000000000000 1_TB=>0b11111111110000000000000000000000 512_GB=>0b11111111111000000000000000000000 256_GB=>0b11111111111100000000000000000000 128_GB=>0b11111111111110000000000000000000 64_GB=>0b11111111111111000000000000000000 32_GB=>0b11111111111111100000000000000000 16_GB=>0b11111111111111110000000000000000 8_GB=>0b11111111111111111000000000000000 4_GB=>0b11111111111111111100000000000000 2_GB=>0b11111111111111111110000000000000 1_GB=>0b11111111111111111111000000000000 512_MB=>0b11111111111111111111100000000000 256_MB=>0b11111111111111111111110000000000 128_MB=>0b11111111111111111111111000000000 64_MB=>0b11111111111111111111111100000000 32_MB=>0b11111111111111111111111110000000 16_MB=>0b11111111111111111111111111000000 8_MB=>0b11111111111111111111111111100000 4_MB=>0b11111111111111111111111111110000 2_MB=>0b11111111111111111111111111111000 1_MB=>0b11111111111111111111111111111000 512_KB=>0b11111111111111111111111111111000 256_KB=>0b11111111111111111111111111111100 128_KB=>0b11111111111111111111111111111110 64_KB=>0b11111111111111111111111111111111

Register Name	<i>PE Bus I/O Base Address Register Enables</i>	
Mnemonic	ES.PE_WRAP_TOP.PE0.PEPBCQ.PBCQ.PEBARS.PE_BUS_BAR_EN_REG	
Address	0000000002012045 (SCOM)	
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_BUS_IO_BAR0_EN: pe bus I/O Base Address Register 0 Enable. Each BAR/Mask set has one enable bit
1	RW	PE_BUS_IO_BAR1_EN: pe bus I/O Base Address Register 1 Enable. Each BAR/Mask set has one enable bit.
2	RW	PE_BUS_IO_BAR2_EN: pe bus I/O Base Address Register 2 Enable. Each BAR/Mask set has one enable bit.
3	RW	PE_BUS_IRSN_RX_EN: Interrupt Routing Source Number Receive Enable. 0: RIS.EOI and RIS.RTN processor bus Ttypes are not accepted from the processor bus 1: RIS.EOI and RIS.RTN processor bus Ttypes are accepted from the processor bus



Register Name	PCI Nest FIR Register
Mnemonic	ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.FIR_REG
Address	0000000002012400 (SCOM) 0000000002012401 (SCOM1) 0000000002012402 (SCOM2)
Attributes	
Description	PCI Nest FIR Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
21	RWX	WOX_AND	WOX_OR	PBUNSUPPORTEDSIZE: PEC Receive a CI Command that matches one of our Bars but is an unsupported size or address alignment CI Loads Size != 1,2,4,8,16,32 with address naturally aligned CI Store Size != 1,2,4,16,32,64,128 with address naturally aligned
22	RWX	WOX_AND	WOX_OR	PBUNSUPPORTEDCMD: PEC Receive a CI Command that matches one of our Bars but is an unsupported Ttype. Supported Ttypes are ci_pr_rd, ci_pr_ooo_w, ci_pr_w, ris.
23	RWX	WOX_AND	WOX_OR	AIB_PE: The internal AIB had a control or credit parity error.
24	RWX	WOX_AND	WOX_OR	ASB_ERROR: The internal SCOM to ASB bridge has an error
25	RWX	WOX_AND	WOX_OR	FOREIGN_LINK_FAIL: A command received ack_dead or link_chk.abort_op indicating the foreign link is down
26	RWX	WOX_AND	WOX_OR	FOREIGN_PB_HANG: Any processor bus command hang error (in the foreign address range)
27	RWX	WOX_AND	WOX_OR	CAPP_ERROR: Error from CAPP Unit for Freezing PHB
28	RWX	WOX_AND	WOX_OR	SYNC_SCOM_ERR: Error bit from SCOM engines, Nest domain
29	RWX	WOX_AND	WOX_OR	Reserved field. (Access type is local_err0)
30	RWX	WOX_AND	WOX_OR	Reserved field. (Access type is local_err1)
31:63	RO	N/A	N/A	Constant = 0b00000000000000000000000000000000

Register Name	PCI Nest FIR Mask Register
Mnemonic	ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.FIR_MASK_REG
Address	0000000002012403 (SCOM) 0000000002012404 (SCOM1) 0000000002012405 (SCOM2)
Attributes	
Description	PCI Nest FIR Mask Register 0 = No Mask 1 = Mask Error

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	BAR_PE_MASK: One of the BARS or BAR Masks register parity error
1	RW	WO_AND	WO_OR	NONBAR_PE_MASK: Any Non Bar register parity error
2	RW	WO_AND	WO_OR	PB_TO_PEC_CE_MASK: ECC Correctable error off of outbound processor bus
3	RW	WO_AND	WO_OR	PB_TO_PEC_UE_MASK: ECC Uncorrectable error off of outbound processor bus
4	RW	WO_AND	WO_OR	PB_TO_PEC_SUE_MASK: ECC Special Uncorrectable error off of outbound processor bus
5	RW	WO_AND	WO_OR	ARY_ECC_CE_MASK: ECC Correctable error on an internal array
6	RW	WO_AND	WO_OR	ARY_ECC_UE_MASK: ECC Uncorrectable error on an internal array
7	RW	WO_AND	WO_OR	ARY_ECC_SUE_MASK: ECC Special Uncorrectable error on an internal array
8	RW	WO_AND	WO_OR	REGISTER_ARRAY_PE_MASK: Parity error on an internal register file
9	RW	WO_AND	WO_OR	PB_INTERFACE_PE_MASK: Parity Error on PB interface(Address/ATag/TTag/RTAG)

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
10	RW	WO_AND	WO_OR	PB_DATA_HANG_ERRORS_MASK: Any processor bus data hang poll error(Only checked for CI Stores)
11	RW	WO_AND	WO_OR	PB_HANG_ERRORS_MASK: Any processor bus command hang error
12	RW	WO_AND	WO_OR	RD_ARE_ERRORS_MASK: Processor bus ARE detected by DMA read or Atomic engines
13	RW	WO_AND	WO_OR	NONRD_ARE_ERRORS_MASK: Processor bus ARE detected by DMA write or Interrupt engines
14	RW	WO_AND	WO_OR	PCI_HANG_ERROR_MASK: PBCQ detected that PCI load, store, EOI or dma read response did not make forward progress
15	RW	WO_AND	WO_OR	PCI_CLOCK_ERROR_MASK: PBCQ has detected that the PCI clock has stopped
16	RW	WO_AND	WO_OR	AIB_FENCE_MASK: The PHB had a severe error and has fenced the AIB
17	RW	WO_AND	WO_OR	HW_ERRORS_MASK: Any misc hardware error
18	RW	WO_AND	WO_OR	UNSOLICITEDPBDATA_MASK: PEC received data with an RTAG matching a Queue that was not expecting data, or too much data was received.
19	RW	WO_AND	WO_OR	UNEXPECTEDCRESP_MASK: PEC received an unexpected Combined Response
20	RW	WO_AND	WO_OR	INVALIDCRESP_MASK: PEC received an Invalid Combined Response
21	RW	WO_AND	WO_OR	PBUNSUPPORTEDSIZE_MASK: PEC Receive a CI Command that matches one of our Bars but is an unsupported size or address alignment CI Loads Size != 1,2,4,8,16,32 with address naturally aligned CI Store Size != 1,2,4,16,32,64,128 with address naturally aligned
22	RW	WO_AND	WO_OR	PBUNSUPPORTEDCMD_MASK: PEC Receive a CI Command that matches one of our Bars but is an unsupported Ttype. Supported Ttypes are ci_pr_rd, ci_pr_ooo_w, ci_pr_w, ris.
23	RW	WO_AND	WO_OR	AIB_PE_MASK: The internal AIB had a control or credit parity error.
24	RW	WO_AND	WO_OR	ASB_ERROR_MASK: The internal SCOM to ASB bridge has an error
25	RW	WO_AND	WO_OR	FOREIGN_LINK_FAIL_MASK: A command received ack_dead or data hang from the foreign interface
26	RW	WO_AND	WO_OR	FOREIGN_PB_HANG_MASK: Any processor bus command hang error (in the foreign address range)
27	RW	WO_AND	WO_OR	CAPP_ERROR_MASK: Error from CAPP Unit for Freezing PHB
28	RW	WO_AND	WO_OR	SYNC_SCOM_ERR_MASK: Error bit from SCOM engines, Nest domain
29	RW	WO_AND	WO_OR	Reserved field. (Access type is local_err0)
30	RW	WO_AND	WO_OR	Reserved field. (Access type is local_err1)
31:63	RO	N/A	N/A	Constant = 0b00000000000000000000000000000000

Register Name	<i>PCI Nest FIR Action0 Register</i>
Mnemonic	ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.FIR_ACTION0_REG
Address	0000000002012406 (SCOM)
Attributes	
Description	PCI Nest FIR Action0 Register



Bits	SCOM	Field Mnemonic: Description
0:30	RW	FIR_ACTION0: Action0 select for corresponding bit in FIR (Action0,Mask) = Action Select (0,0) = Checkstop Error (0,1) = Recoverable Error (1,0) = No Action (1,1) = Freeze
31:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>PCI Nest FIR Action1 Register</i>
Mnemonic	ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.FIR_ACTION1_REG
Address	0000000002012407 (SCOM)
Attributes	
Description	PCI Nest FIR Action1 Register

Bits	SCOM	Field Mnemonic: Description
0:30	RW	FIR_ACTION1: Action1 select for corresponding bit in FIR (Action1,Mask) = Action Select (0,0) = Checkstop Error (0,1) = Recoverable Error (1,0) = No Action (1,1) = Freeze
31:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>Pci Nest Fir Wof Register</i>
Mnemonic	ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.FIR_WOF_REG
Address	0000000002012408 (SCOM)
Attributes	
Description	pci nest fir wof register

Bits	SCOM	Field Mnemonic: Description
0:30	RWX_WCLRR EG	
31:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>Nodal Base Address/Mask Register 0</i>
Mnemonic	ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.PEPBREGS.NODALBAR0_REG
Address	0000000002012410 (SCOM)
Attributes	
Description	Nodal Base Address/Mask Register 0

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_BUS_NODAL_BAR0_EN: PE bus Nodal Base Address Register 0 Enable Each BAR/Mask set has 1 enable bit

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Bits	SCOM	Field Mnemonic: Description
1:14	RW	PE_BUS_NODAL_MASK0: pe bus Nodal Base Address Register Mask 0 This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 4GB up to 64TB. 64_TB=>0b1111111111111111 32_TB=>0b0111111111111111 16_TB=>0b0011111111111111 8_TB=>0b0001111111111111 4_TB=>0b0000111111111111 2_TB=>0b0000011111111111 1_TB=>0b0000001111111111 512_GB=>0b0000000111111111 256_GB=>0b0000000011111111 128_GB=>0b0000000001111111 64_GB=>0b0000000000111111 32_GB=>0b0000000000011111 16_GB=>0b0000000000001111 8_GB=>0b0000000000000111 4_GB=>0b0000000000000011
15:32	RW	PE_BUS_NODAL_BAR0: pe bus Nodal Base Address Register 0 Bits 14 to 31 of the Nodal Base Address 0 range are specified with this IDial. Bits 14 to 31 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 31 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Nodal address range specified by the BAR/Mask pair.
33:63	RO	Constant = 0b00000000000000000000000000000000

Register Name		Nodal Base Address/Mask Register 1
Mnemonic		ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.PEPBREGS.NODALBAR1_REG
Address		0000000002012411 (SCOM)
Attributes		
Description		Nodal Base Address/Mask Register 1
Bits	SCOM	Field Mnemonic: Description
0	RW	PE_BUS_NODAL_BAR1_EN: PE bus Nodal Base Address Register 1 Enable Each BAR/Mask set has 1 enable bit



Bits	SCOM	Field Mnemonic: Description
1:14	RW	PE_BUS_NODAL_MASK1: pe bus Nodal Base Address Register Mask 1 This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 4GB up to 64TB. 64_TB=>0b1111111111111111 32_TB=>0b0111111111111111 16_TB=>0b0011111111111111 8_TB=>0b0001111111111111 4_TB=>0b0000111111111111 2_TB=>0b0000011111111111 1_TB=>0b0000001111111111 512_GB=>0b000000011111111 256_GB=>0b000000001111111 128_GB=>0b000000000111111 64_GB=>0b000000000011111 32_GB=>0b000000000000111 16_GB=>0b000000000000011 8_GB=>0b000000000000001 4_GB=>0b000000000000000
15:32	RW	PE_BUS_NODAL_BAR1: pe bus Nodal Base Address Register 1 Bits 14 to 31 of the Nodal Base Address 1 range are specified with this IDial. Bits 14 to 31 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 31 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Nodal address range specified by the BAR/Mask pair.
33:63	RO	Constant = 0b00000000000000000000000000000000

Register Name		Group Base Address/Mask Register 0
Mnemonic		ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.PEPBREGS.GROUPBAR0_REG
Address		0000000002012412 (SCOM)
Attributes		
Description		Group Base Address/Mask Register 0
Bits	SCOM	Field Mnemonic: Description
0	RW	PE_BUS_GROUP_BAR0_EN: PE bus Group Base Address Register 0 Enable Each BAR/Mask set has 1 enable bit

Registers Specification

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Bits	SCOM	Field Mnemonic: Description
1:14	RW	PE_BUS_GROUP_MASK0: pe bus Group Base Address Register Mask 0 This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 4GB up to 64TB. 64_TB=>0b1111111111111111 32_TB=>0b0111111111111111 16_TB=>0b0011111111111111 8_TB=>0b0001111111111111 4_TB=>0b0000111111111111 2_TB=>0b0000011111111111 1_TB=>0b0000001111111111 512_GB=>0b0000000111111111 256_GB=>0b0000000011111111 128_GB=>0b0000000001111111 64_GB=>0b0000000000111111 32_GB=>0b0000000000011111 16_GB=>0b0000000000001111 8_GB=>0b0000000000000111 4_GB=>0b0000000000000011
15:32	RW	PE_BUS_GROUP_BAR0: pe bus Group Base Address Register 0 Bits 14 to 31 of the Group Base Address 0 range are specified with this IDial. Bits 14 to 31 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 31 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Group address range specified by the BAR/Mask pair.
33:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Group Base Address/Mask Register 1	
Mnemonic	ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.PEPBREGS.GROUPBAR1_REG	
Address	0000000002012413 (SCOM)	
Attributes		
Description	Group Base Address/Mask Register 1	

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_BUS_GROUP_BAR1_EN: PE bus Group Base Address Register 1 Enable Each BAR/Mask set has 1 enable bit



Bits	SCOM	Field Mnemonic: Description
1:14	RW	PE_BUS_GROUP_MASK1: pe bus Group Base Address Register Mask 1 This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 4GB up to 64TB. 64_TB=>0b11111111111111 32_TB=>0b01111111111111 16_TB=>0b00111111111111 8_TB=>0b00011111111111 4_TB=>0b00001111111111 2_TB=>0b00000111111111 1_TB=>0b00000011111111 512_GB=>0b00000001111111 256_GB=>0b00000000111111 128_GB=>0b00000000011111 64_GB=>0b00000000001111 32_GB=>0b000000000000111 16_GB=>0b0000000000000011 8_GB=>0b0000000000000001 4_GB=>0b0000000000000000
15:32	RW	PE_BUS_GROUP_BAR1: pe bus Group Base Address Register 1 Bits 14 to 31 of the Group Base Address 1 range are specified with this IDial. Bits 14 to 31 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 31 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Group address range specified by the BAR/Mask pair.
33:63	RO	Constant = 0b00000000000000000000000000000000

Register Name		Foreign Local Base Address/Mask Register 0
Mnemonic		ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.PEPBREGS.FORL0BAR_REG
Address		0000000002012414 (SCOM)
Attributes		
Description		Foreign Local Base Address/Mask Register 0
Bits	SCOM	Field Mnemonic: Description
0	RW	PE_BUS_FORL0_BAR_EN: PE bus Foreign Link Local 0 Base Address Register Enable Each BAR/Mask set has 1 enable bit

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Bits	SCOM	Field Mnemonic: Description
1:19	RW	PE_BUS_FORL0_MASK: pe bus Foreign Link Local 0 Base Address Register Mask This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 16MB up to 8TB. 16_MB=>0b000000000000000000000000 32_MB=>0b000000000000000000000001 64_MB=>0b000000000000000000000011 128_MB=>0b000000000000000000000111 256_MB=>0b000000000000000000001111 512_MB=>0b000000000000000000011111 1_GB=>0b000000000000000001111111 2_GB=>0b000000000000000011111111 4_GB=>0b000000000000000011111111 8_GB=>0b000000000000000011111111 16_GB=>0b000000000000000011111111 32_GB=>0b000000000000000011111111 64_GB=>0b000000000000000011111111 128_GB=>0b000000000000000011111111 256_GB=>0b000000000000000011111111 512_GB=>0b000000000000000011111111 1_TB=>0b000011111111111111111111 2_TB=>0b001111111111111111111111 4_TB=>0b011111111111111111111111 8_TB=>0b111111111111111111111111
20:45	RW	PE_BUS_FORL0_BAR: pe bus Foreign Link Local 0 Base Address Register Bits 14 to 39 of the Foreign Link Local 0 Base Address range are specified with this IDial. Bits 14 to 39 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 39 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Foreign Link Local 0 address range specified by the BAR/Mask pair.
46:63	RO	Constant = 0b000000000000000000000000

Register Name		Foreign Far Base Address/Mask Register 0
Mnemonic		ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.PEPBREGS.FORF0BAR_REG
Address		0000000002012415 (SCOM)
Attributes		
Description		Foreign Far Base Address/Mask Register 0

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_BUS_FORF0_BAR_EN: PE bus Foreign Link Far 0 Base Address Register Enable Each BAR/Mask set has 1 enable bit

Bits	SCOM	Field Mnemonic: Description
1:19	RW	PE_BUS_FORF0_MASK: pe bus Foreign Link Far 0 Base Address Register Mask This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 16 MB up to 8 TB. 16_MB=>0b00000000000000000000 32_MB=>0b00000000000000000001 64_MB=>0b00000000000000000011 128_MB=>0b00000000000000000111 256_MB=>0b00000000000000001111 512_MB=>0b00000000000000011111 1_GB=>0b00000000000001111111 2_GB=>0b00000000000011111111 4_GB=>0b00000000000111111111 8_GB=>0b00000000011111111111 16_GB=>0b00000000111111111111 32_GB=>0b00000001111111111111 64_GB=>0b00000011111111111111 128_GB=>0b00000111111111111111 256_GB=>0b00001111111111111111 512_GB=>0b00011111111111111111 1_TB=>0b00111111111111111111 2_TB=>0b01111111111111111111 4_TB=>0b11111111111111111111 8_TB=>0b11111111111111111111
20:45	RW	PE_BUS_FORF0_BAR: pe bus Foreign Link Far 0 Base Address Register Bits 14 to 39 of the Foreign Link Far 0 Base Address range are specified with this IDial. Bits 14 to 39 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 39 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Foreign Link Far 0 address range specified by the BAR/Mask pair.
46:63	RO	Constant = 0b00000000000000000000

Register Name	Foreign Local Base Address/Mask Register 1	
Mnemonic	ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.PEPBREGS.FORL1BAR_REG	
Address	000000002012416 (SCOM)	
Attributes		
Description	Foreign Local Base Address/Mask Register 1	

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_BUS_FORL1_BAR_EN: PE bus Foreign Link Local 1 Base Address Register Enable Each BAR/Mask set has 1 enable bit

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Bits	SCOM	Field Mnemonic: Description
1:19	RW	PE_BUS_FORL1_MASK: pe bus Foreign Link Local 1 Base Address Register Mask This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 16 MB up to 8 TB. 16_MB=>0b000000000000000000000000 32_MB=>0b000000000000000000000001 64_MB=>0b000000000000000000000011 128_MB=>0b000000000000000000000111 256_MB=>0b000000000000000000001111 512_MB=>0b000000000000000000011111 1_GB=>0b000000000000000001111111 2_GB=>0b000000000000000011111111 4_GB=>0b000000000000000011111111 8_GB=>0b000000000000000011111111 16_GB=>0b000000000000000011111111 32_GB=>0b000000000000000011111111 64_GB=>0b000000000000000011111111 128_GB=>0b000000000000000011111111 256_GB=>0b000000000000000011111111 512_GB=>0b000000000000000011111111 1_TB=>0b000011111111111111111111 2_TB=>0b001111111111111111111111 4_TB=>0b011111111111111111111111 8_TB=>0b111111111111111111111111
20:45	RW	PE_BUS_FORL1_BAR: pe bus Foreign Link Local 1 Base Address Register Bits 14 to 39 of the Foreign Link Local 1 Base Address range are specified with this IDial. Bits 14 to 39 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 39 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Foreign Link Local 1 address range specified by the BAR/Mask pair.
46:63	RO	Constant = 0b000000000000000000000000

Register Name	Foreign Far Base Address/Mask Register 0	
Mnemonic	ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.PEPBREGS.FORF1BAR_REG	
Address	0000000002012417 (SCOM)	
Attributes		
Description	Foreign Far Base Address/Mask Register 0	

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_BUS_FORF1_BAR_EN: PE bus Foreign Link Far 1 Base Address Register Enable Each BAR/Mask set has 1 enable bit

Bits	SCOM	Field Mnemonic: Description
1:19	RW	PE_BUS_FORF1_MASK: pe bus Foreign Link Far 1 Base Address Register Mask This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 16 MB up to 8 TB. 16_MB=>0b00000000000000000000 32_MB=>0b00000000000000000001 64_MB=>0b00000000000000000011 128_MB=>0b00000000000000000111 256_MB=>0b00000000000000001111 512_MB=>0b00000000000000011111 1_GB=>0b00000000000001111111 2_GB=>0b00000000000011111111 4_GB=>0b00000000000111111111 8_GB=>0b00000000001111111111 16_GB=>0b00000000011111111111 32_GB=>0b00000000111111111111 64_GB=>0b00000001111111111111 128_GB=>0b00000011111111111111 256_GB=>0b00000111111111111111 512_GB=>0b00001111111111111111 1_TB=>0b00011111111111111111 2_TB=>0b00111111111111111111 4_TB=>0b01111111111111111111 8_TB=>0b11111111111111111111
20:45	RW	PE_BUS_FORF1_BAR: pe bus Foreign Link Far 1 Base Address Register Bits 14 to 39 of the Foreign Link Far 1 Base Address range are specified with this IDial. Bits 14 to 39 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 39 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Foreign Link Far 1 address range specified by the BAR/Mask pair.
46:63	RO	Constant = 0b00000000000000000000

Register Name	PE Bus I/O Base Address Register 0
Mnemonic	ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.PEBARS.PE_BUS_IO_BAR0_REG
Address	0000000002012440 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:33	RW	PE_BUS_IO_BAR0: pe bus I/O Base Address Register 0 Bits 14 - 47 of the Base Address range are specified with this IDial. Bits 14 - 47 of a snoop address are compared with this Base Address after ANDing bits 14 - 47 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the address range specified by the BAR/Mask pair.
34:37	RW	Reserved field. (Access type is pe_bus_io_bar0.)
38:63	RO	Constant = 0b00000000000000000000000000000000



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Register Name	PE Bus I/O Base Address Register 1
Mnemonic	ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.PEBARS.PE_BUS_IO_BAR1_REG
Address	0000000002012441 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:33	RW	PE_BUS_IO_BAR1: pe bus I/O Base Address Register 1 Bits 14 - 47 of the Base Address range are specified with this IDial. Bits 14 - 47 of a snoop address are compared with this Base Address after ANDing bits 14 - 47 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the address range specified by the BAR/Mask pair.
34:37	RW	Reserved field. (Access type is pe_bus_io_bar1.)
38:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	PE Bus I/O Base Address Register 2
Mnemonic	ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.PEBARS.PE_BUS_IO_BAR2_REG
Address	0000000002012442 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:37	RW	PE_BUS_IO_BAR2: pe bus I/O Base Address Register 2 Bits 14 - 51 of the Base Address range are specified with this IDial. Bits 14 - 51 of a snoop address are compared with this Base Address If the compare is TRUE, the snoop address falls within the address range specified by the BAR. This BAR is intended for PHB MMIO space which is fixed at 4K; therefore, there is no mask.
38:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	PE Bus I/O Mask Register 0
Mnemonic	ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.PEBARS.PE_BUS_IO_MASK0_REG
Address	0000000002012443 (SCOM)
Attributes	
Description	



Bits	SCOM	Field Mnemonic: Description
0:33	RW	PE_BUS_IO_MASK0: pe bus I/O Base Address Register Mask 0 This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 64KB up to 2PB. 1_PB=>0b00000000000000000000000000000000 512_TB=>0b10000000000000000000000000000000 256_TB=>0b11000000000000000000000000000000 128_TB=>0b11100000000000000000000000000000 64_TB=>0b11110000000000000000000000000000 32_TB=>0b11111000000000000000000000000000 16_TB=>0b11111100000000000000000000000000 8_TB=>0b11111110000000000000000000000000 4_TB=>0b11111111000000000000000000000000 2_TB=>0b11111111100000000000000000000000 1_TB=>0b11111111110000000000000000000000 512_GB=>0b11111111111100000000000000000000 256_GB=>0b11111111111110000000000000000000 128_GB=>0b11111111111111000000000000000000 64_GB=>0b11111111111111100000000000000000 32_GB=>0b11111111111111110000000000000000 16_GB=>0b11111111111111111000000000000000 8_GB=>0b11111111111111111100000000000000 4_GB=>0b11111111111111111110000000000000 2_GB=>0b11111111111111111111000000000000 1_GB=>0b11111111111111111111100000000000 512_MB=>0b11111111111111111111110000000000 256_MB=>0b11111111111111111111111000000000 128_MB=>0b11111111111111111111111100000000 64_MB=>0b11111111111111111111111110000000 32_MB=>0b11111111111111111111111111000000 16_MB=>0b11111111111111111111111111100000 8_MB=>0b111111111111111111111111111100000 4_MB=>0b1111111111111111111111111111100000 2_MB=>0b1111111111111111111111111111110000 1_MB=>0b1111111111111111111111111111111000 512_KB=>0b1111111111111111111111111111111000 256_KB=>0b1111111111111111111111111111111100 128_KB=>0b1111111111111111111111111111111110 64_KB=>0b1111111111111111111111111111111111



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Bits	SCOM	Field Mnemonic: Description
34:63	RO	Constant = 0b00000000000000000000000000000000 1_PB=>0b00000000000000000000000000000000 512_TB=>0b10000000000000000000000000000000 256_TB=>0b11000000000000000000000000000000 128_TB=>0b11100000000000000000000000000000 64_TB=>0b11110000000000000000000000000000 32_TB=>0b11111000000000000000000000000000 16_TB=>0b11111100000000000000000000000000 8_TB=>0b11111110000000000000000000000000 4_TB=>0b11111111000000000000000000000000 2_TB=>0b11111111100000000000000000000000 1_TB=>0b11111111110000000000000000000000 512_GB=>0b11111111111000000000000000000000 256_GB=>0b11111111111100000000000000000000 128_GB=>0b11111111111110000000000000000000 64_GB=>0b11111111111111000000000000000000 32_GB=>0b11111111111111100000000000000000 16_GB=>0b11111111111111110000000000000000 8_GB=>0b11111111111111111000000000000000 4_GB=>0b11111111111111111100000000000000 2_GB=>0b11111111111111111110000000000000 1_GB=>0b11111111111111111111000000000000 512_MB=>0b11111111111111111111100000000000 256_MB=>0b11111111111111111111110000000000 128_MB=>0b11111111111111111111111000000000 64_MB=>0b11111111111111111111111100000000 32_MB=>0b11111111111111111111111110000000 16_MB=>0b11111111111111111111111111000000 8_MB=>0b11111111111111111111111111100000 4_MB=>0b11111111111111111111111111110000 2_MB=>0b11111111111111111111111111111000 1_MB=>0b11111111111111111111111111111100 512_KB=>0b11111111111111111111111111111100 256_KB=>0b11111111111111111111111111111110 128_KB=>0b11111111111111111111111111111111 64_KB=>0b11111111111111111111111111111111

Register Name	PE Bus I/O Mask Register 1
Mnemonic	ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.PEBARS.PE_BUS_IO_MASK1_REG
Address	0000000002012444 (SCOM)
Attributes	
Description	



Bits	SCOM	Field Mnemonic: Description
0:33	RW	PE_BUS_IO_MASK1: pe bus I/O Base Address Register Mask 1. This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 16 MB up to 512 GB. 1_PB=>0b00000000000000000000000000000000 512_TB=>0b10000000000000000000000000000000 256_TB=>0b11000000000000000000000000000000 128_TB=>0b11100000000000000000000000000000 64_TB=>0b11110000000000000000000000000000 32_TB=>0b11111000000000000000000000000000 16_TB=>0b11111100000000000000000000000000 8_TB=>0b11111110000000000000000000000000 4_TB=>0b11111111000000000000000000000000 2_TB=>0b11111111100000000000000000000000 1_TB=>0b11111111110000000000000000000000 512_GB=>0b11111111111000000000000000000000 256_GB=>0b11111111111100000000000000000000 128_GB=>0b11111111111110000000000000000000 64_GB=>0b11111111111111000000000000000000 32_GB=>0b11111111111111100000000000000000 16_GB=>0b11111111111111110000000000000000 8_GB=>0b11111111111111111000000000000000 4_GB=>0b11111111111111111100000000000000 2_GB=>0b11111111111111111110000000000000 1_GB=>0b11111111111111111111000000000000 512_MB=>0b11111111111111111111100000000000 256_MB=>0b11111111111111111111110000000000 128_MB=>0b11111111111111111111111000000000 64_MB=>0b11111111111111111111111100000000 32_MB=>0b11111111111111111111111110000000 16_MB=>0b11111111111111111111111111000000 8_MB=>0b11111111111111111111111111100000 4_MB=>0b11111111111111111111111111110000 2_MB=>0b11111111111111111111111111111000 1_MB=>0b11111111111111111111111111111000 512_KB=>0b11111111111111111111111111111000 256_KB=>0b11111111111111111111111111111100 128_KB=>0b11111111111111111111111111111110 64_KB=>0b11111111111111111111111111111111

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Bits	SCOM	Field Mnemonic: Description
34:63	RO	Constant = 0b00000000000000000000000000000000 1_PB=>0b00000000000000000000000000000000 512_TB=>0b10000000000000000000000000000000 256_TB=>0b11000000000000000000000000000000 128_TB=>0b11100000000000000000000000000000 64_TB=>0b11110000000000000000000000000000 32_TB=>0b11111000000000000000000000000000 16_TB=>0b11111100000000000000000000000000 8_TB=>0b11111110000000000000000000000000 4_TB=>0b11111111000000000000000000000000 2_TB=>0b11111111100000000000000000000000 1_TB=>0b11111111110000000000000000000000 512_GB=>0b11111111110000000000000000000000 256_GB=>0b11111111111000000000000000000000 128_GB=>0b11111111111100000000000000000000 64_GB=>0b11111111111110000000000000000000 32_GB=>0b11111111111111000000000000000000 16_GB=>0b11111111111111100000000000000000 8_GB=>0b11111111111111110000000000000000 4_GB=>0b11111111111111111000000000000000 2_GB=>0b11111111111111111100000000000000 1_GB=>0b11111111111111111110000000000000 512_MB=>0b11111111111111111111000000000000 256_MB=>0b11111111111111111111100000000000 128_MB=>0b11111111111111111111110000000000 64_MB=>0b11111111111111111111111000000000 32_MB=>0b11111111111111111111111100000000 16_MB=>0b11111111111111111111111110000000 8_MB=>0b11111111111111111111111111000000 4_MB=>0b11111111111111111111111111100000 2_MB=>0b11111111111111111111111111110000 1_MB=>0b11111111111111111111111111111000 512_KB=>0b11111111111111111111111111111100 256_KB=>0b11111111111111111111111111111110 128_KB=>0b11111111111111111111111111111111 64_KB=>0b11111111111111111111111111111111

Register Name	PE Bus I/O Base Address Register Enables	
Mnemonic	ES.PE_WRAP_TOP.PE1.PEPBCQ.PBCQ.PEBARS.PE_BUS_BAR_EN_REG	
Address	0000000002012445 (SCOM)	
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_BUS_IO_BAR0_EN: pe bus I/O Base Address Register 0 Enable. Each BAR/Mask set has 1 enable bit.
1	RW	PE_BUS_IO_BAR1_EN: pe bus I/O Base Address Register 1 Enable. Each BAR/Mask set has 1 enable bit.
2	RW	PE_BUS_IO_BAR2_EN: pe bus I/O Base Address Register 2 Enable. Each BAR/Mask set has 1 enable bit.
3	RW	PE_BUS_IRSN_RX_EN: Interrupt Routing Source Number Receive Enable. 0: RIS.EOI and RIS.RTN processor bus Ttypes are not accepted from the processor bus. 1: RIS.EOI and RIS.RTN processor bus Ttypes are accepted from the processor bus.
4	RW	PE_BUS_IRSN_TX_EN: Interrupt Routing Source Number Transmit Enable. 0: RIS.Request processor bus Ttypes are not sent to the processor bus. 1: RIS.Request processor bus Ttypes are sent to the processor bus.

[illegible]

Register Name	<i>PCI Nest FIR Register</i>
Mnemonic	ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.FIR_REG
Address	0000000002012800 (SCOM) 0000000002012801 (SCOM1) 0000000002012802 (SCOM2)
Attributes	
Description	PCI Nest FIR Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	BAR_PE: One of the BARS or BAR Masks register parity error
1	RWX	WOX_AND	WOX_OR	NONBAR_PE: Any Non Bar register parity error
2	RWX	WOX_AND	WOX_OR	PB_TO_PEC_CE: ECC Correctable error off of outbound processor bus
3	RWX	WOX_AND	WOX_OR	PB_TO_PEC_UE: ECC Uncorrectable error off of outbound processor bus
4	RWX	WOX_AND	WOX_OR	PB_TO_PEC_SUE: ECC Special Uncorrectable error off of outbound processor bus
5	RWX	WOX_AND	WOX_OR	ARY_ECC_CE: ECC Correctable error on an internal array
6	RWX	WOX_AND	WOX_OR	ARY_ECC_UE: ECC Uncorrectable error on an internal array
7	RWX	WOX_AND	WOX_OR	ARY_ECC_SUE: ECC Special Uncorrectable error on an internal array
8	RWX	WOX_AND	WOX_OR	REGISTER_ARRAY_PE: Parity error on an internal register file
9	RWX	WOX_AND	WOX_OR	PB_INTERFACE_PE: Parity Error on PB interface(Address/ATag/TTAG/RTAG)
10	RWX	WOX_AND	WOX_OR	PB_DATA_HANG_ERRORS: Any processor bus data hang poll error(Only checked for CI Stores)
11	RWX	WOX_AND	WOX_OR	PB_HANG_ERRORS: Any processor bus command hang error (in the domestic address range)
12	RWX	WOX_AND	WOX_OR	RD_ARE_ERRORS: Processor bus ARE detected by DMA read or Atomic engines
13	RWX	WOX_AND	WOX_OR	NONRD_ARE_ERRORS: Processor bus ARE detected by DMA write or Interrupt engines
14	RWX	WOX_AND	WOX_OR	PCI_HANG_ERROR: PBCQ detected that PCI load, store, EOI or dma read response did not make forward progress
15	RWX	WOX_AND	WOX_OR	PCI_CLOCK_ERROR: PBCQ has detected that the PCI clock has stopped
16	RWX	WOX_AND	WOX_OR	AIB_FENCE: The PHB had a severe error and has fenced the AIB
17	RWX	WOX_AND	WOX_OR	HW_ERRORS: Any misc hardware error
18	RWX	WOX_AND	WOX_OR	UNSOLICITEDPBDATA: PEC received data with an RTAG matching a Queue that was not expecting data, or too much data was received.
19	RWX	WOX_AND	WOX_OR	UNEXPECTEDCRESP: PEC received an unexpected Combined Response
20	RWX	WOX_AND	WOX_OR	INVALIDCRESP: PEC received an Invalid Combined Response
21	RWX	WOX_AND	WOX_OR	PBUNSUPPORTEDSIZE: PEC Receive a CI Command that matches one of our Bars but is an unsupported size or address alignment CI Loads Size != 1,2,4,8,16,32 with address naturally aligned CI Store Size != 1,2,4,16,32,64,128 with address naturally aligned

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
22	RWX	WOX_AND	WOX_OR	PBUNSUPPORTEDCMD: PEC Receive a CI Command that matches one of our Bars but is an unsupported Ttype. Supported Ttypes are ci_pr_rd, ci_pr_ooo_w, ci_pr_w, ris.
23	RWX	WOX_AND	WOX_OR	AIB_PE: The internal AIB had a control or credit parity error.
24	RWX	WOX_AND	WOX_OR	ASB_ERROR: The internal SCOM to ASB bridge has an error
25	RWX	WOX_AND	WOX_OR	FOREIGN_LINK_FAIL: A command received ack_dead or link_chk.abort_op indicating the foreign link is down
26	RWX	WOX_AND	WOX_OR	FOREIGN_PB_HANG: Any processor bus command hang error (in the foreign address range)
27	RWX	WOX_AND	WOX_OR	CAPP_ERROR: Error from CAPP Unit for Freezing PHB
28	RWX	WOX_AND	WOX_OR	SYNC_SCOM_ERR: Error bit from SCOM engines, Nest domain
29	RWX	WOX_AND	WOX_OR	Reserved field. (Access type is local_err0)
30	RWX	WOX_AND	WOX_OR	Reserved field. (Access type is local_err1)
31:63	RO	N/A	N/A	Constant = 0b00000000000000000000000000000000

Register Name	PCI Nest FIR Mask Register
Mnemonic	ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.FIR_MASK_REG
Address	0000000002012803 (SCOM) 0000000002012804 (SCOM1) 0000000002012805 (SCOM2)
Attributes	
Description	PCI Nest FIR Mask Register 0 = No Mask 1 = Mask Error

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	BAR_PE_MASK: One of the BARS or BAR Masks register parity error
1	RW	WO_AND	WO_OR	NONBAR_PE_MASK: Any Non Bar register parity error
2	RW	WO_AND	WO_OR	PB_TO_PEC_CE_MASK: ECC Correctable error off of outbound processor bus
3	RW	WO_AND	WO_OR	PB_TO_PEC_UE_MASK: ECC Uncorrectable error off of outbound processor bus
4	RW	WO_AND	WO_OR	PB_TO_PEC_SUE_MASK: ECC Special Uncorrectable error off of outbound processor bus
5	RW	WO_AND	WO_OR	ARY_ECC_CE_MASK: ECC Correctable error on an internal array
6	RW	WO_AND	WO_OR	ARY_ECC_UE_MASK: ECC Uncorrectable error on an internal array
7	RW	WO_AND	WO_OR	ARY_ECC_SUE_MASK: ECC Special Uncorrectable error on an internal array
8	RW	WO_AND	WO_OR	REGISTER_ARRAY_PE_MASK: Parity error on an internal register file
9	RW	WO_AND	WO_OR	PB_INTERFACE_PE_MASK: Parity Error on PB interface(Address/ATag/Ttag/RTAG)
10	RW	WO_AND	WO_OR	PB_DATA_HANG_ERRORS_MASK: Any processor bus data hang poll error(Only checked for CI Stores)
11	RW	WO_AND	WO_OR	PB_HANG_ERRORS_MASK: Any processor bus command hang error



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
12	RW	WO_AND	WO_OR	RD_ARE_ERRORS_MASK: Processor bus ARE detected by DMA read or Atomic engines
13	RW	WO_AND	WO_OR	NONRD_ARE_ERRORS_MASK: Processor bus ARE detected by DMA write or Interrupt engines
14	RW	WO_AND	WO_OR	PCI_HANG_ERROR_MASK: PBCQ detected that PCI load, store, EOI or dma read response did not make forward progress
15	RW	WO_AND	WO_OR	PCI_CLOCK_ERROR_MASK: PBCQ has detected that the PCI clock has stopped
16	RW	WO_AND	WO_OR	AIB_FENCE_MASK: The PHB had a severe error and has fenced the AIB
17	RW	WO_AND	WO_OR	HW_ERRORS_MASK: Any misc hardware error
18	RW	WO_AND	WO_OR	UNSOLICITEDPBDATA_MASK: PEC received data with an RTAG matching a Queue that was not expecting data, or too much data was received.
19	RW	WO_AND	WO_OR	UNEXPECTEDCRESP_MASK: PEC received an unexpected Combined Response
20	RW	WO_AND	WO_OR	INVALIDCRESP_MASK: PEC received an Invalid Combined Response
21	RW	WO_AND	WO_OR	PBUNSUPPORTEDSIZE_MASK: PEC Receive a CI Command that matches one of our Bars but is an unsupported size or address alignment CI Loads Size != 1,2,4,8,16,32 with address naturally aligned CI Store Size != 1,2,4,16,32,64,128 with address naturally aligned
22	RW	WO_AND	WO_OR	PBUNSUPPORTEDCMD_MASK: PEC Receive a CI Command that matches one of our Bars but is an unsupported Ttype. Supported Ttypes are ci_pr_rd, ci_pr_ooo_w, ci_pr_w, ris.
23	RW	WO_AND	WO_OR	AIB_PE_MASK: The internal AIB had a control or credit parity error.
24	RW	WO_AND	WO_OR	ASB_ERROR_MASK: The internal SCOM to ASB bridge has an error
25	RW	WO_AND	WO_OR	FOREIGN_LINK_FAIL_MASK: A command received ack_dead or data hang from the foreign interface
26	RW	WO_AND	WO_OR	FOREIGN_PB_HANG_MASK: Any processor bus command hang error (in the foreign address range)
27	RW	WO_AND	WO_OR	CAPP_ERROR_MASK: Error from CAPP Unit for Freezing PHB
28	RW	WO_AND	WO_OR	SYNC_SCOM_ERR_MASK: Error bit from SCOM engines, Nest domain
29	RW	WO_AND	WO_OR	Reserved field. (Access type is local_err0)
30	RW	WO_AND	WO_OR	Reserved field. (Access type is local_err1)
31:63	RO	N/A	N/A	Constant = 0b00000000000000000000000000000000

Register Name	PCI Nest FIR Action0 Register
Mnemonic	ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.FIR_ACTION0_REG
Address	0000000002012806 (SCOM)
Attributes	
Description	PCI Nest FIR Action0 Register

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Bits	SCOM	Field Mnemonic: Description
0:30	RW	FIR_ACTION0: Action0 select for corresponding bit in FIR (Action0,Mask) = Action Select (0,0) = Checkstop Error (0,1) = Recoverable Error (1,0) = No Action (1,1) = Freeze
31:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>PCI Nest FIR Action1 Register</i>
Mnemonic	ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.FIR_ACTION1_REG
Address	0000000002012807 (SCOM)
Attributes	
Description	PCI Nest FIR Action1 Register

Bits	SCOM	Field Mnemonic: Description
0:30	RW	FIR_ACTION1: Action1 select for corresponding bit in FIR (Action1,Mask) = Action Select (0,0) = Checkstop Error (0,1) = Recoverable Error (1,0) = No Action (1,1) = Freeze
31:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>Pci Nest Fir Wof Register</i>
Mnemonic	ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.FIR_WOF_REG
Address	0000000002012808 (SCOM)
Attributes	
Description	pci nest fir wof register

Bits	SCOM	Field Mnemonic: Description
0:30	RWX_WCLRR EG	
31:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>Nodal Base Address/Mask Register 0</i>
Mnemonic	ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.PEPBREGS.NODALBAR0_REG
Address	0000000002012810 (SCOM)
Attributes	
Description	Nodal Base Address/Mask Register 0

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_BUS_NODAL_BAR0_EN: PE bus Nodal Base Address Register 0 Enable Each BAR/Mask set has 1 enable bit



Bits	SCOM	Field Mnemonic: Description
1:14	RW	PE_BUS_NODAL_MASK0: pe bus Nodal Base Address Register Mask 0 This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 4GB up to 64TB. 64_TB=>0b11111111111111 32_TB=>0b01111111111111 16_TB=>0b00111111111111 8_TB=>0b00011111111111 4_TB=>0b00001111111111 2_TB=>0b00000111111111 1_TB=>0b00000011111111 512_GB=>0b00000001111111 256_GB=>0b00000000111111 128_GB=>0b00000000011111 64_GB=>0b00000000001111 32_GB=>0b00000000000011 16_GB=>0b00000000000001 8_GB=>0b000000000000001 4_GB=>0b000000000000000
15:32	RW	PE_BUS_NODAL_BAR0: pe bus Nodal Base Address Register 0 Bits 14 to 31 of the Nodal Base Address 0 range are specified with this IDial. Bits 14 to 31 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 31 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Nodal address range specified by the BAR/Mask pair.
33:63	RO	Constant = 0b00000000000000000000000000000000

Register Name		Nodal Base Address/Mask Register 1
Mnemonic		ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.PEPBREGS.NODALBAR1_REG
Address		0000000002012811 (SCOM)
Attributes		
Description		Nodal Base Address/Mask Register 1
Bits	SCOM	Field Mnemonic: Description
0	RW	PE_BUS_NODAL_BAR1_EN: PE bus Nodal Base Address Register 1 Enable Each BAR/Mask set has 1 enable bit

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Bits	SCOM	Field Mnemonic: Description
1:14	RW	PE_BUS_NODAL_MASK1: pe bus Nodal Base Address Register Mask 1 This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 4GB up to 64TB. 64_TB=>0b1111111111111111 32_TB=>0b0111111111111111 16_TB=>0b0011111111111111 8_TB=>0b0001111111111111 4_TB=>0b0000111111111111 2_TB=>0b0000011111111111 1_TB=>0b0000001111111111 512_GB=>0b0000000111111111 256_GB=>0b0000000011111111 128_GB=>0b0000000001111111 64_GB=>0b0000000000111111 32_GB=>0b0000000000001111 16_GB=>0b0000000000000111 8_GB=>0b0000000000000011 4_GB=>0b0000000000000001
15:32	RW	PE_BUS_NODAL_BAR1: pe bus Nodal Base Address Register 1 Bits 14 to 31 of the Nodal Base Address 1 range are specified with this IDial. Bits 14 to 31 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 31 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Nodal address range specified by the BAR/Mask pair.
33:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Group Base Address/Mask Register 0	
Mnemonic	ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.PEPBREGS.GROUPBAR0_REG	
Address	0000000002012812 (SCOM)	
Attributes		
Description	Group Base Address/Mask Register 0	
Bits	SCOM	Field Mnemonic: Description
0	RW	PE_BUS_GROUP_BAR0_EN: PE bus Group Base Address Register 0 Enable Each BAR/Mask set has 1 enable bit



Bits	SCOM	Field Mnemonic: Description
1:14	RW	PE_BUS_GROUP_MASK0: pe bus Group Base Address Register Mask 0 This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 4GB up to 64TB. 64_TB=>0b11111111111111 32_TB=>0b01111111111111 16_TB=>0b00111111111111 8_TB=>0b00011111111111 4_TB=>0b00001111111111 2_TB=>0b00000111111111 1_TB=>0b00000011111111 512_GB=>0b00000001111111 256_GB=>0b00000000111111 128_GB=>0b00000000011111 64_GB=>0b00000000001111 32_GB=>0b00000000000111 16_GB=>0b00000000000011 8_GB=>0b00000000000001 4_GB=>0b00000000000000
15:32	RW	PE_BUS_GROUP_BAR0: pe bus Group Base Address Register 0 Bits 14 to 31 of the Group Base Address 0 range are specified with this IDial. Bits 14 to 31 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 31 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Group address range specified by the BAR/Mask pair.
33:63	RO	Constant = 0b00000000000000000000000000000000

Register Name		Group Base Address/Mask Register 1
Mnemonic		ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.PEPBREGS.GROUPBAR1_REG
Address		0000000002012813 (SCOM)
Attributes		
Description		Group Base Address/Mask Register 1
Bits	SCOM	Field Mnemonic: Description
0	RW	PE_BUS_GROUP_BAR1_EN: PE bus Group Base Address Register 1 Enable Each BAR/Mask set has 1 enable bit

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Bits	SCOM	Field Mnemonic: Description
1:14	RW	PE_BUS_GROUP_MASK1: pe bus Group Base Address Register Mask 1 This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 4GB up to 64TB. 64_TB=>0b11111111111111 32_TB=>0b01111111111111 16_TB=>0b00111111111111 8_TB=>0b00011111111111 4_TB=>0b00001111111111 2_TB=>0b00000111111111 1_TB=>0b00000011111111 512_GB=>0b00000001111111 256_GB=>0b00000000111111 128_GB=>0b00000000011111 64_GB=>0b00000000001111 32_GB=>0b00000000000111 16_GB=>0b00000000000011 8_GB=>0b00000000000001 4_GB=>0b00000000000000
15:32	RW	PE_BUS_GROUP_BAR1: pe bus Group Base Address Register 1 Bits 14 to 31 of the Group Base Address 1 range are specified with this IDial. Bits 14 to 31 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 31 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Group address range specified by the BAR/Mask pair.
33:63	RO	Constant = 0b00000000000000000000000000000000

Register Name		Foreign Local Base Address/Mask Register 0
Mnemonic		ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.PEPBREGS.FORL0BAR_REG
Address		0000000002012814 (SCOM)
Attributes		
Description		Foreign Local Base Address/Mask Register 0
Bits	SCOM	Field Mnemonic: Description
0	RW	PE_BUS_FORL0_BAR_EN: PE bus Foreign Link Local 0 Base Address Register Enable Each BAR/Mask set has 1 enable bit

Bits	SCOM	Field Mnemonic: Description
1:19	RW	PE_BUS_FORL0_MASK: pe bus Foreign Link Local 0 Base Address Register Mask This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 16MB up to 8TB. 16_MB=>0b00000000000000000000 32_MB=>0b00000000000000000001 64_MB=>0b00000000000000000011 128_MB=>0b00000000000000000111 256_MB=>0b00000000000000001111 512_MB=>0b00000000000000011111 1_GB=>0b00000000000001111111 2_GB=>0b00000000000011111111 4_GB=>0b00000000000111111111 8_GB=>0b00000000011111111111 16_GB=>0b00000000111111111111 32_GB=>0b00000001111111111111 64_GB=>0b00000011111111111111 128_GB=>0b00000111111111111111 256_GB=>0b00001111111111111111 512_GB=>0b00011111111111111111 1_TB=>0b00111111111111111111 2_TB=>0b01111111111111111111 4_TB=>0b11111111111111111111 8_TB=>0b11111111111111111111
20:45	RW	PE_BUS_FORL0_BAR: pe bus Foreign Link Local 0 Base Address Register Bits 14 to 39 of the Foreign Link Local 0 Base Address range are specified with this IDial. Bits 14 to 39 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 39 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Foreign Link Local 0 address range specified by the BAR/Mask pair.
46:63	RO	Constant = 0b00000000000000000000

Register Name	Foreign Far Base Address/Mask Register 0	
Mnemonic	ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.PEPBREGS.FORF0BAR_REG	
Address	0000000002012815 (SCOM)	
Attributes		
Description	Foreign Far Base Address/Mask Register 0	

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_BUS_FORF0_BAR_EN: PE bus Foreign Link Far 0 Base Address Register Enable Each BAR/Mask set has 1 enable bit

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Bits	SCOM	Field Mnemonic: Description
1:19	RW	PE_BUS_FORF0_MASK: pe bus Foreign Link Far 0 Base Address Register Mask This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 16 MB up to 8 TB. 16_MB=>0b000000000000000000000000 32_MB=>0b000000000000000000000001 64_MB=>0b000000000000000000000011 128_MB=>0b000000000000000000000111 256_MB=>0b000000000000000000001111 512_MB=>0b000000000000000000011111 1_GB=>0b000000000000000001111111 2_GB=>0b000000000000000011111111 4_GB=>0b000000000000000011111111 8_GB=>0b000000000000000011111111 16_GB=>0b000000000000000011111111 32_GB=>0b000000000000000011111111 64_GB=>0b000000000000000011111111 128_GB=>0b000000000000000011111111 256_GB=>0b000000000000000011111111 512_GB=>0b000000000000000011111111 1_TB=>0b000011111111111111111111 2_TB=>0b001111111111111111111111 4_TB=>0b011111111111111111111111 8_TB=>0b111111111111111111111111
20:45	RW	PE_BUS_FORF0_BAR: pe bus Foreign Link Far 0 Base Address Register Bits 14 to 39 of the Foreign Link Far 0 Base Address range are specified with this IDial. Bits 14 to 39 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 39 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Foreign Link Far 0 address range specified by the BAR/Mask pair.
46:63	RO	Constant = 0b000000000000000000000000

Register Name		Foreign Local Base Address/Mask Register 1
Mnemonic		ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.PEPBREGS.FORL1BAR_REG
Address		0000000002012816 (SCOM)
Attributes		
Description		Foreign Local Base Address/Mask Register 1

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_BUS_FORL1_BAR_EN: PE bus Foreign Link Local 1 Base Address Register Enable Each BAR/Mask set has 1 enable bit

Bits	SCOM	Field Mnemonic: Description
1:19	RW	PE_BUS_FORL1_MASK: pe bus Foreign Link Local 1 Base Address Register Mask This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 16 MB up to 8 TB. 16_MB=>0b00000000000000000000 32_MB=>0b00000000000000000001 64_MB=>0b00000000000000000011 128_MB=>0b00000000000000000111 256_MB=>0b00000000000000001111 512_MB=>0b00000000000000011111 1_GB=>0b00000000000001111111 2_GB=>0b00000000000011111111 4_GB=>0b00000000000111111111 8_GB=>0b00000000011111111111 16_GB=>0b00000000111111111111 32_GB=>0b00000001111111111111 64_GB=>0b00000011111111111111 128_GB=>0b00000111111111111111 256_GB=>0b00001111111111111111 512_GB=>0b00011111111111111111 1_TB=>0b00111111111111111111 2_TB=>0b01111111111111111111 4_TB=>0b11111111111111111111 8_TB=>0b11111111111111111111
20:45	RW	PE_BUS_FORL1_BAR: pe bus Foreign Link Local 1 Base Address Register Bits 14 to 39 of the Foreign Link Local 1 Base Address range are specified with this IDial. Bits 14 to 39 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 39 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Foreign Link Local 1 address range specified by the BAR/Mask pair.
46:63	RO	Constant = 0b00000000000000000000

Register Name	Foreign Far Base Address/Mask Register 0	
Mnemonic	ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.PEPBREGS.FORF1BAR_REG	
Address	0000000002012817 (SCOM)	
Attributes		
Description	Foreign Far Base Address/Mask Register 0	

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_BUS_FORF1_BAR_EN: PE bus Foreign Link Far 1 Base Address Register Enable Each BAR/Mask set has 1 enable bit

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Bits	SCOM	Field Mnemonic: Description
1:19	RW	PE_BUS_FORF1_MASK: pe bus Foreign Link Far 1 Base Address Register Mask This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 16 MB up to 8 TB. 16_MB=>0b000000000000000000000000 32_MB=>0b000000000000000000000001 64_MB=>0b000000000000000000000011 128_MB=>0b000000000000000000000111 256_MB=>0b000000000000000000001111 512_MB=>0b000000000000000000011111 1_GB=>0b000000000000000001111111 2_GB=>0b000000000000000001111111 4_GB=>0b000000000000000001111111 8_GB=>0b000000000000000001111111 16_GB=>0b000000000000000001111111 32_GB=>0b000000000000000001111111 64_GB=>0b000000000000000001111111 128_GB=>0b000000000000000001111111 256_GB=>0b000000000000000001111111 512_GB=>0b000000000000000001111111 1_TB=>0b000000000000000001111111 2_TB=>0b000000000000000001111111 4_TB=>0b000000000000000001111111 8_TB=>0b000000000000000001111111
20:45	RW	PE_BUS_FORF1_BAR: pe bus Foreign Link Far 1 Base Address Register Bits 14 to 39 of the Foreign Link Far 1 Base Address range are specified with this IDial. Bits 14 to 39 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 39 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Foreign Link Far 1 address range specified by the BAR/Mask pair.
46:63	RO	Constant = 0b000000000000000000000000

Register Name	<i>PE Bus I/O Base Address Register 0</i>	
Mnemonic	ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.PEBARS.PE_BUS_IO_BAR0_REG	
Address	0000000002012840 (SCOM)	
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0:33	RW	PE_BUS_IO_BAR0: pe bus I/O Base Address Register 0. Bits 14 - 47 of the Base Address range are specified with this IDial. Bits 14 - 47 of a snoop address are compared with this Base Address after ANDing bits 14 - 47 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the address range specified by the BAR/Mask pair.
34:37	RW	Reserved field. (Access type is pe_bus_io_bar0.)
38:63	RO	Constant = 0b000000000000000000000000



Register Name		PE Bus I/O Base Address Register 1
Mnemonic		ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.PEBARS.PE_BUS_IO_BAR1_REG
Address		0000000002012841 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:33	RW	PE_BUS_IO_BAR1: pe bus I/O Base Address Register 1 Bits 14 - 47 of the Base Address range are specified with this IDial. Bits 14 - 47 of a snoop address are compared with this Base Address after ANDing bits 14 - 47 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the address range specified by the BAR/Mask pair.
34:37	RW	Reserved field. (Access type is pe_bus_io_bar1)
38:63	RO	Constant = 0b000000000000000000000000

Register Name		PE Bus I/O Base Address Register 2
Mnemonic		ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.PEBARS.PE_BUS_IO_BAR2_REG
Address		0000000002012842 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:37	RW	PE_BUS_IO_BAR2: pe bus I/O Base Address Register 2. Bits 14 - 51 of the Base Address range are specified with this IDial. Bits 14 - 51 of a snoop address are compared with this Base Address. If the compare is TRUE, the snoop address falls within the address range specified by the BAR. This BAR is intended for PHB MMIO space which is fixed at 4K, so there is no mask.
38:63	RO	Constant = 0b000000000000000000000000

Register Name		PE Bus I/O Mask Register 0
Mnemonic		ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.PEBARS.PE_BUS_IO_MASK0_REG
Address		0000000002012843 (SCOM)
Attributes		
Description		

[illegible]



Bits	SCOM	Field Mnemonic: Description
34:63	RO	Constant = 0b00000000000000000000000000000000 1_PB=>0b00000000000000000000000000000000 512_TB=>0b10000000000000000000000000000000 256_TB=>0b11000000000000000000000000000000 128_TB=>0b11100000000000000000000000000000 64_TB=>0b11110000000000000000000000000000 32_TB=>0b11111000000000000000000000000000 16_TB=>0b11111100000000000000000000000000 8_TB=>0b11111110000000000000000000000000 4_TB=>0b11111111000000000000000000000000 2_TB=>0b11111111100000000000000000000000 1_TB=>0b11111111110000000000000000000000 512_GB=>0b11111111111000000000000000000000 256_GB=>0b11111111111100000000000000000000 128_GB=>0b11111111111110000000000000000000 64_GB=>0b11111111111111000000000000000000 32_GB=>0b11111111111111100000000000000000 16_GB=>0b11111111111111110000000000000000 8_GB=>0b11111111111111111000000000000000 4_GB=>0b11111111111111111100000000000000 2_GB=>0b11111111111111111110000000000000 1_GB=>0b11111111111111111111000000000000 512_MB=>0b11111111111111111111100000000000 256_MB=>0b11111111111111111111110000000000 128_MB=>0b11111111111111111111111000000000 64_MB=>0b11111111111111111111111100000000 32_MB=>0b11111111111111111111111110000000 16_MB=>0b11111111111111111111111111000000 8_MB=>0b11111111111111111111111111100000 4_MB=>0b11111111111111111111111111110000 2_MB=>0b11111111111111111111111111111000 1_MB=>0b11111111111111111111111111111000 512_KB=>0b11111111111111111111111111111000 256_KB=>0b11111111111111111111111111111100 128_KB=>0b11111111111111111111111111111110 64_KB=>0b11111111111111111111111111111111

Register Name	PE Bus I/O Mask Register 1
Mnemonic	ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.PEBARS.PE_BUS_IO_MASK1_REG
Address	000000002012844 (SCOM)
Attributes	
Description	

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Bits	SCOM	Field Mnemonic: Description
0:33	RW	PE_BUS_IO_MASK1: pe bus I/O Base Address Register Mask 1. This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 16 MB up to 512 GB. 1_PB=>0b00000000000000000000000000000000 512_TB=>0b10000000000000000000000000000000 256_TB=>0b11000000000000000000000000000000 128_TB=>0b11100000000000000000000000000000 64_TB=>0b11110000000000000000000000000000 32_TB=>0b11111000000000000000000000000000 16_TB=>0b11111100000000000000000000000000 8_TB=>0b11111110000000000000000000000000 4_TB=>0b11111111000000000000000000000000 2_TB=>0b11111111100000000000000000000000 1_TB=>0b11111111110000000000000000000000 512_GB=>0b11111111111000000000000000000000 256_GB=>0b11111111111100000000000000000000 128_GB=>0b11111111111110000000000000000000 64_GB=>0b11111111111111000000000000000000 32_GB=>0b11111111111111100000000000000000 16_GB=>0b11111111111111110000000000000000 8_GB=>0b11111111111111111000000000000000 4_GB=>0b11111111111111111100000000000000 2_GB=>0b11111111111111111110000000000000 1_GB=>0b11111111111111111111000000000000 512_MB=>0b11111111111111111111100000000000 256_MB=>0b11111111111111111111110000000000 128_MB=>0b11111111111111111111111000000000 64_MB=>0b11111111111111111111111100000000 32_MB=>0b11111111111111111111111110000000 16_MB=>0b11111111111111111111111111000000 8_MB=>0b11111111111111111111111111100000 4_MB=>0b11111111111111111111111111110000 2_MB=>0b11111111111111111111111111111000 1_MB=>0b11111111111111111111111111111000 512_KB=>0b11111111111111111111111111111000 256_KB=>0b11111111111111111111111111111100 128_KB=>0b11111111111111111111111111111110 64_KB=>0b11111111111111111111111111111111



Bits	SCOM	Field Mnemonic: Description
34:63	RO	Constant = 0b00000000000000000000000000000000 1_PB=>0b00000000000000000000000000000000 512_TB=>0b10000000000000000000000000000000 256_TB=>0b11000000000000000000000000000000 128_TB=>0b11100000000000000000000000000000 64_TB=>0b11110000000000000000000000000000 32_TB=>0b11111000000000000000000000000000 16_TB=>0b11111100000000000000000000000000 8_TB=>0b11111110000000000000000000000000 4_TB=>0b11111111000000000000000000000000 2_TB=>0b11111111100000000000000000000000 1_TB=>0b11111111110000000000000000000000 512_GB=>0b11111111111000000000000000000000 256_GB=>0b11111111111100000000000000000000 128_GB=>0b11111111111110000000000000000000 64_GB=>0b11111111111111000000000000000000 32_GB=>0b11111111111111100000000000000000 16_GB=>0b11111111111111110000000000000000 8_GB=>0b11111111111111111000000000000000 4_GB=>0b11111111111111111100000000000000 2_GB=>0b11111111111111111110000000000000 1_GB=>0b11111111111111111111000000000000 512_MB=>0b11111111111111111111100000000000 256_MB=>0b11111111111111111111110000000000 128_MB=>0b11111111111111111111111000000000 64_MB=>0b11111111111111111111111100000000 32_MB=>0b11111111111111111111111110000000 16_MB=>0b11111111111111111111111111000000 8_MB=>0b11111111111111111111111111100000 4_MB=>0b11111111111111111111111111110000 2_MB=>0b11111111111111111111111111111000 1_MB=>0b11111111111111111111111111111000 512_KB=>0b11111111111111111111111111111000 256_KB=>0b11111111111111111111111111111100 128_KB=>0b11111111111111111111111111111110 64_KB=>0b11111111111111111111111111111111

Register Name	PE Bus I/O Base Address Register Enables
Mnemonic	ES.PE_WRAP_TOP.PE2.PEPBCQ.PBCQ.PEBARS.PE_BUS_BAR_EN_REG
Address	0000000002012845 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	PE_BUS_IO_BAR0_EN: pe bus I/O Base Address Register 0 Enable. Each BAR/Mask set has 1 enable bit.
1	RW	PE_BUS_IO_BAR1_EN: pe bus I/O Base Address Register 1 Enable. Each BAR/Mask set has 1 enable bit.
2	RW	PE_BUS_IO_BAR2_EN: pe bus I/O Base Address Register 2 Enable. Each BAR/Mask set has 1 enable bit.
3	RW	PE_BUS_IRSN_RX_EN: Interrupt Routing Source Number Receive Enable. 0: RIS.EOI and RIS.RTN processor bus Ttypes are not accepted from the processor bus. 1: RIS.EOI and RIS.RTN processor bus Ttypes are accepted from the processor bus.
4	RW	PE_BUS_IRSN_TX_EN: Interrupt Routing Source Number Transmit Enable. 0: RIS.Request processor bus Ttypes are not sent to the processor bus. 1: RIS.Request processor bus Ttypes are sent to the processor bus.



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Bits	SCOM	Field Mnemonic: Description
5:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>APC Master Nodal BAR0 Register</i>
Mnemonic	EN.NX.CXA.CXA_APC1.NODAL_BAR0
Address	000000000201302D (SCOM)
Attributes	
Description	If enabled, mask and address are used to define an address region used for determining Scope to be used for a processor bus command.

Bits	SCOM	Field Mnemonic: Description
0	RW	NODAL_BAR0_ENB: Nodal Bar0 Enable
1:14	RW	NODAL_BAR0_MASK: Nodal Bar0 mask 18:31
15:32	RW	NODAL_BAR0_ADDR: Nodal Bar0 address 14:31
33:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>APC Master Nodal BAR1 Register</i>
Mnemonic	EN.NX.CXA.CXA_APC1.NODAL_BAR1
Address	000000000201302E (SCOM)
Attributes	
Description	If enabled, mask and address are used to define an address region used for determining Scope to be used for a processor bus command.

Bits	SCOM	Field Mnemonic: Description
0	RW	NODAL_BAR1_ENB: Nodal bar1 Enable
1:14	RW	NODAL_BAR1_MASK: Nodal bar1 mask 18:31
15:32	RW	NODAL_BAR1_ADDR: Nodal bar1 address 14:31
33:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>APC Master Global BAR0 Register</i>
Mnemonic	EN.NX.CXA.CXA_APC1.GLOBAL_BAR0
Address	000000000201302F (SCOM)
Attributes	
Description	If enabled, mask and address are used to define an address region used for determining Scope to be used for a processor bus command.

Bits	SCOM	Field Mnemonic: Description
0	RW	GLOBAL_BAR0_ENB: Global bar0 enable
1:14	RW	GLOBAL_BAR0_MASK: Global bar0 mask 18:31
15:32	RW	GLOBAL_BAR0_ADDR: Global bar0 address 14:31
33:63	RO	Constant = 0b00000000000000000000000000000000



Register Name	<i>APC Master Global BAR1 Register</i>
Mnemonic	EN.NX.CXA.CXA_APC1.GLOBAL_BAR1
Address	0000000002013030 (SCOM)
Attributes	
Description	If enabled, mask and address are used to define an address region used for determining Scope to be used for a processor bus command.

Bits	SCOM	Field Mnemonic: Description
0	RW	GLOBAL_BAR1_ENB: Global bar1 enable
1:14	RW	GLOBAL_BAR1_MASK: Global bar1 mask 18:31
15:32	RW	GLOBAL_BAR1_ADDR: Global bar1 address 14:31
33:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	<i>APC Master Foreign Local BAR0 Register</i>
Mnemonic	EN.NX.CXA.CXA_APC1.FOREIGN_LOC_BAR0
Address	0000000002013031 (SCOM)
Attributes	
Description	If enabled, mask and address are used to define an address region used for determining Scope to be used for a processor bus command.

Bits	SCOM	Field Mnemonic: Description
0	RW	FOREIGN_LOC_BAR0_ENB: Foreign Local bar0 enable
1:19	RW	FOREIGN_LOC_BAR0_MASK: Foreign Local bar0 mask 21:39
20:45	RW	FOREIGN_LOC_BAR0_ADDR: Foreign Local bar0 address 14:39
46:63	RO	Constant = 0b000000000000000000000000

Register Name	<i>APC Master Foreign Far BAR0 Register</i>
Mnemonic	EN.NX.CXA.CXA_APC1.FOREIGN_FAR_BAR0
Address	0000000002013032 (SCOM)
Attributes	
Description	If enabled, mask and address are used to define an address region used for determining Scope to be used for a processor bus command.

Bits	SCOM	Field Mnemonic: Description
0	RW	FOREIGN_FAR_BAR0_ENB: Foreign Far bar0 enable
1:19	RW	FOREIGN_FAR_BAR0_MASK: Foreign Far bar0 mask 21:39
20:45	RW	FOREIGN_FAR_BAR0_ADDR: Foreign Far bar0 address 14:39
46:63	RO	Constant = 0b000000000000000000000000

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Register Name	<i>APC Master Foreign Local BAR1 Register</i>
Mnemonic	EN.NX.CXA.CXA_APC1.FOREIGN_LOC_BAR1
Address	0000000002013033 (SCOM)
Attributes	
Description	If enabled, mask and address are used to define an address region used for determining Scope to be used for a processor bus command.

Bits	SCOM	Field Mnemonic: Description
0	RW	FOREIGN_LOC_BAR1_ENB: Foreign Local bar1 enable
1:19	RW	FOREIGN_LOC_BAR1_MASK: Foreign Local bar1 mask 21:39
20:45	RW	FOREIGN_LOC_BAR1_ADDR: Foreign Local bar1 address 14:39
46:63	RO	Constant = 0b00000000000000000000

Register Name	<i>APC Master Foreign Far BAR1 Register</i>
Mnemonic	EN.NX.CXA.CXA_APC1.FOREIGN_FAR_BAR1
Address	0000000002013034 (SCOM)
Attributes	
Description	If enabled, mask and address are used to define an address region used for determining Scope to be used for a processor bus command.

Bits	SCOM	Field Mnemonic: Description
0	RW	FOREIGN_FAR_BAR1_ENB: Foreign Far bar1 enable
1:19	RW	FOREIGN_FAR_BAR1_MASK: Foreign Far bar1 mask 21:39
20:45	RW	FOREIGN_FAR_BAR1_ADDR: Foreign Far bar1 address 14:39
46:63	RO	Constant = 0b00000000000000000000

Register Name	<i>Processor Bus MMIO BAR Register</i>
Mnemonic	EN.NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_MMIO_BAR
Address	000000000201308D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:13	RO	Constant = 0b0000000000000000
14:51	RW	MMIO_BAR: MMIO bar for NX
52	RW	MMIO_BAR_ENABLE: Enable MMIO for NX
53:55	RW	MMIO_BAR_SIZE: MMIO bar size for NX
56:63	RO	Constant = 0b00000000



Register Name		<i>NODAL BAR0 Range Register</i>
Mnemonic		EN.NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_NODAL_BAR0
Address		0000000002013095 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0	RW	NX_PB_NODAL_BAR0_EN: PE bus Nodal Base Address Register 0 Enable. Each BAR/Mask set has one enable bit.
1:14	RW	NX_PB_NODAL_MASK0: pe bus Nodal Base Address Register Mask 0 This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 4GB up to 64TB. 64_TB=>0b11111111111111 32_TB=>0b01111111111111 16_TB=>0b00111111111111 8_TB=>0b00011111111111 4_TB=>0b00001111111111 2_TB=>0b00000111111111 1_TB=>0b00000011111111 512_GB=>0b00000001111111 256_GB=>0b00000000111111 128_GB=>0b00000000011111 64_GB=>0b00000000001111 32_GB=>0b00000000000111 16_GB=>0b00000000000011 8_GB=>0b00000000000001 4_GB=>0b00000000000000
15:32	RW	NX_PB_NODAL_BAR0: pe bus Nodal Base Address Register 0 Bits 14 to 31 of the Nodal Base Address 0 range are specified with this IDial. Bits 14 to 31 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 31 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Nodal address range specified by the BAR/Mask pair.
33:63	RO	Constant = 0b00000000000000000000000000000000

Register Name		<i>NODAL BAR1 Range Register</i>
Mnemonic		EN.NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_NODAL_BAR1
Address		0000000002013096 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0	RW	NX_PB_NODAL_BAR1_EN: PE bus Nodal Base Address Register 1 Enable Each BAR/Mask set has 1 enable bit

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Bits	SCOM	Field Mnemonic: Description
1:14	RW	NX_PB_NODAL_MASK1: pe bus Nodal Base Address Register Mask 1 This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 4GB up to 64TB. 64_TB=>0b11111111111111 32_TB=>0b01111111111111 16_TB=>0b00111111111111 8_TB=>0b00011111111111 4_TB=>0b00001111111111 2_TB=>0b00000111111111 1_TB=>0b00000011111111 512_GB=>0b00000001111111 256_GB=>0b00000000111111 128_GB=>0b00000000011111 64_GB=>0b00000000001111 32_GB=>0b00000000000111 16_GB=>0b00000000000011 8_GB=>0b00000000000001 4_GB=>0b00000000000000
15:32	RW	NX_PB_NODAL_BAR1: pe bus Nodal Base Address Register 1 Bits 14 to 31 of the Nodal Base Address 1 range are specified with this IDial. Bits 14 to 31 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 31 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Nodal address range specified by the BAR/Mask pair.
33:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	GROUP BAR0 Range Register	
Mnemonic	EN.NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_GROUP_BAR0	
Address	0000000002013097 (SCOM)	
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0	RW	NX_PB_GROUP_BAR0_EN: PE bus Group Base Address Register 0 Enable Each BAR/Mask set has 1 enable bit



Bits	SCOM	Field Mnemonic: Description
1:14	RW	NX_PB_GROUP_MASK0: pe bus Group Base Address Register Mask 0 This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 4GB up to 64TB. 64_TB=>0b1111111111111111 32_TB=>0b0111111111111111 16_TB=>0b0011111111111111 8_TB=>0b0001111111111111 4_TB=>0b0000111111111111 2_TB=>0b0000011111111111 1_TB=>0b0000001111111111 512_GB=>0b000000011111111 256_GB=>0b000000001111111 128_GB=>0b000000000111111 64_GB=>0b000000000011111 32_GB=>0b000000000000111 16_GB=>0b000000000000011 8_GB=>0b000000000000001 4_GB=>0b000000000000000
15:32	RW	NX_PB_GROUP_BAR0: pe bus Group Base Address Register 0 Bits 14 to 31 of the Group Base Address 0 range are specified with this IDial. Bits 14 to 31 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 31 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Group address range specified by the BAR/Mask pair.
33:63	RO	Constant = 0b00000000000000000000000000000000

Register Name		GROUP BAR1 Range Register
Mnemonic		EN.NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_GROUP_BAR1
Address		0000000002013098 (SCOM)
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0	RW	NX_PB_GROUP_BAR1_EN: PE bus Group Base Address Register 1 Enable Each BAR/Mask set has 1 enable bit

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Bits	SCOM	Field Mnemonic: Description
1:14	RW	NX_PB_GROUP_MASK1: pe bus Group Base Address Register Mask 1 This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 4GB up to 64TB. 64_TB=>0b11111111111111 32_TB=>0b01111111111111 16_TB=>0b00111111111111 8_TB=>0b00011111111111 4_TB=>0b00001111111111 2_TB=>0b00000111111111 1_TB=>0b00000011111111 512_GB=>0b00000001111111 256_GB=>0b00000000111111 128_GB=>0b00000000011111 64_GB=>0b00000000001111 32_GB=>0b00000000000111 16_GB=>0b00000000000011 8_GB=>0b00000000000001 4_GB=>0b00000000000000
15:32	RW	NX_PB_GROUP_BAR1: pe bus Group Base Address Register 1 Bits 14 to 31 of the Group Base Address 1 range are specified with this IDial. Bits 14 to 31 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 31 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Group address range specified by the BAR/Mask pair.
33:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	FOREIGN_L BAR0 Range Register
Mnemonic	EN.NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_FOREIGN_L_BAR0
Address	0000000002013099 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	NX_PB_FORLO_BAR_EN: PE bus Foreign Link Local 0 Base Address Register Enable Each BAR/Mask set has 1 enable bit

Bits	SCOM	Field Mnemonic: Description
1:19	RW	NX_PB_FORL0_MASK: pe bus Foreign Link Local 0 Base Address Register Mask This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 16MB up to 8TB. 16_MB=>0b000000000000000000000000 32_MB=>0b000000000000000000000001 64_MB=>0b000000000000000000000011 128_MB=>0b000000000000000000000111 256_MB=>0b000000000000000000001111 512_MB=>0b000000000000000000011111 1_GB=>0b000000000000000001111111 2_GB=>0b000000000000000011111111 4_GB=>0b000000000000000011111111 8_GB=>0b000000000000000011111111 16_GB=>0b000000000000000011111111 32_GB=>0b000000000000000011111111 64_GB=>0b000000000000000011111111 128_GB=>0b000000000000000011111111 256_GB=>0b000000000000000011111111 512_GB=>0b000000000000000011111111 1_TB=>0b000000000000000011111111 2_TB=>0b000000000000000011111111 4_TB=>0b000000000000000011111111 8_TB=>0b000000000000000011111111
20:45	RW	NX_PB_FORL0_BAR: pe bus Foreign Link Local 0 Base Address Register Bits 14 to 39 of the Foreign Link Local 0 Base Address range are specified with this IDial. Bits 14 to 39 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 39 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Foreign Link Local 0 address range specified by the BAR/Mask pair.
46:63	RO	Constant = 0b000000000000000000000000

Register Name	<i>FOREIGN_L BAR1 Range Register</i>	
Mnemonic	EN.NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_FOREIGN_L_BAR1	
Address	000000000201309A (SCOM)	
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0	RW	NX_PB_FORL1_BAR_EN: PE bus Foreign Link Local 1 Base Address Register Enable Each BAR/Mask set has 1 enable bit

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Bits	SCOM	Field Mnemonic: Description
1:19	RW	NX_PB_FORL1_MASK: pe bus Foreign Link Local 1 Base Address Register Mask This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 16 MB up to 8 TB. 16_MB=>0b000000000000000000000000 32_MB=>0b000000000000000000000001 64_MB=>0b000000000000000000000011 128_MB=>0b000000000000000000000111 256_MB=>0b000000000000000000001111 512_MB=>0b000000000000000000011111 1_GB=>0b000000000000000001111111 2_GB=>0b000000000000000011111111 4_GB=>0b000000000000000011111111 8_GB=>0b000000000000000011111111 16_GB=>0b000000000000000011111111 32_GB=>0b000000000000000011111111 64_GB=>0b000000000000000011111111 128_GB=>0b000000000000000011111111 256_GB=>0b000000000000000011111111 512_GB=>0b000000000000000011111111 1_TB=>0b000000000000000011111111 2_TB=>0b000000000000000011111111 4_TB=>0b000000000000000011111111 8_TB=>0b000000000000000011111111
20:45	RW	NX_PB_FORL1_BAR: pe bus Foreign Link Local 1 Base Address Register Bits 14 to 39 of the Foreign Link Local 1 Base Address range are specified with this IDial. Bits 14 to 39 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 39 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Foreign Link Local 1 address range specified by the BAR/Mask pair.
46:63	RO	Constant = 0b000000000000000000000000

Register Name	FOREIGN_F BAR0 Range Register	
Mnemonic	EN.NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_FOREIGN_F_BAR0	
Address	000000000201309B (SCOM)	
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0	RW	NX_PB_FORF0_BAR_EN: PE bus Foreign Link Far 0 Base Address Register Enable Each BAR/Mask set has 1 enable bit



Bits	SCOM	Field Mnemonic: Description
1:19	RW	NX_PB_FORF0_MASK: pe bus Foreign Link Far 0 Base Address Register Mask This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 16 MB up to 8 TB. 16_MB=>0b00000000000000000000 32_MB=>0b00000000000000000001 64_MB=>0b00000000000000000011 128_MB=>0b00000000000000000111 256_MB=>0b00000000000000001111 512_MB=>0b00000000000000011111 1_GB=>0b00000000000001111111 2_GB=>0b00000000000011111111 4_GB=>0b00000000000111111111 8_GB=>0b00000000011111111111 16_GB=>0b00000000111111111111 32_GB=>0b00000001111111111111 64_GB=>0b00000011111111111111 128_GB=>0b00000111111111111111 256_GB=>0b00001111111111111111 512_GB=>0b00011111111111111111 1_TB=>0b00111111111111111111 2_TB=>0b01111111111111111111 4_TB=>0b11111111111111111111 8_TB=>0b11111111111111111111
20:45	RW	NX_PB_FORF0_BAR: pe bus Foreign Link Far 0 Base Address Register Bits 14 to 39 of the Foreign Link Far 0 Base Address range are specified with this IDial. Bits 14 to 39 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 39 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Foreign Link Far 0 address range specified by the BAR/Mask pair.
46:63	RO	Constant = 0b00000000000000000000

Register Name	FOREIGN_F BAR1 Range Register	
Mnemonic	EN.NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_FOREIGN_F_BAR1	
Address	000000000201309C (SCOM)	
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0	RW	NX_PB_FORF1_BAR_EN: PE bus Foreign Link Far 1 Base Address Register Enable Each BAR/Mask set has 1 enable bit

Bits	SCOM	Field Mnemonic: Description
1:19	RW	NX_PB_FORF1_MASK: pe bus Foreign Link Far 1 Base Address Register Mask This LDial specifies the size of the address range which is specified by this BAR/Mask pair. The range size must be a power of two. Valid range sizes go from 16 MB up to 8 TB. 16_MB=>0b00000000000000000000 32_MB=>0b00000000000000000001 64_MB=>0b00000000000000000011 128_MB=>0b00000000000000000111 256_MB=>0b00000000000000011111 512_MB=>0b00000000000000111111 1_GB=>0b00000000000001111111 2_GB=>0b00000000000011111111 4_GB=>0b00000000000111111111 8_GB=>0b00000000001111111111 16_GB=>0b00000000111111111111 32_GB=>0b00000001111111111111 64_GB=>0b00000011111111111111 128_GB=>0b00000111111111111111 256_GB=>0b00001111111111111111 512_GB=>0b00011111111111111111 1_TB=>0b00111111111111111111 2_TB=>0b01111111111111111111 4_TB=>0b11111111111111111111 8_TB=>0b11111111111111111111
20:45	RW	NX_PB_FORF1_BAR: pe bus Foreign Link Far 1 Base Address Register Bits 14 to 39 of the Foreign Link Far 1 Base Address range are specified with this IDial. Bits 14 to 39 of the incoming PCI address are compared with this Base Address after ANDing bits 14 to 39 of the corresponding Mask Register with each. If the compare is TRUE, the snoop address falls within the Foreign Link Far 1 address range specified by the BAR/Mask pair.
46:63	RO	Constant = 0b00000000000000000000

Register Name	<i>NX CQ Scale Value For Epsilon Counter</i>
Mnemonic	EN.NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_EPSILON_COUNTER_VALUE
Address	000000000201309D (SCOM)
Attributes	
Description	

[illegible]



Register Name		Processor Bus AS MMIO Base Address Register
Mnemonic		EN.NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_AS_MMIO_BAR
Address		000000000201309E (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:13	RO	Constant = 0b0000000000000000
14:51	RW	AS_MMIO_BAR: MMIO bar for AS
52	RW	AS_MMIO_BAR_ENABLE: Enable mmio for AS
53:55	RW	AS_MMIO_BAR_SIZE: MMIO bar size for AS AS_MMIO_SIZE_OF_256K=>0b000 AS_MMIO_SIZE_OF_512K=>0b001 AS_MMIO_SIZE_OF_1M=>0b010 AS_MMIO_SIZE_OF_2M=>0b011
56:63	RO	Constant = 0b00000000 AS_MMIO_SIZE_OF_256K=>0b000 AS_MMIO_SIZE_OF_512K=>0b001 AS_MMIO_SIZE_OF_1M=>0b010 AS_MMIO_SIZE_OF_2M=>0b011

Register Name		<i>NX_CXA FIR Register</i>		
Mnemonic		EN.NX.CXA.CXA_XPT.XPT_SCOMFIR.FIR_REG		
Address		0000000002013000 (SCOM) 0000000002013001 (SCOM1) 0000000002013002 (SCOM2)		
Attributes				
Description		Local FIR register for the CAPP		
Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	BAR_PE: Informational PE. Generic bucket for errors that are informational.
1	RWX	WOX_AND	WOX_OR	REGISTER_PE: System xstop PE. Generic bucket for errors that are system xstop.
2	RWX	WOX_AND	WOX_OR	MASTER_ARRAY_CE: Correctable error on Master array. Included uOP and cresp arrays
3	RWX	WOX_AND	WOX_OR	MASTER_ARRAY_UE: Uncorrectable error on Master array. Includes uOP and cresp arrays
4	RWX	WOX_AND	WOX_OR	TIMER_EXPIRED_RECOV_ERROR: Precise directory epoch timeout Coarse directory epoch timeout rtagPool epoxh data hang timeout Recovery sequencer hang detection
5	RWX	WOX_AND	WOX_OR	TIMER_EXPIRED_XSTOP_ERROR: Recovery sequencer hang detection
6	RWX	WOX_AND	WOX_OR	PSL_CMD_UE: XPT detected Uncorrectable Error on processor bus data determined to be a PSL command. The PSL command does not propagate past XPT.

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
7	RWX	WOX_AND	WOX_OR	PSL_CMD_SUE: XPT detected Special Uncorrectable Error on processor bus data determined to be a PSL command The PSL command does not propagate past XPT.
8	RWX	WOX_AND	WOX_OR	SNOOP_ARRAY_CE: Correctable error on Snooper array. Includes precise dir, coarse dir, and uOP
9	RWX	WOX_AND	WOX_OR	SNOOP_ARRAY_UE: Uncorrectable error on Snooper array. Includes precise dir, coarse dir, and uOP
10	RWX	WOX_AND	WOX_OR	RECOVERY_FAILED: CAPP recovery failed
11	RWX	WOX_AND	WOX_OR	ILLEGAL_LPC_BAR_ACCESS: Illegal LPC BAR Access. Error detected when a snooper or master write operation is attempted to the fine directories in lpc-only mode, or when the operation hits the LPC BAR region in lpc disjoint mode. Also will fire if a directory hit is found on a read operation within the LPC BAR range.
12	RWX	WOX_AND	WOX_OR	XPT_RECOVERABLE_ERROR: Recoverable errors detected in Transport
13	RWX	WOX_AND	WOX_OR	MASTER_RECOVERABLE_ERROR: Recoverable errors detected in Master
14	RWX	WOX_AND	WOX_OR	SNOOPER_RECOVERABLE_ERROR: Spare FIR bits allocated for future use
15	RWX	WOX_AND	WOX_OR	SECURE_SCOM_ERROR: Error detected in secure scom satellite
16	RWX	WOX_AND	WOX_OR	MASTER_SYS_XSTOP_ERROR: System checkstop errors detected in Master (invalid state, control checker)
17	RWX	WOX_AND	WOX_OR	SNOOPER_SYS_XSTOP_ERROR: System checkstop errors detected in Snooper (invalid state, control checker)
18	RWX	WOX_AND	WOX_OR	XPT_SYS_XSTOP_ERROR: System checkstop errors detected in Transport (invalid state, control checker)
19	RWX	WOX_AND	WOX_OR	MUOP_ERROR_1: Master uOP FIR 1
20	RWX	WOX_AND	WOX_OR	MUOP_ERROR_2: Master uOP FIR 2
21	RWX	WOX_AND	WOX_OR	MUOP_ERROR_3: Master uOP FIR 3
22	RWX	WOX_AND	WOX_OR	SUOP_ERROR_1: Snooper uOP FIR 1
23	RWX	WOX_AND	WOX_OR	SUOP_ERROR_2: Snooper uOP FIR 2
24	RWX	WOX_AND	WOX_OR	SUOP_ERROR_3: Snooper uOP FIR 3
25	RWX	WOX_AND	WOX_OR	POWERBUS_MISC_ERROR: Miscellaneous informational processor bus errors including Unsolicited processor bus data Unsolicited cResp
26	RWX	WOX_AND	WOX_OR	POWERBUS_INTERFACE_PE: Parity error on processor bus interface (address/aTag/tTaag/rTag APC, SNP TLBI)
27	RWX	WOX_AND	WOX_OR	POWERBUS_DATA_HANG_ERROR: Any processor bus data hang poll error
28	RWX	WOX_AND	WOX_OR	POWERBUS_HANG_ERROR: Any processor bus command hang error (domestic address range)
29	RWX	WOX_AND	WOX_OR	LD_CLASS_CMD_ADDR_ERR: Processor bus address error detected by APC on a load-class command
30	RWX	WOX_AND	WOX_OR	ST_CLASS_CMD_ADDR_ERR: Processor bus address error detected by APC on a store-class command
31	RWX	WOX_AND	WOX_OR	PHB_LINK_DOWN: PPHB0 or PHB1 interface has asserted linkdown



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
32	RWX	WOX_AND	WOX_OR	LD_CLASS_CMD_FOREIGN_LINK_FAIL: APC received ack_dead or ack_ed_dead from the foreign interface on a load-class command
33	RWX	WOX_AND	WOX_OR	FOREIGN_LINK_HANG_ERROR: Any processor bus command hang error (foreign address range)
34	RWX	WOX_AND	WOX_OR	XPT_POWERBUS_CE: CE on data received from the processor bus and destined for either XPT data array (and back to the processor bus) or PSL command or link delay response packet.
35	RWX	WOX_AND	WOX_OR	XPT_POWERBUS_UE: UE on data received from the processor bus and destined for XPT data array (and back to the processor bus) or link delay response packet.
36	RWX	WOX_AND	WOX_OR	XPT_POWERBUS_SUE: SUE on data received from the processor bus and destined for XPT data array (and back to the processor bus) or link delay response packet.
37	RWX	WOX_AND	WOX_OR	TLBI_TIMEOUT: TLBI Timeout error. TLBI needs re-IPL to recover
38	RWX	WOX_AND	WOX_OR	TLBI_SEQ_ERR: TLBI seq_err. TLBI needs re-IPL to recover
39	RWX	WOX_AND	WOX_OR	TLBI_BAD_OP_ERR: TLBI bad op error. TLBI needs re-IPL to recover
40	RWX	WOX_AND	WOX_OR	TLBI_SEQ_NUM_PARITY_ERR: Parity error detected on TLBI sequence number
41	RWX	WOX_AND	WOX_OR	ST_CLASS_CMD_FOREIGN_LINK_FAIL: APC received ack_dead or ack_ed_dead from the foreign interface on a store-class command
42	RWX	WOX_AND	WOX_OR	TIME_BASE_ERR: An error has occurred with timebase. This is an indication that the timebase value can no longer assumed to be correct.
43	RWX	WOX_AND	WOX_OR	TRANSPORT_INFORMATIONAL_ERR: Transport Informational Error
44	RWX	WOX_AND	WOX_OR	SPARE_2: Spare FIR bits allocated for future use
45	RWX	WOX_AND	WOX_OR	SPARE_3: Spare FIR bits allocated for future use
46	RWX	WOX_AND	WOX_OR	PSL_CREDIT_TIMEOUT: Ran out of data credits on a snooper fsm or message credits and hit the Epoch timeout while waiting for credit return from psl.
47	RWX	WOX_AND	WOX_OR	SCOM_ERR2: Local FIR Parity Error RAS duplicate
48	RWX	WOX_AND	WOX_OR	SCOM_ERR: Local FIR Parity Error of ACTION/MASK registers
49:63	RO	N/A	N/A	Constant = 0b0000000000000000

Register Name	NX_CXA FIR Mask Register			
Mnemonic	EN.NX.CXA.CXA_XPT.XPT_SCOMFIR.FIR_MASK_REG			
Address	0000000002013003 (SCOM) 0000000002013004 (SCOM1) 0000000002013005 (SCOM2)			
Attributes				
Description	Error mask register mask for corresponding bit in FIR (0) = corresponding FIR bit is not masked (1) = corresponding FIR bit is masked			

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	BAR_PE_MASK: Informational PE Mask. Generic bucket for errors that are informational

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
1	RW	WO_AND	WO_OR	REGISTER_PE_MASK: System xstop PE Mask. Generic bucket for errors that are system xstop.
2	RW	WO_AND	WO_OR	MASTER_ARRAY_CE_MASK: Correctable error on Master array. Includes uOP and cresp arrays Mask
3	RW	WO_AND	WO_OR	MASTER_ARRAY_UE_MASK: Uncorrectable error on Master array. Includes uOP and cresp arrays Mask
4	RW	WO_AND	WO_OR	TIMER_EXPIRED_RECOV_ERROR_MASK: Precise directory epoch timeout Mask Coarse directory epoch timeout Mask rtagPool epoxh data hang timeout Mask Recovery sequencer hang detection Mask
5	RW	WO_AND	WO_OR	TIMER_EXPIRED_XSTOP_ERROR_MASK: Recovery sequencer hang detection Mask
6	RW	WO_AND	WO_OR	PSL_CMD_UE_MASK: XPT detected Uncorrectable Error on PowerBus data determined to be a PSL command Mask The PSL command does not propagate past XPT.
7	RW	WO_AND	WO_OR	PSL_CMD_SUE_MASK: XPT detected Special Uncorrectable Error on processor bus data determined to be a PSL command Mask The PSL command does not propagate past XPT.
8	RW	WO_AND	WO_OR	SNOOP_ARRAY_CE_MASK: Correctable error on Snooper array. Includes precise dir, coarse dir, and uOP Mask
9	RW	WO_AND	WO_OR	SNOOP_ARRAY_UE_MASK: Uncorrectable error on Snooper array. Includes precise dir, coarse dir, and uOP Mask
10	RW	WO_AND	WO_OR	RECOVERY_FAILED_MASK: CAPP recovery failed Mask
11	RW	WO_AND	WO_OR	ILLEGAL_LPC_BAR_ACCESS_MASK: Illegal LPC BAR Access Mask. Error detected when a snooper or master write operation is attempted to the fine directories in lpc-only mode, or when the operation hits the LPC BAR region in lpc disjoint mode. Also will fire if a directory hit is found on a read operation within the LPC BAR range.
12	RW	WO_AND	WO_OR	XPT_RECOVERABLE_ERROR_MASK: Recoverable errors detected in xpt Mask
13	RW	WO_AND	WO_OR	MASTER_RECOVERABLE_ERROR_MASK: Recoverable errors detected in Master Mask
14	RW	WO_AND	WO_OR	SNOOPER_RECOVERABLE_ERROR_MASK: Spare FIR bits allocated for future use Mask
15	RW	WO_AND	WO_OR	SECURE_SCOM_ERROR_MASK: Error detected in secure scom satellite Mask
16	RW	WO_AND	WO_OR	MASTER_SYS_XSTOP_ERROR_MASK: System checkstop errors detected in Master (invalid state, control checker) Mask
17	RW	WO_AND	WO_OR	SNOOPER_SYS_XSTOP_ERROR_MASK: System checkstop errors detected in Snooper (invalid state, control checker) Mask
18	RW	WO_AND	WO_OR	XPT_SYS_XSTOP_ERROR_MASK: System checkstop errors detected in Transport (invalid state, control checker) Mask
19	RW	WO_AND	WO_OR	MUOP_ERROR_1_MASK: Master uOP FIR 1 Mask
20	RW	WO_AND	WO_OR	MUOP_ERROR_2_MASK: Master uOP FIR 2 Mask
21	RW	WO_AND	WO_OR	MUOP_ERROR_3_MASK: Master uOP FIR 3 Mask
22	RW	WO_AND	WO_OR	SUOP_ERROR_1_MASK: Snooper uOP FIR 1 Mask



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
23	RW	WO_AND	WO_OR	SUOP_ERROR_2_MASK: Snooper uOP FIR 2 Mask
24	RW	WO_AND	WO_OR	SUOP_ERROR_3_MASK: Snooper uOP FIR 3 Mask
25	RW	WO_AND	WO_OR	POWERBUS_MISC_ERROR_MASK: Miscellaneous informational processor bus errors Mask including Unsolicited processor bus data Unsolicited cResp
26	RW	WO_AND	WO_OR	POWERBUS_INTERFACE_PE_MASK: Parity error on processor bus interface (address/aTag/tTag/rTag APC, SNP TLBI) Mask
27	RW	WO_AND	WO_OR	POWERBUS_DATA_HANG_ERROR_MASK: Any processor bus data hang poll error Mask
28	RW	WO_AND	WO_OR	POWERBUS_HANG_ERROR_MASK: Any processor bus command hang error (domestic address range) mask
29	RW	WO_AND	WO_OR	LD_CLASS_CMD_ADDR_ERR_MASK: Processor bus address error detected by APC on a load-class command mask
30	RW	WO_AND	WO_OR	ST_CLASS_CMD_ADDR_ERR_MASK: Processor bus address error detected by APC on a store-class command mask
31	RW	WO_AND	WO_OR	PHB_LINK_DOWN_MASK: PPHB0 or PHB1 interface has asserted linkdown mask
32	RW	WO_AND	WO_OR	LD_CLASS_CMD_FOREIGN_LINK_FAIL_MASK: APC received ack_dead or ack_ed_dead from the foreign interface on a load-class command Mask
33	RW	WO_AND	WO_OR	FOREIGN_LINK_HANG_ERROR_MASK: Any processor bus command hang error (foreign address range) Mask
34	RW	WO_AND	WO_OR	XPT_POWERBUS_CE_MASK: CE on data received from the processor bus and destined for either XPT data array (and back to the processor bus) or PSL command or link delay response packet mask
35	RW	WO_AND	WO_OR	XPT_POWERBUS_UE_MASK: UE on data received from the processor bus and destined for XPT data array (and back to the processor bus) or link delay response packet Mask
36	RW	WO_AND	WO_OR	XPT_POWERBUS_SUE_MASK: SUE on data received from the processor bus and destined for XPT data array (and back to the processor bus) or link delay response packet Mask
37	RW	WO_AND	WO_OR	TLBI_TIMEOUT_MASK: TLBI Timeout error. TLBI needs re-IPL to recover Mask
38	RW	WO_AND	WO_OR	TLBI_SEQ_ERR_MASK: TLBI seq_err. TLBI needs re-IPL to recover Mask
39	RW	WO_AND	WO_OR	TLBI_BAD_OP_ERR_MASK: TLBI bad op error. TLBI needs re-IPL to recover Mask
40	RW	WO_AND	WO_OR	TLBI_SEQ_NUM_PARITY_ERR_MASK: Parity error detected on TLBI sequence number Mask
41	RW	WO_AND	WO_OR	ST_CLASS_CMD_FOREIGN_LINK_FAIL_MASK: APC received ack_dead or ack_ed_dead from the foreign interface on a store-class command Mask
42	RW	WO_AND	WO_OR	TIME_BASE_ERR_MASK: An error has occurred with timebase. This is an indication that the timebase value can no longer assumed to be correct.
43	RW	WO_AND	WO_OR	TRANSPORT_INFORMATIONAL_ERR_MASK: Transport Informational Error Mask
44	RW	WO_AND	WO_OR	SPARE_2_MASK: Spare FIR bits allocated for future use Mask
45	RW	WO_AND	WO_OR	SPARE_3_MASK: Spare FIR bits allocated for future use Mask

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
46	RW	WO_AND	WO_OR	PSL_CREDIT_TIMEOUT_MASK: Ran out of data credits on a snoop fsm or message credits and hit the Epoch timeout while waiting for credit return from psl Mask
47	RW	WO_AND	WO_OR	SCOM_ERR2_MASK: Local FIR Parity Error RAS duplicate Mask
48	RW	WO_AND	WO_OR	SCOM_ERR_MASK: Local FIR Parity Error of ACTION/MASK registers Mask
49:63	RO	N/A	N/A	Constant = 0b0000000000000000

Register Name		<i>Pervasive FIR Action 0 Register</i>
Mnemonic		EN.NX.CXA.CXA_XPT.XPT_SCOMFIR.FIR_ACTION0_REG
Address		0000000002013006 (SCOM)
Attributes		
Description		Action Select for the FIR bits
Bits	SCOM	Field Mnemonic: Description
0:48	RO	FIR_ACTION0: MSB of action select for corresponding bit in FIR (Action0,Action1) = Action Select (0,0) = Platform Checkstop (0,1) = Recovered Attention (1,0) = Masked (recov_int FIR output not connected) (1,1) = CAPP Machine Check

Register Name		<i>Pervasive FIR Action 1 Register</i>
Mnemonic		EN.NX.CXA.CXA_XPT.XPT_SCOMFIR.FIR_ACTION1_REG
Address		0000000002013007 (SCOM)
Attributes		
Description		Second bit of action select if necessary
Bits	SCOM	Field Mnemonic: Description
0:48	RO	FIR_ACTION1: LSB of action select for corresponding bit in FIR (Action0,Action1) = Action Select (0,0) = Platform Checkstop (0,1) = Recovered Attention (1,0) = Masked (recov_int FIR output not connected) (1,1) = CAPP Machine Check

Register Name		<i>Snoop Error Report Register - SCOM Access Of Snp C_err_rpt Latches</i>
Mnemonic		EN.NX.CXA.CXA_SNPFE.SNP_REGS.CXA_SNP_ERROR_REPORT_REG
Address		000000000201300A (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:31	ROX	CXA_SNP_C_ERR_RPT_HOLD_DATA: SNP c_err_report_hold value.
32:63	RO	Constant = 0b00000000000000000000000000000000



Register Name		<i>APC Master Error Report Reg</i>
Mnemonic		EN.NX.CXA.CXA_APC1.ERRRPT
Address		000000000201300B (SCOM)
Attributes		
Description		output of APC cerr_rpt hold latches.
Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is apc_collision)
1	ROX	Reserved field. (Access type is fsm_sm_error)
2	ROX	Reserved field. (Access type is rbufsm_error)
3	ROX	Reserved field. (Access type is wbuf_sm_error)
4	ROX	Reserved field. (Access type is perr_bar_reg)
5	ROX	Reserved field. (Access type is perr_nonbar_reg)
6	ROX	Reserved field. (Access type is rtag_hang_epoch)
7	ROX	Reserved field. (Access type is crsp0_regs_ce_err)
8	ROX	Reserved field. (Access type is crsp1_regs_ce_err)
9	ROX	Reserved field. (Access type is uop_regs_ce_err)
10	ROX	Reserved field. (Access type is crsp0_regs_ue_err)
11	ROX	Reserved field. (Access type is crsp1_regs_ue_err)
12	ROX	Reserved field. (Access type is uop_regs_ue_err)
13	ROX	Reserved field. (Access type is crsp0_regs_atag_perr)
14	ROX	Reserved field. (Access type is crsp0_regs_ttag_perr)
15	ROX	Reserved field. (Access type is crsp1_regs_atag_perr)
16	ROX	Reserved field. (Access type is crsp1_regs_ttag_perr)
17	ROX	Reserved field. (Access type is fir_action1)
18	ROX	Reserved field. (Access type is fir_action2)
19	ROX	Reserved field. (Access type is fir_action3)
20	ROX	Reserved field. (Access type is unexpected_cresp)
21	ROX	Reserved field. (Access type is Id_class_are_error)
22	ROX	Reserved field. (Access type is st_class_are_error)
23	ROX	Reserved field. (Access type is Id_class_ack_dead)
24	ROX	Reserved field. (Access type is foreign_op_hang)
25	ROX	Reserved field. (Access type is domestic_op_hang)
26	ROX	Reserved field. (Access type is st_class_ack_dead)
27	ROX	Reserved field. (Access type is activate_fsmerr)
28	ROX	Reserved field. (Access type is spare1)
29	ROX	Reserved field. (Access type is spare2)
30:63	RO	Constant = 0b00000000000000000000000000000000

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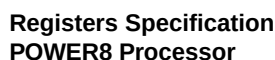
Register Name		<i>Transport Error Hold Register</i>
Mnemonic		EN.NX.CXA.XPT_ERROR_REPORT
Address		000000000201300C (SCOM)
Attributes		
Description		The XPT Error Report Register contains hold latches for the conditions that result in FIR errors.
Bits	SCOM	Field Mnemonic: Description
0	ROX	XPT_PSL_CMD_UE_ERRHOLD: PSL Command Uncorrectable Error
1	ROX	XPT_PSL_CMD_SUE_ERRHOLD: PSL Command Special Uncorrectable Error
2	ROX	XPT_SC_RDATA_PARITY_ERRHOLD: EPT Register Read Data Parity Error
3	ROX	APC_SC_RDATA_PARITY_ERRHOLD: APC Register Read Data Parity Error
4	ROX	SN_SC_RDATA_PARITY_ERRHOLD: Snoop Register Read Data Parity Error
5	ROX	NX_DATA_RTAG_PARITY_ERRHOLD: Processor Bus RTAG Parity Error
6	ROX	NXPBXPT_PBRCV_ECC_CE_ERRHOLD: Processor Bus Data or PSL Command Correctable Error
7	ROX	NXPBXPT_PBRCV_ECC_UE_ERRHOLD: Processor Bus Data Uncorrectable Error
8	ROX	NXPBXPT_PBRCV_ECC_SUE_ERRHOLD: Processor Bus Data Special Uncorrectable Error
9	ROX	XPT_DBG_CTL_REG_PARITY_ERRHOLD: Debug Bus Mux Control Register Write Data Parity Error
10	ROX	XPT_CFG_REG_PARITY_ERRHOLD: Transport Control Register Write Data Parity Error
11	ROX	CAPP_ERR_STAT_CTL_REG_PARITY_ERRHOLD: CAPP Error Status and Control Register Write Data Parity Error
12	ROX	PMU_CNTRA_CFG_REG_PARITY_ERRHOLD: PMU Counter Configuration Register0 Write Data Parity Error
13	ROX	PMU_CNTRB_CFG_REG_PARITY_ERRHOLD: PMU Counter Configuration Register1 Write Data Parity Error
14	ROX	XPT_PMU_EVENT_SEL_REG_PARITY_ERRHOLD: XPT PMU Event Select Register Write Data Parity Error
15	ROX	PE0_CXA_LINKDOWN_ERRHOLD: PE0 Link Down
16	ROX	PE1_CXA_LINKDOWN_ERRHOLD: PE1 Link Down
17	ROX	SB_SCOM_ERRHOLD: Secure SCOM Internal Error
18	ROX	PBXMIT_MSGQ_SEQ_ERRHOLD: Transport Message Queue Sequencer Not One Hot Error
19	ROX	PBXMIT_DXMIT_SEQ_ERRHOLD: Transport Transmit Queue Sequencer Not One Hot Error
20	ROX	EPH_REC_TMR_CNTL_REG_PARITY_ERRHOLD: Epoch and Recovery Timers Control Register Write Data Parity Error
21	ROX	RCS_RECOVERY_FAILED_ERRHOLD: CAPP recovery failed
22	ROX	RCS_STATE_MACHINE_ERRHOLD: Recovery sequencer FSM invalid state
23	ROX	NXPBXPT_PBRCV_LNK_RSP_ECC_UE_ERRHOLD: Secure Link Response Packet UE
24	ROX	NXPBXPT_PBRCV_LNK_RSP_ECC_SUE_ERRHOLD: Secure Link Response Packet SUE
25	ROX	LNK_RSP_PKT_DISCARDED_ERRHOLD: Secure Link Response Packet discarded
26	ROX	SECURE_LNK_RSP_PKT_NOT_VALID_ERRHOLD: Secure Link Response Packet not valid
27	ROX	SECURE_LNK_SCOM_CONFLICT_ERRHOLD: Secure Link Response Packet conflict with scom access
28	ROX	UNSOLICITED_DATA_RCV_ERROR_ERRHOLD: Unsolicited Data Received
29	ROX	AS_RCMD0_PARITY_ERR_ERRHOLD: AS as Endpoint rcmd0 Parity Error
30	ROX	AS_REGS_PARITY_ERR_ERRHOLD: AS as Endpoint Register Parity Error



Bits	SCOM	Field Mnemonic: Description
31	ROX	AS_SM_ERROR_ERRHOLD: AS as Endpoint State Machine Error
32	ROX	AS_REG_RDATA_PERR_ERRHOLD: AS as Endpoint Register Read Data Parity Error
33	ROX	DFS_SM_ERROR_ERRHOLD: DFS State Machine Error
34	ROX	TB_XPT_ERROR_FIR_ERR_ERRHOLD: Time Base Error
35	ROX	TB_CMD_DISCARDED_ERRHOLD: Time Base Command Discarded
36	ROX	TB_REG_RDATA_PERR_ERRHOLD: Time Base Command Discarded
37	ROX	RNG_WR_ENBL_REG_PERR_ERRHOLD: RNG Write Enable Configuration Register Parity Error
38	ROX	RCS_RECOVERY_TIMEOUT_ERRHOLD: CAPP Recovery timeout
39	ROX	TBST0_BADIN_ERRHOLD: Timebase state machine in State 0 and SCOM tfmr write of bit (18) move_chip_tod_to_tb
40	ROX	TBST6_BADIN_ERRHOLD: Timebase state machine in State 6 and SCOM tfmr write of 1 bit (18) move_chip_tod_to_tb
41	ROX	TBST7_BADIN_ERRHOLD: Timebase state machine in State 7 and SCOM tfmr write of 1 bit (16) load_tod_mod or (18) move_chip_tod_to_tb
42	ROX	TWO_TFMRMDS_ERR_ERRHOLD: SCOM tfmr write of 1 to both bits (16) load_tod_mod and bit (18) move_chip_tod_to_tb
43	ROX	TB_MISSING_SYNC_ERRHOLD: Indicates a sync pulse was not received in the time specified by the sync_bit_sel control bits
44	ROX	TB_MISSING_STEP_ERRHOLD: Indicates that a step pulse was not received in the time specified by the max_cyc_bet_steps control bits
45	ROX	TB_RESIDUE_ERR_ERRHOLD: Indicates a parity or residue error has compromised the integrity of the TimeBase
46	ROX	TX_TFMR_CORRUPT_ERRHOLD: Indicates a parity error has been detected on the TFMR register
47	ROX	TBST_CORRUPT_ERRHOLD: Indicates a TFMR invalid TB state machine state
48	ROX	TBST9_BADIN_ERRHOLD: Timebase state machine in State 9 and SCOM tfmr write of 1 bit (16) load_tod_mod or (18) move_chip_tod_to_tb
49:63	RO	Constant = 0b0000000000000000

Register Name	TLBI Error Hold Register
Mnemonic	EN.NX.CXA.CXA_XPT.XPT_SCOMFIR.TLBI_ERROR_REPORT
Address	00000000201300D (SCOM)
Attributes	
Description	The TLBI Error Report Register contains hold latches for the conditions that result in FIR errors.

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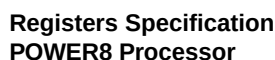
Bits	SCOM	Field Mnemonic: Description
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	Error Inject Register
Mnemonic	EN.NX.CXA.APC_ERRINJ
Address	0000000002013010 (SCOM)
Attributes	
Description	Error Inject Register controls error injection.

Bits	SCOM	Field Mnemonic: Description
0	RW	APC_ERRINJ_ENABLE: APC Master Error Inject Enable
1	RW	APC_ERRINJ_DBLERR: APC Master 0=inject 1 bit ECC error, 1=inject 2 bit ECC error
2	RW	APC_ERRINJ_CONTINUOUS: APC Master 0= inject error once, 1=inject error continuously
3:7	RO	Constant = 0b000000
8:11	RW	APC_ERRINJ_TARGET: APC Master error inject target selection
12	RW	SNP_ERROR_INJECT_ENABLE: SNP Master Error Inject Enable
13	RW	SNP_INJECT_DBL_ECC_ERROR: SNP Master 0=inject 1 bit ECC error, 1=inject 2 bit ECC error
14	RW	SNP_INJECT_CONTINUOUS_ERROR: SNP Master 0= inject error once, 1=inject error continuously
15:16	RO	Constant = 0b00
17:23	RW	SNP_ERROR_INJECT_TARGET: SNP Master error inject target selection
24:31	RO	Constant = 0b00000000
32	RW	XPT_ERROR_INJECT_ENABLE: XPT Master Error Inject Enable
33:34	RW	XPT_ERROR_TYPE: XPT Error Type 00=inject CE, 01=inject UE, 10=inject SUE, 11=reserved
35	RW	XPT_INJECT_CONTINUOUS_ERROR: XPT Continuous Mode 1=continuously inject the error, 0=inject on the next operation
36:39	RW	XPT_ERROR_INJECT_TARGET: XPT Error Inject Target 0000=write buffer array 0, 0001=write buffer array 1, 0010-1111=reserved
40:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	CAPP Epoch And Recovery Timers Control Register
Mnemonic	EN.NX.CXA.CXA_XPT.XPT_EPT.CAPP_EPOCH_AND_RECOVERY_TMR_CONTROL
Address	000000000201302C (SCOM)
Attributes	
Description	The Epoch and Recovery Timers Control Register contains the enables and period controls for the Epoch and Recovery Timers.

Bits	SCOM	Field Mnemonic: Description
0	RW	EPOCH_TIMER_ENABLE: When = 1 the Epoch Timer is enabled; otherwise it is disabled.
1	RW	RECOVERY_TIMER_ENABLE: When = 1 the recovery Timer is enabled; otherwise it is disabled.
2:31	RO	Constant = 0b00000000000000000000000000000000





Register Name		Processor Bus Debug Control Register 1
Mnemonic		EN.NX.PBI.CQ_WRAP.NXCQ_SCOM.NX_PB_DEBUG_REG
Address		0000000002013090 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:7	RW	NXCQ_TRACE_CNTL: 0 - 0= trace cq shim i/f; 1= trace queues 1:2 - reserved 3 - trace a fixed queue number when tracing queues 4:7 - queue number when tracing a fixed queue
8:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name		NX Snapshot Of Debug Bus Bits 0 - 63
Mnemonic		EN.NX.PBI.CQ_WRAP.NX_DEBUG_SNAPSHOT_0
Address		00000000020130A4 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:63	ROX	NX_DEBUG_SNAPSHOT_B0_63: NX Snapshot of Debug Bus bits 0 to 63

Register Name		NX Snapshot Of Debug Bus Bits 64 - 87
Mnemonic		EN.NX.PBI.CQ_WRAP.NX_DEBUG_SNAPSHOT_1
Address		00000000020130A5 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:23	ROX	NX_DEBUG_SNAPSHOT_B64_87: NX Snapshot of Debug Bus bits 64 to 87
24:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name		DMA And Engine Fault Isolation Register		
Mnemonic		EN.NX.DBG.NX_DMA_ENG_FIR		
Address		0000000002013100 (SCOM) 0000000002013101 (SCOM1) 0000000002013102 (SCOM2)		
Attributes				
Description		DMA and Engine Fault Isolation Register		
Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	RESERVED_00_FIR: Reserved FIR bit 0.
1	RWX	WOX_AND	WOX_OR	ICS_INVALID_STATE_FIR: ICS invalid state error FIR bit
2	RWX	WOX_AND	WOX_OR	RESERVED_02_FIR: Reserved FIR bit 2.
3	RWX	WOX_AND	WOX_OR	RESERVED_03_FIR: Reserved FIR bit 3.
4	RWX	WOX_AND	WOX_OR	CH0_842_ECC_CE_FIR: Channel 0 842 array corrected ECC error FIR bit

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
5	RWX	WOX_AND	WOX_OR	CH0_842_ECC_UE_FIR: Channel 0 842 array uncorrectable ECC error FIR bit
6	RWX	WOX_AND	WOX_OR	CH1_842_ECC_CE_FIR: Channel 1 842 array corrected ECC error FIR bit
7	RWX	WOX_AND	WOX_OR	CH1_842_ECC_UE_FIR: Channel 1 842 array uncorrectable ECC error FIR bit
8	RWX	WOX_AND	WOX_OR	NONZERO_CSB_CC_FIR: DMA non-zero CSB CC detected FIR bit. Programming error.
9	RWX	WOX_AND	WOX_OR	DMA_ECC_CE_FIR: DMA array correctable ECC error FIR bit
10	RWX	WOX_AND	WOX_OR	DMA_OUTWR_INRD_ECC_CE_FIR: DMA outbound write/inbound read correctable ECC error FIR bit
11	RWX	WOX_AND	WOX_OR	CH5_AMF_ECC_CE_FIR: Channel 5 AMF array corrected ECC error FIR bit
12	RWX	WOX_AND	WOX_OR	CH6_AMF_ECC_CE_FIR: Channel 6 AMF array corrected ECC error FIR bit
13	RWX	WOX_AND	WOX_OR	CH7_AMF_ECC_CE_FIR: Channel 7 AMF array corrected ECC error FIR bit
14	RWX	WOX_AND	WOX_OR	OTHER_SCOM_SAT_FIR: Error from other SCOM satellites FIR bit
15	RWX	WOX_AND	WOX_OR	DMA_INVALID_STATE_RECOV_FIR: DMA invalid state error FIR bit. Unrecoverable despite name
16	RWX	WOX_AND	WOX_OR	DMA_INVALID_STATE_UNRECOV_FIR: DMA invalid state error FIR bit
17	RWX	WOX_AND	WOX_OR	DMA_ECC_UE_FIR: DMA array uncorrectable ECC error FIR bit
18	RWX	WOX_AND	WOX_OR	DMA_OUTWR_INRD_ECC_UE_FIR: DMA outbound write/inbound read uncorrectable ECC error FIR bit
19	RWX	WOX_AND	WOX_OR	DMA_INRD_DONE_ERR_FIR: DMA inbound read error FIR bit
20	RWX	WOX_AND	WOX_OR	CH0_INVALID_STATE_FIR: Channel 0 invalid state error FIR bit
21	RWX	WOX_AND	WOX_OR	CH1_INVALID_STATE_FIR: Channel 1 invalid state error FIR bit
22	RWX	WOX_AND	WOX_OR	CH2_INVALID_STATE_FIR: Channel 2 invalid state error FIR bit
23	RWX	WOX_AND	WOX_OR	CH3_INVALID_STATE_FIR: Channel 3 invalid state error FIR bit
24	RWX	WOX_AND	WOX_OR	CH4_INVALID_STATE_FIR: Channel 4 invalid state error FIR bit
25	RWX	WOX_AND	WOX_OR	CH5_INVALID_STATE_FIR: Channel 5 invalid state error FIR bit
26	RWX	WOX_AND	WOX_OR	CH6_INVALID_STATE_FIR: Channel 6 invalid state error FIR bit
27	RWX	WOX_AND	WOX_OR	CH7_INVALID_STATE_FIR: Channel 7 invalid state error FIR bit
28	RWX	WOX_AND	WOX_OR	CH5_AMF_ECC_UE_FIR: Channel 5 AMF array uncorrectable ECC error FIR bit
29	RWX	WOX_AND	WOX_OR	CH6_AMF_ECC_UE_FIR: Channel 6 AMF array uncorrectable ECC error FIR bit
30	RWX	WOX_AND	WOX_OR	CH7_AMF_ECC_UE_FIR: Channel 7 AMF array uncorrectable ECC error FIR bit
31	RWX	WOX_AND	WOX_OR	CRB_ECC_UE_FIR: UE error on CRB(CSB address, CCB) FIR bit
32	RWX	WOX_AND	WOX_OR	CRB_ECC_SUE_FIR: SUE error on CRB(CSB address, CCB) FIR bit
33	RWX	WOX_AND	WOX_OR	DMA_OUTWR_INRD_ECC_SUE_FIR: SUE error on something other than CRB(CSB address, CCB) FIR bit
34	RWX	WOX_AND	WOX_OR	RESERVED_34_FIR: Reserved FIR bit 34
35	RWX	WOX_AND	WOX_OR	RESERVED_35_FIR: Reserved FIR bit 35

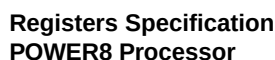


Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
36	RWX	WOX_AND	WOX_OR	CH4_AMF_ECC_CE_FIR: Channel 4 AMF array corrected ECC error FIR bit
37	RWX	WOX_AND	WOX_OR	CH4_AMF_ECC_UE_FIR: Channel 4 AMF array uncorrectable ECC error FIR bit
38	RWX	WOX_AND	WOX_OR	RESERVED_38_FIR: Reserved FIR bit 38
39	RWX	WOX_AND	WOX_OR	RESERVED_39_FIR: Reserved FIR bit 39
40	RWX	WOX_AND	WOX_OR	RESERVED_40_FIR: Reserved FIR bit 40
41	RWX	WOX_AND	WOX_OR	RESERVED_41_FIR: Reserved FIR bit 41
42	RWX	WOX_AND	WOX_OR	RESERVED_42_FIR: Reserved FIR bit 42
43	RWX	WOX_AND	WOX_OR	RESERVED_43_FIR: Reserved FIR bit 43
44	RWX	WOX_AND	WOX_OR	RESERVED_44_FIR: Reserved FIR bit 44
45	RWX	WOX_AND	WOX_OR	RESERVED_45_FIR: Reserved FIR bit 45
46	RWX	WOX_AND	WOX_OR	RESERVED_46_FIR: Reserved FIR bit 46
47	RWX	WOX_AND	WOX_OR	RESERVED_47_FIR: Reserved FIR bit 47
48	RWX	WOX_AND	WOX_OR	FIR_SCOM_PE_FIR: FIR/SCOM satellite parity error FIR bit
49	RWX	WOX_AND	WOX_OR	FIR_SCOM_PE_DUP_FIR: FIR/SCOM satellite parity error FIR bit duplicate
50:63	RO	N/A	N/A	Constant = 0b0000000000000000

Register Name		DMA And Engine FIR Mask Register		
Mnemonic		EN.NX.DBG.NX_DMA_ENG_FIR_MASK		
Address		0000000002013103 (SCOM) 0000000002013104 (SCOM1) 0000000002013105 (SCOM2)		
Attributes				
Description				

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:49	RW	WO_AND	WO_OR	NX_DMA_ENG_FIR_MASK_00_36: DMA and Engine FIR Mask Register
50:63	RO	N/A	N/A	Constant = 0b00000000000000

Register Name		<i>Debug Mux Control Register</i>
Mnemonic		EN.NX.DBG.NX_DEBUGMUX_CTRL
Address		00000000201310A (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:46	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000
47:63	RW	NX_DEBUGMUX_CTRL_47_63: NX Debug Bus Selects

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:19	RW	WO_AND	WO_OR	NX_CQ_FIR_MASK:

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Register Name	<i>NX_AS FIR Register</i>
Mnemonic	EN.NX.AS.FIR_REG
Address	00000000020130C0 (SCOM) 00000000020130C1 (SCOM1) 00000000020130C2 (SCOM2)
Attributes	
Description	Local FIR register for the Accelerator Switchboard

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	SND_ARY_UE: Send Array Uncorrectable ECC Error
1	RWX	WOX_AND	WOX_OR	MMIO_DAT_UE: MMIO Store Data Uncorrectable ECC Error
2	RWX	WOX_AND	WOX_OR	COPREQ_DAT_UE: Copreq Data Uncorrectable ECC Error
3	RWX	WOX_AND	WOX_OR	PBCQ_Q_INFO_PE: MMIO Operation Info Parity Error
4	RWX	WOX_AND	WOX_OR	RCMD0_ADDR_PE: Reflected Command 0 Address Parity Error
5	RWX	WOX_AND	WOX_OR	RCMD0_TTAG_PE: Reflected Command 0 TTag Parity Error
6	RWX	WOX_AND	WOX_OR	RCMD1_ADDR_PE: Reflected Command 1 Address Parity Error
7	RWX	WOX_AND	WOX_OR	RCMD1_TTAG_PE: Reflected Command 1 TTag Parity Error
8	RWX	WOX_AND	WOX_OR	MAL_FMD_MMIO_ST: Malformed MMIO Store Error
9	RWX	WOX_AND	WOX_OR	DATA_HANG: Data Hang Error
10	RWX	WOX_AND	WOX_OR	INVLD_NDOT_ERR: Invalid use of non-dot PBT Error
11	RWX	WOX_AND	WOX_OR	CMPL_CNT_ERR: Completion Count Error
12	RWX	WOX_AND	WOX_OR	MULT_CAM_HIT_ERR: Multiple CAM Hits Error
13	RWX	WOX_AND	WOX_OR	PFIFO_RTY_ERR: Hypervisor FIFO Retry Error
14	RWX	WOX_AND	WOX_OR	FL_FIFO_OVFLW: Foreign Link Outbound FIFO Overflow
15	RWX	WOX_AND	WOX_OR	EG_CMD_OVFLW: EG Overflow Error
16	RWX	WOX_AND	WOX_OR	DISABLED_EG_ERR: Cmd uses disabled EG Error
17	RWX	WOX_AND	WOX_OR	INVLD_RWIN_ERR: Invalid Receive Window Used Error
18	RWX	WOX_AND	WOX_OR	CW_UNEXPECTED_CRSP_ERR: Unexpected cresp detected by Credit write error
19	RWX	WOX_AND	WOX_OR	IMPL_DMA_ERR: Implied DMA Error
20	RWX	WOX_AND	WOX_OR	SHIFT_MODE_ERR: Implied DMA Error
21	RWX	WOX_AND	WOX_OR	CR0_ATAG_PE: cResp0 Atag Parity Error
22	RWX	WOX_AND	WOX_OR	CR0_TTAG_PE: cResp0 Atag Parity Error
23	RWX	WOX_AND	WOX_OR	CR1_ATAG_PE: cResp1 Atag Parity Error
24	RWX	WOX_AND	WOX_OR	CR1_TTAG_PE: cResp1 Atag Parity Error
25	RWX	WOX_AND	WOX_OR	CREDWT_RTY_ERR: Unexpected or Unsupported Retry on Credit Write
26	RWX	WOX_AND	WOX_OR	CW_ADR_ERR: Credit Write Address Error
27	RWX	WOX_AND	WOX_OR	NTFY_UNEXPECTED_CRSP_ERR: Unexpected cresp on Notify error
28	RWX	WOX_AND	WOX_OR	RCV_TAB_UE: Receive Table Ucorrectable ECC Error

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
29	RWX	WOX_AND	WOX_OR	MMIO_CR_DARY_UE: MMIO Copreq Data Array Uncorrectable ECC Error
30	RWX	WOX_AND	WOX_OR	AS_EG_CE: Correctable Error in AS_EG
31	RWX	WOX_AND	WOX_OR	EG_SCOM_ERR: AS_EG Scom Error
32	RWX	WOX_AND	WOX_OR	PM_WRITE_ERR: Page Migration Register Write Error
33	RWX	WOX_AND	WOX_OR	EG_RSVD_2_ERR: Reserved Error
34	RWX	WOX_AND	WOX_OR	DSLC_INTF_PE: DSLC Interface Parity Error
35	RWX	WOX_AND	WOX_OR	AS_IN_CE: Correctable Error in AS_IN
36	RWX	WOX_AND	WOX_OR	AS_IN_UNSUP_CFG: AS_IN detected unsupported config
37	RWX	WOX_AND	WOX_OR	COPREQ_CRESP_ERR: Copreq Cresp Error
38	RWX	WOX_AND	WOX_OR	CREDWT_CRESP_ERR: Credwt Cresp Error
39	RWX	WOX_AND	WOX_OR	DSLC_CFG_ERR: DSLC Config Error
40	RWX	WOX_AND	WOX_OR	EG_RSVD_3_ERR: Reserved Error
41	RWX	WOX_AND	WOX_OR	SCOM_ERR: Scom Error
42	RWX	WOX_AND	WOX_OR	SCOM_ERR_DUP: Scom Error

Register Name	AS_IN FIR Mask Register
Mnemonic	EN.NX.AS.FIR_MASK_REG
Address	00000000020130C3 (SCOM) 00000000020130C4 (SCOM1) 00000000020130C5 (SCOM2)
Attributes	
Description	Error mask register (Action0, Mask) = Action Select (0,0) = Recoverable Error (0,1) = Masked (1,x) = Checkstop Error

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	SND_ARY_UE_MASK: Send Array Uncorrectable ECC Error Mask
1	RW	WO_AND	WO_OR	MMIO_DAT_UE_MASK: MMIO Store Data Uncorrectable ECC Error Mask
2	RW	WO_AND	WO_OR	COPREQ_DAT_UE_MASK: Copreq Data Uncorrectable ECC Error Mask
3	RW	WO_AND	WO_OR	PBCQ_Q_INFO_PE_MASK: MMIO Operation Info Parity Error Mask
4	RW	WO_AND	WO_OR	RCMD0_ADDR_PE_MASK: Reflected Command 0 Address Parity Error Mask
5	RW	WO_AND	WO_OR	RCMD0_TTAG_PE_MASK: Reflected Command 0 TTag Parity Error Mask
6	RW	WO_AND	WO_OR	RCMD1_ADDR_PE_MASK: Reflected Command 1 Address Parity Error Mask
7	RW	WO_AND	WO_OR	RCMD1_TTAG_PE_MASK: Reflected Command 1 TTag Parity Error Mask
8	RW	WO_AND	WO_OR	MAL_FMD_MMIO_ST_MASK: Malformed MMIO Store Error Mask
9	RW	WO_AND	WO_OR	DATA_HANG_MASK: Data Hang Error Mask
10	RW	WO_AND	WO_OR	INVLD_NDOT_ERR_MASK: Invalid use of non-dot PBT Error Mask
11	RW	WO_AND	WO_OR	CMPL_CNT_ERR_MASK: Completion Count Error Mask
12	RW	WO_AND	WO_OR	MULT_CAM_HIT_ERR_MASK: Multiple CAM Hit Error Mask



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
13	RW	WO_AND	WO_OR	PFIFO_RTY_ERR_MASK: Hypervisor FIFO Retry Error Mask
14	RW	WO_AND	WO_OR	FL_FIFO_OVFLW_MASK: Foreign Link Outbound FIFO Overflow Mask
15	RW	WO_AND	WO_OR	EG_CMD_OVFLW_MASK: EG Overflow Error Mask
16	RW	WO_AND	WO_OR	DISABLED_EG_ERR_MASK: Cmd uses disabled EG Error Mask
17	RW	WO_AND	WO_OR	INVLD_RWIN_ERR_MASK: Invalid Receive Window Used Error Mask
18	RW	WO_AND	WO_OR	CW_UNEXPECTED_CRSP_ERR_MASK: Unexpected cresp detected by Credit write error Mask
19	RW	WO_AND	WO_OR	IMPL_DMA_ERR_MASK: Implied DMA Error Mask
20	RW	WO_AND	WO_OR	SHIFT_MODE_ERR_MASK: Implied DMA Error Mask
21	RW	WO_AND	WO_OR	CR0_ATAG_PE_MASK: cResp0 Atag Parity Error Mask
22	RW	WO_AND	WO_OR	CR0_TTAG_PE_MASK: cResp0 Atag Parity Error Mask
23	RW	WO_AND	WO_OR	CR1_ATAG_PE_MASK: cResp1 Atag Parity Error Mask
24	RW	WO_AND	WO_OR	CR1_TTAG_PE_MASK: cResp1 Atag Parity Error Mask
25	RW	WO_AND	WO_OR	CREDWT_RTY_ERR_MASK: Unexpected or Unsupported Retry on Credit Write Mask
26	RW	WO_AND	WO_OR	CW_ADR_ERR_MASK: Credit Write Address Error Mask
27	RW	WO_AND	WO_OR	NTFY_UNEXPECTED_CRSP_ERR_MASK: Unexpected crsp on Notify error Mask
28	RW	WO_AND	WO_OR	RCV_TAB_UE_MASK: Receive Table Ucorrectable ECC Error Mask
29	RW	WO_AND	WO_OR	MMIO_CR_DARY_UE_MASK: MMIO Copreq Data Array Ucorrectable ECC Error Mask
30	RW	WO_AND	WO_OR	AS_EG_CE_MASK: Correctable Error in AS_EG mask
31	RW	WO_AND	WO_OR	EG_SCOM_ERR_MASK: AS_EG Scom Error Mask
32	RW	WO_AND	WO_OR	PM_WRITE_ERR_MASK: Page Migration Register Write Error Mask
33	RW	WO_AND	WO_OR	EG_RSVD_2_ERR_MASK: Reserved Error Mask
34	RW	WO_AND	WO_OR	DSLC_INTF_PE_MASK: DSLC Interface Parity Error Mask
35	RW	WO_AND	WO_OR	AS_IN_CE_MASK: Correctable Error in AS_IN mask
36	RW	WO_AND	WO_OR	AS_IN_UNSUP_CFG_MASK: AS_IN detected unsupported config mask
37	RW	WO_AND	WO_OR	COPREQ_CRESP_ERR_MASK: Copreq Cresp Error mask
38	RW	WO_AND	WO_OR	CREDWT_CRESP_ERR_MASK: Credwt Cresp Error mask
39	RW	WO_AND	WO_OR	DSLC_CFG_ERR_MASK: DSLC Config Error
40	RW	WO_AND	WO_OR	EG_RSVD_3_ERR_MASK: Reserved Error Mask
41	RW	WO_AND	WO_OR	SCOM_ERR_MASK: Scom Error Mask
42	RW	WO_AND	WO_OR	SCOM_ERR_DUP_MASK: Scom Error Duplicate Mask

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Registers Specification

POWER8 Processor

Register Name		<i>MCD Recovery Pre Epsilon Configuration Register</i>
Mnemonic		EH.PB.MCD.MCDCTL.MCD_PRE_EP
Address		000000000201340B (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:1	RW	MCD_PBH_CMD_DROP_PRIORITY: Sets mcd_pbh_cmd_drop_priority to the processor bus. 00 - default 01 - chksw
2:39	RO	Constant = 0b00000000000000000000000000000000
40:43	RW	MCD_RTY_COUNT: MCD Recovery Retry Count
44	RO	Constant = 0b0
45:47	RW	MCD_REC_SHORT_TEST:
48:49	RO	Constant = 0b00
50:63	RW	MCD_PRE_EPSILON: MCD Recovery Pre Epsilon

Register Name		<i>MCD TOP (mcd_cn00) Configuration Register</i>
Mnemonic		EH.PB.MCD.MCDCTL.MCD_TOP
Address		000000000201340C (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0	RW	MCD_TOP_VALID: MCD_TOP valid.
1:4	RW	MCD_TOP_CPG: MCD_TOP number of memory controllers per group. 1=>0b1000 2=>0b0100 4=>0b0010 8=>0b0001
5	RO	Constant = 0b0 1=>0b1000 2=>0b0100 4=>0b0010 8=>0b0001
6:8	RW	MCD_TOP_GRP_MBR_ID: MCD_TOP group member identification



Bits	SCOM	Field Mnemonic: Description
9:29	RW	MCD_TOP_GRP_SIZE: MCD_TOP group size 16MB=>0b00000000000000000000 32MB=>0b000000000000000000001 64MB=>0b0000000000000000000011 128MB=>0b00000000000000000000111 256MB=>0b000000000000000000001111 512MB=>0b0000000000000000000011111 1GB=>0b00000000000000000000111111 2GB=>0b000000000000000000001111111 4GB=>0b0000000000000000000011111111 8GB=>0b00000000000000000000111111111 16GB=>0b000000000000000000001111111111 32GB=>0b0000000000000000000011111111111 64GB=>0b00000000000000000000111111111111 128GB=>0b000000000000000000001111111111111 256GB=>0b0000000000000000000011111111111111 512GB=>0b0000000000000000000011111111111111 1TB=>0b00000000000000000000111111111111111 2TB=>0b000000000000000000001111111111111111 4TB=>0b0000000000000000000011111111111111111 8TB=>0b00000000000000000000111111111111111111 16TB=>0b000000000000000000001111111111111111111 32TB=>0b0000000000000000000011111111111111111111
30:55	RW	MCD_TOP_GRP_BASE: MCD_TOP base address
56:58	RO	Constant = 0b000
59	RW	MCD_TOP_SCOPE: MCD_TOP system or foreign scope select
60:61	RW	MCD_TOP_LINK_ID: MCD_TOP foreign scope link ID.
62	RW	MCD_TOP_NO_ARRAY_ALLOC: MCD_TOP disable array allocation.
63	RW	MCD_TOP_ALWAYS_RTY: MCD_TOP disable array access and force rty_dinc response.

Register Name	<i>MCD_STR (mcd_cn01) Configuration Register</i>
Mnemonic	EH.PB.MCD.MCDCTL.MCD_STR
Address	000000000201340D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MCD_STR_VALID: MCD_str valid.
1:4	RW	MCD_STR_CPG: MCD_str number of memory controllers per group. 1=>0b1000 2=>0b0100 4=>0b0010 8=>0b0001
5	RO	Constant = 0b0 1=>0b1000 2=>0b0100 4=>0b0010 8=>0b0001

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Bits	SCOM	Field Mnemonic: Description
6:8	RW	MCD_STR_GRP_MBR_ID: MCD_str group member identification
9:29	RW	MCD_STR_GRP_SIZE: MCD_STR group size 16MB=>0b00000000000000000000 32MB=>0b000000000000000000001 64MB=>0b0000000000000000000011 128MB=>0b00000000000000000000111 256MB=>0b000000000000000000001111 512MB=>0b0000000000000000000011111 1GB=>0b00000000000000000000111111 2GB=>0b000000000000000000001111111 4GB=>0b0000000000000000000011111111 8GB=>0b00000000000000000000111111111 16GB=>0b000000000000000000001111111111 32GB=>0b0000000000000000000011111111111 64GB=>0b00000000000000000000111111111111 128GB=>0b000000000000000000001111111111111 256GB=>0b0000000000000000000011111111111111 512GB=>0b00000000000000000000111111111111111 1TB=>0b000000000000000000001111111111111111 2TB=>0b0000000000000000000011111111111111111 4TB=>0b00000000000000000000111111111111111111 8TB=>0b000000000000000000001111111111111111111 16TB=>0b0000000000000000000011111111111111111111 32TB=>0b00000000000000000000111111111111111111111
30:55	RW	MCD_STR_GRP_BASE: MCD_STR base address
56:58	RO	Constant = 0b000
59	RW	MCD_STR_SCOPE: MCD_str system or foreign scope select
60:61	RW	MCD_STR_LINK_ID: MCD_str foreign scope link ID.
62	RW	MCD_STR_NO_ARRAY_ALLOC: MCD_STR disable array allocation.
63	RW	MCD_STR_ALWAYS_RTY: MCD_STR disable array array access and force rty_dinc response.

Register Name	<i>MCD BOT (mcd_cn10) Configuration Register</i>	
Mnemonic	EH.PB.MCD.MCDCTL.MCD_BOT	
Address	000000000201340E (SCOM)	
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0	RW	MCD_BOT_VALID: MCD_bot valid.
1:4	RW	MCD_BOT_CPG: MCD_bot number of memory controllers per group. 1=>0b1000 2=>0b0100 4=>0b0010 8=>0b0001



Bits	SCOM	Field Mnemonic: Description
5	RO	Constant = 0b0 1=>0b1000 2=>0b0100 4=>0b0010 8=>0b0001
6:8	RW	MCD_BOT_GRP_MBR_ID: MCD_bot group member identification
9:29	RW	MCD_BOT_GRP_SIZE: MCD_BOT group size 16MB=>0b00000000000000000000 32MB=>0b00000000000000000001 64MB=>0b00000000000000000011 128MB=>0b00000000000000000111 256MB=>0b00000000000000001111 512MB=>0b00000000000000011111 1GB=>0b00000000000000111111 2GB=>0b00000000000001111111 4GB=>0b00000000000011111111 8GB=>0b00000000000111111111 16GB=>0b00000000001111111111 32GB=>0b00000000011111111111 64GB=>0b00000000111111111111 128GB=>0b00000001111111111111 256GB=>0b00000011111111111111 512GB=>0b00000011111111111111 1TB=>0b00000111111111111111 2TB=>0b00001111111111111111 4TB=>0b00011111111111111111 8TB=>0b00111111111111111111 16TB=>0b01111111111111111111 32TB=>0b11111111111111111111
30:55	RW	MCD_BOT_GRP_BASE: MCD_BOT base address
56:58	RO	Constant = 0b000
59	RW	MCD_BOT_SCOPE: MCD_bot system or foreign scope select
60:61	RW	MCD_BOT_LINK_ID: MCD_bot foreign scope link ID.
62	RW	MCD_BOT_NO_ARRAY_ALLOC: MCD_BOT disable array allocation.
63	RW	MCD_BOT_ALWAYS_RTY: MCD_BOT disable array array access and force rty_dinc response.

Register Name	<i>MCD_CHA (mcd_cn11) Configuration Register</i>
Mnemonic	EH.PB.MCD.MCDCTL.MCD_CHA
Address	000000000201340F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	MCD_CHA_VALID: MCD_cha valid.

Registers Specification

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Bits	SCOM	Field Mnemonic: Description
1:4	RW	MCD_CHA_CPG: MCD_cha number of memory controllers per group. 1=>0b1000 2=>0b0100 4=>0b0010 8=>0b0001
5	RO	Constant = 0b0 1=>0b1000 2=>0b0100 4=>0b0010 8=>0b0001
6:8	RW	MCD_CHA_GRP_MBR_ID: MCD_cha group member identification
9:29	RW	MCD_CHA_GRP_SIZE: MCD_CHA group size 16MB=>0b000000000000000000000000 32MB=>0b000000000000000000000001 64MB=>0b000000000000000000000011 128MB=>0b000000000000000000000111 256MB=>0b000000000000000000001111 512MB=>0b000000000000000000111111 1GB=>0b000000000000000001111111 2GB=>0b000000000000000011111111 4GB=>0b000000000000000111111111 8GB=>0b000000000000011111111111 16GB=>0b000000000001111111111111 32GB=>0b000000000111111111111111 64GB=>0b000000001111111111111111 128GB=>0b000000011111111111111111 256GB=>0b000000011111111111111111 512GB=>0b000000111111111111111111 1TB=>0b000001111111111111111111 2TB=>0b000011111111111111111111 4TB=>0b000111111111111111111111 8TB=>0b001111111111111111111111 16TB=>0b011111111111111111111111 32TB=>0b111111111111111111111111
30:55	RW	MCD_CHA_GRP_BASE: MCD_CHA base address
56:58	RO	Constant = 0b000
59	RW	MCD_CHA_SCOPE: MCD_cha system or foreign scope select
60:61	RW	MCD_CHA_LINK_ID: MCD_cha foreign scope link ID.
62	RW	MCD_CHA_NO_ARRAY_ALLOC: MCD_CHA disable array allocation.
63	RW	MCD_CHA_ALWAYS_RTY: MCD_CHA disable array array access and force rty_dinc response.

Register Name	<i>MCD Even Recovery Control Register</i>
Mnemonic	EH.PB.MCD.MCDCTL.MCD_REC_EVEN
Address	000000002013410 (SCOM)
Attributes	
Description	



Bits	SCOM	Field Mnemonic: Description
0	RWX	MCD_REC_EVEN_ENABLE: 0 to 1 transition needed to start, reset to 0 at end of request.
1	ROX	MCD_REC_EVEN_COMPLETE:
2	RW	MCD_REC_EVEN_CONTINUOUS:
3	ROX	MCD_REC_EVEN_REG_STAT:
4	ROX	MCD_REC_EVEN_RESULT_STAT:
5	ROX	MCD_REC_EVEN_REQ_PEND:
6:7	RO	Constant = 0b00
8:19	RW	MCD_REC_EVEN_PACE_DELAY:
20	RW	MCD_REC_EVEN_RECOVER_ALL:
21	ROX	MCD_REC_EVEN_RECOVER_ALL_FAIL:
22:39	RW	MCD_REC_EVEN_GRAN_ADDR:
40:43	RW	MCD_REC_EVEN_CONFIG_SEL:
44	ROX	MCD_REC_EVEN_ADDR_ERROR:
45	RO	Constant = 0b0
46:63	RW	MCD_REC_EVEN_GRAN_COUNT:

Register Name	<i>MCD Odd Recovery Control Register</i>
Mnemonic	EH.PB.MCD.MCDCTL.MCD_REC_ODD
Address	0000000002013411 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX	MCD_REC_ODD_ENABLE: 0 to 1 transition needed to start, reset to 0 at end of request.
1	ROX	MCD_REC_ODD_COMPLETE:
2	RW	MCD_REC_ODD_CONTINUOUS:
3	ROX	MCD_REC_ODD_REG_STAT:
4	ROX	MCD_REC_ODD_RESULT_STAT:
5	ROX	MCD_REC_ODD_REQ_PEND:
6:7	RO	Constant = 0b00
8:19	RW	MCD_REC_ODD_PACE_DELAY:
20	RW	MCD_REC_ODD_RECOVER_ALL:
21	ROX	MCD_REC_ODD_RECOVER_ALL_FAIL:
22:39	RW	MCD_REC_ODD_GRAN_ADDR:
40:43	RW	MCD_REC_ODD_CONFIG_SEL:
44	ROX	MCD_REC_ODD_ADDR_ERROR:
45	RO	Constant = 0b0
46:63	RW	MCD_REC_ODD_GRAN_COUNT:



Registers Specification

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Register Name	GP Register 1
Mnemonic	EN.PB.TPC.GP1
Address	0000000004000001 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	NOT_USED18: Not used. Reset (0).
1	ROX	NOT_USED19: Not used. Reset (0).
2	ROX	NOT_USED20: Not used. Reset (0).
3	ROX	TRA_TC_ABIST_DONE_DC: X bus asynchronous trace arrays ABIST done. Reset (0).
4	ROX	NOT_USED21: Not used. Reset (0).
5	ROX	NOT_USED22: Not used. Reset (0).
6	ROX	NOT_USED23: Not used. Reset (0).
7	ROX	NOT_USED24: Not used. Reset (0).
8	ROX	NOT_USED25: Not used. Reset (0).
9	ROX	NOT_USED26: Not used. Reset (0).
10	ROX	NOT_USED27: Not used. Reset (0).
11	ROX	NOT_USED28: Not used. Reset (0).
12	ROX	NOT_USED29: Not used. Reset (0).
13	ROX	NOT_USED30: Not used. Reset (0).
14	ROX	NOT_USED31: Not used. Reset (0).
15	ROX	TC_OPCG_DONE_DC: Clock control OPCG done, Reset (0).
16	ROX	FREE_USAGE0: chiplet specific, Reset (0).
17	ROX	FREE_USAGE1: chiplet specific, Reset (0).
18	ROX	FREE_USAGE2: chiplet specific, Reset (0).
19	ROX	FREE_USAGE3: chiplet specific, Reset (0).
20	ROX	FREE_USAGE4: chiplet specific, Reset (0).
21	ROX	FREE_USAGE5: chiplet specific, Reset (0).
22	ROX	FREE_USAGE6: chiplet specific, Reset (0).
23	ROX	FREE_USAGE7: chiplet specific, Reset (0).

Register Name	GP Register 2
Mnemonic	EN.PB.TPC.GP2
Address	0000000004000002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:23	RW	GPIN_MASKING: GPIN bitwise interrupt masking



Register Name		<i>Clk Ajust Config</i>
Mnemonic		EH.TPCHIP.NET.PCBSLXB.CLK_ADJ_SET
Address		00000000040F0016 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:31	RW	CLK_ADJ_SET_REG: Clk adj config

Register Name		<i>PSCOMLE Mode Register</i>
Mnemonic		EN.PB.TPC.EPS.PSC.PSCOM_MODE_REG
Address		0000000004010000 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RW	ABORT_ON_PCB_ADDR_PARITY_ERROR: abort_on_PCB_addr_parity_error
1	RW	ABORT_ON_PCB_WDATA_PARITY_ERROR: abort_on_PCB_wdata_parity_error
2	RW	ABORT_ON_DL_RETURN_P0_ERROR: abort_on_DL_return_P0_error
3	RW	ABORT_ON_DL_RETURN_WDATA_PARITY_ERROR: abort_on_DL_return_wdata_parity_error
4	RW	WATCHDOG_ENABLE: watchdog_enable
5:6	RW	SCOM_HANG_LIMIT: 0b11: 256, 0b10:512, 0b01:768, 0b00:1023
7	RW	FORCE_ALL_RINGS: set to logic 1 if all rings should be enable independent of ring address
8	RW	FSM_SELFRESET_ON_STATEVEC_PARITYERROR_ENABLE: fsm_selfreset_on_statevec_parityerror_enable
9:11	RW	RESERVED_PSCOM_MODE_LT: reserved

Register Name		<i>Debug Status Register</i>
Mnemonic		EN.PB.TPC.EPS.PSC.DEBUG_STATUS_REG
Address		0000000004010004 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RWX	LOCAL_TRACE_RUN_IN: local trace run
1:2	RWX	TRACE_STATE_LAT: trace state latch
3	RWX	TRACE_FREEZE: trace freeze
4:5	RWX	COND3_STATE_LT: condition 3 state latch
6:7	RWX	COND5_STATE_LT: condition 5 state latch
8	RWX	HISTORY_CONDITION0_LT: condition event history for condition0_lt
9	RWX	HISTORY_CONDITION1_LT: condition event history for condition1_lt
10	RWX	HISTORY_COND2_3_EVENT: condition event history for cond2_3_event



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Bits	PCB	Field Mnemonic: Description
11	RWX	HISTORY_COND2_TIMEOUT: condition event history for cond2_timeout
12	RWX	HISTORY_COND4_5_EVENT: condition event history for cond4_5_event
13	RWX	HISTORY_COND4_TIMEOUT: condition event history for cond4_timeout
14:15	RWX	RESERVED_TCDBG_STATUS_LT: reserved, set to zero

Register Name	<i>Trace Array High Data Register</i>
Mnemonic	EN.PB.TPC.TRA0.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG
Address	0000000004010400 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63

Register Name	<i>Trace Array Low Data Register</i>
Mnemonic	EN.PB.TPC.TRA0.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG
Address	0000000004010401 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95
32:41	ROX	TRACE_ADDRESS: Trace Address
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank
51	ROX	TRACE_LAST_BANK_VALID: Trace Last Bank Valid
52	ROX	TRACE_WRITE_ON_RUN: Trace Write-On-Run indicator
53	ROX	TRACE_RUNNING: Trace Run indicator
54:63	ROX	TRACE_HOLD_ADDRESS: Trace Hold Address (pointing to last entry)

Register Name	<i>Trace Array High Data Register</i>
Mnemonic	EN.PB.TPC.TRA1.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG
Address	0000000004010800 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63



Register Name		Trace Array Low Data Register
Mnemonic		EN.PB.TPC.TRA1.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG
Address		0000000004010801 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95
32:41	ROX	TRACE_ADDRESS: Trace Address
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank
51	ROX	TRACE_LAST_BANK_VALID: Trace Last Bank Valid
52	ROX	TRACE_WRITE_ON_RUN: Trace Write-On-Run indicator
53	ROX	TRACE_RUNNING: Trace Run indicator
54:63	ROX	TRACE_HOLD_ADDRESS: Trace Hold Address (pointing to last entry)

Register Name		Processor Bus PBEN IOX Domain FIR0 Register
Mnemonic		EN.PB.PBEN.MISC_IO.SCOM.FIR_REG
Address		0000000004010C00 (SCOM) 0000000004010C01 (SCOM1) 0000000004010C02 (SCOM2)
Attributes		
Description		

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	X0_LINK_RCV_CE: x0 link rcv ce
1	RWX	WOX_AND	WOX_OR	X0_LINK_RCV_DERR: x0 link rcv derr
2	RWX	WOX_AND	WOX_OR	X0_LINK_RCV_UE: x0 link rcv ue
3	RWX	WOX_AND	WOX_OR	X1_LINK_RCV_CE: x1 link rcv ce
4	RWX	WOX_AND	WOX_OR	X1_LINK_RCV_DERR: x1 link rcv derr
5	RWX	WOX_AND	WOX_OR	X1_LINK_RCV_UE: x1 link rcv ue
6	RWX	WOX_AND	WOX_OR	X2_LINK_RCV_CE: x2 link rcv ce
7	RWX	WOX_AND	WOX_OR	X2_LINK_RCV_DERR: x2 link rcv derr
8	RWX	WOX_AND	WOX_OR	X2_LINK_RCV_UE: x2 link rcv ue
9	RWX	WOX_AND	WOX_OR	X3_LINK_RCV_CE: x3 link rcv ce
10	RWX	WOX_AND	WOX_OR	X3_LINK_RCV_DERR: x3 link rcv derr
11	RWX	WOX_AND	WOX_OR	X3_LINK_RCV_UE: x3 link rcv ue
12	RWX	WOX_AND	WOX_OR	X_LINK_SND_CE: x link rcv ce
13	RWX	WOX_AND	WOX_OR	X_LINK_SND_SUE: x link rcv sue
14	RWX	WOX_AND	WOX_OR	X_LINK_SND_UE: x link rcv ue
15	RWX	WOX_AND	WOX_OR	X_LINK_CR_OVERFLOW: x link command/response/data buffer overflow
16	RWX	WOX_AND	WOX_OR	X0_LINK_FMR_ERR: x0 link framer error
17	RWX	WOX_AND	WOX_OR	X1_LINK_FMR_ERR: x1 link framer error



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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
18	RWX	WOX_AND	WOX_OR	X2_LINK_FMR_ERR: x2 link framer error
19	RWX	WOX_AND	WOX_OR	X3_LINK_FMR_ERR: x3 link framer error
20	RWX	WOX_AND	WOX_OR	X_LINK_PSR_ERR: x link parser error
21:35	RWX	WOX_AND	WOX_OR	Reserved field. (Access type is unused.)
36	RWX	WOX_AND	WOX_OR	FIR_SCOM_ERR_DUP: pben iox fir_scom_err
37	RWX	WOX_AND	WOX_OR	FIR_SCOM_ERR: pben iox fir_scom_err
38:63	RO	N/A	N/A	Constant = 0b000000000000000000000000

Register Name	<i>Processor Bus PBEN IOX Domain FIR MASK Register</i>
Mnemonic	EN.PB.PBEN.MISC_IO.SCOM.FIR_MASK_REG
Address	0000000004010C03 (SCOM) 0000000004010C04 (SCOM1) 0000000004010C05 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	X0_LINK_RCV_CE_MASK: x0 link rcv ce
1	RW	WO_AND	WO_OR	X0_LINK_RCV_DERR_MASK: x0 link rcv derr
2	RW	WO_AND	WO_OR	X0_LINK_RCV_UE_MASK: x0 link rcv ue
3	RW	WO_AND	WO_OR	X1_LINK_RCV_CE_MASK: x1 link rcv ce
4	RW	WO_AND	WO_OR	X1_LINK_RCV_DERR_MASK: x1 link rcv derr
5	RW	WO_AND	WO_OR	X1_LINK_RCV_UE_MASK: x1 link rcv ue
6	RW	WO_AND	WO_OR	X2_LINK_RCV_CE_MASK: x2 link rcv ce
7	RW	WO_AND	WO_OR	X2_LINK_RCV_DERR_MASK: x2 link rcv derr
8	RW	WO_AND	WO_OR	X2_LINK_RCV_UE_MASK: x2 link rcv ue
9	RW	WO_AND	WO_OR	X3_LINK_RCV_CE_MASK: x3 link rcv ce
10	RW	WO_AND	WO_OR	X3_LINK_RCV_DERR_MASK: x3 link rcv derr
11	RW	WO_AND	WO_OR	X3_LINK_RCV_UE_MASK: x3 link rcv ue
12	RW	WO_AND	WO_OR	X_LINK_SND_CE_MASK: x link rcv ce
13	RW	WO_AND	WO_OR	X_LINK_SND_SUE_MASK: x link rcv sue
14	RW	WO_AND	WO_OR	X_LINK_SND_UE_MASK: x link rcv ue
15	RW	WO_AND	WO_OR	X_LINK_CR_OVERFLOW_MASK: x link command/response/data buffer overflow
16	RW	WO_AND	WO_OR	X0_LINK_FMR_ERR_MASK: x0 link framer error
17	RW	WO_AND	WO_OR	X1_LINK_FMR_ERR_MASK: x1 link framer error
18	RW	WO_AND	WO_OR	X2_LINK_FMR_ERR_MASK: x2 link framer error
19	RW	WO_AND	WO_OR	X3_LINK_FMR_ERR_MASK: x3 link framer error
20	RW	WO_AND	WO_OR	X_LINK_PSR_ERR_MASK: x link parser error
21:35	RW	WO_AND	WO_OR	
36	RW	WO_AND	WO_OR	FIR_SCOM_ERR_MASK_DUP: pben iox fir_scom_err_mask_dup



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
37	RW	WO_AND	WO_OR	FIR_SCOM_ERR_MASK: pben iox fir_scom_err_mask
38:63	RO	N/A	N/A	Constant = 0b000000000000000000000000

Register Name	Processor Bus PBEN IOX Domain FIR Action 0 Register
Mnemonic	EN.PB.PBEN.MISC_IO.SCOM.FIR_REG_ACTION0
Address	0000000004010C06 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:37	RW	PB_IOX_FIR_ACTION0: processor bus PBEN IOX domain action select for corresponding bit in FIR (Action0,Action1) = Action Select (0,0) = Checkstop (0,1) = Recoverable Error to Service Processor (1,0) = Recoverable Interrupt to Processor (1,1) = Invalid
38:63	RO	Constant = 0b000000000000000000000000

Register Name	Processor Bus PBEN IOX Domain FIR Action 1 Register
Mnemonic	EN.PB.PBEN.MISC_IO.SCOM.FIR_REG_ACTION1
Address	0000000004010C07 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:37	RW	PB_IOX_FIR_ACTION1: Processor bus FIR LSB of action select for corresponding bit in FIR (Action0,Action1) = Action Select (0,0) = Checkstop (0,1) = Recoverable Error to Service Processor (1,0) = Recoverable Interrupt to Processor (1,1) = Invalid
38:63	RO	Constant = 0b000000000000000000000000

Register Name	Processor Bus PBEN IOX Domain Mode Register
Mnemonic	EN.PB.PBEN.MISC_IO.SCOM.PB_X_MODE
Address	0000000004010C0A (SCOM)
Attributes	
Description	00 = x_avp_mode 01 = x_4B_mode 02:03 = x_mode_spare 04 = x_trace_enable 05:07 = x_trace_select 08 = x_trace_framer_mode 09:10 = x_trace_override 11 = x_trace_spare 12:15 = x_tod_wait_limit 16 = x_Enable_perfttrace - perfttrace mode enabled, bits 5:10 become irrelevant, but x_trace_enable=1 is required 17 = x_perfttrace_prescale - wide-angle view - perfcounts are prescaled by 128 18 = x_perfttrace_fixed_win - take a sample every 255 or 255x128 cycles 19 = Link X0 trained 20 = Link X1 trained 21 = Link X2 trained 22 = Link X3 trained 23 = reserved 24:31 = Link X0 Round-trip Delay 32:39 = Link X1 Round-trip Delay 40:47 = Link X2 Round-trip Delay 48:55 = Link X3 Round-trip Delay 56:63 = reserved

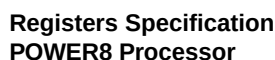


Registers Specification
POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
0	RW	X_AVP_MODE: 0 = functional mode 1 = ivp mode
1	RW	X_4B_MODE: 0 = 8 Byte mode 1 = 4 Byte mode



Bits	SCOM	Field Mnemonic: Description
2:3	RW	
4	RW	X_TRACE_ENABLE: 0 = disabled 1 = enabled
5:7	RW	X_TRACE_SELECT: 000 X0 input trace 001 X1 input trace 010 X2 input trace 011 X3 input trace 100 X0 output trace 101 X1 output trace 110 X2 output trace 111 X3 output trace
8	RW	X_TRACE_FRAMER_MODE: Framer trace is bits 78:87 of both _hi and _lo traces. 0 = default mode 1 = alternate trace mode
9:10	RW	X_TRACE_OVERRIDE: This overrides the _lo(0:87) trace. 00 normal (xlink trace, see bits 05:08, uses pb_dbg_mx_prev) 01 reserved 10 override _lo with OBS trace 11 override _lo with ei4 trace
11	RW	Reserved field. (Access type is x_trace_spare.)
12:15	RW	X_TOD_WAIT_LIMIT: Limits the maximum wait before sending the TOD on the x-link. The TOD gets priority if it has been held for this number of cycles 0000 disables the feature 0100 is the default
16	RW	X_ENABLE_PERFTRACE: This dial overrides all other trace modes with perfcounter data. Also, requires x_trace_enable = 1. When 1, both trace arrays are fed link utilization counter data.
17	RW	X_PERFTRACE_PRESCALE: Adds a 128x prescalar to perftrace mode (that is, bigger windows, lower resolution).
18	RW	X_PERFTRACE_FIXED_WIN: When 1, it forces a perftrace sample to be taken every 255 cycles. When x_perftrace_prescale is also equal to `1`, a sample is taken every 255 x 128 = 32640 cycles.
19	ROX	Reserved field. (Access type is Link_X0_trained.)
20	ROX	Reserved field. (Access type is Link_X1_trained.)
21	ROX	Reserved field. (Access type is Link_X2_trained.)
22	ROX	Reserved field. (Access type is Link_X3_trained.)
23	RO	Constant = 0b0
24:31	ROX	Reserved field. (Access type is Link_X0_Round_trip_Delay.)
32:39	ROX	Reserved field. (Access type is Link_X1_Round_trip_Delay.)
40:47	ROX	Reserved field. (Access type is Link_X2_Round_trip_Delay.)
48:55	ROX	Reserved field. (Access type is Link_X3_Round_trip_Delay.)
56:63	RO	Constant = 0b00000000

[illegible]

Version 1.2
15 June 2016



Bits	SCOM	Field Mnemonic: Description
0	NCX	Reserved field. (Access type is rx_psi_ioreset_wo_pulse_slow_signal)
1	RWX	RX_PSI_PATTERN_CHECK_EN: Enables the drive pattern to be tested.. DMB 0b0 = No pattern checking 0b1 = Check for drive pattern DISABLED=>0b0 ENABLED=>0b1
2:3	RWX	RX_PSI_PATTERN_SEL: RX pattern select. DMB 0b00 = ei4 busy patt A 0b01 = ei4 busy patt B 0b10 = 16 bit legacy 0b11 = IE3 Busy IAP Pattern EI4A=>0b00 EI4B=>0b01 LEGACY16=>0b10 EI3BUSY=>0b11
4	RWX	RX_PSI_CLK_INVERT: Used to invert the polarity of the CLK.. DMB 0b0 = Normal CLK Polarity (default) 0b1 = CLK Inverted NORMAL=>0b0 INVERTED=>0b1
5	RWX	RX_PSI_LANE_INVERT: Used to invert the polarity of the data lane.. DMB 0b0 = Normal Data Lane Polarity (default) 0b1 = Data Lane Inverted NORMAL=>0b0 INVERTED=>0b1
6	RWX	RX_PSI_PDWN: Used to power down the PSI RX clock and data path.. MBS 0b0 = Operational (default) 0b1 = Clock and data path are powered off NORMAL=>0b0 POWERDOWN=>0b1
7:13	RWX	RX_PSI_CLK_DLY: Clock delay setting. Default value is 300ps at the fast corner.. DMB
14:20	RWX	RX_PSI_DATA_DLY: Data delay setting. Default value is 300ps at the fast corner.. DMB
21:25	RWX	RX_PSI_DEGLITCH_CLK_DLY: Clock deglitcher delay setting. Default value is 300ps at the fast corner.. DMB
26:30	RWX	RX_PSI_DEGLITCH_DATA_DLY: Data deglitcher-match delay setting. To match clock line, default value is 300ps at the fast corner.. DMB
31	RO	Constant = 0b0

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Register Name		<i>RX Status Register</i>
Mnemonic		PSI.PSI_MAC.PSI_SCOM.PSI_SCOM_REGS.RX_PSI_STATUS
Address		0000000004012422 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is rx_psi_pattern_check_pass_ro_signal)
1	ROX	Reserved field. (Access type is rx_psi_pattern_check_fail_ro_signal)
2	ROX	Reserved field. (Access type is rx_psi_no_pattern_found_ro_signal)
3	RO	Constant = 0b0
4:7	RWX	RX_PSI_LD_UNLD_DLY: Current PSI load to unload delay. TBD. DMB
8	RWX	RX_PSI_OVER_OR_UNDERRUN_ERR: FIFO Overrun or Underrun Error. TBD. DMB
9	RWX	RX_PSI_STATUS_CLEAR: Clears Pattern check status. DMB
10:15	RWX	RX_PSI_STATUS_SPARE: Spares. TBD. DMB
16:31	RO	Constant = 0b0000000000000000

Register Name		<i>TX Cntl Register</i>
Mnemonic		PSI.PSI_MAC.PSI_SCOM.PSI_SCOM_REGS.TX_PSI_CNTL
Address		0000000004012430 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0	NCX	Reserved field. (Access type is tx_psi_ioreset_wo_pulse_slow_signal)
1	RWX	TX_PSI_DRV_PATTERN_EN: Enables the drive pattern to be driven.. DMB 0b0 = No pattern driven 0b1 = Drive pattern DISABLED=>0b0 ENABLED=>0b1
2:3	RWX	TX_PSI_PATTERN_SEL: TX pattern select. DMB 0b00 = ei4 busy patt A 0b01 = ei4 busy patt B 0b10 = 16 bit legacy 0b11 = IE3 Busy IAP Pattern EI4A=>0b00 EI4B=>0b01 LEGACY16=>0b10 EI3BUSY=>0b11



Bits	SCOM	Field Mnemonic: Description
4:5	RWX	TX_PSI_CLK_QUIESCE_P: Used to force the output of the CLK P lane to a particular value.. DMB 0b00 = Functional CLK (default) 0b01 = Quiesce CLK to a Static 0 value 0b10 = Quiesce CLK to a Static 1 value 0b11 = Tri-State CLK Output FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
6:7	RWX	TX_PSI_CLK_QUIESCE_N: Used to force the output of the CLK N lane to a particular value.. DMB 0b00 = Functional CLK (default) 0b01 = Quiesce CLK to a Static 0 value 0b10 = Quiesce CLK to a Static 1 value 0b11 = Tri-State CLK Output FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
8:9	RWX	TX_PSI_LANE_QUIESCE: Used to force the output of the data lane to a particular value.. DMB 0b00 = Functional Data (default) 0b01 = Quiesce Lane to a Static 0 value 0b10 = Quiesce Lane to a Static 1 value 0b11 = Tri-State Lane Output FUNCTIONAL=>0b00 QUIESCE_TO_0=>0b01 QUIESCE_TO_1=>0b10 QUIESCE_TO_Z=>0b11
10	RWX	TX_PSI_CLK_INVERT: Used to invert the polarity of the CLK.. DMB 0b0 = Normal CLK Polarity (default) 0b1 = CLK Inverted NORMAL=>0b0 INVERTED=>0b1
11	RWX	TX_PSI_LANE_INVERT: Used to invert the polarity of the data lane.. DMB 0b0 = Normal Data Lane Polarity (default) 0b1 = Data Lane Inverted NORMAL=>0b0 INVERTED=>0b1
12	RWX	TX_PSI_PDWN: Used to power down the PSI TX clock and data path.. MBS 0b0 = Operational (default) 0b1 = Clock and data path are powered off NORMAL=>0b0 POWERDOWN=>0b1

Registers Specification

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Bits	SCOM	Field Mnemonic: Description
13	RWX	TX_PSI_BIST_EN: Used to run TX BIST. . JGR 0b0 = TX BIST disabled 0b1 = TX BIST enabled DISABLED=>0b0 ENABLED=>0b1
14:23	RO	Constant = 0b0000000000 DISABLED=>0b0 ENABLED=>0b1
24:31	RWX	TX_PSI_CNTRL_SPARE: Spares. TBD. DMB

Register Name	OPCG Control Register 0
Mnemonic	EN.PB.TPC.OPCG_REG0
Address	0000000004030002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	RUNN_MODE: runn-mode if 1 or BIST mode if 0
1	RWX	OPCG_GO: opcg go (start sequence)
2	RWX	RUN_SCAN0: run scan0 (will override all BIST mode settings but the scan_ratio)
3	RW	SCAN0_MODE: set PRPGs in scan0_mode but do not run automatic scan0 sequence
4:8	RW	SCAN_RATIO: scan_ratio (n=0-15: (n+1):1, 16: 24:1, 17: 32:1, 18: 48:1, 19: 64:1, 20: 128:1)
9	RW	INOP_FORCE_SG: Set SG high during INOP
10:13	RW	INOP_ALIGN: INOP phase alignment (0: none, 1: 2:1, 2: 3:1, 3: 4:1, 4: 6:1, 5: 8:1, 6: 12:1, 7: 16:1, 8: 24:1)
14:20	RW	INOP_WAIT: INOP cycle delay (1-127)
21:24	RWX	SNOP_ALIGN: BIST mode: SNOP phase alignment (like INOP), runn-mode: loopcnt(0:3)
25:27	RWX	SNOP_WAIT: BIST mode: SNOP cycle delay (0-7), runn-mode: loopcnt(4:6)
28:31	RWX	ENOP_ALIGN: BIST mode: ENOP phase alignment (like INOP), runn-mode: loopcnt(7:10)
32:34	RWX	ENOP_WAIT: BIST mode: ENOP cycle delay (0-7), runn-mode: loopcnt(11:13)
35	RWX	ENOP_FORCE_SG: BIST mode: Set SG high during ENOP, runn-mode: loopcnt(14)
36:63	RWX	LOOP_COUNT: BIST mode: loop count (l = 1-2^28 (about 5 minutes LBIST)), runn-mode: loopcnt(15:42)

Register Name	OPCG Control Register 1
Mnemonic	EN.PB.TPC.OPCG_REG1
Address	0000000004030003 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	FUNC_CAPT_COUNT: BIST mode: capture cycles (1-12) encoded as capture cycle - 1

Bits	PCB	Field Mnemonic: Description
4:8	RW	FUNC_CAPT_SEQ01_01F: BIST mode: capture cycle 1 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
9:13	RW	FUNC_CAPT_SEQ02_02F: BIST mode: capture cycle 2 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
14:18	RW	FUNC_CAPT_SEQ03_03F: BIST mode: capture cycle 3 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
19:23	RW	FUNC_CAPT_SEQ04_04F: BIST mode: capture cycle 4 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
24:28	RW	FUNC_CAPT_SEQ05_05F: BIST mode: capture cycle 5 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
29:33	RW	FUNC_CAPT_SEQ06_06F: BIST mode: capture cycle 6 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
34:38	RW	FUNC_CAPT_SEQ07_07F: BIST mode: capture cycle 7 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
39:43	RW	FUNC_CAPT_SEQ08_08F: BIST mode: capture cycle 8 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
44:48	RW	FUNC_CAPT_SEQ09_01FBY2: BIST mode: capture cycle 1 for slow domain or cycle 9 for single mesh support(sl, nsl, ary, sg, fce)
49:53	RW	FUNC_CAPT_SEQ10_02FBY2: BIST mode: capture cycle 2 for slow domain or cycle 10 for single mesh support(sl, nsl, ary, sg, fce)
54:58	RW	FUNC_CAPT_SEQ11_03FBY2: BIST mode: capture cycle 3 for slow domain or cycle 11 for single mesh support(sl, nsl, ary, sg, fce)
59:63	RW	FUNC_CAPT_SEQ12_04FBY2: BIST mode: capture cycle 4 for slow domain or cycle 12 for single mesh support(sl, nsl, ary, sg, fce)

Register Name	OPCG Control Register 2
Mnemonic	EN.PB.TPC.OPCG_REG2
Address	0000000004030004 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:11	RW	SCAN_COUNT: BIST mode: Channel scan count (s = 0-4095) runn-mode: start_abist match value(0:11)
12:23	RW	MISR_A_VAL: BIST mode: a value for MISR aperture, runn-mode: start_abist match value(12:23)
24:35	RW	MISR_B_VAL: BIST mode: b value for MISR aperture, runn-mode: start_abist match value(24:35)
36:47	RW	MISR_INIT_WAIT: BIST mode: delay MISR aperture, MISRs get active after this number of loops
48	RW	OPCG_SUPPRESS_EVEN_CLK: OPCG will only create even and not odd clocks. Used for runn to create only one clock in fast domain. Default is 0
49:51	RW	OPCG_PAD_VALUE: After setting all DC signals, wait this many number of cycle x 16 before applying tholds
52	RW	USE_F_AND_FDIV2: BIST mode: if 1, use 8 f and 4 f/2 pattern concurrently, else use 1-12 local mesh patterns
53	RW	USE_ARY_CLK_DURING_FILL: BIST mode: Fire nsl_ary_clock during NSL-fill runn-mode: stop run-n on xstop
54	RW	SG_HIGH_DURING_FILL: BIST mode: Hold SG high during NSL-fill and SNOP runn-mode: OPCG engine controls start_abist (overrides GP0 setting)

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Bits	PCB	Field Mnemonic: Description
55	RW	RTIM_THOLD_FORCE: force rtim_thold low when not in test_dc mode (must be 0 at all time)
56	RW	LBIST_SKITTER_CTL: BIST mode: 0: enable skitter during lbist_ip, 1: enable skitter when misr_active
57	RW	MISR_MODE: BIST mode: MISR aperture mode (0: a-1 to b-1, 1: start to a and b to end)
58	RW	INFINITE_MODE: infinite mode
59:63	RW	NSL_FILL_COUNT: BIST mode: NSL-fill count (0-31)

Register Name	<i>Opcg Start Register</i>
Mnemonic	EN.PB.TPC.OPCG_REG3
Address	0000000004030005 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	OPCG_GO2: opcg go for broadcast sequences (start sequence)
1	RW	RUN_OPCG_ON_UPDATE_DR: start opcg engine when scan updated (update_dr) received (set pulse)
2	RW	RUN_OPCG_ON_CAPTURE_DR: start opcg engine when scan updated (capture_dr) received (set pulse)
3:4	RW	ALIGN_SOURCE_SELECT: 0: use inopa setting from opcg_reg0, 1: use rising edge of sync pulse, 2: use input from unit (for AVP)
5:7	RW	PRPG_WEIGHTING: prpg_activate: 1/2, 1/4, 1/8, 1/16, 1/2, 3/4, 7/8, 15/16
8:19	RWX	PRPG_VALUE: set to 0 for prpg always on, else seed
20	RW	EXTEND_INOPW_ENOPW: extend I/ENOPW: add 256 cycles if i/enop>0, else 257+max i/enop
21	RW	EXTEND_SNOPW: add 256 cycles if snop>0, else 257+max snop
22	RW	FORCE_SG_HIGH_DURING_SNOP: force sg high during snop
23:31	RW	CHKSW: Reserved for debug switches (keep 0 unless chksw required)
32:43	RW	PRPG_A_VAL: a value for PRPG aperture
44:55	RW	PRPG_B_VAL: b value for PRPG aperture
56	RW	PRPG_MODE: PRPG aperture mode (0: a-1 to b-1, 1: start to a and b to end)
57	RW	SCAN_CLK_USE_EVEN: Generate scan clock in odd cycle instead of even. Default is 0
58:63	RW	SPARE3: spares

Register Name	<i>Start/stop Of Clocks</i>
Mnemonic	EN.PB.TPC.CLK_REGION
Address	0000000004030006 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RWX	CLOCK_CMD: command for clock control: 00 NOP 01 START 10 STOP 11 PULSE (one pulse)
2:3	RO	Constant = 0b00
4	RWX	CLOCK_REGION_PERV: for clock region perv (Pervasive)



Bits	PCB	Field Mnemonic: Description
5	RWX	CLOCK_REGION_FASTUNIT0: for clock region iox
6	RWX	CLOCK_REGION_FASTUNIT1: for clock region iopsi
7	RWX	CLOCK_REGION_UNIT2: for clock region xb
8	RWX	CLOCK_REGION_UNIT3: for clock region unit3 region is UNUSED
9	RWX	CLOCK_REGION_UNIT4: for clock region unit4 region is UNUSED
10	RWX	CLOCK_REGION_UNIT5: for clock region unit5 region is UNUSED
11	RWX	CLOCK_REGION_PLL: for clock region pll region is UNUSED
12:19	RO	Constant = 0b00000000
20	RWX	SEL_THOLD_SL: select sl tholds
21	RWX	SEL_THOLD_NSL: select nsl tholds
22	RWX	SEL_THOLD_ARY: select array thold

Register Name	Scan Region And Type
Mnemonic	EN.PB.TPC.SCANSELQ
Address	0000000004030007 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	Constant = 0b000
3	RW_WCLRPA RT	SCANSEL_CLK_VITL: scan clock region vitl (Vital = Clock)
4	RWX	SCANSEL_CLK_PERV: scan clock region perv (Pervasive)
5	RWX	SCANSEL_CLK_FASTUNIT0: scan clock region iox
6	RWX	SCANSEL_CLK_FASTUNIT1: scan clock region iopsi
7	RWX	SCANSEL_CLK_UNIT2: scan clock region xb
8	RWX	SCANSEL_CLK_UNIT3: scan clock region unit3 region is UNUSED
9	RWX	SCANSEL_CLK_UNIT4: scan clock region unit4 region is UNUSED
10	RWX	SCANSEL_CLK_UNIT5: scan clock region unit5 region is UNUSED
11	RWX	SCANSEL_CLK_PLL: scan clock region pll region is UNUSED
12:19	RO	Constant = 0b00000000
20	RW	SCANSEL_FUNC: scan chain func (functional)
21	RW	SCANSEL_CFG: scan chain mode (boot config and debug config)
22	RW	SCANSEL_CCFG_GPTR: scan chain ccfg / gptra (Pervasive: CC config, Others: GPTR)
23	RW	SCANSEL_REGF: scan chain regf (register files)
24	RW	SCANSEL_LBIST: scan chain lbist (LBIST)
25	RW	SCANSEL_ABIST: scan chain abist (ABIST)
26	RW	SCANSEL_REPR: scan chain repr (Array Repair)
27	RW	SCANSEL_TIME: scan chain time (Array Timing)
28	RW	SCANSEL_BNDY_FARY: scan chain bndy (Boundary I/O's)

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Bits	PCB	Field Mnemonic: Description
29	RW	SCANSEL_FARR: scan chain farr (fast array unload)
30	RW	SCANSEL_CMSK: scan chain cmsk (lbist channel mask)

Register Name	Clocks Running
Mnemonic	EN.PB.TPC.CLOCK_STAT
Address	0000000004030008 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	CLOCK_STATUS_PERV_FUNC_SL: status of perv func_sl_thold 0=run, 1=stop
1	ROX	CLOCK_STATUS_PERV_FUNC_NSL: status of perv func_nsl_thold 0=run, 1=stop
2	ROX	CLOCK_STATUS_PERV_ARY_NSL: status of perv ary_nsl_thold 0=run, 1=stop
3	ROX	CLOCK_STATUS_FASTUNIT0_ODD_FUNC_SL: status of iox_odd func_sl_thold 0=run, 1=stop
4	ROX	CLOCK_STATUS_FASTUNIT0_EVEN_FUNC_SL: status of iox_even func_sl_thold 0=run, 1=stop
5	ROX	CLOCK_STATUS_FASTUNIT0_ODD_FUNC_NSL: status of iox_odd func_nsl_thold 0=run, 1=stop
6	ROX	CLOCK_STATUS_FASTUNIT0_EVEN_FUNC_NSL: status of iox_even func_nsl_thold 0=run, 1=stop
7	ROX	CLOCK_STATUS_FASTUNIT0_ODD_ARY_NSL: status of iox_odd ary_nsl_thold 0=run, 1=stop
8	ROX	CLOCK_STATUS_FASTUNIT0_EVEN_ARY_NSL: status of iox_even ary_nsl_thold 0=run, 1=stop
9	ROX	CLOCK_STATUS_FASTUNIT1_ODD_FUNC_SL: status of iopsi_odd func_sl_thold 0=run, 1=stop
10	ROX	CLOCK_STATUS_FASTUNIT1_EVEN_FUNC_SL: status of iopsi_even func_sl_thold 0=run, 1=stop
11	ROX	CLOCK_STATUS_FASTUNIT1_ODD_FUNC_NSL: status of iopsi_odd func_nsl_thold 0=run, 1=stop
12	ROX	CLOCK_STATUS_FASTUNIT1_EVEN_FUNC_NSL: status of iopsi_even func_nsl_thold 0=run, 1=stop
13	ROX	CLOCK_STATUS_FASTUNIT1_ODD_ARY_NSL: status of iopsi_odd ary_nsl_thold 0=run, 1=stop
14	ROX	CLOCK_STATUS_FASTUNIT1_EVEN_ARY_NSL: status of iopsi_even ary_nsl_thold 0=run, 1=stop
15	ROX	CLOCK_STATUS_UNIT2_FUNC_SL: status of xb func_sl_thold 0=run, 1=stop
16	ROX	CLOCK_STATUS_UNIT2_FUNC_NSL: status of xb func_nsl_thold 0=run, 1=stop
17	ROX	CLOCK_STATUS_UNIT2_ARY_NSL: status of xb ary_nsl_thold 0=run, 1=stop
18	ROX	CLOCK_STATUS_UNIT3_FUNC_SL: status of unit3 func_sl_thold 0=run, 1=stop region is UNUSED
19	ROX	CLOCK_STATUS_UNIT3_FUNC_NSL: status of unit3 func_nsl_thold 0=run, 1=stop region is UNUSED
20	ROX	CLOCK_STATUS_UNIT3_ARY_NSL: status of unit3 ary_nsl_thold 0=run, 1=stop region is UNUSED
21	ROX	CLOCK_STATUS_UNIT4_FUNC_SL: status of unit4 func_sl_thold 0=run, 1=stop region is UNUSED
22	ROX	CLOCK_STATUS_UNIT4_FUNC_NSL: status of unit4 func_nsl_thold 0=run, 1=stop region is UNUSED
23	ROX	CLOCK_STATUS_UNIT4_ARY_NSL: status of unit4 ary_nsl_thold 0=run, 1=stop region is UNUSED
24	ROX	CLOCK_STATUS_UNIT5_FUNC_SL: status of unit5 func_sl_thold 0=run, 1=stop region is UNUSED
25	ROX	CLOCK_STATUS_UNIT5_FUNC_NSL: status of unit5 func_nsl_thold 0=run, 1=stop region is UNUSED
26	ROX	CLOCK_STATUS_UNIT5_ARY_NSL: status of unit5 ary_nsl_thold 0=run, 1=stop region is UNUSED
27	ROX	CLOCK_STATUS_PLL_FUNC_SL: status of pll func_sl_thold 0=run, 1=stop region is UNUSED
28	ROX	CLOCK_STATUS_PLL_FUNC_NSL: status of pll func_nsl_thold 0=run, 1=stop region is UNUSED
29	ROX	CLOCK_STATUS_PLL_ARY_NSL: status of pll ary_nsl_thold 0=run, 1=stop region is UNUSED



Bits	PCB	Field Mnemonic: Description
30:63	RO	Constant = 0b11111111111111111111111111111111

Register Name	Error Status Of CC
Mnemonic	EN.PB.TPC.ERROR_STATUS
Address	0000000004030009 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	PCB_WRITE_NOT_ALLOWED: PCB access error: write not allowed
1	RWX	PCB_READ_NOT_ALLOWED: PCB access error: read not allowed
2	RWX	PCB_PARITY_ERR_ON_CMD: PCB access error: parity error on PCB command
3	RWX	PCB_ADDRESS_NOT_VALID: PCB access error: address not valid
4	RWX	PCB_PARITY_ADDR_ERR: PCB access error: parity error on address
5	RWX	PCB_PARITY_DATA_ERR: PCB access error: parity error on data
6	RWX	PCB_PROTECTED_ACCESS_INVALID: PCB access error: protection violation
7	RWX	PCB_PARITY_SPCIF_ERR: parity error from special packet interface
8	RWX	PCB_WRITE_AND_OPCG: PCB write while opcg in progress
9	RWX	CLOCK_CMD_CONFLICT: clock command conflict: previous one was not yet completed (includes those triggered by tc_sync_clk_stop)
10	RWX	SCAN_COLLISION: scan collision - high when scan protection error occurred
11	RWX	OPCG_TRIGGER_ERROR: opcg triggered while in progress
12	RWX	OPCG_PARITY_ERROR: opcg state machine parity error - during test its OK, but in system its a error
13	RWX	PHASE_CNT_CORRUPTED: phase hold counter corruption detected
14:15	RWX	CC_PAR_ERR: parity error in CC registers (1. opcg & sync config parity error, 2. clock mux parity error)
16	RWX	GPIO_PAR_ERR: parity error in GP0 register
17	RWX	SECURITY_VIOLATION: security_violation - when Chip protection is active and you try a clock start, pulse, which is invalid at this time

Register Name	CC Protect Mode Register
Mnemonic	EN.PB.TPC.CC_PROTECT_MODE_REG
Address	00000000040303FE (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	CC_READ_PROTECT_ENABLE: Enable read protection
1	RW	CC_WRITE_PROTECT_ENABLE: Enable write protection

Registers Specification

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Register Name		Global Checkstop FIR
Mnemonic		EN.PB.TPC.XFIR
Address		0000000004040000 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RWX	XFIR_IN0: summary bit(any xstop)
1	RWX	XFIR_IN1: xstop from other chiplets
2	RWX	XFIR_IN2: Unused
3	RWX	XFIR_IN3: xstop from pervasive unit
4	RWX	XFIR_IN4: xstop from asynchronous PB north (pben)
5	RWX	XFIR_IN5: xstop from I/O unit Xbus(0) POWER8 only
6	RWX	XFIR_IN6: xstop from I/O unit Xbus(1)
7	RWX	XFIR_IN7: xstop from I/O unit Xbus(2) POWER8 only
8	RWX	XFIR_IN8: xstop from I/O unit Xbus(3) POWER8 only
9	RWX	XFIR_IN9: xstop from I/O unit for psi link
10:25	RWX	XFIR_IN10: Unused
26	RWX	XFIR_IN26: xstop on debug trigger

Register Name		Global Recoverable FIR
Mnemonic		EN.PB.TPC.RFIR
Address		0000000004040001 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	ROX	RFIR_IN0: Unused
1	ROX	LFIR_RECOV_ERR: Recoverable error from pervasive unit
2	ROX	RFIR_IN4: recov from asynchronous PB north (pben)
3	ROX	RFIR_IN5: recov from IO unit Xbus(0) POWER8 only
4	ROX	RFIR_IN6: recov from IO unit Xbus(1)
5	ROX	RFIR_IN7: recov from IO unit Xbus(2) POWER8 only
6	ROX	RFIR_IN8: recov from IO unit Xbus(3) POWER8 only
7	ROX	RFIR_IN9: recov from io unit for psi link
8:23	ROX	RFIR_IN10: Unused



Register Name		<i>FIR Mask</i>
Mnemonic		EN.PB.TPC.FIR_MASK
Address		0000000004040002 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RW	FIR_MASK_IN0: mask for xfir summary bit(any xstop)
1	RW	FIR_MASK_IN1: mask for xfir from other chiplets
2	RW	FIR_MASK_IN2: Unused
3	RW	FIR_MASK_IN3: mask for xfir from pervasive unit
4	RW	FIR_MASK_IN4: mask for asynchronous PB north (pben)XFIR and RFIR
5	RW	FIR_MASK_IN5: mask for I/O unit Xbus(0) POWER8 only XFIR and RFIR
6	RW	FIR_MASK_IN6: mask for I/O unit Xbus(1) XFIR and RFIR
7	RW	FIR_MASK_IN7: mask for I/O unit Xbus(2) POWER8 only XFIR and RFIR
8	RW	FIR_MASK_IN8: Mask for I/O unit Xbus(3) POWER8 only XFIR and RFIR
9	RW	FIR_MASK_IN9: Mask for I/O unit for psi link XFIR and RFIR
10:25	RW	FIR_MASK_IN10: Unused
26	RW	FIR_MASK_IN26: Mask for debug trigger

Register Name		<i>Special Attention</i>		
Mnemonic		EN.PB.TPC.SPATTN		
Address		0000000004040004 (PCB) 0000000004040005 (PCB1) 0000000004040006 (PCB2)		
Attributes				
Description				
Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0:9	ROX	NCX	NCX	SPATTN_IN0: Unused special attentions

Register Name		<i>Special Attention Mask</i>
Mnemonic		EN.PB.TPC.SPA_MASK
Address		0000000004040007 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:9	RW	SPA_MASK_IN: Special attention mask

Registers Specification

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Register Name		Mode Register
Mnemonic		EN.PB.TPC.EPS.FIR.MODE_REG
Address		0000000004040008 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RW	MODE_IN0: Enable Clockstop on Checkstop
1	RW	MODE_IN1: Enable Clockstop on Recoverable
2	RW	MODE_IN2: Enable Clockstop on Spattn
3	RW	MODE_IN3: Core-only Spattn
4	RW	MODE_IN4: Stop Chip TOD on Checkstop
5	RW	MODE_IN5: Stop Chip TOD on Recoverable
6	RW	MODE_IN6: Disable propagation of checkstop to other chips
7	RW	MODE_IN7: Turns xstop on trig into clkstp on trig
8	RW	MODE_IN8: Enable xstop on special attention
9	RW	MODE_IN9: mask_direct/local_error
10	RW	MODE_IN10: mask_xstop_to_pcb
11	RW	MODE_IN11: mask external xstop
12:15	RW	MODE_IN: Unused

Register Name		Local FIR		
Mnemonic		EN.PB.TPC.LOCAL_FIR		
Address		000000000404000A (PCB) 000000000404000B (PCB1) 000000000404000C (PCB2)		
Attributes				
Description				
Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_IN0: CFIR internal parity error
1	RWX	WOX_AND	WOX_OR	FIR_IN1: local errors from GPIO (PCB error)
2	RWX	WOX_AND	WOX_OR	FIR_IN2: local errors from CC (PCB error)
3	RWX	WOX_AND	WOX_OR	FIR_IN3: local errors from CC (OPCG, parity, scan collision, ...)
4	RWX	WOX_AND	WOX_OR	FIR_IN4: local errors from PSC (PCB error)
5	RWX	WOX_AND	WOX_OR	FIR_IN5: local errors from PSC (parity error)
6	RWX	WOX_AND	WOX_OR	FIR_IN6: local errors from Thermal (parity error)
7	RWX	WOX_AND	WOX_OR	FIR_IN7: local errors from Thermal (PCB error)
8	RWX	WOX_AND	WOX_OR	FIR_IN8: local errors from Thermal (Trip error critical)
9	RWX	WOX_AND	WOX_OR	FIR_IN9: local errors from Thermal (Trip error fatal)
10:13	RWX	WOX_AND	WOX_OR	FIR_IN10: local errors from Trace Array
14	RWX	WOX_AND	WOX_OR	FIR_IN14: local errors from dcadj



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
15:39	RWX	WOX_AND	WOX_OR	FIR_IN15: unused local errors
40	RWX	WOX_AND	WOX_OR	FIR_IN40: malfunction alert (local xstop in another chiplet)

Register Name	Local FIR Mask			
Mnemonic	EN.PB.TPC.EPS.FIR.LOCAL_FIR_MASK			
Address	000000000404000D (PCB) 000000000404000E (PCB1) 000000000404000F (PCB2)			
Attributes				
Description				

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0:40	RW	WO_AND	WO_OR	LFIR_MASK_IN: mask for LEM error collection vector

Register Name	Local FIR Action0			
Mnemonic	EN.PB.TPC.EPS.FIR.LOCAL_FIR_ACTION0			
Address	0000000004040010 (PCB)			
Attributes				
Description				

Bits	PCB	Field Mnemonic: Description
0:40	RW	FIR_ACTION0_IN: action0 mask

Register Name	Local FIR Action1			
Mnemonic	EN.PB.TPC.EPS.FIR.LOCAL_FIR_ACTION1			
Address	0000000004040011 (PCB)			
Attributes				
Description				

Bits	PCB	Field Mnemonic: Description
0:40	RW	FIR_ACTION1_IN: action1 mask

Register Name	Pervasive FIR Register			
Mnemonic	XBUS01.X0.BUSCTL.SC0M.FIR_REG			
Address	0000000004011000 (SC0M) 0000000004011001 (SC0M1) 0000000004011002 (SC0M2)			
Attributes				
Description	Local FIR register for the chip pervasive logic			

Bits	SC0M	SC0M1	SC0M2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_RX_INVALID_STATE_OR_PARITY_ERROR: FIR Register - A RX state machine parity or mode register parity error has occurred.

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
1	RWX	WOX_AND	WOX_OR	FIR_TX_INVALID_STATE_OR_PARITY_ERROR: FIR Register - A TX state machine parity or mode register parity error has occurred.
2	RWX	WOX_AND	WOX_OR	FIR_GCR_HANG_ERROR: FIR Register - The per-bus GCR ring hang detector error has occurred.
3:7	RWX	WOX_AND	WOX_OR	RESERVED3_7: FIR Register - Reserved.
8	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_TRAINING_ERROR: FIR Register - An Initialization Training error has occurred on Bus0.
9	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_SPARE_DEPLOYED: FIR Register - A Spare lane has been deployed to repair another lane on Bus0.
10	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_MAX_SPARES_EXCEEDED: FIR Register - The maximum number of spare lanes has been exceeded on Bus0. The bus is no longer capable of transferring data.
11	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_RECAL_OR_DYN_REPAIR_ERROR: FIR Register - A bus recal or dynamic repair error has occurred on Bus0.
12	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_TOO_MANY_BUS_ERRORS: FIR Register - A bus has experienced too many random lane errors on Bus0.
13:15	RWX	WOX_AND	WOX_OR	RESERVED13_15: FIR Register - Reserved.
16	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_TRAINING_ERROR: FIR Register - An Initialization Training error has occurred on Bus1.
17	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_SPARE_DEPLOYED: FIR Register - A Spare lane has been deployed to repair another lane on Bus1.
18	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_MAX_SPARES_EXCEEDED: FIR Register - The maximum number of spare lanes has been exceeded on Bus1. The bus is no longer capable of transferring data.
19	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_RECAL_OR_DYN_REPAIR_ERROR: FIR Register - A bus recal or dynamic repair error has occurred on Bus1.
20	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_TOO_MANY_BUS_ERRORS: FIR Register - A bus has experienced too many random lane errors on Bus1.
21:23	RWX	WOX_AND	WOX_OR	RESERVED21_23: FIR Register - Reserved.
24	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_TRAINING_ERROR: FIR Register - An Initialization Training error has occurred on Bus2.
25	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_SPARE_DEPLOYED: FIR Register - A Spare lane has been deployed to repair another lane on Bus2.
26	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_MAX_SPARES_EXCEEDED: FIR Register - The maximum number of spare lanes has been exceeded on Bus2. The bus is no longer capable of transferring data.
27	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_RECAL_OR_DYN_REPAIR_ERROR: FIR Register - A bus recal or dynamic repair error has occurred on Bus2.
28	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_TOO_MANY_BUS_ERRORS: FIR Register - A bus has experienced too many random lane errors on Bus2.
29:31	RWX	WOX_AND	WOX_OR	RESERVED29_31: FIR Register - Reserved.
32	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_TRAINING_ERROR: FIR Register - An Initialization Training error has occurred on Bus3.
33	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_SPARE_DEPLOYED: FIR Register - A Spare lane has been deployed to repair another lane on Bus3.
34	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_MAX_SPARES_EXCEEDED: FIR Register - The maximum number of spare lanes has been exceeded on Bus3. The bus is no longer capable of transferring data.

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
35	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_RECAL_OR_DYN_REPAIR_ERROR: FIR Register - A bus recal or dynamic repair error has occurred on Bus3.
36	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_TOO_MANY_BUS_ERRORS: FIR Register - A bus has experienced too many random lane errors on Bus3.
37:39	RWX	WOX_AND	WOX_OR	RESERVED37_39: FIR Register - Reserved.
40	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_TRAINING_ERROR: FIR Register - An Initialization Training error has occurred on Bus4.
41	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_SPARE_DEPLOYED: FIR Register - A Spare lane has been deployed to repair another lane on Bus4.
42	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_MAX_SPARES_EXCEEDED: FIR Register - The maximum number of spare lanes has been exceeded on Bus4. The bus is no longer capable of transferring data.
43	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_RECAL_OR_DYN_REPAIR_ERROR: FIR Register - A bus recal or dynamic repair error has occurred on Bus4.
44	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_TOO_MANY_BUS_ERRORS: FIR Register - A bus has experienced too many random lane errors on Bus4.
45:47	RWX	WOX_AND	WOX_OR	RESERVED45_47: FIR Register - Reserved.
48	RWX	WOX_AND	WOX_OR	FIR_SCOMFIR_ERROR: FIR Register- A SCOM FSM or FIR register parity error has occurred.
49	RWX	WOX_AND	WOX_OR	FIR_SCOMFIR_ERROR_CLONE: FIR Register- A SCOM FSM or FIR register parity error has occurred.
50:63	RO	N/A	N/A	Constant = 0b0000000000000000

Register Name	<i>Pervasive FIR Mask Register</i>
Mnemonic	XBUS01.X0.BUSCTL.SCOM.FIR_MASK_REG
Address	0000000004011003 (SCOM) 0000000004011004 (SCOM1) 0000000004011005 (SCOM2)
Attributes	
Description	Error mask register (Action0,Mask) = Action Select (0,0) = Recoverable Error (0,1) = Masked

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_RX_INVALID_STATE_OR_PARITY_ERROR_MASK: FIR Register Mask - Mask RX state machine parity or mode register parity error.
1	RWX	WOX_AND	WOX_OR	FIR_TX_INVALID_STATE_OR_PARITY_ERROR_MASK: FIR Register Mask - Mask TX state machine parity or mode register parity error.
2	RWX	WOX_AND	WOX_OR	FIR_GCR_HANG_ERROR_MASK: FIR Register Mask - Mask GCR ring hang detector error.
3:7	RWX	WOX_AND	WOX_OR	RESERVED3_7_MASK: FIR Register - Reserved.
8	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_TRAINING_ERROR_MASK: FIR Register Mask - Mask Initialization Training error on Bus0.
9	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_SPARE_DEPLOYED_MASK: FIR Register Mask - Mask Spare lane has been deployed indication on Bus0.
10	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_MAX_SPARES_EXCEEDED_MASK: FIR Register Mask - Mask maximum number of spare lanes has been exceeded error on Bus0.

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
11	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_RECAL_OR_DYN_REPAIR_ERROR_MASK: FIR Register Mask - Mask bus recal or dynamic repair error on Bus0.
12	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_TOO_MANY_BUS_ERRORS_MASK: FIR Register Mask - Mask too many random lane error on Bus0.
13:15	RWX	WOX_AND	WOX_OR	RESERVED13_15_MASK: FIR Register - Reserved.
16	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_TRAINING_ERROR_MASK: FIR Register Mask - Mask Initialization Training error on Bus1.
17	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_SPARE_DEPLOYED_MASK: FIR Register Mask - Mask Spare lane has been deployed indication on Bus1.
18	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_MAX_SPARES_EXCEEDED_MASK: FIR Register Mask - Mask maximum number of spare lanes has been exceeded error on Bus1.
19	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_RECAL_OR_DYN_REPAIR_ERROR_MASK: FIR Register Mask - Mask bus recal or dynamic repair error on Bus1.
20	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_TOO_MANY_BUS_ERRORS_MASK: FIR Register Mask - Mask too many random lane error on Bus1.
21:23	RWX	WOX_AND	WOX_OR	RESERVED21_23_MASK: FIR Register - Reserved.
24	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_TRAINING_ERROR_MASK: FIR Register Mask - Mask Initialization Training error on Bus2.
25	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_SPARE_DEPLOYED_MASK: FIR Register Mask - Mask Spare lane has been deployed indication on Bus2.
26	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_MAX_SPARES_EXCEEDED_MASK: FIR Register Mask - Mask maximum number of spare lanes has been exceeded error on Bus2.
27	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_RECAL_OR_DYN_REPAIR_ERROR_MASK: FIR Register Mask - Mask bus recal or dynamic repair error on Bus2.
28	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_TOO_MANY_BUS_ERRORS_MASK: FIR Register Mask - Mask too many random lane error on Bus2.
29:31	RWX	WOX_AND	WOX_OR	RESERVED29_31_MASK: FIR Register - Reserved.
32	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_TRAINING_ERROR_MASK: FIR Register Mask - Mask Initialization Training error on Bus3.
33	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_SPARE_DEPLOYED_MASK: FIR Register Mask - Mask Spare lane has been deployed indication on Bus3.
34	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_MAX_SPARES_EXCEEDED_MASK: FIR Register Mask - Mask maximum number of spare lanes has been exceeded error on Bus3.
35	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_RECAL_OR_DYN_REPAIR_ERROR_MASK: FIR Register Mask - Mask bus recal or dynamic repair error on Bus3.
36	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_TOO_MANY_BUS_ERRORS_MASK: FIR Register Mask - Mask too many random lane error on Bus3.
37:39	RWX	WOX_AND	WOX_OR	RESERVED37_39_MASK: FIR Register - Reserved.
40	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_TRAINING_ERROR_MASK: FIR Register Mask - Mask Initialization Training error on Bus4.
41	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_SPARE_DEPLOYED_MASK: FIR Register Mask - Mask Spare lane has been deployed indication on Bus4.
42	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_MAX_SPARES_EXCEEDED_MASK: FIR Register Mask - Mask maximum number of spare lanes has been exceeded error on Bus4.
43	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_RECAL_OR_DYN_REPAIR_ERROR_MASK: FIR Register Mask - Mask bus recal or dynamic repair error on Bus4.



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
44	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_TOO_MANY_BUS_ERRORS_MASK: FIR Register Mask - Mask too many random lane error on Bus4.
45:47	RWX	WOX_AND	WOX_OR	RESERVED45_47_MASK: FIR Register - Res47ved.
48	RWX	WOX_AND	WOX_OR	INTERNAL_SCOM_ERROR_MASK: Internal SCOM Error Mask
49	RWX	WOX_AND	WOX_OR	INTERNAL_SCOM_ERROR_MASK_CLONE: Internal SCOM Error Mask Clone
50:63	RO	N/A	N/A	Constant = 0b0000000000000000

Register Name	<i>Pervasive FIR Register</i>
Mnemonic	XBUS01.X1.BUSCTL.SCOM.FIR_REG
Address	0000000004011400 (SCOM) 0000000004011401 (SCOM1) 0000000004011402 (SCOM2)
Attributes	
Description	Local FIR register for the chip pervasive logic

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_RX_INVALID_STATE_OR_PARITY_ERROR: FIR Register - A RX state machine parity or mode register parity error has occurred.
1	RWX	WOX_AND	WOX_OR	FIR_TX_INVALID_STATE_OR_PARITY_ERROR: FIR Register - A TX state machine parity or mode register parity error has occurred.
2	RWX	WOX_AND	WOX_OR	FIR_GCR_HANG_ERROR: FIR Register - The per-bus GCR ring hang detector error has occurred.
3:7	RWX	WOX_AND	WOX_OR	RESERVED3_7: FIR Register - Reserved.
8	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_TRAINING_ERROR: FIR Register - An Initialization Training error has occurred on Bus0.
9	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_SPARE_DEPLOYED: FIR Register - A Spare lane has been deployed to repair another lane on Bus0.
10	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_MAX_SPARES_EXCEEDED: FIR Register - The maximum number of spare lanes has been exceeded on Bus0. The bus is no longer capable of transferring data.
11	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_RECAL_OR_DYN_REPAIR_ERROR: FIR Register - A bus recal or dynamic repair error has occurred on Bus0.
12	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_TOO_MANY_BUS_ERRORS: FIR Register - A bus has experienced too many random lane errors on Bus0.
13:15	RWX	WOX_AND	WOX_OR	RESERVED13_15: FIR Register - Reserved.
16	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_TRAINING_ERROR: FIR Register - An Initialization Training error has occurred on Bus1.
17	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_SPARE_DEPLOYED: FIR Register - A Spare lane has been deployed to repair another lane on Bus1.
18	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_MAX_SPARES_EXCEEDED: FIR Register - The maximum number of spare lanes has been exceeded on Bus1. The bus is no longer capable of transferring data.
19	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_RECAL_OR_DYN_REPAIR_ERROR: FIR Register - A bus recal or dynamic repair error has occurred on Bus1.

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
20	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_TOO_MANY_BUS_ERRORS: FIR Register - A bus has experienced too many random lane errors on Bus1.
21:23	RWX	WOX_AND	WOX_OR	RESERVED21_23: FIR Register - Reserved.
24	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_TRAINING_ERROR: FIR Register - An Initialization Training error has occurred on Bus2.
25	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_SPARE_DEPLOYED: FIR Register - A Spare lane has been deployed to repair another lane on Bus2.
26	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_MAX_SPARES_EXCEEDED: FIR Register - The maximum number of spare lanes has been exceeded on Bus2. The bus is no longer capable of transferring data.
27	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_RECAL_OR_DYN_REPAIR_ERROR: FIR Register - A bus recal or dynamic repair error has occurred on Bus2.
28	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_TOO_MANY_BUS_ERRORS: FIR Register - A bus has experienced too many random lane errors on Bus2.
29:31	RWX	WOX_AND	WOX_OR	RESERVED29_31: FIR Register - Reserved.
32	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_TRAINING_ERROR: FIR Register - An Initialization Training error has occurred on Bus3.
33	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_SPARE_DEPLOYED: FIR Register - A Spare lane has been deployed to repair another lane on Bus3.
34	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_MAX_SPARES_EXCEEDED: FIR Register - The maximum number of spare lanes has been exceeded on Bus3. The bus is no longer capable of transferring data.
35	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_RECAL_OR_DYN_REPAIR_ERROR: FIR Register - A bus recal or dynamic repair error has occurred on Bus3.
36	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_TOO_MANY_BUS_ERRORS: FIR Register - A bus has experienced too many random lane errors on Bus3.
37:39	RWX	WOX_AND	WOX_OR	RESERVED37_39: FIR Register - Reserved.
40	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_TRAINING_ERROR: FIR Register - An Initialization Training error has occurred on Bus4.
41	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_SPARE_DEPLOYED: FIR Register - A Spare lane has been deployed to repair another lane on Bus4.
42	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_MAX_SPARES_EXCEEDED: FIR Register - The maximum number of spare lanes has been exceeded on Bus4. The bus is no longer capable of transferring data.
43	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_RECAL_OR_DYN_REPAIR_ERROR: FIR Register - A bus recal or dynamic repair error has occurred on Bus4.
44	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_TOO_MANY_BUS_ERRORS: FIR Register - A bus has experienced too many random lane errors on Bus4.
45:47	RWX	WOX_AND	WOX_OR	RESERVED45_47: FIR Register - Reserved.
48	RWX	WOX_AND	WOX_OR	FIR_SCOMFIR_ERROR: FIR Register- A SCOM FSM or FIR register parity error has occurred.
49	RWX	WOX_AND	WOX_OR	FIR_SCOMFIR_ERROR_CLONE: FIR Register- A SCOM FSM or FIR register parity error has occurred.
50:63	RO	N/A	N/A	Constant = 0b0000000000000000

[illegible]

Register Name	<i>Write Configuration Data To Cpm 0-3</i>
Mnemonic	EN.PB.TPC.EPS.THERM.CPM_CONFIG_WRITE_REG0
Address	0000000004050000 (PCB)
Attributes	
Description	0-11: CPM0, 12-23: CPM1, 24-35: CPM2

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Bits	PCB	Field Mnemonic: Description
0:11	WOX	CPM0_CONFIG_DATA: Address ending in: 0x00 contains CPM0 CONFIG_DATA 0x01 contains CPM0 ENCODED value indicating location of edge in 12-bit sampler 15 means all ones 0 means 0b100000000000 1 means 0b110000000000 2 means 0b111000000000 3 means 0b111100000000 4 means 0b111110000000 5 means 0b111111000000 6 means 0b111111100000 7 means 0b111111110000 8 means 0b111111111000 9 means 0b111111111100 10 means 0b111111111110 11 means 0b111111111111 0x02 contains CPM0 RAW value of the actual 12-bit sampler



Bits	PCB	Field Mnemonic: Description
12:15	N/A	Not implemented.
16:27	WOX	CPM1_CONFIG_DATA: Address ending in: 0x00 contains CPM1 CONFIG_DATA 0x01 contains CPM1 ENCODED value indicating location of edge in 12-bit sampler 15 means all ones 0 means 0b100000000000 1 means 0b110000000000..... 11 means 0b111111111111 0x02 contains CPM1 RAW value of the actual 12-bit sampler CPM1 is only available in EX core chiplets
28:31	N/A	Not implemented.
32:43	WOX	CPM2_CONFIG_DATA: Address ending in: 0x00 contains CPM2 CONFIG_DATA 0x01 contains CPM2 ENCODED value indicating location of edge in 12-bit sampler 15 means all ones 0 means 0b100000000000 1 means 0b110000000000..... 11 means 0b111111111111 0x02 contains CPM2 RAW value of the actual 12-bit sampler CPM2 is only available in EX core chiplets
44:63	N/A	Not implemented..

Register Name	<i>DTS Thermal Sensor Loop1 Results</i>
Mnemonic	EN.PB.TPC.EPS.THERM.DTS_RESULT0
Address	0000000004050000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:15	ROX	DTS_0_RESULT: Calibrated DTS Result of sensor with ID 0.
16:31	ROX	DTS_1_RESULT: Calibrated DTS Result of sensor with ID 1.
32:47	ROX	DTS_2_RESULT: Calibrated DTS Result of sensor with ID 2.
48:63	RO	Constant = 0b0000000000000000

Register Name	<i>Multicast Group 1</i>
Mnemonic	EH.TPCHIP.NET.PCBSLXB.MULTICAST_GROUP_1
Address	00000000040F0001 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	Constant = 0b111
3:5	RW	MULTICAST1_GROUP: multicast group1 setting

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Register Name		Multicast Group 2
Mnemonic		EH.TPCHIP.NET.PCBSLXB.MULTICAST_GROUP_2
Address		00000000040F0002 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:2	RO	Constant = 0b111
3:5	RW	MULTICAST2_GROUP: multicast group2 setting

Register Name		Multicast Group 3
Mnemonic		EH.TPCHIP.NET.PCBSLXB.MULTICAST_GROUP_3
Address		00000000040F0003 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:2	RO	Constant = 0b111
3:5	RW	MULTICAST3_GROUP: multicast group3 setting

Register Name		Multicast Group 4
Mnemonic		EH.TPCHIP.NET.PCBSLXB.MULTICAST_GROUP_4
Address		00000000040F0004 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:2	RO	Constant = 0b111
3:5	RW	MULTICAST4_GROUP: multicast group4 setting

Register Name		GP3 Register (NA In PERV CPLT)		
Mnemonic		EH.TPCHIP.NET.PCBSLXB.GP3_REG		
Address		00000000040F0012 (PCB) 00000000040F0013 (PCB1) 00000000040F0014 (PCB2)		
Attributes				
Description				
Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good.
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset.
2	RWX	RWX_WAND	RWX_WOR	GLSMUX_RESET: Glsmux reset for test purpose and stuck active mesh protection. Notice no clocks in the EX if this bit is set.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Put the DPLL in test mode.



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
4	RWX	RWX_WAND	RWX_WOR	PLL_RST: Put PLL in reset state.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYP: Enable PLL bypass.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pcb_access.)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access.)
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	PM_PI_DECODE: Test override for power management. EX chiplet only.
22	RWX	RWX_WAND	RWX_WOR	RESCLK_DIS: Resonant clocking disable.
23:25	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access.)
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave reports 'Chiplet Offline'.
27	RWX	RWX_WAND	RWX_WOR	TP_LVLTRANS_FENCE: Electrical winkel fence. Mainly used by power management.
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.
29:31	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)

Register Name	<i>Lock Indications From PLLs</i>
Mnemonic	EH.TPCHIP.NET.PCBSLXB.PLL_LOCK_REG
Address	00000000040F0019 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	ROX	Reserved field. (Access type is lock)

Register Name	<i>Hang Pulse Generation Register 0</i>
Mnemonic	EH.TPCHIP.NET.PCBSLXB.HANG_PULSE_0_REG
Address	00000000040F0020 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_0: Value of hang pulse 0. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$

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Bits	PCB	Field Mnemonic: Description
6	RW	SUPPRESS_HANG_0: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 6</i>
Mnemonic	EH.TPCHIP.NET.PCBSLXB.HANG_PULSE_6_REG
Address	00000000040F0026 (PCB)
Attributes	
Description	This hang counter is exclusively used for the heartbeat generation

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_6: Value of hang pulse 6. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_6: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Divider For Hang Counter Clock</i>
Mnemonic	EH.TPCHIP.NET.PCBSLXB.PRE_COUNTER_REG
Address	00000000040F0028 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PRE_COUNTER: Divider for hang counter clock. Divides clock by n+1 (default: n=0)

Register Name	<i>GP Register 1</i>
Mnemonic	ES.PBES_WRAP_TOP.TPC.GP1
Address	0000000008000001 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	PBES_TC_ABIST_DONE_DC: Processor Bus Asynchronous South Complex ABIST done. Reset (0).
1	ROX	NOT_USED20: Not used. Reset (0).
2	ROX	NOT_USED21: Not used. Reset (0).
3	ROX	TRA_TC_ABIST_DONE_DC: Processor Bus Async South Trace Array ABIST done. Reset (0).
4	ROX	NOT_USED22: Not used. Reset (0).
5	ROX	NOT_USED23: Not used. Reset (0).
6	ROX	NOT_USED24: Not used. Reset (0).
7	ROX	NOT_USED25: Not used. Reset (0).
8	ROX	NOT_USED26: Not used. Reset (0).
9	ROX	NOT_USED27: Not used. Reset (0).
10	ROX	NOT_USED28: Not used. Reset (0).



Bits	PCB	Field Mnemonic: Description
11	ROX	NOT_USED29: Not used. Reset (0).
12	ROX	NOT_USED30: Not used. Reset (0).
13	ROX	NOT_USED31: Not used. Reset (0).
14	ROX	NOT_USED32: Not used. Reset (0).
15	ROX	TC_OPCG_DONE_DC: Clock control OPCG done. Reset (0).
16	ROX	FREE_USAGE0: Chiplet specific. Reset (0).
17	ROX	FREE_USAGE1: Chiplet specific. Reset (0).
18	ROX	FREE_USAGE2: Chiplet specific. Reset (0).
19	ROX	FREE_USAGE3: Chiplet specific. Reset (0).
20	ROX	FREE_USAGE4: Chiplet specific. Reset (0).
21	ROX	FREE_USAGE5: Chiplet specific. Reset (0).
22	ROX	FREE_USAGE6: Chiplet specific. Reset (0).
23	ROX	FREE_USAGE7: Chiplet specific. Reset (0).

Register Name		GP Register 2
Mnemonic		ES.PBES_WRAP_TOP.TPC.GP2
Address		0000000008000002 (PCB)
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:23	RW	GPIN_MASKING: GPIN bit-wise interrupt masking

Register Name		PSCOMLE Mode Register
Mnemonic		ES.PBES_WRAP_TOP.TPC.EPS.PSC.PSCOM_MODE_REG
Address		0000000008010000 (PCB)
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	RW	ABORT_ON_PCB_ADDR_PARITY_ERROR: abort_on_PCB_addr_parity_error
1	RW	ABORT_ON_PCB_WDATA_PARITY_ERROR: abort_on_PCB_wdata_parity_error
2	RW	ABORT_ON_DL_RETURN_P0_ERROR: abort_on_DL_return_P0_error
3	RW	ABORT_ON_DL_RETURN_WDATA_PARITY_ERROR: abort_on_DL_return_wdata_parity_error
4	RW	WATCHDOG_ENABLE: watchdog_enable
5:6	RW	SCOM_HANG_LIMIT: 0b11: 256 0b10: 512 0b01: 768 0b00: 1023
7	RW	FORCE_ALL_RINGS: Set to logic 1, if all rings should be enabled independent of ring address.



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Bits	PCB	Field Mnemonic: Description
8	RW	FSM_SELFRESET_ON_STATEVEC_PARITYERROR_ENABLE: fsm_selfreset_on_statevec_parityerror_enable
9:11	RW	RESERVED_PSCOM_MODE_LT: Reserved

Register Name	<i>Debug Status Register</i>
Mnemonic	ES.PBES_WRAP_TOP.TPC.EPS.PSC.DEBUG_STATUS_REG
Address	0000000008010004 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	LOCAL_TRACE_RUN_IN: local trace run
1:2	RWX	TRACE_STATE_LAT: trace state latch
3	RWX	TRACE_FREEZE: trace freeze
4:5	RWX	COND3_STATE_LT: condition 3 state latch
6:7	RWX	COND5_STATE_LT: condition 5 state latch
8	RWX	HISTORY_CONDITION0_LT: condition event history for condition0_lt
9	RWX	HISTORY_CONDITION1_LT: condition event history for condition1_lt
10	RWX	HISTORY_COND2_3_EVENT: condition event history for cond2_3_event
11	RWX	HISTORY_COND2_TIMEOUT: condition event history for cond2_timeout
12	RWX	HISTORY_COND4_5_EVENT: condition event history for cond4_5_event
13	RWX	HISTORY_COND4_TIMEOUT: condition event history for cond4_timeout
14:15	RWX	RESERVED_TCDBG_STATUS_LT: reserved, set to zero

Register Name	<i>Trace Array High Data Register</i>
Mnemonic	ES.PBES_WRAP_TOP.TPC.TRA.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG
Address	0000000008010400 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63

Register Name	<i>Trace Array Low Data Register</i>
Mnemonic	ES.PBES_WRAP_TOP.TPC.TRA.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG
Address	0000000008010401 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95



Bits	SCOM	Field Mnemonic: Description
32:41	ROX	TRACE_ADDRESS: Trace Address
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank
51	ROX	TRACE_LAST_BANK_VALID: Trace Last Bank Valid
52	ROX	TRACE_WRITE_ON_RUN: Trace Write-On-Run indicator
53	ROX	TRACE_RUNNING: Trace Run indicator
54:63	ROX	TRACE_HOLD_ADDRESS: Trace Hold Address (pointing to last entry)

Register Name	OPCG Control Register 0
Mnemonic	ES.PBES_WRAP_TOP.TPC.OPCG_REG0
Address	0000000008030002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	RUNN_MODE: runn-mode if 1 or BIST mode if 0
1	RWX	OPCG_GO: opcg go (start sequence)
2	RWX	RUN_SCAN0: run scan0 (will override all BIST mode settings but the scan_ratio)
3	RW	SCAN0_MODE: set PRPGs in scan0_mode but do not run automatic scan0 sequence
4:8	RW	SCAN_RATIO: scan_ratio (n = 0-15: (n+1):1, 16: 24:1, 17: 32:1, 18: 48:1, 19: 64:1, 20: 128:1)
9	RW	INOP_FORCE_SG: Set SG high during INOP
10:13	RW	INOP_ALIGN: INOP phase alignment (0: none, 1: 2:1, 2: 3:1, 3: 4:1, 4: 6:1, 5: 8:1, 6: 12:1, 7: 16:1, 8: 24:1)
14:20	RW	INOP_WAIT: INOP cycle delay (1-127)
21:24	RWX	SNOP_ALIGN: BIST mode: SNOP phase alignment (like INOP), runn-mode: loopcnt(0:3)
25:27	RWX	SNOP_WAIT: BIST mode: SNOP cycle delay (0-7), run-mode: loopcnt(4:6)
28:31	RWX	ENOP_ALIGN: BIST mode: ENOP phase alignment (like INOP), runn-mode: loopcnt(7:10)
32:34	RWX	ENOP_WAIT: BIST mode: ENOP cycle delay (0-7), runn-mode: loopcnt(11:13)
35	RWX	ENOP_FORCE_SG: BIST mode: Set SG high during ENOP, runn-mode: loopcnt(14)
36:63	RWX	LOOP_COUNT: BIST mode: loop count (l = 1-2 ²⁸ (about 5 minutes LBIST)), runn-mode: loopcnt(15:42)

Register Name	OPCG Control Register 1
Mnemonic	ES.PBES_WRAP_TOP.TPC.OPCG_REG1
Address	0000000008030003 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	FUNC_CAPT_COUNT: BIST mode: capture cycles (1-12) encoded as capture cycle - 1
4:8	RW	FUNC_CAPT_SEQ01_01F: BIST mode: capture cycle 1 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
9:13	RW	FUNC_CAPT_SEQ02_02F: BIST mode: capture cycle 2 for fast domain or single mesh support(sl, nsl, ary, sg, fce)

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Bits	PCB	Field Mnemonic: Description
14:18	RW	FUNC_CAPT_SEQ03_03F: BIST mode: capture cycle 3 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
19:23	RW	FUNC_CAPT_SEQ04_04F: BIST mode: capture cycle 4 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
24:28	RW	FUNC_CAPT_SEQ05_05F: BIST mode: capture cycle 5 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
29:33	RW	FUNC_CAPT_SEQ06_06F: BIST mode: capture cycle 6 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
34:38	RW	FUNC_CAPT_SEQ07_07F: BIST mode: capture cycle 7 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
39:43	RW	FUNC_CAPT_SEQ08_08F: BIST mode: capture cycle 8 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
44:48	RW	FUNC_CAPT_SEQ09_01FBY2: BIST mode: capture cycle 1 for slow domain or cycle 9 for single mesh support(sl, nsl, ary, sg, fce)
49:53	RW	FUNC_CAPT_SEQ10_02FBY2: BIST mode: capture cycle 2 for slow domain or cycle 10 for single mesh support(sl, nsl, ary, sg, fce)
54:58	RW	FUNC_CAPT_SEQ11_03FBY2: BIST mode: capture cycle 3 for slow domain or cycle 11 for single mesh support(sl, nsl, ary, sg, fce)
59:63	RW	FUNC_CAPT_SEQ12_04FBY2: BIST mode: capture cycle 4 for slow domain or cycle 12 for single mesh support(sl, nsl, ary, sg, fce)

Register Name	OPCG Control Register 2
Mnemonic	ES.PBES_WRAP_TOP.TPC.OPCG_REG2
Address	0000000008030004 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:11	RW	SCAN_COUNT: BIST mode: Channel scan count (s = 0-4095) runn-mode: start_abist match value(0:11)
12:23	RW	MISR_A_VAL: BIST mode: a value for MISR aperture, runn-mode: start_abist match value(12:23)
24:35	RW	MISR_B_VAL: BIST mode: b value for MISR aperture, runn-mode: start_abist match value(24:35)
36:47	RW	MISR_INIT_WAIT: BIST mode: delay MISR aperture, MISRs get active after this number of loops
48	RW	OPCG_SUPPRESS_EVEN_CLK: OPCG will only create even and not odd clocks. Used for runn to create only one clock in fast domain. Default is 0
49:51	RW	OPCG_PAD_VALUE: After setting all DC signals, wait this many number of cycle x 16 before applying tholds
52	RW	USE_F_AND_FDIV2: BIST mode: if 1, use 8 f and 4 f/2 pattern concurrently, else use 1-12 local mesh patterns
53	RW	USE_ARY_CLK_DURING_FILL: BIST mode: Fire nsl_ary_clock during NSL-fill runn-mode: stop run-n on xstop
54	RW	SG_HIGH_DURING_FILL: BIST mode: Hold SG high during NSL-fill runn-mode: OPCG engine controls start_abist (overrides GP0 setting)
55	RW	RTIM_THOLD_FORCE: force rtim_thold low when not in test_dc mode (must be 0 at all time)
56	RW	LBIST_SKITTER_CTL: BIST mode: 0: enable skitter during lbist_ip, 1: enable skitter when misr_active
57	RW	MISR_MODE: BIST mode: MISR aperture mode (0: a-1 to b-1, 1: start to a and b to end)



Bits	PCB	Field Mnemonic: Description
58	RW	INFINITE_MODE: infinite mode
59:63	RW	NSL_FILL_COUNT: BIST mode: NSL-fill count (0-31)

Register Name	<i>Opcg Start Register</i>
Mnemonic	ES.PBES_WRAP_TOP.TPC.OPCG_REG3
Address	0000000008030005 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	OPCG_GO2: opcg go for broadcast sequences (start sequence).
1	RW	RUN_OPCG_ON_UPDATE_DR: start opcg engine when scan updated (update_dr) received (set pulse).
2	RW	RUN_OPCG_ON_CAPTURE_DR: Start opcg engine when scan updated (capture_dr) received (set pulse).
3:4	RW	ALIGN_SOURCE_SELECT: 0: Use inopa setting from opcg_reg0 1: use rising edge of sync pulse 2: use input from unit (for AVP)
5:7	RW	PRPG_WEIGHTING: prpg_activate: 1/2, 1/4, 1/8, 1/16, 1/2, 3/4, 7/8, 15/16
8:19	RWX	PRPG_VALUE: Set to 0 for prpg always on, else seed.
20	RW	EXTEND_INOPW_ENOPW: extend I/ENOPW: add 256 cycles if i/enop>0, else 257+max i/enop.
21	RW	EXTEND_SNOPW: Add 256 cycles if snop>0, else 257+max snop.
22	RW	FORCE_SG_HIGH_DURING_SNOP: Force sg high during snop.
23:31	RW	CHKSW: Reserved for debug switches (keep 0 unless chksw required).
32:43	RW	PRPG_A_VAL: a value for PRPG aperture.
44:55	RW	PRPG_B_VAL: b value for PRPG aperture.
56	RW	PRPG_MODE: PRPG aperture mode (0: a-1 to b-1, 1: start to a and b to end).
57	RW	SCAN_CLK_USE_EVEN: Generate scan clock in odd cycle instead of even. Default is 0.
58	RWX	AUTO_SCAN0: Runs a full scan0 on chiplet to clear all data.
59:63	RW	SPARE3: Spares.

Register Name	<i>Start/stop Of Clocks</i>
Mnemonic	ES.PBES_WRAP_TOP.TPC.CLK_REGION
Address	0000000008030006 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RWX	CLOCK_CMD: command for clock control: 00 NOP 01 START 10 STOP 11 PULSE (one pulse)
2:3	RO	Constant = 0b00
4	RWX	CLOCK_REGION_PERV: for clock region perv (Pervasive)
5	RWX	CLOCK_REGION_UNIT0: for clock region ab

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Bits	PCB	Field Mnemonic: Description
6	RWX	CLOCK_REGION_UNIT1: for clock region ioa
7	RWX	CLOCK_REGION_UNIT2: for clock region unit2 region is UNUSED
8	RWX	CLOCK_REGION_UNIT3: for clock region unit3 region is UNUSED
9	RWX	CLOCK_REGION_UNIT4: for clock region unit4 region is UNUSED
10	RWX	CLOCK_REGION_UNIT5: for clock region unit5 region is UNUSED
11	RWX	CLOCK_REGION_PLL: for clock region pll
12	RWX	CLOCK_REGION_OSCSW: for clock region oscsw region is UNUSED
13:19	RO	Constant = 0b00000000
20	RWX	SEL_THOLD_SL: select sl tholds
21	RWX	SEL_THOLD_NSL: select nsl tholds
22	RWX	SEL_THOLD_ARY: select array thold

Register Name	Scan Region And Type
Mnemonic	ES.PBES_WRAP_TOP.TPC.SCANSELQ
Address	0000000008030007 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	Constant = 0b000
3	RW_WCLRPA RT	SCANSEL_CLK_VITL: scan clock region vitl (Vital = Clock)
4	RWX	SCANSEL_CLK_PERV: scan clock region perv (Pervasive)
5	RWX	SCANSEL_CLK_UNIT0: scan clock region ab
6	RWX	SCANSEL_CLK_UNIT1: scan clock region ioa
7	RWX	SCANSEL_CLK_UNIT2: scan clock region unit2 region is UNUSED
8	RWX	SCANSEL_CLK_UNIT3: scan clock region unit3 region is UNUSED
9	RWX	SCANSEL_CLK_UNIT4: scan clock region unit4 region is UNUSED
10	RWX	SCANSEL_CLK_UNIT5: scan clock region unit5 region is UNUSED
11	RWX	SCANSEL_CLK_PLL: scan clock region pll
12	RWX	SCANSEL_CLK_OSCSW: scan clock region oscsw region is UNUSED
13:19	RO	Constant = 0b00000000
20	RW	SCANSEL_FUNC: scan chain func (functional)
21	RW	SCANSEL_CFG: scan chain mode (boot config and debug config)
22	RW	SCANSEL_CCFG_GPTR: scan chain ccfg / gptra (Pervasive: CC config, Others: GPTR)
23	RW	SCANSEL_REGF: scan chain regf (register files)
24	RW	SCANSEL_LBIST: scan chain lbist (LBIST)
25	RW	SCANSEL_ABIST: scan chain abst (ABIST)
26	RW	SCANSEL_REPR: scan chain repr (Array Repair)
27	RW	SCANSEL_TIME: scan chain time (Array Timing)



Bits	PCB	Field Mnemonic: Description
28	RW	SCANSEL_BNDY: scan chain bndy (Boundary I/O's)
29	RW	SCANSEL_FARR: scan chain farr (fast array unload)
30	RW	SCANSEL_CMSK: scan chain cmsk (lbist channel mask)

Register Name	<i>Clocks Running</i>
Mnemonic	ES.PBES_WRAP_TOP.TPC.CLOCK_STAT
Address	0000000008030008 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	CLOCK_STATUS_PERV_FUNC_SL: status of perv func_sl_thold 0=run, 1=stop
1	ROX	CLOCK_STATUS_PERV_FUNC_NSL: status of perv func_nsl_thold 0=run, 1=stop
2	ROX	CLOCK_STATUS_PERV_ARY_NSL: status of perv ary_nsl_thold 0=run, 1=stop
3	ROX	CLOCK_STATUS_UNIT0_FUNC_SL: status of ab func_sl_thold 0=run, 1=stop
4	ROX	CLOCK_STATUS_UNIT0_FUNC_NSL: status of ab func_nsl_thold 0=run, 1=stop
5	ROX	CLOCK_STATUS_UNIT0_ARY_NSL: status of ab ary_nsl_thold 0=run, 1=stop
6	ROX	CLOCK_STATUS_UNIT1_FUNC_SL: status of ioa func_sl_thold 0=run, 1=stop
7	ROX	CLOCK_STATUS_UNIT1_FUNC_NSL: status of ioa func_nsl_thold 0=run, 1=stop
8	ROX	CLOCK_STATUS_UNIT1_ARY_NSL: status of ioa ary_nsl_thold 0=run, 1=stop
9	ROX	CLOCK_STATUS_UNIT2_FUNC_SL: status of unit2 func_sl_thold 0=run, 1=stop region is UNUSED
10	ROX	CLOCK_STATUS_UNIT2_FUNC_NSL: status of unit2 func_nsl_thold 0=run, 1=stop region is UNUSED
11	ROX	CLOCK_STATUS_UNIT2_ARY_NSL: status of unit2 ary_nsl_thold 0=run, 1=stop region is UNUSED
12	ROX	CLOCK_STATUS_UNIT3_FUNC_SL: status of unit3 func_sl_thold 0=run, 1=stop region is UNUSED
13	ROX	CLOCK_STATUS_UNIT3_FUNC_NSL: status of unit3 func_nsl_thold 0=run, 1=stop region is UNUSED
14	ROX	CLOCK_STATUS_UNIT3_ARY_NSL: status of unit3 ary_nsl_thold 0=run, 1=stop region is UNUSED
15	ROX	CLOCK_STATUS_UNIT4_FUNC_SL: status of unit4 func_sl_thold 0=run, 1=stop region is UNUSED
16	ROX	CLOCK_STATUS_UNIT4_FUNC_NSL: status of unit4 func_nsl_thold 0=run, 1=stop region is UNUSED
17	ROX	CLOCK_STATUS_UNIT4_ARY_NSL: status of unit4 ary_nsl_thold 0=run, 1=stop region is UNUSED
18	ROX	CLOCK_STATUS_UNIT5_FUNC_SL: status of unit5 func_sl_thold 0=run, 1=stop region is UNUSED
19	ROX	CLOCK_STATUS_UNIT5_FUNC_NSL: status of unit5 func_nsl_thold 0=run, 1=stop region is UNUSED
20	ROX	CLOCK_STATUS_UNIT5_ARY_NSL: status of unit5 ary_nsl_thold 0=run, 1=stop region is UNUSED
21	ROX	CLOCK_STATUS_PLL_FUNC_SL: status of pll func_sl_thold 0=run, 1=stop
22	ROX	CLOCK_STATUS_PLL_FUNC_NSL: status of pll func_nsl_thold 0=run, 1=stop
23	ROX	CLOCK_STATUS_PLL_ARY_NSL: status of pll ary_nsl_thold 0=run, 1=stop
24	ROX	CLOCK_STATUS_OSCSW_FUNC_SL: status of oscsw func_sl_thold 0=run, 1=stop region is UNUSED
25	ROX	CLOCK_STATUS_OSCSW_FUNC_NSL: status of oscsw func_nsl_thold 0=run, 1=stop region is UNUSED
26	ROX	CLOCK_STATUS_OSCSW_ARY_NSL: status of oscsw ary_nsl_thold 0=run, 1=stop region is UNUSED
27:63	RO	Constant = 0b111111111111111111111111111111111111111111111111111

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Register Name		Error Status Of CC
Mnemonic		ES.PBES_WRAP_TOP.TPC.ERROR_STATUS
Address		0000000008030009 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RWX	PCB_WRITE_NOT_ALLOWED: PCB access error: write not allowed
1	RWX	PCB_READ_NOT_ALLOWED: PCB access error: read not allowed
2	RWX	PCB_PARITY_ERR_ON_CMD: PCB access error: parity error on PCB command
3	RWX	PCB_ADDRESS_NOT_VALID: PCB access error: address not valid
4	RWX	PCB_PARITY_ADDR_ERR: PCB access error: parity error on address
5	RWX	PCB_PARITY_DATA_ERR: PCB access error: parity error on data
6	RWX	PCB_PROTECTED_ACCESS_INVALID: PCB access error: protection violation
7	RWX	PCB_PARITY_SPCIF_ERR: parity error from special packet interface
8	RWX	PCB_WRITE_AND_OPCG: PCB write while opcg in progress
9	RWX	CLOCK_CMD_CONFLICT: clock command conflict: previous one was not yet completed (includes those triggered by tc_sync_clk_stop)
10	RWX	SCAN_COLLISION: scan collision
11	RWX	OPCG_TRIGGER_ERROR: opcg triggered while in progress
12	RWX	OPCG_PARITY_ERROR: opcg state machine parity error
13	RWX	PHASE_CNT_CORRUPTED: phase hold counter corruption detected
14:15	RWX	CC_PAR_ERR: parity error in CC registers (1. opcg & sync config parity error, 2. clock mux parity error)
16	RWX	GPIO_PAR_ERR: parity error in GP0 register
17	RWX	SECURITY_VIOLATION: security_violation - when Chip protection is active and you try a clock start, pulse, which is invalid at this time

Register Name		CC Protect Mode Register
Mnemonic		ES.PBES_WRAP_TOP.TPC.CC_PROTECT_MODE_REG
Address		00000000080303FE (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RW	CC_READ_PROTECT_ENABLE: Enable read protection
1	RW	CC_WRITE_PROTECT_ENABLE: Enable write protection



Register Name		Global Checkstop FIR
Mnemonic		ES.PBES_WRAP_TOP.TPC.XFIR
Address		0000000008040000 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RWX	XFIR_IN0: summary bit(any xstop)
1	RWX	XFIR_IN1: xstop from other chiplets
2	RWX	XFIR_IN2: Unused
3	RWX	XFIR_IN3: xstop from pervasive unit
4	RWX	XFIR_IN4: xstop from pbes
5	RWX	XFIR_IN5: xstop from I/O unit A bus
6:25	RWX	XFIR_IN6: Unused
26	RWX	XFIR_IN26: xstop on debug trigger

Register Name		Global Recoverable FIR
Mnemonic		ES.PBES_WRAP_TOP.TPC.RFIR
Address		0000000008040001 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	ROX	RFIR_IN0: Unused
1	ROX	LFIR_RECOV_ERR: Recoverable error from pervasive unit
2	ROX	RFIR_IN2: Recoverable error from pbes
3	ROX	RFIR_IN3: Recoverable error from I/O unit a bus
4:23	ROX	RFIR_IN_UNUSED: Unused

Register Name		FIR Mask
Mnemonic		ES.PBES_WRAP_TOP.TPC.FIR_MASK
Address		0000000008040002 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RW	FIR_MASK_IN0: Mask for xfir summary bit(any xstop)
1	RW	FIR_MASK_IN1: Mask for xfir other chiplets
2	RW	FIR_MASK_IN2: Unused
3	RW	FIR_MASK_IN3: Mask for xfir from pervasive unit error
4	RW	FIR_MASK_IN4: Mask for pbes XFIR and RFIR
5	RW	FIR_MASK_IN5: Mask for I/O unit a bus XFIR and RFIR

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Bits	PCB	Field Mnemonic: Description
6:25	RW	FIR_MASK_IN6: Unused
26	RW	FIR_MASK_IN26: Mask for debug trigger

Register Name	<i>Special Attention</i>			
Mnemonic	ES.PBES_WRAP_TOP.TPC.SPATTN			
Address	0000000008040004 (PCB) 0000000008040005 (PCB1) 0000000008040006 (PCB2)			
Attributes				
Description				

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0:9	ROX	NCX	NCX	SPATTN_IN0: unused special attentions

Register Name	<i>Special Attention Mask</i>			
Mnemonic	ES.PBES_WRAP_TOP.TPC.SPA_MASK			
Address	0000000008040007 (PCB)			
Attributes				
Description				

Bits	PCB	Field Mnemonic: Description
0:9	RW	SPA_MASK_IN: special attention mask

Register Name	<i>Mode Register</i>			
Mnemonic	ES.PBES_WRAP_TOP.TPC.EPS.FIR.MODE_REG			
Address	0000000008040008 (PCB)			
Attributes				
Description				

Bits	PCB	Field Mnemonic: Description
0	RW	MODE_IN0: Enable Clockstop on Checkstop
1	RW	MODE_IN1: Enable Clockstop on Recoverable
2	RW	MODE_IN2: Enable Clockstop on Spattn
3	RW	MODE_IN3: Core-only Spattn
4	RW	MODE_IN4: Stop Chip TOD on Checkstop
5	RW	MODE_IN5: Stop Chip TOD on Recoverable
6	RW	MODE_IN6: Disable propagation of checkstop to other chips
7	RW	MODE_IN7: turns xstop on trig into clkstp on trig
8	RW	MODE_IN8: enable xstop on special attention
9	RW	MODE_IN9: mask_direct/local_error
10	RW	MODE_IN10: mask_xstop_to_pcb



Bits	PCB	Field Mnemonic: Description
11	RW	MODE_IN11: mask external xstop
12:15	RW	MODE_IN: unused

Register Name	Local FIR
Mnemonic	ES.PBES_WRAP_TOP.TPC.LOCAL_FIR
Address	000000000804000A (PCB) 000000000804000B (PCB1) 000000000804000C (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_IN0: CFIR internal parity error
1	RWX	WOX_AND	WOX_OR	FIR_IN1: local errors from GPIO (PCB error)
2	RWX	WOX_AND	WOX_OR	FIR_IN2: local errors from CC (PCB error)
3	RWX	WOX_AND	WOX_OR	FIR_IN3: local errors from CC (OPCG, parity, scan collision, ...)
4	RWX	WOX_AND	WOX_OR	FIR_IN4: local errors from PSC (PCB error)
5	RWX	WOX_AND	WOX_OR	FIR_IN5: local errors from PSC (parity error)
6	RWX	WOX_AND	WOX_OR	FIR_IN6: local errors from Thermal (parity error)
7	RWX	WOX_AND	WOX_OR	FIR_IN7: local errors from Thermal (PCB error)
8	RWX	WOX_AND	WOX_OR	FIR_IN8: local errors from Thermal (Trip error critical)
9	RWX	WOX_AND	WOX_OR	FIR_IN9: local errors from Thermal (Trip error fatal)
10	RWX	WOX_AND	WOX_OR	FIR_IN10: local errors from Trace Array (error)
11	RWX	WOX_AND	WOX_OR	FIR_IN11: local errors from Trace Array (scom error)
12:39	RWX	WOX_AND	WOX_OR	FIR_IN12: unused local errors
40	RWX	WOX_AND	WOX_OR	FIR_IN40: malfunction alert (local xstop in another chiplet)

Register Name	Local FIR Mask
Mnemonic	ES.PBES_WRAP_TOP.TPC.EPS.FIR.LOCAL_FIR_MASK
Address	000000000804000D (PCB) 000000000804000E (PCB1) 000000000804000F (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0:40	RW	WO_AND	WO_OR	LFIR_MASK_IN: mask for LEM error collection vector

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Register Name		Local FIR Action0
Mnemonic		ES.PBES_WRAP_TOP.TPC.EPS.FIR.LOCAL_FIR_ACTION0
Address		0000000008040010 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:40	RW	FIR_ACTION0_IN: action0 mask

Register Name		Local FIR Action1
Mnemonic		ES.PBES_WRAP_TOP.TPC.EPS.FIR.LOCAL_FIR_ACTION1
Address		0000000008040011 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:40	RW	FIR_ACTION1_IN: action1 mask

Register Name		Pervasive FIR Register		
Mnemonic		ABUS.BUSCTL.SCOM.FIR_REG		
Address		0000000008010C00 (SCOM) 0000000008010C01 (SCOM1) 0000000008010C02 (SCOM2)		
Attributes				
Description		Local FIR register for the chip pervasive logic		
Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_RX_INVALID_STATE_OR_PARITY_ERROR: FIR Register - A RX state machine parity or mode register parity error has occurred.
1	RWX	WOX_AND	WOX_OR	FIR_TX_INVALID_STATE_OR_PARITY_ERROR: FIR Register - A TX state machine parity or mode register parity error has occurred.
2	RWX	WOX_AND	WOX_OR	FIR_GCR_HANG_ERROR: FIR Register - The per-bus GCR ring hang detector error has occurred.
3:7	RWX	WOX_AND	WOX_OR	RESERVED3_7: FIR Register - Reserved.
8	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_TRAINING_ERROR: FIR Register - An Initialization Training error has occurred on Bus0.
9	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_SPARE_DEPLOYED: FIR Register - A Spare lane has been deployed to repair another lane on Bus0.
10	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_MAX_SPARES_EXCEEDED: FIR Register - The maximum number of spare lanes has been exceeded on Bus0. The bus is no longer capable of transferring data.
11	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_RECAL_OR_DYN_REPAIR_ERROR: FIR Register - A bus recal or dynamic repair error has occurred on Bus0.
12	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_TOO_MANY_BUS_ERRORS: FIR Register - A bus has experienced too many random lane errors on Bus0.
13:15	RWX	WOX_AND	WOX_OR	RESERVED13_15: FIR Register - Reserved.



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
16	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_TRAINING_ERROR: FIR Register - An Initialization Training error has occurred on Bus1.
17	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_SPARE_DEPLOYED: FIR Register - A Spare lane has been deployed to repair another lane on Bus1.
18	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_MAX_SPARES_EXCEEDED: FIR Register - The maximum number of spare lanes has been exceeded on Bus1. The bus is no longer capable of transferring data.
19	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_RECAL_OR_DYN_REPAIR_ERROR: FIR Register - A bus recal or dynamic repair error has occurred on Bus1.
20	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_TOO_MANY_BUS_ERRORS: FIR Register - A bus has experienced too many random lane errors on Bus1.
21:23	RWX	WOX_AND	WOX_OR	RESERVED21_23: FIR Register - Reserved.
24	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_TRAINING_ERROR: FIR Register - An Initialization Training error has occurred on Bus2.
25	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_SPARE_DEPLOYED: FIR Register - A Spare lane has been deployed to repair another lane on Bus2.
26	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_MAX_SPARES_EXCEEDED: FIR Register - The maximum number of spare lanes has been exceeded on Bus2. The bus is no longer capable of transferring data.
27	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_RECAL_OR_DYN_REPAIR_ERROR: FIR Register - A bus recal or dynamic repair error has occurred on Bus2.
28	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_TOO_MANY_BUS_ERRORS: FIR Register - A bus has experienced too many random lane errors on Bus2.
29:31	RWX	WOX_AND	WOX_OR	RESERVED29_31: FIR Register - Reserved.
32	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_TRAINING_ERROR: FIR Register - An Initialization Training error has occurred on Bus3.
33	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_SPARE_DEPLOYED: FIR Register - A Spare lane has been deployed to repair another lane on Bus3.
34	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_MAX_SPARES_EXCEEDED: FIR Register - The maximum number of spare lanes has been exceeded on Bus3. The bus is no longer capable of transferring data.
35	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_RECAL_OR_DYN_REPAIR_ERROR: FIR Register - A bus recal or dynamic repair error has occurred on Bus3.
36	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_TOO_MANY_BUS_ERRORS: FIR Register - A bus has experienced too many random lane errors on Bus3.
37:39	RWX	WOX_AND	WOX_OR	RESERVED37_39: FIR Register - Reserved.
40	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_TRAINING_ERROR: FIR Register - An Initialization Training error has occurred on Bus4.
41	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_SPARE_DEPLOYED: FIR Register - A Spare lane has been deployed to repair another lane on Bus4.
42	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_MAX_SPARES_EXCEEDED: FIR Register - The maximum number of spare lanes has been exceeded on Bus4. The bus is no longer capable of transferring data.
43	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_RECAL_OR_DYN_REPAIR_ERROR: FIR Register - A bus recal or dynamic repair error has occurred on Bus4.
44	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_TOO_MANY_BUS_ERRORS: FIR Register - A bus has experienced too many random lane errors on Bus4.
45:47	RWX	WOX_AND	WOX_OR	RESERVED45_47: FIR Register - Reserved.

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
48	RWX	WOX_AND	WOX_OR	FIR_SCOMFIR_ERROR: FIR Register- A SCOM FSM or FIR register parity error has occurred.
49	RWX	WOX_AND	WOX_OR	FIR_SCOMFIR_ERROR_CLONE: FIR Register- A SCOM FSM or FIR register parity error has occurred.
50:63	RO	N/A	N/A	Constant = 0b0000000000000000

Register Name	<i>Pervasive FIR Mask Register</i>
Mnemonic	ABUS.BUSCTL.SC.COM.FIR_MASK_REG
Address	0000000008010C03 (SCOM) 0000000008010C04 (SCOM1) 0000000008010C05 (SCOM2)
Attributes	
Description	Error mask register (Action0,Mask) = Action Select (0,0) = Recoverable Error (0,1) = Masked

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_RX_INVALID_STATE_OR_PARITY_ERROR_MASK: FIR Register Mask - Mask RX state machine parity or mode register parity error.
1	RWX	WOX_AND	WOX_OR	FIR_TX_INVALID_STATE_OR_PARITY_ERROR_MASK: FIR Register Mask - Mask TX state machine parity or mode register parity error.
2	RWX	WOX_AND	WOX_OR	FIR_GCR_HANG_ERROR_MASK: FIR Register Mask - Mask GCR ring hang detector error.
3:7	RWX	WOX_AND	WOX_OR	RESERVED3_7_MASK: FIR Register - Reserved.
8	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_TRAINING_ERROR_MASK: FIR Register Mask - Mask Initialization Training error on Bus0.
9	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_SPARE_DEPLOYED_MASK: FIR Register Mask - Mask Spare lane has been deployed indication on Bus0.
10	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_MAX_SPARES_EXCEEDED_MASK: FIR Register Mask - Mask maximum number of spare lanes has been exceeded error on Bus0.
11	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_RECAL_OR_DYN_REPAIR_ERROR_MASK: FIR Register Mask - Mask bus recal or dynamic repair error on Bus0.
12	RWX	WOX_AND	WOX_OR	FIR_RX_BUS0_TOO_MANY_BUS_ERRORS_MASK: FIR Register Mask - Mask too many random lane error on Bus0.
13:15	RWX	WOX_AND	WOX_OR	RESERVED13_15_MASK: FIR Register - Reserved.
16	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_TRAINING_ERROR_MASK: FIR Register Mask - Mask Initialization Training error on Bus1.
17	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_SPARE_DEPLOYED_MASK: FIR Register Mask - Mask Spare lane has been deployed indication on Bus1.
18	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_MAX_SPARES_EXCEEDED_MASK: FIR Register Mask - Mask maximum number of spare lanes has been exceeded error on Bus1.
19	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_RECAL_OR_DYN_REPAIR_ERROR_MASK: FIR Register Mask - Mask bus recal or dynamic repair error on Bus1.
20	RWX	WOX_AND	WOX_OR	FIR_RX_BUS1_TOO_MANY_BUS_ERRORS_MASK: FIR Register Mask - Mask too many random lane error on Bus1.
21:23	RWX	WOX_AND	WOX_OR	RESERVED21_23_MASK: FIR Register - Reserved.
24	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_TRAINING_ERROR_MASK: FIR Register Mask - Mask Initialization Training error on Bus2.



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
25	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_SPARE_DEPLOYED_MASK: FIR Register Mask - Mask Spare lane has been deployed indication on Bus2.
26	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_MAX_SPARES_EXCEEDED_MASK: FIR Register Mask - Mask maximum number of spare lanes has been exceeded error on Bus2.
27	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_RECAL_OR_DYN_REPAIR_ERROR_MASK: FIR Register Mask - Mask bus recal or dynamic repair error on Bus2.
28	RWX	WOX_AND	WOX_OR	FIR_RX_BUS2_TOO_MANY_BUS_ERRORS_MASK: FIR Register Mask - Mask too many random lane error on Bus2.
29:31	RWX	WOX_AND	WOX_OR	RESERVED29_31_MASK: FIR Register - Reserved.
32	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_TRAINING_ERROR_MASK: FIR Register Mask - Mask Initialization Training error on Bus3.
33	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_SPARE_DEPLOYED_MASK: FIR Register Mask - Mask Spare lane has been deployed indication on Bus3.
34	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_MAX_SPARES_EXCEEDED_MASK: FIR Register Mask - Mask maximum number of spare lanes has been exceeded error on Bus3.
35	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_RECAL_OR_DYN_REPAIR_ERROR_MASK: FIR Register Mask - Mask bus recal or dynamic repair error on Bus3.
36	RWX	WOX_AND	WOX_OR	FIR_RX_BUS3_TOO_MANY_BUS_ERRORS_MASK: FIR Register Mask - Mask too many random lane error on Bus3.
37:39	RWX	WOX_AND	WOX_OR	RESERVED37_39_MASK: FIR Register - Reserved.
40	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_TRAINING_ERROR_MASK: FIR Register Mask - Mask Initialization Training error on Bus4.
41	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_SPARE_DEPLOYED_MASK: FIR Register Mask - Mask Spare lane has been deployed indication on Bus4.
42	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_MAX_SPARES_EXCEEDED_MASK: FIR Register Mask - Mask maximum number of spare lanes has been exceeded error on Bus4.
43	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_RECAL_OR_DYN_REPAIR_ERROR_MASK: FIR Register Mask - Mask bus recal or dynamic repair error on Bus4.
44	RWX	WOX_AND	WOX_OR	FIR_RX_BUS4_TOO_MANY_BUS_ERRORS_MASK: FIR Register Mask - Mask too many random lane error on Bus4.
45:47	RWX	WOX_AND	WOX_OR	RESERVED45_47_MASK: FIR Register - Reserved.
48	RWX	WOX_AND	WOX_OR	INTERNAL_SCOM_ERROR_MASK: Internal SCOM Error Mask
49	RWX	WOX_AND	WOX_OR	INTERNAL_SCOM_ERROR_MASK_CLONE: Internal SCOM Error Mask Clone
50:63	RO	N/A	N/A	Constant = 0b0000000000000000

Register Name	Normal SCOM Mode Reg
Mnemonic	ABUS.BUSCTL.SCOM.SCOM_MODE_PB
Address	0000000008010C20 (SCOM)
Attributes	
Description	



Registers Specification

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Bits	SCOM	Field Mnemonic: Description
0	RWX	GCR_TEST_MODE: GCR test mode. Put register logic into GCR test mode, which allows all read/write registers to be read and written by diagnostic code to verify all register accesses. This mode gates off both logic inputs to the registers, as well as the outputs from the logic. The outputs are gated to their scanflush value.
1	RWX	ENABLE_GCR_OFL_BUFF: Enables the second GCR overflow buffer, one is used by default



Bits	SCOM	Field Mnemonic: Description
2:7	RWX	IORESET_HARD_BUS0: I/O hard reset per-bus and GCR reset. Enables a hard reset on bus 0-5 (this is application dependent and bus 1-5 might not be present). A GCR reset affects all buses because any of them might be corrupted. 0b000000 = Functional (default) 0b100000 = Reset Bus 0 0b010000 = Reset Bus 1 0b001000 = Reset Bus 2 0b000100 = Reset Bus 3 0b000010 = Reset Bus 4 0b000001 = Reset Bus 5 0b111111 = Reset all local buses and perform a GCR reset.jfg FUNCTIONAL=>0b000000 RESET0=>0b100000 RESET1=>0b010000 RESET2=>0b001000 RESET3=>0b000100 RESET4=>0b000010 RESET5=>0b000001 RESETGCR=>0b111111
8:10	RWX	GCR_HANG_DET_SEL: GCR hang detect threshold Select
11	ROX	GCR_BUFFER_ENABLED_RO_SIGNAL: 1 when the second GCR buffer is enabled
12	RWX	GCR_HANG_ERROR_MASK: Mask for GCR Hang error when the second buffer is enabled
13	RWX	GCR_HANG_ERROR_INJ: Inject for GCR Hang Error
14:21	RWX	SCOM_MODE_PB_SPARES: SCOM Mode Reg Spares
22:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name		Lock Indications From PLLs
Mnemonic		EH.TPCHIP.NET.PCBSLAB.PLL_LOCK_REG
Address		00000000080F0019 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:3	ROX	Reserved field. (Access type is lock)

Register Name		Write Configuration Data To CPM 0-3
Mnemonic		ES.PBES_WRAP_TOP.TPC.EPS.THERM.CPM_CONFIG_WRITE_REG0
Address		0000000008050000 (PCB)
Attributes		
Description		0-11: CPM0, 12-23: CPM1, 24-35: CPM2

Registers Specification

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Bits	PCB	Field Mnemonic: Description
0:11	WOX	CPM0_CONFIG_DATA: Address ending in: 0x00 contains CPM0 CONFIG_DATA 0x01 contains CPM0 ENCODED value indicating location of edge in 12-bit sampler 15 means all ones 0 means 0b100000000000 1 means 0b110000000000 2 means 0b111000000000 3 means 0b111100000000 4 means 0b111110000000 5 means 0b111111000000 6 means 0b111111100000 7 means 0b111111110000 8 means 0b111111111000 9 means 0b111111111100 10 means 0b111111111110 11 means 0b111111111111 0x02 contains CPM0 RAW value of the actual 12-bit sampler
12:15	N/A	Not implemented.
16:27	WOX	CPM1_CONFIG_DATA: Address ending in: 0x00 contains CPM1 CONFIG_DATA 0x01 contains CPM1 ENCODED value indicating location of edge in 12-bit sampler 15 means all ones 0 means 0b100000000000 1 means 0b110000000000..... 11 means 0b111111111111 0x02 contains CPM1 RAW value of the actual 12-bit sampler CPM1 is only available in EX core chiplets
28:31	N/A	Not implemented.
32:43	WOX	CPM2_CONFIG_DATA: Address ending in: 0x00 contains CPM2 CONFIG_DATA 0x01 contains CPM2 ENCODED value indicating location of edge in 12-bit sampler 15 means all ones 0 means 0b100000000000 1 means 0b110000000000..... 11 means 0b111111111111 0x02 contains CPM2 RAW value of the actual 12-bit sampler CPM2 is only available in EX core chiplets



Bits	PCB	Field Mnemonic: Description
44:63	N/A	Not implemented.

Register Name	<i>DTS Thermal Sensor Loop1 Results</i>
Mnemonic	ES.PBES_WRAP_TOP.TPC.EPS.THERM.DTS_RESULT0
Address	0000000008050000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:15	ROX	DTS_0_RESULT: Calibrated DTS Result of sensor with ID 0.
16:31	ROX	DTS_1_RESULT: Calibrated DTS Result of sensor with ID 1.
32:47	ROX	DTS_2_RESULT: Calibrated DTS Result of sensor with ID 2.
48:63	RO	Constant = 0b0000000000000000

Register Name	<i>Multicast Group 1</i>
Mnemonic	EH.TPCHIP.NET.PCBSLAB.MULTICAST_GROUP_1
Address	00000000080F0001 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	Constant = 0b111
3:5	RW	MULTICAST1_GROUP: multicast group1 setting

Register Name	<i>Multicast Group 2</i>
Mnemonic	EH.TPCHIP.NET.PCBSLAB.MULTICAST_GROUP_2
Address	00000000080F0002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	Constant = 0b111
3:5	RW	MULTICAST2_GROUP: multicast group2 setting

Register Name	<i>Multicast Group 3</i>
Mnemonic	EH.TPCHIP.NET.PCBSLAB.MULTICAST_GROUP_3
Address	00000000080F0003 (PCB)
Attributes	
Description	

Registers Specification

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Bits	PCB	Field Mnemonic: Description
0:2	RO	Constant = 0b111
3:5	RW	MULTICAST3_GROUP: multicast group3 setting

Register Name	Multicast Group 4
Mnemonic	EH.TPCHIP.NET.PCBSLAB.MULTICAST_GROUP_4
Address	00000000080F0004 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	Constant = 0b111
3:5	RW	MULTICAST4_GROUP: multicast group4 setting

Register Name	GP3 Register (NA In PERV CPLT)
Mnemonic	EH.TPCHIP.NET.PCBSLAB.GP3_REG
Address	00000000080F0012 (PCB) 00000000080F0013 (PCB1) 00000000080F0014 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset
2	RWX	RWX_WAND	RWX_WOR	GLSMUX_RESET: Glsmux reset for test purpose and stuck active mesh protection. Notice no clocks in the EX if this bit is set.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Put the DPLL in test mode.
4	RWX	RWX_WAND	RWX_WOR	PLL_RST: Put PLL in reset state.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYP: Enable PLL bypass.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pcb_access)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	PM_PI_DECODE: Test override for power management. EX chiplet only.



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
22	RWX	RWX_WAND	RWX_WOR	RESCLK_DIS: Resonant clocking disable.
23:25	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave will report 'Chiplet Offline'.
27	RWX	RWX_WAND	RWX_WOR	TP_LVLTRANS_FENCE: Electrical winkel fence. Mainly used by power management.
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.
29:31	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)

Register Name	<i>Hang Pulse Generation Register 0</i>
Mnemonic	EH.TPCHIP.NET.PCBSLAB.HANG_PULSE_0_REG
Address	00000000080F0020 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_0: Value of hang pulse 0. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_0: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 6</i>
Mnemonic	EH.TPCHIP.NET.PCBSLAB.HANG_PULSE_6_REG
Address	00000000080F0026 (PCB)
Attributes	
Description	This hang counter is exclusively used for the heartbeat generation

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_6: Value of hang pulse 6. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_6: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Divider For Hang Counter Clock</i>
Mnemonic	EH.TPCHIP.NET.PCBSLAB.PRE_COUNTER_REG
Address	00000000080F0028 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PRE_COUNTER: Divider for hang counter clock. Divides clock by n+1 (default: n=0)



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Register Name		Processor Bus PBES IOA Domain FIR0 Register		
Mnemonic		ES.PBES_WRAP_TOP.PBES_TOP.MISC_IO.SCOM.PB_IOA_FIR_REG		
Address		0000000008010800 (SCOM) 0000000008010801 (SCOM1) 0000000008010802 (SCOM2)		
Attributes				
Description				
Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	A0LINK_FMR_ERROR: a0link_fmr_error
1	RWX	WOX_AND	WOX_OR	A1LINK_FMR_ERROR: a1link_fmr_error
2	RWX	WOX_AND	WOX_OR	A2LINK_FMR_ERROR: a2link_fmr_error
3	RWX	WOX_AND	WOX_OR	A0LINK_PSR_ERR: a0link_psr_err
4	RWX	WOX_AND	WOX_OR	A1LINK_PSR_ERR: a1link_psr_err
5	RWX	WOX_AND	WOX_OR	A2LINK_PSR_ERR: a2link_psr_err
6	RWX	WOX_AND	WOX_OR	A0LINK_PSR_COR_ERR: a0link_psr_cor_err - the link experienced a correctable error
7	RWX	WOX_AND	WOX_OR	A0LINK_PSR_DERR_ERR: a0link_psr_derr_err - we received a data packet with DErr set from the other chip
8	RWX	WOX_AND	WOX_OR	A0LINK_PSR_UNC_ERR: a0link_psr_unc_err - the link experienced an uncorrectable error
9	RWX	WOX_AND	WOX_OR	A1LINK_PSR_COR_ERR: a1link_psr_cor_err - the link experienced a correctable error
10	RWX	WOX_AND	WOX_OR	A1LINK_PSR_DERR_ERR: a1link_psr_derr_err - we received a data packet with DErr set from the other chip
11	RWX	WOX_AND	WOX_OR	A1LINK_PSR_UNC_ERR: a1link_psr_unc_err - the link experienced an uncorrectable error
12	RWX	WOX_AND	WOX_OR	A2LINK_PSR_COR_ERR: a2link_psr_cor_err - the link experienced a correctable error
13	RWX	WOX_AND	WOX_OR	A2LINK_PSR_DERR_ERR: a2link_psr_derr_err - we received a data packet with DErr set from the other chip
14	RWX	WOX_AND	WOX_OR	A2LINK_PSR_UNC_ERR: a2link_psr_unc_err - the link experienced an uncorrectable error
15	RWX	WOX_AND	WOX_OR	A0LINK_FMR_COR_ERR_HI: a0link_fmr_cor_err_hi
16	RWX	WOX_AND	WOX_OR	A0LINK_FMR_COR_ERR_LO: a0link_fmr_cor_err_lo
17	RWX	WOX_AND	WOX_OR	A0LINK_FMR_SUE_ERR_HI: a0link_fmr_sue_err_hi
18	RWX	WOX_AND	WOX_OR	A0LINK_FMR_SUE_ERR_LO: a0link_fmr_sue_err_lo
19	RWX	WOX_AND	WOX_OR	A0LINK_FMR_UNC_ERR_HI: a0link_fmr_unc_err_hi
20	RWX	WOX_AND	WOX_OR	A0LINK_FMR_UNC_ERR_LO: a0link_fmr_unc_err_lo
21	RWX	WOX_AND	WOX_OR	A1LINK_FMR_COR_ERR_HI: a1link_fmr_cor_err_hi
22	RWX	WOX_AND	WOX_OR	A1LINK_FMR_COR_ERR_LO: a1link_fmr_cor_err_lo
23	RWX	WOX_AND	WOX_OR	A1LINK_FMR_SUE_ERR_HI: a1link_fmr_sue_err_hi
24	RWX	WOX_AND	WOX_OR	A1LINK_FMR_SUE_ERR_LO: a1link_fmr_sue_err_lo
25	RWX	WOX_AND	WOX_OR	A1LINK_FMR_UNC_ERR_HI: a1link_fmr_unc_err_hi
26	RWX	WOX_AND	WOX_OR	A1LINK_FMR_UNC_ERR_LO: a1link_fmr_unc_err_lo



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
27	RWX	WOX_AND	WOX_OR	A2LINK_FMR_COR_ERR_HI: a2link_fmr_cor_err_hi
28	RWX	WOX_AND	WOX_OR	A2LINK_FMR_COR_ERR_LO: a2link_fmr_cor_err_lo
29	RWX	WOX_AND	WOX_OR	A2LINK_FMR_SUE_ERR_HI: a2link_fmr_sue_err_hi
30	RWX	WOX_AND	WOX_OR	A2LINK_FMR_SUE_ERR_LO: a2link_fmr_sue_err_lo
31	RWX	WOX_AND	WOX_OR	A2LINK_FMR_UNC_ERR_HI: a2link_fmr_unc_err_hi
32	RWX	WOX_AND	WOX_OR	A2LINK_FMR_UNC_ERR_LO: a2link_fmr_unc_err_lo
33	RWX	WOX_AND	WOX_OR	A0_OBS_CR_OVERFLOW_FIR_ERR: A0 outbound switch overflow
34	RWX	WOX_AND	WOX_OR	A1_OBS_CR_OVERFLOW_FIR_ERR: A1 outbound switch overflow
35	RWX	WOX_AND	WOX_OR	A2_OBS_CR_OVERFLOW_FIR_ERR: A2 outbound switch overflow
36	RWX	WOX_AND	WOX_OR	FIR_SCOM_ERR_DUP: PBES IOA FIR_SCOM_err
37	RWX	WOX_AND	WOX_OR	FIR_SCOM_ERR: PBES IOA FIR_SCOM_err
38:63	RO	N/A	N/A	Constant = 0b000000000000000000000000

Register Name	<i>Processor Bus PBES IOA Domain FIR MASK Register</i>
Mnemonic	ES.PBES_WRAP_TOP.PBES_TOP.MISC_IO.SCOM.PB_IOA_FIR_MASK_REG
Address	0000000008010803 (SCOM) 0000000008010804 (SCOM1) 0000000008010805 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	A0LINK_FMR_ERROR_MASK: a0link_fmr_error_mask
1	RW	WO_AND	WO_OR	A1LINK_FMR_ERROR_MASK: a1link_fmr_error_mask
2	RW	WO_AND	WO_OR	A2LINK_FMR_ERROR_MASK: a2link_fmr_error_mask
3	RW	WO_AND	WO_OR	A0LINK_PSR_ERR_MASK: a0link_psr_err_mask
4	RW	WO_AND	WO_OR	A1LINK_PSR_ERR_MASK: a1link_psr_err_mask
5	RW	WO_AND	WO_OR	A2LINK_PSR_ERR_MASK: a2link_psr_err_mask
6	RW	WO_AND	WO_OR	A0LINK_PSR_COR_ERR_MASK: a0link_psr_cor_err_mask
7	RW	WO_AND	WO_OR	A0LINK_PSR_DERR_ERR_MASK: a0link_psr_derr_err_mask
8	RW	WO_AND	WO_OR	A0LINK_PSR_UNC_ERR_MASK: a0link_psr_unc_err_mask
9	RW	WO_AND	WO_OR	A1LINK_PSR_COR_ERR_MASK: a1link_psr_cor_err_mask
10	RW	WO_AND	WO_OR	A1LINK_PSR_DERR_ERR_MASK: a1link_psr_derr_err_mask
11	RW	WO_AND	WO_OR	A1LINK_PSR_UNC_ERR_MASK: a1link_psr_unc_err_mask
12	RW	WO_AND	WO_OR	A2LINK_PSR_COR_ERR_MASK: a2link_psr_cor_err_mask
13	RW	WO_AND	WO_OR	A2LINK_PSR_DERR_ERR_MASK: a2link_psr_derr_err_mask
14	RW	WO_AND	WO_OR	A2LINK_PSR_UNC_ERR_MASK: a2link_psr_unc_err_mask
15	RW	WO_AND	WO_OR	A0LINK_FMR_COR_ERR_HI_MASK: a0link_fmr_cor_err_hi_mask
16	RW	WO_AND	WO_OR	A0LINK_FMR_COR_ERR_LO_MASK: a0link_fmr_cor_err_lo_mask
17	RW	WO_AND	WO_OR	A0LINK_FMR_SUE_ERR_HI_MASK: a0link_fmr_sue_err_hi_mask

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
18	RW	WO_AND	WO_OR	A0LINK_FMR_SUE_ERR_LO_MASK: a0link_fmr_sue_err_lo_mask
19	RW	WO_AND	WO_OR	A0LINK_FMR_UNC_ERR_HI_MASK: a0link_fmr_unc_err_hi_mask
20	RW	WO_AND	WO_OR	A0LINK_FMR_UNC_ERR_LO_MASK: a0link_fmr_unc_err_lo_mask
21	RW	WO_AND	WO_OR	A1LINK_FMR_COR_ERR_HI_MASK: a1link_fmr_cor_err_hi_mask
22	RW	WO_AND	WO_OR	A1LINK_FMR_COR_ERR_LO_MASK: a1link_fmr_cor_err_lo_mask
23	RW	WO_AND	WO_OR	A1LINK_FMR_SUE_ERR_HI_MASK: a1link_fmr_sue_err_hi_mask
24	RW	WO_AND	WO_OR	A1LINK_FMR_SUE_ERR_LO_MASK: a1link_fmr_sue_err_lo_mask
25	RW	WO_AND	WO_OR	A1LINK_FMR_UNC_ERR_HI_MASK: a1link_fmr_unc_err_hi_mask
26	RW	WO_AND	WO_OR	A1LINK_FMR_UNC_ERR_LO_MASK: a1link_fmr_unc_err_lo_mask
27	RW	WO_AND	WO_OR	A2LINK_FMR_COR_ERR_HI_MASK: a2link_fmr_cor_err_hi_mask
28	RW	WO_AND	WO_OR	A2LINK_FMR_COR_ERR_LO_MASK: a2link_fmr_cor_err_lo_mask
29	RW	WO_AND	WO_OR	A2LINK_FMR_SUE_ERR_HI_MASK: a2link_fmr_sue_err_hi_mask
30	RW	WO_AND	WO_OR	A2LINK_FMR_SUE_ERR_LO_MASK: a2link_fmr_sue_err_lo_mask
31	RW	WO_AND	WO_OR	A2LINK_FMR_UNC_ERR_HI_MASK: a2link_fmr_unc_err_hi_mask
32	RW	WO_AND	WO_OR	A2LINK_FMR_UNC_ERR_LO_MASK: a2link_fmr_unc_err_lo_mask
33	RW	WO_AND	WO_OR	A0_OBS_CR_OVERFLOW_FIR_MASK: A0 outbound switch overflow mask
34	RW	WO_AND	WO_OR	A1_OBS_CR_OVERFLOW_FIR_MASK: A1 outbound switch overflow mask
35	RW	WO_AND	WO_OR	A2_OBS_CR_OVERFLOW_FIR_MASK: a2 outbound switch overflow mask
36	RW	WO_AND	WO_OR	FIR_SCOM_ERR_MASK_DUP: PBES IOA FIR_SCOM_err_mask_dup
37	RW	WO_AND	WO_OR	FIR_SCOM_ERR_MASK: PBES IOA FIR_SCOM_err_mask
38:63	RO	N/A	N/A	Constant = 0b000000000000000000000000

Register Name		Processor Bus PBES IOA Domain FIR Action 0 Register
Mnemonic		ES.PBES_WRAP_TOP.PBES_TOP.MISC_IO.SCOM.PB_IOA_FIR_ACTION0_REG
Address		0000000008010806 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:37	RW	PB_IOA_FIR_ACTION0: Processor Bus PBES IOA domain action select for corresponding bit in FIR (Action0,Action1) = Action Select (0,0) = Checkstop (0,1) = Recoverable Error to Service Processor (1,0) = Recoverable Interrupt to Processor (1,1) = Invalid
38:63	RO	Constant = 0b000000000000000000000000



Register Name		Processor Bus PBES IOA Domain FIR Action 1 Register
Mnemonic		ES.PBES_WRAP_TOP.PBES_TOP.MISC_IO.SCOM.PB_IOA_FIR_ACTION1_REG
Address		0000000008010807 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:37	RW	PB_IOA_FIR_ACTION1: Processor bus FIR LSB of action select for corresponding bit in FIR (Action0,Action1) = Action Select (0,0) = Checkstop (0,1) = Recoverable Error to Service Processor (1,0) = Recoverable Interrupt to Processor (1,1) = Invalid
38:63	RO	Constant = 0b00000000000000000000000000000000

Register Name		Processor Bus PBES IOA Domain Mode Register
Mnemonic		ES.PBES_WRAP_TOP.PBES_TOP.MISC_IO.SCOM.PB_IOA_MODE
Address		000000000801080A (SCOM)
Attributes		
Description		Bit Function 00 = AVP mode 01 = Disable outbound ECC correction 02 = Disable inbound ECC correction 03 = clear captured outbound syndromes (self-resets to 0) Also clears related CE/UE/SUE c_err_rpt hold latches. 04 = clear captured inbound symbols (self-resets to 0) 05 = Enable Error Injection on A0 06 = Enable Error Injection on A1 07 = Enable Error Injection on A2 08 = Outbound ECC error inject mode. 0=single-shot, 1=solid (writing this register with any value will reset the single-shot logic) 09:10 = Beat selector for error injection. 0=A, 1=B, 2=C, 3=D. 11 = Inject on bit 16 (to create a UE) 12:15 = Selects a bit to inject an SBE on - 0:15 16:20 = Link data buffer credits. Max of 16 allowed. Controls the number of of octwords in flight over the link. 21:31 = spare 32 = Link A0 is trained 33 = Link A1 is trained 34 = Link A2 is trained 35:39 = Reserved 40:47 = Link A0 round-trip Delay. $2 + (\text{Delay}-4)/2$ = Fmr input to parser output on other chip in a_nclk cycles. 48:55 = Link A1 round-trip Delay. $2 + (\text{Delay}-4)/2$ = Fmr input to parser output on other chip in a_nclk cycles. 56:63 = Link A2 round-trip Delay. $2 + (\text{Delay}-4)/2$ = Fmr input to parser output on other chip in a_nclk cycles.

Bits	SCOM	Field Mnemonic: Description
0	RW	AVP_MODE: AVP mode
1	RW	DISABLE_ECC_OUT: Disable outbound ECC correction
2	RW	DISABLE_ECC_IN: Disable inbound ECC correction
3	WO_1P	CLEAR_SYNDROME_OUT: clear captured outbound syndromes (self-resets to 0). Also clears related CE/UE/SUE c_err_rpt hold latches.
4	WO_1P	CLEAR_SYMBOL_IN: clear captured inbound symbols (self-resets to 0)
5	RW	ENABLE_INJECT_A0_OUT: Enable Error Injection on A0
6	RW	ENABLE_INJECT_A1_OUT: Enable Error Injection on A1
7	RW	ENABLE_INJECT_A2_OUT: Enable Error Injection on A2
8	RW	INJECT_MODE: Outbound ECC error inject mode. 0=single-shot, 1=solid (writing this register with any value will reset the single-shot logic)
9:10	RW	INJECT_BEAT_SELECT: Beat selector for error injection. 0=A, 1=B, 2=C, 3=D.
11	RW	INJECT_BIT_16: Inject on bit 16 (to create a UE)
12:15	RW	INJECT_BIT_0_15: Selects a bit to inject an SBE on - 0:15
16:20	RW	DATA_BUF_OW_CRED: Link data buffer credits. Max of 16 allowed. Controls the number of of octwords in flight over the link.

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Bits	SCOM	Field Mnemonic: Description
21:31	RW	Reserved field. (Access type is mode_spare)
32	ROX	Reserved field. (Access type is Link_A0_trained)
33	ROX	Reserved field. (Access type is Link_A1_trained)
34	ROX	Reserved field. (Access type is Link_A2_trained)
35:39	RO	Constant = 0b00000
40:47	ROX	Reserved field. (Access type is Link_A0_Delay)
48:55	ROX	Reserved field. (Access type is Link_A1_Delay)
56:63	ROX	Reserved field. (Access type is Link_A2_Delay)

Register Name	Processor Bus PBES IOA Domain Trace Control Register
Mnemonic	ES.PBES_WRAP_TOP.PBES_TOP.MISC_IO.SCOM.PB_IOA_TRACE_CFG
Address	0000000008010812 (SCOM)
Attributes	
Description	Processor Bus PBES IOA Domain Trace Control Register

Bits	SCOM	Field Mnemonic: Description
0:1	RW	A0_OUT_SEL0: A0 Outbound selector for bits 0:27 00 - disabled 01 - link data (selection must be exclusive) 10 - group B (some inbound/outbound pairing allowed in bits 56:87) 11 - group C (inbound/outbound can be paired - each uses half of the field) all selected fields for a bit group are OR'd together, so each group of bits should have only one source selected (except for groups B/C)
2:3	RW	A0_OUT_SEL1: A0 Outbound selector for bits 28:55
4:5	RW	A0_OUT_SEL2: A0 Outbound selector for bits 56:87
6:7	RW	A1_OUT_SEL0: A1 Outbound selector for bits 0:27
8:9	RW	A1_OUT_SEL1: A1 Outbound selector for bits 28:55
10:11	RW	A1_OUT_SEL2: A1 Outbound selector for bits 56:87
12:13	RW	A2_OUT_SEL0: A2 Outbound selector for bits 0:27
14:15	RW	A2_OUT_SEL1: A2 Outbound selector for bits 28:55
16:17	RW	A2_OUT_SEL2: A2 Outbound selector for bits 56:87
18:19	RW	A0_IN_SEL0: A0 Inbound selector for bits 0:27
20:21	RW	A0_IN_SEL1: A0 Inbound selector for bits 28:55
22:23	RW	A0_IN_SEL2: A0 Inbound selector for bits 56:87
24:25	RW	A1_IN_SEL0: A1 Inbound selector for bits 0:27
26:27	RW	A1_IN_SEL1: A1 Inbound selector for bits 28:55
28:29	RW	A1_IN_SEL2: A1 Inbound selector for bits 56:87
30:31	RW	A2_IN_SEL0: A2 Inbound selector for bits 0:27
32:33	RW	A2_IN_SEL1: A2 Inbound selector for bits 28:55
34:35	RW	A2_IN_SEL2: A2 Inbound selector for bits 56:87
36	RW	A0_DOBS_TRCSEL: A0 dobs trtsel - drives bits 00:19 of trace bus
37	RW	A1_DOBS_TRCSEL: A1_dobs_trtsel - drives bits 20:39 of trace bus
38	RW	A2_DOBS_TRCSEL: A2_dobs_trtsel - drives bits 40:59 of trace bus
39	RW	PHY_TRCSEL: PHY_trtsel - drives entire trace bus

Bits	SCOM	Field Mnemonic: Description
40	RW	ENABLE_PERFTRACE: Enable_perfrace - perfrace mode enabled, bits 0:39 of this register become don't cares
41	RW	ENABLE_PERFTRACE_PRESCALE: Enable_perfrace_prescale - wide-angle view - perfcounets are prescaled by 128
42	RW	ENABLE_PERFTRACE_FIXED_WIN: Enable_perfrace_fixed_win - 0=take a sample every 255 cycles, 1=every 255x128 cycles
43	RW	Reserved field. (Access type is spare)
44:63	RO	Constant = 0b00000000000000000000

Register Name	Processor Bus PBES IOA Framer Configuration Register
Mnemonic	ES.PBES_WRAP_TOP.PBES_TOP.MISC_IO.SCOM.PB_IOA_FMR_CFG
Address	0000000008010813 (SCOM)
Attributes	
Description	When written, the contents of this register will update shadow copies in the framers. The relevant dials are listed below. bit shadow dial description 00:03 ALink_TOD_Wait_Limit - how long to wait to pair up a TOD with something before forcing TOD out the link 04:07 ALink_pRsp_Wait_Limit - how long to wait to pair up a pRsp with something before forcing pRsp out the link 08:11 ALink_CQ_Wait_Limit - how long to wait to pair up cresp queue credits with something before forcing them out the link 12:15 A0Link_DC_Wait_Limit - how long to wait to pair up data credits with something before forcing them out the link 16:19 A1Link_DC_Wait_Limit - how long to wait to pair up data credits with something before forcing them out the link 20:23 A2Link_DC_Wait_Limit - how long to wait to pair up data credits with something before forcing them out the link 24 ALink_OctWord_Pack - When 1, framer will keep octwords together when sending data. When zero, data can be interrupted every 8 bytes. 25 ALink_OctWord_Pack_Priority - If ALink_OctWord_Pack=ON, this switch dictates whether the 32B have low priority to start (OFF), or high (ON). Once started, we then send the 32B in a block. 26:31 Spare 32:63 Reserved

Bits	SCOM	Field Mnemonic: Description
0:3	RW	PB_IOA_FMR_CFGTODWT: transfers to ALink_TOD_Wait_Limit - how long to wait to pair up a TOD with something before forcing TOD out the link
4:7	RW	PB_IOA_FMR_CFGPRSPWT: transfers to ALink_pRsp_Wait_Limit - how long to wait to pair up a pRsp with something before forcing pRsp out the link
8:11	RW	PB_IOA_FMR_CFGCQWT: transfers to ALink_CQ_Wait_Limit - how long to wait to pair up cresp queue credits with something before forcing them out the link
12:15	RW	PB_IOA0_FMR_CFGDCWT: transfers to IOA0.IOA.ALink_DC_Wait_Limit - how long to wait to pair up data credits with something before forcing them out the link
16:19	RW	PB_IOA1_FMR_CFGDCWT: transfers to IOA1.IOA.ALink_DC_Wait_Limit - how long to wait to pair up data credits with something before forcing them out the link
20:23	RW	PB_IOA2_FMR_CFGDCWT: transfers to IOA2.IOA.ALink_DC_Wait_Limit - how long to wait to pair up data credits with something before forcing them out the link
24	RW	PB_IOA_FMR_CFGOWP: transfers to ALink_OctWord_Pack - When 1, framer will keep octwords together when sending data. When zero, data can be interrupted every 8 bytes.
25	RW	PB_IOA_FMR_CFGOWPP: transfers to ALink_OctWord_Pack_Priority - If ALink_OctWord_Pack=ON, this switch dictates whether the 32B have low priority to start (OFF), or high (ON). Once started, we then send the 32B in a block.
26:31	RW	Reserved field. (Access type is ALink_spare.)

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Register Name	GP Register 1
Mnemonic	ES.PE_WRAP_TOP.TPC.GP1
Address	0000000009000001 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	PART0_TC_ABIST_DONE_DC: PCI express asynchronous, PB foreign fabric asynchronous ABIST done. Reset (0).
1	ROX	NOT_USED18: Not used. Reset (0).
2	ROX	NOT_USED19: Not used. Reset (0).
3	ROX	TRA_TC_ABIST_DONE_DC: PCI Asynchronous South Trace Array ABIST done. Reset (0).
4	ROX	NOT_USED20: Not used. Reset (0).
5	ROX	NOT_USED21: Not used. Reset (0).
6	ROX	NOT_USED22: Not used. Reset (0).
7	ROX	PLLPCIE_TP_DTESTOUT_DC: Not used. Reset (0).
8	ROX	NOT_USED23: Not used. Reset (0).
9	ROX	NOT_USED24: Not used. Reset (0).
10	ROX	NOT_USED25: Not used. Reset (0).
11	ROX	NOT_USED26: Not used. Reset (0).
12	ROX	NOT_USED27: Not used. Reset (0).
13	ROX	NOT_USED28: Not used. Reset (0).
14	ROX	NOT_USED29: Not used. Reset (0).
15	ROX	TC_OPCG_DONE_DC: Clock control OPCG done. Reset (0).
16	ROX	FREE_USAGE0: chiplet specific, Reset (0).
17	ROX	FREE_USAGE1: chiplet specific, Reset (0).
18	ROX	FREE_USAGE2: chiplet specific, Reset (0).
19	ROX	FREE_USAGE3: chiplet specific, Reset (0).
20	ROX	FREE_USAGE4: chiplet specific, Reset (0).
21	ROX	FREE_USAGE5: chiplet specific, Reset (0).
22	ROX	FREE_USAGE6: chiplet specific, Reset (0).
23	ROX	FREE_USAGE7: chiplet specific, Reset (0).

Register Name	GP Register 2
Mnemonic	ES.PE_WRAP_TOP.TPC.GP2
Address	0000000009000002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:23	RW	GPIN_MASKING: GPIN bitwise interrupt masking



Register Name	GP Register 4			
Mnemonic	ES.PE_WRAP_TOP.TPC.GP4			
Address	0000000009000003 (PCB) 0000000009000006 (PCB1) 0000000009000007 (PCB2)			
Attributes				
Description				
Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0:5	RWX	WOX_AND	WOX_OR	TC_PROBE0_SEL_DC: Probe 0 select. Reset (0b000000).
6:7	RWX	WOX_AND	WOX_OR	NOT_USED30: Not used: 0b0. Reset (0b00).
8:13	RWX	WOX_AND	WOX_OR	TC_PROBE1_SEL_DC: Probe 1 select. Reset (0b000000).
14:15	RWX	WOX_AND	WOX_OR	NOT_USED31: Not used: 0b0. Reset (0b00).
16:21	RWX	WOX_AND	WOX_OR	TC_PROBE2_SEL_DC: Probe 2 select. Reset (0b000000)
22:23	RWX	WOX_AND	WOX_OR	NOT_USED32: Not used: 0b0. Reset (0b00)
24:29	RWX	WOX_AND	WOX_OR	TC_PROBE3_SEL_DC: tc_probe3_sel_dc(0:5) / tcpci_sense_sel_dc(0:2), -, Reset (0b000000).
30	RWX	WOX_AND	WOX_OR	NOT_USED33: Not used: 0b0. Reset (0b0).
31	RWX	WOX_AND	WOX_OR	TC_GP4_OFLOW_FEH_SEL_DC: ABIST: When 1, fail bit is overflow; otherwise, it is a fail. Reset (0b0).
32	RWX	WOX_AND	WOX_OR	TC_PCI_RATIO_DC_0: Reset (0b0).
33	RWX	WOX_AND	WOX_OR	TC_PCI_RATIO_DC_1: Reset (0b0).
34	RWX	WOX_AND	WOX_OR	TC_PCI_RATIO_OV_DC: Reset (13s: 0b1 c22: 0b0).
35	RWX	WOX_AND	WOX_OR	NOT_USED34: Not used. Reset (0b0).
36	RWX	WOX_AND	WOX_OR	NOT_USED35: Not used. Reset (0b0).
37	RWX	WOX_AND	WOX_OR	TC_IOP0_SYS_RESET_PHY_DC_B: Reset (0b0).
38	RWX	WOX_AND	WOX_OR	TC_IOP1_SYS_RESET_PHY_DC_B: Reset (0b0).
39	RWX	WOX_AND	WOX_OR	NOT_USED36: Not used. Reset (0b0).
40	RWX	WOX_AND	WOX_OR	NOT_USED37: Not used. Reset (13s: 0b1 c22: 0b0)
41	RWX	WOX_AND	WOX_OR	TC_IOP_LANE_CFG_DC_0: Reset (0b0).
42	RWX	WOX_AND	WOX_OR	TC_IOP_LANE_CFG_DC_1: Reset (0b0).
43	RWX	WOX_AND	WOX_OR	TC_IOP_LANE_CFG_DC_2: Reset (0b0).
44	RWX	WOX_AND	WOX_OR	TC_IOP_LANE_CFG_DC_3: Reset (0b0).
45	RWX	WOX_AND	WOX_OR	TC_PCI_CS_HW250620_DISABLE_DC: Not used. Reset (0b0).
46	RWX	WOX_AND	WOX_OR	NOT_USED39: Not used. Reset (13s: 0b1 c22: 0b0)
47	RWX	WOX_AND	WOX_OR	TC_IOP0_SWAP_DC_0: Reset (0b0).
48	RWX	WOX_AND	WOX_OR	TC_IOP0_SWAP_DC_1: Reset (0b0).
49	RWX	WOX_AND	WOX_OR	TC_IOP0_SWAP_DC_2: Reset (0b0).
50	RWX	WOX_AND	WOX_OR	NOT_USED40: Not used. Reset (0b0).
51	RWX	WOX_AND	WOX_OR	NOT_USED41: Not used. Reset (0b0).

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
52	RWX	WOX_AND	WOX_OR	NOT_USED42: Not used. Reset (13s: 0b1 c22: 0b0)
53	RWX	WOX_AND	WOX_OR	TC_IOP1_SWAP_DC_0: Reset (0b0).
54	RWX	WOX_AND	WOX_OR	TC_IOP1_SWAP_DC_1: Reset (0b0)
55	RWX	WOX_AND	WOX_OR	TC_IOP1_SWAP_DC_2: Reset (0b0).
56	RWX	WOX_AND	WOX_OR	NOT_USED43: Not used. Reset (0b0).
57	RWX	WOX_AND	WOX_OR	NOT_USED44: Not used. Reset (0b0).
58	RWX	WOX_AND	WOX_OR	NOT_USED45: Not used. Reset (13s: 0b1 c22: 0b0)
59	RWX	WOX_AND	WOX_OR	NOT_USED46: Not used. Reset (0b0).
60	RWX	WOX_AND	WOX_OR	NOT_USED47: Not used. Reset (0b0).
61	RWX	WOX_AND	WOX_OR	TC_PBF0_ENABLE_DC: Reset (0b0).
62	RWX	WOX_AND	WOX_OR	TC_PBF1_ENABLE_DC: Reset (0b0).
63	RWX	WOX_AND	WOX_OR	NOT_USED48: Not used. Reset (0b0).

Register Name	<i>PSCOMLE Mode Register</i>
Mnemonic	ES.PE_WRAP_TOP.TPC.EPS.PSC.PSCOM_MODE_REG
Address	0000000009010000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	ABORT_ON_PCB_ADDR_PARITY_ERROR: Abort on PCB address parity error.
1	RW	ABORT_ON_PCB_WDATA_PARITY_ERROR: Abort on PCB wdata parity error.
2	RW	ABORT_ON_DL_RETURN_P0_ERROR: Abort on DL return P0 error.
3	RW	ABORT_ON_DL_RETURN_WDATA_PARITY_ERROR: Abort on DL return wdata parity error.
4	RW	WATCHDOG_ENABLE: Watchdog enable.
5:6	RW	SCOM_HANG_LIMIT: 0b00: 1023 0b01: 768 0b10: 512 0b11: 256
7	RW	FORCE_ALL_RINGS: Set to logic 1, if all rings should be enabled independent of ring address.
8	RW	FSM_SELFRESET_ON_STATEVEC_PARITYERROR_ENABLE: FSM self-reset on statevec parity error enable.
9:11	RW	RESERVED_PSCOM_MODE_LT: Reserved.



Register Name		Processor Bus PBES IOF1 Internal Error Readout Register																																																																
Mnemonic		ES.PBES_WRAP_TOP.PBES_TOP.MISC_IOF.SCOM.PB_IOF1_ERR_DETAIL																																																																
Address		0000000009010812 (SCOM)																																																																
Attributes																																																																		
Description		These errors can be masked with their individual c_err_rpt masks - see pbs_iof.fig																																																																
		<table><tr><td>Bit</td><td>Description</td></tr><tr><td>0</td><td>F1 Outbound rCmd address parity error.</td></tr><tr><td>1</td><td>F1 Outbound PB data credit overflow.</td></tr><tr><td>2</td><td>F1 Outbound cRes description p credit overflow.</td></tr><tr><td>3</td><td>F1 Outbound crsp0 txid error - cResp probably lost.</td></tr><tr><td>4</td><td>F1 Outbound crsp1 txid error - cResp probably los.</td></tr><tr><td>5</td><td>F1 collision between PB dhdr and ASB dhdr. Data corrupted.</td></tr><tr><td>6</td><td>F1 Outbound data header parity error.</td></tr><tr><td>7</td><td>F1 Outbound pResp parity error.</td></tr><tr><td>8</td><td>F1 Outbound pResp txid error - pResp probably lost.</td></tr><tr><td>9</td><td>F1 Outbound rCmd txid error - rCmd probably lost.</td></tr><tr><td>10</td><td>F1 Outbound tTag parity error.</td></tr><tr><td>11</td><td>F1 Outbound sfStat parity error.</td></tr><tr><td>12 – 24</td><td>Reserved.</td></tr><tr><td>25</td><td>F1 Outbound Switch rcmd overflow error.</td></tr><tr><td>26</td><td>F1 Outbound Switch prsp overflow error.</td></tr><tr><td>27</td><td>F1 Outbound Switch crsp0 overflow error.</td></tr><tr><td>28</td><td>F1 Outbound Switch crsp1 overflow error.</td></tr><tr><td>29</td><td>F1 Outbound Switch c0 e2e crd overflow error.</td></tr><tr><td>30</td><td>F1 Outbound Switch c1 e2e crd overflow error.</td></tr><tr><td>31</td><td>F1 Outbound Switch crsp crd overflow error.</td></tr><tr><td>32 - 35</td><td>F1 Inbound data_a parity error (1 bit/nibble).</td></tr><tr><td>36 - 39</td><td>F1 Inbound data_b parity error (1 bit/nibble).</td></tr><tr><td>40 - 43</td><td>F1 Inbound data_c parity error (1 bit/nibble).</td></tr><tr><td>44 - 47</td><td>F1 Inbound data_d parity error (1 bit/nibble).</td></tr><tr><td>48</td><td>F1 Inbound rCmd address parity error.</td></tr><tr><td>49</td><td>F1 pcie->psr control bus parity error.</td></tr><tr><td>50</td><td>F1 Inbound missing data error. (Unexpected data header).</td></tr><tr><td>51</td><td>F1 Inbound missing data header.(Unexpected data).</td></tr><tr><td>52</td><td>F1 Inbound tTag parity error.</td></tr><tr><td>53</td><td>F1 Inbound data credit overflow error.</td></tr><tr><td>54 - 63</td><td>Reserved.</td></tr></table>	Bit	Description	0	F1 Outbound rCmd address parity error.	1	F1 Outbound PB data credit overflow.	2	F1 Outbound cRes description p credit overflow.	3	F1 Outbound crsp0 txid error - cResp probably lost.	4	F1 Outbound crsp1 txid error - cResp probably los.	5	F1 collision between PB dhdr and ASB dhdr. Data corrupted.	6	F1 Outbound data header parity error.	7	F1 Outbound pResp parity error.	8	F1 Outbound pResp txid error - pResp probably lost.	9	F1 Outbound rCmd txid error - rCmd probably lost.	10	F1 Outbound tTag parity error.	11	F1 Outbound sfStat parity error.	12 – 24	Reserved.	25	F1 Outbound Switch rcmd overflow error.	26	F1 Outbound Switch prsp overflow error.	27	F1 Outbound Switch crsp0 overflow error.	28	F1 Outbound Switch crsp1 overflow error.	29	F1 Outbound Switch c0 e2e crd overflow error.	30	F1 Outbound Switch c1 e2e crd overflow error.	31	F1 Outbound Switch crsp crd overflow error.	32 - 35	F1 Inbound data_a parity error (1 bit/nibble).	36 - 39	F1 Inbound data_b parity error (1 bit/nibble).	40 - 43	F1 Inbound data_c parity error (1 bit/nibble).	44 - 47	F1 Inbound data_d parity error (1 bit/nibble).	48	F1 Inbound rCmd address parity error.	49	F1 pcie->psr control bus parity error.	50	F1 Inbound missing data error. (Unexpected data header).	51	F1 Inbound missing data header.(Unexpected data).	52	F1 Inbound tTag parity error.	53	F1 Inbound data credit overflow error.	54 - 63	Reserved.
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Bits	SCOM	Field Mnemonic: Description																																																																
0:11	ROX																																																																	

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
12:24	RO	Constant = 0b00000000000000
25:53	ROX	
54:63	RO	Constant = 0b000000000000

Register Name	<i>Processor Bus PBES IOF Framer Configuration Register</i>	
Mnemonic	ES.PBES_WRAP_TOP.PBES_TOP.MISC_IOF.SCOM.PB_IOF_FMR_CFG	
Address	0000000009010813 (SCOM)	
Attributes		
Description	When written, the contents of this register update shadow copies in the framers. The relevant dials are listed below.	
	Bit Shadow	Dial Description
	0 - 3	FLink_AS_Wait_Limit. Indicates how long to wait to pair up Accelerator Switchboard Data credits with something before forcing them out the link.
	4 - 7	FLink_pRsp_Wait_Limit. Indicates how long to wait to pair up a pRsp with something before forcing pRsp out the link.
	8 - 11	FLink_CQ_Wait_Limit. Indicates how long to wait to pair up cresp queue credits with something before forcing them out the link.
	12 - 15	F0Link_DC_Wait_Limit. Indicates how long to wait to pair up coherent data credits with something before forcing them out the link.
	16 - 19	F1Link_DC_Wait_Limit. Indicates how long to wait to pair up coherent data credits with something before forcing them out the link.
	20	FLink_OctWord_Pack - When 1, the framer keeps octwords together when sending data. When zero, data can be interrupted every 8 bytes.
	21	FLink_OctWord_Pack_Priority. If ALink_OctWord_Pack = ON, this switch dictates whether the 32-bytes have low priority to start (OFF), or high (ON). Once started, send the 32 bytes in a block.
	22 - 23	Spare.
	24 - 63	Reserved.

Bits	SCOM	Field Mnemonic: Description
0:3	RW	PB_IOF_FMR_CFGASCWT: transfers to FLink_AS_Wait_Limit - how long to wait to pair up Accelerator Switchboard Data credits with something before forcing them out the link
4:7	RW	PB_IOF_FMR_CFGPRSPWT: transfers to FLink_pRsp_Wait_Limit - how long to wait to pair up a pRsp with something before forcing pRsp out the link
8:11	RW	PB_IOF_FMR_CFGCQWT: transfers to FLink_CQ_Wait_Limit - how long to wait to pair up cresp queue credits with something before forcing them out the link
12:15	RW	PB_IOF0_FMR_CFGDCWT: transfers to ioF0.ioF.FLink_DC_Wait_Limit - how long to wait to pair up coherent data credits with something before forcing them out the link
16:19	RW	PB_IOF1_FMR_CFGDCWT: transfers to ioF1.ioF.FLink_DC_Wait_Limit - how long to wait to pair up coherent data credits with something before forcing them out the link
20	RW	PB_IOF_FMR_CFGOWP: transfers to FLink_OctWord_Pack - When 1, framer will keep octwords together when sending data. When zero, data can be interrupted every 8 bytes.
21	RW	PB_IOF_FMR_CFGOWPP: transfers to FLink_OctWord_Pack_Priority - If FLink_OctWord_Pack=ON, this switch dictates whether the 32B have low priority to start (OFF), or high (ON). Once started, we then send the 32B in a block.



Bits	SCOM	Field Mnemonic: Description
22:23	RW	Reserved field. (Access type is FLink_spare.)

Register Name	<i>Debug Status Register</i>
Mnemonic	ES.PE_WRAP_TOP.TPC.EPS.PSC.DEBUG_STATUS_REG
Address	0000000009010004 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	LOCAL_TRACE_RUN_IN: Local trace run
1:2	RWX	TRACE_STATE_LAT: Trace state latch
3	RWX	TRACE_FREEZE: Trace freeze
4:5	RWX	COND3_STATE_LT: Condition 3 state latch
6:7	RWX	COND5_STATE_LT: Condition 5 state latch
8	RWX	HISTORY_CONDITION0_LT: Condition event history for condition0_lt
9	RWX	HISTORY_CONDITION1_LT: Condition event history for condition1_lt
10	RWX	HISTORY_COND2_3_EVENT: Condition event history for cond2_3_event
11	RWX	HISTORY_COND2_TIMEOUT: Condition event history for cond2_timeout
12	RWX	HISTORY_COND4_5_EVENT: Condition event history for cond4_5_event
13	RWX	HISTORY_COND4_TIMEOUT: Condition event history for cond4_timeout
14:15	RWX	RESERVED_TCDBG_STATUS_LT: Reserved, set to zero

Register Name	<i>Trace Array High Data Register</i>
Mnemonic	ES.PE_WRAP_TOP.TPC.TRA.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG
Address	0000000009010400 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63

Register Name	<i>Trace Array Low Data Register</i>
Mnemonic	ES.PE_WRAP_TOP.TPC.TRA.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG
Address	0000000009010401 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95
32:41	ROX	TRACE_ADDRESS: Trace Address
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank



Bits	SCOM	Field Mnemonic: Description
0:37	RW	PE_AIB_BASEADDR_REG: PE AIB bus Base Address Register
38:63	RO	Constant = 0b000000000000000000000000

[illegible]

Register Name		<i>PE Bus ASB Base Address Register</i>
Mnemonic		ES.PE_WRAP_TOP.PE2.PEPBCQ.PBAIB.PEAIBREGS.PE_SYS_PH3_BASEADDR_REG
Address		00000000901280B (SCOM)
Attributes		
Description		PE Bus ASB Base Address Register
Bits	SCOM	Field Mnemonic: Description
0:37	RW	PE_AIB_BASEADDR_REG: PE AIB bus Base Address Register
38:63	RO	Constant = 0b000000000000000000000000

Register Name		OPCG Control Register 0
Mnemonic		ES.PE_WRAP_TOP.TPC.OPCG_REG0
Address		000000009030002 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RW	RUNN_MODE: runn-mode if 1 or BIST mode if 0
1	RWX	OPCG_GO: opcg go (start sequence)
2	RWX	RUN_SCAN0: run scan0 (will override all BIST mode settings but the scan_ratio)
3	RW	SCAN0_MODE: set PRPGs in scan0_mode but do not run automatic scan0 sequence
4:8	RW	SCAN_RATIO: scan_ratio (n=0-15: (n+1):1, 16: 24:1, 17: 32:1, 18: 48:1, 19: 64:1, 20: 128:1)
9	RW	INOP_FORCE_SG: Set SG high during INOP
10:13	RW	INOP_ALIGN: INOP phase alignment (0: none, 1: 2:1, 2: 3:1, 3: 4:1, 4: 6:1, 5: 8:1, 6: 12:1, 7: 16:1, 8: 24:1)
14:20	RW	INOP_WAIT: INOP cycle delay (1-127)
21:24	RWX	SNOP_ALIGN: BIST mode: SNOP phase alignment (like INOP), runn-mode: loopcnt(0:3)
25:27	RWX	SNOP_WAIT: BIST mode: SNOP cycle delay (0-7), runn-mode: loopcnt(4:6)
28:31	RWX	ENOP_ALIGN: BIST mode: ENOP phase alignment (like INOP), runn-mode: loopcnt(7:10)

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Bits	PCB	Field Mnemonic: Description
32:34	RWX	ENOP_WAIT: BIST mode: ENOP cycle delay (0-7), runn-mode: loopcnt(11:13)
35	RWX	ENOP_FORCE_SG: BIST mode: Set SG high during ENOP, runn-mode: loopcnt(14)
36:63	RWX	LOOP_COUNT: BIST mode: loop count ($l = 1-2^{28}$ (about 5 minutes LBIST)), runn-mode: loopcnt(15:42)

Register Name	OPCG Control Register 1
Mnemonic	ES.PE_WRAP_TOP.TPC.OPCG_REG1
Address	0000000009030003 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	FUNC_CAPT_COUNT: BIST mode: capture cycles (1-12) encoded as capture cycle - 1
4:8	RW	FUNC_CAPT_SEQ01_01F: BIST mode: capture cycle 1 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
9:13	RW	FUNC_CAPT_SEQ02_02F: BIST mode: capture cycle 2 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
14:18	RW	FUNC_CAPT_SEQ03_03F: BIST mode: capture cycle 3 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
19:23	RW	FUNC_CAPT_SEQ04_04F: BIST mode: capture cycle 4 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
24:28	RW	FUNC_CAPT_SEQ05_05F: BIST mode: capture cycle 5 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
29:33	RW	FUNC_CAPT_SEQ06_06F: BIST mode: capture cycle 6 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
34:38	RW	FUNC_CAPT_SEQ07_07F: BIST mode: capture cycle 7 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
39:43	RW	FUNC_CAPT_SEQ08_08F: BIST mode: capture cycle 8 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
44:48	RW	FUNC_CAPT_SEQ09_01FBY2: BIST mode: capture cycle 1 for slow domain or cycle 9 for single mesh support(sl, nsl, ary, sg, fce)
49:53	RW	FUNC_CAPT_SEQ10_02FBY2: BIST mode: capture cycle 2 for slow domain or cycle 10 for single mesh support(sl, nsl, ary, sg, fce)
54:58	RW	FUNC_CAPT_SEQ11_03FBY2: BIST mode: capture cycle 3 for slow domain or cycle 11 for single mesh support(sl, nsl, ary, sg, fce)
59:63	RW	FUNC_CAPT_SEQ12_04FBY2: BIST mode: capture cycle 4 for slow domain or cycle 12 for single mesh support(sl, nsl, ary, sg, fce)

Register Name	OPCG Control Register 2
Mnemonic	ES.PE_WRAP_TOP.TPC.OPCG_REG2
Address	0000000009030004 (PCB)
Attributes	
Description	



Bits	PCB	Field Mnemonic: Description
0:11	RW	SCAN_COUNT: BIST mode: Channel scan count (s = 0-4095) runn-mode: start_abist match value(0:11)
12:23	RW	MISR_A_VAL: BIST mode: a value for MISR aperture, runn-mode: start_abist match value(12:23)
24:35	RW	MISR_B_VAL: BIST mode: b value for MISR aperture, runn-mode: start_abist match value(24:35)
36:47	RW	MISR_INIT_WAIT: BIST mode: delay MISR aperture, MISRs get active after this number of loops
48	RW	OPCG_SUPPRESS_EVEN_CLK: OPCG will only create even and not odd clocks. Used for runn to create only one clock in fast domain. Default is 0

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Bits	PCB	Field Mnemonic: Description
49:51	RW	OPCG_PAD_VALUE: After setting all DC signals, wait this many number of cycle x 16 before applying tholds
52	RW	USE_F_AND_FDIV2: BIST mode: if 1, use 8 f and 4 f/2 pattern concurrently, else use 1-12 local mesh patterns
53	RW	USE_ARY_CLK_DURING_FILL: BIST mode: Fire nsl_ary_clock during NSL-fill runn-mode: stop run-n on xstop
54	RW	SG_HIGH_DURING_FILL: BIST mode: Hold SG high during NSL-fill runn-mode: OPCG engine controls start_abist (overrides GP0 setting)
55	RW	RTIM_THOLD_FORCE: force rtim_thold low when not in test_dc mode (must be 0 at all time)
56	RW	LBIST_SKITTER_CTL: BIST mode: 0: enable skitter during lbist_ip, 1: enable skitter when misr_active
57	RW	MISR_MODE: BIST mode: MISR aperture mode (0: a-1 to b-1, 1: start to a and b to end)
58	RW	INFINITE_MODE: infinite mode
59:63	RW	NSL_FILL_COUNT: BIST mode: NSL-fill count (0-31)

Register Name	Opcg Start Register
Mnemonic	ES.PE_WRAP_TOP.TPC.OPCG_REG3
Address	0000000009030005 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	OPCG_GO2: opcg go for broadcast sequences (start sequence)
1	RW	RUN_OPCG_ON_UPDATE_DR: start opcg engine when scan updated (update_dr) received (set pulse)
2	RW	RUN_OPCG_ON_CAPTURE_DR: start opcg engine when scan updated (capture_dr) received (set pulse)
3:4	RW	ALIGN_SOURCE_SELECT: 0: Use inopa setting from opcg_reg0 1: Use rising edge of sync pulse 2: Use input from unit (for AVP)
5:7	RW	PRPG_WEIGHTING: prpg_activate: 1/2, 1/4, 1/8, 1/16, 1/2, 3/4, 7/8, 15/16
8:19	RWX	PRPG_VALUE: Set to 0 for prpg always on, else seed
20	RW	EXTEND_INOPW_ENOPW: Extend I/ENOPW: add 256 cycles if i/enopw>0, else 257+max i/enop
21	RW	EXTEND_SNOPW: Add 256 cycles if snop>0, else 257+max snop
22	RW	FORCE_SG_HIGH_DURING_SNOP: force sg high during snop
23:31	RW	CHKSW: Reserved for debug switches (keep 0 unless chksw required).
32:43	RW	PRPG_A_VAL: a value for PRPG aperture
44:55	RW	PRPG_B_VAL: b value for PRPG aperture
56	RW	PRPG_MODE: PRPG aperture mode (0: a-1 to b-1, 1: start to a and b to end)
57	RW	SCAN_CLK_USE_EVEN: Generate scan clock in odd cycle instead of even. Default is 0.
58	RWX	AUTO_SCAN0: Runs a full scan0 on chiplet to clear all data.
59:63	RW	SPARE3: Spares.



Register Name		<i>Start/Stop of Clocks</i>
Mnemonic		ES.PE_WRAP_TOP.TPC.CLK_REGION
Address		0000000009030006 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:1	RWX	CLOCK_CMD: command for clock control: 00 NOP 01 START 10 STOP 11 PULSE (one pulse)
2:3	RO	Constant = 0b00
4	RWX	CLOCK_REGION_PERV: for clock region perv (Pervasive)
5	RWX	CLOCK_REGION_UNIT0: for clock region pci0
6	RWX	CLOCK_REGION_UNIT1: for clock region pci1
7	RWX	CLOCK_REGION_UNIT2: for clock region pci2
8	RWX	CLOCK_REGION_UNIT3: for clock region unit3 region is UNUSED
9	RWX	CLOCK_REGION_UNIT4: for clock region iopci
10	RWX	CLOCK_REGION_UNIT5: for clock region pbf
11	RWX	CLOCK_REGION_PLL: for clock region pll
12	RWX	CLOCK_REGION_OSCSW: for clock region oscsw region is UNUSED
13:19	RO	Constant = 0b0000000
20	RWX	SEL_THOLD_SL: select sl tholds
21	RWX	SEL_THOLD_NSL: select nsl tholds
22	RWX	SEL_THOLD_ARY: select array thold

Register Name		<i>Scan Region And Type</i>
Mnemonic		ES.PE_WRAP_TOP.TPC.SCANSELQ
Address		0000000009030007 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:2	RO	Constant = 0b000
3	RW_WCLRPA RT	SCANSEL_CLK_VITL: Scan clock region vital (vital = clock)
4	RWX	SCANSEL_CLK_PERV: Scan clock region pervasive
5	RWX	SCANSEL_CLK_UNIT0: Scan clock region pci0
6	RWX	SCANSEL_CLK_UNIT1: Scan clock region pci1
7	RWX	SCANSEL_CLK_UNIT2: Scan clock region pci2
8	RWX	SCANSEL_CLK_UNIT3: Scan clock region unit3 region is UNUSED
9	RWX	SCANSEL_CLK_UNIT4: Scan clock region iopci
10	RWX	SCANSEL_CLK_UNIT5: Scan clock region pbf
11	RWX	SCANSEL_CLK_PLL: Scan clock region pll
12	RWX	SCANSEL_CLK_OSCSW: Scan clock region oscsw region is UNUSED

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Bits	PCB	Field Mnemonic: Description
13:19	RO	Constant = 0b00000000
20	RW	SCANSEL_FUNC: Scan chain functional
21	RW	SCANSEL_CFG: Scan chain mode (boot config and debug config)
22	RW	SCANSEL_CCFG_GPTR: Scan chain ccfg / gptra (Pervasive: CC config, Others: GPTR)
23	RW	SCANSEL_REGF: Scan chain register files
24	RW	SCANSEL_LBIST: Scan chain LBIST
25	RW	SCANSEL_ABIST: Scan chain ABIST
26	RW	SCANSEL_REPR: Scan chain repr (Array Repair)
27	RW	SCANSEL_TIME: Scan chain time (Array Timing)
28	RW	SCANSEL_BNDY: Scan chain bndy (Boundary I/O's)
29	RW	SCANSEL_FARR: Scan chain fast array unload
30	RW	SCANSEL_CMSK: Scan chain cmsk (lbist channel mask)

Register Name	<i>Clocks Running</i>
Mnemonic	ES.PE_WRAP_TOP.TPC.CLOCK_STAT
Address	0000000009030008 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	CLOCK_STATUS_PERV_FUNC_SL: Status of perv func_sl_thold 0 = Run 1 = Stop
1	ROX	CLOCK_STATUS_PERV_FUNC_NSL: Status of perv func_nsl_thold 0 = Run 1 = Stop
2	ROX	CLOCK_STATUS_PERV_ARY_NSL: Status of perv ary_nsl_thold 0 = Run 1 = Stop
3	ROX	CLOCK_STATUS_UNIT0_FUNC_SL: Status of pci0 func_sl_thold 0 = Run 1 = Stop
4	ROX	CLOCK_STATUS_UNIT0_FUNC_NSL: Status of pci0 func_nsl_thold 0 = Run 1 = Stop
5	ROX	CLOCK_STATUS_UNIT0_ARY_NSL: Status of pci0 ary_nsl_thold 0 = Run 1 = Stop
6	ROX	CLOCK_STATUS_UNIT1_FUNC_SL: Status of pci1 func_sl_thold 0 = Run 1 = Stop
7	ROX	CLOCK_STATUS_UNIT1_FUNC_NSL: Status of pci1 func_nsl_thold 0 = Run 1 = Stop



Bits	PCB	Field Mnemonic: Description
8	ROX	CLOCK_STATUS_UNIT1_ARY_NSL: status of pci1 ary_nsl_thold 0 = Run 1 = Stop
9	ROX	CLOCK_STATUS_UNIT2_FUNC_SL: status of pci2 func_sl_thold 0 = Run 1 = Stop
10	ROX	CLOCK_STATUS_UNIT2_FUNC_NSL: status of pci2 func_nsl_thold 0 = Run 1 = Stop
11	ROX	CLOCK_STATUS_UNIT2_ARY_NSL: status of pci2 ary_nsl_thold 0 = Run 1 = Stop
12	ROX	CLOCK_STATUS_UNIT3_FUNC_SL: status of unit3 func_sl_thold 0 = Run 1 = Stop, region is UNUSED
13	ROX	CLOCK_STATUS_UNIT3_FUNC_NSL: status of unit3 func_nsl_thold 0 = Run 1 = Stop, region is UNUSED
14	ROX	CLOCK_STATUS_UNIT3_ARY_NSL: status of unit3 ary_nsl_thold 0 = Run 1 = Stop, region is UNUSED
15	ROX	CLOCK_STATUS_UNIT4_FUNC_SL: status of iopci func_sl_thold 0 = Run 1 = Stop
16	ROX	CLOCK_STATUS_UNIT4_FUNC_NSL: status of iopci func_nsl_thold 0 = Run 1 = Stop
17	ROX	CLOCK_STATUS_UNIT4_ARY_NSL: status of iopci ary_nsl_thold 0 = Run 1 = Stop
18	ROX	CLOCK_STATUS_UNIT5_FUNC_SL: status of pbf func_sl_thold 0 = Run 1 = Stop
19	ROX	CLOCK_STATUS_UNIT5_FUNC_NSL: status of pbf func_nsl_thold 0 = Run 1 = Stop
20	ROX	CLOCK_STATUS_UNIT5_ARY_NSL: status of pbf ary_nsl_thold 0 = Run 1 = Stop
21	ROX	CLOCK_STATUS_PLL_FUNC_SL: status of pll func_sl_thold 0 = Run 1 = Stop
22	ROX	CLOCK_STATUS_PLL_FUNC_NSL: status of pll func_nsl_thold 0 = Run 1 = Stop
23	ROX	CLOCK_STATUS_PLL_ARY_NSL: status of pll ary_nsl_thold 0 = Run 1 = Stop
24	ROX	CLOCK_STATUS_OSCSW_FUNC_SL: status of oscsw func_sl_thold 0 = Run 1 = Stop, region is UNUSED

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Bits	PCB	Field Mnemonic: Description
25	ROX	CLOCK_STATUS_OSCSW_FUNC_NSL: status of oscsw func_nsl_thold 0 = Run 1 = Stop, region is UNUSED
26	ROX	CLOCK_STATUS_OSCSW_ARY_NSL: status of oscsw ary_nsl_thold 0 = Run 1 = Stop, region is UNUSED
27:63	RO	Constant = 0b1111111111111111111111111111111111111111111111111111111111111111

Register Name	Error Status Of CC
Mnemonic	ES.PE_WRAP_TOP.TPC.ERROR_STATUS
Address	0000000009030009 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	PCB_WRITE_NOT_ALLOWED: PCB access error: write not allowed
1	RWX	PCB_READ_NOT_ALLOWED: PCB access error: read not allowed
2	RWX	PCB_PARITY_ERR_ON_CMD: PCB access error: parity error on PCB command
3	RWX	PCB_ADDRESS_NOT_VALID: PCB access error: address not valid
4	RWX	PCB_PARITY_ADDR_ERR: PCB access error: parity error on address
5	RWX	PCB_PARITY_DATA_ERR: PCB access error: parity error on data
6	RWX	PCB_PROTECTED_ACCESS_INVALID: PCB access error: protection violation
7	RWX	PCB_PARITY_SPCIF_ERR: parity error from special packet interface
8	RWX	PCB_WRITE_AND_OPCG: PCB write while opcg in progress
9	RWX	CLOCK_CMD_CONFLICT: Clock command conflict: previous one was not yet completed (includes those triggered by tc_sync_clk_stop)
10	RWX	SCAN_COLLISION: Scan collision
11	RWX	OPCG_TRIGGER_ERROR: opcg triggered while in progress
12	RWX	OPCG_PARITY_ERROR: opcg state machine parity error
13	RWX	PHASE_CNT_CORRUPTED: Phase hold counter corruption detected
14:15	RWX	CC_PAR_ERR: Parity error in CC registers (1. opcg & sync config parity error, 2. clock mux parity error)
16	RWX	GPIO_PAR_ERR: Parity error in GP0 register
17	RWX	SECURITY_VIOLATION: Security violation - when chip protection is active and a clock start or pulse is tried, which is invalid at this time

Register Name	CC Protect Mode Register
Mnemonic	ES.PE_WRAP_TOP.TPC.CC_PROTECT_MODE_REG
Address	00000000090303FE (PCB)
Attributes	
Description	



Bits	PCB	Field Mnemonic: Description
0	RW	CC_READ_PROTECT_ENABLE: Enable read protection
1	RW	CC_WRITE_PROTECT_ENABLE: Enable write protection

Register Name	Global Checkstop FIR
Mnemonic	ES.PE_WRAP_TOP.TPC.XFIR
Address	0000000009040000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	XFIR_IN0: summary bit(any xstop)
1	RWX	XFIR_IN1: xstop from other chiplets
2	RWX	XFIR_IN2: Unused
3	RWX	XFIR_IN3: xstop from pervasive unit
4	RWX	XFIR_IN4: xstop from pci0
5	RWX	XFIR_IN5: xstop from pci1
6	RWX	XFIR_IN6: xstop from pci2
7	RWX	XFIR_IN7: unused
8	RWX	XFIR_IN8: xstop from asynchronous foreign fabric (pbf)
9	RWX	XFIR_IN9: xstop from iopci0
10	RWX	XFIR_IN10: xstop from iopci1
11:25	RWX	XFIR_IN11: unused
26	RWX	XFIR_IN26: xstop on debug trigger and local_xstop to recoverable

Register Name	Global Recoverable FIR
Mnemonic	ES.PE_WRAP_TOP.TPC.RFIR
Address	0000000009040001 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	RFIR_IN0: local checkstop from PCI (informational)
1	ROX	LFIR_RECOV_ERR: recoverable error from pervasive unit
2	ROX	RFIR_IN4: recov from pci0
3	ROX	RFIR_IN5: recov from pci1
4	ROX	RFIR_IN6: recov from pci2
5	ROX	RFIR_IN7: unused
6	ROX	RFIR_IN8: recov from asynchronous foreign fabric (pbf)
7	ROX	RFIR_IN9: recov from iopci0
8	ROX	RFIR_IN10: recov from iopci1

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Bits	PCB	Field Mnemonic: Description
9:23	ROX	RFIR_IN11: unused

Register Name	<i>FIR Mask</i>
Mnemonic	ES.PE_WRAP_TOP.TPC.FIR_MASK
Address	0000000009040002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	FIR_MASK_IN0: mask for xfir summary bit(any xstop)
1	RW	FIR_MASK_IN1: mask for xfir from other chiplets
2	RW	FIR_MASK_IN2: Unused
3	RW	FIR_MASK_IN3: mask for xfir from pervasive unit
4	RW	FIR_MASK_IN4: mask for pci0 XFIR and RFIR
5	RW	FIR_MASK_IN5: mask for pci1 XFIR and RFIR
6	RW	FIR_MASK_IN6: mask for pci2 XFIR and RFIR
7	RW	FIR_MASK_IN7: unused
8	RW	FIR_MASK_IN8: mask for asynchronous foreign fabric (pbf) XFIR and RFIR
9	RW	FIR_MASK_IN9: mask for iopci0 XFIR and RFIR
10	RW	FIR_MASK_IN10: mask for iopci1 XFIR and RFIR
11:25	RW	FIR_MASK_IN11: unused
26	RW	FIR_MASK_IN26: mask for debug trigger and local xstop to recoverable error

Register Name	<i>Special Attention</i>
Mnemonic	ES.PE_WRAP_TOP.TPC.SPATTN
Address	0000000009040004 (PCB) 0000000009040005 (PCB1) 0000000009040006 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	ROX	NCX	NCX	SPATTN_IN0: Special Attention from PB foreign Fabric Asynchronous (dsmp)
1:9	ROX	NCX	NCX	SPATTN_IN1: unused special attentions

Register Name	<i>Special Attention Mask</i>
Mnemonic	ES.PE_WRAP_TOP.TPC.SPA_MASK
Address	0000000009040007 (PCB)
Attributes	
Description	



Bits	PCB	Field Mnemonic: Description
0:9	RW	SPA_MASK_IN: special attention mask

Register Name	<i>Mode Register</i>
Mnemonic	ES.PE_WRAP_TOP.TPC.EPS.FIR.MODE_REG
Address	0000000009040008 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	MODE_IN0: Enable Clockstop on Checkstop
1	RW	MODE_IN1: Enable Clockstop on Recoverable
2	RW	MODE_IN2: Enable Clockstop on Spattn
3	RW	MODE_IN3: Core-only Spattn
4	RW	MODE_IN4: Stop Chip TOD on Checkstop
5	RW	MODE_IN5: Stop Chip TOD on Recoverable
6	RW	MODE_IN6: Disable propagation of checkstop to other chips
7	RW	MODE_IN7: turns xstop on trig into clkstp on trig
8	RW	MODE_IN8: enable xstop on special attention
9	RW	MODE_IN9: mask_direct/local_error
10	RW	MODE_IN10: mask_xstop_to_pcb
11	RW	MODE_IN11: mask external xstop
12:15	RW	MODE_IN: unused

Register Name	<i>Local FIR</i>
Mnemonic	ES.PE_WRAP_TOP.TPC.LOCAL_FIR
Address	000000000904000A (PCB) 000000000904000B (PCB1) 000000000904000C (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_IN0: CFIR internal parity error
1	RWX	WOX_AND	WOX_OR	FIR_IN1: local errors from GPIO (PCB error)
2	RWX	WOX_AND	WOX_OR	FIR_IN2: local errors from CC (PCB error)
3	RWX	WOX_AND	WOX_OR	FIR_IN3: local errors from CC (OPCG, parity, scan collision, ...)
4	RWX	WOX_AND	WOX_OR	FIR_IN4: local errors from PSC (PCB error)
5	RWX	WOX_AND	WOX_OR	FIR_IN5: local errors from PSC (parity error)
6	RWX	WOX_AND	WOX_OR	FIR_IN6: local errors from Thermal (parity error)
7	RWX	WOX_AND	WOX_OR	FIR_IN7: local errors from Thermal (PCB error)
8	RWX	WOX_AND	WOX_OR	FIR_IN8: local errors from Thermal (Trip error critical)

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
9	RWX	WOX_AND	WOX_OR	FIR_IN9: local errors from Thermal (Trip error fatal)
10	RWX	WOX_AND	WOX_OR	FIR_IN10: local errors from Trace Array (error)
11	RWX	WOX_AND	WOX_OR	FIR_IN11: local errors from Trace Array (scom error)
12:39	RWX	WOX_AND	WOX_OR	FIR_IN12: unused local errors
40	RWX	WOX_AND	WOX_OR	FIR_IN40: malfunction alert (local xstop in another chiplet)

Register Name	Local FIR Mask			
Mnemonic	ES.PE_WRAP_TOP.TPC.EPS.FIR.LOCAL_FIR_MASK			
Address	000000000904000D (PCB) 000000000904000E (PCB1) 000000000904000F (PCB2)			
Attributes				
Description				

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0:40	RW	WO_AND	WO_OR	LFIR_MASK_IN: mask for LEM error collection vector

Register Name	Local FIR Action0			
Mnemonic	ES.PE_WRAP_TOP.TPC.EPS.FIR.LOCAL_FIR_ACTION0			
Address	0000000009040010 (PCB)			
Attributes				
Description				

Bits	PCB	Field Mnemonic: Description
0:40	RW	FIR_ACTION0_IN: action0 mask

Register Name	Local FIR Action1			
Mnemonic	ES.PE_WRAP_TOP.TPC.EPS.FIR.LOCAL_FIR_ACTION1			
Address	0000000009040011 (PCB)			
Attributes				
Description				

Bits	PCB	Field Mnemonic: Description
0:40	RW	FIR_ACTION1_IN: action1 mask

Register Name	Processor Bus PBES IOF Domain FIR0 Register			
Mnemonic	ES.PBES_WRAP_TOP.PBES_TOP.MISC_IOF.SCOM.PB_IOF_FIR_REG			
Address	0000000009010800 (SCOM) 0000000009010801 (SCOM1) 0000000009010802 (SCOM2)			
Attributes				
Description				



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:3	RWX	WOX_AND	WOX_OR	F0_MAILBOX_WRITTEN: f0 mailbox written(0:3)
4	RWX	WOX_AND	WOX_OR	F0_RX_DETECT: f0 rx detect
5	RWX	WOX_AND	WOX_OR	F0_LINK_TRAINING_DONE: f0 link training done
6	RWX	WOX_AND	WOX_OR	F0LINK_TRAINED: f0link trained
7	RWX	WOX_AND	WOX_OR	F0LINK_FIR_ERR: f0link fir err
8	RWX	WOX_AND	WOX_OR	F0LINK_FMR_PSR_OBS_ERR: f0link fmr psr obs err - see pb_iof0_err_detail for details, and clear that register before attempting to clear this bit.
9	RWX	WOX_AND	WOX_OR	F0LINK_FMR_COR_ERR: f0link outbound correctable data err
10	RWX	WOX_AND	WOX_OR	F0LINK_FMR_SUE_ERR: f0link outbound Special UE data err
11	RWX	WOX_AND	WOX_OR	F0LINK_FMR_UNC_ERR: f0link outbound uncorrectable data err
12	RWX	WOX_AND	WOX_OR	F0_EQ_FAILED: f0 eq failed
13	RWX	WOX_AND	WOX_OR	F0_REPLAY_THRESHOLD: f0 replay threshold
14	RWX	WOX_AND	WOX_OR	F0_CRC_ERROR: f0 CRC Error
15	RWX	WOX_AND	WOX_OR	F0_LOST_PACKET: f0 Lost Packet
16	RWX	WOX_AND	WOX_OR	F0_NAK_RECEIVED: f0 Nak Received
17	RWX	WOX_AND	WOX_OR	F0_REPLAY_TIMER_ERROR: f0 Replay Timer error
18	RWX	WOX_AND	WOX_OR	F0_RETRAIN_THRESHOLD: f0 retrain threshold
19	RWX	WOX_AND	WOX_OR	F0_REPLAY_NUM_RETRAIN: f0 Replay Num retrain
20	RWX	WOX_AND	WOX_OR	F0_RX_ERROR: f0 rx error
21	RWX	WOX_AND	WOX_OR	F0_DESKEW_ERROR: f0 deskew error
22	RWX	WOX_AND	WOX_OR	F0_FRAMING_ERROR: f0 framing error
23	RWX	WOX_AND	WOX_OR	F0_OS_RECEIVED: f0 OS received
24	RWX	WOX_AND	WOX_OR	F0_ECC_CE_ERR: f0 ecc ce/rec buf overrun err
25	RWX	WOX_AND	WOX_OR	F0_ECC_UE_ERR: f0 ecc ue err
26	RWX	WOX_AND	WOX_OR	F0_RETRAIN_ERR: f0 retrain err
27	RWX	WOX_AND	WOX_OR	F0_TRAINING_ERR: f0 training err
28	RWX	WOX_AND	WOX_OR	F0_UNRECOV_ERR: f0 unrecov err
29	RWX	WOX_AND	WOX_OR	F0_INTERNAL_ERR: f0 internal err
30	RWX	WOX_AND	WOX_OR	F0_REPLAY_FULL_ERROR: f0 replay full err
31	RWX	WOX_AND	WOX_OR	F1_REPLAY_FULL_ERROR: f1 replay full err
32:35	RWX	WOX_AND	WOX_OR	F1_MAILBOX_WRITTEN: f1 mailbox written(0:3)
36	RWX	WOX_AND	WOX_OR	F1_RX_DETECT: f1 rx detect
37	RWX	WOX_AND	WOX_OR	F1_LINK_TRAINING_DONE: f1 link training done
38	RWX	WOX_AND	WOX_OR	F1LINK_TRAINED: f1link trained
39	RWX	WOX_AND	WOX_OR	F1LINK_FIR_ERR: f1link fir err
40	RWX	WOX_AND	WOX_OR	F1LINK_FMR_PSR_OBS_ERR: f1link fmr psr obs err - see pb_iof1_err_detail for details, and clear that register before attempting to clear this bit.
41	RWX	WOX_AND	WOX_OR	F1LINK_FMR_COR_ERR: f1link outbound correctable data err
42	RWX	WOX_AND	WOX_OR	F1LINK_FMR_SUE_ERR: f1link outbound Special UE data err

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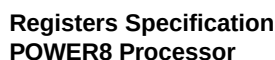
Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
43	RWX	WOX_AND	WOX_OR	F1LINK_FMR_UNC_ERR: f1link outbound uncorrectable data err
44	RWX	WOX_AND	WOX_OR	F1_EQ_FAILED: f1 eq failed
45	RWX	WOX_AND	WOX_OR	F1_REPLAY_THRESHOLD: f1 replay threshold
46	RWX	WOX_AND	WOX_OR	F1_CRC_ERROR: f1 CRC Error
47	RWX	WOX_AND	WOX_OR	F1_LOST_PACKET: f1 Lost Packet
48	RWX	WOX_AND	WOX_OR	F1_NAK_RECEIVED: f1 Nak Received
49	RWX	WOX_AND	WOX_OR	F1_REPLAY_TIMER_ERROR: f1 Replay Timer error
50	RWX	WOX_AND	WOX_OR	F1_RETRAIN_THRESHOLD: f1 retrain threshold
51	RWX	WOX_AND	WOX_OR	F1_REPLAY_NUM_RETRAIN: f1 Replay Num retrain
52	RWX	WOX_AND	WOX_OR	F1_RX_ERROR: f1 rx error
53	RWX	WOX_AND	WOX_OR	F1_DESKEW_ERROR: f1 deskew error
54	RWX	WOX_AND	WOX_OR	F1_FRAMING_ERROR: f1 framing error
55	RWX	WOX_AND	WOX_OR	F1_OS_RECEIVED: f1 OS received
56	RWX	WOX_AND	WOX_OR	F1_ECC_CE_ERR: f1 ecc ce/rec buf overrun err
57	RWX	WOX_AND	WOX_OR	F1_ECC_UE_ERR: f1 ecc ue err
58	RWX	WOX_AND	WOX_OR	F1_RETRAIN_ERR: f1 retrain err
59	RWX	WOX_AND	WOX_OR	F1_TRAINING_ERR: f1 training err
60	RWX	WOX_AND	WOX_OR	F1_UNRECOV_ERR: f1 unrecov err
61	RWX	WOX_AND	WOX_OR	F1_INTERNAL_ERR: f1 internal err
62	RWX	WOX_AND	WOX_OR	Reserved field. (Access type is FIR_SCOM_err_dup)
63	RWX	WOX_AND	WOX_OR	Reserved field. (Access type is FIR_SCOM_err)

Register Name	Processor Bus PBES IOF Domain FIR MASK Register
Mnemonic	ES.PBES_WRAP_TOP.PBES_TOP.MISC_IOF.SC.COM.PB_IOF_FIR_MASK_REG
Address	0000000009010803 (SCOM) 0000000009010804 (SCOM1) 0000000009010805 (SCOM2)
Attributes	
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:3	RW	WO_AND	WO_OR	F0_MAILBOX_WRITTEN_MASK: f0 mailbox written mask(0:3)
4	RW	WO_AND	WO_OR	F0_RX_DETECT_MASK: f0 rx detect mask
5	RW	WO_AND	WO_OR	F0_LINK_TRAINING_DONE_MASK: f0 link training done mask
6	RW	WO_AND	WO_OR	F0LINK_TRAINED_MASK: f0link trained mask
7	RW	WO_AND	WO_OR	F0LINK_FIR_ERR_MASK: f0link fir err mask
8	RW	WO_AND	WO_OR	F0LINK_FMR_PSR_OBS_ERR_MASK: f0link fmr psr err mask
9	RW	WO_AND	WO_OR	F0LINK_FMR_COR_ERR_MASK: f0link outbound correctable data err mask
10	RW	WO_AND	WO_OR	F0LINK_FMR_SUE_ERR_MASK: f0link outbound Special UE data err mask



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
11	RW	WO_AND	WO_OR	F0LINK_FMR_UNC_ERR_MASK: f0link outbound uncorrectable data err mask
12	RW	WO_AND	WO_OR	F0_EQ_FAILED_MASK: f0 eq failed mask
13	RW	WO_AND	WO_OR	F0_REPLAY_THRESHOLD_MASK: f0 replay threshold mask
14	RW	WO_AND	WO_OR	F0_CRC_ERROR_MASK: f0 CRC Error mask
15	RW	WO_AND	WO_OR	F0_LOST_PACKET_MASK: f0 Lost Packet mask
16	RW	WO_AND	WO_OR	F0_NAK_RECEIVED_MASK: f0 Nak Received mask
17	RW	WO_AND	WO_OR	F0_REPLAY_TIMER_ERROR_MASK: f0 Replay Timer error mask
18	RW	WO_AND	WO_OR	F0_RETRAIN_THRESHOLD_MASK: f0 retrain threshold mask
19	RW	WO_AND	WO_OR	F0_REPLAY_NUM_RETRAIN_MASK: f0 Replay Num retrain mask
20	RW	WO_AND	WO_OR	F0_RX_ERROR_MASK: f0 rx error mask
21	RW	WO_AND	WO_OR	F0_DESKEW_ERROR_MASK: f0 deskew error mask
22	RW	WO_AND	WO_OR	F0_FRAMING_ERROR_MASK: f0 framing error mask
23	RW	WO_AND	WO_OR	F0_OS_RECEIVED_MASK: f0 OS received mask
24	RW	WO_AND	WO_OR	F0_ECC_CE_ERR_MASK: f0 ecc ce/rec buf overrun err mask
25	RW	WO_AND	WO_OR	F0_ECC_UE_ERR_MASK: f0 ecc ue err mask
26	RW	WO_AND	WO_OR	F0_RETRAIN_ERR_MASK: f0 retrain err mask
27	RW	WO_AND	WO_OR	F0_TRAINING_ERR_MASK: f0 training err mask
28	RW	WO_AND	WO_OR	F0_UNRECOV_ERR_MASK: f0 unrecov err mask
29	RW	WO_AND	WO_OR	F0_INTERNAL_ERR_MASK: f0 internal err mask
30	RW	WO_AND	WO_OR	F0_REPLAY_FULL_ERROR_MASK: f0 replay full err mask
31	RW	WO_AND	WO_OR	F1_REPLAY_FULL_ERROR_MASK: f1 replay full err mask
32:35	RW	WO_AND	WO_OR	F1_MAILBOX_WRITTEN_MASK: f1 mailbox written mask(0:3)
36	RW	WO_AND	WO_OR	F1_RX_DETECT_MASK: f1 rx detect mask
37	RW	WO_AND	WO_OR	F1_LINK_TRAINING_DONE_MASK: f1 link training done mask
38	RW	WO_AND	WO_OR	F1LINK_TRAINED_MASK: f1link trained mask
39	RW	WO_AND	WO_OR	F1LINK_FIR_ERR_MASK: f1link fir err mask
40	RW	WO_AND	WO_OR	F1LINK_FMR_PSR_OBS_ERR_MASK: f1link fmr psr err mask
41	RW	WO_AND	WO_OR	F1LINK_FMR_COR_ERR_MASK: f1link outbound correctable data err mask
42	RW	WO_AND	WO_OR	F1LINK_FMR_SUE_ERR_MASK: f1link outbound Special UE data err mask
43	RW	WO_AND	WO_OR	F1LINK_FMR_UNC_ERR_MASK: f1link outbound uncorrectable data err mask
44	RW	WO_AND	WO_OR	F1_EQ_FAILED_MASK: f1 eq failed mask
45	RW	WO_AND	WO_OR	F1_REPLAY_THRESHOLD_MASK: f1 replay threshold mask
46	RW	WO_AND	WO_OR	F1_CRC_ERROR_MASK: f1 CRC Error mask
47	RW	WO_AND	WO_OR	F1_LOST_PACKET_MASK: f1 Lost Packet mask
48	RW	WO_AND	WO_OR	F1_NAK_RECEIVED_MASK: f1 Nak Received mask
49	RW	WO_AND	WO_OR	F1_REPLAY_TIMER_ERROR_MASK: f1 Replay Timer error mask
50	RW	WO_AND	WO_OR	F1_RETRAIN_THRESHOLD_MASK: f1 retrain threshold mask



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
51	RW	WO_AND	WO_OR	F1_REPLAY_NUM_RETRAIN_MASK: f1 Replay Num retrain mask
52	RW	WO_AND	WO_OR	F1_RX_ERROR_MASK: f1 rx error mask
53	RW	WO_AND	WO_OR	F1_DESKEW_ERROR_MASK: f1 deskew error mask
54	RW	WO_AND	WO_OR	F1_FRAMING_ERROR_MASK: f1 framing error mask
55	RW	WO_AND	WO_OR	F1_OS_RECEIVED_MASK: f1 OS received mask
56	RW	WO_AND	WO_OR	F1_ECC_CE_ERR_MASK: f1 ecc ce/rec buf overrun err mask
57	RW	WO_AND	WO_OR	F1_ECC_UE_ERR_MASK: f1 ecc ue err mask
58	RW	WO_AND	WO_OR	F1_RETRAIN_ERR_MASK: f1 retrain err mask
59	RW	WO_AND	WO_OR	F1_TRAINING_ERR_MASK: f1 training err mask
60	RW	WO_AND	WO_OR	F1_UNRECOV_ERR_MASK: f1 unrecov err mask
61	RW	WO_AND	WO_OR	F1_INTERNAL_ERR_MASK: f1 internal err mask
62	RW	WO_AND	WO_OR	Reserved field. (Access type is FIR_SCOM_err_dup_mask)
63	RW	WO_AND	WO_OR	Reserved field. (Access type is FIR_SCOM_err_mask)

Register Name	<i>FIR Status Register</i>
Mnemonic	IOP.IOP_X880.IOP_PMA0.IOP_PMA_PLL0.IOP_PMA_PLL_RLM.IOP_PMA_PLL_REG_CONTROL.FIR_STATUS_REG
Address	0000000009011400 (SCOM) 0000000009011401 (SCOM1) 0000000009011402 (SCOM2)
Attributes	
Description	Fault Isolation Status Register : Addr=00h:RW, Addr=01h:Clear, Addr=02h:Set

[illegible]



Register Name	<i>FIR Mask Register</i>
Mnemonic	IOP.IOP_X880.IOP_PMA0.IOP_PMA_PLL0.IOP_PMA_PLL_RLM.IOP_PMA_PLL_REG_CONTROL.FIR_MASK_REG
Address	0000000009011403 (SCOM) 0000000009011404 (SCOM1) 0000000009011405 (SCOM2)
Attributes	
Description	Fault Isolation Mask Register : Addr=03h:RW, Addr=04h:Clear, Addr=05h:Set

[illegible]

Register Name	<i>FIR Action 0 Register</i>
Mnemonic	IOP.IOP_X880.IOP_PMA0.IOP_PMA_PLL0.IOP_PMA_PLL_RLM.IOP_PMA_PLL_REG_CONTROL.FIR_ACTION0_REG
Address	000000009011406 (SCOM)
Attributes	
Description	Action 0 Select for the FIR bits

[illegible]

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Register Name	<i>FIR Action 1 Register</i>
Mnemonic	IOP.IOP_X880.IOP_PMA0.IOP_PMA_PLL0.IOP_PMA_PLL_RLM.IOP_PMA_PLL_REG_CONTROL.FIR_ACTION1_REG
Address	0000000009011407 (SCOM)
Attributes	
Description	Action 1 Select for the FIR bits

Bits	SCOM	Field Mnemonic: Description
0:8	RO	FIR_ACTION1_REG_ACTION1: Fault Isolation Action 1 Register MSB of action select for corresponding bit in FIR (Action0, Action1, Mask) = Action Select (0,0,x) = Checkstop Error (0,1,0) = Recoverable Error (1,0,0) = Recoverable Interrupt (1,1,0) = Machine Check (x,x,1) = Masked
9:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>FIR WOF Register</i>
Mnemonic	IOP.IOP_X880.IOP_PMA0.IOP_PMA_PLL0.IOP_PMA_PLL_RLM.IOP_PMA_PLL_REG_CONTROL.FIR_WOF_REG
Address	0000000009011408 (SCOM)
Attributes	
Description	Who is on first register indicates which error occurred first

Bits	SCOM	Field Mnemonic: Description
0:8	RWX_WCLRR EG	FIR_WOF_REG_WOF: WOF Register locks on first error
9:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>FIR Status Register</i>
Mnemonic	IOP.IOP_X881.IOP_PMA0.IOP_PMA_PLL0.IOP_PMA_PLL_RLM.IOP_PMA_PLL_REG_CONTROL.FIR_STATUS_REG
Address	0000000009011840 (SCOM) 0000000009011841 (SCOM1) 0000000009011842 (SCOM2)
Attributes	
Description	Fault Isolation Status Register : Addr=00h:RW, Addr=01h:Clear, Addr=02h:Set

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_G2_PLL_CCERR_STATUS: FIR Status Register : G2 PLL Calibration Error
1	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_G3_PLL_CCERR_STATUS: FIR Status Register : G3 PLL Calibration Error
2	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_TX_A_ERR_STATUS: FIR Status Register : TX A Bifurcate Calibration Error
3	RWX	WOX_AND	WOX_OR	FIR_STATUS_REG_TX_B_ERR_STATUS: FIR Status Register : TX B Bifurcate Calibration Error

[illegible]

Register Name	<i>FIR Mask Register</i>
Mnemonic	IOP.IOP_X881.IOP_PMA0.IOP_PMA_PLL0.IOP_PMA_PLL_RLM.IOP_PMA_PLL_REG_CONTROL.FIR_MASK_REG
Address	0000000009011843 (SCOM) 0000000009011844 (SCOM1) 0000000009011845 (SCOM2)
Attributes	
Description	Fault Isolation Mask Register : Addr=03h:RW, Addr=04h:Clear, Addr=05h:Set

[illegible]

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Register Name	<i>FIR Action 0 Register</i>
Mnemonic	IOP.IOP_X881.IOP_PMA0.IOP_PMA_PLL0.IOP_PMA_PLL_RLM.IOP_PMA_PLL_REG_CONTROL.FIR_ACTION0_REG
Address	0000000009011846 (SCOM)
Attributes	
Description	Action 0 Select for the FIR bits

Bits	SCOM	Field Mnemonic: Description
0:8	RO	FIR_ACTION0_REG_ACTION0: Fault Isolation Action 0 Register MSB of action select for corresponding bit in FIR (Action0, Action1, Mask) = Action Select (0,0,x) = Checkstop Error (0,1,0) = Recoverable Error (1,0,0) = Recoverable Interrupt (1,1,0) = Machine Check (x,x,1) = Masked
9:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>FIR Action 1 Register</i>
Mnemonic	IOP.IOP_X881.IOP_PMA0.IOP_PMA_PLL0.IOP_PMA_PLL_RLM.IOP_PMA_PLL_REG_CONTROL.FIR_ACTION1_REG
Address	0000000009011847 (SCOM)
Attributes	
Description	Action 1 Select for the FIR bits

Bits	SCOM	Field Mnemonic: Description
0:8	RO	FIR_ACTION1_REG_ACTION1: Fault Isolation Action 1 Register MSB of action select for corresponding bit in FIR (Action0, Action1, Mask) = Action Select (0,0,x) = Checkstop Error (0,1,0) = Recoverable Error (1,0,0) = Recoverable Interrupt (1,1,0) = Machine Check (x,x,1) = Masked
9:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>FIR WOF Register</i>
Mnemonic	IOP.IOP_X881.IOP_PMA0.IOP_PMA_PLL0.IOP_PMA_PLL_RLM.IOP_PMA_PLL_REG_CONTROL.FIR_WOF_REG
Address	0000000009011848 (SCOM)
Attributes	
Description	Who is on first register indicates which error occurred first

Bits	SCOM	Field Mnemonic: Description
0:8	RWX_WCLRR EG	FIR_WOF_REG_WOF: WOF Register locks on first error
9:63	RO	Constant = 0b0000000000000000000000000000000000000000000000000000000000000000



Register Name		<i>Lock Indications From PLLs</i>
Mnemonic		EH.TPCHIP.NET.PCBSLPCI.PLL_LOCK_REG
Address		00000000090F0019 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:3	ROX	Reserved field. (Access type is lock)

Register Name		<i>Write Configuration Data To Cpm 0-3</i>
Mnemonic		ES.PE_WRAP_TOP.TPC.EPS.THERM.CPM_CONFIG_WRITE_REG0
Address		0000000009050000 (PCB)
Attributes		
Description		0-11: CPM0, 12-23: CPM1, 24-35: CPM2

Bits	PCB	Field Mnemonic: Description
0:11	WOX	CPM0_CONFIG_DATA: Address ending in: 0x00 contains CPM0 CONFIG_DATA 0x01 contains CPM0 ENCODED value indicating location of edge in 12-bit sampler 15 means all ones 0 means 0b100000000000 1 means 0b110000000000 2 means 0b111000000000 3 means 0b111100000000 4 means 0b111110000000 5 means 0b111111000000 6 means 0b111111100000 7 means 0b111111110000 8 means 0b111111111000 9 means 0b111111111100 10 means 0b111111111110 11 means 0b111111111111 0x02 contains CPM0 RAW value of the actual 12-bit sampler
12:15	N/A	Not implemented.
16:27	WOX	CPM1_CONFIG_DATA: Address ending in: 0x00 contains CPM1 CONFIG_DATA 0x01 contains CPM1 ENCODED value indicating location of edge in 12-bit sampler 15 means all ones 0 means 0b100000000000 1 means 0b110000000000..... 11 means 0b111111111111 0x02 contains CPM1 RAW value of the actual 12-bit sampler CPM1 is only available in EX core chiplets
28:31	N/A	Not implemented.
32:43	WOX	CPM2_CONFIG_DATA: Address ending in: 0x00 contains CPM2 CONFIG_DATA 0x01 contains CPM2 ENCODED value indicating location of edge in 12-bit sampler 15 means all ones 0 means 0b100000000000 1 means 0b110000000000..... 11 means 0b111111111111 0x02 contains CPM2 RAW value of the actual 12-bit sampler CPM2 is only available in EX core chiplets

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Bits	PCB	Field Mnemonic: Description
44:63	N/A	Not implemented.

Register Name	<i>DTS Thermal Sensor Loop1 Results</i>
Mnemonic	ES.PE_WRAP_TOP.TPC.EPS.THERM.DTS_RESULT0
Address	0000000009050000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:15	ROX	DTS_0_RESULT: Calibrated DTS Result of sensor with ID 0.
16:31	ROX	DTS_1_RESULT: Calibrated DTS Result of sensor with ID 1.
32:47	ROX	DTS_2_RESULT: Calibrated DTS Result of sensor with ID 2.
48:63	RO	Constant = 0b0000000000000000

Register Name	<i>Multicast Group 1</i>
Mnemonic	EH.TPCHIP.NET.PCBSLPCI.MULTICAST_GROUP_1
Address	00000000090F0001 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	Constant = 0b111
3:5	RW	MULTICAST1_GROUP: multicast group1 setting

Register Name	<i>Multicast Group 2</i>
Mnemonic	EH.TPCHIP.NET.PCBSLPCI.MULTICAST_GROUP_2
Address	00000000090F0002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	Constant = 0b111
3:5	RW	MULTICAST2_GROUP: multicast group2 setting

Register Name	<i>Multicast Group 3</i>
Mnemonic	EH.TPCHIP.NET.PCBSLPCI.MULTICAST_GROUP_3
Address	00000000090F0003 (PCB)
Attributes	
Description	



Bits	PCB	Field Mnemonic: Description
0:2	RO	Constant = 0b111
3:5	RW	MULTICAST3_GROUP: multicast group3 setting

Register Name	Multicast Group 4
Mnemonic	EH.TPCHIP.NET.PCBSLPCI.MULTICAST_GROUP_4
Address	00000000090F0004 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	Constant = 0b111
3:5	RW	MULTICAST4_GROUP: multicast group4 setting

Register Name	GP3 Register (NA In PERV CPLT)
Mnemonic	EH.TPCHIP.NET.PCBSLPCI.GP3_REG
Address	00000000090F0012 (PCB) 00000000090F0013 (PCB1) 00000000090F0014 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset
2	RWX	RWX_WAND	RWX_WOR	GLSMUX_RESET: Glsmux reset for test purpose and stuck active mesh protection. Notice no clocks in the EX if this bit is set.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Put the DPLL in test mode.
4	RWX	RWX_WAND	RWX_WOR	PLL_RST: Put PLL in reset state.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYP: Enable PLL bypass.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pcb_access)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	PM_PI_DECODE: Test override for power management. EX chiplet only.

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
22	RWX	RWX_WAND	RWX_WOR	RESCLK_DIS: Resonant clocking disable.
23:25	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave will report 'Chiplet Offline'.
27	RWX	RWX_WAND	RWX_WOR	TP_LVLTRANS_FENCE: Electrical winkel fence. Mainly used by power management.
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.
29:31	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)

Register Name	Hang Pulse Generation Register 6
Mnemonic	EH.TPCHIP.NET.PCBSLPCI.HANG_PULSE_6_REG
Address	00000000090F0026 (PCB)
Attributes	
Description	This hang counter is exclusively used for the heartbeat generation

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_6: Value of hang pulse 6. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 > \text{value} > 0$
6	RW	SUPPRESS_HANG_6: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	Divider For Hang Counter Clock
Mnemonic	EH.TPCHIP.NET.PCBSLPCI.PRE_COUNTER_REG
Address	00000000090F0028 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PRE_COUNTER: Divider for hang counter clock. Divides clock by n+1 (default: n=0)

Register Name	GP Register 0
Mnemonic	EXP.TP.ECO_DOM.GP0
Address	0000000010000000 (PCB) 0000000010000004 (PCB1) 0000000010000005 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	NOT_USED0: Not used. Reset (0b0).
1	RWX	WOX_AND	WOX_OR	TC_SYNCCLK_MUXSEL_DC: syncclk mux for DPLL. Reset (0b1).
2	RWX	WOX_AND	WOX_OR	TC_GPIO_FLUSHMODE_INH_DC: Prevent plats from going into flush mode (initial value 1). Reset (0b1).



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
3	RWX	WOX_AND	WOX_OR	TC_GPIO_FORCEALIGN: Force align signal to be sent (initial value 1, drop before dropping flushmode_inh). Reset (0b1).
4	RWX	WOX_AND	WOX_OR	TC_GPIO_AVP_MODE_DC: Enable AVP mode. Reset (0b0).
5	RWX	WOX_AND	WOX_OR	TCEX_GCLK_ENABLE_CLK_DC_B_CORE_NCLK: ECO mode core clock disable. Reset (0b0).
6	RWX	WOX_AND	WOX_OR	TC_SCAN_DIS_DC_B: Disable scan - set output of scan chain to zero. Reset (0b0).
7	RWX	WOX_AND	WOX_OR	TC_SKIT_MODE_BIST_DC: Enable Skitter measuring during BIST. Reset (0b0).
8	RWX	WOX_AND	WOX_OR	TC_LBIST_EN_DC: LBIST mode. Reset (0b0).
9	RWX	WOX_AND	WOX_OR	TC_LBIST_AC_MODE_DC: LBIST ac mode. Reset (0b0).
10	RWX	WOX_AND	WOX_OR	TC_LBIST_ARY_WRT_THRU_DC: Array write-through mode - set array in bypass mode. Reset (0b0)
11	RWX	WOX_AND	WOX_OR	TC_ABIST_MODE_DC: perv and L3*. Reset (0b0)
12	RWX	WOX_AND	WOX_OR	TC_ABIST_START_TEST_DC: Set to start ABIST testing. Reset (0b0).
13	RWX	WOX_AND	WOX_OR	TC_ABIST_MODE2_DC: PC and L2. Reset (0b0).
14	RWX	WOX_AND	WOX_OR	TC_ATPG_EN_DC: ATPG mode. Reset (0b0).
15	RWX	WOX_AND	WOX_OR	TC_SCAN_PROTECT_DC: Scan protection enable (initial value 1). Reset (0b1).
16	RWX	WOX_AND	WOX_OR	NOT_USED1: Not used. Reset (0b1)
17	RWX	WOX_AND	WOX_OR	NOT_USED2: Not used. Reset (0b0).
18	RWX	WOX_AND	WOX_OR	NOT_USED3: Not used. Reset (0b0).
19	RWX	WOX_AND	WOX_OR	TC_L3_FENCE_EDRAM: L3 fence EDRAM, Reset (0b1).
20	RWX	WOX_AND	WOX_OR	TC_DBG_TRACE_START: Start trace to debug macros. Reset (0b0).
21	RWX	WOX_AND	WOX_OR	TC_DBG_TRACE_STOP: Stop trace to debug macros. Reset (0b0).
22	RWX	WOX_AND	WOX_OR	TC_DBG_TRACE_RESET: Reset trace to debug macros. Reset (0b0).
23	RWX	WOX_AND	WOX_OR	NOT_USED4: Not used. Reset (0b0).
24:25	RWX	WOX_AND	WOX_OR	TC_GPIO_CLKDIV_SEL_DC: Select clock divider ratio for probing. Reset (0b0).
26	RWX	WOX_AND	WOX_OR	NOT_USED5: Not used. Reset (0b0).
27	RWX	WOX_AND	WOX_OR	NOT_USED6: not used: 0b0. Reset (0b0).
28:31	RWX	WOX_AND	WOX_OR	TC_DBG_MUXSEL_DC: Nest debug bus selects(0:3). Reset (0b0).
32:39	RWX	WOX_AND	WOX_OR	TC_PSRO_SEL_DC: PSRO selects(0:7). Reset (0b0).
40:42	RWX	WOX_AND	WOX_OR	TC_NODE_ID_DC: Node ID. Reset (0b0).
43:45	RWX	WOX_AND	WOX_OR	TC_CHIP_ID_DC: Chip ID. Reset (0b0).
46	RWX	WOX_AND	WOX_OR	NOT_USED7: Not used. Reset (0b0).
47	RWX	WOX_AND	WOX_OR	NOT_USED8: Not used. Reset (0b0).
48	RWX	WOX_AND	WOX_OR	NOT_USED9: Not used. Reset (0b0).
49	RWX	WOX_AND	WOX_OR	NOT_USED10: Not used. Reset (0b0).
50	RWX	WOX_AND	WOX_OR	NOT_USED11: Not used. Reset (0b0).
51	RWX	WOX_AND	WOX_OR	NOT_USED12: Not used. Reset (0b0).
52	RWX	WOX_AND	WOX_OR	NOT_USED13: Not used. Reset (0b0).

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
53	RWX	WOX_AND	WOX_OR	NOT_USED14: Not used. Reset (0b0).
54	RWX	WOX_AND	WOX_OR	NOT_USED15: Not used. Reset (0b0).
55	RWX	WOX_AND	WOX_OR	NOT_USED16: Not used. Reset (0b0).
56	RWX	WOX_AND	WOX_OR	NOT_USED17: Not used. Reset (0b0).
57	RWX	WOX_AND	WOX_OR	NOT_USED18: Not used. Reset (0b0).
58	RWX	WOX_AND	WOX_OR	NOT_USED19: Not used. Reset (0b0).
59	RWX	WOX_AND	WOX_OR	NOT_USED20: Not used. Reset (0b0).
60	RWX	WOX_AND	WOX_OR	TC_MASK_CC_PCB_ERR_DC: Mask for pcb error (access or parity) in CC. Reset (0b0).
61	RWX	WOX_AND	WOX_OR	TC_MASK_CC_SCAN_OPCG_ERR_DC: Mask for pcb write while OPCG_IP / scan collision in CC. Reset (0b0).
62	RWX	WOX_AND	WOX_OR	TC_CC_LCC_EDGE_DELAYED_DC: Offset the clocking in the f domain by one cycle. Reset (0b1).
63	RWX	WOX_AND	WOX_OR	TC_FENCE_PERV_DC: Fence pervasive logic during scan (initial value 1). Reset (0b1).

Register Name	GP3 Register (NA In PERV CPLT)
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.GP3_REG
Address	00000000110F0012 (PCB) 00000000110F0013 (PCB1) 00000000110F0014 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset
2	RWX	RWX_WAND	RWX_WOR	GLSMUX_RESET: Glsmux reset for test purpose and stuck active mesh protection. Notice no clocks in the EX if this bit is set.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Put the DPLL in test mode.
4	RWX	RWX_WAND	RWX_WOR	PLL_RST: Put PLL in reset state.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYP: Enable PLL bypass.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pcb_access)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	PM_PI_DECODE: Test override for power management. EX chiplet only.
22	RWX	RWX_WAND	RWX_WOR	RESCLK_DIS: Resonant clocking disable.
23:25	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave will report 'Chiplet Offline'.
27	RWX	RWX_WAND	RWX_WOR	TP_LVLTRANS_FENCE: Electrical winkel fence. Mainly used by power management.
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.
29:31	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)

Register Name	GP3 Register (NA In PERV CPLT)
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.GP3_REG
Address	00000000120F0012 (PCB) 00000000120F0013 (PCB1) 00000000120F0014 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset
2	RWX	RWX_WAND	RWX_WOR	GLSMUX_RESET: Glsmux reset for test purpose and stuck active mesh protection. Notice no clocks in the EX if this bit is set.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Put the DPLL in test mode.
4	RWX	RWX_WAND	RWX_WOR	PLL_RST: Put PLL in reset state.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYP: Enable PLL bypass.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pcb_access)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	PM_PI_DECODE: Test override for power management. EX chiplet only.
22	RWX	RWX_WAND	RWX_WOR	RESCLK_DIS: Resonant clocking disable.
23:25	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)



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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave will report 'Chiplet Offline'.
27	RWX	RWX_WAND	RWX_WOR	TP_LVLTRANS_FENCE: Electrical winkel fence. Mainly used by power management.
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.
29:31	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)

Register Name	GP3 Register (NA In PERV CPLT)
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.GP3_REG
Address	00000000130F0012 (PCB) 00000000130F0013 (PCB1) 00000000130F0014 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset
2	RWX	RWX_WAND	RWX_WOR	GLSMUX_RESET: Glsmux reset for test purpose and stuck active mesh protection. Notice no clocks in the EX if this bit is set.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Put the DPLL in test mode.
4	RWX	RWX_WAND	RWX_WOR	PLL_RST: Put PLL in reset state.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYP: Enable PLL bypass.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pcb_access)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	PM_PI_DECODE: Test override for power management. EX chiplet only.
22	RWX	RWX_WAND	RWX_WOR	RESCLK_DIS: Resonant clocking disable.
23:25	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave will report 'Chiplet Offline'.
27	RWX	RWX_WAND	RWX_WOR	TP_LVLTRANS_FENCE: Electrical winkel fence. Mainly used by power management.
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
29:31	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)

Register Name	GP3 Register (NA In PERV CPLT)
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.GP3_REG
Address	00000000140F0012 (PCB) 00000000140F0013 (PCB1) 00000000140F0014 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset
2	RWX	RWX_WAND	RWX_WOR	GLSMUX_RESET: Glsmux reset for test purpose and stuck active mesh protection. Notice no clocks in the EX if this bit is set.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Put the DPLL in test mode.
4	RWX	RWX_WAND	RWX_WOR	PLL_RST: Put PLL in reset state.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYP: Enable PLL bypass.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pcb_access)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	PM_PI_DECODE: Test override for power management. EX chiplet only.
22	RWX	RWX_WAND	RWX_WOR	RESCLK_DIS: Resonant clocking disable.
23:25	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave will report 'Chiplet Offline'.
27	RWX	RWX_WAND	RWX_WOR	TP_LVLTRANS_FENCE: Electrical winkel fence. Mainly used by power management.
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.
29:31	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)

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Register Name	GP3 Register (NA In PERV CPLT)
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.GP3_REG
Address	00000000150F0012 (PCB) 00000000150F0013 (PCB1) 00000000150F0014 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset
2	RWX	RWX_WAND	RWX_WOR	GLSMUX_RESET: Glsmux reset for test purpose and stuck active mesh protection. Notice no clocks in the EX if this bit is set.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Put the DPLL in test mode.
4	RWX	RWX_WAND	RWX_WOR	PLL_RST: Put PLL in reset state.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYP: Enable PLL bypass.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pcb_access)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	PM_PI_DECODE: Test override for power management. EX chiplet only.
22	RWX	RWX_WAND	RWX_WOR	RESCLK_DIS: Resonant clocking disable.
23:25	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave will report 'Chiplet Offline'.
27	RWX	RWX_WAND	RWX_WOR	TP_LVLTRANS_FENCE: Electrical winkel fence. Mainly used by power management.
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.
29:31	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)

Register Name	GP3 Register (NA In PERV CPLT)
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.GP3_REG
Address	00000000160F0012 (PCB) 00000000160F0013 (PCB1) 00000000160F0014 (PCB2)
Attributes	
Description	



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset
2	RWX	RWX_WAND	RWX_WOR	GLSMUX_RESET: Glsmux reset for test purpose and stuck active mesh protection. Notice no clocks in the EX if this bit is set.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Put the DPLL in test mode.
4	RWX	RWX_WAND	RWX_WOR	PLL_RST: Put PLL in reset state.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYP: Enable PLL bypass.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pcb_access)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	PM_PI_DECODE: Test override for power management. EX chiplet only.
22	RWX	RWX_WAND	RWX_WOR	RESCLK_DIS: Resonant clocking disable.
23:25	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave will report 'Chiplet Offline'.
27	RWX	RWX_WAND	RWX_WOR	TP_LVLTRANS_FENCE: Electrical winkel fence. Mainly used by power management.
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.
29:31	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)

Register Name	GP3 Register (NA In PERV CPLT)
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.GP3_REG
Address	00000000190F0012 (PCB) 00000000190F0013 (PCB1) 00000000190F0014 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset
2	RWX	RWX_WAND	RWX_WOR	GLSMUX_RESET: Glsmux reset for test purpose and stuck active mesh protection. Notice no clocks in the EX if this bit is set.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Put the DPLL in test mode.

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
4	RWX	RWX_WAND	RWX_WOR	PLL_RST: Put PLL in reset state.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYP: Enable PLL bypass.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pcb_access)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	PM_PI_DECODE: Test override for power management. EX chiplet only.
22	RWX	RWX_WAND	RWX_WOR	RESCLK_DIS: Resonant clocking disable.
23:25	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave will report 'Chiplet Offline'.
27	RWX	RWX_WAND	RWX_WOR	TP_LVLTRANS_FENCE: Electrical winkel fence. Mainly used by power management.
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.
29:31	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)

Register Name	GP3 Register (NA In PERV CPLT)
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.GP3_REG
Address	000000001A0F0012 (PCB) 000000001A0F0013 (PCB1) 000000001A0F0014 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset
2	RWX	RWX_WAND	RWX_WOR	GLSMUX_RESET: Glsmux reset for test purpose and stuck active mesh protection. Notice no clocks in the EX if this bit is set.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Put the DPLL in test mode.
4	RWX	RWX_WAND	RWX_WOR	PLL_RST: Put PLL in reset state.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYP: Enable PLL bypass.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pcb_access)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	PM_PI_DECODE: Test override for power management. EX chiplet only.
22	RWX	RWX_WAND	RWX_WOR	RESCLK_DIS: Resonant clocking disable.
23:25	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave will report 'Chiplet Offline'.
27	RWX	RWX_WAND	RWX_WOR	TP_LVLTRANS_FENCE: Electrical winkel fence. Mainly used by power management.
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.
29:31	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)

Register Name	GP3 Register (NA In PERV CPLT)
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.GP3_REG
Address	000000001B0F0012 (PCB) 000000001B0F0013 (PCB1) 000000001B0F0014 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset
2	RWX	RWX_WAND	RWX_WOR	GLSMUX_RESET: Glsmux reset for test purpose and stuck active mesh protection. Notice no clocks in the EX if this bit is set.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Put the DPLL in test mode.
4	RWX	RWX_WAND	RWX_WOR	PLL_RST: Put PLL in reset state.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYP: Enable PLL bypass.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pcb_access)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	PM_PI_DECODE: Test override for power management. EX chiplet only.
22	RWX	RWX_WAND	RWX_WOR	RESCLK_DIS: Resonant clocking disable.
23:25	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave will report 'Chiplet Offline'.
27	RWX	RWX_WAND	RWX_WOR	TP_LVLTRANS_FENCE: Electrical winkel fence. Mainly used by power management.
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.
29:31	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)

Register Name	GP3 Register (NA In PERV CPLT)
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.GP3_REG
Address	000000001C0F0012 (PCB) 000000001C0F0013 (PCB1) 000000001C0F0014 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset
2	RWX	RWX_WAND	RWX_WOR	GLSMUX_RESET: Glsmux reset for test purpose and stuck active mesh protection. Notice no clocks in the EX if this bit is set.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Put the DPLL in test mode.
4	RWX	RWX_WAND	RWX_WOR	PLL_RST: Put PLL in reset state.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYP: Enable PLL bypass.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pcb_access)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	PM_PI_DECODE: Test override for power management. EX chiplet only.
22	RWX	RWX_WAND	RWX_WOR	RESCLK_DIS: Resonant clocking disable.
23:25	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave will report 'Chiplet Offline'.
27	RWX	RWX_WAND	RWX_WOR	TP_LVLTRANS_FENCE: Electrical winkel fence. Mainly used by power management.
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.
29:31	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)

Register Name	GP3 Register (NA In PERV CPLT)
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.GP3_REG
Address	000000001D0F0012 (PCB) 000000001D0F0013 (PCB1) 000000001D0F0014 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset
2	RWX	RWX_WAND	RWX_WOR	GLSMUX_RESET: Glsmux reset for test purpose and stuck active mesh protection. Notice no clocks in the EX if this bit is set.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Put the DPLL in test mode.
4	RWX	RWX_WAND	RWX_WOR	PLL_RST: Put PLL in reset state.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYP: Enable PLL bypass.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pcb_access)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	PM_PI_DECODE: Test override for power management. EX chiplet only.
22	RWX	RWX_WAND	RWX_WOR	RESCLK_DIS: Resonant clocking disable.
23:25	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave will report 'Chiplet Offline'.
27	RWX	RWX_WAND	RWX_WOR	TP_LVLTRANS_FENCE: Electrical winkel fence. Mainly used by power management.
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.
29:31	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)

Register Name	GP3 Register (NA In PERV CPLT)
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.GP3_REG
Address	000000001E0F0012 (PCB) 000000001E0F0013 (PCB1) 000000001E0F0014 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset
2	RWX	RWX_WAND	RWX_WOR	GLSMUX_RESET: Glsmux reset for test purpose and stuck active mesh protection. Notice no clocks in the EX if this bit is set.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Put the DPLL in test mode.
4	RWX	RWX_WAND	RWX_WOR	PLL_RST: Put PLL in reset state.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYP: Enable PLL bypass.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pcb_access)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	PM_PI_DECODE: Test override for power management. EX chiplet only.
22	RWX	RWX_WAND	RWX_WOR	RESCLK_DIS: Resonant clocking disable.
23:25	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave will report 'Chiplet Offline'.
27	RWX	RWX_WAND	RWX_WOR	TP_LVLTRANS_FENCE: Electrical winkel fence. Mainly used by power management.
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
29:31	RWX	RWX_WAND	RWX_WOR	Reserved field. (Access type is pm_access)

Register Name	<i>Scratch Register 0</i>		
Mnemonic	EXP.EC.PC.SCR0		
Address	0000000000000008 (SPRD) 0000000010013283 (SCOM)		
Attributes			
Description			

Bits	SPRD	SCOM	Field Mnemonic: Description
0:63	RW	RW	

Register Name	<i>Scratch Register 1</i>		
Mnemonic	EXP.EC.PC.SCR1		
Address	0000000000000009 (SPRD) 0000000010013284 (SCOM)		
Attributes			
Description			

Bits	SPRD	SCOM	Field Mnemonic: Description
0:63	RW	RW	

4. POWER8 PSIHB Chiplet

The POWER8 processor registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
EN.TPC.PSIHB.DMA_UP_ADDR	0x0000000002010914	683
EN.TPC.PSIHB.NOTRUST_BAR0	0x0000000002013F40	688
EN.TPC.PSIHB.NOTRUST_BAR0MASK	0x0000000002013F42	688
EN.TPC.PSIHB.NOTRUST_BAR1	0x0000000002013F41	688
EN.TPC.PSIHB.NOTRUST_BAR1MASK	0x0000000002013F43	689
EN.TPC.PSIHB.PSIHB_DEBUG_REG	0x0000000002010911	682
EN.TPC.PSIHB.PSIHB_ERROR_MASK_REG	0x000000000201090F	681
EN.TPC.PSIHB.PSIHB_FIR_ACTION0_REG	0x0000000002010906	676
EN.TPC.PSIHB.PSIHB_FIR_ACTION1_REG	0x0000000002010907	677
EN.TPC.PSIHB.PSIHB_FIR_MASK_REG	0x0000000002010903	675
EN.TPC.PSIHB.PSIHB_FIR_REG	0x0000000002010900	673
EN.TPC.PSIHB.PSIHB_INTERRUPT1_REG	0x0000000002010916	685
EN.TPC.PSIHB.PSIHB_INTERRUPT2_REG	0x0000000002010917	685
EN.TPC.PSIHB.PSIHB_INTERRUPT3_REG	0x0000000002010918	686
EN.TPC.PSIHB.PSIHB_INTERRUPT4_REG	0x0000000002010919	686
EN.TPC.PSIHB.PSIHB_INTERRUPT5_REG	0x000000000201091A	686
EN.TPC.PSIHB.PSIHB_INTERRUPT_REG	0x0000000002010910	684
EN.TPC.PSIHB.PSIHB_INTERRUPT_STATUS	0x0000000002010915	683
EN.TPC.PSIHB.PSIHB_ISRN_REG	0x000000000201091B	687
EN.TPC.PSIHB.PSIHB_STATUS_CTL_REG	0x000000000201090E	679
EN.TPC.PSIHB.PSI_BRIDGE_BAR_REG	0x000000000201090A	678
EN.TPC.PSIHB.PSI_BRIDGE_FSP_BAR_REG	0x000000000201090B	678
EN.TPC.PSIHB.PSI_FSP_MMR_REG	0x000000000201090C	679
EN.TPC.PSIHB.PSI_TCE_ADDR_REG	0x0000000002013F44	689
EN.TPC.PSIHB.TRUST_CONTROL	0x0000000002013F45	690

The POWER8 processor registers are listed in the following tables.

Register Name	<i>PSI Host Bridge FIR Register</i>
Mnemonic	EN.TPC.PSIHB.PSIHB_FIR_REG
Address	0000000002010900 (SCOM) 0000000002010901 (SCOM1) 0000000002010902 (SCOM2)
Attributes	
Description	PSI Host Bridge FIR Register

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PB_ECC_ERR_CE: CE from processor bus data
1	RWX	WOX_AND	WOX_OR	PB_ECC_ERR_UE: UE from processor bus data
2	RWX	WOX_AND	WOX_OR	PB_ECC_ERR_SUE: SUE from processor bus data
3	RWX	WOX_AND	WOX_OR	INTERRUPT_FROM_ERROR: Interrupt Condition present in PSIHB
4	RWX	WOX_AND	WOX_OR	INTERRUPT_FROM_FSP: Interrupt from FSP is being processed
5	RWX	WOX_AND	WOX_OR	FSP_ECC_ERR_CE: CE from PSILL data
6	RWX	WOX_AND	WOX_OR	FSP_ECC_ERR_UE: UE from PSILL data
7	RWX	WOX_AND	WOX_OR	ERROR_STATE: Error bit set, ignores the interrupt mask
8	RWX	WOX_AND	WOX_OR	INVALID_TTYPE: Invalid TType Hit on PHB or FSP bar
9	RWX	WOX_AND	WOX_OR	INVALID_CRESP: Invalid CResp returned to command issued by PSIHB
10	RWX	WOX_AND	WOX_OR	PB_DATA_TIME_OUT: processor bus time out waiting for data grant
11	RWX	WOX_AND	WOX_OR	PB_PARITY_ERROR: PB parity error
12	RWX	WOX_AND	WOX_OR	FSP_ACCESS_TRUSTED_SPACE: FSP tried access to trusted space
13	RWX	WOX_AND	WOX_OR	UNEXPECTED_PB: Unexpected PB CRESP or DATA
14	RWX	WOX_AND	WOX_OR	INTERRUPT_REG_CHANGE_WHILE_ACTIVE: Interrupt register change while interrupt still pending
15	RWX	WOX_AND	WOX_OR	INTERRUPT0_ADDRESS_ERROR: PSI Interrupt address Error
16	RWX	WOX_AND	WOX_OR	INTERRUPT1_ADDRESS_ERROR: OCC Interrupt address Error
17	RWX	WOX_AND	WOX_OR	INTERRUPT2_ADDRESS_ERROR: FSI Interrupt address Error
18	RWX	WOX_AND	WOX_OR	INTERRUPT3_ADDRESS_ERROR: LPC Interrupt address Error
19	RWX	WOX_AND	WOX_OR	INTERRUPT4_ADDRESS_ERROR: LOCAL ERROR Interrupt address Error
20	RWX	WOX_AND	WOX_OR	INTERRUPT5_ADDRESS_ERROR: HOST ERROR Interrupt address Error
21	RWX	WOX_AND	WOX_OR	TCBR_TP_PSI_GLB_ERR_0: PSI global error bit 0
22	RWX	WOX_AND	WOX_OR	TCBR_TP_PSI_GLB_ERR_1: PSI global error bit 1
23	RWX	WOX_AND	WOX_OR	UPSTREAM_FIR: Upstream error
24:26	RWX	WOX_AND	WOX_OR	SPARE_FIR: Spare fir
27	RWX	WOX_AND	WOX_OR	SCOM_ERROR: scom error
28	RWX	WOX_AND	WOX_OR	FIR_PARITY_ERROR: fir parity Error
29:63	RO	RO	RO	Reserved



Register Name	PSI Host Bridge FIR Mask Register
Mnemonic	EN.TPC.PSIHB.PSIHB_FIR_MASK_REG
Address	0000000002010903 (SCOM) 0000000002010904 (SCOM1) 0000000002010905 (SCOM2)
Attributes	
Description	PSI Host Bridge FIR Mask Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	PB_ECC_ERR_CE_MASK: Mask for CE from processor bus data
1	RW	WO_AND	WO_OR	PB_ECC_ERR_UE_MASK: Mask for UE from processor bus data
2	RW	WO_AND	WO_OR	PB_ECC_ERR_SUE_MASK: Mask for SUE from processor bus data
3	RW	WO_AND	WO_OR	INTERRUPT_FROM_ERROR_MASK: Mask for Interrupt Condition present in PSIHB
4	RW	WO_AND	WO_OR	INTERRUPT_FROM_FSP_MASK: Mask for Interrupt from FSP is being processed
5	RW	WO_AND	WO_OR	FSP_ECC_ERR_CE_MASK: Mask for CE from PSILL data
6	RW	WO_AND	WO_OR	FSP_ECC_ERR_UE_MASK: Mask for UE from PSILL data
7	RW	WO_AND	WO_OR	ERROR_STATE_MASK: Mask for Error bit set, ignores the interrupt mask
8	RW	WO_AND	WO_OR	INVALID_TTYPE_MASK: Mask for Invalid TType Hit on PHB or FSP bar
9	RW	WO_AND	WO_OR	INVALID_CRESP_MASK: Mask for Invalid CResp returned to command issued by PSIHB
10	RW	WO_AND	WO_OR	PB_DATA_TIME_OUT_MASK: Mask for processor bus time out waiting for data grant
11	RW	WO_AND	WO_OR	PB_PARITY_ERROR_MASK: PB parity error
12	RW	WO_AND	WO_OR	FSP_ACCESS_TRUSTED_SPACE_MASK: FSP tried access to trusted space
13	RW	WO_AND	WO_OR	UNEXPECTED_PB_MASK: Unexpected PB CRESP or DATA
14	RW	WO_AND	WO_OR	INTERRUPT_REG_CHANGE_WHILE_ACTIVE_MASK: Interrupt register change while interrupt still pending
15	RW	WO_AND	WO_OR	INTERRUPT0_ADDRESS_ERROR_MASK: PSI Interrupt address error_mask
16	RW	WO_AND	WO_OR	INTERRUPT1_ADDRESS_ERROR_MASK: OCC Interrupt address error_mask
17	RW	WO_AND	WO_OR	INTERRUPT2_ADDRESS_ERROR_MASK: FSI Interrupt address error_mask
18	RW	WO_AND	WO_OR	INTERRUPT3_ADDRESS_ERROR_MASK: LPC Interrupt address error_mask
19	RW	WO_AND	WO_OR	INTERRUPT4_ADDRESS_ERROR_MASK: LOCAL error_mask Interrupt address error_mask
20	RW	WO_AND	WO_OR	INTERRUPT5_ADDRESS_ERROR_MASK: HOST error_mask Interrupt address error_mask
21	RW	WO_AND	WO_OR	TCBR_TP_PSI_GLB_ERR_0_MASK: PSI global_mask error bit 0
22	RW	WO_AND	WO_OR	TCBR_TP_PSI_GLB_ERR_1_MASK: PSI global_mask error bit 1
23	RW	WO_AND	WO_OR	UPSTREAM_FIR_MASK: Upstream error



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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
24:26	RW	WO_AND	WO_OR	SPARE_FIR_MASK: Spare fir
27	RW	WO_AND	WO_OR	SCOM_ERROR_MASK: scom Error
28	RW	WO_AND	WO_OR	FIR_PARITY_ERROR_MASK: fir parity Error
29:63	RO	RO	RO	Reserved

Register Name	<i>PSI Host Bridge FIR Action0 Register</i>
Mnemonic	EN.TPC.PSIHB.PSIHB_FIR_ACTION0_REG
Address	0000000002010906 (SCOM)
Attributes	
Description	PSI Host Bridge FIR Action0 Register Action select for corresponding bit in FIR (Action0,Action1) = Action Select (0,0) = No Error (0,1) = recoverable error (1,0) = Checkstop Error (1,1) = unused

Bits	SCOM	Field Mnemonic: Description
0	RO	PB_ECC_ERR_CE_ACTION0: Action0 for CE from processor bus data
1	RO	PB_ECC_ERR_UE_ACTION0: Action0 for UE from processor bus data
2	RO	PB_ECC_ERR_SUE_ACTION0: Action0 for SUE from processor bus data
3	RO	INTERRUPT_FROM_ERROR_ACTION0: Action0 for Interrupt Condition present in PSIHB
4	RO	INTERRUPT_FROM_FSP_ACTION0: Action0 for Interrupt from FSP is being processed
5	RO	FSP_ECC_ERR_CE_ACTION0: Action0 for CE from PSILL data
6	RO	FSP_ECC_ERR_UE_ACTION0: Action0 for UE from PSILL data
7	RO	ERROR_STATE_ACTION0: Action0 for Error bit set, ignores the interrupt mask
8	RO	INVALID_TTYPE_ACTION0: Action0 for Invalid TType Hit on PHB or FSP bar
9	RO	INVALID_CRESP_ACTION0: Action0 for Invalid CResp returned to command issued by PSIHB
10	RO	PB_DATA_TIME_OUT_ACTION0: Action0 for processor bus time out waiting for data grant
11	RO	PB_PARITY_ERROR_ACTION0: PB parity error
12	RO	FSP_ACCESS_TRUSTED_SPACE_ACTION0: FSP tried access to trusted space
13	RO	UNEXPECTED_PB_ACTION0: Unexpected PB CRESP or DATA
14	RO	INTERRUPT_REG_CHANGE_WHILE_ACTIVE_ACTION0: Interrupt register change while interrupt still pending
15	RO	INTERRUPT0_ADDRESS_ERROR_ACTION0: PSI Interrupt address error_action0
16	RO	INTERRUPT1_ADDRESS_ERROR_ACTION0: OCC Interrupt address error_action0
17	RO	INTERRUPT2_ADDRESS_ERROR_ACTION0: FSI Interrupt address error_action0
18	RO	INTERRUPT3_ADDRESS_ERROR_ACTION0: LPC Interrupt address error_action0
19	RO	INTERRUPT4_ADDRESS_ERROR_ACTION0: LOCAL error_action0 Interrupt address error_action0
20	RO	INTERRUPT5_ADDRESS_ERROR_ACTION0: HOST error_action0 Interrupt address error_action0
21	RO	TCBR_TP_PSI_GLB_ERR_0_ACTION0: PSI global_action0 error bit 0
22	RO	TCBR_TP_PSI_GLB_ERR_1_ACTION0: PSI global_action0 error bit 1



Bits	SCOM	Field Mnemonic: Description
23	RO	UPSTREAM_FIR_ACTION0: Upstream error
24:26	RO	SPARE_FIR_ACTION0: Spare fir
27	RO	SCOM_ERROR_ACTION0: scom Error
28	RO	FIR_PARITY_ERROR_ACTION0: fir parity Error
29:63	RO	Reserved

Register Name	<i>PSI Host Bridge FIR Action1 Register</i>
Mnemonic	EN.TPC.PSIHB.PSIHB_FIR_ACTION1_REG
Address	0000000002010907 (SCOM)
Attributes	
Description	PSI Host Bridge FIR action1 Register Action select for corresponding bit in FIR (Action0,Action1) = Action Select (0,0) = No Error (0,1) = recoverable error (1,0) = Checkstop Error (1,1) = unused

Bits	SCOM	Field Mnemonic: Description
0	RO	PB_ECC_ERR_CE_ACTION1: Action1 for CE from processor bus data
1	RO	PB_ECC_ERR_UE_ACTION1: Action1 for UE from processor bus data
2	RO	PB_ECC_ERR_SUE_ACTION1: Action1 for SUE from processor bus data
3	RO	INTERRUPT_FROM_ERROR_ACTION1: Action1 for Interrupt Condition present in PSIHB
4	RO	INTERRUPT_FROM_FSP_ACTION1: Action1 for Interrupt from FSP is being processed
5	RO	FSP_ECC_ERR_CE_ACTION1: Action1 for CE from PSILL data
6	RO	FSP_ECC_ERR_UE_ACTION1: Action1 for UE from PSILL data
7	RO	ERROR_STATE_ACTION1: Action1 for Error bit set, ignores the interrupt mask
8	RO	INVALID_TTYPE_ACTION1: Action1 for Invalid TType Hit on PHB or FSP bar
9	RO	INVALID_CRESP_ACTION1: Action1 for Invalid CResp returned to command issued by PSIHB
10	RO	PB_DATA_TIME_OUT_ACTION1: Action1 for processor bus time out waiting for data grant
11	RO	PB_PARITY_ERROR_ACTION1: PB parity error
12	RO	FSP_ACCESS_TRUSTED_SPACE_ACTION1: FSP tried access to trusted space
13	RO	UNEXPECTED_PB_ACTION1: Unexpected PB CRESP or DATA
14	RO	INTERRUPT_REG_CHANGE_WHILE_ACTIVE_ACTION1: Interrupt register change while interrupt still pending
15	RO	INTERRUPT0_ADDRESS_ERROR_ACTION1: PSI Interrupt address error_action1
16	RO	INTERRUPT1_ADDRESS_ERROR_ACTION1: OCC Interrupt address error_action1
17	RO	INTERRUPT2_ADDRESS_ERROR_ACTION1: FSI Interrupt address error_action1
18	RO	INTERRUPT3_ADDRESS_ERROR_ACTION1: LPC Interrupt address error_action1
19	RO	INTERRUPT4_ADDRESS_ERROR_ACTION1: LOCAL error_action1 Interrupt address error_action1
20	RO	INTERRUPT5_ADDRESS_ERROR_ACTION1: HOST error_action1 Interrupt address error_action1
21	RO	TCBR_TP_PSI_GLB_ERR_0_ACTION1: PSI global_action1 error bit 0

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Bits	SCOM	Field Mnemonic: Description
22	RO	TCBR_TP_PSI_GLB_ERR_1_ACTION1: PSI global_action1 error bit 1
23	RO	UPSTREAM_FIR_ACTION1: Upstream error
24:26	RO	SPARE_FIR_ACTION1: Spare fir
27	RO	SCOM_ERROR_ACTION1: scom Error
28	RO	FIR_PARITY_ERROR_ACTION1: fir parity Error
29:63	RO	Reserved

Register Name	<i>PSIHBAR - Host Bridge Base Address Register</i>
Mnemonic	EN.TPC.PSIHB.PSI_BRIDGE_BAR_REG
Address	000000000201090A (SCOM)
Attributes	SCOM: 0x0A MMIO: 0x00
Description	The Bridge Base Address Register 0 identifies the address range which contains the MMIO accessible PSIHB registers. The least significant 20 bits of the 46 bit address is Reserved since the address is fixed at a 1MB boundary. Register can be written by SCOM only.

Bits	SCOM	Field Mnemonic: Description
0:13	RO	Reserved
14:43	RWX	BRIDGE BASE ADDRESS: The Bridge Base Address contains the address range which contains the MMIO accessible PSIHB unit registers.
44:62	RO	Reserved
63	RWX	VALID/ENABLED: This bit, when set to '1', enables MMIO access to the PSIHB register space and indicates that bits 14:43 contain a valid system memory address.

Register Name	<i>FSPBAR - FSP Base Address Register</i>
Mnemonic	EN.TPC.PSIHB.PSI_BRIDGE_FSP_BAR_REG
Address	000000000201090B (SCOM)
Attributes	SCOM: 0x0B MMIO: 0x08
Description	This register defines the 46 bit system address used to identify the start of FSP MMIO region within the system memory address space. The alignment of this region is dictated by its size as specified by the FSP memory mask register. The memory space is enabled by a bit in the PSIHC register.

Bits	SCOM	Field Mnemonic: Description
0:13	RO	Reserved
14:31	RWX	FSP MMIO SPACE BASE ADDRESS: Writing Bits 14:15 will update PSIHB_Up_ADDR bits 14:15
32:43	RWX	FSP MMIO SPACE BASE ADDRESS: Varies with FSP MMIO Region size as determined FSM Memory Mask Register. - Each bit of this field participates in the base address decode when the corresponding bit in the FSP Memory Mask Register is set to '1' - Each bit in this field does not participate in the base address decode when the corresponding bit in the FSP Memory Mask Register is set to '0'
44:63	RO	Reserved



Register Name	FSPMMR - FSP Memory Mask Register
Mnemonic	EN.TPC.PSIHB.PSI_FSP_MMR_REG
Address	000000000201090C (SCOM)
Attributes	SCOM: 0x0C MMIO: 0x10
Description	This register defines the size and alignment of the FSP MMIO region within the system memory address space.

Bits	SCOM	Field Mnemonic: Description
0:31	RO	Reserved
32:43	RWX	MASK BITS: Each bit, when set to '1', enables the corresponding bit in the FSPBAR to participate in the decode of the base address, thereby defining the size and alignment of the FSP MMIO region. Valid settings range from 4 GB (232) to 1 MB (220). Some example settings are: B'1111 1111 1111': FSP MMIO region is 220 (1 MB) in size and alignment B'1111 1111 0000': FSP MMIO region is 224 (16 MB) in size and alignment B'1111 1100 0000': FSP MMIO region is 226 (64 MB) in size and alignment B'0000 0000 0000': FSP MMIO region is 232 (4GB) in size and alignment
44:63	RO	Reserved

Register Name	PHBCSR - PSI Host Bridge Control/Status Register
Mnemonic	EN.TPC.PSIHB.PSIHB_STATUS_CTL_REG
Address	000000000201090E (SCOM)
Attributes	SCOM: 0x0E MMIO: 0x20
Description	This register contains controls and status for the PSI Host Bridge function. The register is divided into four two byte fields. • Bits 0:11 are control bits. • Bits 16:18 are summary condition indicators. • Bits 32:43 indicate errors detected within the PSIHB. Any active bit in this field causes the PSIHB to enter the error state. Only the first error detected causes a bit to be set in this field. Subsequent errors are not recorded until the field is cleared by software. • Bits 48:52 indicate errors with an operation received from the FSP. Any active bit in this field causes an error response packet to be sent to the FSP. Only the first error detected causes a bit to be set in this field. Subsequent errors are not recorded until the field is cleared. Sending the error response packet clears this field, or it can be cleared by software.

Bits	SCOM	Field Mnemonic: Description
0	RWX	FSP CMD ENABLE: When set to '0', all DMA and Interrupt commands issued by the FSP are ignored by the PSIHB. If an operation is received from the FSP when this bit is '0', a type 1 error condition is signaled to the FSP using the errack signal, and an Error Response packet (if enabled) is sent with an indication that FSP commands are not enabled in the CEC. When set to '1', all DMA and interrupt commands issued by the FSP are accepted and executed.
1	RWX	FSP MMIO ENABLE: When set to '0', the FSPBAR is ignored and no MMIO operations are issued to the FSP. When set to '1', MMIO operations to the FSP memory region defined by the FSPBAR are accepted and transmitted to the FSP.
2	RWX	Spare
3	RWX	FSP INTERRUPT ENABLE: When set to '0', bit 17 of the PSIHB does not cause an interrupt pending condition to CEC Firmware. When set to '1', bit 17 of the PSIHB causes an interrupt pending condition to CEC Firmware.

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Bits	SCOM	Field Mnemonic: Description
4	RWX	ERROR RESPONSE ENABLE: When set to '0', bits 48 to 52 of the PSIHBC do not cause an error response packet to be sent to the FSP. When set to '1', bits 48 to 52 of the PSIHBC cause an error response packet to be sent to the FSP.
5	RWX	PSI LINK ENABLE: When '0', causes the PSI TX to drive 0's on the link. When '1', causes PSI TX to drive the idle pattern on the link
6	RWX	FSP RESET: When this bit transitions from '0' to '1', an encoded reset sequence is sent to the FSP.
7	WOX_6P	PSIHB RESET: Write only bit. When written to '1', all state machines and internal control latches that are otherwise inaccessible to software are reset. Note that latches accessible by software, such as error indicators and error masks, are not reset by this bit.
8:11	RWX	MMIO ADDRESS MASK: These bit controls the use of system address bits 32:35 when transmitting an address to the FSP. When a bit in this mask is set to '1', the corresponding address bit is passed as is from the CEC to the PSI/FSP, otherwise the corresponding address bit is sent to the PSI/FSP as '0'. Note that upper order bits 16:31 are always masked off and are never passed to the FSP.
12:15	RO	Reserved
16	ROX	CEC PSI INTERRUPT: Set to '1' by hardware when an interruption condition is present in the PSIHB.
17	RWX	FSP INTERRUPT: Set to '1' when an Interrupt set command is received from the incoming PSI interface Set to '0' when an Interrupt reset command is received from the incoming PSI interface
18	ROX	FSP LINK ACTIVE: Set to '1' by hardware when the PSI link is active and working
19	ROX	OUTBOUND QUEUE BUSY: Set to '1' by hardware when an outbound command or data queue is active or pending transfer.
20	ROX	INBOUND QUEUE BUSY: Set to '1' by hardware when an inbound command or data queue is active or pending transfer.
21	ROX	LOAD REPLY OUTSTANDING: Set to '1' by hardware when the PSIHB receives an MMIO load command, reset to '0' by hardware when the reply data is delivered to the CEC.
22	ROX	DMA READ REPLY OUTSTANDING: Set to '1' by hardware when the PSIHB receives a DMAR command from the FSP, reset to '0' by hardware when the reply data is delivered to the FSP.
23	ROX	INTERRUPT COMMAND EXPECTED: Set to '1' by hardware when the PSIHB goes interrupt pending (requests an interrupt command be sent on the fabric), reset to '0' by hardware when an EOI is received and no subsequent interrupts are pending.
24:31	RO	Reserved
32	ROX	PSI REPORTED ERROR: Set to '1' when the PSI macro detects a fatal error.
33	RWX	LINK INACTIVE TRANSITION: Set to '1' when the PSI link transitions from '1' to '0'.
34	RWX	FSP ACK TIME-OUT: Set when a command to the FSP interface has not been acknowledged (ready not re-activated) within 2 ticks of the system hang pulse.
35	RWX	MMIO LOAD TIME-OUT: Set when a reply packet is not received within 2 ticks after an MMIO load is sent to the FSP
36	RWX	MMIO LENGTH ERROR: Set when an MMIO is targets the region defined by the GXBAR and has a length of anything other than 8 bytes.
37	RWX	MMIO ADDRESS ERROR: Set when an MMIO operation targets the region defined by the GXBAR but does not target one of the defined registers.
38	RWX	MMIO TTYPE ERROR: Set when an operation targets the region defined by the GXBAR or FSP bar, but is not a valid operation type. Operations issued to this space must be non-cacheable stores or loads only.
39	RWX	UNCORRECTABLE ERROR (UE) DETECTED: Set when a double bit error is detected on the interface between the incoming PSI macro and the PSIHB PSI attach function.
40	RWX	INTERNAL PARITY ERROR: Set when a parity error is detected in the controls or data flow of the PSIHB PSI attach function.



Bits	SCOM	Field Mnemonic: Description
41	RWX	FSP SYNCHRONOUS ERROR ALERT 1: Set when an error detected by the FSP is reported synchronously via the errack signal, and the FSP is able to continue accepting commands.
42	RWX	FSP SYNCHRONOUS ERROR ALERT 2: Set when an error detected by the FSP is reported synchronously via the errack signal, and the FSP is unable to continue accepting commands.
43	RWX	FSP COMMAND ERROR DETECTED: Set when PSIHBC detects an error with an incoming command as indicated by PSIHBC bits 48 to 52. This bit is masked off for normal operation. That is, errors with incoming operations are normally reported to the FSP, do not cause entry into error state, and are ignored by CEC firmware. This bit allows for optional reporting and handling of these types of errors by the CEC.
44:47	RO	Reserved
48	RWX	ADDRESS ERROR: Set when a DMA operation targets a system memory address that does not exist.
48	RWX	TCE EXTENT ERROR: Set when a DMA operation would result in a TCE fetch beyond the end of the TCE table in system memory.
50	RWX	PAGE FAULT: Set when a DMA access uses a TCE entry that is inconsistent with the access control bits of the TCE.
51	RWX	INVALID OP CODE: Set when an incoming command does not contain a valid opcode.
52	RWX	INVALID READ: Set when a read is received before read response data has been returned for a prior read.
53:63	RO	Reserved

Register Name	PSISEMR - PSIHBC Status / Error Mask Register
Mnemonic	EN.TPC.PSIHB.PSIHB_ERROR_MASK_REG
Address	000000000201090F (SCOM)
Attributes	SCOM: 0x0F MMIO: 0x28
Description	This register contains mask bits which can prevent the corresponding status bits from being set and also controls whether or not an interrupt condition is set

Bits	SCOM	Field Mnemonic: Description
0:15	RO	Reserved
16:27	RWX	ERROR DISABLE 1: Prevent Status and Error State by bits 32:43 of PSIHBCR Any bit when set to '1' prevents hardware from setting the corresponding bit in PSIHBC bits 32:43. Entry into the error state is also prevented.
28:31	RO	Reserved
32:43	RWX	INTERRUPT DISABLE: Prevent Interrupt Condition by bits 32:43 of PSIHBCR Any bit when set to '1' prevents hardware from signaling an interrupt to the CEC FW when the corresponding bit in PSIHBC bits 32:43 is set.
44:47	RO	Reserved
48:52	RWX	ERROR DISABLE 2: Prevent Status and Error packet launch by bits 48:52 of PSIHBCR Any bit when set to '1' prevents hardware from setting the corresponding bit in PSIHBC bits 48:52.
53:63	RO	Reserved

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Register Name	PHBDSR - PSIH B Debug Setting Register
Mnemonic	EN.TPC.PSIHB.PSIHB_DEBUG_REG
Address	0000000002010911 (SCOM)
Attributes	SCOM: 0x11 MMIO: 0x38
Description	This register contains the controls for injecting correctable and uncorrectable on to the processor bus and the Link Layer interfaces and for selecting what signals are traced by the trace bus. Bit mappings on SCOM and MMIO are different

Bits	SCOM	Field Mnemonic: Description
0:1	RWX	Link Layer Insert Error: "00" - No Error Injected "01" or "10" - CE inserted "11" - UE inserted
2	RWX	LINK LAYER ONE ERROR: When set to '1' from '0', a single error from bits 0:1 is injected unless bit 3 is set, then it is ignored
3	RWX	LINK LAYER CONTINUOUS ERROR: When set to '1', the error from bits 0:1 will be continuously injected until cleared
4:7	RO	Reserved
8:9	RWX	Processor bus Insert Error: "00" - No Error Injected "01" or "10" - CE inserted "11" - UE inserted
10	RWX	POWERBUS ONE ERROR: When set to '1' from '0', a single error from bits 8:9 is injected unless bit 11 is set, then it is ignored
11	RWX	POWERBUS CONTINUOUS ERROR: When set to '1', the error from bits 8:9 will be continuously injected until cleared
12:15	RO	Reserved
16:19	RWX	TRACE BUS CONTROLS: "00xx" - PSI LL interface is traced. Any other setting will trace different internal state machines
20:63	RO	Reserved

Register Name	PHBCSR - PSI Host Bridge Set Control/Status Register
Mnemonic	EN.TPC.PSIHB.PSIHB_STATUS_CTL_REG
Address	0000000002010912 (SCOM1)
Attributes	SCOM: 0x12 MMIO: 0x40
Description	This register is used as a bitwise set of the PHBCSR register. When this register is updated, any '1's will cause the correlating bits in the PHBCSR to set to a '1'. This is a write only register.

Bits	SCOM1	Field Mnemonic: Description
0:11	WOX_OR	PBHC SR CONTROL BITS
12:16	RO	Reserved
17	WOX_OR	PBHC SR FSP INTERRUPT
18:32	RO	Reserved
33:43	WOX_OR	ERROR STATUS 1
44:47	RO	Reserved



Bits	SCOM1	Field Mnemonic: Description
48:52	WOX_OR	ERROR STATUS 2
53:63	RO	Reserved

Register Name	<i>PHBCCR - PSI Host Bridge Clear Control/ Status Register</i>
Mnemonic	EN.TPC.PSIHB.PSIHB_STATUS_CTL_REG
Address	0000000002010913 (SCOM2)
Attributes	SCOM: 0x13 MMIO: 0x48
Description	This register is used as a bitwise clear of the PHBCSR register. When this register is updated, any '1's will cause the correlating bits in the PHBCSR to set to a '0'. This is a write only register.

Bits	SCOM2	Field Mnemonic: Description
0:11	WOX_CLEAR	PBHCSR CONTROL BITS
12:16	RO	Reserved
17	WOX_CLEAR	PBHCSR FSP INTERRUPT
18:32	RO	Reserved
33:43	WOX_CLEAR	ERROR STATUS 1
44:47	RO	Reserved
48:52	WOX_CLEAR	ERROR STATUS 2
53:63	WOX_CLEAR	Reserved

Register Name	<i>PHBDSR - DMA Upper Address Register</i>
Mnemonic	EN.TPC.PSIHB.DMA_UP_ADDR
Address	0000000002010914 (SCOM)
Attributes	SCOM: 0x14 MMIO: 0x50
Description	The DMA Upper Address Register identifies the upper two address bits in order to extend FSI address and define the escape address so that it can update the upper two bits.

Bits	SCOM	Field Mnemonic: Description
0:5	RW	Reserved
6:7	RWX	DMA BASE UPPER ADDRESS BITS: DMA Upper Address (14:15)
8:15	RO	Reserved
16:63	RW	DMA ESCAPE ADDRESS: Escape address for FSI update of bit 6:7. Default is FFFFFFFF00

Register Name	<i>Interrupt Status</i>
Mnemonic	EN.TPC.PSIHB.PSIHB_INTERRUPT_STATUS
Address	0000000002010915 (SCOM)
Attributes	SCOM: 0x15 MMIO: 0x58
Description	This register is read only and it reflects the interrupt signal state coming into the PSIHB.

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Bits	SCOM	Field Mnemonic: Description
0:26	RO	Reserved
27	ROX	OCC INTERRUPT: Set to '1' when an Interrupt line from the OCC is active
28	ROX	FSI INTERRUPT: Set to '1' when an Interrupt line from the FSI is active
29	ROX	LPC INTERRUPT: Set to '1' when an Interrupt line from the LPC is active
30	ROX	LOCAL ERROR INTERRUPT: Set to '1' when an Interrupt line from the LOCAL ERROR is active
31	ROX	HOST ERROR INTERRUPT: Set to '1' when an Interrupt line from the HOST ERROR is active
32	ROX	PSI INTERRUPT ADDRESS ERROR MASK: Set to '1' by hardware when address error CRESP is encountered. This mask off this interrupt. To reset, write to this register (any value will reset all Mask bits)
33	ROX	OCC INTERRUPT ADDRESS ERROR MASK: Set to '1' by hardware when address error CRESP is encountered. This mask off this interrupt. To reset, write to this register (any value will reset all Mask bits)
34	ROX	FSI INTERRUPT ADDRESS ERROR MASK: Set to '1' by hardware when address error CRESP is encountered. This mask off this interrupt. To reset, write to this register (any value will reset all Mask bits)
35	ROX	LPC INTERRUPT ADDRESS ERROR MASK: Set to '1' by hardware when address error CRESP is encountered. This mask off this interrupt. To reset, write to this register (any value will reset all Mask bits)
36	ROX	LOCAL ERROR INTERRUPT ADDRESS ERROR MASK: Set to '1' by hardware when address error CRESP is encountered. This mask off this interrupt. To reset, write to this register (any value will reset all Mask bits)
37	ROX	HOST ERROR INTERRUPT ADDRESS ERROR MASK: Set to '1' by hardware when address error CRESP is encountered. This mask off this interrupt. To reset, write to this register (any value will reset all Mask bits)
38:63	ROX	Reserved

Register Name	<i>XIVR - FSP</i>
Mnemonic	EN.TPC.PSIHB.PSIHB_INTERRUPT_REG
Address	0000000002010910 (SCOM)
Attributes	SCOM: 0x10 MMIO: 0x30
Description	This register contains the XIVR used to signal interrupts to the CEC firmware.

Bits		Field Mnemonic: Description
0:7	RO	Reserved
8:23	RWX	SERVER NUMBER: See Interrupt Control Presenter chapter for definition of the this field. As the POWER8 processor supports Type II interrupts, the low order 2 bits are the link pointer.
24:31	RWX	PRIORITY: Interrupt is disabled when priority is set to x'FF'
32:34	RWX	INTERRUPT SOURCE NUMBER
35:38	RO	Reserved
39	ROX	INTERRUPT COMMAND EXPECTED: Set to '1' by hardware when the PSIHB goes interrupt pending (requests an interrupt command be sent on the fabric), reset to '0' by hardware when an EOI is received and no subsequent interrupts are pending.
40:63	RO	Reserved



Register Name	<i>XIVR - OCC</i>
Mnemonic	EN.TPC.PSIHB.PSIHB_INTERRUPT1_REG
Address	0000000002010916 (SCOM)
Attributes	SCOM: 0x16 MMIO: 0x60
Description	This register contains the XIVR used to signal interrupts to the CEC firmware. Uses the FSP BUID.

Bits	SCOM	Field Mnemonic: Description
0:7	RO	Reserved
8:23	RWX	SERVER NUMBER: See Interrupt Control Presenter chapter for definition of the this field. As the POWER8 processor supports Type II interrupts, the low order 2 bits are the link pointer.
24:31	RWX	PRIORITY: Interrupt is disabled when priority is set to x'FF'
32:34	RWX	INTERRUPT SRC NUMBER
35:38	RO	Reserved
39	ROX	INTERRUPT COMMAND EXPECTED: Set to '1' by hardware when the PSIHB goes interrupt pending (requests an interrupt command be sent on the fabric), reset to '0' by hardware when an EOI is received and no subsequent interrupts are pending.
40:63	RO	Reserved

Register Name	<i>XIVR - FSI</i>
Mnemonic	EN.TPC.PSIHB.PSIHB_INTERRUPT2_REG
Address	0000000002010917 (SCOM)
Attributes	SCOM: 0x17 MMIO: 0x68
Description	This register contains the XIVR used to signal interrupts to the CEC firmware. Uses the FSP BUID

Bits	SCOM	Field Mnemonic: Description
0:7	RO	Reserved
8:23	RWX	SERVER NUMBER: See Interrupt Control Presenter chapter for definition of the this field. As the POWER8 processor supports Type II interrupts, the low order 2 bits are the link pointer.
24:31	RWX	PRIORITY: Interrupt is disabled when priority is set to x'FF'
32:34	RWX	INTERRUPT SOURCE NUMBER
35:38	RO	Reserved
39	ROX	INTERRUPT COMMAND EXPECTED: Set to '1' by hardware when the PSIHB goes interrupt pending (requests an interrupt command be sent on the fabric), reset to '0' by hardware when an EOI is received and no subsequent interrupts are pending.
40:63	RO	Reserved

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Register Name	<i>XIVR - LPC</i>
Mnemonic	EN.TPC.PSIHB.PSIHB_INTERRUPT3_REG
Address	0000000002010918 (SCOM)
Attributes	SCOM: 0x18 MMIO: 0070
Description	This register contains the XIVR used to signal interrupts to the CEC firmware. Uses the FSP BUID.

Bits	SCOM	Field Mnemonic: Description
0:7	RO	Reserved
8:23	RWX	SERVER NUMBER: See Interrupt Control Presenter chapter for definition of the this field. As the POWER8 processor supports Type II interrupts, the low order 2 bits are the link pointer.
24:31	RWX	PRIORITY: Interrupt is disabled when priority is set to x'FF'
32:34	RWX	INTERRUPT SOURCE NUMBER
35:38	RO	Reserved
39	ROX	INTERRUPT COMMAND EXPECTED: Set to '1' by hardware when the PSIHB goes interrupt pending (requests an interrupt command be sent on the fabric), reset to '0' by hardware when an EOI is received and no subsequent interrupts are pending.
40:63	RO	Reserved

Register Name	<i>XIVR - Local Error</i>
Mnemonic	EN.TPC.PSIHB.PSIHB_INTERRUPT4_REG
Address	0000000002010919 (SCOM)
Attributes	SCOM: 0x19 MMIO: 0078
Description	This register contains the XIVR used to signal interrupts to the CEC firmware. Uses the FSP BUID.

Bits	SCOM	Field Mnemonic: Description
0:7	RO	Reserved
8:23	RWX	SERVER NUMBER: See Interrupt Control Presenter chapter for definition of the this field. As the POWER8 processor supports Type II interrupts, the low order 2 bits are the link pointer.
24:31	RWX	PRIORITY: Interrupt is disabled when priority is set to x'FF'
32:34	RWX	INTERRUPT SOURCE NUMBER
35:38	RO	Reserved
39	ROX	INTERRUPT COMMAND EXPECTED: Set to '1' by hardware when the PSIHB goes interrupt pending (requests an interrupt command be sent on the fabric), reset to '0' by hardware when an EOI is received and no subsequent interrupts are pending.
40:63	RO	Reserved

Register Name	<i>XIVR - Host Error</i>
Mnemonic	EN.TPC.PSIHB.PSIHB_INTERRUPT5_REG
Address	000000000201091A (SCOM)
Attributes	SCOM: 0x1A MMIO: 0080
Description	This register contains the XIVR used to signal interrupts to the CEC firmware. Uses the FSP BUID.



Bits	SCOM	Field Mnemonic: Description
0:7	RO	Reserved
8:23	RWX	SERVER NUMBER: See Interrupt Control Presenter chapter for definition of the this field. As the POWER8 processor supports Type II interrupts, the low order 2 bits are the link pointer.
24:31	RWX	PRIORITY: Interrupt is disabled when priority is set to x'FF'
32:34	RWX	INTERRUPT SOURCE NUMBER
35:38	RO	Reserved
39	ROX	INTERRUPT COMMAND EXPECTED: Set to '1' by hardware when the PSIHb goes interrupt pending (requests an interrupt command be sent on the fabric), reset to '0' by hardware when an EOI is received and no subsequent interrupts are pending.
40:63	RO	Reserved

Register Name	<i>Interrupt Requester Source Compare Register</i>
Mnemonic	EN.TPC.PSIHB.PSIHB_ISRN_REG
Address	000000000201091B (SCOM)
Attributes	SCOM: 0x1B MMIO: 0x88
Description	This register contains the registers that identifies the PSIHb interrupt source number. This replaces the BUID.

Bits	SCOM	Field Mnemonic: Description
0:18	RWX	IRSN COMPARE REGISTER: Interrupt source programmable compare register. When creating a ris Interrupt Request command the PSHB masks its IRSN_compare register with its IRSN_compare_mask and adds (via OR) the internal device Interrupt source number to the lower three order bits. The Interrupt Source number are specified in each individual XIVR. When a ris cmd is detected PSIHb detects if it is the target of that command by taking the command bits 18 to 24, 26 to 36 are masked by the unit's IRSN_compare_mask and then compared to the unit's IRSN_compare register. The internal device Interrupt number is derived from the lower order three bits.
19:28	RO	Reserved
29	WOX	ICS RESET: This reset the Interrupt sequence and queues. This is a set only bit.
30	RWX	DOWNSTREAM INTERRUPT ENABLE: This enables the PSI to snoop EOI and RET commands from the PowerBus. When disable, PSIHb will provide the LPC_ACK to these commands
31	RWX	UPSTREAM INTERRUPT ENABLE: This enables the PSI to send Interrupts to the PowerBus
32:50	RWX	IRSN COMPARE MASK: 32:37 - These are hardcoded to '1' in the hardware 38-50 - These are programmable
51:63	RO	Reserved

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Register Name	<i>Untrusted Bar 0 Register</i>
Mnemonic	EN.TPC.PSIHB.NOTRUST_BAR0
Address	0000000002013F40 (SCOM)
Attributes	SCOM: 0x20 No MMIO Access
Description	This register defines the 30bit system address used to identify the memory space that the FSP can write while in Trusted Boot mode. A Untrusted BAR register set consist of Untrused_BAR and Untrustedmem_BARmsk. Each Bar register set opens an area to be accessible by the FSP via PSI and such becomes untrusted. The access is possible when the condition (write_address AND untrusted_BARmsk) = untrusted_BAR) becomes true (and not TCE) Please note: The mask defines not only the width of the area but also the boundary on which the area starts. Both address and mask register will be implemented logically as 64 Bit register. The Bits 0 to address start position are not implemented and are always zero. (e.g. p8 Bits 0 to 13 are not implemented) The Bits 44 to 63 are not implemented and are always zero, such allowing for a minimal area of 1Meg (starting in a 1Meg boundary) At clock start all implemented bits of the untrused_BAR is set to '1' and all bits of the untrusted_BARmsk is set to '0', such that all write accesses to memory are blocked.

Bits	SCOM	Field Mnemonic: Description
0:13	RO	Reserved
14:43	RWX	UNTRUSTED BAR0: Address of untrusted memory area, defaults to all 1s.
44:63	RO	Reserved

Register Name	<i>Untrusted Bar 1 Register</i>
Mnemonic	EN.TPC.PSIHB.NOTRUST_BAR1
Address	0000000002013F41 (SCOM)
Attributes	SCOM: 0x21 No MMIO access
Description	This register defines the 30bit system address used to identify the memory space that the FSP can write while in Trusted Boot mode.

Bits	SCOM	Field Mnemonic: Description
0:13	RO	Reserved
14:43	RWX	UNTRUSTED BAR1: Address of untrusted memory area, defaults to all 1s.
44:63	RO	Reserved

Register Name	<i>Untrusted BarMask 0 Register</i>
Mnemonic	EN.TPC.PSIHB.NOTRUST_BAR0MASK
Address	0000000002013F42 (SCOM)
Attributes	SCOM: 0x22 No MMIO access
Description	This register defines the 30bit system address used to identify the memory space that the FSP can write while in Trusted Boot mode.

Bits	SCOM	Field Mnemonic: Description
0:13	RO	Reserved
14:43	RWX	UNTRUSTED BAR0 MASK: Mask for address of untrusted memory area, defaults to all 0s.
44:63	RO	Reserved

Register Name	<i>Untrusted BarMask 1 Register</i>
Mnemonic	EN.TPC.PSIHB.NOTRUST_BAR1MASK
Address	0000000002013F43 (SCOM)
Attributes	SCOM: 0x23 No MMIO access
Description	This register defines the 30bit system address used to identify the memory space that the FSP can write while in Trusted Boot mode.

Bits	SCOM	Field Mnemonic: Description
0:13	RO	Reserved
14:43	RWX	UNTRUSTED BAR1 MASK: Mask for address of untrusted memory area, defaults to all 0s.
44:63	RO	Reserved

Register Name	<i>TAR - TCE Address Register</i>
Mnemonic	EN.TPC.PSIHB.PSI_TCE_ADDR_REG
Address	0000000002013F44 (SCOM)
Attributes	SCOM: 0x24 MMIO: 0x18
Description	This register identifies the start and size of the TCE table in system memory. This register is used to translate DMA addresses to System Memory addresses only when "enable TCE", bit (2) of FSP_C is set to '1'.

Bits	SCOM	Field Mnemonic: Description
0:13	RO	Reserved
14:41	RWX	TCE TABLE STARTING ADDRESS
42:47	RWX	TCE ADDR MOD: Varies with #TCE Entries, bits 61:63 of TAR: TCE Table Starting Address bits 42 to 47 when TAR bits 61:63 = '000' TCE Table Starting Address bits 42 to 46 when TAR bits 61:63 = '001' TCE Table Starting Address bit 42 when TAR bits 61:63 = '01X' Reserved when TAR bits 61:63 = '1XX'
48:60	RO	Reserved
61:63	RWX	# TCE ENTRIES: This bit determines the maximum number of entries in the TCE table and consequently the maximum FSP DMA address that can be translated. 000: TCE Entries = 8K, Max TCE Address Offset = FFF8, Max FSP Address = 1FF FFFF 001: TCE Entries = 16K, Max TCE Address Offset = 1 FFF8, Max FSP Address = 3FF FFFF 01x: TCE Entries = 256K, Max TCE Address Offset = 1F FFF8, Max FSP Address = 3FFF FFFF 1xx: TCE Entries = 512K, Max TCE Address Offset = 3F FFF8, Max FSP Address = 7FFF FFFF

Registers Specification

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Register Name	<i>TCE - Translation Control Entry</i>
Mnemonic	TCE
Address	
Attributes	Address: N/A Access: None
Description	TCE's are fetched from the TCE table in system memory and cached in the PSIH. Up to 2 TCE's may be cached simultaneously and either TCE may be used for either DMA reads or DMA writes.

Bits	SCOM	Field Mnemonic: Description
0:13	RO	Reserved
14:51	RWX	RPN: This is the real address of the page pointed to by the TCE. The low 12 bits of the FSP DMA address is appended to the real page number to form the complete main store DMA address.
52:61	RO	Reserved
62:63	RWX	Access Control 00 - No Access Allowed (page fault) 01 - Read Only Access 10 - Write Only Access 11 - Read or Write Access

Register Name	<i>PSI Host Bridge Secure Control Register</i>
Mnemonic	EN.TPC.PSIHB.TRUST_CONTROL
Address	0000000002013F45 (SCOM)
Attributes	SCOM: 0x25 MMIO: 0090
Description	This register contains controls for the PSI Host Bridge secure boot function.

Bits	SCOM	Field Mnemonic: Description
0:1	RO	Reserved
2	RWX	TCE ENABLE: This bit controls the use of TCE's to translate incoming FSP addresses to system memory addresses. When set to '1', DMA operations within the low 32 bit FSP address space use the TCE mechanism to access the 48 bit system address space. This bit is similar to the Winnipeg PHB Configuration Register, bit 2.
3:63	RO	Reserved



5. POWER8: EX Chiplet

The POWER8 Processor registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
EXP.EC.FX.FXU_REG0_HOLD_OUT	0x0000000010013300	888
EXP.EC.FX.FXU_REG1_HOLD_OUT	0x0000000010013301	889
EXP.EC.FX.FXU_REG2_HOLD_OUT	0x0000000010013302	889
EXP.EC.FX.FXU_REG3_HOLD_OUT	0x0000000010013303	889
EXP.EC.FX.FXU_REG4_HOLD_OUT	0x0000000010013304	889
EXP.EC.IFU.I.IFFDM.IFFDM_DBG0A_LEV1_CTL	0x000000001001338A	901
EXP.EC.IFU.I.IFFDM.IFFDM_DBG0B_LEV1_CTL	0x000000001001338B	902
EXP.EC.IFU.I.IFFDM.IFFDM_DBG0_LEV2_CTL	0x000000001001338E	905
EXP.EC.IFU.I.IFFDM.IFFDM_DBG1A_LEV1_CTL	0x000000001001338C	903
EXP.EC.IFU.I.IFFDM.IFFDM_DBG1B_LEV1_CTL	0x000000001001338D	904
EXP.EC.IFU.I.IFFDM.IFFDM_DBG1_LEV2_CTL	0x000000001001338F	906
EXP.EC.IFU.I.IFFDM.IFFDM_DBG2_LEV2_CTL	0x0000000010013390	908
EXP.EC.IFU.I.IFFDM.IFFDM_DBG3A_LEV2_CTL	0x0000000010013392	911
EXP.EC.IFU.I.IFFDM.IFFDM_DBG3_LEV2_CTL	0x0000000010013391	909
EXP.EC.IFU.I.IFFDM.IFFDM_IFDMX_OUT1A	0x0000000010013386	897
EXP.EC.IFU.I.IFFDM.IFFDM_IFDMX_OUT1B	0x0000000010013387	898
EXP.EC.IFU.I.IFFDM.IFFDM_IFDMX_OUT2A	0x0000000010013388	899
EXP.EC.IFU.I.IFFDM.IFFDM_IFDMX_OUT2B	0x0000000010013389	900
EXP.EC.IFU.I.IFFDM.IFFDM_MACRO_ENB	0x0000000010013393	912
EXP.EC.IFU.I.IFFDM.IFFDM_SJAR_ADDR	0x0000000010013394	913
EXP.EC.IFU.I.IFFDM.IFFDM_SJAR_DATA	0x0000000010013395	913
EXP.EC.IFU.IFU_REG0_HOLD_OUT	0x0000000010013381	896
EXP.EC.IFU.IFU_REG1_HOLD_OUT	0x0000000010013382	896
EXP.EC.IFU.IFU_REG2_HOLD_OUT	0x0000000010013383	897
EXP.EC.IFU.IFU_REG3_HOLD_OUT	0x0000000010013384	897
EXP.EC.IFU.IFU_REG4_HOLD_OUT	0x0000000010013385	897
EXP.EC.IFU.TCC_CERR_RESET	0x0000000010013380	896
EXP.EC.LS.LSU_REG0_HOLD_OUT	0x00000000100133C0	913
EXP.EC.LS.LSU_REG10_HOLD_OUT	0x00000000100133CA	919
EXP.EC.LS.LSU_REG11_HOLD_OUT	0x00000000100133CB	919
EXP.EC.LS.LSU_REG12_HOLD_OUT	0x00000000100133CC	920
EXP.EC.LS.LSU_REG13_HOLD_OUT	0x00000000100133CD	920
EXP.EC.LS.LSU_REG14_HOLD_OUT	0x00000000100133CE	920
EXP.EC.LS.LSU_REG15_HOLD_OUT	0x00000000100133CF	921
EXP.EC.LS.LSU_REG1_HOLD_OUT	0x00000000100133C1	914
EXP.EC.LS.LSU_REG2_HOLD_OUT	0x00000000100133C2	914
EXP.EC.LS.LSU_REG3_HOLD_OUT	0x00000000100133C3	915
EXP.EC.LS.LSU_REG4_HOLD_OUT	0x00000000100133C4	915
EXP.EC.LS.LSU_REG5_HOLD_OUT	0x00000000100133C5	916
EXP.EC.LS.LSU_REG6_HOLD_OUT	0x00000000100133C6	916
EXP.EC.LS.LSU_REG7_HOLD_OUT	0x00000000100133C7	917
EXP.EC.LS.LSU_REG8_HOLD_OUT	0x00000000100133C8	918
EXP.EC.LS.LSU_REG9_HOLD_OUT	0x00000000100133C9	918



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Mnemonic	Address	Page
EXP.EC.PC.PC_NE.FIR.CORE_ACTION0	0x0000000010013106	847
EXP.EC.PC.PC_NE.FIR.CORE_ACTION1	0x0000000010013107	848
EXP.EC.PC.PC_NE.FIR.CORE_FIR	0x0000000010013100	843
EXP.EC.PC.PC_NE.FIR.CORE_FIRMASK	0x0000000010013103	845
EXP.EC.PC.PC_NE.FIR.CORE_WOF	0x0000000010013108	850
EXP.EC.PC.PC_NE.FIR.FIR_ERRINJREG	0x000000001001310A	853
EXP.EC.PC.PC_NE.FIR.FIR_MODEREG	0x000000001001310C	854
EXP.EC.PC.PC_NE.FIR.FIR_RANDOMLFSR	0x0000000010013109	853
EXP.EC.PC.PC_NE.FIR.RAM_CTRL_REG	0x0000000010013C01	922
EXP.EC.PC.PC_NE.FIR.RAM_MODE_REG	0x0000000010013C00	921
EXP.EC.PC.PC_NE.FIR.RAM_STATUS_REG	0x0000000010013C02	922
EXP.EC.PC.PC_NE.FIR.RCVY_THOLD_VAL	0x000000001001310D	855
EXP.EC.PC.PC_NE.FIR.RECOV_THRESHOLD	0x000000001001310B	854
EXP.EC.PC.PC_NE.FIR.RESET_KEEPER	0x000000001001310F	855
EXP.EC.PC.PC_NE.FIR.THREAD_ACTIVE	0x000000001001310E	855
EXP.EC.PC.PC_NE.FIR.TRUSTED_BOOT_EN_REG	0x0000000010013C03	922
EXP.EC.PC.PC_NE.PCNE_DEBUG_SEL0	0x0000000010013111	857
EXP.EC.PC.PC_NE.PCNE_DEBUG_SEL1	0x0000000010013112	857
EXP.EC.PC.PC_NE.PCNE_DEBUG_SEL2	0x0000000010013113	857
EXP.EC.PC.PC_NE.PCNE_REG0_HOLD_OUT	0x000000001001300D	780
EXP.EC.PC.PC_NE.PCNE_REG1_HOLD_OUT	0x000000001001301D	789
EXP.EC.PC.PC_NE.PCNE_REG2_HOLD_OUT	0x000000001001302D	797
EXP.EC.PC.PC_NE.PCNE_REG3_HOLD_OUT	0x000000001001303D	806
EXP.EC.PC.PC_NE.PCNE_REG4_HOLD_OUT	0x000000001001304D	815
EXP.EC.PC.PC_NE.PCNE_REG5_HOLD_OUT	0x000000001001305D	824
EXP.EC.PC.PC_NE.PCNE_REG6_HOLD_OUT	0x000000001001306D	833
EXP.EC.PC.PC_NE.PCNE_REG7_HOLD_OUT	0x000000001001307D	842
EXP.EC.PC.PC_NE.PCNE_REG8_HOLD_OUT	0x0000000010013110	856
EXP.EC.PC.PC_NE.TCTL0.DIRECT_CONTROLS	0x0000000010013000	773
EXP.EC.PC.PC_NE.TCTL0.HANG_CONTROL	0x0000000010013003	776
EXP.EC.PC.PC_NE.TCTL0.POW_STATUS	0x0000000010013004	777
EXP.EC.PC.PC_NE.TCTL0.RAS_MODEREG	0x0000000010013001	774
EXP.EC.PC.PC_NE.TCTL0.RAS_STATUS	0x0000000010013002	774
EXP.EC.PC.PC_NE.TCTL0.SDI	0x0000000010013009	779
EXP.EC.PC.PC_NE.TCTL0.SDI_MASK	0x000000001001300C	780
EXP.EC.PC.PC_NE.TCTL0.SPATTN	0x0000000010013005	778
EXP.EC.PC.PC_NE.TCTL0.SPATTN_MASK	0x0000000010013008	779
EXP.EC.PC.PC_NE.TCTL1.DIRECT_CONTROLS	0x0000000010013010	781
EXP.EC.PC.PC_NE.TCTL1.HANG_CONTROL	0x0000000010013013	784
EXP.EC.PC.PC_NE.TCTL1.POW_STATUS	0x0000000010013014	785
EXP.EC.PC.PC_NE.TCTL1.RAS_MODEREG	0x0000000010013011	782
EXP.EC.PC.PC_NE.TCTL1.RAS_STATUS	0x0000000010013012	783
EXP.EC.PC.PC_NE.TCTL1.SDI	0x0000000010013019	788
EXP.EC.PC.PC_NE.TCTL1.SDI_MASK	0x000000001001301C	788
EXP.EC.PC.PC_NE.TCTL1.SPATTN	0x0000000010013015	787
EXP.EC.PC.PC_NE.TCTL1.SPATTN_MASK	0x0000000010013018	787
EXP.EC.PC.PC_NE.TCTL2.DIRECT_CONTROLS	0x0000000010013020	789
EXP.EC.PC.PC_NE.TCTL2.HANG_CONTROL	0x0000000010013023	792



Mnemonic	Address	Page
EXP.EC.PC.PC_NE.TCTL2.POW_STATUS	0x0000000010013024	793
EXP.EC.PC.PC_NE.TCTL2.RAS_MODEREG	0x0000000010013021	790
EXP.EC.PC.PC_NE.TCTL2.RAS_STATUS	0x0000000010013022	791
EXP.EC.PC.PC_NE.TCTL2.SDI	0x0000000010013029	796
EXP.EC.PC.PC_NE.TCTL2.SDI_MASK	0x000000001001302C	796
EXP.EC.PC.PC_NE.TCTL2.SPATTN	0x0000000010013025	795
EXP.EC.PC.PC_NE.TCTL2.SPATTN_MASK	0x0000000010013028	795
EXP.EC.PC.PC_NE.TCTL3.DIRECT_CONTROLS	0x0000000010013030	797
EXP.EC.PC.PC_NE.TCTL3.HANG_CONTROL	0x0000000010013033	801
EXP.EC.PC.PC_NE.TCTL3.POW_STATUS	0x0000000010013034	802
EXP.EC.PC.PC_NE.TCTL3.RAS_MODEREG	0x0000000010013031	798
EXP.EC.PC.PC_NE.TCTL3.RAS_STATUS	0x0000000010013032	799
EXP.EC.PC.PC_NE.TCTL3.SDI	0x0000000010013039	805
EXP.EC.PC.PC_NE.TCTL3.SDI_MASK	0x000000001001303C	805
EXP.EC.PC.PC_NE.TCTL3.SPATTN	0x0000000010013035	804
EXP.EC.PC.PC_NE.TCTL3.SPATTN_MASK	0x0000000010013038	804
EXP.EC.PC.PC_NE.TCTL4.DIRECT_CONTROLS	0x0000000010013040	806
EXP.EC.PC.PC_NE.TCTL4.HANG_CONTROL	0x0000000010013043	810
EXP.EC.PC.PC_NE.TCTL4.POW_STATUS	0x0000000010013044	811
EXP.EC.PC.PC_NE.TCTL4.RAS_MODEREG	0x0000000010013041	807
EXP.EC.PC.PC_NE.TCTL4.RAS_STATUS	0x0000000010013042	808
EXP.EC.PC.PC_NE.TCTL4.SDI	0x0000000010013049	814
EXP.EC.PC.PC_NE.TCTL4.SDI_MASK	0x000000001001304C	814
EXP.EC.PC.PC_NE.TCTL4.SPATTN	0x0000000010013045	813
EXP.EC.PC.PC_NE.TCTL4.SPATTN_MASK	0x0000000010013048	813
EXP.EC.PC.PC_NE.TCTL5.DIRECT_CONTROLS	0x0000000010013050	815
EXP.EC.PC.PC_NE.TCTL5.HANG_CONTROL	0x0000000010013053	819
EXP.EC.PC.PC_NE.TCTL5.POW_STATUS	0x0000000010013054	820
EXP.EC.PC.PC_NE.TCTL5.RAS_MODEREG	0x0000000010013051	816
EXP.EC.PC.PC_NE.TCTL5.RAS_STATUS	0x0000000010013052	817
EXP.EC.PC.PC_NE.TCTL5.SDI	0x0000000010013059	823
EXP.EC.PC.PC_NE.TCTL5.SDI_MASK	0x000000001001305C	823
EXP.EC.PC.PC_NE.TCTL5.SPATTN	0x0000000010013055	822
EXP.EC.PC.PC_NE.TCTL5.SPATTN_MASK	0x0000000010013058	822
EXP.EC.PC.PC_NE.TCTL6.DIRECT_CONTROLS	0x0000000010013060	824
EXP.EC.PC.PC_NE.TCTL6.HANG_CONTROL	0x0000000010013063	828
EXP.EC.PC.PC_NE.TCTL6.POW_STATUS	0x0000000010013064	829
EXP.EC.PC.PC_NE.TCTL6.RAS_MODEREG	0x0000000010013061	825
EXP.EC.PC.PC_NE.TCTL6.RAS_STATUS	0x0000000010013062	826
EXP.EC.PC.PC_NE.TCTL6.SDI	0x0000000010013069	832
EXP.EC.PC.PC_NE.TCTL6.SDI_MASK	0x000000001001306C	832
EXP.EC.PC.PC_NE.TCTL6.SPATTN	0x0000000010013065	831
EXP.EC.PC.PC_NE.TCTL6.SPATTN_MASK	0x0000000010013068	831
EXP.EC.PC.PC_NE.TCTL7.DIRECT_CONTROLS	0x0000000010013070	833
EXP.EC.PC.PC_NE.TCTL7.HANG_CONTROL	0x0000000010013073	837
EXP.EC.PC.PC_NE.TCTL7.POW_STATUS	0x0000000010013074	838
EXP.EC.PC.PC_NE.TCTL7.RAS_MODEREG	0x0000000010013071	834
EXP.EC.PC.PC_NE.TCTL7.RAS_STATUS	0x0000000010013072	835



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EXP.EC.PC.PC_NE.TCTL7.SDI	0x0000000010013079	841
EXP.EC.PC.PC_NE.TCTL7.SDI_MASK	0x000000001001307C	841
EXP.EC.PC.PC_NE.TCTL7.SPATTN	0x0000000010013075	840
EXP.EC.PC.PC_NE.TCTL7.SPATTN_MASK	0x0000000010013078	840
EXP.EC.PC.PC_NW.PCNW_REG0_HOLD_OUT	0x00000000100132A9	875
EXP.EC.PC.PC_NW.PCNW_REG1_HOLD_OUT	0x00000000100132AA	876
EXP.EC.PC.PC_NW.PROCESSOR_CORE_PFTH_MODEREG	0x00000000100132A7	875
EXP.EC.PC.PC_NW.SPRD.CTRL	0x0000000010013282	859
EXP.EC.PC.PC_NW.SPRD.DEBUG_CONTROLS	0x00000000100132AF	878
EXP.EC.PC.PC_NW.SPRD.HID0	0x000000001001329C	870
EXP.EC.PC.PC_NW.SPRD.HMEER	0x000000001001329B	870
EXP.EC.PC.PC_NW.SPRD.HV_STATE	0x000000001001329D	871
EXP.EC.PC.PC_NW.SPRD.L0_SCOM_SPRC	0x0000000010013280	858
EXP.EC.PC.PC_NW.SPRD.PCNW_DBGBUS_SEL	0x00000000100132AE	877
EXP.EC.PC.PC_NW.SPRD.PFTH_THROT_REG	0x00000000100132AD	877
EXP.EC.PC.PC_NW.SPRD.SCOM_SPRC_OCC	0x00000000100132AB	877
EXP.EC.PC.PC_NW.SPRD.SPR_MODE	0x0000000010013281	858
EXP.EC.PC.PC_NW.SPRD.T0_HMER	0x000000001001328B	862
EXP.EC.PC.PC_NW.SPRD.T1_HMER	0x000000001001328C	863
EXP.EC.PC.PC_NW.SPRD.T2_HMER	0x000000001001328D	864
EXP.EC.PC.PC_NW.SPRD.T3_HMER	0x000000001001328E	865
EXP.EC.PC.PC_NW.SPRD.T4_HMER	0x000000001001328F	866
EXP.EC.PC.PC_NW.SPRD.T5_HMER	0x0000000010013290	867
EXP.EC.PC.PC_NW.SPRD.T6_HMER	0x0000000010013291	868
EXP.EC.PC.PC_NW.SPRD.T7_HMER	0x0000000010013292	869
EXP.EC.PC.PC_NW.TFC.TOD_READ	0x00000000100132A1	872
EXP.EC.PC.PC_NW.TFC.TOD_SYNC000	0x00000000100132A1	872
EXP.EC.PC.PC_NW.TFC.TOD_SYNC001	0x00000000100132A1	872
EXP.EC.PC.PC_NW.TFC.TOD_SYNC010	0x00000000100132A1	873
EXP.EC.PC.PC_NW.TFC.TOD_SYNC011	0x00000000100132A1	873
EXP.EC.PC.PC_NW.TFC.TOD_SYNC100	0x00000000100132A1	873
EXP.EC.PC.PC_NW.TFC.TOD_SYNC101	0x00000000100132A1	874
EXP.EC.PC.PC_NW.TFC.TOD_SYNC110	0x00000000100132A1	874
EXP.EC.PC.PC_NW.TFC.TOD_SYNC111	0x00000000100132A1	874
EXP.EC.PC.PC_NW.TFP.PWM_EVENTS	0x00000000100132A2	874
EXP.EC.PC.PC_NW.TFP.SPURR_FREQ_DETECT_CYC_CNT	0x000000001001329E	871
EXP.EC.PC.PC_NW.TFP.SPURR_FREQ_REF	0x00000000100132A0	872
EXP.EC.PC.PC_NW.TFP.SPURR_FREQ_SCALE	0x000000001001329F	871
EXP.EC.PC.PC_NW.TRACE0.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	0x0000000010012C00	769
EXP.EC.PC.PC_NW.TRACE0.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	0x0000000010012C01	769
EXP.EC.PC.PC_NW.TRACE1.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	0x0000000010012C40	770
EXP.EC.PC.PC_NW.TRACE1.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	0x0000000010012C41	770
EXP.EC.PC.PC_NW.TRACE2.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	0x0000000010012C80	770
EXP.EC.PC.PC_NW.TRACE2.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	0x0000000010012C81	771
EXP.EC.PC.PC_NW.TRACE3.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	0x0000000010012CC0	771
EXP.EC.PC.PC_NW.TRACE3.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	0x0000000010012CC1	771
EXP.EC.PC.PC_S.IMA_EVENT_MASK	0x00000000100132CF	883
EXP.EC.PC.PC_S.ITRACE.TOD_STEP_CHECK	0x00000000100132D3	887



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EXP.EC.PC.PC_S.PCS_REG0_HOLD_OUT	0x00000000100132CB	882
EXP.EC.PC.PC_S.PCS_REG1_HOLD_OUT	0x00000000100132D5	887
EXP.EC.PC.PC_S.PMUC.SIER_MASK	0x00000000100132C9	881
EXP.EC.PC.PC_S.PMUC.SRC_MASK	0x00000000100132CA	881
EXP.EC.PC.PC_S.PMUT0.PMU_SCOM	0x00000000100132C1	879
EXP.EC.PC.PC_S.PMUT1.PMU_SCOM	0x00000000100132C2	879
EXP.EC.PC.PC_S.PMUT2.PMU_SCOM	0x00000000100132C3	879
EXP.EC.PC.PC_S.PMUT3.PMU_SCOM	0x00000000100132C4	880
EXP.EC.PC.PC_S.PMUT4.PMU_SCOM	0x00000000100132C5	880
EXP.EC.PC.PC_S.PMUT5.PMU_SCOM	0x00000000100132C6	880
EXP.EC.PC.PC_S.PMUT6.PMU_SCOM	0x00000000100132C7	881
EXP.EC.PC.PC_S.PMUT7.PMU_SCOM	0x00000000100132C8	881
EXP.EC.PC.PC_S.SPR_S.CORE_FUSES	0x00000000100132CE	883
EXP.EC.PC.PC_S.SPR_S.FIR_HONORMARKS	0x00000000100132C0	878
EXP.EC.PC.PC_S.SPR_S.HBI_INVALIDATE_ERAT	0x00000000100132CD	882
EXP.EC.PC.PC_S.SPR_S.PCS_DBGBUS_SEL	0x00000000100132D2	885
EXP.EC.PC.PC_S.SPR_S.PMU_INDIRECT_SCOMC_EN_REG	0x00000000100132D4	887
EXP.EC.PC.PC_S.SPR_S.PMU_SCOMC_REG	0x00000000100132D0	884
EXP.EC.PC.PC_S.SPR_S.RMSC_PAGE_SIZE	0x00000000100132CC	882
EXP.EC.PC.PC_S.TRACE4.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	0x0000000010012D00	772
EXP.EC.PC.PC_S.TRACE4.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	0x0000000010012D01	772
EXP.EC.PC.PC_S.TRACE5.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	0x0000000010012D40	772
EXP.EC.PC.PC_S.TRACE5.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	0x0000000010012D41	772
EXP.EC.PC.SCR0	0x0000000010013283	671
EXP.EC.PC.SCR1	0x0000000010013284	671
EXP.EC.PC.SCR2	0x0000000010013285	860
EXP.EC.PC.SCR3	0x0000000010013286	860
EXP.EC.PC.SCR4	0x0000000010013287	861
EXP.EC.PC.SCR5	0x0000000010013288	861
EXP.EC.PC.SCR6	0x0000000010013289	861
EXP.EC.PC.SCR7	0x000000001001328A	861
EXP.EC.SD.ISU_DEBUG_CTRL	0x000000001001334A	896
EXP.EC.SD.ISU_REG0_HOLD_OUT	0x0000000010013340	890
EXP.EC.SD.ISU_REG1_HOLD_OUT	0x0000000010013341	890
EXP.EC.SD.ISU_REG2_HOLD_OUT	0x0000000010013342	891
EXP.EC.SD.ISU_REG3_HOLD_OUT	0x0000000010013343	892
EXP.EC.SD.ISU_REG4_HOLD_OUT	0x0000000010013344	892
EXP.EC.SD.ISU_REG5_HOLD_OUT	0x0000000010013345	893
EXP.EC.SD.ISU_REG6_HOLD_OUT	0x0000000010013346	893
EXP.EC.SD.ISU_REG7_HOLD_OUT	0x0000000010013347	894
EXP.EC.SD.ISU_REG8_HOLD_OUT	0x0000000010013348	895
EXP.EC.SD.ISU_REG9_HOLD_OUT	0x0000000010013349	895
EXP.L2.L2MISC.L2CERRS.EPS_REG	0x0000000010012814	766
EXP.L2.L2MISC.L2CERRS.ERR_INJ_REG	0x000000001001280C	759
EXP.L2.L2MISC.L2CERRS.ERR_RPT0	0x0000000010012815	766
EXP.L2.L2MISC.L2CERRS.ERR_RPT1	0x0000000010012816	769
EXP.L2.L2MISC.L2CERRS.FIR_ACTION0_REG	0x0000000010012806	756
EXP.L2.L2MISC.L2CERRS.FIR_ACTION1_REG	0x0000000010012807	757



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Mnemonic	Address	Page
EXP.L2.L2MISC.L2CERRS.FIR_MASK_REG	0x0000000010012803	756
EXP.L2.L2MISC.L2CERRS.FIR_REG	0x0000000010012800	754
EXP.L2.L2MISC.L2CERRS.HA_CMD_REG	0x0000000010012810	763
EXP.L2.L2MISC.L2CERRS.HA_STAT_REG	0x0000000010012811	764
EXP.L2.L2MISC.L2CERRS.LINEDEL_TRIG_REG	0x000000001001280D	761
EXP.L2.L2MISC.L2CERRS.MODE_REG0	0x000000001001280A	757
EXP.L2.L2MISC.L2CERRS.MODE_REG1	0x000000001001280B	758
EXP.L2.L2MISC.L2CERRS.MP_CMD_REG	0x0000000010012812	765
EXP.L2.L2MISC.L2CERRS.MP_STAT_REG	0x0000000010012813	765
EXP.L2.L2MISC.L2CERRS.PHYP_PURGE_CMD_REG	0x000000001001280F	762
EXP.L2.L2MISC.L2CERRS.PRD_PURGE_CMD_REG	0x000000001001280E	761
EXP.L3.L3_ARB.L3CACTL.DRAM_REF_REG	0x000000001001080F	725
EXP.L3.L3_MISC.L3CERRS.BAR1_REG	0x000000001001080B	722
EXP.L3.L3_MISC.L3CERRS.BAR2_REG	0x0000000010010813	727
EXP.L3.L3_MISC.L3CERRS.BAR_GRP_MASK_REG	0x0000000010010816	729
EXP.L3.L3_MISC.L3CERRS.EDRAM_REG	0x000000001001080C	723
EXP.L3.L3_MISC.L3CERRS.ERR_INJ_REG	0x000000001001080D	723
EXP.L3.L3_MISC.L3CERRS.FIR_ACTION0_REG	0x0000000010010806	721
EXP.L3.L3_MISC.L3CERRS.FIR_ACTION1_REG	0x0000000010010807	721
EXP.L3.L3_MISC.L3CERRS.FIR_MASK_REG	0x0000000010010803	719
EXP.L3.L3_MISC.L3CERRS.FIR_REG	0x0000000010010800	718
EXP.L3.L3_MISC.L3CERRS.L3PRF_CMD_REG	0x000000001001082C	738
EXP.L3.L3_MISC.L3CERRS.L3_CTL_CHECK_RD0_REG	0x0000000010010810	725
EXP.L3.L3_MISC.L3CERRS.L3_CTL_CHECK_RD1_REG	0x0000000010010817	730
EXP.L3.L3_MISC.L3CERRS.L3_HA_CONTROL_REG	0x0000000010010819	731
EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_MEM_BLK_BAR0	0x000000001001081D	732
EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_MEM_BLK_BAR1	0x000000001001081E	733
EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_MEM_BLK_BAR2	0x000000001001081F	733
EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_MEM_BLK_BAR3	0x0000000010010820	733
EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_MEM_BLK_BAR4	0x0000000010010821	734
EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_MEM_BLK_BAR5	0x0000000010010822	734
EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_MEM_BLK_CONS0	0x0000000010010823	734
EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_MEM_BLK_CONS1	0x0000000010010824	734
EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_MEM_BLK_CONS2	0x0000000010010825	735
EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_MEM_BLK_CONS3	0x0000000010010826	735
EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_MEM_BLK_CONS4	0x0000000010010827	735
EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_MEM_BLK_CONS5	0x0000000010010828	736
EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_MEM_BLK_CTL	0x000000001001081C	732
EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_TBL_BAR	0x0000000010010818	730
EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_TBL_RD_PNTR	0x000000001001081A	731
EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_TBL_SAVERESTORE_WR_PNTR	0x0000000010010832	740
EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_TBL_WR_PNTR	0x000000001001081B	731
EXP.L3.L3_MISC.L3CERRS.L3_RD_EPSILON_CFG_REG	0x0000000010010829	736
EXP.L3.L3_MISC.L3CERRS.L3_RTIM_PERIOD_MONITOR	0x0000000010010812	727
EXP.L3.L3_MISC.L3CERRS.L3_WR_EPSILON_CFG_REG	0x000000001001082A	737
EXP.L3.L3_MISC.L3CERRS.LINE_DELETED_MEMBERS_REG	0x0000000010010815	728
EXP.L3.L3_MISC.L3CERRS.LRU_VIC_ALLOC_REG	0x0000000010010811	726
EXP.L3.L3_MISC.L3CERRS.MODE_REG0	0x000000001001082B	737



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EXP.L3.L3_MISC.L3CERRS.MODE_REG1	0x000000001001080A	721
EXP.L3.L3_MISC.L3CERRS.PHYP_PURGE_REG	0x0000000010010814	728
EXP.L3.L3_MISC.L3CERRS.PR_D_PURGE_REG	0x000000001001080E	724
EXP.L3.L3_PRF.L3CACPRF.L3PRF_HIT01_REG	0x000000001001082D	739
EXP.L3.L3_PRF.L3CACPRF.L3PRF_HIT23_REG	0x000000001001082E	739
EXP.L3.L3_PRF.L3CACPRF.L3PRF_HIT45_REG	0x000000001001082F	739
EXP.L3.L3_PRF.L3CACPRF.L3PRF_HIT67_REG	0x0000000010010830	739
EXP.L3.L3_PRF.L3CACPRF.L3PRF_MISS_REG	0x0000000010010831	740
EXP.NC.NCMISC.NCSCOMS.ERR_RPT_REG	0x0000000010010C0C	744
EXP.NC.NCMISC.NCSCOMS.FIR_ACTION0_REG	0x0000000010010C06	742
EXP.NC.NCMISC.NCSCOMS.FIR_ACTION1_REG	0x0000000010010C07	743
EXP.NC.NCMISC.NCSCOMS.FIR_MASK_REG	0x0000000010010C03	741
EXP.NC.NCMISC.NCSCOMS.FIR_REG	0x0000000010010C00	740
EXP.NC.NCMISC.NCSCOMS.INJ_REG	0x0000000010010C0B	744
EXP.NC.NCMISC.NCSCOMS.NCU_MODE_REG	0x0000000010010C0A	743
EXP.NC.NCMISC.NCSCOMS.NCU_MODE_REG2	0x0000000010010C0D	745
EXP.NC.NCMISC.NCSCOMS.NCU_MODE_REG3	0x0000000010010C0E	745
EXP.TP.CORE_DOM.TRAL20.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	0x0000000010012000	753
EXP.TP.CORE_DOM.TRAL20.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	0x0000000010012001	753
EXP.TP.CORE_DOM.TRAL21.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	0x0000000010012400	754
EXP.TP.CORE_DOM.TRAL21.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	0x0000000010012401	754
EXP.TP.ECO_DOM.CC_ATOMIC_LOCK_REG	0x00000000100303FF	942
EXP.TP.ECO_DOM.CC_PROTECT_MODE_REG	0x00000000100303FE	942
EXP.TP.ECO_DOM.CHTM.SC.HTM_CSEL	0x0000000010011007	751
EXP.TP.ECO_DOM.CHTM.SC.HTM_CTRL	0x0000000010011005	750
EXP.TP.ECO_DOM.CHTM.SC.HTM_IMA_PDBAR	0x000000001001100B	752
EXP.TP.ECO_DOM.CHTM.SC.HTM_IMA_STATUS	0x000000001001100A	752
EXP.TP.ECO_DOM.CHTM.SC.HTM_LAST	0x0000000010011003	749
EXP.TP.ECO_DOM.CHTM.SC.HTM_MEM	0x0000000010011001	747
EXP.TP.ECO_DOM.CHTM.SC.HTM_MODE	0x0000000010011000	745
EXP.TP.ECO_DOM.CHTM.SC.HTM_PTRC	0x0000000010011006	751
EXP.TP.ECO_DOM.CHTM.SC.HTM_STAT	0x0000000010011002	748
EXP.TP.ECO_DOM.CHTM.SC.HTM_TRIG	0x0000000010011004	749
EXP.TP.ECO_DOM.CHTM.SC.MEM_OP_CTR	0x0000000010011008	751
EXP.TP.ECO_DOM.CLK_REGION	0x0000000010030006	939
EXP.TP.ECO_DOM.CLOCK_STAT	0x0000000010030008	940
EXP.TP.ECO_DOM.EPS.DBG.DBG_INST1_COND_REG_1	0x00000000100107C1	709
EXP.TP.ECO_DOM.EPS.DBG.DBG_INST1_COND_REG_2	0x00000000100107C2	712
EXP.TP.ECO_DOM.EPS.DBG.DBG_INST2_COND_REG_1	0x00000000100107C3	713
EXP.TP.ECO_DOM.EPS.DBG.DBG_INST2_COND_REG_2	0x00000000100107C4	714
EXP.TP.ECO_DOM.EPS.DBG.DBG_MODE_REG	0x00000000100107C0	708
EXP.TP.ECO_DOM.EPS.DBG.DBG_TRACE_MODE_REG_2	0x00000000100107CB	717
EXP.TP.ECO_DOM.EPS.DBG.DBG_TRACE_REG_0	0x00000000100107C9	714
EXP.TP.ECO_DOM.EPS.DBG.DBG_TRACE_REG_1	0x00000000100107CA	716
EXP.TP.ECO_DOM.EPS.FIR.LOCAL_FIR_ACTION0	0x0000000010040010	946
EXP.TP.ECO_DOM.EPS.FIR.LOCAL_FIR_ACTION1	0x0000000010040011	946
EXP.TP.ECO_DOM.EPS.FIR.LOCAL_FIR_MASK	0x000000001004000D	945
EXP.TP.ECO_DOM.EPS.FIR.MODE_REG	0x0000000010040008	944



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EXP.TP.ECO_DOM.EPS.PSC.ADDR_TRAP_REG	0x0000000010010003	706
EXP.TP.ECO_DOM.EPS.PSC.ATOMIC_LOCK_REG	0x00000000100103FF	708
EXP.TP.ECO_DOM.EPS.PSC.DEBUG_STATUS_REG	0x0000000010010004	707
EXP.TP.ECO_DOM.EPS.PSC.PSCOM_ERROR_MASK	0x0000000010010002	706
EXP.TP.ECO_DOM.EPS.PSC.PSCOM_MODE_REG	0x0000000010010000	704
EXP.TP.ECO_DOM.EPS.PSC.PSCOM_STATUS_ERROR_REG	0x0000000010010001	704
EXP.TP.ECO_DOM.EPS.PSC.PSCOM_WRITE_PROTECT_REG	0x0000000010010005	707
EXP.TP.ECO_DOM.EPS.THERM.CONTROL_REG	0x0000000010050012	955
EXP.TP.ECO_DOM.EPS.THERM.CPM_CONFIG_WRITE_REG0	0x0000000010050000	946
EXP.TP.ECO_DOM.EPS.THERM.CPM_CONFIG_WRITE_REG1	0x0000000010050001	947
EXP.TP.ECO_DOM.EPS.THERM.DTS_RESULT0	0x0000000010050000	947
EXP.TP.ECO_DOM.EPS.THERM.DTS_RESULT1	0x0000000010050001	948
EXP.TP.ECO_DOM.EPS.THERM.DTS_TRC_RESULT	0x0000000010050003	948
EXP.TP.ECO_DOM.EPS.THERM.ENC_CPM_RESULT0	0x0000000010050008	950
EXP.TP.ECO_DOM.EPS.THERM.ENC_CPM_RESULT1	0x0000000010050009	951
EXP.TP.ECO_DOM.EPS.THERM.ERR_STATUS_REG	0x0000000010050013	955
EXP.TP.ECO_DOM.EPS.THERM.INJECT_REG	0x0000000010050011	954
EXP.TP.ECO_DOM.EPS.THERM.RAW_CPM_RESULT0	0x0000000010050005	949
EXP.TP.ECO_DOM.EPS.THERM.RAW_CPM_RESULT1	0x0000000010050006	950
EXP.TP.ECO_DOM.EPS.THERM.SKITTER_CLKSRC_REG	0x0000000010050016	957
EXP.TP.ECO_DOM.EPS.THERM.SKITTER_DATA0	0x0000000010050019	957
EXP.TP.ECO_DOM.EPS.THERM.SKITTER_DATA1	0x000000001005001A	957
EXP.TP.ECO_DOM.EPS.THERM.SKITTER_DATA2	0x000000001005001B	958
EXP.TP.ECO_DOM.EPS.THERM.SKITTER_FORCE_REG	0x0000000010050014	957
EXP.TP.ECO_DOM.EPS.THERM.SKITTER_MODE_REG	0x0000000010050010	954
EXP.TP.ECO_DOM.EPS.THERM.THERM_MODE_REG	0x000000001005000F	952
EXP.TP.ECO_DOM.EPS.THERM.TIMESTAMP_COUNTER_READ	0x000000001005001C	958
EXP.TP.ECO_DOM.ERROR_STATUS	0x0000000010030009	941
EXP.TP.ECO_DOM.FIR_MASK	0x0000000010040002	943
EXP.TP.ECO_DOM.GP0	0x0000000010000000	658
EXP.TP.ECO_DOM.GP1	0x0000000010000001	701
EXP.TP.ECO_DOM.GP2	0x0000000010000002	702
EXP.TP.ECO_DOM.GP4	0x0000000010000003	702
EXP.TP.ECO_DOM.GPIO_ATOMIC_LOCK_REG	0x00000000100003FF	704
EXP.TP.ECO_DOM.GPIO_PROTECT_MODE_REG	0x00000000100003FE	703
EXP.TP.ECO_DOM.LOCAL_FIR	0x000000001004000A	945
EXP.TP.ECO_DOM.OHA.OHA_ACTIVITY_AND_FREQU_REG	0x0000000010020004	926
EXP.TP.ECO_DOM.OHA.OHA_ACTIVITY_SAMPLE_MODE_REG	0x0000000010020000	923
EXP.TP.ECO_DOM.OHA.OHA_AISS_IO_REG	0x0000000010020014	933
EXP.TP.ECO_DOM.OHA.OHA_ARCH_IDLE_STATE_REG	0x0000000010020011	931
EXP.TP.ECO_DOM.OHA.OHA_COUNTER_REG	0x0000000010020005	926
EXP.TP.ECO_DOM.OHA.OHA_CPM_CTRL_REG	0x000000001002000A	928
EXP.TP.ECO_DOM.OHA.OHA_CPM_HIST_RESET_REG	0x0000000010020013	932
EXP.TP.ECO_DOM.OHA.OHA_ERROR_AND_ERROR_MASK_REG	0x000000001002000E	930
EXP.TP.ECO_DOM.OHA.OHA_LOW_ACTIVITY_DETECT_MODE_REG	0x0000000010020003	925
EXP.TP.ECO_DOM.OHA.OHA_MODE_REG	0x000000001002000D	929
EXP.TP.ECO_DOM.OHA.OHA_PMU_CONFIG_REG	0x0000000010020012	932
EXP.TP.ECO_DOM.OHA.OHA_PPT_BAR_REG	0x0000000010020015	935



Mnemonic	Address	Page
EXP.TP.ECO_DOM.OHA.OHA_PROXY_LEGACY_REG	0x0000000010020007	927
EXP.TP.ECO_DOM.OHA.OHA_PROXY_REG	0x0000000010020006	926
EXP.TP.ECO_DOM.OHA.OHA_RO_STATUS_REG	0x000000001002000B	929
EXP.TP.ECO_DOM.OHA.OHA_SKITTER_CTRL_MODE_REG	0x0000000010020008	927
EXP.TP.ECO_DOM.OHA.OHA_VCS_ACTIVITY_CNT_REG	0x0000000010020001	925
EXP.TP.ECO_DOM.OHA.OHA_VDD_ACTIVITY_CNT_REG	0x0000000010020002	925
EXP.TP.ECO_DOM.OPCG_REG0	0x0000000010030002	936
EXP.TP.ECO_DOM.OPCG_REG1	0x0000000010030003	937
EXP.TP.ECO_DOM.OPCG_REG2	0x0000000010030004	937
EXP.TP.ECO_DOM.OPCG_REG3	0x0000000010030005	938
EXP.TP.ECO_DOM.PHASE_SHADOW	0x0000000010030001	936
EXP.TP.ECO_DOM.RFIR	0x0000000010040001	943
EXP.TP.ECO_DOM.SCANSELQ	0x0000000010030007	939
EXP.TP.ECO_DOM.SPATTN	0x0000000010040004	944
EXP.TP.ECO_DOM.SPA_MASK	0x0000000010040007	944
EXP.TP.ECO_DOM.SYNC_CONFIG	0x0000000010030000	935
EXP.TP.ECO_DOM.TRAECO.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	0x0000000010010400	708
EXP.TP.ECO_DOM.TRAECO.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	0x0000000010010401	708
EXP.TP.ECO_DOM.XFIR	0x0000000010040000	942

The POWER8 Processor registers are listed in the following tables.

Register Name	<i>GP Register 0</i>
Mnemonic	EXP.TP.ECO_DOM.GP0
Address	0000000010000000 (PCB) 0000000010000004 (PCB1) 0000000010000005 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	NOT_USED0: not used, Reset(0b0)
1	RWX	WOX_AND	WOX_OR	TC_SYNCCLK_MUXSEL_DC: syncclk mux for DPLL, Reset(0b1)
2	RWX	WOX_AND	WOX_OR	TC_GPIO_FLUSHMODE_INH_DC: Prevent plats from going into flush mode (init value 1), Reset(0b1)
3	RWX	WOX_AND	WOX_OR	TC_GPIO_FORCEALIGN: Force align signal to be sent (init value 1, drop before dropping flushmode_inh), Reset(0b1)
4	RWX	WOX_AND	WOX_OR	TC_GPIO_AVP_MODE_DC: Enable AVP mode, Reset(0b0)
5	RWX	WOX_AND	WOX_OR	TCEX_GCLK_ENABLE_CLK_DC_B__CORE_NCLK: ECO mode core clock disable, Reset(0b0)
6	RWX	WOX_AND	WOX_OR	TC_SCAN_DIS_DC_B: Disable scan - set output of scan chain to zero, Reset(0b0)

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
7	RWX	WOX_AND	WOX_OR	TC_SKIT_MODE_BIST_DC: Enable Skitter measuring during BIST, Reset(0b0)
8	RWX	WOX_AND	WOX_OR	TC_LBIST_EN_DC: LBIST mode, Reset(0b0)
9	RWX	WOX_AND	WOX_OR	TC_LBIST_AC_MODE_DC: LBIST AC mode, Reset(0b0)
10	RWX	WOX_AND	WOX_OR	TC_LBIST_ARY_WRT_THRU_DC: Array write-through mode - set Array in bypass mode, Reset(0b0)
11	RWX	WOX_AND	WOX_OR	TC_ABIST_MODE_DC: perv and L3*, Reset(0b0)
12	RWX	WOX_AND	WOX_OR	TC_ABIST_START_TEST_DC: Set to start ABIST testing, Reset(0b0)
13	RWX	WOX_AND	WOX_OR	TC_ABIST_MODE2_DC: PC and L2, Reset(0b0)
14	RWX	WOX_AND	WOX_OR	TC_ATPG_EN_DC: ATPG mode, Reset(0b0)
15	RWX	WOX_AND	WOX_OR	TC_SCAN_PROTECT_DC: Scan protection enable (init value 1), Reset(0b1)
16	RWX	WOX_AND	WOX_OR	NOT_USED1: not used, Reset(0b1)
17	RWX	WOX_AND	WOX_OR	NOT_USED2: not used, Reset(0b0)
18	RWX	WOX_AND	WOX_OR	NOT_USED3: not used, Reset(0b0)
19	RWX	WOX_AND	WOX_OR	TC_L3_FENCE_EDRAM: L3 fence eDRAM, Reset(0b1)
20	RWX	WOX_AND	WOX_OR	TC_DBG_TRACE_START: Start trace to debug macros, Reset(0b0)
21	RWX	WOX_AND	WOX_OR	TC_DBG_TRACE_STOP: Stop trace to debug macros, Reset(0b0)
22	RWX	WOX_AND	WOX_OR	TC_DBG_TRACE_RESET: Reset trace to debug macros, Reset(0b0)
23	RWX	WOX_AND	WOX_OR	NOT_USED4: not used, Reset(0b0)
24:25	RWX	WOX_AND	WOX_OR	TC_GPIO_CLKDIV_SEL_DC: Select clock divider ratio for probing, Reset(0b0)
26	RWX	WOX_AND	WOX_OR	NOT_USED5: not used, Reset(0b0)
27	RWX	WOX_AND	WOX_OR	NOT_USED6: not used: 0b0, Reset(0b0)
28:31	RWX	WOX_AND	WOX_OR	TC_DBG_MUXSEL_DC: Nest debug bus selects(0:3), Reset(0b0)
32:39	RWX	WOX_AND	WOX_OR	TC_PSRO_SEL_DC: PSRO selects(0:7), Reset(0b0)
40:42	RWX	WOX_AND	WOX_OR	TC_NODE_ID_DC: Node ID, Reset(0b0)
43:45	RWX	WOX_AND	WOX_OR	TC_CHIP_ID_DC: Chip ID, Reset(0b0)
46	RWX	WOX_AND	WOX_OR	NOT_USED7: not used, Reset(0b0)
47	RWX	WOX_AND	WOX_OR	NOT_USED8: not used, Reset(0b0)
48	RWX	WOX_AND	WOX_OR	NOT_USED9: not used, Reset(0b0)
49	RWX	WOX_AND	WOX_OR	NOT_USED10: not used, Reset(0b0)
50	RWX	WOX_AND	WOX_OR	NOT_USED11: not used, Reset(0b0)
51	RWX	WOX_AND	WOX_OR	NOT_USED12: not used, Reset(0b0)
52	RWX	WOX_AND	WOX_OR	NOT_USED13: not used, Reset(0b0)
53	RWX	WOX_AND	WOX_OR	NOT_USED14: not used, Reset(0b0)
54	RWX	WOX_AND	WOX_OR	NOT_USED15: not used, Reset(0b0)
55	RWX	WOX_AND	WOX_OR	NOT_USED16: not used, Reset(0b0)
56	RWX	WOX_AND	WOX_OR	NOT_USED17: not used, Reset(0b0)
57	RWX	WOX_AND	WOX_OR	NOT_USED18: not used, Reset(0b0)
58	RWX	WOX_AND	WOX_OR	NOT_USED19: not used, Reset(0b0)



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
59	RWX	WOX_AND	WOX_OR	NOT_USED20: not used, Reset(0b0)
60	RWX	WOX_AND	WOX_OR	TC_MASK_CC_PCB_ERR_DC: Mask for PCB error (access or parity) in CC, Reset(0b0)
61	RWX	WOX_AND	WOX_OR	TC_MASK_CC_SCAN_OPCG_ERR_DC: Mask for PCB write while OPCG_IP / scan collision in CC, Reset(0b0)
62	RWX	WOX_AND	WOX_OR	TC_CC_LCC_EDGE_DELAYED_DC: Offset the clocking in the f domain by one cycle, Reset(0b1)
63	RWX	WOX_AND	WOX_OR	TC_FENCE_PERV_DC: Fence pervasive logic during scan (init value 1), Reset(0b1)

Register Name	GP Register 1
Mnemonic	EXP.TP.ECO_DOM.GP1
Address	0000000010000001 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	TRAECO_TC_ABIST_DONE_DC: ECO trace arrays ABIST done, Reset(0)
1	ROX	PC_TC_ABIST_DONE_DC: Core ABIST done, Reset(0)
2	ROX	L3_TC_ABIST_DONE_DC: L3 ABIST done, Reset(0)
3	ROX	L2CPLX_TC_ABIST_DONE_DC: L2, L2 trace arrays ABIST done, Reset(0)
4	ROX	ECODOM_TC_DIAG_PORT: Diag out of L3, Reset(0)
5	ROX	COREDOM_TC_DIAG_PORT: diag out of core+L2, Reset(0)
6	ROX	NOT_USED21: not used, Reset(0)
7	ROX	NOT_USED22: not used, Reset(0)
8	ROX	PC_TC_VALID_NOT_HV_MODE: Set if core is in a valid non HV mode after clock stop (Firmware debug), Reset(0)
9	ROX	PC_TC_AVP_OUT: Set if the AVP running on the core set the appropriate SPR bit, Reset(0)
10	ROX	NOT_USED23: not used, Reset(0)
11	ROX	NOT_USED24: not used, Reset(0)
12	ROX	NOT_USED25: not used, Reset(0)
13	ROX	NOT_USED26: not used, Reset(0)
14	ROX	NOT_USED27: not used, Reset(0)
15	ROX	TC_OPCG_DONE_DC: Clock control OPCG done, Reset(0)
16	ROX	FREE_USAGE0: chiplet specific, Reset(0)
17	ROX	FREE_USAGE1: chiplet specific, Reset(0)
18	ROX	FREE_USAGE2: chiplet specific, Reset(0)
19	ROX	FREE_USAGE3: chiplet specific, Reset(0)
20	ROX	FREE_USAGE4: chiplet specific, Reset(0)
21	ROX	FREE_USAGE5: chiplet specific, Reset(0)
22	ROX	FREE_USAGE6: chiplet specific, Reset(0)

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Bits	PCB	Field Mnemonic: Description
23	ROX	FREE_USAGE7: chiplet specific, Reset(0)

Register Name	GP Register 2
Mnemonic	EXP.TP.ECO_DOM.GP2
Address	0000000010000002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:23	RW	GPIN_MASKING: GPIN bitwise interrupt masking

Register Name	GP Register 4
Mnemonic	EXP.TP.ECO_DOM.GP4
Address	0000000010000003 (PCB) 0000000010000006 (PCB1) 0000000010000007 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0:5	RWX	WOX_AND	WOX_OR	TC_PROBE0_SEL_DC: Probe 0 select - Reset(0b000000)
6:7	RWX	WOX_AND	WOX_OR	NOT_USED28: not used: 0b0, Reset(0b00)
8:13	RWX	WOX_AND	WOX_OR	TC_PROBE1_SEL_DC: Probe 1 select - Reset(0b000000)
14:15	RWX	WOX_AND	WOX_OR	NOT_USED29: not used: 0b0, Reset(0b00)
16:21	RWX	WOX_AND	WOX_OR	TC_PROBE2_SEL_DC: Probe 2 select - Reset(0b000000)
22:23	RWX	WOX_AND	WOX_OR	NOT_USED30: not used: 0b0, Reset(0b00)
24:29	RWX	WOX_AND	WOX_OR	TC_PROBE3_SEL_DC: tc_probe3_sel_dc(0:5) / tcex_amux_sel_dc(0:2), tcl3_amux_sel_dc(0:2), Reset(0b000000)
30	RWX	WOX_AND	WOX_OR	NOT_USED31: not used: 0b0, Reset(0b0)
31	RWX	WOX_AND	WOX_OR	TC_GP4_OFLOW_FEH_SEL_DC: ABIST: when 1, fail bit is overflow, otherwise its a fail, Reset(0b0)
32	RWX	WOX_AND	WOX_OR	NOT_USED32: not used, Reset(0b0)
33	RWX	WOX_AND	WOX_OR	NOT_USED33: not used, Reset(0b0)
34	RWX	WOX_AND	WOX_OR	NOT_USED34: not used, Reset(13s: 0b1 c22: 0b0)
35	RWX	WOX_AND	WOX_OR	NOT_USED35: not used, Reset(0b0)
36	RWX	WOX_AND	WOX_OR	NOT_USED36: not used, Reset(0b0)
37	RWX	WOX_AND	WOX_OR	NOT_USED37: not used, Reset(0b0)
38	RWX	WOX_AND	WOX_OR	NOT_USED38: not used, Reset(0b0)
39	RWX	WOX_AND	WOX_OR	TC_DPLL_SS_ENABLE_DC: Internal Spread Spectrum Enable, Reset(0b0)



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
40	RWX	WOX_AND	WOX_OR	NOT_USED39: not used, Reset(13s: 0b1 c22: 0b0)
41	RWX	WOX_AND	WOX_OR	NOT_USED40: not used, Reset(0b0)
42	RWX	WOX_AND	WOX_OR	NOT_USED41: not used, Reset(0b0)
43	RWX	WOX_AND	WOX_OR	NOT_USED42: not used, Reset(0b0)
44	RWX	WOX_AND	WOX_OR	NOT_USED43: not used, Reset(0b0)
45	RWX	WOX_AND	WOX_OR	NOT_USED44: not used, Reset(0b0)
46	RWX	WOX_AND	WOX_OR	NOT_USED45: not used, Reset(13s: 0b1 c22: 0b0)
47	RWX	WOX_AND	WOX_OR	NOT_USED46: not used, Reset(0b0)
48	RWX	WOX_AND	WOX_OR	NOT_USED47: not used, Reset(0b0)
49	RWX	WOX_AND	WOX_OR	NOT_USED48: not used, Reset(0b0)
50	RWX	WOX_AND	WOX_OR	NOT_USED49: not used, Reset(0b0)
51	RWX	WOX_AND	WOX_OR	NOT_USED50: not used, Reset(0b0)
52	RWX	WOX_AND	WOX_OR	NOT_USED51: not used, Reset(13s: 0b1 c22: 0b0)
53	RWX	WOX_AND	WOX_OR	NOT_USED52: not used, Reset(0b0)
54	RWX	WOX_AND	WOX_OR	NOT_USED53: not used, Reset(0b0)
55	RWX	WOX_AND	WOX_OR	NOT_USED54: not used, Reset(0b0)
56	RWX	WOX_AND	WOX_OR	NOT_USED55: not used, Reset(0b0)
57	RWX	WOX_AND	WOX_OR	NOT_USED56: not used, Reset(0b0)
58	RWX	WOX_AND	WOX_OR	NOT_USED57: not used, Reset(13s: 0b1 c22: 0b0)
59	RWX	WOX_AND	WOX_OR	NOT_USED58: not used, Reset(0b0)
60	RWX	WOX_AND	WOX_OR	NOT_USED59: not used, Reset(0b0)
61	RWX	WOX_AND	WOX_OR	NOT_USED60: not used, Reset(0b0)
62	RWX	WOX_AND	WOX_OR	NOT_USED61: not used, Reset(0b0)
63	RWX	WOX_AND	WOX_OR	NOT_USED62: not used, Reset(0b0)

Register Name	CC Protect Mode Register
Mnemonic	EXP.TP.ECO_DOM.GPIO_PROTECT_MODE_REG
Address	00000000100003FE (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	GPIO_READ_PROTECT_ENABLE: Enable read protection
1	RW	GPIO_WRITE_PROTECT_ENABLE: Enable write protection

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Register Name	<i>Atomic Lock Register</i>
Mnemonic	EXP.TP.ECO_DOM.GPIO_ATOMIC_LOCK_REG
Address	00000000100003FF (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	GPIO_ATOMIC_LOCK_ENABLE: Enable atomic lock
1:4	ROX	GPIO_ATOMIC_ID: Atomic ID

Register Name	<i>PSCOMLE Mode Register</i>
Mnemonic	EXP.TP.ECO_DOM.EPS.PSC.PSCOM_MODE_REG
Address	0000000010010000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	ABORT_ON_PCB_ADDR_PARITY_ERROR: abort_on_PCB_addr_parity_error
1	RW	ABORT_ON_PCB_WDATA_PARITY_ERROR: abort_on_PCB_wdata_parity_error
2	RW	ABORT_ON_DL_RETURN_P0_ERROR: abort_on_DL_return_P0_error
3	RW	ABORT_ON_DL_RETURN_WDATA_PARITY_ERROR: abort_on_DL_return_wdata_parity_error
4	RW	WATCHDOG_ENABLE: watchdog_enable
5:6	RW	SCOM_HANG_LIMIT: 0b11: 256, 0b10:512, 0b01:768, 0b00:1023
7	RW	FORCE_ALL_RINGS: set to logic 1 if all rings should be enable independent of ring address
8	RW	FSM_SELFRESET_ON_STATEVEC_PARITYERROR_ENABLE: fsm_selfreset_on_statevec_parityerror_enable
9:11	RW	RESERVED_PSCOM_MODE_LT: reserved

Register Name	<i>PSCOMLE Error Register</i>
Mnemonic	EXP.TP.ECO_DOM.EPS.PSC.PSCOM_STATUS_ERROR_REG
Address	0000000010010001 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	ACCUMULATED_PCB_WDATA_PARITY_ERROR: Accumulated_PCB_wdata_parity_error
1	RWX	ACCUMULATED_PCB_ADDRESS_PARITY_ERROR: Accumulated_PCB_address_parity_error
2	RWX	ACCUMULATED_DL_RETURN_WDATA_PARITY_ERROR: Accumulated_DL_return_wdata_parity_error
3	RWX	ACCUMULATED_DL_RETURN_P0_ERROR: Accumulated_DL_return_P0_error
4	RWX	ACCUMULATED_UL_RDATA_PARITY_ERROR: Accumulated_UL_rdata_parity_error



Bits	PCB	Field Mnemonic: Description
5	RWX	ACCUMULATED_UL_P0_ERROR: Accumulated_UL_P0_error
6	RWX	ACCUMULATED_PARITY_ERROR_ON_INTERFACE_MACHINE: Accumulated_parity_error_on_interface_machine
7	RWX	ACCUMULATED_PARITY_ERROR_ON_P2S_MACHINE: Accumulated_parity_error_on_p2s_machine
8	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Accumulated_timeout_while_waiting_for_ULCCH
9	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Accumulated_timeout_while_waiting_for_DLDCH_return
10	RWX	ACCUMULATED_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Accumulated_timeout_while_waiting_for_ULDCH
11	RWX	ACCUMULATED_PSCOM_PARALLEL_WRITE_NVLD: Accumulated_pscom_parallel_write_nvld
12	RWX	ACCUMULATED_PSCOM_PARALLEL_READ_NVLD: Accumulated_pscom_parallel_read_nvld
13	RWX	ACCUMULATED_PSCOM_PARALLEL_ADDR_INVALID: Accumulated_pscom_parallel_addr_invalid
14	RWX	ACCUMULATED_PCB_COMMAND_PARITY_ERROR: Accumulated_PCB_command_parity_error
15	RWX	ACCUMULATED_GENERAL_TIMEOUT: Accumulated_General_timeout
16	RWX	ACCUMULATED_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Accumulated_satellite_acknowledge_access_violation
17	RWX	ACCUMULATED_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Accumulated_satellite_acknowledge_invalid_register
18	RWX	TRAPPED_PCB_WDATA_PARITY_ERROR: Trapped_PCB_wdata_parity_error
19	RWX	TRAPPED_PCB_ADDRESS_PARITY_ERROR: Trapped_PCB_address_parity_error
20	RWX	TRAPPED_DL_RETURN_WDATA_PARITY_ERROR: Trapped_DL_return_wdata_parity_error
21	RWX	TRAPPED_DL_RETURN_P0_ERROR: Trapped_DL_return_P0_error
22	RWX	TRAPPED_UL_RDATA_PARITY_ERROR: Trapped_UL_rdata_parity_error
23	RWX	TRAPPED_UL_P0_ERROR: Trapped_UL_P0_error
24	RWX	TRAPPED_PARITY_ERROR_ON_INTERFACE_MACHINE: Trapped_parity_error_on_interface_machine
25	RWX	TRAPPED_PARITY_ERROR_ON_P2S_MACHINE: Trapped_parity_error_on_p2s_machine
26	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_ULCCH: Trapped_timeout_while_waiting_for_ULCCH
27	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: Trapped_timeout_while_waiting_for_DLDCH_return
28	RWX	TRAPPED_TIMEOUT_WHILE_WAITING_FOR_ULDCH: Trapped_timeout_while_waiting_for_ULDCH
29	RWX	TRAPPED_PSCOM_PARALLEL_WRITE_NVLD: Trapped_pscom_parallel_write_nvld
30	RWX	TRAPPED_PSCOM_PARALLEL_READ_NVLD: Trapped_pscom_parallel_read_nvld
31	RWX	TRAPPED_PSCOM_PARALLEL_ADDR_INVALID: Trapped_pscom_parallel_addr_invalid
32	RWX	TRAPPED_PCB_COMMAND_PARITY_ERROR: Trapped_PCB_command_parity_error
33	RWX	TRAPPED_GENERAL_TIMEOUT: Trapped_General_timeout
34	RWX	TRAPPED_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: Trapped_satellite_acknowledge_access_violation
35	RWX	TRAPPED_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: Trapped_satellite_acknowledge_invalid_register

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Register Name	<i>PSCOMLE Error Mask Register</i>
Mnemonic	EXP.TP.ECO_DOM.EPS.PSC.PSCOM_ERROR_MASK
Address	0000000010010002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	MASK_PCB_WDATA_PARITY_ERROR: mask_PCB_wdata_parity_error
1	RW	MASK_PCB_ADDRESS_PARITY_ERROR: mask_PCB_address_parity_error
2	RW	MASK_DL_RETURN_WDATA_PARITY_ERROR: mask_DL_return_wdata_parity_error
3	RW	MASK_DL_RETURN_P0_ERROR: mask_DL_return_P0_error
4	RW	MASK_UL_RDATA_PARITY_ERROR: mask_UL_rdata_parity_error
5	RW	MASK_UL_P0_ERROR: mask_UL_P0_error
6	RW	MASK_PARITY_ERROR_ON_INTERFACE_MACHINE: mask_parity_error_on_interface_machine
7	RW	MASK_PARITY_ERROR_ON_P2S_MACHINE: mask_parity_error_on_p2s_machine
8	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_ULCCH: mask_timeout_while_waiting_for_ULCCH
9	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_DLDCH_RETURN: mask_timeout_while_waiting_for_DLDCH_return
10	RW	MASK_TIMEOUT_WHILE_WAITING_FOR_ULDCH: mask_timeout_while_waiting_for_ULDCH
11	RW	MASK_PSCOM_PARALLEL_WRITE_NVLD: mask_pscom_parallel_write_nvld
12	RW	MASK_PSCOM_PARALLEL_READ_NVLD: mask_pscom_parallel_read_nvld
13	RW	MASK_PSCOM_PARALLEL_ADDR_INVALID: mask_pscom_parallel_addr_invalid
14	RW	MASK_PCB_COMMAND_PARITY_ERROR: mask_PCB_command_parity_error
15	RW	MASK_GENERAL_TIMEOUT: mask_general_timeout
16	RW	MASK_SATELLITE_ACKNOWLEDGE_ACCESS_VIOLATION: mask_satellite_acknowledge_access_violation
17	RW	MASK_SATELLITE_ACKNOWLEDGE_INVALID_REGISTER: mask_satellite_acknowledge_invalid_register

Register Name	<i>PSCOMLE Address Trap Register</i>
Mnemonic	EXP.TP.ECO_DOM.EPS.PSC.ADDR_TRAP_REG
Address	0000000010010003 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:15	ROX	PCB_ADDRESS_OF_LAST_TRANSACTION_WITH_ERROR: PCB_address_of_last_transaction_with_error
16	ROX	PCB_READ_NOTWRITE_OF_LAST_TRANSACTION_WITH_ERROR: PCB_read_notwrite_of_last_transaction_with_error
17	ROX	RESERVED_ADDR_LAST_TRAP_LT: reserved_0
18:30	ROX	SERIAL2PARALLEL_STATE_MACHINE_AT_TIME_OF_ERROR: Serial2Parallel_state_machine_at_time_of_error



Bits	PCB	Field Mnemonic: Description
31	ROX	SATELLITE_ACKNOWLEDGE_BIT_RETURN_PARITY: Satellite acknowledge bit: set to 1 if no parity error detected of Sat.No and Ack-bits
32	ROX	SATELLITE_ACKNOWLEDGE_BIT_WRITE_PARITY_ERROR: set if write parity error detected by satellite
33	ROX	SATELLITE_ACKNOWLEDGE_BIT_ACCESS_VIOLATION: set if invalid read or write access detected by satellite
34	ROX	SATELLITE_ACKNOWLEDGE_BIT_INVALID_REGISTER: set if invalid register address detected by satellite

Register Name	<i>Debug Status Register</i>
Mnemonic	EXP.TP.ECO_DOM.EPS.PSC.DEBUG_STATUS_REG
Address	0000000010010004 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	LOCAL_TRACE_RUN_IN: local trace run
1:2	RWX	TRACE_STATE_LAT: trace state latch
3	RWX	TRACE_FREEZE: trace freeze
4:5	RWX	COND3_STATE_LT: condition 3 state latch
6:7	RWX	COND5_STATE_LT: condition 5 state latch
8	RWX	HISTORY_CONDITION0_LT: condition event history for condition0_lt
9	RWX	HISTORY_CONDITION1_LT: condition event history for condition1_lt
10	RWX	HISTORY_COND2_3_EVENT: condition event history for cond2_3_event
11	RWX	HISTORY_COND2_TIMEOUT: condition event history for cond2_timeout
12	RWX	HISTORY_COND4_5_EVENT: condition event history for cond4_5_event
13	RWX	HISTORY_COND4_TIMEOUT: condition event history for cond4_timeout
14:15	RWX	RESERVED_TCDBG_STATUS_LT: reserved, set to zero

Register Name	<i>PSCOMLE Modewrite Protect Enable Register</i>
Mnemonic	EXP.TP.ECO_DOM.EPS.PSC.PSCOM_WRITE_PROTECT_REG
Address	0000000010010005 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	ENABLE_SERIAL_RING_WRITE_PROTECT: enable_serial_ring_write_protect
1	RW	RESERVED_WRITE_PROTECT: enable_serial_ring_write_protect

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Register Name	<i>Atomic Lock Register</i>
Mnemonic	EXP.TP.ECO_DOM.EPS.PSC.ATOMIC_LOCK_REG
Address	00000000100103FF (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	ATOMIC_LOCK_ENABLE: Enable atomic lock
1:4	ROX	ATOMIC_ID: Atomic ID

Register Name	<i>Trace Array High Data Register</i>
Mnemonic	EXP.TP.ECO_DOM.TRAECO.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG
Address	0000000010010400 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63

Register Name	<i>Trace Array Low Data Register</i>
Mnemonic	EXP.TP.ECO_DOM.TRAECO.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG
Address	0000000010010401 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95
32:41	ROX	TRACE_ADDRESS: Trace Address
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank
51	ROX	TRACE_LAST_BANK_VALID: Trace Last Bank Valid
52	ROX	TRACE_WRITE_ON_RUN: Trace Write-On-Run indicator
53	ROX	TRACE_RUNNING: Trace Run indicator
54:63	ROX	TRACE_HOLD_ADDRESS: Trace Hold Address (pointing to last entry)

Register Name	<i>Debug Macro Configuration Register 0 For Config Component</i>
Mnemonic	EXP.TP.ECO_DOM.EPS.DBG.DBG_MODE_REG
Address	00000000100107C0 (SCOM)
Attributes	
Description	



Bits	SCOM	Field Mnemonic: Description
0:2	RW	GLB_BRCST_MODE: global_broadcast_mode (0 to 2): 100: dbg_trace_run & dbg_trace_freeze 101: pc_tcdbg_trace_run_fncl & dbg_trace_freeze 110: dbg_triggers_out(0 to 1) 111: pc_tcdbg_triggers(0 to 1) (from core) glb_brcst_mode
3:4	RW	TRACE_SEL_MODE: Select source for trace_run and bank 01: core trace run & bank 10: tp broadcast run & 0 11: tc_dbg_inter_brcst latched trace_sel_mode
5:6	RW	TRIG_SEL_MODE: Select source for tcdbg_trigger(0) 01: global broadcast 11: pc_tcdbg_trigger (from core) trig_sel_mode
7	RW	STOP_ON_XSTOP_SELECTION: enable trace stop on checkstop stop_on_xstop_selection
8	RW	STOP_ON_RECOV_ERR_SELECTION: enable trace stop on recoverable error stop_on_recov_err_selection
9	RW	STOP_ON_SPATTN_SELECTION: enable trace stop on special attention stop_on_spattn_selection
10	RW	FREEZE_SEL_MODE: select freeze source: 0: local debug freeze 1: via broadcast: tp_tcdbg_glb_brcst(1) freeze_sel_mode
11:15	RO	constant=0b00000
16:31	ROX	dbg_status dbg_status
32:63	RO	constant=0b00000000000000000000000000000000

Register Name	<i>Debug Macro Configuration Register 1 For Front End 1 Component</i>
Mnemonic	EXP.TP.ECO_DOM.EPS.DBG.DBG_INST1_COND_REG_1
Address	00000000100107C1 (SCOM)
Attributes	
Description	

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Bits	SCOM	Field Mnemonic: Description
0:6	RW	INST1_COND1_SEL_A: Multiplexer for cond1_trig_in(0) 000 select constant 0 001 select constant 1 -- CONDITION FEEDBACK -- 002 select inst1_dbg_cond1 003 select inst1_dbg_cond2 004 select inst1_dbg_cond3 005 select inst1_dbg_cond2timeout 006 select inst2_dbg_cond1 007 select inst2_dbg_cond2 008 select inst2_dbg_cond3 009 select inst2_dbg_cond2timeout 010 select inst3_dbg_cond1 - unused, tied down 011 select inst3_dbg_cond2 - unused, tied down 012 select inst3_dbg_cond3 - unused, tied down 013 select inst3_dbg_cond2timeout - unused, tied down 014 select inst4_dbg_cond1 - unused, tied down 015 select inst4_dbg_cond2 - unused, tied down 016 select inst4_dbg_cond3 - unused, tied down 017 select inst4_dbg_cond2timeout - unused, tied down 018 select inst1_dbg_trig_sp 019 select inst2_dbg_trig_sp 020 select inst3_dbg_trig_sp - unused, tied down 021 select inst4_dbg_trig_sp - unused, tied down 022 select tctrc_tcdbg_trigger_a(0) 023 select tctrc_tcdbg_trigger_b(0) 024 select tctrc_tcdbg_trigger_a(0) and tctrc_tcdbg_trigger_b(0) 025 select tctrc_tcdbg_trigger_a(1) 026 select tctrc_tcdbg_trigger_b(1) 027 select tctrc_tcdbg_trigger_a(1) and tctrc_tcdbg_trigger_b(1) 028 select tctrc_tcdbg_trigger_a(2) 029 select tctrc_tcdbg_trigger_b(2) 030 select tctrc_tcdbg_trigger_a(2) and tctrc_tcdbg_trigger_b(2) 031 select tctrc_tcdbg_trigger_a(3) 032 select tctrc_tcdbg_trigger_b(3) 033 select tctrc_tcdbg_trigger_a(3) and tctrc_tcdbg_trigger_b(3) 034 select tctrc_tcdbg_trigger_a(4) 035 select tctrc_tcdbg_trigger_b(4) 036 select tctrc_tcdbg_trigger_a(4) and tctrc_tcdbg_trigger_b(4) 037 select tctrc_tcdbg_trigger_a(5) 038 select tctrc_tcdbg_trigger_b(5) 039 select tctrc_tcdbg_trigger_a(5) and tctrc_tcdbg_trigger_b(5) 040 select tctrc_tcdbg_trigger_a(6) 041 select tctrc_tcdbg_trigger_b(6) 042 select tctrc_tcdbg_trigger_a(6) and tctrc_tcdbg_trigger_b(6) 043 select tctrc_tcdbg_trigger_a(7) 044 select tctrc_tcdbg_trigger_b(7) 045 select tctrc_tcdbg_trigger_a(7) and tctrc_tcdbg_trigger_b(7) 046 select tctrc_tcdbg_trigger_a(8) 047 select tctrc_tcdbg_trigger_b(8) 048 select tctrc_tcdbg_trigger_a(8) and tctrc_tcdbg_trigger_b(8) 049 select tctrc_tcdbg_trigger_a(9) 050 select tctrc_tcdbg_trigger_b(9) 051 select tctrc_tcdbg_trigger_a(9) and tctrc_tcdbg_trigger_b(9) 052 select xstop_err 053 select recov_err 054 select spattn 055 select fir_dbg_local_xstop_err 056 select tc_dbg_inter_brcst(0) 057 select tc_dbg_inter_brcst(1)

Bits	SCOM	Field Mnemonic: Description
		-- LOGIC (UNIT) TRIGGERS -- EP: 0:3 L3C0, 4:7 L3C1, 8:9 GX, 10 TP (hang), 11 spare, 12:13 MCA, 14:15 spare ES: 0:4 L4C, 5:6 L4F, 7:8 TPTOD, 9 TP (hang), 10:15 spare 102 select logic_trigger_in(0) 103 select logic_trigger_in(1) 104 select logic_trigger_in(2) 105 select logic_trigger_in(3) 106 select logic_trigger_in(4) 107 select logic_trigger_in(5) 108 select logic_trigger_in(6) 109 select logic_trigger_in(7) 110 select logic_trigger_in(8) 111 select logic_trigger_in(9) 112 select logic_trigger_in(10) 113 select logic_trigger_in(11) 114 select logic_trigger_in(12) 115 select logic_trigger_in(13) 116 select logic_trigger_in(14) 117 select logic_trigger_in(15) -- CORE TRIGGERS (EP chip only) -- Note: set core_slave_mode to honor ec[0:5]_tc_trace_run 118 select core trigger 0: any rising edge of ec[0:5]_tc_trace_run(0) 119 select core trigger 1: any rising edge of ec[0:5]_tc_trace_run(1) 120 select core trigger 2: any falling edge of ec[0:5]_tc_trace_run(0) 121 select core trigger 3: any falling edge of ec[0:5]_tc_trace_run(1) -- BROADCAST / ERRORS 122 select glb_trc_bdcst_rcv (received global broadcast) 123 select edge detected fir_dbg_xstop_err 124 select edge detected fir_dbg_recov_err 125 select edge detected fir_dbg_spatn 126 ... 127 select constant 0 (unused)
7:13	RW	INST1_COND1_SEL_B: Multiplexer for cond1_trig_in(1) Selection as cond1_trig_in(0)
14:20	RW	INST1_COND2_SEL_A: Multiplexer for cond2_trig_in(0) Selection as cond1_trig_in(0)
21:27	RW	INST1_COND2_SEL_B: Multiplexer for cond2_trig_in(1) Selection as cond1_trig_in(0)
28	RW	INST1_C1_INAROW_MODE: front end instance 1 c1_inarow_mode
29	RW	INST1_AND_TRIGGER_MODE1: front end instance 1 and trigger mode condition1
30	RW	INST1_NOT_TRIGGER_MODE1: front end instance 1 inverted trigger mode condition1
31	RW	INST1_EDGE_TRIGGER_MODE1: front end instance 1 edge trigger mode condition1
32:34	RW	INST1_X_COUPLE_SELECT1: cond1_mode_lt(4..6) = inst1_x_couple_select UNUSED
35	RW	INST1_C2_INAROW_MODE: front end instance 1 Counter 2 in-a-rwo mode
36	RW	INST1_AND_TRIGGER_MODE2: front end instance 1 and trigger mode2
37	RW	INST1_NOT_TRIGGER_MODE2: front end instance 1 inverted (not) trigger
38	RW	INST1_EDGE_TRIGGER_MODE2: front end instance 1 edge trigger
39:41	RW	INST1_X_COUPLE_SELECT2: front end instance 1 cross couple selection UNUSED
42	RW	INST1_COND3_ENABLE_RESET: front end instance 1 condition3 enable
43	RW	INST1_EXACT_TO_MODE: front end instance 1 exact timeout mode
44	RW	INST1_RESET_C2TIMER_ON_C1: front end instance 1 reset condition2 timer on condition1
45	RW	INST1_RESET_C3_ON_C0: front end instance 1 reset condition3 on condition0



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Bits	SCOM	Field Mnemonic: Description
46	RW	INST1_SLOW_TO_MODE: front end instance 1 slow timeout mode
47	RW	INST1_EXACT_RESET_C3_ON_TO: front end instance 1 exact reset condition3 on timeout
48:51	RW	INST1_C1_COUNT_LT: inst1 condition1 counter compare value
52:55	RW	INST1_C2_COUNT_LT: inst1 condition2 counter compare value
56:58	RW	INST1_RESET_C3_SELECT: front end instance 1: reset condition3 for reset_c3_on_c0 0b100: dbg_cross_couple_triggers(4) 0b101: dbg_cross_couple_triggers(12) 0b110: dbg_cross_couple_triggers(20) 0b111: dbg_cross_couple_triggers(28)
59:63	RW	INST1_CROSS_COUPLE_SELECT_1_A: Cross coupling: 00000 - selects inst1_cond1_trig_a 00001 - selects inst1_cond1_trig_b 00010 - selects inst1_cond2_trig_a 00011 - selects inst1_cond2_trig_b 00100 - selects inst1_condition1 00101 - selects inst1_condition2 00110 - selects inst1_condition3 00111 - selects inst1_cond2_timeout 01000 - selects inst2_cond1_trig_a 01001 - selects inst2_cond1_trig_b 01010 - selects inst2_cond2_trig_a 01011 - selects inst2_cond2_trig_b 01100 - selects inst2_condition1 01101 - selects inst2_condition2 01110 - selects inst2_condition3 01111 - selects inst2_cond2_timeout 10000 - selects inst3_cond1_trig_a 10001 - selects inst3_cond1_trig_b 10010 - selects inst3_cond2_trig_a 10011 - selects inst3_cond2_trig_b 10100 - selects inst3_condition1 10101 - selects inst3_condition2 10110 - selects inst3_condition3 10111 - selects inst3_cond2_timeout 11000 - selects inst4_cond1_trig_a 11001 - selects inst4_cond1_trig_b 11010 - selects inst4_cond2_trig_a 11011 - selects inst4_cond2_trig_b 11100 - selects inst4_condition1 11101 - selects inst4_condition2 11110 - selects inst4_condition3 11111 - selects inst4_cond2_timeout

Register Name	<i>Debug Macro Configuration Register 2 For Front End 1 Component</i>	
Mnemonic	EXP.TP.ECO_DOM.EPS.DBG.DBG_INST1_COND_REG_2	
Address	00000000100107C2 (SCOM)	
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0:4	RW	INST1_CROSS_COUPLE_SELECT_1_B: inst1_cross_couple_select_1_b
5:9	RW	INST1_CROSS_COUPLE_SELECT_2_A: inst1_cross_couple_select_2_a



Bits	SCOM	Field Mnemonic: Description
10:14	RW	INST1_CROSS_COUPLE_SELECT_2_B: inst1_cross_couple_select_2_b
15:38	RW	INST1_SP_COUNT_LT: compare value for special counter sp_cnt_lt in debug component 1
39:62	RW	INST1_TO_CMP_LT_VALUE: timeout counter to_cmp compare value for dbg_cond_comp_1
63	RW	INST1_FORCE_TEST_MODE: force test mode to indicate to compare without actual compare

Register Name	<i>Debug Macro Configuration Register 3 For Front End 2 Component</i>
Mnemonic	EXP.TP.ECO_DOM.EPS.DBG.DBG_INST2_COND_REG_1
Address	00000000100107C3 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:6	RW	INST2_COND1_SEL_A: like inst1_cond1_sel_a
7:13	RW	INST2_COND1_SEL_B: like inst1_cond1_sel_b
14:20	RW	INST2_COND2_SEL_A: like inst1_cond2_sel_a
21:27	RW	INST2_COND2_SEL_B: like inst1_cond2_sel_b
28	RW	INST2_C1_INAROW_MODE: cond1_mode_lt(0) = c1_inarow_mode
29	RW	INST2_AND_TRIGGER_MODE1: cond1_mode_lt(1) = inst2_and_trigger_mode1
30	RW	INST2_NOT_TRIGGER_MODE1: cond1_mode_lt(2) = inst2_not_trigger_mode1
31	RW	INST2_EDGE_TRIGGER_MODE1: cond1_mode_lt(3) = inst2_edge_trigger_mode1
32:34	RW	INST2_X_COUPLE_SELECT1: cond1_mode_lt(4..6) = inst2_x_couple_select UNUSED
35	RW	INST2_C2_INAROW_MODE: front end instance 2 Counter 2 in-a-rwo mode
36	RW	INST2_AND_TRIGGER_MODE2: front end instance 2 and trigger mode2
37	RW	INST2_NOT_TRIGGER_MODE2: front end instance 2 inverted (not) trigger
38	RW	INST2_EDGE_TRIGGER_MODE2: front end instance 2 edge trigger
39:41	RW	INST2_X_COUPLE_SELECT2: front end instance 2 cross couple selection UNUSED
42	RW	INST2_COND3_ENABLE_RESET: front end instance 2 condition3 enable
43	RW	INST2_EXACT_TO_MODE: front end instance 2 exact timeout mode
44	RW	INST2_RESET_C2TIMER_ON_C1: front end instance 2 reset condition2 timer on condition1
45	RW	INST2_RESET_C3_ON_C0: front end instance 2 reset condition3 on condition0
46	RW	INST2_SLOW_TO_MODE: front end instance 2 slow timeout mode
47	RW	INST2_EXACT_RESET_C3_ON_TO: front end instance 2 exact reset condition3 on timeout
48:51	RW	INST2_C1_COUNT_LT: Like inst1 condition1 counter compare value
52:55	RW	INST2_C2_COUNT_LT: Like inst1 condition2 counter compare value
56:58	RW	INST2_RESET_C3_SELECT: front end instance 1: reset condition3 for reset_c3_on_c0 0b100: dbg_cross_couple_triggers(4) 0b101: dbg_cross_couple_triggers(12) 0b110: dbg_cross_couple_triggers(20) 0b111: dbg_cross_couple_triggers(28)
59:63	RW	INST2_CROSS_COUPLE_SELECT_1_A: like inst1_crous_couple_select_1_a

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Register Name	<i>Debug Macro Configuration Register 4 For Front End 2 Component</i>
Mnemonic	EXP.TP.ECO_DOM.EPS.DBG.DBG_INST2_COND_REG_2
Address	00000000100107C4 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	INST2_CROSS_COUPLE_SELECT_1_B: Like inst1_cross_couple_select_1_b
5:9	RW	INST2_CROSS_COUPLE_SELECT_2_A: Like inst1_cross_couple_select_2_a
10:14	RW	INST2_CROSS_COUPLE_SELECT_2_B: Like inst1_cross_couple_select_2_b
15:38	RW	INST2_SP_COUNT_LT: compare value for special counter sp_cnt_lt in debug component 1
39:62	RW	INST2_TO_CMP_LT_VALUE: timeout counter to_cmp compare value for dbg_cond_comp_1
63	RW	INST2_FORCE_TEST_MODE: force test mode to indicate to compare without actual compare

Register Name	<i>Debug Macro Configuration Register 10 For Debug Backed Component</i>
Mnemonic	EXP.TP.ECO_DOM.EPS.DBG.DBG_TRACE_REG_0
Address	00000000100107C9 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	INST1_COND3_ENABLE: Enable of instance 1 condition 3
1	RW	INST2_COND3_ENABLE: Enable of instance 2 condition 3
2	RW	INST3_COND3_ENABLE: UNUSED
3	RW	INST4_COND3_ENABLE: UNUSED
4	RW	INST1_SLOW_LFSR_MODE: Enable slow lfsr mode of front end instance 1
5	RW	INST2_SLOW_LFSR_MODE: Enable slow lfsr mode of front end instance 2
6	RW	INST3_SLOW_LFSR_MODE: UNUSED
7	RW	INST4_SLOW_LFSR_MODE: UNUSED
8:9	RW	INST1_CONDITION1_TRIG_SEL: Select inst1 condition1 for output (external) triggers 00 = do nothing 01 = trigger_out(0) 10 = trigger_out(1) 11 = trigger_out(2)
10:11	RW	INST1_CONDITION2_TRIG_SEL: Select inst1 condition2 for output (external) triggers 00 = do nothing 01 = trigger_out(0) 10 = trigger_out(1) 11 = trigger_out(2)
12:13	RW	INST1_C2_TIMEOUT_TRIG_SEL: Select inst1 c2 time-out counter for output (external) triggers 00 = do nothing 01 = trigger_out(0) 10 = trigger_out(1) 11 = trigger_out(2)

Bits	SCOM	Field Mnemonic: Description
14:15	RW	INST2_CONDITION1_TRIG_SEL: Select inst2 condition1 for output (external) triggers 00 = do nothing 01 = trigger_out(0) 10 = trigger_out(1) 11 = trigger_out(2)
16:17	RW	INST2_CONDITION2_TRIG_SEL: Select inst2 condition2 trigger for output (external) triggers 00 = do nothing 01 = trigger_out(0) 10 = trigger_out(1) 11 = trigger_out(2)
18:19	RW	INST2_C2_TIMEOUT_TRIG_SEL: Select inst2 c2 time-out counter for output (external) triggers 00 = do nothing 01 = trigger_out(0) 10 = trigger_out(1) 11 = trigger_out(2)
20:31	RO	constant=0b00000000000000
32	RW	EXT_TRIG_ON_STOP: enable trigger on stop
33	RW	EXT_TRIG_ON_FREEZE: enable trigger on freeze
34:38	RW	CORE_RAS0_TRIG_SEL:
39:43	RW	CORE_RAS1_TRIG_SEL:
44:45	RW	PC_TP_TRIG_SEL:
46:49	RW	DBG_ARM_SEL:
50:53	RW	TRIG0_LEVEL_SEL: Select additional conditions for output (external) trigger signal trigger_out(0) Note: some are N/A for zG+ (inst3/4 conditions are tied to zero) 0001 = inst1_cond3_state_int(1) 0010 = inst1_cond3_state_int(0) 0011 = inst2_cond3_state_int(1) 0100 = inst2_cond3_state_int(0) 0101 = inst3_cond3_state_int(1) 0110 = inst3_cond3_state_int(0) 0111 = inst4_cond3_state_int(1) 1000 = inst4_cond3_state_int(0) 1001 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) 1010 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) 1011 = inst3_cond3_state_int(1) or inst4_cond3_state_int(1) 1100 = inst3_cond3_state_int(1) and inst4_cond3_state_int(1) 1101 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) 1110 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) and inst3_cond3_state_int(1) 1111 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) or inst4_cond3_state_int(1)

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Bits	SCOM	Field Mnemonic: Description
54:57	RW	TRIG1_LEVEL_SEL: Select additional conditions for output (external) trigger signal trigger_out(1) Note: some are N/A for zG+ (inst3/4 conditions are tied to zero) 0001 = inst1_cond3_state_int(1) 0010 = inst1_cond3_state_int(0) 0011 = inst2_cond3_state_int(1) 0100 = inst2_cond3_state_int(0) 0101 = inst3_cond3_state_int(1) 0110 = inst3_cond3_state_int(0) 0111 = inst4_cond3_state_int(1) 1000 = inst4_cond3_state_int(0) 1001 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) 1010 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) 1011 = inst3_cond3_state_int(1) or inst4_cond3_state_int(1) 1100 = inst3_cond3_state_int(1) and inst4_cond3_state_int(1) 1101 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) 1110 = inst1_cond3_state_int(1) and inst2_cond3_state_int(1) and inst3_cond3_state_int(1) 1111 = inst1_cond3_state_int(1) or inst2_cond3_state_int(1) or inst3_cond3_state_int(1) or inst4_cond3_state_int(1)
58:63	RO	constant=0b0000000

Register Name	<i>Debug Macro Configuration Register 11 For Backed Component</i>
Mnemonic	EXP.TP.ECO_DOM.EPS.DBG.DBG_TRACE_REG_1
Address	00000000100107CA (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:1	RW	INST1_CONDITION1_ACTION_DO: Inst1 action selection , condition1: 00 = nothing, 01 = start, 10 = stop, 11 = run-N: start now, stop after n cycles
2:3	RW	INST1_CONDITION2_ACTION_DO: Inst1 action selection , condition2: 00 = nothing, 01 = start, 10 = stop, 11 = run-N: start now, stop after n cycles
4:5	RW	INST1_C2_TIMEOUT_ACTION_DO: Inst1 action selection , c2_timeout: 00 = nothing, 01 = start, 10 = stop, 11 = run-N: start now, stop after n cycles
6:7	RW	INST2_CONDITION1_ACTION_DO: inst2 action selection , condition1: 00 = nothing, 01 = start, 10 = stop, 11 = run-N: start now, stop after n cycles
8:9	RW	INST2_CONDITION2_ACTION_DO: Inst2 action selection , condition2: 00 = nothing, 01 = start, 10 = stop, 11 = run-N: start now, stop after n cycles
10:11	RW	INST2_C2_TIMEOUT_ACTION_DO: Inst2 action selection , c2_timeout: 00 = nothing, 01 = start, 10 = stop, 11 = run-N: start now, stop after n cycles
12:23	RO	constant=0b000000000000
24	RW	INST1_CONDITION1_ACTION_WAITN: for wait-N
25	RW	INST1_CONDITION2_ACTION_WAITN: for wait-N
26	RW	INST1_C2_TIMEOUT_ACTION_WAITN: for wait-N



Bits	SCOM	Field Mnemonic: Description
27	RW	INST2_CONDITION1_ACTION_WAITN: for wait-N
28	RW	INST2_CONDITION2_ACTION_WAITN: for wait-N
29	RW	INST2_C2_TIMEOUT_ACTION_WAITN: for wait-N
30:35	RO	constant=0b000000
36	RW	INST1_CONDITION1_ACTION_BANK: trace bank switch (inst1, condition1)
37	RW	INST1_CONDITION2_ACTION_BANK: trace bank switch (inst1, condition2)
38	RW	INST1_C2_TIMEOUT_ACTION_BANK: trace bank switch (inst1, c2_timeout)
39	RW	INST2_CONDITION1_ACTION_BANK: trace bank switch (inst2, condition1)
40	RW	INST2_CONDITION2_ACTION_BANK: trace bank switch (inst2, condition2)
41	RW	INST2_C2_TIMEOUT_ACTION_BANK: trace bank switch (inst2, c2_timeout)
42:47	RO	constant=0b000000
48:50	RW	INST1_CHECKSTOP_MODE_LT: Select additional condition with fir_error_lt for dbg_fir_xstop_on_trig output: 000 = inst1_condition1_lt 001 = inst1_condition2_lt 010 = inst1_condition3_lt 011 = inst1_cond2_timeout_lt 1XX = disable checkstop_mode
51	RW	INST1_CHECKSTOP_MODE_SELECTOR: enable_fir_trig_xstop: enable checkstop on debug trigger: 0 = disable checkstop on debug trigger 1 = enable checkstop on debug trigger
52:54	RW	INST2_CHECKSTOP_MODE_LT: Select additional condition with fir_error_lt for dbg_fir_xstop_on_trig output: 000 = inst2_condition1_lt 001 = inst2_condition2_lt 010 = inst2_condition3_lt 011 = inst2_cond2_timeout_lt 1XX = disable checkstop_mode
55	RW	INST2_CHECKSTOP_MODE_SELECTOR: enable_fir_error_xstop: enable checkstop on fir error: 0 = disable checkstop on fir error 1 = enable checkstop on fir error
56:63	RO	constant=0b00000000

Register Name	<i>Debug Macro Configuration Register 12 For Backed Component</i>
Mnemonic	EXP.TP.ECO_DOM.EPS.DBG.DBG_TRACE_MODE_REG_2
Address	00000000100107CB (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	RW	RUNN_COUNT_COMPARE_VALUE: Compare value for the run-N counter used in trace modes run-N and wait-N
16	RW	IMM_FREEZE_MODE: immediate freeze mode
17	RW	STOP_ON_ERR: stop and freeze on xstop
18	RW	BANK_ON_RUNN_MATCH: bank switch on runn match



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Bits	SCOM	Field Mnemonic: Description
19	RW	FORCE_TEST_MODE: force run-N condition to be true
20	RW	ACCUM_HIST_MODE: accumulate history mode, do not clear history mode when trace_run active
21	RW	FRZ_COUNT_ON_FRZ: freeze condition counters on trace freeze

Register Name	L3 FIR Register
Mnemonic	EXP.L3.L3_MISC.L3CERRS.FIR_REG
Address	0000000010010800 (SCOM) 0000000010010801 (SCOM1) 0000000010010802 (SCOM2)
Attributes	
Description	L3 FIR Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PB_CMD_ERR: processor bus Command Error detected by PBIEX
1	RWX	WOX_AND	WOX_OR	PB_DATA_ERR: processor bus Command Error detected by PBIEX
2	RWX	WOX_AND	WOX_OR	SPARE_FIR0: Spare Fir
3	RWX	WOX_AND	WOX_OR	L3_DRAM_POS_WL_FAIL: This error indicates at least 1 CE and 1 UE have occurred within 1 fabric data hang pulse interval. This is an indication that a word line fail may be occurring.
4	RWX	WOX_AND	WOX_OR	L3_CAC_RD_CE_DET_NOT_LINDEL_REQ: CE detected on L3 Cache read that is not a line delete request
5	RWX	WOX_AND	WOX_OR	L3_CAC_RD_UE_DET: UE detected on L3 Cache read
6	RWX	WOX_AND	WOX_OR	L3_CAC_RD_SUE_DET: SUE detected on L3 Cache read
7	RWX	WOX_AND	WOX_OR	L3_CAC_WR_DATA_CE_FROM_PB: CE detected on processor bus write data for Prefetch, LCO or Cache Inject
8	RWX	WOX_AND	WOX_OR	L3_CAC_WR_DATA_UE_FROM_PB: UE detected on processor bus write data for Prefetch, LCO or Cache Inject
9	RWX	WOX_AND	WOX_OR	L3_CAC_WR_DATA_SUE_FROM_PB: SUE detected on processor bus write data for Prefetch, LCO or Cache Inject
10	RWX	WOX_AND	WOX_OR	L3_CAC_WR_DATA_CE_FROM_L2: CE detected on write data from L2 CPI buffer
11	RWX	WOX_AND	WOX_OR	L3_CAC_WR_DATA_UE_FROM_L2: UE detected on write data from L2 CPI buffer
12	RWX	WOX_AND	WOX_OR	L3_CAC_WR_DATA_SUE_FROM_L2: SUE detected on write data from L2 CPI buffer
13	RWX	WOX_AND	WOX_OR	L3_DIR_RD_CE_DET: Directory CE Occurred
14	RWX	WOX_AND	WOX_OR	L3_DIR_RD_UE_DET: Directory UE Occurred
15	RWX	WOX_AND	WOX_OR	L3_DIR_RD_PHANTOM_ERROR: Directory error occurred but not found during correction sequence
16	RWX	WOX_AND	WOX_OR	L3_CO_SN_CRESP_ADDR_ERR: Received addr_error cresp on Snoop Machine or Castout Operation
17	RWX	WOX_AND	WOX_OR	L3_PF_CRESP_ADDR_ERR: Received addr_error cresp for Prefetch Operation



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
18	RWX	WOX_AND	WOX_OR	L3_ADDR_HANG_DETECTED: Some L3 machine hung waiting for combined response or flink hang
19	RWX	WOX_AND	WOX_OR	L3_FLINK_0_LOAD_ACK_DEAD: I3 prefetch received ack_dead cresp from foreign link 0
20	RWX	WOX_AND	WOX_OR	L3_FLINK_0_STORE_ACK_DEAD: I3 castout or snoop machine received ack_dead cresp from foreign link 0
21	RWX	WOX_AND	WOX_OR	L3_FLINK_1_LOAD_ACK_DEAD: I3 prefetch received ack_dead cresp from foreign link 1
22	RWX	WOX_AND	WOX_OR	L3_FLINK_1_STORE_ACK_DEAD: I3 castout or snoop machine received ack_dead cresp from foreign link 1
23	RWX	WOX_AND	WOX_OR	L3_MACH_HANG_DETECTED: Prefetch or Write Inject machine processor bus data hang check
24	RWX	WOX_AND	WOX_OR	L3_HW_CONTROL_ERR: Hardware Control Error. See Hardware Control Error Read0/1 SCOM Registers for details.
25	RWX	WOX_AND	WOX_OR	L3_SNOOP_SW_ERR_DETECTED: Cache Inhibited operation was hit in the L3 directory. This is usually a software bug.
26	RWX	WOX_AND	WOX_OR	L3_LINE_DEL_CE_DONE: Snoop Machine or Read machine has performed a line delete
27	RWX	WOX_AND	WOX_OR	L3_DRAM_ERROR: Dram Command Collision Error
28	RWX	WOX_AND	WOX_OR	L3_LRU_ERROR: Invalid LRU value, most likely SRAM error
29	RWX	WOX_AND	WOX_OR	L3_ALL_MEMBERS_DELETED_ERROR: All members are either column or line deleted in some CGC class
30	RWX	WOX_AND	WOX_OR	L3_REFRESH_TIMER_ERROR: Refresh timer pulse either wasn't configured to run properly or has stopped
31	RWX	WOX_AND	WOX_OR	L3_HA_CONSUMER_SW_ACCESS_ERR: Consumer writing to dirty address memory block
32	RWX	WOX_AND	WOX_OR	L3_HA_PRODUCER_SW_ACCESS_ERR: Producer consuming dirty address memory block
33	RWX	WOX_AND	WOX_OR	L3_HA_LINE_IN_CONSUMER_CAC_ERR: Line marked as HA found in consumer cache
34	RWX	WOX_AND	WOX_OR	L3_HA_TABLE_IN_PRODUCER_CAC_ERR: Dirty address table found in producer cache
35	RWX	WOX_AND	WOX_OR	L3_HA_LOG_OVERFLOW_ERR: The HA table write pointer to lap the read pointer
36	RWX	WOX_AND	WOX_OR	SCOM_ERR1: SCOM Error Fir 1
37	RWX	WOX_AND	WOX_OR	SCOM_ERR2: SCOM Error Fir 2
38:63	RO	N/A	N/A	constant=0b00000000000000000000000000000000

Register Name	L3 FIR Mask Register
Mnemonic	EXP.L3.L3_MISC.L3CERRS.FIR_MASK_REG
Address	0000000010010803 (SCOM) 0000000010010804 (SCOM1) 0000000010010805 (SCOM2)
Attributes	
Description	L3 FIR Mask Register

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	Reserved field. (Access type is pb_cmd_err_mask)
1	RW	WO_AND	WO_OR	Reserved field. (Access type is pb_data_err_mask)
2	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_spare_error1_mask)
3	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_dram_pos_wl_fail_mask)
4	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_cac_rd_ce_det_not_lindel_req_mask)
5	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_cac_rd_ue_det_mask)
6	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_cac_rd_sue_det_mask)
7	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_cac_wr_data_ce_from_pb_mask)
8	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_cac_wr_data_ue_from_pb_mask)
9	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_cac_wr_data_sue_from_pb_mask)
10	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_cac_wr_data_ce_from_l2_mask)
11	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_cac_wr_data_ue_from_l2_mask)
12	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_cac_wr_data_sue_from_l2_mask)
13	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_dir_rd_ce_det_mask)
14	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_dir_rd_ue_det_mask)
15	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_dir_rd_phantom_error_mask)
16	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_co_sn_cresp_addr_err_mask)
17	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_pf_cresp_addr_err_mask)
18	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_addr_hang_detected_mask)
19	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_flink_0_load_ack_dead_mask)
20	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_flink_0_store_ack_dead_mask)
21	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_flink_1_load_ack_dead_mask)
22	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_flink_1_store_ack_dead_mask)
23	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_mach_hang_detected_mask)
24	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_hw_control_err_mask)
25	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_snoop_sw_err_detected_mask)
26	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_line_del_ce_done_mask)
27	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_dram_error_mask)
28	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_lru_error_mask)
29	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_all_members_deleted_error_mask)
30	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_refresh_timer_error_mask)
31	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_ha_consumer_sw_access_err_mask)
32	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_ha_producer_sw_access_err_mask)
33	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_ha_line_in_consumer_cac_err_mask)
34	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_ha_table_in_producer_cac_err_mask)
35	RW	WO_AND	WO_OR	Reserved field. (Access type is l3_ha_log_overflow_err_mask)
36	RW	WO_AND	WO_OR	Reserved field. (Access type is scom_err_mask1)
37	RW	WO_AND	WO_OR	Reserved field. (Access type is scom_err_mask2)
38:63	RO	N/A	N/A	constant=0b00000000000000000000000000000000

Register Name	<i>L3 FIR Action0 Register</i>
Mnemonic	EXP.L3.L3_MISC.L3CERRS.FIR_ACTION0_REG
Address	0000000010010806 (SCOM)
Attributes	
Description	I3 FIR Action0 Register

Bits	SCOM	Field Mnemonic: Description
0:37	RW	FIR_ACTION0: Action0 select for corresponding bit in FIR (Action0,Action1) = Action Select (0,0) = Checkstop Error (0,1) = Recoverable Error (1,0) = Reserved (1,1) = Local Core Checkstop
38:63	RO	constant=0b000000000000000000000000

Register Name	<i>L3 FIR Action1 Register</i>
Mnemonic	EXP.L3.L3_MISC.L3CERRS.FIR_ACTION1_REG
Address	0000000010010807 (SCOM)
Attributes	
Description	I3 FIR Action1 Register

Bits	SCOM	Field Mnemonic: Description
0:37	RW	FIR_ACTION1: Action1 select for corresponding bit in FIR (Action0,Action1) = Action Select (0,0) = Checkstop Error (0,1) = Recoverable Error (1,0) = Reserved (1,1) = Local Core Checkstop
38:63	RO	constant=0b000000000000000000000000

Register Name	<i>L3 Mode Register 1</i>
Mnemonic	EXP.L3.L3_MISC.L3CERRS.MODE_REG1
Address	000000001001080A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	L3_LCO_ENABLE_CFG: When on, enables lateral cast outs. If set, the user MUST configure group, id, and victim fields in this register! Also, when modifying any of the target IDs or victim bits while the machine is running. You must scom write this bit OFF, and then write it back ON along with the other updates. A leading edge detect of 0 to 1 causes the logic to sample the other bits.
1	RW	L3_LCO_TARGET_GROUP: Set the target group/chip for this chiplet
2:5	RW	L3_LCO_TARGET_ID: Set the target ID for this chiplet



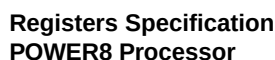
Bits	SCOM	Field Mnemonic: Description
35:63	RO	constant=0b00000000000000000000000000000000 Values: SIZE_4_GB=>0b00000000000000000000 SIZE_8_GB=>0b00000000000000000001 SIZE_16_GB=>0b00000000000000000011 SIZE_32_GB=>0b00000000000000000111 SIZE_64_GB=>0b00000000000000001111 SIZE_128_GB=>0b00000000000000111111 SIZE_256_GB=>0b00000000000011111111 SIZE_512_GB=>0b00000000001111111111 SIZE_1_TB=>0b00000000011111111111 SIZE_2_TB=>0b00000000111111111111 SIZE_4_TB=>0b00000001111111111111 SIZE_8_TB=>0b00000011111111111111 SIZE_16_TB=>0b00000111111111111111 SIZE_32_TB=>0b00001111111111111111 SIZE_64_TB=>0b00011111111111111111 SIZE_128_TB=>0b00111111111111111111 SIZE_256_TB=>0b01111111111111111111 SIZE_512_TB=>0b11111111111111111111

Register Name	L3 eDRAM And Charge Pump Register
Mnemonic	EXP.L3.L3_MISC.L3CERRS.EDRAM_REG
Address	000000001001080C (SCOM)
Attributes	
Description	

[illegible]

Register Name	L3 Error Inject Register
Mnemonic	EXP.L3.L3_MISC.L3CERRS.ERR_INJ_REG
Address	000000001001080D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX_WOR	L3_SINGLE_CAC_ERR_INJ: When on, injects a single error into the cache
1	RW	L3_SOLID_CAC_ERR_INJ: When on, injects a solid error into the cache

[illegible]



Register Name	L3 Refresh Timer Control Register And Init DRAM
Mnemonic	EXP.L3.L3_ARB.L3CACTL.DRAM_REF_REG
Address	000000001001080F (SCOM)
Attributes	
Description	

[illegible]

Register Name	L3 Control Check Read Register 0
Mnemonic	EXP.L3.L3_MISC.L3CERRS.L3_CTL_CHECK_RD0_REG
Address	0000000010010810 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RO	L3SDRTL0_CHECKSTOP_ERR: l3sdrtl0_checkstop_err
1	RO	L3SDRTL1_CHECKSTOP_ERR: l3sdrtl1_checkstop_err
2	RO	L3CORTR_NO_LCO_TGTS_ERR: l3contr_no_lco_tgts_err
3:4	RO	RCMD_TTAG_P_ERR: rcmd_ttag_p_err
5:6	RO	RCMD_ADDR_P_ERR: rcmd_addr_p_err
7:8	RO	CRESP_TTAG_P_ERR: cresp_ttag_p_err

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Bits	SCOM	Field Mnemonic: Description
9:10	RO	CRESP_ATAG_P_ERR: cresp_atag_p_err
11	RO	DATA_RTAG_P_ERR: data_rtag_p_err
12:13	RO	PF_UNSOLICITED_CRESP_ERR: pf_unsolicited_cresp_err
14:15	RO	SN_UNSOLICITED_CRESP_ERR: sn_unsolicited_cresp_err
16:17	RO	CO_UNSOLICITED_CRESP_ERR: co_unsolicited_cresp_err
18	RO	WI_UNSOLICITED_DATA_ERR: wi_unsolicited_data_err
19	RO	PF_UNSOLICITED_DATA_ERR: pf_unsolicited_data_err
20:23	RO	TM_CAM_ERR: tm_cam_err
24	RO	COFSM_ADDR_ERR: cofsm_addr_err
25	RO	SNFSM_ADDR_ERR: snfsm_addr_err
26	RO	L3SDRTL0_CACHE_INHIBIT_ERR: l3sdrtl0_cache_inhibit_err
27	RO	L3SDRTL1_CACHE_INHIBIT_ERR: l3sdrtl1_cache_inhibit_err
28:29	RO	FLINK_0_STORE_ACK_DEAD_ERR: flink_0_store_ack_dead_err
30:31	RO	FLINK_1_STORE_ACK_DEAD_ERR: flink_1_store_ack_dead_err
32	RO	SN_MACHINE_HANG_ERR: sn_machine_hang_err
33	RO	RD_MACHINE_HANG_ERR: rd_machine_hang_err
34	RO	CI_MACHINE_HANG_ERR: ci_machine_hang_err
35	RO	CO_MACHINE_HANG_ERR: co_machine_hang_err
36:63	RO	constant=0b00000000000000000000000000000000

Register Name	<i>L3 LRU Victim Allocation Control Register</i>
Mnemonic	EXP.L3.L3_MISC.L3CERRS.LRU_VIC_ALLOC_REG
Address	0000000010010811 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	L3_COLUMN_ALLOC_LMT_CFG: This register has two different modes. Each bit corresponds to one cgc member. When l3_column_alloc_md_cfg is zero these bits will remove member from LRU alloc only. When l3_column_alloc_md_cfg is one these bits will behave as described in the description for l3_column_alloc_md_cfg=one.
8:9	RW	L3_COLUMN_ALLOC_MD_CFG: When 01, the column alloc lmt bits will cause L2 COs to choose from members whose bits are 1 and LCOs to choose from members whose bits are 0. When 01 the column_alloc_lmt bits will block a member from used. NOTE: members cannot be truly deleted when using the l3_column_alloc_md_cfg=01. When 10, Segregated LPAR Mode Values: NORMAL_MODE=>0b00 SEGREGATED_LCO_MODE=>0b01 SEGREGATED_LPAR_MODE=>0b10



Bits	SCOM	Field Mnemonic: Description
10:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000 Values: NORMAL_MODE=>0b00 SEGREGATED_LCO_MODE=>0b01 SEGREGATED_LPAR_MODE=>0b10

Register Name	Indicates The Period Of The Rtim Pulse From Pervasive
Mnemonic	EXP.L3.L3_MISC.L3CERRS.L3_RTIM_PERIOD_MONITOR
Address	0000000010010812 (SCOM)
Attributes	
Description	

[illegible]

Register Name	L3 Bar2 Register
Mnemonic	EXP.L3.L3_MISC.L3CERRS.BAR2_REG
Address	0000000010010813 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:17	RW	L3_BAR2_ADDR: Base Address 2, aa14:31
18:34	RW	L3_BAR2_ADDR_MASK: Sets group size for BAR2, aa14:31 Values: SIZE_4_GB=>0b000000000000000000 SIZE_8_GB=>0b000000000000000001 SIZE_16_GB=>0b000000000000000011 SIZE_32_GB=>0b000000000000000111 SIZE_64_GB=>0b000000000000011111 SIZE_128_GB=>0b000000000001111111 SIZE_256_GB=>0b000000000011111111 SIZE_512_GB=>0b000000000111111111 SIZE_1_TB=>0b000000001111111111 SIZE_2_TB=>0b000000001111111111 SIZE_4_TB=>0b000000011111111111 SIZE_8_TB=>0b000000111111111111 SIZE_16_TB=>0b000001111111111111 SIZE_32_TB=>0b000011111111111111 SIZE_64_TB=>0b000111111111111111 SIZE_128_TB=>0b001111111111111111 SIZE_256_TB=>0b011111111111111111 SIZE_512_TB=>0b111111111111111111
35	RW	L3_BAR2_ENABLE: When on, will enable the BAR2 compare for lpc predict. The result of the BAR2 compare is ORd with the BAR1 compare to produce the lpc match.

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Bits	SCOM	Field Mnemonic: Description
36:63	RO	constant=0b00000000000000000000000000000000

Register Name	<i>L3 Hypervisor Purge Register</i>
Mnemonic	EXP.L3.L3_MISC.L3CERRS.PHYP_PURGE_REG
Address	0000000010010814 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX_WOR	L3_PHPY_PURGE_REQ: When set, will initiate a purge of the type specified by the ttype field beginning at the address specified in the address field. This bit will remain set until the purge is completed.
1:4	RW	L3_PHPY_PURGE_TTYPE: This field specifies which kind of operation is to be done, full purge, single line purge, single line delete, full blind purge or dynamic purge. Values: FULL_PURGE=>0b0000 SNGL_PURGE=>0b0001 SNGL_DELETE=>0b0010 FULL_BLIND_PURGE=>0b0100 DYNAMIC_PURGE=>0b0101
5	RWX_WOR	L3_PHPY_LINE_DEL_ON_NEXT_CE: When set, will cause RD and Snoop machines to delete the line on the next occurrence of a CE. This bit will be reset by hew when the line delete is done.
6	RW	L3_PHPY_LINE_DEL_ON_ALL_CE: When set, will cause RD and Snoop machines to delete the line on every occurrence of a CE.
7:8	RW	Reserved field. (Access type is l3_phyp_purge_reserved_1)
9	ROX	L3_PHPY_PURGE_BUSY_ERR: When set, indicates that a purge was requested when this register was still busy from a previous purge request. The request that caused this bit to be set will be dropped.
10:12	RW	Reserved field. (Access type is l3_phyp_purge_reserved_2)
13:28	RW	L3_PHPY_PURGE_DIR_ADDR: Specifies the directory address to begin the purge. 13:15 specifies the member(0:7) and 16:28 specifies the cgc(44:56). Note: the member is only used for single line delete/purge. Full, blind and dynamic always purge all 8 ways of the cache.
29:63	RO	constant=0b00000000000000000000000000000000

Register Name	<i>L3 Line Deleted Members Count Register</i>
Mnemonic	EXP.L3.L3_MISC.L3CERRS.LINE_DELETED_MEMBERS_REG
Address	0000000010010815 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RWX	L3_LINE_DELETED_MEMBERS: L3 Line Deleted member count. This register monitors the number of deleted members in any access congruence class. It can be cleared and will simply continue monitoring
4:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000



Register Name		L3 BAR Group Mask Register
Mnemonic		EXP.L3.L3_MISC.L3CERRS.BAR_GRP_MASK_REG
Address		0000000010010816 (SCOM)
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0:16	RW	L3_BAR1_GRP_ADDR_MASK: Sets group size for grp BAR1, aa15:31 Values: SIZE_4_GB=>0b0000000000000000 SIZE_8_GB=>0b0000000000000001 SIZE_16_GB=>0b0000000000000011 SIZE_32_GB=>0b0000000000000111 SIZE_64_GB=>0b0000000000001111 SIZE_128_GB=>0b0000000000011111 SIZE_256_GB=>0b0000000001111111 SIZE_512_GB=>0b0000000011111111 SIZE_1_TB=>0b0000000011111111 SIZE_2_TB=>0b0000000111111111 SIZE_4_TB=>0b0000001111111111 SIZE_8_TB=>0b0000011111111111 SIZE_16_TB=>0b0000111111111111 SIZE_32_TB=>0b0001111111111111 SIZE_64_TB=>0b0011111111111111 SIZE_128_TB=>0b0111111111111111 SIZE_256_TB=>0b1111111111111111 SIZE_512_TB=>0b1111111111111111
17:33	RW	L3_BAR2_GRP_ADDR_MASK: Sets group size for grp bar2, aa15:31 Values: SIZE_4_GB=>0b0000000000000000 SIZE_8_GB=>0b0000000000000001 SIZE_16_GB=>0b0000000000000011 SIZE_32_GB=>0b0000000000000111 SIZE_64_GB=>0b0000000000001111 SIZE_128_GB=>0b0000000000011111 SIZE_256_GB=>0b0000000001111111 SIZE_512_GB=>0b0000000011111111 SIZE_1_TB=>0b0000000011111111 SIZE_2_TB=>0b0000000111111111 SIZE_4_TB=>0b0000001111111111 SIZE_8_TB=>0b0000011111111111 SIZE_16_TB=>0b0000111111111111 SIZE_32_TB=>0b0001111111111111 SIZE_64_TB=>0b0011111111111111 SIZE_128_TB=>0b0111111111111111 SIZE_256_TB=>0b1111111111111111 SIZE_512_TB=>0b1111111111111111
34	RW	L3_BAR2_GRP_ENABLE: When on, will enable the BAR2 group compare for lpc predict. The result of the BAR2 group compare is ORd with the BAR1 group compare to produce the lpc match. This enable should be set to the same value as l3_bar2_enable.
35:63	RO	constant=0b00000000000000000000000000000000

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Register Name	<i>L3 Control Check Read Register 1</i>
Mnemonic	EXP.L3.L3_MISC.L3CERRS.L3_CTL_CHECK_RD1_REG
Address	0000000010010817 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RO	PF_MACHINE_HANG_ERR: pf_machine_hang_err
1	RO	WI_MACHINE_HANG_ERR: wi_machine_hang_err
2	RO	L3L2CTL_RD_OVERRUN_CHK_ERR: l3l2ctl_rd_overrun_ck_err
3	RO	L3L2CTL_PF_OVERRUN_CHK_ERR: l3l2ctl_pf_overrun_ck_err
4	RO	L3CICTL_CI_OVERRUN_CHK_ERR: l3l2ctl_ci_overrun_ck_err
5	RO	L3XMEMA0_DW_DIR_HIT_ERR: l3xmema0_dw_dir_hit_err
6	RO	L3XMEMA1_DW_DIR_HIT_ERR: l3xmema1_dw_dir_hit_err
7	RO	L3XMEMA0_CRW_DIR_HIT_ERR: l3xmema0_crw_dir_hit_err
8	RO	L3XMEMA1_CRW_DIR_HIT_ERR: l3xmema1_crw_dir_hit_err
9	RO	PBEXCA0_CMD_REQ_ERR0: pbexca0_cmd_req_err0
10	RO	PBEXCA0_CMD_REQ_ERR1: pbexca0_cmd_req_err1
11	RO	PBEXCA0_CMD_REQ_ERR2: pbexca0_cmd_req_err2
12	RO	PBEXCA1_CMD_REQ_ERR0: pbexca1_cmd_req_err0
13	RO	PBEXCA1_CMD_REQ_ERR1: pbexca1_cmd_req_err1
14	RO	PBEXCA1_CMD_REQ_ERR2: pbexca1_cmd_req_err2
15	RO	MC_FP_MATE_CMD_ERR0: mc_fp_mate_cmd_err0
16	RO	MC_FP_MATE_CMD_ERR1: mc_fp_mate_cmd_err1
17	RO	L3PBEXCA0_OVERFLOW_ERR: l3pbexca0_overflow_err
18	RO	L3PBEXCA1_OVERFLOW_ERR: l3pbexca1_overflow_err
19	RO	L3PBEXCA0_UNDERFLOW_ERR: l3pbexca0_underflow_err
20	RO	L3PBEXCA1_UNDERFLOW_ERR: l3pbexca1_underflow_err
21	RO	L3SDRTL0_HA_BDOPS_HIT_DADRTBL_ERR: l3sdrtl0_ha_bdops_hit_dadrtbl_err
22	RO	L3SDRTL1_HA_BDOPS_HIT_DADRTBL_ERR: l3sdrtl1_ha_bdops_hit_dadrtbl_err
23	RO	PF_MACHINE_W4DT_HANG_ERR: pf_machine_w4dt_hang_err
24	RO	WI_MACHINE_W4DT_HANG_ERR: wi_machine_w4dt_hang_err
25:59	RO	constant=0b00000000000000000000000000000000

Register Name	<i>Base Address Of L3 HA Dirty Address Table.</i>
Mnemonic	EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_TBL_BAR
Address	0000000010010818 (SCOM)
Attributes	
Description	



Bits	SCOM	Field Mnemonic: Description
0:1	RO	constant=0b00
2:31	RW	L3_HA_TABLE_BAR: HA dirty address table BAR 14:43.
32:59	RO	constant=0b00000000000000000000000000000000

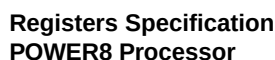
Register Name	L3 HA Control Register.
Mnemonic	EXP.L3.L3_MISC.L3CERRS.L3_HA_CONTROL_REG
Address	0000000010010819 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	L3_HA_DIRTY_ADDR_TBL_SEQ_WARN_SEL: Controls when the L3 will report a DirtyAddrTable Overflow Warning to the core. This must be set to allow for a guardband of 1.5x the L3 size (that is, 12MB) The value in this pointer represents the how close (in terms of sectors) the HA_DirtyAddrTable_Seg_Wr_Pntr(0:5) can come to the HA_DirtyAddrTable_Seg_Rd_Pntr(0:5) before the L3 will activate the overflow warning to the core.
5:8	RW	Reserved field. (Access type is l3_HA_control_spare)
9:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	HA Dirty Address Table Read Pointer
Mnemonic	EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_TBL_RD_PNTR
Address	000000001001081A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:4	RW	L3_HA_TABLE_SEG_RD_PTR: DirtyAddrTable consists of 32 segments. This value indicates the current segment that is being read (may not yet be fully read). this pointer is written by the hypervisor to indicate to hardware the location of Read_Pntr in the FIFO. The Rd_Pntr is used by the hardware with the DirtyAddrTbl_Seg_Wr_Pntr to determine how full the DirtyAddrTable is and if an overflow warning indication should be driven to the core(that is, HA DirtyAddrTable is close to overflowing). Hypervisor should update this pointer as when it finishes processing a segment worth of entries in the FIFO.
5:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	HA Dirty Address Table Write Pointer
Mnemonic	EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_TBL_WR_PNTR
Address	000000001001081B (SCOM)
Attributes	
Description	



Register Name	<i>HA Dirty Address Mem Block Control Reg.</i>	
Mnemonic	EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_MEM_BLK_CTL	
Address	000000001001081C (SCOM)	
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:5	RWX	L3_HA_DIRTY_ADDR_MEM_BLOCK_ENABLE: Enables HA_DirtyAddrMemBlock grp 0:5 access checking. L3 hardware must reset this bit when it detects the chiplet has been put into Fast or Deep Winkle. Hypervisor will re-enable this register when this chiplet is brought back up out of winkle.
6:7	RW	Reserved field. (Access type is l3_ha_reserved)
8:10	RW	L3_HA_DIRTY_ADDR_MEM_BLOCK_SEG_SIZE: Indication of the HA DirtyAddrMemBlock Size. (1MB Table represents 16MB of a data footprint). Values: 16MB=>0b000 32MB=>0b001 64MB=>0b010 128MB=>0b011 256MB=>0b100
11:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000 Values: 16MB=>0b000 32MB=>0b001 64MB=>0b010 128MB=>0b011 256MB=>0b100

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Bits	SCOM	Field Mnemonic: Description
28:51	RO	constant=0b000000000000000000000000

Register Name	<i>HA Dirty Address Mem Block Bar.</i>
Mnemonic	EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_MEM_BLK_BAR1
Address	000000001001081E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:1	RO	constant=0b00
2:27	RW	L3_HA_DIRTY_ADDR_MEM_BLOCK_BAR_1: HA dirty address table memory block BAR.
28:51	RO	constant=0b000000000000000000000000

Register Name	<i>HA Dirty Address Mem Block Bar.</i>
Mnemonic	EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_MEM_BLK_BAR2
Address	000000001001081F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:1	RO	constant=0b00
2:27	RW	L3_HA_DIRTY_ADDR_MEM_BLOCK_BAR_2: HA dirty address table memory block BAR.
28:51	RO	constant=0b000000000000000000000000

Register Name	<i>HA Dirty Address Mem Block Bar.</i>
Mnemonic	EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_MEM_BLK_BAR3
Address	0000000010010820 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:1	RO	constant=0b00
2:27	RW	L3_HA_DIRTY_ADDR_MEM_BLOCK_BAR_3: HA dirty address table memory block BAR.
28:51	RO	constant=0b000000000000000000000000

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Register Name	<i>HA Dirty Address Mem Block Bar.</i>
Mnemonic	EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_MEM_BLK_BAR4
Address	0000000010010821 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:1	RO	constant=0b00
2:27	RW	L3_HA_DIRTY_ADDR_MEM_BLOCK_BAR_4: HA dirty address table memory block BAR.
28:51	RO	constant=0b000000000000000000000000

Register Name	<i>HA Dirty Address Mem Block Bar.</i>
Mnemonic	EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_MEM_BLK_BAR5
Address	0000000010010822 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:1	RO	constant=0b00
2:27	RW	L3_HA_DIRTY_ADDR_MEM_BLOCK_BAR_5: HA dirty address table memory block BAR.
28:51	RO	constant=0b000000000000000000000000

Register Name	<i>HA Dirty Address Mem Block Consumer Reg.</i>
Mnemonic	EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_MEM_BLK_CONS0
Address	0000000010010823 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:11	RW	L3_HA_DIRTY_ADDR_MEM_BLOCK_CONS_EN_0: HA Dirty address mem block consumer enable.
12	RO	constant=0b0
13:15	RW	L3_HA_DIRTY_ADDR_MEM_BLOCK_CHIP_ID_0: HA Dirty address mem block chip id.
16:63	RO	constant=0b000000000000000000000000000000000000000000

Register Name	<i>HA Dirty Address Mem Block Consumer Reg.</i>
Mnemonic	EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_MEM_BLK_CONS1
Address	0000000010010824 (SCOM)
Attributes	
Description	



Bits	SCOM	Field Mnemonic: Description
0:11	RW	L3_HA_DIRTY_ADDR_MEM_BLOCK_CONS_EN_1: HA Dirty address mem block consumer enable.
12	RO	constant=0b0
13:15	RW	L3_HA_DIRTY_ADDR_MEM_BLOCK_CHIP_ID_1: HA Dirty address mem block chip id.
16:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>HA Dirty Address Mem Block Consumer Reg.</i>
Mnemonic	EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_MEM_BLK_CONS2
Address	0000000010010825 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:11	RW	L3_HA_DIRTY_ADDR_MEM_BLOCK_CONS_EN_2: HA Dirty address mem block consumer enable.
12	RO	constant=0b0
13:15	RW	L3_HA_DIRTY_ADDR_MEM_BLOCK_CHIP_ID_2: HA Dirty address mem block chip id.
16:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>HA Dirty Address Mem Block Consumer Reg.</i>
Mnemonic	EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_MEM_BLK_CONS3
Address	0000000010010826 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:11	RW	L3_HA_DIRTY_ADDR_MEM_BLOCK_CONS_EN_3: HA Dirty address mem block consumer enable.
12	RO	constant=0b0
13:15	RW	L3_HA_DIRTY_ADDR_MEM_BLOCK_CHIP_ID_3: HA Dirty address mem block chip id.
16:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>HA Dirty Address Mem Block Consumer Reg.</i>
Mnemonic	EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_MEM_BLK_CONS4
Address	0000000010010827 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:11	RW	L3_HA_DIRTY_ADDR_MEM_BLOCK_CONS_EN_4: HA Dirty address mem block consumer enable.
12	RO	constant=0b0
13:15	RW	L3_HA_DIRTY_ADDR_MEM_BLOCK_CHIP_ID_4: HA Dirty address mem block chip id.



Register Name	L3 Write Epsilon Config Register
Mnemonic	EXP.L3.L3_MISC.L3CERRS.L3_WR_EPSILON_CFG_REG
Address	000000001001082A (SCOM)
Attributes	
Description	

[illegible]

Register Name	L3 Mode Register 0
Mnemonic	EXP.L3.L3_MISC.L3CERRS.MODE_REG0
Address	000000001001082B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	L3_DISABLED_CFG: When on, disables this L3
1	RW	L3_DMAP_CI_EN_CFG: When on, puts L3 Cast-Ins into direct map mode
2	RW	L3_RDSN_LINEDEL_UE_EN: When on, enables RD and SN machines to line delete when they see cache read UEs. This needs to be set in IPL process
3	RW	L3_NO_ALLOCATE_MODE_EN: When on, enables the L3 to enter a non-allocation mode after a UE occurs
4	RWX	L3_NO_ALLOCATE_MODE_ACTIVE: When on, indicates that L3 is currently in non-allocation mode.
5	RW	L3_NOD_USE_GRP_RSRC_EN: When on, enables node pump requests to use group resource in pbi. L3 will receive group grant even though request was nodal scope.
6	RW	L3_IS_ECO_CFG: When on, indicates that this l3 is in ECO mode and will be reflected as such in DCache bits.
7	RW	L3_MODE_REG0_SPARE7: Spare.
8	RW	L3_LCO_RTY_LIMIT_DISABLE: When set, will never use an LCO retry limit count to change to CO_memory
9	RW	L3_LCO_HASH_GLOBAL_DIS: When on, disables ALL master LCO hash related behaviors.

[illegible]

Register Name	L3 Profiler Command Register
Mnemonic	EXP.L3.L3_MISC.L3CERRS.L3PRF_CMD_REG
Address	000000001001082C (SCOM)
Attributes	
Description	

[illegible]



Register Name	<i>L3 Profiler Hit01 Counter Register</i>
Mnemonic	EXP.L3.L3_PRF.L3CACPRF.L3PRF_HIT01_REG
Address	000000001001082D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	L3PRF_HIT0_COUNT: L3 profiler hit0 counter register
16:31	ROX	L3PRF_HIT1_COUNT: L3 profiler hit1 counter register
32:63	RO	constant=0b00000000000000000000000000000000

Register Name	<i>L3 Profiler Hit23 Counter Register</i>
Mnemonic	EXP.L3.L3_PRF.L3CACPRF.L3PRF_HIT23_REG
Address	000000001001082E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	L3PRF_HIT2_COUNT: L3 profiler hit2 counter register
16:31	ROX	L3PRF_HIT3_COUNT: L3 profiler hit3 counter register
32:63	RO	constant=0b00000000000000000000000000000000

Register Name	<i>L3 Profiler Hit45 Counter Register</i>
Mnemonic	EXP.L3.L3_PRF.L3CACPRF.L3PRF_HIT45_REG
Address	000000001001082F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	L3PRF_HIT4_COUNT: L3 profiler hit4 counter register
16:31	ROX	L3PRF_HIT5_COUNT: L3 profiler hit5 counter register
32:63	RO	constant=0b00000000000000000000000000000000

Register Name	<i>L3 Profiler Hit67 Counter Register</i>
Mnemonic	EXP.L3.L3_PRF.L3CACPRF.L3PRF_HIT67_REG
Address	0000000010010830 (SCOM)
Attributes	
Description	

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Bits	SCOM	Field Mnemonic: Description
0:15	ROX	L3PRF_HIT6_COUNT: L3 profiler hit6 counter register
16:31	ROX	L3PRF_HIT7_COUNT: L3 profiler hit7 counter register
32:63	RO	constant=0b00000000000000000000000000000000

Register Name	<i>L3 Profiler Miss Counter Register</i>
Mnemonic	EXP.L3.L3_PRF.L3CACPRF.L3PRF_MISS_REG
Address	0000000010010831 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	L3PRF_MISS_COUNT: L3 profiler miss counter register
16:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>HA Dirty Address Table SaveRestore Write Pointer</i>
Mnemonic	EXP.L3.L3_MISC.L3CERRS.L3_HA_DIRTY_ADDR_TBL_SAVERESTORE_WR_PNTR
Address	0000000010010832 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:16	RW	L3_HA_TABLE_SEG_SAVERESTORE_WR_PTR: DirtyAddrTable consists of 32 segments. This value indicates the current segment being written by hardware (may not yet be fully written). This pointer is sourced by hardware and read by the hypervisor to indicate the location of the Write_Pointer in the FIFO. Used by the hypervisor with the DirtyAddrTbl_Seg_RD_Pntr to determine how full the DirtyAddrTable is and if it is empty. The hypervisor should only write this registers at initialization time (that is, when the DirtyAddrTable FIFO is empty and inactive and the Rd_Pntr and Wr_Pntr are being set to zero). Any write to the register will trigger L3 Wr_Pntr(0:4) to take on this new value and also reset the L3's internal intrasegment wr_pntr value to point at the beginning of the segment.
17	RWX	Reserved field. (Access type is sequence_number)
18:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

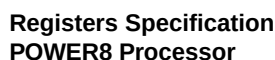
Register Name	<i>NCU FIR Register</i>
Mnemonic	EXP.NC.NCMISC.NCSCOMS.FIR_REG
Address	0000000010010C00 (SCOM) 0000000010010C01 (SCOM1) 0000000010010C02 (SCOM2)
Attributes	
Description	NCU FIR Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	CONTROL_ERR: Hardware control error.

[illegible]

Register Name	NCU FIR Mask Register
Mnemonic	EXP.NC.NCMISC.NCSCOMS.FIR_MASK_REG
Address	0000000010010C03 (SCOM) 0000000010010C04 (SCOM1) 0000000010010C05 (SCOM2)
Attributes	
Description	NCU FIR Mask Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	CONTROL_ERR_MASK: Hardware control error.
1	RW	WO_AND	WO_OR	TLBIE_SW_ERR_MASK: TLBIE received illegal AP/LP field from core.
2	RW	WO_AND	WO_OR	ST_ADDR_ERR_MASK: Store address machine or TLBIE/sync machine received addr_err cresp.
3	RW	WO_AND	WO_OR	LD_ADDR_ERR_MASK: Load address machine received addr_err cresp.
4	RW	WO_AND	WO_OR	ST_FOREIGN0_ACK_DEAD_MASK: Store received ack_dead on foreign link0.



Register Name	NCU FIR Action0 Register
Mnemonic	EXP.NC.NCMISC.NCSCOMS.FIR_ACTION0_REG
Address	0000000010010C06 (SCOM)
Attributes	
Description	NCU FIR Action0 Register

[illegible]



Register Name	NCU FIR Action1 Register
Mnemonic	EXP.NC.NCMISC.NCSCOMS.FIR_ACTION1_REG
Address	0000000010010C07 (SCOM)
Attributes	
Description	NCU FIR Action1 Register

[illegible]

Register Name	NCU Mode Register
Mnemonic	EXP.NC.NCMISC.NCSCOMS.NCU_MODE_REG
Address	0000000010010C0A (SCOM)
Attributes	
Description	

[illegible]



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Register Name	NCU Flush And Error Injection Register
Mnemonic	EXP.NC.NCMISC.NCSCOMS.INJ_REG
Address	0000000010010C0B (SCOM)
Attributes	
Description	

[illegible]

Register Name	<i>NCU Error Rpt Register</i>
Mnemonic	EXP.NC.NCMISC.NCSCOMS.ERR_RPT_REG
Address	0000000010010C0C (SCOM)
Attributes	
Description	

[illegible]



Register Name	<i>NCU Mode Register</i>
Mnemonic	EXP.NC.NCMISC.NCSCOMS.NCU_MODE_REG2
Address	0000000010010C0D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	RW	HANG_POLL_PULSE_DIV: Hang pulse divider.
4:7	RW	MASTER_CP_DATA_POLL_PULSE_DIV: Store/Load Master data hang divider.
8:11	RW	MASTER_TLB_DATA_POLL_PULSE_DIV: TLBIE Master data hang divider bits 0:4.
12:15	RW	TLB_SNOOP_DATA_POLL_PULSE_DIV: TLBIE Snooper data hang divider.
16:19	RW	TLB_STG1_HANG_POLL_PULSE_DIV: TLB master stg1 Hang pulse divider.
20:23	RW	TLB_STG2_HANG_POLL_PULSE_DIV: TLB master stg2 Hang pulse divider.
24	RW	MASTER_TLB_DATA_POLL_PULSE_DIV: TLBIE Master data hang divider bits 0:4.
25	RW	TLB_SNOOP_DATA_POLL_PULSE_DIV: TLBIE Snooper data hang divider.
26:63	RO	constant=0b000000000000000000000000000000000000000000000000000

Register Name	<i>NCU Mode Register</i>
Mnemonic	EXP.NC.NCMISC.NCSCOMS.NCU_MODE_REG3
Address	0000000010010C0E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	TLBIE_STALL_EN: Enables NCU stalling the core if NCU are overflowing with tlbies.
1:3	RW	TLBIE_STALL_THRESHOLD: The # of tlbies pending needed before the NCU will start the stall count. The minimum is 1; the maximum is 7
4:7	RW	TLBIE_STALL_CMPLT_CNT: The # of tlbies to be completed before NCU stops stalling the core. The minimum that should be set is 1; the maximum is 8
8:15	RW	TLBIE_STALL_DELAY_CNT: The # of cycles we will wait while over threshold before actually stalling the core. This count is in increments of 128 cycles, up to 32K
16:20	RW	TLB_SNOOP_DATA_POLL_PULSE_DIV2: TLBIE Snooper data hang divider.
21:63	RO	constant=0b000000000000000000000000000000000000000000000000000

Register Name	<i>HTM Collection Mode Register</i>
Mnemonic	EXP.TP.ECO_DOM.CHTM.SC.HTM_MODE
Address	0000000010011000 (SCOM)
Attributes	
Description	

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Bits	SCOM	Field Mnemonic: Description
0	RW	HTMSC_MODE_HTM_ENABLE: HTM enable, set by software to start htm trace
1:2	RW	HTMSC_MODE_CONTENT_SEL: HTM MODE: Core instruction trace, LLAT trace, OHA trace, or Direct Memory Write Values: CORE=>0b00 LLAT=>0b01 OHA=>0b10 DWM=>0b11
3	RW	HTMSC_MODE_WRITE_TTYPE: Unused bit
4:9	RW	HTMSC_MODE_CAPTURE: HTM capture mode(0:5) has different meanings according to the Content Select: When htm_mode_q(1 TO 2) == 00, that is, Core Instruction Trace 00xxxx : tc_pc_trace_active asserted when HTM_STAT[Tracing]=1 to purge the ERAT when entering and exiting trace 01xxxx : tc_pc_trace_active asserted when HTM_MODE[HTM_Trace_enable]=1 to purge the ERAT only at the beginning When htm_mode_q(1 TO 2) == 01, that is, LLAT Trace 0xxxxx : capture on assertion of I2_htm_llat_disp_req, that is, any dispatch request 1xxxxx : capture on assertion of I2_htm_llat_disp_req AND I2_llat_htm_rcdisp_occurred, that is, only on passed dispatch x0xxxx : capture on assertion of I2_htm_llat_disp_req, that is, loads or stores x1xxxx : capture on assertion of I2_htm_llat_disp_req AND I2_llat_htm_rcdisp_id_not_st, that is, only loads xx0xxx : capture on assertion of I2_llat_htm_pbl3hit_dval xx1xxx : no capture on assertion of I2_llat_htm_pbl3hit_dval - enable embedded timestamp When htm_mode_q(1 TO 2) == 11, that is, Direct Memory Write 1xxxxx : Enable HPMC-IMA Mode x1xxxx : Enable Power Proxy Write Mode
10	RO	Reserved.
11:12	RW	HTMSC_MODE_SPARE_1TO2: Spare bits
13	RW	HTMSC_MODE_WRAP: 0 = Stop trace when reach top of trace memory 1 = Trace will continue until a stop trigger is received. Wrap to beginning of trace memory when the top has been reached
14	RW	HTMSC_MODE_DIS_TSTAMP: 0 = write of timestamps enabled 1 = disable writing of time stamps
15	RW	HTMSC_MODE_SINGLE_TSTAMP: 0 = additional timestamp written on timer overflow 1 = timestamp only before new record (if enabled)
16	RW	HTMSC_MODE_DIS_STALL: 0 = core execution stalls when buffer full, Core Trace only 1 = core instruction trace stall disabled
17	RW	HTMSC_MODE_MARKERS_ONLY: 0 = default, override to global 1 = as programmed

[illegible]

Register Name	HTM Trace Memory Configuration Register
Mnemonic	EXP.TP.ECO_DOM.CHTM.SC.HTM_MEM
Address	0000000010011001 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	HTMSC_MEM_ALLOC: 0 = memory based address not configured 1 = memory address configured This bit must be written to zero before setting since the HTM looks for the 0->1 transition to indicate the memory address has been updated
1:3	RW	HTMSC_MEM_SCOPE: Configure the Scope used when writing the HTM Trace memory If the scope is not large enough, the HTM will get an address error If the scope is too large, HTM will experience excessive delay Set scope to system if chtm memory is on foreign link Values: NODAL=>0b000 GROUP=>0b001 SYSTEM=>0b010 REMOTE=>0b011
4:5	RW	HTMSC_MEM_PRIORITY: Configure the starting priority used when writing the HTM Trace memory. Values: LOW=>0b00 MEDIUM=>0b01 HIGH=>0b10
6:12	RO	constant=0b00000000 Values: LOW=>0b00 MEDIUM=>0b01 HIGH=>0b10
13	RW	HTMSC_MEM_SIZE_SMALL: 0 = Trace Mem Size from 512M to 256G 1 = Trace Mem Size from 16M to 8G
14:39	RW	HTMSC_MEM_BASE: Trace memory base address (14:39). The Trace Memory Base Address must be aligned on a Trace Memory Size boundary

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Bits	SCOM	Field Mnemonic: Description
40:48	RW	HTMSC_MEM_SIZE: When htmsc_mem_size_small=0, these bits define the mask to bits (26:35) of the Trace Memory Base Address and define the size of the trace memory between 512MB and 256GB When htmsc_mem_size_small=1, these bits define the mask to bits (31:39) of the Trace Memory Base address and define the size of the trace memory between 16MB and 8GB Values: 512M_OR_16M=>0b000000000 1G_OR_32M=>0b000000001 2G_OR_64M=>0b000000011 4G_OR_128M=>0b000000111 8G_OR_256M=>0b000001111 16G_OR_512M=>0b000011111 32G_OR_1G=>0b000111111 64G_OR_2G=>0b001111111 128G_OR_4G=>0b011111111 256G_OR_8G=>0b111111111
49:60	RO	constant=0b0000000000000 Values: 512M_OR_16M=>0b000000000 1G_OR_32M=>0b000000001 2G_OR_64M=>0b000000011 4G_OR_128M=>0b000000111 8G_OR_256M=>0b000001111 16G_OR_512M=>0b000011111 32G_OR_1G=>0b000111111 64G_OR_2G=>0b001111111 128G_OR_4G=>0b011111111 256G_OR_8G=>0b111111111

Register Name	HTM Trace Status Register
Mnemonic	EXP.TP.ECO_DOM.CHTM.SC.HTM_STAT
Address	0000000010011002 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	HTMCO_STATUS_PURGE_IN_PROG: Purge in Progress
1	ROX	HTMCO_STATUS_PURGE_DONE: Purge Done
2	ROX	HTMCO_STATUS_CRESP_OV: Not set in CHTM
3	ROX	HTMCO_STATUS_REPAIR: Address Repair: Asserted on occurrence of address error to indicate the need of software to clear and update HTM_MEM. Will stay high until HTM_MEM updated
4	ROX	HTMCO_STATUS_BUF_WAIT: Buffer Waiting: Asserted on condition of data buffers full in tracing state. Any markers, stamps, and trace data will be lost
5	ROX	STATUS_TRIG_DROPPED_Q: Buffer Overrun Trigger: Asserted on buffer overrun due to trigger lost. Cleared on the writing of 1 to the Reset Trigger bit, htmsc_trig_reset
6	ROX	HTMCO_STATUS_ADDR_ERROR: Address Error: Asserted on address error when write buffer was allocated. Need to set new address range
7	ROX	STATUS_REC_DROPPED_Q: Buffer Overrun Data: Asserted on buffer overrun due to trace data lost. Cleared on the writing of 1 to the Reset Trigger bit, htmsc_trig_reset

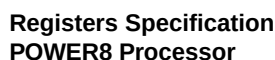
[illegible]

Register Name	HTM Last Address Register
Mnemonic	EXP.TP.ECO_DOM.CHTM.SC.HTM_LAST
Address	0000000010011003 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:13	RO	constant=0b00000000000000
14:56	ROX	HTM_LAST_ADDRESS: The last cache line address of the memory trace. Guaranteed valid only when HTM is in the Complete state
57:63	RO	constant=0b00000000

Register Name	HTM SCOM Trigger Register
Mnemonic	EXP.TP.ECO_DOM.CHTM.SC.HTM_TRIG
Address	0000000010011004 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	HTMSC_TRIG_START: Start trigger
1	RW	HTMSC_TRIG_STOP: Stop trigger
2	RW	HTMSC_TRIG_PAUSE: Pause trigger





Bits	SCOM	Field Mnemonic: Description
11:12	RW	HTMSC_CTRL_SPARE1112: Spare bits
13	RW	HTMSC_CTRL_XSTOP_STOP: Stop on XSTOP 1 = stop trigger on chiplet XSTOP 0 = ignore chiplet XSTOP
14:15	RW	HTMSC_CTRL_SPARE1415: Spare bits
16:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>HTM Per Thread Run Counter</i>
Mnemonic	EXP.TP.ECO_DOM.CHTM.SC.HTM_PTRC
Address	0000000010011006 (SCOM)
Attributes	
Description	Memory Access Counter

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	HTM_PTRC_THREAD0: run counter for thread 0
16:31	ROX	HTM_PTRC_THREAD1: run counter for thread 1
32:47	ROX	HTM_PTRC_THREAD2: run counter for thread 2
48:63	ROX	HTM_PTRC_THREAD3: run counter for thread 3

Register Name	<i>HTM Carry Select Register For Per Thread Run Counter</i>
Mnemonic	EXP.TP.ECO_DOM.CHTM.SC.HTM_CSEL
Address	0000000010011007 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:1	RW	HTMSC_PTRC_CSEL: 00 = IH 256ms TPMD Sampling 01 = HV/MR/HE 32ms TPMD Sampling 10 = Micro-partition <= 10ms 11 = Micro-partition <= 1ms
2:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>Mem Op Ctr</i>
Mnemonic	EXP.TP.ECO_DOM.CHTM.SC.MEM_OP_CTR
Address	0000000010011008 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	MEM_OP_CTR_OUT: Memory Access Counter
32:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

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Register Name	HTM IMA STATUS
Mnemonic	EXP.TP.ECO_DOM.CHTM.SC.HTM_IMA_STATUS
Address	000000001001100A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	HTMSC_IMA_ERROR: IMA ERROR :NCU transfer error. De-asserted after performing the CHTM HPMC-IMA reset sequence.
1	ROX	HTMSC_IMA_TRACE_ACTIVE: IMA Trace Active: IMA idle indicator
2	ROX	HTMSC_PDBAR_ERROR: PDBAR Parity Error. De-asserted after performing the CHTM HPMC-IMA reset sequence.
3:4	ROX	HTMSC_IMA_RESERVED: Reserved
5:11	ROX	HTMSC_IMA_FSM: Display Current IMA FSM State 01 Disabled 02 Idle 04 Clear 08 Capture 10 Write LDBAR 20 Write PDBAR 40 Error
12:15	ROX	HTMSC_IMA_COUNT: Number of writes completed to LDBAR or PDBAR address. Counts 0 to 7
16:31	ROX	HTMSC_IMA_UNUSED: Unused
32	ROX	HTMSC_PPW_ERROR: PPXY Error: NCU transfer error. De-asserted after performing the CHTM PPXY reset sequence.
33	ROX	HTMSC_PPW_READY: PPXY Ready. tchtm_tcoha_ppw_ready asserted.
34:39	ROX	HTMSC_PPW_FSM: Display Current PPXY FSM state 01 Disabled 02 Idle 04 Clear 08 Capture 10 Write 20 Error
40:63	RO	constant=0b000000000000000000000000

Register Name	HTM IMA PDBAR	
Mnemonic	EXP.TP.ECO_DOM.CHTM.SC.HTM_IMA_PDBAR	
Address	000000001001100B (SCOM)	
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0	RO	constant=0b0



Bits	SCOM	Field Mnemonic: Description
1	RW	HTMSC_IMA_ENABLE_SPLIT_CORE: This bit controls the indexing of the PDBAR address for the starting address of the write to the PDBAR space. 0 = big core mode 1 = split core mode
2:4	RW	HTMSC_IMA_PDBAR_SPARE2TO4:
5:7	RW	HTMSC_IMA_PDBAR_SCOPE: Configure the Scope used for direct memory write The scope will be forced to a group minimum unless HTM_MODE(dis_force_group)=1 Foreign scope is not supported Values: NODAL=>0b000 GROUP=>0b001 SYSTEM=>0b010 REMOTE=>0b011
8:13	RW	HTMSC_IMA_PDBAR_SPARE8TO13:
14:50	RW	HTMSC_IMA_PDBAR: IMA Write Physical Base Address PDBAR spare bit 2 to 4 PDBAR spare bit 8 to 13
51:63	RO	constant=0b00000000000000

Register Name		<i>Trace Array High Data Register</i>
Mnemonic		EXP.TP.CORE_DOM.TRAL20.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG
Address		0000000010012000 (SCOM)
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63

Register Name		<i>Trace Array Low Data Register</i>
Mnemonic		EXP.TP.CORE_DOM.TRAL20.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG
Address		0000000010012001 (SCOM)
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95
32:41	ROX	TRACE_ADDRESS: Trace Address
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank
51	ROX	TRACE_LAST_BANK_VALID: Trace Last Bank Valid
52	ROX	TRACE_WRITE_ON_RUN: Trace Write-On-Run indicator
53	ROX	TRACE_RUNNING: Trace Run indicator
54:63	ROX	TRACE_HOLD_ADDRESS: Trace Hold Address (pointing to last entry)

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Register Name	<i>Trace Array High Data Register</i>		
Mnemonic	EXP.TP.CORE_DOM.TRAL21.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG		
Address	0000000010012400 (SCOM)		
Attributes			
Description			

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63

Register Name	<i>Trace Array Low Data Register</i>		
Mnemonic	EXP.TP.CORE_DOM.TRAL21.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG		
Address	0000000010012401 (SCOM)		
Attributes			
Description			

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95
32:41	ROX	TRACE_ADDRESS: Trace Address
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank
51	ROX	TRACE_LAST_BANK_VALID: Trace Last Bank Valid
52	ROX	TRACE_WRITE_ON_RUN: Trace Write-On-Run indicator
53	ROX	TRACE_RUNNING: Trace Run indicator
54:63	ROX	TRACE_HOLD_ADDRESS: Trace Hold Address (pointing to last entry)

Register Name	<i>L2 FIR Register</i>		
Mnemonic	EXP.L2.L2MISC.L2CERRS.FIR_REG		
Address	0000000010012800 (SCOM) 0000000010012801 (SCOM1) 0000000010012802 (SCOM2)		
Attributes			
Description	L2 FIR Register		

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	CACHE_RD_CE: Hardware Trigger Mechanism at the point the cache read occurs that detects a CE by ECCCK on RC/CO/SN read. Note: PRD counts the number of these and then will trigger LineDelete.
1	RWX	WOX_AND	WOX_OR	CACHE_RD_UE: The hardware Trigger Mechanism at the point the cache read occurs that detects a UE (non SUE) by ECCCK on RC/CO/SN read.
2	RWX	WOX_AND	WOX_OR	CACHE_RD_SUE: The hardware Trigger Mechanism at the point the cache read occurs that detects a SUE by ECCCK on RC/CO/SN read.
3	RWX	WOX_AND	WOX_OR	HW_DIR_INITIATED_LINE_DELETE_OCCURRED: The hardware-initiated Line Delete occurred (ld state injected into the dir) by RC or SN machine.



Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
4	RWX	WOX_AND	WOX_OR	CACHE_UE_SUE_DETECTED_ON_MODIFIED_LINE_BY_CO: L2 Castout where L2 cache read detected UE/SUE and Line is M,Mu,T,Tn
5	RWX	WOX_AND	WOX_OR	CACHE_UE_SUE_DETECTED_ON_NON_MODIFIED_LINE_BY_CO: L2 Castout where L2 cache read detected UE/SUE and Line is Me,Te,Ten,SI,S
6	RWX	WOX_AND	WOX_OR	DIR_CE_DETECTED: L2 corrected a CE in the L2 directory
7	RWX	WOX_AND	WOX_OR	DIR_UE_DETECTED: L2 detected a UE in the L2 directory
8	RWX	WOX_AND	WOX_OR	DIR_STUCK_BIT_CE: L2 detected a SBCE in the L2 directory
9	RWX	WOX_AND	WOX_OR	DIR_SBCE_REPAIR_FAILED: PEC attempted to repair and CO a SBCE condition but failed (for example, CO disp failed). Cache line was lost.
10	RWX	WOX_AND	WOX_OR	MULTIPLE_DIR_ERRORS_DETECTED: DEPRICATED: THIS FIR BIT SHOULD ALWAYS BE MASKED. Multiple CE/UE detected between 2 hang 'early hang' pulse time window
11	RWX	WOX_AND	WOX_OR	LRU_READ_ERROR_DETECTED: LRU array has illegal value in it(due to flipped bit)
12	RWX	WOX_AND	WOX_OR	RC_processor bus_DATA_TIMEOUT: RC timed out waiting for processor bus to return data.
13	RWX	WOX_AND	WOX_OR	NCU_processor bus_DATA_TIMEOUT: NCU timed out waiting for processor bus to return data.
14	RWX	WOX_AND	WOX_OR	HW_CONTROL_ERROR: Internal hardware control error
15	RWX	WOX_AND	WOX_OR	LRU_ALL_MEMBERS_IN_CGC_ARE_LINE_DELETED: All members in a single congruence class has been deleted
16	RWX	WOX_AND	WOX_OR	CACHE_INHIBITED_HIT_CACHEABLE_ERROR: Cache Inhibited Ld/St hit a line in the L2 cache. SW error
17	RWX	WOX_AND	WOX_OR	RC_LOAD_RECIVED_PB_CRESP_ADR_ERR: RC was doing a fabric op on behalf of a load and got an cresp=addr_err
18	RWX	WOX_AND	WOX_OR	RC_STORE_RECIVED_PB_CRESP_ADR_ERR: RC was doing a fabric op on behalf of a store and got an cresp=addr_err
19	RWX	WOX_AND	WOX_OR	RC_POWBUS_DATA_CE_ERR_FROM_F2CHK: RC incoming Power Bus data had a CE error.
20	RWX	WOX_AND	WOX_OR	RC_POWBUS_DATA_UE_ERR_FROM_F2CHK: RC incoming Power Bus data had a UE error.
21	RWX	WOX_AND	WOX_OR	RC_POWBUS_DATA_SUE_ERR_FROM_F2CHK: RC incoming Power Bus data had a SUE error.
22	RWX	WOX_AND	WOX_OR	CO_ICSW_UE_SUE_DATA_ERR_FROM_F2CHK: CO cache read data has UE or SUE error.
23	RWX	WOX_AND	WOX_OR	RC_LOAD_RECIVED_PB_CRESP_ADR_ERR_FOR_HYP: RC was doing a fabric op on behalf of a load and got an cresp=addr_err for hyp memory
24	RWX	WOX_AND	WOX_OR	RCDAT_RD_PARITY_ERR: RCDAT read parity error.
25	RWX	WOX_AND	WOX_OR	CO_ICSW_RTY_BUSY_ABT_ERR: co_icsw_rty_busy_abt_err
26	RWX	WOX_AND	WOX_OR	HA_LOG_STOP_SW_ERR: ha_log_stop_sw_err
27	RWX	WOX_AND	WOX_OR	RC_LOAD_RECEIVED_PB_ACK_DEAD_FROM_FOREIGN0: rc_load_received_pb_ack_dead_from_foreign0
28	RWX	WOX_AND	WOX_OR	RC_LOAD_RECEIVED_PB_ACK_DEAD_FROM_FOREIGN1: rc_load_received_pb_ack_dead_from_foreign1
29	RWX	WOX_AND	WOX_OR	RC_STORE_RECEIVED_PB_ACK_DEAD_FROM_FOREIGN0: rc_store_received_pb_ack_dead_from_foreign0

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
30	RWX	WOX_AND	WOX_OR	RC_STORE_RECEIVED_PB_ACK_DEAD_FROM_FOREIGN1: rc_store_received_pb_ack_dead_from_foreign1
31	RWX	WOX_AND	WOX_OR	ILLEGAL_MPALOG_TPID_SW_ERR: illegal tpid combination on mpalog
32	RWX	WOX_AND	WOX_OR	UNEXP_HA_ST_ERR: HA store after ha_log_stop
33	RWX	WOX_AND	WOX_OR	HA_LINE_IN_CONS_CACHE_ERR: HA line in consumer cache.
34	RWX	WOX_AND	WOX_OR	HA_TABLE_IN_PROD_CACHE_ERR: HA table in producer cache.
35	RWX	WOX_AND	WOX_OR	ILLEGAL_LOG_STOP_SW_ERR: Illegal tpid combination on halogstop.
36	RWX	WOX_AND	WOX_OR	CACHE_RD_CE_AND_UE: Cache read CE and UE popped within a short hang pulse. Could be a triple bit error.
37:47	RWX	WOX_AND	WOX_OR	SPARE: spare
48	RWX	WOX_AND	WOX_OR	SCOM_ERR1: scom error
49	RWX	WOX_AND	WOX_OR	SCOM_ERR2: scom error
50:63	RO	N/A	N/A	constant=0b000000000000000

Register Name	L2 FIR Mask Register
Mnemonic	EXP.L2.L2MISC.L2CERRS.FIR_MASK_REG
Address	0000000010012803 (SCOM) 0000000010012804 (SCOM1) 0000000010012805 (SCOM2)
Attributes	
Description	L2 FIR Mask Register

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0:49	RW	WO_AND	WO_OR	L2_FIR_MASK: L2 Fir mask reg
50:63	RO	N/A	N/A	constant=0b000000000000000

Register Name	L2 FIR Action0 Register
Mnemonic	EXP.L2.L2MISC.L2CERRS.FIR_ACTION0_REG
Address	0000000010012806 (SCOM)
Attributes	
Description	L2 FIR Action0 Register

Bits	SCOM	Field Mnemonic: Description
0:49	RW	FIR_ACTION0: Action0 select for corresponding bit in FIR (Action0,Action1) = Action Select (0,0) = Checkstop Error (0,1) = Recoverable Error (1,0) = Reserved (1,1) = Local Core Checkstop
50:63	RO	constant=0b000000000000000



Register Name	L2 FIR Action1 Register	
Mnemonic	EXP.L2.L2MISC.L2CERRS.FIR_ACTION1_REG	
Address	0000000010012807 (SCOM)	
Attributes		
Description	L2 FIR Action1 Register	

Bits	SCOM	Field Mnemonic: Description
0:49	RW	FIR_ACTION1: Action1 select for corresponding bit in FIR (Action0,Action1) = Action Select (0,0) = Checkstop Error (0,1) = Recoverable Error (1,0) = Reserved (1,1) = Local Core Checkstop
50:63	RO	constant=0b0000000000000000

Register Name	L2 Mode Register 0	
Mnemonic	EXP.L2.L2MISC.L2CERRS.MODE_REG0	
Address	000000001001280A (SCOM)	
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0	RW	CFG_LRU_DIRECT_MAP: Not all combinations are supported. Enables direct-mapped LRU mode.
1	RW	CFG_RANDOM_EN: Not all combinations are supported. Enables random LRU mode.
2	RW	CFG_SINGLE_MEM_EN: Not all combinations are supported. Enables only 1 member per congruence class to be used.
3:10	RW	CFG_SINGLE_MEM: Not all combinations are supported. One-hot member to use in single member mode. Values: FLUSH_STATE=>0b00000000 SET0=>0b10000000 SET1=>0b01000000 SET2=>0b00100000 SET3=>0b00010000 SET4=>0b00001000 SET5=>0b00000100 SET6=>0b00000010 SET7=>0b00000001
11	RW	CFG_L3_DIS: Indicates that the L3 below the L2 is disabled
12	RW	CFG_CO_SOFT_PURGE_ME_SX_EN: Enables CO soft purge on shared. All Me and Sx cache lines are dropped when they are cast-out of the L2.
13	RW	CFG_CO_SOFT_PURGE_ALL_LINES_EN: Enables CO soft purge on modified. All Mx and Tx cache lines are dropped when they are cast out of the L2. This mode is ONLY intended for use at bootup where software is destroying the boot-code pre-loaded into the L2 by flushing the L2. Note: While this bit is set, if ICSWs or Part64B lines are attempted, the COFSM will discard these ops.
14	RW	CFG_DCBZ_TRASHMODE_EN: Enable RC, for L2 trash mode, to treat 128B-marked stores or DCBZs such that RC will not go to the processor bus but instead pretend that it received a cresp=go_m. Software Restriction: ICSW and ICSWcr instructions should NOT be issued while in this mode (reproducible trash mode) since this will cause the COFSM to go to the processor bus. If trash is being run as non-reproducible (that is, PB active), then ICSW/ICSWcr can be sent and the COFSM will attempt them on the power bus.

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Bits	SCOM	Field Mnemonic: Description
15	RW	CFG_CAC_ERR_REPAIR_EN: Cache error repair enable. Enables RC and SN to trigger a purge action (of the line they are working on) if they detect a CE/UE/SUE on a cache read.
16	RW	CFG_LINEDEL_ON_CAC_UE_EN: Enable line delete on cache UE (or software trig_det ce). L2 RC/SN, upon detecting UE (or software trig_det ce) on a cache read, will trigger a purge of the line and write the dir=Id. The Id will cause the L2 to never allocate into this physical location (that is, the L2 assumes these cache line cells are damaged. Note: If this bit is set to Disable, then sw trig_det ce should not be activated. If software trig_det is activated, the RC will purge the line on CE, but the software trig_det ce masking will never reset since it is waiting for the RC to indicate that it wrote an Id on behalf of the ce (which this bit prevented).
17	RW	CFG_HW_TRIG_LINEDEL_LDDISP_CE_EN: Warning: This is for lab debug ONLY!!! Enable line delete on detection of any RC dispatch of a Load that is an L2hit that results is a cache CE or UE (SUE will not trigger the LineDelete). Upon detecting CE/UE on a cache read, will trigger a purge of the line and write the dir=Id. The Id will cause the L2 to never allocate into this physical location (that is, the L2 assumes these cache line cells are damaged). Warning: This aggressive LineDelete policy could cause soft CEs to quickly form a large number of LineDelete locations in the cache (that is, to the point where a cgc in the L2 has been completely LineDeleted away...causing a hang). This lab-only mode is intended for early-bringup parts.
18:20	RW	CFG_L2_PB_ARB_RATE_SEL: Selects how fast the L2 requests to the PB Values: FULL_RATE=>0b000 CAN_L3PF=>0b001 EVERY64_CAN_L3PF=>0b100 EVERY128_CAN_L3PF=>0b101 EVERY256_CAN_L3PF=>0b110 EVERY512_CAN_L3PF=>0b111
21	RW	CFG_HASH_L3_ADDR_EN: COMMENTS TO BE ADDED LATER
22	RW	CFG_RC_FRC_DISP_EQ_NTM_INIG_SI_TO_RCR_EN: Enables TM trash mode where In or Ig goes to L3 instead of PB.
23	RW	Reserved field. (Access type is rsv)
24:27	RW	CFG_Q_BIT_TPID: QOS bits help PB and MC arbitrate.
28	RW	CFG_STQ_PF_EN: Enables store spawned prefetching.
29	RW	CFG_DCACHE_CAPP_LPC_MODE_EN: Enables store spawned prefetching.
30:31	RW	Reserved field. (Access type is mode_reg0_spare)
32:63	RO	constant=0b00000000000000000000000000000000

Register Name	L2 Mode Register 1
Mnemonic	EXP.L2.L2MISC.L2CERRS.MODE_REG1
Address	000000001001280B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	CFG_ECCCK_CE_UE_SUE_ERR_DET_DIS: When 1, causes eccck CE,UE,SUE to all be gated off from being seen by RC/CO/SN and FIR logic (that is, rcdsp masks ECCCK signals). This bit is meant as a fail-safe mode. All errors will be ignored by RC/CO/SN FIR bits wont get set SUE data that is brought in or forms due to misses will LOSE is SUE stamp on the next L2 Id/st hit (that is, RC ignores all errors and assumes data should be used as is

[illegible]

Register Name	L2 Error Injection Register
Mnemonic	EXP.L2.L2MISC.L2CERRS.ERR_INJ_REG
Address	000000001001280C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:2	RW	ERR_INJ_DW_TYPE: 000 => disable error injection 001 => dir CE inject next write 010 => dir CE inject every write 011 => dir CE inject 1 of the writes 100 => rsv 101 => dir UE inject on next write 110 => rsv 111 => rsv Values: DW_ERR_INJ_DIS=>0b000 DW_CE_NEXT=>0b001 DW_CE_EVERY=>0b010 DW_CE_LFSR=>0b011 DW_UE_NEXT=>0b101
3	RO	constant=0b0 Values: DW_ERR_INJ_DIS=>0b000 DW_CE_NEXT=>0b001 DW_CE_EVERY=>0b010 DW_CE_LFSR=>0b011 DW_UE_NEXT=>0b101

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Bits	SCOM	Field Mnemonic: Description
4:7	RW	ERR_INJ_CW_TYPE: 0000 => disable error injection 0001 => rsv 0010 => rsv 0011 => rsv 0100 => CE injection next write one 32B sector if RC cw_vect has one 32B sector marked in 1st 64B first two 32B sectors if 1st two sectors of RC cw_vect are being written 0101 => CE injection every write(all 32B sectors written are corrupted) 0110 => CE injection 25 of the writes one 32B sector if RC cw_vect has one 32B sector marked in 1st 64B first two 32B sectors if 1st two sectors of RC cw_vect are being written 0100 => rsv 1000 => UE injection next write (see CE rules) 1001 => UE injection every write(see CE rules) 1010 => rsv 1011 => rsv 1100 => SUE injection next write(see CE rules) 1101 => SUE injection every write(see CE rules) 1110 => rsv 1111 => rsv Values: CW_ERR_INJ_DIS=>0b0000 CW_CE_NEXT=>0b0100 CW_CE_EVERY=>0b0101 CW_CE_LFSR=>0b0110 CW_UE_NEXT=>0b1000 CW_UE_EVERY=>0b1001 CW_SUE_NEXT=>0b1100 CW_SUE_EVERY=>0b1101
8:9	RW	ERR_INJ_STQ_TYPE: 00 => disable error injection 01 => rsv 10 => parity injection next write (into stq cra) 11 => parity injection every write (into stq cra) Values: STQ_ERR_INJ_DIS=>0b00 STQ_PE_NEXT=>0b10 STQ_PE_EVERY=>0b11
10:12	RW	ERR_INJ_CPI_TYPE: 000 => disable error injection 001 => rsv 010 => rsv 011 => rsv 100 => CE injection next write (via eccck)(1st 64B read in 128B corrupted) 101 => CE injection every write (via eccck) (all 128B read in 128B corrupted) 110 => UE injection next write (via eccck) 111 => UE injection every write (via eccck) Values: CPI_ERR_INJ_DIS=>0b000 CPI_CE_NEXT=>0b100 CPI_CE_EVERY=>0b101 CPI_UE_NEXT=>0b110 CPI_UE_EVERY=>0b111



Bits	SCOM	Field Mnemonic: Description
13:63	RO	constant=0b000000000000000000000000000000000000000000 Values: CPI_ERR_INJ_DIS=>0b000 CPI_CE_NEXT=>0b100 CPI_CE_EVERY=>0b101 CPI_UE_NEXT=>0b110 CPI_UE_EVERY=>0b111

Register Name	<i>L2 One Shot Line Delete On Next CE Trigger Register</i>
Mnemonic	EXP.L2.L2MISC.L2CERRS.LINEDEL_TRIG_REG
Address	000000001001280D (SCOM)
Attributes	
Description	

[illegible]

Register Name	PRD Purge Engine Command Register
Mnemonic	EXP.L2.L2MISC.L2CERRS.PRD_PURGE_CMD_REG
Address	000000001001280E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	PRD_PURGE_CMD_TRIGGER: When this register is written and this trigger bit is being loaded with a 1, this will cause the Purge Engine Mechanism to start up. Note: the reg_busy must be 0 (that is, completion bit set) before the state of any of the purge_cmd register is changed.

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Bits	SCOM	Field Mnemonic: Description
1:4	RW	PRD_PURGE_CMD_TYPE: 0000 L2 Cache_Flush mem(0:2), addr(48:55), bank (ra56), must all be set to 0s. (see Note1) 0010 L2 Dir Line_Delete mem(0:2), addr(48:55), bank (ra56), must be set to the directory entry being deleted. The RC will victimize entry and write directory to Id (see note1). 0011 L2 Cache_mini_flush mem(0:2) and bank must be set to 0. addr(48:55) can be set to any cgc. L2 will flush all 8 members in the next 32 cgc Values: L2CAC_FLUSH=>0b0000 L2DIR_LINE_DEL=>0b0010 L2CAC_MINI_FLUSH=>0b0011
5:8	RO	constant=0b0000 Values: L2CAC_FLUSH=>0b0000 L2DIR_LINE_DEL=>0b0010 L2CAC_MINI_FLUSH=>0b0011
9	RWX	PRD_PURGE_CMD_REG_BUSY: Command Register is waiting to be serviced by purge state machine.
10	ROX	PRD_PURGE_CMD_PRGSM_BUSY_ON_THIS: Purge machine has taken this register's command.
11	ROX	PRD_PURGE_CMD_PRGSM_BUSY: Purge machine is currently busy on something.
12:16	RO	constant=0b00000
17:19	RW	PRD_PURGE_CMD_MEM: member associated with L2 LineDelete commands For a L2 Cache_Flush command, member(0:2) must be set to 0b000.
20:27	RW	PRD_PURGE_CMD_CGC: cgc address for L2 Line_Delete commands For a L2 Cache_Flush command, cgc(0:7) must be set to 0x00.
28	RW	PRD_PURGE_CMD_BANK: bank for L2 Line_Delete commands For a L2 Cache_Flush command, bank must be set to 0.
29	RWX	PRD_PURGE_CMD_ERR: Tried to write cmd_reg while cmd_reg_busy = 1 or illegal ttype.
30:63	RO	constant=0b00000000000000000000000000000000

Register Name	<i>Hypervisor Purge Engine Command Register</i>
Mnemonic	EXP.L2.L2MISC.L2CERRS.PHYP_PURGE_CMD_REG
Address	000000001001280F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	PHYP_PURGE_CMD_TRIGGER: When this register is written and this trigger bit is being loaded with a 1, this will cause the Purge Engine Mechanism to start up. Note: the reg_busy must be 0 (that is, completion bit set) before the state of any of the purge_cmd register is changed.

Bits	SCOM	Field Mnemonic: Description
1:4	RW	PHYP_PURGE_CMD_TYPE: 0000 L2 Cache_Flush mem(0:2), addr(48:55), bank (ra56), must all be set to 0s. (see Note1) 0010 L2 Dir Line_Delete mem(0:2), addr(48:55), bank (ra56), must be set to the directory entry being deleted. The RC will victimize entry and write directory to Id (see note1). 0011 L2 Cache_mini_flush mem(0:2) and bank must be set to 0. addr(48:55) can be set to any cgc. L2 will flush all 8 members in the next 32 cgc Values: L2CAC_FLUSH=>0b0000 L2DIR_LINE_DEL=>0b0010 L2CAC_MINI_FLUSH=>0b0011
5:8	RO	constant=0b0000 Values: L2CAC_FLUSH=>0b0000 L2DIR_LINE_DEL=>0b0010 L2CAC_MINI_FLUSH=>0b0011
9	RWX	PHYP_PURGE_CMD_REG_BUSY: Command Register is waiting to be serviced by purge state machine.
10	ROX	PHYP_PURGE_CMD_PRGSM_BUSY_ON_THIS: Purge machine has taken this register's command.
11	ROX	PHYP_PURGE_CMD_PRGSM_BUSY: Purge machine is currently busy on something.
12:16	RO	constant=0b00000
17:19	RW	PHYP_PURGE_CMD_MEM: member associated with L2 LineDelete commands For a L2 Cache_Flush command, member(0:2) must be set to 0b000.
20:27	RW	PHYP_PURGE_CMD_CGC: cgc address for L2 Line_Delete commands For a L2 Cache_Flush command, cgc(0:7) must be set to 0x00.
28	RW	PHYP_PURGE_CMD_BANK: bank for L2 Line_Delete commands For a L2 Cache_Flush command, bank must be set to 0.
29	RWX	PHYP_PURGE_CMD_ERR: Tried to write cmd_reg while cmd_reg_busy = 1 or illegal ttype.
30:63	RO	constant=0b00000000000000000000000000000000

Register Name	HA Command Register
Mnemonic	EXP.L2.L2MISC.L2CERRS.HA_CMD_REG
Address	0000000010012810 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	HA_CMD_TRIGGER: When this register is written and this trigger bit is being loaded with a 1, this will cause the Purge Engine Mechanism to start up. If a new HA walk is triggered before a previous one is done then the purge machine will restart with a OR of the new and previous HA walk's tpid bits set. All HA walks should end with a done bit in the status register.

[illegible]

Register Name	HA Status Register
Mnemonic	EXP.L2.L2MISC.L2CERRS.HA_STAT_REG
Address	0000000010012811 (SCOM)
Attributes	
Description	

[illegible]



Register Name	<i>MP Command Register, Do Not Use, This Function Is No Longer Supported</i>
Mnemonic	EXP.L2.L2MISC.L2CERRS.MP_CMD_REG
Address	0000000010012812 (SCOM)
Attributes	
Description	

[illegible]

Register Name	MP Status Register
Mnemonic	EXP.L2.L2MISC.L2CERRS.MP_STAT_REG
Address	0000000010012813 (SCOM)
Attributes	
Description	



Bits	SCOM	Field Mnemonic: Description
0	ROX	FIR14_NCCTL_NLDSM_ERR: err_rpt hold
1	ROX	FIR14_NCCTL_RLD_BARRIER_ERR: err_rpt hold
2	ROX	FIR14_NCCTL_SNP_ERR: err_rpt hold
3	ROX	FIR14_NCCTL_TLBIE_ACK_ERR: err_rpt hold
4	ROX	FIR14_NCCTL_SYNC_ERR: err_rpt hold
5	ROX	FIR14_NCCTL_VSYNC_ERR: err_rpt hold
6	ROX	FIR14_TMCTL_TIDX_TEND_LDST_SEQ_ERR: err_rpt hold

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Bits	SCOM	Field Mnemonic: Description
7	ROX	FIR14_RVCTL_ERR: err_rpt hold
8	ROX	FIR14_SRCTL0_BAD_HPC_ERR: err_rpt hold
9	ROX	FIR14_SRCTL1_BAD_HPC_ERR: err_rpt hold
10	ROX	FIR14_PBARB_FSM_REQ_OVERFLOW_ERR: err_rpt hold
11	ROX	FIR14_PBARB_TRASHMODE_PB_REQ_ERR: err_rpt hold
12	ROX	FIR14_L3PF_MACH_DONE_ERR: err_rpt hold
13	ROX	FIR14_RCMD0_TTAG_PERR: err_rpt hold
14	ROX	FIR14_RCMD1_TTAG_PERR: err_rpt hold
15	ROX	FIR14_CR0_TTAG_PERR: err_rpt hold
16	ROX	FIR14_CR0_ATAG_PERR: err_rpt hold
17	ROX	FIR14_CR1_TTAG_PERR: err_rpt hold
18	ROX	FIR14_CR1_ATAG_PERR: err_rpt hold
19	ROX	FIR14_RCMD0_ADDR_PERR: err_rpt hold
20	ROX	FIR14_RCMD1_ADDR_PERR: err_rpt hold
21	ROX	FIR9_PEC_PHASE3_TIMEOUT: err_rpt hold
22	ROX	FIR9_PEC_PHASE4_SAME_ERR: err_rpt hold
23	ROX	FIR9_PEC_PHASE4_RCCO_DISP_FAIL: err_rpt hold
24	ROX	FIR9_PEC_PHASE5_TIMEOUT: err_rpt hold
25	ROX	FIR14_B01_BOTH_ACTIVE: err_rpt hold
26	ROX	FIR14_PHANTOM_B01_REQ: err_rpt hold
27	ROX	FIR14_RC_UNEXP_F2_DATA_ERR: err_rpt hold
28	ROX	FIR14_RC_UNEXP_PURG_HIT_ERR: err_rpt hold
29	ROX	FIR14_RCX_UNEXP_IDLE_PBL3_DATA_ERR: err_rpt hold
30	ROX	FIR14_RCX_UNEXP_IDLE_PB_CRESP_ERR: err_rpt hold
31	ROX	FIR14_COX_UNEXP_IDLE_PB_CRESP_ERR: err_rpt hold
32	ROX	FIR14_RCX_UNEXP_IDLE_L3_CRESP_ERR: err_rpt hold
33	ROX	FIR14_RCX_UNEXP_IDLE_L3_DWDONE_ERR: err_rpt hold
34	ROX	FIR14_RCX_UNEXP_PB_RC_DTAG_PCHK_ERR: err_rpt hold
35	ROX	FIR14_DW_SET_REF_WITH_FLAG_IDLE_ERR: err_rpt hold
36	ROX	FIR14_KILL_REF_WITH_FLAG_IDLE_ERR: err_rpt hold
37	ROX	FIR14_HAMP_CNT_UNDERFLOW_ERR: err_rpt hold
38	ROX	FIR14_DW_SET_SI_BY_MACH: err_rpt hold
39	ROX	FIR14_PD_DIR_MULT_HIT: err_rpt hold
40	ROX	FIR14_B0_SD_DIR_MULT_HIT: err_rpt hold
41	ROX	FIR14_B1_SD_DIR_MULT_HIT: err_rpt hold
42	ROX	FIR14_HANG_WAITING_FOR_FP_MATE: err_rpt hold
43	ROX	FIR14_BAD_FP_MATE: err_rpt hold
44	ROX	FIR14_LSU_TAG_REUSE_ERR: err_rpt hold
45	ROX	FIR14_IFU_MULT_REQ_ERR: err_rpt hold



Bits	SCOM	Field Mnemonic: Description
46	ROX	FIR14_XPF_MULT_REQ_ERR: err_rpt hold
47	ROX	FIR14_XLT_TAG_REUSE_ERR: err_rpt hold
48	ROX	FIR14_L3PF_REQ_ERR: err_rpt hold
49	ROX	FIR14_NCU_TID_DONE_ERR: err_rpt hold
50:63	RO	constant=0b0000000000000000

Register Name	ERROR REPORT REGISTER0
Mnemonic	EXP.L2.L2MISC.L2CERRS.ERR_RPT1
Address	0000000010012816 (SCOM)
Attributes	
Description	

[illegible]

Register Name	Trace Array High Data Register
Mnemonic	EXP.EC.PC.PC_NW.TRACE0.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG
Address	0000000010012C00 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63

Register Name	Trace Array Low Data Register
Mnemonic	EXP.EC.PC.PC_NW.TRACE0.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG
Address	0000000010012C01 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95
32:41	ROX	TRACE_ADDRESS: Trace Address



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Bits	SCOM	Field Mnemonic: Description
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank
51	ROX	TRACE_LAST_BANK_VALID: Trace Last Bank Valid
52	ROX	TRACE_WRITE_ON_RUN: Trace Write-On-Run indicator
53	ROX	TRACE_RUNNING: Trace Run indicator
54:63	ROX	TRACE_HOLD_ADDRESS: Trace Hold Address (pointing to last entry)

Register Name	<i>Trace Array High Data Register</i>
Mnemonic	EXP.EC.PC.PC_NW.TRACE1.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG
Address	0000000010012C40 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63

Register Name	<i>Trace Array Low Data Register</i>
Mnemonic	EXP.EC.PC.PC_NW.TRACE1.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG
Address	0000000010012C41 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95
32:41	ROX	TRACE_ADDRESS: Trace Address
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank
51	ROX	TRACE_LAST_BANK_VALID: Trace Last Bank Valid
52	ROX	TRACE_WRITE_ON_RUN: Trace Write-On-Run indicator
53	ROX	TRACE_RUNNING: Trace Run indicator
54:63	ROX	TRACE_HOLD_ADDRESS: Trace Hold Address (pointing to last entry)

Register Name	<i>Trace Array High Data Register</i>
Mnemonic	EXP.EC.PC.PC_NW.TRACE2.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG
Address	0000000010012C80 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63



Register Name	<i>Trace Array Low Data Register</i>
Mnemonic	EXP.EC.PC.PC_NW.TRACE2.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG
Address	0000000010012C81 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95
32:41	ROX	TRACE_ADDRESS: Trace Address
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank
51	ROX	TRACE_LAST_BANK_VALID: Trace Last Bank Valid
52	ROX	TRACE_WRITE_ON_RUN: Trace Write-On-Run indicator
53	ROX	TRACE_RUNNING: Trace Run indicator
54:63	ROX	TRACE_HOLD_ADDRESS: Trace Hold Address (pointing to last entry)

Register Name	<i>Trace Array High Data Register</i>
Mnemonic	EXP.EC.PC.PC_NW.TRACE3.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG
Address	0000000010012CC0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63

Register Name	<i>Trace Array Low Data Register</i>
Mnemonic	EXP.EC.PC.PC_NW.TRACE3.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG
Address	0000000010012CC1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95
32:41	ROX	TRACE_ADDRESS: Trace Address
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank
51	ROX	TRACE_LAST_BANK_VALID: Trace Last Bank Valid
52	ROX	TRACE_WRITE_ON_RUN: Trace Write-On-Run indicator
53	ROX	TRACE_RUNNING: Trace Run indicator
54:63	ROX	TRACE_HOLD_ADDRESS: Trace Hold Address (pointing to last entry)



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Register Name	<i>Trace Array High Data Register</i>	
Mnemonic	EXP.EC.PC.PC_S.TRACE4.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	
Address	0000000010012D00 (SCOM)	
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63

Register Name	<i>Trace Array Low Data Register</i>	
Mnemonic	EXP.EC.PC.PC_S.TRACE4.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	
Address	0000000010012D01 (SCOM)	
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95
32:41	ROX	TRACE_ADDRESS: Trace Address
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank
51	ROX	TRACE_LAST_BANK_VALID: Trace Last Bank Valid
52	ROX	TRACE_WRITE_ON_RUN: Trace Write-On-Run indicator
53	ROX	TRACE_RUNNING: Trace Run indicator
54:63	ROX	TRACE_HOLD_ADDRESS: Trace Hold Address (pointing to last entry)

Register Name	<i>Trace Array High Data Register</i>	
Mnemonic	EXP.EC.PC.PC_S.TRACE5.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	
Address	0000000010012D40 (SCOM)	
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace Array Data 0:63

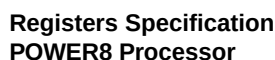
Register Name	<i>Trace Array Low Data Register</i>	
Mnemonic	EXP.EC.PC.PC_S.TRACE5.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	
Address	0000000010012D41 (SCOM)	
Attributes		
Description		



Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95
32:41	ROX	TRACE_ADDRESS: Trace Address
42:50	ROX	TRACE_LAST_BANK: Trace Last Bank
51	ROX	TRACE_LAST_BANK_VALID: Trace Last Bank Valid
52	ROX	TRACE_WRITE_ON_RUN: Trace Write-On-Run indicator
53	ROX	TRACE_RUNNING: Trace Run indicator
54:63	ROX	TRACE_HOLD_ADDRESS: Trace Hold Address (pointing to last entry)

Register Name	Direct Injects Into Logic - No Latches!!
Mnemonic	EXP.EC.PC.PC_NE.TCTL0.DIRECT_CONTROLS
Address	0000000010013000 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:41	RO	constant=0b0000000000000000000000000000000000000000
42	WOX_1P	Reserved field. (Access type is dc_prestart_sleep)
43	WOX_1P	Reserved field. (Access type is dc_prestart_winkle)
44	WOX_1P	Reserved field. (Access type is dc_clear_maint)
45	WOX_1P	Reserved field. (Access type is dc_ntc_flush)
46	RO	constant=0b0
47	WOX_1P	Reserved field. (Access type is dc_prestart_nap)
48	WOX_1P	Reserved field. (Access type is dc_cancel_lost)
49	WOX_1P	Reserved field. (Access type is dc_reset_maint)
50	RO	constant=0b0
51	WOX_1P	Reserved field. (Access type is dc_set_maint)
52	WOX_1P	Reserved field. (Access type is dc_goto_quiesce_state)
53	RO	constant=0b0
54:55	WOX_1P	Reserved field. (Access type is dc_inj_test_hang)
56	WOX_1P	Reserved field. (Access type is dc_core_running)
57	WOX_1P	Reserved field. (Access type is dc_hang_inject)
58	WOX_1P	Reserved field. (Access type is dc_smt_start_suppress)
59	RO	constant=0b0
60	WOX_1P	Reserved field. (Access type is dc_sreset_request)
61	WOX_1P	Reserved field. (Access type is dc_core_step)
62	WOX_1P	Reserved field. (Access type is dc_core_start)
63	WOX_1P	Reserved field. (Access type is dc_core_stop)



Bits	SCOM	Field Mnemonic: Description
0:42	RO	constant=0b00000000000000000000000000000000000000000000
43	RW	MR_THREAD_IN_DEBUG_MODE: enable logic which should run only in the lab: iTrace, debug_bus, FP0
44	RW	MR_PMON_INHIBIT: perfmon inhibit
45	RW	MR_FENCE_INTERRUPTS: SP fence interrupts
46	RW	MR_STOP_FETCH: SP stop fetch
47	RW	MR_STOP_PREFETCH: SP stop prefetch to LSU
48	RW	MR_STOP_DISPATCH: SP stop dispatch
49	RW	MR_SINGLE_DECODE: Single Instruction Decode Mode When setting this switch to one, also set switch mr_one_ppc_mode of the ras_modereg to one Function similar to HID0[4] single_decode except HID0[4] forces one ppc mode beneath the covers Before changing this bit, the thread must first be in maintenance mode (ref. direct_controls.mr_core_stop)
50	RW	MR_DO_SINGLE_MODE: Single Instruction Completion Mode Before changing this bit, the thread must first be in maintenance mode (ref. direct_controls.mr_core_stop)
51	RW	MR_ONE_PPC_MODE: One PPC instruction per group mode Before changing this bit, the thread must first be in maintenance mode (ref. direct_controls.mr_core_stop)
52:53	RW	MR_HANG_TEST_CTRL: hang test control, clear testhang
54:56	RW	MR_ATTEMPT_GPS_HR: attempt GPS hang recovery "1xx": attempt recovery on core hang "x1x": attempt recovery on nest hang "xx1": attempt recovery on ambiguous hang
57	RW	MR_HANG_DIS: disable hang detection and state-machine
58	RW	MR_ON_COREHNG: enable Debug Interrupt on core hang
59	RW	MR_ON_AMBIHNG: enable Debug Interrupt on ambi hang
60	RW	MR_ON_NESTHNG: enable Debug Interrupt on nest hang
61	RW	MR_RECOV_ENABLE: enable RECOVERY by SCOM
62	RW	MR_BLOCK_HMI_ON_MAINT: block hmi in maintenance mode
63	RW	MR_FENCE_INTR_ON_CHECKSTOP: allow interrupt of checkstop occurred

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Bits	SCOM	Field Mnemonic: Description
0:19	ROX	STAT: quiesce status 0 - entire row quiesced 1 - ISU is quiesced 2 - checkstop caused 3 - quiesce request by ISU 4 - ISU completed quiesced 5 - ISU quiesced by ATTN instr 6 - ISU quiesce by LSU DABR dbg mode 7 - ISU gct is empty (safe indication) 8 - ISU srq is empty (safe indication) 9 - LSU has no outstanding transactions to GPS 10 - LSU quiesced AND GUS idle 11 - Completion stopped by checkstop 12 - Group/Inst Completed since last maint op 13 - NTC flush not sace and caused checkstop 14 - Demand ifetch from IFU pending 15 - eat is empty 16 - nest active determination 17 - nest active determination 18 - nest active determination 19 - enable stop dispatch after 1st SCOM start happens
20	ROX	Reserved field. (Access type is por_state)
21	ROX	Reserved field. (Access type is core_maint_mode)
22	ROX	Reserved field. (Access type is pmc_quiesce_req)
23	ROX	OTHER_THREAD_ACTIVE: any other thread is active, hang control wise
24:26	ROX	HANG_FSM: hang recovery FSM state: good bad worse lost
27	RO	constant=0b0
28	ROX	HANG_HIST0: intelligent hang detected as core or ambiguous hang since last sp_cancel_lost
29	ROX	HANG_HIST1: intelligent hang detected as nest or ambiguous hang since last sp_cancel_lost
30	ROX	HANG_HIST2: hang_state bad was entered since last sp_cancel_lost
31	ROX	HANG_HIST3: hang_state lost was entered since last sp_cancel_lost
32	RO	constant=0b0
33:40	ROX	HR_COMP_CNT: hang recovery completion counter
41	ROX	SMT_DEAD_STOP: SMT dead stop
42	ROX	STOP_FETCH: stop fetch
43	ROX	STOP_DISPATCH: stop dispatch
44	ROX	STOP_COMPLETION: stop completion
45	ROX	HOLD_DECODE: hold decode
46	ROX	Reserved field. (Access type is ext_intr_pending)
47	ROX	Reserved field. (Access type is isu_lsu_empty_internal)
48	ROX	THREAD_ENABLED: this thread was enabled by PMC when reading status

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Bits	SCOM	Field Mnemonic: Description
49:52	ROX	POW_STATUS_THREAD_STATE: Thread state: quiesce => 0b1000 starting => 0b0100 run => 0b0010 stopping => 0b0001 Values: QUIESCE=>0b1000 STARTING=>0b0100 RUN=>0b0010 STOPPING=>0b0001
53	RO	constant=0b0 Values: QUIESCE=>0b1000 STARTING=>0b0100 RUN=>0b0010 STOPPING=>0b0001
54	ROX	MAINT_SINGLE_MODE: maintenance single instruction mode
55	RO	constant=0b0
56	ROX	Reserved field. (Access type is core_step_or_resume_pending)
57:63	RO	constant=0b0000000

Register Name	<i>Hang Recovery Control Register</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL0.HANG_CONTROL
Address	0000000010013003 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	CORE_HANG_LIMIT: core hang limit hang_ctrl(0 to 7); init = 0x9F = 3 hang pulses
8:15	RW	NEST_HANG_LIMIT: GPS hang limit hang_ctrl(8 to 15); init = 0x2D = 100 hang pulses
16:18	RW	FLUSH_TIMEOUT_MODE: flush timeout mode ntc_mode_none => 0b000 ntc_stephang_mode => 0b001 ntc_chkstp_mode => 0b010 ntc_attn_mode => 0b100 ntc_quiesce_mode => 0b011 Values: NTC_MODE_NONE=>0b000 NTC_STEPHANG_MODE=>0b001 NTC_CHKSTP_MODE=>0b010 NTC_ATTN_MODE=>0b100 NTC_QUIESCE_MODE=>0b011
19:28	RW	FLUSH_LIMIT: ntc flush counter timeout limit
29	RW	NTC_TIMED_OUT_MODE: enablentc timeout counter action
30	RW	RETURN_GOOD_ON_COMP: return good on completion without waiting for a hang_pulse after seen completion

Bits	SCOM	Field Mnemonic: Description
31	RW	ANY_GROUP_MODE: any group mode
32:39	RW	COMP_CNT_LIMIT_LT: completion count mode
40	RW	EN_RAND_NTC_FLUSH: enable random ntc flushes using random_pulse
41:42	RW	Reserved field. (Access type is hr_spare)
43:50	RW	ACTIVE_MASK_LT: active mask latch for hang condition enable/disable
51:58	RW	TLBIE_STALL_LIMIT: tlbie stall limit hang_ctrl(51 to 58); init = 0x99 = 50 hang pulses
59:63	RO	constant=0b000000

Register Name	<i>Power Management Status Register</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL0.POW_STATUS
Address	0000000010013004 (SCOM)
Attributes	
Description	For Debug : (0:1 - Thread State, 2:3- Power State, 6:8 - SMT Mode, 9:15 - IRQ Nodoze/ext/decr/debug/hdec/pmon/sp_att, 16:19 - Sreset_type, 20 - Sreset Pending, 21 - DBG Fetch Stop, 22 - Async Pending, 23:25 - PMC Pm_state, 26:29 - Quiesce Arbitration State, 30:33 - PMC To Pow Spare)

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	POW_STATUS_THREAD_STATE: Thread state: quiesce => 0b1000 starting => 0b0100 run => 0b0010 stopping => 0b0001 Values: QUIESCE=>0b1000 STARTING=>0b0100 RUN=>0b0010 STOPPING=>0b0001
4:5	ROX	PMC_POW_STATE: 00 - run, 01 - doze, 10 - nap, 11 - sleep/winkle Values: RUN=>0b00 DOZE=>0b01 NAP=>0b10 SLEEP=>0b11
6:8	ROX	PMC_SMT_MODE: 00 - power_on_ST, 01 - ST, 10 - SMT2, 11 - SMT4 Values: POWER_ON_ST=>0b000 ST=>0b001 SMT2_SH=>0b010 SMT2_SP=>0b011 SMT4=>0b100 SMT8=>0b101
9	ROX	HMI_INTR: hardware maintenance interrupt
10	ROX	Reserved field. (Access type is ext_intr)
11	ROX	DECR_INTR: decremter interrupt
12	ROX	Reserved field. (Access type is debug_intr)
13	ROX	HDEC_INTR: hypervisor decremter interrupt

Registers Specification

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Bits	SCOM	Field Mnemonic: Description
14	ROX	Reserved field. (Access type is pmu_intr)
15	ROX	SP_ATTN_INTR: special attention interrupt
16:18	ROX	SRESET_TYPE: one of the switches and ldi to set to force sreset through scan sreset_null => 0b000 sreset_req_and_thr_en => 0b001 sreset_req_and_thr_disa => 0b010 decr_intr_and_thr_disa => 0b011 ext_intr_and_thr_disa => 0b100 hmi_intr_and_thr_disa => 0b101 sdi_intr_and_thr_disa => 0b110 awake_from_sleep => 0b111 Values: SRESET_NULL=>0b000 SRESET_REQ_AND_THR_EN=>0b001 SRESET_REQ_AND_THR_DISA=>0b010 DECR_INTR_AND_THR_DISA=>0b011 EXT_INTR_AND_THR_DISA=>0b100 HMI_INTR_AND_THR_DISA=>0b101 SDI_INTR_AND_THR_DISA=>0b110 AWAKE_FROM_SLEEP=>0b111
19	ROX	Reserved field. (Access type is sreset_type) Values: SRESET_NULL=>0b000 SRESET_REQ_AND_THR_EN=>0b001 SRESET_REQ_AND_THR_DISA=>0b010 DECR_INTR_AND_THR_DISA=>0b011 EXT_INTR_AND_THR_DISA=>0b100 HMI_INTR_AND_THR_DISA=>0b101 SDI_INTR_AND_THR_DISA=>0b110 AWAKE_FROM_SLEEP=>0b111
20	ROX	SRESET_PENDING: one of the switches and ldi to set to force sreset through scan
21	ROX	DBG_FETCH_STOP: pause fetching for debug workaround
22	ROX	ASYNCR_PENDING: asynchronous interrupt pending
23:25	ROX	CORE_POW_STATE: 000: run 100: doze 101: nap 110: sleep 111: rvinkle
26:29	ROX	Reserved field. (Access type is qui_arb_state_one_hot)
30:33	ROX	PMC_TCTL_SPARE: 4 spare pins
34:63	RO	constant=0b00000000000000000000000000000000

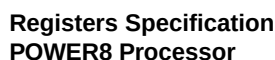
Register Name	SPATTN Register
Mnemonic	EXP.EC.PC.PC_NE.TCTL0.SPATTN
Address	0000000010013005 (SCOM1) 0000000010013006 (SCOM2) 0000000010013007 (SCOM)
Attributes	
Description	

[illegible]

Register Name	SPATTN_MASK Register
Mnemonic	EXP.EC.PC.PC_NE.TCTL0.SPATTN_MASK
Address	0000000010013008 (SCOM)
Attributes	
Description	

[illegible]

Register Name	SDI Register
Mnemonic	EXP.EC.PC.PC_NE.TCTL0.SDI
Address	0000000010013009 (SCOM1) 000000001001300A (SCOM2) 000000001001300B (SCOM)
Attributes	
Description	



Register Name	SDI_MASK Register
Mnemonic	EXP.EC.PC.PC_NE.TCTL0.SDI_MASK
Address	000000001001300C (SCOM)
Attributes	
Description	

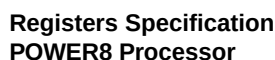
[illegible]

Register Name	PC_NE Error Report Hold_out Register0
Mnemonic	EXP.EC.PC.PC_NE.PCNE_REG0_HOLD_OUT
Address	000000001001300D (SCOM)
Attributes	
Description	

[illegible]

Register Name	Direct Injects Into Logic - No Latches!!
Mnemonic	EXP.EC.PC.PC_NE.TCTL1.DIRECT_CONTROLS
Address	0000000010013010 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:41	RO	constant=0b0000000000000000000000000000000000000000
42	WOX_1P	Reserved field. (Access type is dc_prestart_sleep)
43	WOX_1P	Reserved field. (Access type is dc_prestart_winkle)
44	WOX_1P	Reserved field. (Access type is dc_clear_maint)
45	WOX_1P	Reserved field. (Access type is dc_ntc_flush)
46	RO	constant=0b0
47	WOX_1P	Reserved field. (Access type is dc_prestart_nap)
48	WOX_1P	Reserved field. (Access type is dc_cancel_lost)
49	WOX_1P	Reserved field. (Access type is dc_reset_maint)
50	RO	constant=0b0
51	WOX_1P	Reserved field. (Access type is dc_set_maint)
52	WOX_1P	Reserved field. (Access type is dc_goto_quiesce_state)
53	RO	constant=0b0
54:55	WOX_1P	Reserved field. (Access type is dc_inj_test_hang)
56	WOX_1P	Reserved field. (Access type is dc_core_running)
57	WOX_1P	Reserved field. (Access type is dc_hang_inject)
58	WOX_1P	Reserved field. (Access type is dc_smt_start_suppress)
59	RO	constant=0b0
60	WOX_1P	Reserved field. (Access type is dc_sreset_request)





Register Name	<i>Ra Status</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL1.RAS_STATUS
Address	0000000010013012 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:19	ROX	STAT: quiesce status 0 - entire row quiesced 1 - ISU is quiesced 2 - checkstop caused 3 - quiesce request by ISU 4 - ISU completed quiesced 5 - ISU quiesced by ATTN instr 6 - ISU quiesce by LSU DABR dbg mode 7 - ISU gct is empty (safe indication) 8 - ISU srq is empty (safe indication) 9 - LSU has no outstanding transactions to GPS 10 - LSU quiesced AND GUS idle 11 - Completion stopped by checkstop 12 - Group/Inst Completed since last maint op 13 - NTC flush not sace and caused checkstop 14 - Demand ifetch from IFU pending 15 - eat is empty 16 - nest active determination 17 - nest active determination 18 - nest active determination 19 - enable stop dispatch after 1st SCOM start happens
20	ROX	Reserved field. (Access type is por_state)
21	ROX	Reserved field. (Access type is core_maint_mode)
22	ROX	Reserved field. (Access type is pmc_quiesce_req)
23	ROX	OTHER_THREAD_ACTIVE: any other thread is active, hang control wise
24:26	ROX	HANG_FSM: hang recovery FSM state: good bad worse lost
27	RO	constant=0b0
28	ROX	HANG_HIST0: intelligent hang detected as core or ambiguous hang since last sp_cancel_lost
29	ROX	HANG_HIST1: intelligent hang detected as nest or ambiguous hang since last sp_cancel_lost
30	ROX	HANG_HIST2: hang_state bad was entered since last sp_cancel_lost
31	ROX	HANG_HIST3: hang_state lost was entered since last sp_cancel_lost
32	RO	constant=0b0
33:40	ROX	HR_COMP_CNT: hang recovery completion counter
41	ROX	SMT_DEAD_STOP: SMT dead stop
42	ROX	STOP_FETCH: stop fetch
43	ROX	STOP_DISPATCH: stop dispatch
44	ROX	STOP_COMPLETION: stop completion
45	ROX	HOLD_DECODE: hold decode
46	ROX	Reserved field. (Access type is ext_intr_pending)
47	ROX	Reserved field. (Access type is isu_isu_empty_internal)

Registers Specification

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Bits	SCOM	Field Mnemonic: Description
48	ROX	THREAD_ENABLED: this thread was enabled by PMC when reading status
49:52	ROX	POW_STATUS_THREAD_STATE: Thread state: quiesce => 0b1000 starting => 0b0100 run => 0b0010 stopping => 0b0001 Values: QUIESCE=>0b1000 STARTING=>0b0100 RUN=>0b0010 STOPPING=>0b0001
53	RO	constant=0b0 Values: QUIESCE=>0b1000 STARTING=>0b0100 RUN=>0b0010 STOPPING=>0b0001
54	ROX	MAINT_SINGLE_MODE: maintenance single instruction mode
55	RO	constant=0b0
56	ROX	Reserved field. (Access type is core_step_or_resume_pending)
57:63	RO	constant=0b0000000

Register Name	<i>Hang Recovery Control Register</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL1.HANG_CONTROL
Address	0000000010013013 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	CORE_HANG_LIMIT: core hang limit hang_ctrl(0 to 7); init = 0x9F = 3 hang pulses
8:15	RW	NEST_HANG_LIMIT: GPS hang limit hang_ctrl(8 to 15); init = 0x2D = 100 hang pulses
16:18	RW	FLUSH_TIMEOUT_MODE: flush timeout mode ntc_mode_none => 0b000 ntc_stephang_mode => 0b001 ntc_chkstp_mode => 0b010 ntc_attn_mode => 0b100 ntc_quiesce_mode => 0b011 Values: NTC_MODE_NONE=>0b000 NTC_STEPHANG_MODE=>0b001 NTC_CHKSTP_MODE=>0b010 NTC_ATTEN_MODE=>0b100 NTC_QUIESCE_MODE=>0b011
19:28	RW	FLUSH_LIMIT: ntc flush counter timeout limit
29	RW	NTC_TIMED_OUT_MODE: enablentc timeout counter action



Bits	SCOM	Field Mnemonic: Description
30	RW	RETURN_GOOD_ON_COMP: return good on completion without waiting for a hang_pulse after seen completion
31	RW	ANY_GROUP_MODE: any group mode
32:39	RW	COMP_CNT_LIMIT_LT: completion count mode
40	RW	EN_RAND_NTC_FLUSH: enable random ntc flushes using random_pulse
41:42	RW	Reserved field. (Access type is hr_spare)
43:50	RW	ACTIVE_MASK_LT: active mask latch for hang condition enable/disable
51:58	RW	TLBIE_STALL_LIMIT: tlbie stall limit hang_ctrl(51 to 58); init = 0x99 = 50 hang pulses
59:63	RO	constant=0b00000

Register Name	Power Management Status Register For Debug
Mnemonic	EXP.EC.PC.PC_NE.TCTL1.POW_STATUS
Address	0000000010013014 (SCOM)
Attributes	
Description	0:1 - Thread State, 2:3- Power State, 6:8 - SMT Mode, 9:15 - IRQ Nodoze/ext/decr/debug/hdec/pmon/sp_att, 16:19 - Sreset_type, 20 - Sreset Pending, 21 - DBG Fetch Stop, 22 - Async Pending, 23:25 - PMC Pm_state, 26:29 - Quiesce Arbitration State, 30:33 - PMC To Pow Spare

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	POW_STATUS_THREAD_STATE: Thread state: quiesce => 0b1000 starting => 0b0100 run => 0b0010 stopping => 0b0001 Values: QUIESCE=>0b1000 STARTING=>0b0100 RUN=>0b0010 STOPPING=>0b0001
4:5	ROX	PMC_POW_STATE: 00 - run, 01 - doze, 10 - nap, 11 - sleep/winkle Values: RUN=>0b00 DOZE=>0b01 NAP=>0b10 SLEEP=>0b11
6:8	ROX	PMC_SMT_MODE: 00 - power_on_ST, 01 - ST, 10 - SMT2, 11 - SMT4 Values: POWER_ON_ST=>0b000 ST=>0b001 SMT2_SH=>0b010 SMT2_SP=>0b011 SMT4=>0b100 SMT8=>0b101
9	ROX	HMI_INTR: hardware maintenance interrupt
10	ROX	Reserved field. (Access type is ext_intr)
11	ROX	DECR_INTR: decrementer interrupt

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
12	ROX	Reserved field. (Access type is debug_intr)
13	ROX	HDEC_INTR: hypervisor decremter interrupt
14	ROX	Reserved field. (Access type is pmu_intr)
15	ROX	SP_ATTN_INTR: special attention interrupt
16:18	ROX	SRESET_TYPE: one of the switches and ldial to set to force sreset through scan sreset_null => 0b000 sreset_req_and_thr_en => 0b001 sreset_req_and_thr_disa => 0b010 decr_intr_and_thr_disa => 0b011 ext_intr_and_thr_disa => 0b100 hmi_intr_and_thr_disa => 0b101 sdi_intr_and_thr_disa => 0b110 awake_from_sleep => 0b111 Values: SRESET_NULL=>0b000 SRESET_REQ_AND_THR_EN=>0b001 SRESET_REQ_AND_THR_DISA=>0b010 DECR_INTR_AND_THR_DISA=>0b011 EXT_INTR_AND_THR_DISA=>0b100 HMI_INTR_AND_THR_DISA=>0b101 SDI_INTR_AND_THR_DISA=>0b110 AWAKE_FROM_SLEEP=>0b111
19	ROX	Reserved field. (Access type is sreset_type) Values: SRESET_NULL=>0b000 SRESET_REQ_AND_THR_EN=>0b001 SRESET_REQ_AND_THR_DISA=>0b010 DECR_INTR_AND_THR_DISA=>0b011 EXT_INTR_AND_THR_DISA=>0b100 HMI_INTR_AND_THR_DISA=>0b101 SDI_INTR_AND_THR_DISA=>0b110 AWAKE_FROM_SLEEP=>0b111
20	ROX	SRESET_PENDING: one of the switches and ldial to set to force sreset through scan
21	ROX	DBG_FETCH_STOP: pause fetching for debug workaround
22	ROX	ASYNC_PENDING: asynchronous interrupt pending
23:25	ROX	CORE_POW_STATE: 000: run 100: doze 101: nap 110: sleep 111: rvwinkle
26:29	ROX	Reserved field. (Access type is qui_arb_state_one_hot)
30:33	ROX	PMC_TCTL_SPARE: 4 spare pins
34:63	RO	constant=0b00000000000000000000000000000000



Register Name	<i>SPATTN Register</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL1.SPATTN
Address	0000000010013015 (SCOM1) 0000000010013016 (SCOM2) 0000000010013017 (SCOM)
Attributes	
Description	

[illegible]

Register Name	SPATTN_MASK Register
Mnemonic	EXP.EC.PC.PC_NE.TCTL1.SPATTN_MASK
Address	0000000010013018 (SCOM)
Attributes	
Description	

[illegible]

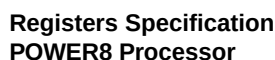


Register Name	PC_NE Error Report Hold_out Register1
Mnemonic	EXP.EC.PC.PC_NE.PCNE_REG1_HOLD_OUT
Address	000000001001301D (SCOM)
Attributes	
Description	

[illegible]

Register Name	Direct Injects Into Logic - No Latches!!
Mnemonic	EXP.EC.PC.PC_NE.TCTL2.DIRECT_CONTROLS
Address	0000000010013020 (SCOM)
Attributes	
Description	

[illegible]





Bits	SCOM	Field Mnemonic: Description
59	RW	MR_ON_AMBIHNG: enable Debug Interrupt on ambi hang
60	RW	MR_ON_NESTHNG: enable Debug Interrupt on nest hang
61	RW	MR_RECOV_ENABLE: enable RECOVERY by SCOM
62	RW	MR_BLOCK_HMI_ON_MAINT: block hmi in maintenance mode
63	RW	MR_FENCE_INTR_ON_CHECKSTOP: allow interrupt of checkstop occurred

Register Name	Ra Status
Mnemonic	EXP.EC.PC.PC_NE.TCTL2.RAS_STATUS
Address	0000000010013022 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:19	ROX	STAT: quiesce status 0 - entire row quiesced 1 - ISU is quiesced 2 - checkstop caused 3 - quiesce request by ISU 4 - ISU completed quiesced 5 - ISU quiesced by ATTN instr 6 - ISU quiesce by LSU DABR dbg mode 7 - ISU gct is empty (safe indication) 8 - ISU srq is empty (safe indication) 9 - LSU has no outstanding transactions to GPS 10 - LSU quiesced AND GUS idle 11 - Completion stopped by checkstop 12 - Group/Inst Completed since last maint op 13 - NTC flush not sace and caused checkstop 14 - Demand ifetch from IFU pending 15 - eat is empty 16 - nest active determination 17 - nest active determination 18 - nest active determination 19 - enable stop dispatch after 1st SCOM start happens
20	ROX	Reserved field. (Access type is por_state)
21	ROX	Reserved field. (Access type is core_maint_mode)
22	ROX	Reserved field. (Access type is pmc_quiesce_req)
23	ROX	OTHER_THREAD_ACTIVE: any other thread is active, hang control wise
24:26	ROX	HANG_FSM: hang recovery FSM state: good bad worse lost
27	RO	constant=0b0
28	ROX	HANG_HIST0: intelligent hang detected as core or ambiguous hang since last sp_cancel_lost
29	ROX	HANG_HIST1: intelligent hang detected as nest or ambiguous hang since last sp_cancel_lost
30	ROX	HANG_HIST2: hang_state bad was entered since last sp_cancel_lost
31	ROX	HANG_HIST3: hang_state lost was entered since last sp_cancel_lost
32	RO	constant=0b0
33:40	ROX	HR_COMP_CNT: hang recovery completion counter

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
41	ROX	SMT_DEAD_STOP: SMT dead stop
42	ROX	STOP_FETCH: stop fetch
43	ROX	STOP_DISPATCH: stop dispatch
44	ROX	STOP_COMPLETION: stop completion
45	ROX	HOLD_DECODE: hold decode
46	ROX	Reserved field. (Access type is ext_intr_pending)
47	ROX	Reserved field. (Access type is isu_isu_empty_internal)
48	ROX	THREAD_ENABLED: this thread was enabled by PMC when reading status
49:52	ROX	POW_STATUS_THREAD_STATE: Thread state: quiesce => 0b1000 starting => 0b0100 run => 0b0010 stopping => 0b0001 Values: QUIESCE=>0b1000 STARTING=>0b0100 RUN=>0b0010 STOPPING=>0b0001
53	RO	constant=0b0 Values: QUIESCE=>0b1000 STARTING=>0b0100 RUN=>0b0010 STOPPING=>0b0001
54	ROX	MAINT_SINGLE_MODE: maintenance single instruction mode
55	RO	constant=0b0
56	ROX	Reserved field. (Access type is core_step_or_resume_pending)
57:63	RO	constant=0b0000000

Register Name		Hang Recovery Control Register
Mnemonic		EXP.EC.PC.PC_NE.TCTL2.HANG_CONTROL
Address		0000000010013023 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:7	RW	CORE_HANG_LIMIT: core hang limit hang_ctrl(0 to 7); init = 0x9F = 3 hang pulses
8:15	RW	NEST_HANG_LIMIT: GPS hang limit hang_ctrl(8 to 15); init = 0x2D = 100 hang pulses

Bits	SCOM	Field Mnemonic: Description
16:18	RW	FLUSH_TIMEOUT_MODE: flush timeout mode ntc_mode_none => 0b000 ntc_stephang_mode => 0b001 ntc_chkstp_mode => 0b010 ntc_attn_mode => 0b100 ntc_quiesce_mode => 0b011 Values: NTC_MODE_NONE=>0b000 NTC_STEPHANG_MODE=>0b001 NTC_CHKSTP_MODE=>0b010 NTC_ATTN_MODE=>0b100 NTC_QUIESCE_MODE=>0b011
19:28	RW	FLUSH_LIMIT: ntc flush counter timeout limit
29	RW	NTC_TIMED_OUT_MODE: enablentc timeout counter action
30	RW	RETURN_GOOD_ON_COMP: return good on completion without waiting for a hang_pulse after seen completion
31	RW	ANY_GROUP_MODE: any group mode
32:39	RW	COMP_CNT_LIMIT_LT: completion count mode
40	RW	EN_RAND_NTC_FLUSH: enable random ntc flushes using random_pulse
41:42	RW	Reserved field. (Access type is hr_spare)
43:50	RW	ACTIVE_MASK_LT: active mask latch for hang condition enable/disable
51:58	RW	TLBIE_STALL_LIMIT: tlbie stall limit hang_ctrl(51 to 58); init = 0x99 = 50 hang pulses
59:63	RO	constant=0b00000

Register Name	<i>Power Management Status Register For Debug</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL2.POW_STATUS
Address	0000000010013024 (SCOM)
Attributes	
Description	(0:1 - Thread State, 2:3- Power State, 6:8 - SMT Mode, 9:15 - IRQ Nodoe/ext/decr/debug/hdec/pmon/sp_att, 16:19 - Sreset_type, 20 - Sreset Pending, 21 - DBG Fetch Stop, 22 - Async Pending, 23:25 - PMC Pm_state, 26:29 - Quiesce Arbitration State, 30:33 - PMC To Pow Spare)

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	POW_STATUS_THREAD_STATE: Thread state: quiesce => 0b1000 starting => 0b0100 run => 0b0010 stopping => 0b0001 Values: QUIESCE=>0b1000 STARTING=>0b0100 RUN=>0b0010 STOPPING=>0b0001

Registers Specification

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Bits	SCOM	Field Mnemonic: Description
4:5	ROX	PMC_POW_STATE: 00 - run, 01 - doze, 10 - nap, 11 - sleep/winkle Values: RUN=>0b00 DOZE=>0b01 NAP=>0b10 SLEEP=>0b11
6:8	ROX	PMC_SMT_MODE: 00 - power_on_ST, 01 - ST, 10 - SMT2, 11 - SMT4 Values: POWER_ON_ST=>0b000 ST=>0b001 SMT2_SH=>0b010 SMT2_SP=>0b011 SMT4=>0b100 SMT8=>0b101
9	ROX	HMI_INTR: hardware maintenance interrupt
10	ROX	Reserved field. (Access type is ext_intr)
11	ROX	DECR_INTR: decrementer interrupt
12	ROX	Reserved field. (Access type is debug_intr)
13	ROX	HDEC_INTR: hypervisor decrementer interrupt
14	ROX	Reserved field. (Access type is pmu_intr)
15	ROX	SP_ATTN_INTR: special attention interrupt
16:18	ROX	SRESET_TYPE: one of the switches and ldi to set to force sreset through scan sreset_null => 0b000 sreset_req_and_thr_en => 0b001 sreset_req_and_thr_disa => 0b010 decr_intr_and_thr_disa => 0b011 ext_intr_and_thr_disa => 0b100 hmi_intr_and_thr_disa => 0b101 sdi_intr_and_thr_disa => 0b110 awake_from_sleep => 0b111 Values: SRESET_NULL=>0b000 SRESET_REQ_AND_THR_EN=>0b001 SRESET_REQ_AND_THR_DISA=>0b010 DECR_INTR_AND_THR_DISA=>0b011 EXT_INTR_AND_THR_DISA=>0b100 HMI_INTR_AND_THR_DISA=>0b101 SDI_INTR_AND_THR_DISA=>0b110 AWAKE_FROM_SLEEP=>0b111
19	ROX	Reserved field. (Access type is sreset_type) Values: SRESET_NULL=>0b000 SRESET_REQ_AND_THR_EN=>0b001 SRESET_REQ_AND_THR_DISA=>0b010 DECR_INTR_AND_THR_DISA=>0b011 EXT_INTR_AND_THR_DISA=>0b100 HMI_INTR_AND_THR_DISA=>0b101 SDI_INTR_AND_THR_DISA=>0b110 AWAKE_FROM_SLEEP=>0b111
20	ROX	SRESET_PENDING: one of the switches and ldi to set to force sreset through scan
21	ROX	DBG_FETCH_STOP: pause fetching for debug workaround
22	ROX	ASYNC_PENDING: asynchronous interrupt pending



Bits	SCOM	Field Mnemonic: Description
23:25	ROX	CORE_POW_STATE: 000: run 100: doze 101: nap 110: sleep 111: rwinkle
26:29	ROX	Reserved field. (Access type is qui_arb_state_one_hot)
30:33	ROX	PMC_TCTL_SPARE: 4 spare pins
34:63	RO	constant=0b00000000000000000000000000000000

Register Name	<i>SPATTN Register</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL2.SPATTN
Address	0000000010013025 (SCOM1) 0000000010013026 (SCOM2) 0000000010013027 (SCOM)
Attributes	
Description	

[illegible]

Register Name	SPATTN_MASK Register
Mnemonic	EXP.EC.PC.PC_NE.TCTL2.SPATTN_MASK
Address	0000000010013028 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	SPATTN_CORE_CODE_TO_SP_MSK: Mask of Core code to service processor
1	RW	SPATTN_ATTN_COMPLETE_MSK: Mask of SP-ATTN instruction

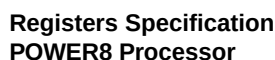


Bits	SCOM	Field Mnemonic: Description
0	RW	SDI_SW_USE_1_MSK: Mask of sw_use_1 - Available for use by Service Processor to get attention of the hypervisor
1	RW	SDI_SW_USE_2_MSK: Mask of sw_use_2 - Available for use by Service Processor to get attention of the hypervisor
2	RW	SDI_SW_USE_3_MSK: Mask of sw_use_3 - Available for use by Service Processor to get attention of the hypervisor
3	RW	SDI_HANG_RECV_OR_CHSW QUIESCE_TIMEOUT_MSK: Mask of Hang Recovery or chsw Quiesce Timeout
4	RW	SDI_EXT_TRIGGER_MSK: Mask of RAS trigger
5	RW	SDI_COREHANG_MSK: Mask of Thread Hang with CORE Source indication (modeable)
6	RW	SDI_AMBIHANG_MSK: Mask of Thread Hang with AMBIGUOUS Source indication (modeable)
7	RW	SDI_NESTHANG_MSK: Mask of Thread Hang with NEST Source indication (modeable)
8:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	PC_NE Error Report Hold_out Register2
Mnemonic	EXP.EC.PC.PC_NE.PCNE_REG2_HOLD_OUT
Address	000000001001302D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is TCTL2_ASYNC_INT_IN_RAM_hold_out)
1	ROX	Reserved field. (Access type is TCTL2_ATTNREG_PARITY_hold_out)
2	ROX	Reserved field. (Access type is TCTL2_DIREG_PARITY_hold_out)
3	ROX	Reserved field. (Access type is TCTL2_HANG_STATE_BAD_hold_out)
4	ROX	Reserved field. (Access type is TCTL2_HANG_STATE_LOST_hold_out)
5	ROX	Reserved field. (Access type is TCTL2_MY_SRESET_hold_out)
6	ROX	Reserved field. (Access type is TCTL2_PPC_COMPLETE_hold_out)
7	ROX	Reserved field. (Access type is TCTL2_RECOV_IN_MAINT_hold_out)
8	ROX	Reserved field. (Access type is TCTL2_DC_CORE_STEP_hold_out)
9	RO	constant=0b0
10:12	ROX	Reserved field. (Access type is TCTL2_THREAD_HANG_hold_out)
13:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	Direct Injects Into Logic - No Latches!!
Mnemonic	EXP.EC.PC.PC_NE.TCTL3.DIRECT_CONTROLS
Address	0000000010013030 (SCOM)
Attributes	
Description	



Register Name	<i>RAS Mode Register</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL3.RAS_MODEREG
Address	0000000010013031 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:42	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000
43	RW	MR_THREAD_IN_DEBUG_MODE: enable logic which should run only in the lab: iTrace, debug_bus, FP0
44	RW	MR_PMON_INHIBIT: perfmon inhibit
45	RW	MR_FENCE_INTERRUPTS: SP fence interrupts
46	RW	MR_STOP_FETCH: SP stop fetch
47	RW	MR_STOP_PREFETCH: SP stop prefetch to LSU
48	RW	MR_STOP_DISPATCH: SP stop dispatch

Bits	SCOM	Field Mnemonic: Description
49	RW	MR_SINGLE_DECODE: Single Instruction Decode Mode When setting this switch to one, also set switch mr_one_ppc_mode of the ras_modereg to one Function similar to HID0[4] single_decode except HID0[4] forces one ppc mode beneath the covers Before changing this bit, the thread must first be in maintenance mode (ref. direct_controls.mr_core_stop)
50	RW	MR_DO_SINGLE_MODE: Single Instruction Completion Mode Before changing this bit, the thread must first be in maintenance mode (ref. direct_controls.mr_core_stop)
51	RW	MR_ONE_PPC_MODE: One PPC instruction per group mode Before changing this bit, the thread must first be in maintenance mode (ref. direct_controls.mr_core_stop)
52:53	RW	MR_HANG_TEST_CTRL: hang test control, clear testhang
54:56	RW	MR_ATTEMPT_GPS_HR: attempt GPS hang recovery "1xx": attempt recovery on core hang "x1x": attempt recovery on nest hang "xx1": attempt recovery on ambiguous hang
57	RW	MR_HANG_DIS: disable hang detection and state-machine
58	RW	MR_ON_COREHNG: enable Debug Interrupt on core hang
59	RW	MR_ON_AMBIHNG: enable Debug Interrupt on ambi hang
60	RW	MR_ON_NESTHNG: enable Debug Interrupt on nest hang
61	RW	MR_RECOV_ENABLE: enable RECOVERY by SCOM
62	RW	MR_BLOCK_HMI_ON_MAINT: block hmi in maintenance mode
63	RW	MR_FENCE_INTR_ON_CHECKSTOP: allow interrupt of checkstop occurred

Register Name	<i>Ra Status</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL3.RAS_STATUS
Address	0000000010013032 (SCOM)
Attributes	
Description	

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
0:19	ROX	STAT: quiesce status 0 - entire row quiesced 1 - ISU is quiesced 2 - checkstop caused 3 - quiesce request by ISU 4 - ISU completed quiesced 5 - ISU quiesced by ATTN instr 6 - ISU quiesce by LSU DABR dbg mode 7 - ISU gct is empty (safe indication) 8 - ISU srq is empty (safe indication) 9 - LSU has no outstanding transactions to GPS 10 - LSU quiesced AND GUS idle 11 - Completion stopped by checkstop 12 - Group/Inst Completed since last maint op 13 - NTC flush not sace and caused checkstop 14 - Demand ifetch from IFU pending 15 - eat is empty 16 - nest active determination 17 - nest active determination 18 - nest active determination 19 - enable stop dispatch after 1st SCOM start happens
20	ROX	Reserved field. (Access type is por_state)
21	ROX	Reserved field. (Access type is core_maint_mode)
22	ROX	Reserved field. (Access type is pmc_quiesce_req)
23	ROX	OTHER_THREAD_ACTIVE: any other thread is active, hang control wise
24:26	ROX	HANG_FSM: hang recovery FSM state: good bad worse lost
27	RO	constant=0b0
28	ROX	HANG_HIST0: intelligent hang detected as core or ambiguous hang since last sp_cancel_lost
29	ROX	HANG_HIST1: intelligent hang detected as nest or ambiguous hang since last sp_cancel_lost
30	ROX	HANG_HIST2: hang_state bad was entered since last sp_cancel_lost
31	ROX	HANG_HIST3: hang_state lost was entered since last sp_cancel_lost
32	RO	constant=0b0
33:40	ROX	HR_COMP_CNT: hang recovery completion counter
41	ROX	SMT_DEAD_STOP: SMT dead stop
42	ROX	STOP_FETCH: stop fetch
43	ROX	STOP_DISPATCH: stop dispatch



Bits	SCOM	Field Mnemonic: Description
44	ROX	STOP_COMPLETION: stop completion
45	ROX	HOLD_DECODE: hold decode
46	ROX	Reserved field. (Access type is ext_intr_pending)
47	ROX	Reserved field. (Access type is isu_isu_empty_internal)
48	ROX	THREAD_ENABLED: this thread was enabled by PMC when reading status
49:52	ROX	POW_STATUS_THREAD_STATE: Thread state: quiesce => 0b1000 starting => 0b0100 run => 0b0010 stopping => 0b0001 Values: QUIESCE=>0b1000 STARTING=>0b0100 RUN=>0b0010 STOPPING=>0b0001
53	RO	constant=0b0 Values: QUIESCE=>0b1000 STARTING=>0b0100 RUN=>0b0010 STOPPING=>0b0001
54	ROX	MAINT_SINGLE_MODE: maintenance single instruction mode
55	RO	constant=0b0
56	ROX	Reserved field. (Access type is core_step_or_resume_pending)
57:63	RO	constant=0b0000000

Register Name	<i>Hang Recovery Control Register</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL3.HANG_CONTROL
Address	0000000010013033 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	CORE_HANG_LIMIT: core hang limit hang_ctrl(0 to 7); init = 0x9F = 3 hang pulses
8:15	RW	NEST_HANG_LIMIT: GPS hang limit hang_ctrl(8 to 15); init = 0x2D = 100 hang pulses

Registers Specification

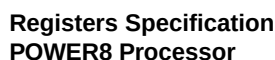
POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
16:18	RW	FLUSH_TIMEOUT_MODE: flush timeout mode ntc_mode_none => 0b000 ntc_stephang_mode => 0b001 ntc_chkstp_mode => 0b010 ntc_attn_mode => 0b100 ntc_quiesce_mode => 0b011 Values: NTC_MODE_NONE=>0b000 NTC_STEPHANG_MODE=>0b001 NTC_CHKSTP_MODE=>0b010 NTC_ATTN_MODE=>0b100 NTC_QUIESCE_MODE=>0b011
19:28	RW	FLUSH_LIMIT: ntc flush counter timeout limit
29	RW	NTC_TIMED_OUT_MODE: enablentc timeout counter action
30	RW	RETURN_GOOD_ON_COMP: return good on completion without waiting for a hang_pulse after seen completion
31	RW	ANY_GROUP_MODE: any group mode
32:39	RW	COMP_CNT_LIMIT_LT: completion count mode
40	RW	EN_RAND_NTC_FLUSH: enable random ntc flushes using random_pulse
41:42	RW	Reserved field. (Access type is hr_spare)
43:50	RW	ACTIVE_MASK_LT: active mask latch for hang condition enable/disable
51:58	RW	TLBIE_STALL_LIMIT: tlbie stall limit hang_ctrl(51 to 58); init = 0x99 = 50 hang pulses
59:63	RO	constant=0b000000

Register Name	Power Management Status Register For Debug
Mnemonic	EXP.EC.PC.PC_NE.TCTL3.POW_STATUS
Address	0000000010013034 (SCOM)
Attributes	
Description	(0:1 - Thread State, 2:3- Power State, 6:8 - SMT Mode, 9:15 - IRQ Nodoe/ext/decr/debug/hdec/pmon/sp_att, 16:19 - Sreset_type, 20 - Sreset Pending, 21 - DBG Fetch Stop, 22 - Async Pending, 23:25 - PMC Pm_state, 26:29 - Quiesce Arbitration State, 30:33 - PMC To Pow Spare)

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	POW_STATUS_THREAD_STATE: Thread state: quiesce => 0b1000 starting => 0b0100 run => 0b0010 stopping => 0b0001 Values: QUIESCE=>0b1000 STARTING=>0b0100 RUN=>0b0010 STOPPING=>0b0001

Bits	SCOM	Field Mnemonic: Description
4:5	ROX	PMC_POW_STATE: 00 - run, 01 - doze, 10 - nap, 11 - sleep/winkle Values: RUN=>0b00 DOZE=>0b01 NAP=>0b10 SLEEP=>0b11
6:8	ROX	PMC_SMT_MODE: 00 - power_on_ST, 01 - ST, 10 - SMT2, 11 - SMT4 Values: POWER_ON_ST=>0b000 ST=>0b001 SMT2_SH=>0b010 SMT2_SP=>0b011 SMT4=>0b100 SMT8=>0b101
9	ROX	HMI_INTR: hardware maintenance interrupt
10	ROX	Reserved field. (Access type is ext_intr)
11	ROX	DECR_INTR: decrementer interrupt
12	ROX	Reserved field. (Access type is debug_intr)
13	ROX	HDEC_INTR: hypervisor decrementer interrupt
14	ROX	Reserved field. (Access type is pmu_intr)
15	ROX	SP_ATTN_INTR: special attention interrupt
16:18	ROX	SRESET_TYPE: one of the switches and ldi to set to force sreset through scan sreset_null => 0b000 sreset_req_and_thr_en => 0b001 sreset_req_and_thr_disa => 0b010 decr_intr_and_thr_disa => 0b011 ext_intr_and_thr_disa => 0b100 hmi_intr_and_thr_disa => 0b101 sdi_intr_and_thr_disa => 0b110 awake_from_sleep => 0b111 Values: SRESET_NULL=>0b000 SRESET_REQ_AND_THR_EN=>0b001 SRESET_REQ_AND_THR_DISA=>0b010 DECR_INTR_AND_THR_DISA=>0b011 EXT_INTR_AND_THR_DISA=>0b100 HMI_INTR_AND_THR_DISA=>0b101 SDI_INTR_AND_THR_DISA=>0b110 AWAKE_FROM_SLEEP=>0b111
19	ROX	Reserved field. (Access type is sreset_type) Values: SRESET_NULL=>0b000 SRESET_REQ_AND_THR_EN=>0b001 SRESET_REQ_AND_THR_DISA=>0b010 DECR_INTR_AND_THR_DISA=>0b011 EXT_INTR_AND_THR_DISA=>0b100 HMI_INTR_AND_THR_DISA=>0b101 SDI_INTR_AND_THR_DISA=>0b110 AWAKE_FROM_SLEEP=>0b111
20	ROX	SRESET_PENDING: one of the switches and ldi to set to force sreset through scan
21	ROX	DBG_FETCH_STOP: pause fetching for debug workaround
22	ROX	ASYNC_PENDING: asynchronous interrupt pending



Register Name	<i>SPATTN Register</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL3.SPATTN
Address	0000000010013035 (SCOM1) 0000000010013036 (SCOM2) 0000000010013037 (SCOM)
Attributes	
Description	

[illegible]

Register Name	SPATTN_MASK Register
Mnemonic	EXP.EC.PC.PC_NE.TCTL3.SPATTN_MASK
Address	0000000010013038 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	SPATTN_CORE_CODE_TO_SP_MSK: Mask of Core code to service processor
1	RW	SPATTN_ATTN_COMPLETE_MSK: Mask of SP-ATTN instruction

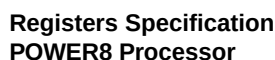


Bits	SCOM	Field Mnemonic: Description
2	RW	SPATTN_CORE_CHECKSTOP_RECOVERY_HANDSHAKE_MSK: Mask of core checkstop recovery handshake, alt: DABR SoftStop caused core quiesce
3	RW	SPATTN_CIABR QUIESCED_MSK: Mask of CIABR Quiesce caused core quiesce
4	RW	SPATTN_RECOVERY_BREAKPOINT_MSK: Mask of Attention from Core RECOVERY macro caused special attention
5	RW	SPATTN_NTC_ATTN_MSK: Mask of ntc_flush timeout
6	RW	SPATTN_THERM_MAX_MSK: Mask of edge detection on connected thermal maximum. External leveled signal detected.
7	RW	SPATTN_SPR_INSTR_STOP_MSK: Mask of instruction Stop Request from Hypervisor via SPR
8:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>SDI Register</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL3.SDI
Address	0000000010013039 (SCOM1) 000000001001303A (SCOM2) 000000001001303B (SCOM)
Attributes	
Description	

Bits	SCOM1	SCOM2	SCOM	Field Mnemonic: Description
0	WOX_AND	WOX_OR	RWX	SDI_SW_USE_1: sw_use_1 - Available for use by Service Processor to get attention of the hypervisor
1	WOX_AND	WOX_OR	RWX	SDI_SW_USE_2: sw_use_2 - Available for use by Service Processor to get attention of the hypervisor
2	WOX_AND	WOX_OR	RWX	SDI_SW_USE_3: sw_use_3 - Available for use by Service Processor to get attention of the hypervisor
3	WOX_AND	WOX_OR	RWX	SDI_HANG_RECV_OR_CHSW QUIESCE_TIMEOUT: Hang Recovery or chsw Quiesce Timeout
4	WOX_AND	WOX_OR	RWX	SDI_EXT_TRIGGER: RAS trigger
5	WOX_AND	WOX_OR	RWX	SDI_COREHANG: Thread Hang with CORE Source indication (modeable)
6	WOX_AND	WOX_OR	RWX	SDI_AMBIHANG: Thread Hang with AMBIGUOUS Source indication (modeable)
7	WOX_AND	WOX_OR	RWX	SDI_NESTHANG: Thread Hang with NEST Source indication (modeable)
8:63	RO	RO	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>SDI_MASK Register</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL3.SDI_MASK
Address	000000001001303C (SCOM)
Attributes	
Description	



Register Name	PC_NE Error Report Hold_out Register3
Mnemonic	EXP.EC.PC.PC_NE.PCNE_REG3_HOLD_OUT
Address	000000001001303D (SCOM)
Attributes	
Description	

[illegible]

Register Name	<i>Direct Injects Into Logic - No Latches!!</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL4.DIRECT_CONTROLS
Address	0000000010013040 (SCOM)
Attributes	
Description	

[illegible]

Register Name	<i>RAS Mode Register</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL4.RAS_MODEREG
Address	0000000010013041 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:42	RO	constant=0b000000000000000000000000000000000000000000
43	RW	MR_THREAD_IN_DEBUG_MODE: enable logic which should run only in the lab: iTrace, debug_bus, FP0
44	RW	MR_PMON_INHIBIT: perfmon inhibit
45	RW	MR_FENCE_INTERRUPTS: SP fence interrupts
46	RW	MR_STOP_FETCH: SP stop fetch
47	RW	MR_STOP_PREFETCH: SP stop prefetch to LSU
48	RW	MR_STOP_DISPATCH: SP stop dispatch

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
49	RW	MR_SINGLE_DECODE: Single Instruction Decode Mode When setting this switch to one, also set switch mr_one_ppc_mode of the ras_modereg to one Function similar to HID0[4] single_decode except HID0[4] forces one ppc mode beneath the covers Before changing this bit, the thread must first be in maintenance mode (ref. direct_controls.mr_core_stop)
50	RW	MR_DO_SINGLE_MODE: Single Instruction Completion Mode Before changing this bit, the thread must first be in maintenance mode (ref. direct_controls.mr_core_stop)
51	RW	MR_ONE_PPC_MODE: One PPC instruction per group mode Before changing this bit, the thread must first be in maintenance mode (ref. direct_controls.mr_core_stop)
52:53	RW	MR_HANG_TEST_CTRL: hang test control, clear testhang
54:56	RW	MR_ATTEMPT_GPS_HR: attempt GPS hang recovery "1xx": attempt recovery on core hang "x1x": attempt recovery on nest hang "xx1": attempt recovery on ambiguous hang
57	RW	MR_HANG_DIS: disable hang detection and state-machine
58	RW	MR_ON_COREHNG: enable Debug Interrupt on core hang
59	RW	MR_ON_AMBIHNG: enable Debug Interrupt on ambi hang
60	RW	MR_ON_NESTHNG: enable Debug Interrupt on nest hang
61	RW	MR_RECOV_ENABLE: enable RECOVERY by SCOM
62	RW	MR_BLOCK_HMI_ON_MAINT: block hmi in maintenance mode
63	RW	MR_FENCE_INTR_ON_CHECKSTOP: allow interrupt of checkstop occurred

Register Name	<i>Ra Status</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL4.RAS_STATUS
Address	0000000010013042 (SCOM)
Attributes	
Description	



Bits	SCOM	Field Mnemonic: Description
0:19	ROX	STAT: quiesce status 0 - entire row quiesced 1 - ISU is quiesced 2 - checkstop caused 3 - quiesce request by ISU 4 - ISU completed quiesced 5 - ISU quiesced by ATTN instr 6 - ISU quiesce by LSU DABR dbg mode 7 - ISU gct is empty (safe indication) 8 - ISU srq is empty (safe indication) 9 - LSU has no outstanding transactions to GPS 10 - LSU quiesced AND GUS idle 11 - Completion stopped by checkstop 12 - Group/Inst Completed since last maint op 13 - NTC flush not sace and caused checkstop 14 - Demand ifetch from IFU pending 15 - eat is empty 16 - nest active determination 17 - nest active determination 18 - nest active determination 19 - enable stop dispatch after 1st SCOM start happens
20	ROX	Reserved field. (Access type is por_state)
21	ROX	Reserved field. (Access type is core_maint_mode)
22	ROX	Reserved field. (Access type is pmc_quiesce_req)
23	ROX	OTHER_THREAD_ACTIVE: any other thread is active, hang control wise
24:26	ROX	HANG_FSM: hang recovery FSM state: good bad worse lost
27	RO	constant=0b0
28	ROX	HANG_HIST0: intelligent hang detected as core or ambiguous hang since last sp_cancel_lost
29	ROX	HANG_HIST1: intelligent hang detected as nest or ambiguous hang since last sp_cancel_lost
30	ROX	HANG_HIST2: hang_state bad was entered since last sp_cancel_lost
31	ROX	HANG_HIST3: hang_state lost was entered since last sp_cancel_lost
32	RO	constant=0b0
33:40	ROX	HR_COMP_CNT: hang recovery completion counter
41	ROX	SMT_DEAD_STOP: SMT dead stop
42	ROX	STOP_FETCH: stop fetch
43	ROX	STOP_DISPATCH: stop dispatch

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
44	ROX	STOP_COMPLETION: stop completion
45	ROX	HOLD_DECODE: hold decode
46	ROX	Reserved field. (Access type is ext_intr_pending)
47	ROX	Reserved field. (Access type is isu_isu_empty_internal)
48	ROX	THREAD_ENABLED: this thread was enabled by PMC when reading status
49:52	ROX	POW_STATUS_THREAD_STATE: Thread state: quiesce => 0b1000 starting => 0b0100 run => 0b0010 stopping => 0b0001 Values: QUIESCE=>0b1000 STARTING=>0b0100 RUN=>0b0010 STOPPING=>0b0001
53	RO	constant=0b0 Values: QUIESCE=>0b1000 STARTING=>0b0100 RUN=>0b0010 STOPPING=>0b0001
54	ROX	MAINT_SINGLE_MODE: maintenance single instruction mode
55	RO	constant=0b0
56	ROX	Reserved field. (Access type is core_step_or_resume_pending)
57:63	RO	constant=0b0000000

Register Name	Hang Recovery Control Register
Mnemonic	EXP.EC.PC.PC_NE.TCTL4.HANG_CONTROL
Address	0000000010013043 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	CORE_HANG_LIMIT: core hang limit hang_ctrl(0 to 7); init = 0x9F = 3 hang pulses
8:15	RW	NEST_HANG_LIMIT: GPS hang limit hang_ctrl(8 to 15); init = 0x2D = 100 hang pulses

Bits	SCOM	Field Mnemonic: Description
16:18	RW	FLUSH_TIMEOUT_MODE: flush timeout mode ntc_mode_none => 0b000 ntc_stephang_mode => 0b001 ntc_chkstp_mode => 0b010 ntc_attn_mode => 0b100 ntc_quiesce_mode => 0b011 Values: NTC_MODE_NONE=>0b000 NTC_STEPHANG_MODE=>0b001 NTC_CHKSTP_MODE=>0b010 NTC_ATTN_MODE=>0b100 NTC_QUIESCE_MODE=>0b011
19:28	RW	FLUSH_LIMIT: ntc flush counter timeout limit
29	RW	NTC_TIMED_OUT_MODE: enablentc timeout counter action
30	RW	RETURN_GOOD_ON_COMP: return good on completion without waiting for a hang_pulse after seen completion
31	RW	ANY_GROUP_MODE: any group mode
32:39	RW	COMP_CNT_LIMIT_LT: completion count mode
40	RW	EN_RAND_NTC_FLUSH: enable random ntc flushes using random_pulse
41:42	RW	Reserved field. (Access type is hr_spare)
43:50	RW	ACTIVE_MASK_LT: active mask latch for hang condition enable/disable
51:58	RW	TLBIE_STALL_LIMIT: tlbie stall limit hang_ctrl(51 to 58); init = 0x99 = 50 hang pulses
59:63	RO	constant=0b00000

Register Name	<i>Power Management Status Register For Debug</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL4.POW_STATUS
Address	0000000010013044 (SCOM)
Attributes	
Description	(0:1 - Thread State, 2:3- Power State, 6:8 - SMT Mode, 9:15 - IRQ Nodoe/ext/decr/debug/hdec/pmon/sp_att, 16:19 - Sreset_type, 20 - Sreset Pending, 21 - DBG Fetch Stop, 22 - Async Pending, 23:25 - PMC Pm_state, 26:29 - Quiesce Arbitration State, 30:33 - PMC To Pow Spare)

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	POW_STATUS_THREAD_STATE: Thread state: quiesce => 0b1000 starting => 0b0100 run => 0b0010 stopping => 0b0001 Values: QUIESCE=>0b1000 STARTING=>0b0100 RUN=>0b0010 STOPPING=>0b0001

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
4:5	ROX	PMC_POW_STATE: 00 - run, 01 - doze, 10 - nap, 11 - sleep/winkle Values: RUN=>0b00 DOZE=>0b01 NAP=>0b10 SLEEP=>0b11
6:8	ROX	PMC_SMT_MODE: 00 - power_on_ST, 01 - ST, 10 - SMT2, 11 - SMT4 Values: POWER_ON_ST=>0b000 ST=>0b001 SMT2_SH=>0b010 SMT2_SP=>0b011 SMT4=>0b100 SMT8=>0b101
9	ROX	HMI_INTR: hardware maintenance interrupt
10	ROX	Reserved field. (Access type is ext_intr)
11	ROX	DECR_INTR: decrementer interrupt
12	ROX	Reserved field. (Access type is debug_intr)
13	ROX	HDEC_INTR: hypervisor decrementer interrupt
14	ROX	Reserved field. (Access type is pmu_intr)
15	ROX	SP_ATTN_INTR: special attention interrupt
16:18	ROX	SRESET_TYPE: one of the switches and ldi to set to force sreset through scan sreset_null => 0b000 sreset_req_and_thr_en => 0b001 sreset_req_and_thr_disa => 0b010 decr_intr_and_thr_disa => 0b011 ext_intr_and_thr_disa => 0b100 hmi_intr_and_thr_disa => 0b101 sdi_intr_and_thr_disa => 0b110 awake_from_sleep => 0b111 Values: SRESET_NULL=>0b000 SRESET_REQ_AND_THR_EN=>0b001 SRESET_REQ_AND_THR_DISA=>0b010 DECR_INTR_AND_THR_DISA=>0b011 EXT_INTR_AND_THR_DISA=>0b100 HMI_INTR_AND_THR_DISA=>0b101 SDI_INTR_AND_THR_DISA=>0b110 AWAKE_FROM_SLEEP=>0b111
19	ROX	Reserved field. (Access type is sreset_type) Values: SRESET_NULL=>0b000 SRESET_REQ_AND_THR_EN=>0b001 SRESET_REQ_AND_THR_DISA=>0b010 DECR_INTR_AND_THR_DISA=>0b011 EXT_INTR_AND_THR_DISA=>0b100 HMI_INTR_AND_THR_DISA=>0b101 SDI_INTR_AND_THR_DISA=>0b110 AWAKE_FROM_SLEEP=>0b111
20	ROX	SRESET_PENDING: one of the switches and ldi to set to force sreset through scan
21	ROX	DBG_FETCH_STOP: pause fetching for debug workaround
22	ROX	ASYNC_PENDING: asynchronous interrupt pending



Bits	SCOM	Field Mnemonic: Description
23:25	ROX	CORE_POW_STATE: 000: run 100: doze 101: nap 110: sleep 111: rvwinkle
26:29	ROX	Reserved field. (Access type is qui_arb_state_one_hot)
30:33	ROX	PMC_TCTL_SPARE: 4 spare pins
34:63	RO	constant=0b00000000000000000000000000000000

Register Name	<i>SPATTN Register</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL4.SPATTN
Address	0000000010013045 (SCOM1) 0000000010013046 (SCOM2) 0000000010013047 (SCOM)
Attributes	
Description	

[illegible]

Register Name	SPATTN_MASK Register
Mnemonic	EXP.EC.PC.PC_NE.TCTL4.SPATTN_MASK
Address	0000000010013048 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	SPATTN_CORE_CODE_TO_SP_MSK: Mask of Core code to service processor
1	RW	SPATTN_ATTN_COMPLETE_MSK: Mask of SP-ATTN instruction



Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
2	RW	SPATTN_CORE_CHECKSTOP_RECOVERY_HANDSHAKE_MSK: Mask of core checkstop recovery handshake, alt: DABR SoftStop caused core quiesce
3	RW	SPATTN_CIABR QUIESCED_MSK: Mask of CIABR Quiesce caused core quiesce
4	RW	SPATTN_RECOVERY_BREAKPOINT_MSK: Mask of Attention from Core RECOVERY macro caused special attention
5	RW	SPATTN_NTC_ATTEN_MSK: Mask of ntc_flush timeout
6	RW	SPATTN_THERM_MAX_MSK: Mask of edge detection on connected thermal maximum. External leveled signal detected.
7	RW	SPATTN_SPR_INSTR_STOP_MSK: Mask of instruction Stop Request from Hypervisor via SPR
8:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>SDI Register</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL4.SDI
Address	0000000010013049 (SCOM1) 000000001001304A (SCOM2) 000000001001304B (SCOM)
Attributes	
Description	

Bits	SCOM1	SCOM2	SCOM	Field Mnemonic: Description
0	WOX_AND	WOX_OR	RWX	SDI_SW_USE_1: sw_use_1 - Available for use by Service Processor to get attention of the hypervisor
1	WOX_AND	WOX_OR	RWX	SDI_SW_USE_2: sw_use_2 - Available for use by Service Processor to get attention of the hypervisor
2	WOX_AND	WOX_OR	RWX	SDI_SW_USE_3: sw_use_3 - Available for use by Service Processor to get attention of the hypervisor
3	WOX_AND	WOX_OR	RWX	SDI_HANG_RECV_OR_CHSW QUIESCE_TIMEOUT: Hang Recovery or chsw Quiesce Timeout
4	WOX_AND	WOX_OR	RWX	SDI_EXT_TRIGGER: RAS trigger
5	WOX_AND	WOX_OR	RWX	SDI_COREHANG: Thread Hang with CORE Source indication (modeable)
6	WOX_AND	WOX_OR	RWX	SDI_AMBIHANG: Thread Hang with AMBIGUOUS Source indication (modeable)
7	WOX_AND	WOX_OR	RWX	SDI_NESTHANG: Thread Hang with NEST Source indication (modeable)
8:63	RO	RO	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>SDI_MASK Register</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL4.SDI_MASK
Address	000000001001304C (SCOM)
Attributes	
Description	

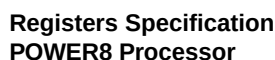


Bits	SCOM	Field Mnemonic: Description
0	RW	SDI_SW_USE_1_MSK: Mask of sw_use_1 - Available for use by Service Processor to get attention of the hypervisor
1	RW	SDI_SW_USE_2_MSK: Mask of sw_use_2 - Available for use by Service Processor to get attention of the hypervisor
2	RW	SDI_SW_USE_3_MSK: Mask of sw_use_3 - Available for use by Service Processor to get attention of the hypervisor
3	RW	SDI_HANG_RECV_OR_CHSW QUIESCE_TIMEOUT_MSK: Mask of Hang Recovery or chsw Quiesce Timeout
4	RW	SDI_EXT_TRIGGER_MSK: Mask of RAS trigger
5	RW	SDI_COREHANG_MSK: Mask of Thread Hang with CORE Source indication (modeable)
6	RW	SDI_AMBIHANG_MSK: Mask of Thread Hang with AMBIGUOUS Source indication (modeable)
7	RW	SDI_NESTHANG_MSK: Mask of Thread Hang with NEST Source indication (modeable)
8:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	PC_NE Error Report Hold_out Register4
Mnemonic	EXP.EC.PC.PC_NE.PCNE_REG4_HOLD_OUT
Address	000000001001304D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is TCTL4_ASYNC_INT_IN_RAM_hold_out)
1	ROX	Reserved field. (Access type is TCTL4_ATTNREG_PARITY_hold_out)
2	ROX	Reserved field. (Access type is TCTL4_DIREG_PARITY_hold_out)
3	ROX	Reserved field. (Access type is TCTL4_HANG_STATE_BAD_hold_out)
4	ROX	Reserved field. (Access type is TCTL4_HANG_STATE_LOST_hold_out)
5	ROX	Reserved field. (Access type is TCTL4_MY_SRESET_hold_out)
6	ROX	Reserved field. (Access type is TCTL4_PPC_COMPLETE_hold_out)
7	ROX	Reserved field. (Access type is TCTL4_RECOV_IN_MAINT_hold_out)
8	ROX	Reserved field. (Access type is TCTL4_DC_CORE_STEP_hold_out)
9	RO	constant=0b0
10:12	ROX	Reserved field. (Access type is TCTL4_THREAD_HANG_hold_out)
13:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	Direct Injects Into Logic - No Latches!!
Mnemonic	EXP.EC.PC.PC_NE.TCTL5.DIRECT_CONTROLS
Address	0000000010013050 (SCOM)
Attributes	
Description	



Register Name	<i>RAS Mode Register</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL5.RAS_MODEREG
Address	0000000010013051 (SCOM)
Attributes	
Description	

[illegible]



Bits	SCOM	Field Mnemonic: Description
49	RW	MR_SINGLE_DECODE: Single Instruction Decode Mode When setting this switch to one, also set switch mr_one_ppc_mode of the ras_modereg to one Function similar to HID0[4] single_decode except HID0[4] forces one ppc mode beneath the covers Before changing this bit, the thread must first be in maintenance mode (ref. direct_controls.mr_core_stop)
50	RW	MR_DO_SINGLE_MODE: Single Instruction Completion Mode Before changing this bit, the thread must first be in maintenance mode (ref. direct_controls.mr_core_stop)
51	RW	MR_ONE_PPC_MODE: One PPC instruction per group mode Before changing this bit, the thread must first be in maintenance mode (ref. direct_controls.mr_core_stop)
52:53	RW	MR_HANG_TEST_CTRL: hang test control, clear testhang
54:56	RW	MR_ATTEMPT_GPS_HR: attempt GPS hang recovery "1xx": attempt recovery on core hang "x1x": attempt recovery on nest hang "xx1": attempt recovery on ambiguous hang
57	RW	MR_HANG_DIS: disable hang detection and state-machine
58	RW	MR_ON_COREHNG: enable Debug Interrupt on core hang
59	RW	MR_ON_AMBIHNG: enable Debug Interrupt on ambi hang
60	RW	MR_ON_NESTHNG: enable Debug Interrupt on nest hang
61	RW	MR_RECOV_ENABLE: enable RECOVERY by SCOM
62	RW	MR_BLOCK_HMI_ON_MAINT: block hmi in maintenance mode
63	RW	MR_FENCE_INTR_ON_CHECKSTOP: allow interrupt of checkstop occurred

Register Name	<i>Ra Status</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL5.RAS_STATUS
Address	0000000010013052 (SCOM)
Attributes	
Description	

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
0:19	ROX	STAT: quiesce status 0 - entire row quiesced 1 - ISU is quiesced 2 - checkstop caused 3 - quiesce request by ISU 4 - ISU completed quiesced 5 - ISU quiesced by ATTN instr 6 - ISU quiesce by LSU DABR dbg mode 7 - ISU gct is empty (safe indication) 8 - ISU srq is empty (safe indication) 9 - LSU has no outstanding transactions to GPS 10 - LSU quiesced AND GUS idle 11 - Completion stopped by checkstop 12 - Group/Inst Completed since last maint op 13 - NTC flush not sace and caused checkstop 14 - Demand ifetch from IFU pending 15 - eat is empty 16 - nest active determination 17 - nest active determination 18 - nest active determination 19 - enable stop dispatch after 1st SCOM start happens
20	ROX	Reserved field. (Access type is por_state)
21	ROX	Reserved field. (Access type is core_maint_mode)
22	ROX	Reserved field. (Access type is pmc_quiesce_req)
23	ROX	OTHER_THREAD_ACTIVE: any other thread is active, hang control wise
24:26	ROX	HANG_FSM: hang recovery FSM state: good bad worse lost
27	RO	constant=0b0
28	ROX	HANG_HIST0: intelligent hang detected as core or ambiguous hang since last sp_cancel_lost
29	ROX	HANG_HIST1: intelligent hang detected as nest or ambiguous hang since last sp_cancel_lost
30	ROX	HANG_HIST2: hang_state bad was entered since last sp_cancel_lost
31	ROX	HANG_HIST3: hang_state lost was entered since last sp_cancel_lost
32	RO	constant=0b0
33:40	ROX	HR_COMP_CNT: hang recovery completion counter
41	ROX	SMT_DEAD_STOP: SMT dead stop
42	ROX	STOP_FETCH: stop fetch
43	ROX	STOP_DISPATCH: stop dispatch



Bits	SCOM	Field Mnemonic: Description
44	ROX	STOP_COMPLETION: stop completion
45	ROX	HOLD_DECODE: hold decode
46	ROX	Reserved field. (Access type is ext_intr_pending)
47	ROX	Reserved field. (Access type is isu_isu_empty_internal)
48	ROX	THREAD_ENABLED: this thread was enabled by PMC when reading status
49:52	ROX	POW_STATUS_THREAD_STATE: Thread state: quiesce => 0b1000 starting => 0b0100 run => 0b0010 stopping => 0b0001 Values: QUIESCE=>0b1000 STARTING=>0b0100 RUN=>0b0010 STOPPING=>0b0001
53	RO	constant=0b0 Values: QUIESCE=>0b1000 STARTING=>0b0100 RUN=>0b0010 STOPPING=>0b0001
54	ROX	MAINT_SINGLE_MODE: maintenance single instruction mode
55	RO	constant=0b0
56	ROX	Reserved field. (Access type is core_step_or_resume_pending)
57:63	RO	constant=0b0000000

Register Name	<i>Hang Recovery Control Register</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL5.HANG_CONTROL
Address	0000000010013053 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	CORE_HANG_LIMIT: core hang limit hang_ctrl(0 to 7); init = 0x9F = 3 hang pulses
8:15	RW	NEST_HANG_LIMIT: GPS hang limit hang_ctrl(8 to 15); init = 0x2D = 100 hang pulses

Registers Specification

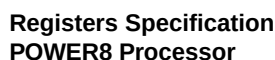
POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
16:18	RW	FLUSH_TIMEOUT_MODE: flush timeout mode ntc_mode_none => 0b000 ntc_stephang_mode => 0b001 ntc_chkstp_mode => 0b010 ntc_attn_mode => 0b100 ntc_quiesce_mode => 0b011 Values: NTC_MODE_NONE=>0b000 NTC_STEPHANG_MODE=>0b001 NTC_CHKSTP_MODE=>0b010 NTC_ATTEN_MODE=>0b100 NTC_QUIESCE_MODE=>0b011
19:28	RW	FLUSH_LIMIT: ntc flush counter timeout limit
29	RW	NTC_TIMED_OUT_MODE: enablentc timeout counter action
30	RW	RETURN_GOOD_ON_COMP: return good on completion without waiting for a hang_pulse after seen completion
31	RW	ANY_GROUP_MODE: any group mode
32:39	RW	COMP_CNT_LIMIT_LT: completion count mode
40	RW	EN_RAND_NTC_FLUSH: enable random ntc flushes using random_pulse
41:42	RW	Reserved field. (Access type is hr_spare)
43:50	RW	ACTIVE_MASK_LT: active mask latch for hang condition enable/disable
51:58	RW	TLBIE_STALL_LIMIT: tlbie stall limit hang_ctrl(51 to 58); init = 0x99 = 50 hang pulses
59:63	RO	constant=0b00000

Register Name	Power Management Status Register For Debug
Mnemonic	EXP.EC.PC.PC_NE.TCTL5.POW_STATUS
Address	0000000010013054 (SCOM)
Attributes	
Description	<i>(0:1 - Thread State, 2:3- Power State, 6:8 - SMT Mode, 9:15 - IRQ, Nodoze/ext/decr/debug/hdec/pmon/sp_att, 16:19 - Sreset_type, 20 - Sreset Pending, 21 - DBG Fetch Stop, 22 - Async Pending, 23:25 - PMC Pm_state, 26:29 - Quiesce Arbitration State, 30:33 - PMC To Pow Spare)</i>

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	POW_STATUS_THREAD_STATE: Thread state: quiesce => 0b1000 starting => 0b0100 run => 0b0010 stopping => 0b0001 Values: QUIESCE=>0b1000 STARTING=>0b0100 RUN=>0b0010 STOPPING=>0b0001

Bits	SCOM	Field Mnemonic: Description
4:5	ROX	PMC_POW_STATE: 00 - run, 01 - doze, 10 - nap, 11 - sleep/winkle Values: RUN=>0b00 DOZE=>0b01 NAP=>0b10 SLEEP=>0b11
6:8	ROX	PMC_SMT_MODE: 00 - power_on_ST, 01 - ST, 10 - SMT2, 11 - SMT4 Values: POWER_ON_ST=>0b000 ST=>0b001 SMT2_SH=>0b010 SMT2_SP=>0b011 SMT4=>0b100 SMT8=>0b101
9	ROX	HMI_INTR: hardware maintenance interrupt
10	ROX	Reserved field. (Access type is ext_intr)
11	ROX	DECR_INTR: decrementer interrupt
12	ROX	Reserved field. (Access type is debug_intr)
13	ROX	HDEC_INTR: hypervisor decrementer interrupt
14	ROX	Reserved field. (Access type is pmu_intr)
15	ROX	SP_ATTN_INTR: special attention interrupt
16:18	ROX	SRESET_TYPE: one of the switches and ldi al to set to force sreset through scan sreset_null => 0b000 sreset_req_and_thr_en => 0b001 sreset_req_and_thr_disa => 0b010 decr_intr_and_thr_disa => 0b011 ext_intr_and_thr_disa => 0b100 hmi_intr_and_thr_disa => 0b101 sdi_intr_and_thr_disa => 0b110 awake_from_sleep => 0b111 Values: SRESET_NULL=>0b000 SRESET_REQ_AND_THR_EN=>0b001 SRESET_REQ_AND_THR_DISA=>0b010 DECR_INTR_AND_THR_DISA=>0b011 EXT_INTR_AND_THR_DISA=>0b100 HMI_INTR_AND_THR_DISA=>0b101 SDI_INTR_AND_THR_DISA=>0b110 AWAKE_FROM_SLEEP=>0b111
19	ROX	Reserved field. (Access type is sreset_type) Values: SRESET_NULL=>0b000 SRESET_REQ_AND_THR_EN=>0b001 SRESET_REQ_AND_THR_DISA=>0b010 DECR_INTR_AND_THR_DISA=>0b011 EXT_INTR_AND_THR_DISA=>0b100 HMI_INTR_AND_THR_DISA=>0b101 SDI_INTR_AND_THR_DISA=>0b110 AWAKE_FROM_SLEEP=>0b111
20	ROX	SRESET_PENDING: one of the switches and ldi al to set to force sreset through scan
21	ROX	DBG_FETCH_STOP: pause fetching for debug workaround
22	ROX	ASYNC_PENDING: asynchronous interrupt pending



Register Name	<i>SPATTN Register</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL5.SPATTN
Address	0000000010013055 (SCOM1) 0000000010013056 (SCOM2) 0000000010013057 (SCOM)
Attributes	
Description	

Register Name	SPATTN_MASK Register
Mnemonic	EXP.EC.PC.PC_NE.TCTL5.SPATTN_MASK
Address	0000000010013058 (SCOM)
Attributes	
Description	

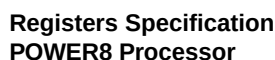


Bits	SCOM	Field Mnemonic: Description
2	RW	SPATTN_CORE_CHECKSTOP_RECOVERY_HANDSHAKE_MSK: Mask of core checkstop recovery handshake, alt: DABR SoftStop caused core quiesce
3	RW	SPATTN_CIABR QUIESCED_MSK: Mask of CIABR Quiesce caused core quiesce
4	RW	SPATTN_RECOVERY_BREAKPOINT_MSK: Mask of Attention from Core RECOVERY macro caused special attention
5	RW	SPATTN_NTC_ATTN_MSK: Mask of ntc_flush timeout
6	RW	SPATTN_THERM_MAX_MSK: Mask of edge detection on connected thermal maximum. External leveled signal detected.
7	RW	SPATTN_SPR_INSTR_STOP_MSK: Mask of instruction Stop Request from Hypervisor via SPR
8:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>SDI Register</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL5.SDI
Address	0000000010013059 (SCOM1) 000000001001305A (SCOM2) 000000001001305B (SCOM)
Attributes	
Description	

Bits	SCOM1	SCOM2	SCOM	Field Mnemonic: Description
0	WOX_AND	WOX_OR	RWX	SDI_SW_USE_1: sw_use_1 - Available for use by Service Processor to get attention of the hypervisor
1	WOX_AND	WOX_OR	RWX	SDI_SW_USE_2: sw_use_2 - Available for use by Service Processor to get attention of the hypervisor
2	WOX_AND	WOX_OR	RWX	SDI_SW_USE_3: sw_use_3 - Available for use by Service Processor to get attention of the hypervisor
3	WOX_AND	WOX_OR	RWX	SDI_HANG_RECV_OR_CHSW QUIESCE_TIMEOUT: Hang Recovery or chsw Quiesce Timeout
4	WOX_AND	WOX_OR	RWX	SDI_EXT_TRIGGER: RAS trigger
5	WOX_AND	WOX_OR	RWX	SDI_COREHANG: Thread Hang with CORE Source indication (modeable)
6	WOX_AND	WOX_OR	RWX	SDI_AMBIHANG: Thread Hang with AMBIGUOUS Source indication (modeable)
7	WOX_AND	WOX_OR	RWX	SDI_NESTHANG: Thread Hang with NEST Source indication (modeable)
8:63	RO	RO	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>SDI_MASK Register</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL5.SDI_MASK
Address	000000001001305C (SCOM)
Attributes	
Description	



Register Name	PC_NE Error Report Hold_out Register5
Mnemonic	EXP.EC.PC.PC_NE.PCNE_REG5_HOLD_OUT
Address	000000001001305D (SCOM)
Attributes	
Description	

[illegible]

Register Name	Direct Injects Into Logic - No Latches!!
Mnemonic	EXP.EC.PC.PC_NE.TCTL6.DIRECT_CONTROLS
Address	0000000010013060 (SCOM)
Attributes	
Description	

[illegible]

Register Name	<i>RAS Mode Register</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL6.RAS_MODEREG
Address	0000000010013061 (SCOM)
Attributes	
Description	

[illegible]

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
49	RW	MR_SINGLE_DECODE: Single Instruction Decode Mode When setting this switch to one, also set switch mr_one_ppc_mode of the ras_modereg to one Function similar to HID0[4] single_decode except HID0[4] forces one ppc mode beneath the covers Before changing this bit, the thread must first be in maintenance mode (ref. direct_controls.mr_core_stop)
50	RW	MR_DO_SINGLE_MODE: Single Instruction Completion Mode Before changing this bit, the thread must first be in maintenance mode (ref. direct_controls.mr_core_stop)
51	RW	MR_ONE_PPC_MODE: One PPC instruction per group mode Before changing this bit, the thread must first be in maintenance mode (ref. direct_controls.mr_core_stop)
52:53	RW	MR_HANG_TEST_CTRL: hang test control, clear testhang
54:56	RW	MR_ATTEMPT_GPS_HR: attempt GPS hang recovery "1xx": attempt recovery on core hang "x1x": attempt recovery on nest hang "xx1": attempt recovery on ambiguous hang
57	RW	MR_HANG_DIS: disable hang detection and state-machine
58	RW	MR_ON_COREHNG: enable Debug Interrupt on core hang
59	RW	MR_ON_AMBIHNG: enable Debug Interrupt on ambi hang
60	RW	MR_ON_NESTHNG: enable Debug Interrupt on nest hang
61	RW	MR_RECOV_ENABLE: enable RECOVERY by SCOM
62	RW	MR_BLOCK_HMI_ON_MAINT: block hmi in maintenance mode
63	RW	MR_FENCE_INTR_ON_CHECKSTOP: allow interrupt of checkstop occurred

Register Name	<i>Ra Status</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL6.RAS_STATUS
Address	0000000010013062 (SCOM)
Attributes	
Description	



Bits	SCOM	Field Mnemonic: Description
0:19	ROX	STAT: quiesce status 0 - entire row quiesced 1 - ISU is quiesced 2 - checkstop caused 3 - quiesce request by ISU 4 - ISU completed quiesced 5 - ISU quiesced by ATTN instr 6 - ISU quiesce by LSU DABR dbg mode 7 - ISU gct is empty (safe indication) 8 - ISU srq is empty (safe indication) 9 - LSU has no outstanding transactions to GPS 10 - LSU quiesced AND GUS idle 11 - Completion stopped by checkstop 12 - Group/Inst Completed since last maint op 13 - NTC flush not sace and caused checkstop 14 - Demand ifetch from IFU pending 15 - eat is empty 16 - nest active determination 17 - nest active determination 18 - nest active determination 19 - enable stop dispatch after 1st SCOM start happens
20	ROX	Reserved field. (Access type is por_state)
21	ROX	Reserved field. (Access type is core_maint_mode)
22	ROX	Reserved field. (Access type is pmc_quiesce_req)
23	ROX	OTHER_THREAD_ACTIVE: any other thread is active, hang control wise
24:26	ROX	HANG_FSM: hang recovery FSM state: good bad worse lost
27	RO	constant=0b0
28	ROX	HANG_HIST0: intelligent hang detected as core or ambiguous hang since last sp_cancel_lost
29	ROX	HANG_HIST1: intelligent hang detected as nest or ambiguous hang since last sp_cancel_lost
30	ROX	HANG_HIST2: hang_state bad was entered since last sp_cancel_lost
31	ROX	HANG_HIST3: hang_state lost was entered since last sp_cancel_lost
32	RO	constant=0b0
33:40	ROX	HR_COMP_CNT: hang recovery completion counter
41	ROX	SMT_DEAD_STOP: SMT dead stop
42	ROX	STOP_FETCH: stop fetch
43	ROX	STOP_DISPATCH: stop dispatch

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
44	ROX	STOP_COMPLETION: stop completion
45	ROX	HOLD_DECODE: hold decode
46	ROX	Reserved field. (Access type is ext_intr_pending)
47	ROX	Reserved field. (Access type is isu_isu_empty_internal)
48	ROX	THREAD_ENABLED: this thread was enabled by PMC when reading status
49:52	ROX	POW_STATUS_THREAD_STATE: Thread state: quiesce => 0b1000 starting => 0b0100 run => 0b0010 stopping => 0b0001 Values: QUIESCE=>0b1000 STARTING=>0b0100 RUN=>0b0010 STOPPING=>0b0001
53	RO	constant=0b0 Values: QUIESCE=>0b1000 STARTING=>0b0100 RUN=>0b0010 STOPPING=>0b0001
54	ROX	MAINT_SINGLE_MODE: maintenance single instruction mode
55	RO	constant=0b0
56	ROX	Reserved field. (Access type is core_step_or_resume_pending)
57:63	RO	constant=0b0000000

Register Name	Hang Recovery Control Register
Mnemonic	EXP.EC.PC.PC_NE.TCTL6.HANG_CONTROL
Address	0000000010013063 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	CORE_HANG_LIMIT: core hang limit hang_ctrl(0 to 7); init = 0x9F = 3 hang pulses
8:15	RW	NEST_HANG_LIMIT: GPS hang limit hang_ctrl(8 to 15); init = 0x2D = 100 hang pulses

Bits	SCOM	Field Mnemonic: Description
16:18	RW	FLUSH_TIMEOUT_MODE: flush timeout mode ntc_mode_none => 0b000 ntc_stephang_mode => 0b001 ntc_chkstp_mode => 0b010 ntc_attn_mode => 0b100 ntc_quiesce_mode => 0b011 Values: NTC_MODE_NONE=>0b000 NTC_STEPHANG_MODE=>0b001 NTC_CHKSTP_MODE=>0b010 NTC_ATTN_MODE=>0b100 NTC_QUIESCE_MODE=>0b011
19:28	RW	FLUSH_LIMIT: ntc flush counter timeout limit
29	RW	NTC_TIMED_OUT_MODE: enablentc timeout counter action
30	RW	RETURN_GOOD_ON_COMP: return good on completion without waiting for a hang_pulse after seen completion
31	RW	ANY_GROUP_MODE: any group mode
32:39	RW	COMP_CNT_LIMIT_LT: completion count mode
40	RW	EN_RAND_NTC_FLUSH: enable random ntc flushes using random_pulse
41:42	RW	Reserved field. (Access type is hr_spare)
43:50	RW	ACTIVE_MASK_LT: active mask latch for hang condition enable/disable
51:58	RW	TLBIE_STALL_LIMIT: tlbie stall limit hang_ctrl(51 to 58); init = 0x99 = 50 hang pulses
59:63	RO	constant=0b00000

Register Name	<i>Power Management Status Register For Debug</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL6.POW_STATUS
Address	0000000010013064 (SCOM)
Attributes	
Description	(0:1 - Thread State, 2:3- Power State, 6:8 - SMT Mode, 9:15 - IRQ Nodoe/ext/decr/debug/hdec/pmon/sp_att, 16:19 - Sreset_type, 20 - Sreset Pending, 21 - DBG Fetch Stop, 22 - Async Pending, 23:25 - PMC Pm_state, 26:29 - Quiesce Arbitration State, 30:33 - PMC To Pow Spare)

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	POW_STATUS_THREAD_STATE: Thread state: quiesce => 0b1000 starting => 0b0100 run => 0b0010 stopping => 0b0001 Values: QUIESCE=>0b1000 STARTING=>0b0100 RUN=>0b0010 STOPPING=>0b0001

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
4:5	ROX	PMC_POW_STATE: 00 - run, 01 - doze, 10 - nap, 11 - sleep/winkle Values: RUN=>0b00 DOZE=>0b01 NAP=>0b10 SLEEP=>0b11
6:8	ROX	PMC_SMT_MODE: 00 - power_on_ST, 01 - ST, 10 - SMT2, 11 - SMT4 Values: POWER_ON_ST=>0b000 ST=>0b001 SMT2_SH=>0b010 SMT2_SP=>0b011 SMT4=>0b100 SMT8=>0b101
9	ROX	HMI_INTR: hardware maintenance interrupt
10	ROX	Reserved field. (Access type is ext_intr)
11	ROX	DECR_INTR: decrementer interrupt
12	ROX	Reserved field. (Access type is debug_intr)
13	ROX	HDEC_INTR: hypervisor decrementer interrupt
14	ROX	Reserved field. (Access type is pmu_intr)
15	ROX	SP_ATTN_INTR: special attention interrupt
16:18	ROX	SRESET_TYPE: one of the switches and ldial to set to force sreset through scan sreset_null => 0b000 sreset_req_and_thr_en => 0b001 sreset_req_and_thr_disa => 0b010 decr_intr_and_thr_disa => 0b011 ext_intr_and_thr_disa => 0b100 hmi_intr_and_thr_disa => 0b101 sdi_intr_and_thr_disa => 0b110 awake_from_sleep => 0b111 Values: SRESET_NULL=>0b000 SRESET_REQ_AND_THR_EN=>0b001 SRESET_REQ_AND_THR_DISA=>0b010 DECR_INTR_AND_THR_DISA=>0b011 EXT_INTR_AND_THR_DISA=>0b100 HMI_INTR_AND_THR_DISA=>0b101 SDI_INTR_AND_THR_DISA=>0b110 AWAKE_FROM_SLEEP=>0b111
19	ROX	Reserved field. (Access type is sreset_type) Values: SRESET_NULL=>0b000 SRESET_REQ_AND_THR_EN=>0b001 SRESET_REQ_AND_THR_DISA=>0b010 DECR_INTR_AND_THR_DISA=>0b011 EXT_INTR_AND_THR_DISA=>0b100 HMI_INTR_AND_THR_DISA=>0b101 SDI_INTR_AND_THR_DISA=>0b110 AWAKE_FROM_SLEEP=>0b111
20	ROX	SRESET_PENDING: one of the switches and ldial to set to force sreset through scan
21	ROX	DBG_FETCH_STOP: pause fetching for debug workaround
22	ROX	ASYNC_PENDING: asynchronous interrupt pending



Bits	SCOM	Field Mnemonic: Description
23:25	ROX	CORE_POW_STATE: 000: run 100: doze 101: nap 110: sleep 111: rvwinkle
26:29	ROX	Reserved field. (Access type is qui_arb_state_one_hot)
30:33	ROX	PMC_TCTL_SPARE: 4 spare pins
34:63	RO	constant=0b00000000000000000000000000000000

Register Name	<i>SPATTN Register</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL6.SPATTN
Address	0000000010013065 (SCOM1) 0000000010013066 (SCOM2) 0000000010013067 (SCOM)
Attributes	
Description	

[illegible]

Register Name	SPATTN_MASK Register
Mnemonic	EXP.EC.PC.PC_NE.TCTL6.SPATTN_MASK
Address	0000000010013068 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	SPATTN_CORE_CODE_TO_SP_MSK: Mask of Core code to service processor
1	RW	SPATTN_ATTN_COMPLETE_MSK: Mask of SP-ATTN instruction



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Bits	SCOM	Field Mnemonic: Description
2	RW	SPATTN_CORE_CHECKSTOP_RECOVERY_HANDSHAKE_MSK: Mask of core checkstop recovery handshake, alt: DABR SoftStop caused core quiesce
3	RW	SPATTN_CIABR QUIESCED_MSK: Mask of CIABR Quiesce caused core quiesce
4	RW	SPATTN_RECOVERY_BREAKPOINT_MSK: Mask of Attention from Core RECOVERY macro caused special attention
5	RW	SPATTN_NTC_ATTEN_MSK: Mask of ntc_flush timeout
6	RW	SPATTN_THERM_MAX_MSK: Mask of edge detection on connected thermal maximum. External leveled signal detected.
7	RW	SPATTN_SPR_INSTR_STOP_MSK: Mask of instruction Stop Request from Hypervisor via SPR
8:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>SDI Register</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL6.SDI
Address	0000000010013069 (SCOM1) 000000001001306A (SCOM2) 000000001001306B (SCOM)
Attributes	
Description	

Bits	SCOM1	SCOM2	SCOM	Field Mnemonic: Description
0	WOX_AND	WOX_OR	RWX	SDI_SW_USE_1: sw_use_1 - Available for use by Service Processor to get attention of the hypervisor
1	WOX_AND	WOX_OR	RWX	SDI_SW_USE_2: sw_use_2 - Available for use by Service Processor to get attention of the hypervisor
2	WOX_AND	WOX_OR	RWX	SDI_SW_USE_3: sw_use_3 - Available for use by Service Processor to get attention of the hypervisor
3	WOX_AND	WOX_OR	RWX	SDI_HANG_RECV_OR_CHSW QUIESCE_TIMEOUT: Hang Recovery or chsw Quiesce Timeout
4	WOX_AND	WOX_OR	RWX	SDI_EXT_TRIGGER: RAS trigger
5	WOX_AND	WOX_OR	RWX	SDI_COREHANG: Thread Hang with CORE Source indication (modeable)
6	WOX_AND	WOX_OR	RWX	SDI_AMBIHANG: Thread Hang with AMBIGUOUS Source indication (modeable)
7	WOX_AND	WOX_OR	RWX	SDI_NESTHANG: Thread Hang with NEST Source indication (modeable)
8:63	RO	RO	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>SDI_MASK Register</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL6.SDI_MASK
Address	000000001001306C (SCOM)
Attributes	
Description	

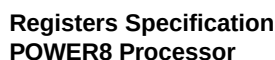


Bits	SCOM	Field Mnemonic: Description
0	RW	SDI_SW_USE_1_MSK: Mask of sw_use_1 - Available for use by Service Processor to get attention of the hypervisor
1	RW	SDI_SW_USE_2_MSK: Mask of sw_use_2 - Available for use by Service Processor to get attention of the hypervisor
2	RW	SDI_SW_USE_3_MSK: Mask of sw_use_3 - Available for use by Service Processor to get attention of the hypervisor
3	RW	SDI_HANG_RECV_OR_CHSW QUIESCE_TIMEOUT_MSK: Mask of Hang Recovery or chsw Quiesce Timeout
4	RW	SDI_EXT_TRIGGER_MSK: Mask of RAS trigger
5	RW	SDI_COREHANG_MSK: Mask of Thread Hang with CORE Source indication (modeable)
6	RW	SDI_AMBIHANG_MSK: Mask of Thread Hang with AMBIGUOUS Source indication (modeable)
7	RW	SDI_NESTHANG_MSK: Mask of Thread Hang with NEST Source indication (modeable)
8:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>PC_NE Error Report Hold_out Register6</i>
Mnemonic	EXP.EC.PC.PC_NE.PCNE_REG6_HOLD_OUT
Address	000000001001306D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is TCTL6_ASYNC_INT_IN_RAM_hold_out)
1	ROX	Reserved field. (Access type is TCTL6_ATTNREG_PARITY_hold_out)
2	ROX	Reserved field. (Access type is TCTL6_DIREG_PARITY_hold_out)
3	ROX	Reserved field. (Access type is TCTL6_HANG_STATE_BAD_hold_out)
4	ROX	Reserved field. (Access type is TCTL6_HANG_STATE_LOST_hold_out)
5	ROX	Reserved field. (Access type is TCTL6_MY_SRESET_hold_out)
6	ROX	Reserved field. (Access type is TCTL6_PPC_COMPLETE_hold_out)
7	ROX	Reserved field. (Access type is TCTL6_RECOV_IN_MAINT_hold_out)
8	ROX	Reserved field. (Access type is TCTL6_DC_CORE_STEP_hold_out)
9	RO	constant=0b0
10:12	ROX	Reserved field. (Access type is TCTL6_THREAD_HANG_hold_out)
13:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>Direct Injects Into Logic - No Latches</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL7.DIRECT_CONTROLS
Address	0000000010013070 (SCOM)
Attributes	
Description	



Register Name	<i>RAS Mode Register</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL7.RAS_MODEREG
Address	0000000010013071 (SCOM)
Attributes	
Description	

[illegible]



Bits	SCOM	Field Mnemonic: Description
49	RW	MR_SINGLE_DECODE: Single Instruction Decode Mode When setting this switch to one, also set switch mr_one_ppc_mode of the ras_modereg to one Function similar to HID0[4] single_decode except HID0[4] forces one ppc mode beneath the covers Before changing this bit, the thread must first be in maintenance mode (ref. direct_controls.mr_core_stop)
50	RW	MR_DO_SINGLE_MODE: Single Instruction Completion Mode Before changing this bit, the thread must first be in maintenance mode (ref. direct_controls.mr_core_stop)
51	RW	MR_ONE_PPC_MODE: One PPC instruction per group mode Before changing this bit, the thread must first be in maintenance mode (ref. direct_controls.mr_core_stop)
52:53	RW	MR_HANG_TEST_CTRL: hang test control, clear testhang
54:56	RW	MR_ATTEMPT_GPS_HR: attempt GPS hang recovery "1xx": attempt recovery on core hang "x1x": attempt recovery on nest hang "xx1": attempt recovery on ambiguous hang
57	RW	MR_HANG_DIS: disable hang detection and state-machine
58	RW	MR_ON_COREHNG: enable Debug Interrupt on core hang
59	RW	MR_ON_AMBIHNG: enable Debug Interrupt on ambi hang
60	RW	MR_ON_NESTHNG: enable Debug Interrupt on nest hang
61	RW	MR_RECOV_ENABLE: enable RECOVERY by SCOM
62	RW	MR_BLOCK_HMI_ON_MAINT: block hmi in maintenance mode
63	RW	MR_FENCE_INTR_ON_CHECKSTOP: allow interrupt of checkstop occurred

Register Name	<i>Ra Status</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL7.RAS_STATUS
Address	0000000010013072 (SCOM)
Attributes	
Description	

Registers Specification

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Bits	SCOM	Field Mnemonic: Description
0:19	ROX	STAT: quiesce status 0 - entire row quiesced 1 - ISU is quiesced 2 - checkstop caused 3 - quiesce request by ISU 4 - ISU completed quiesced 5 - ISU quiesced by ATTN instr 6 - ISU quiesce by LSU DABR dbg mode 7 - ISU gct is empty (safe indication) 8 - ISU srq is empty (safe indication) 9 - LSU has no outstanding transactions to GPS 10 - LSU quiesced AND GUS idle 11 - Completion stopped by checkstop 12 - Group/Inst Completed since last maint op 13 - NTC flush not sace and caused checkstop 14 - Demand ifetch from IFU pending 15 - eat is empty 16 - nest active determination 17 - nest active determination 18 - nest active determination 19 - enable stop dispatch after 1st SCOM start happens
20	ROX	Reserved field. (Access type is por_state)
21	ROX	Reserved field. (Access type is core_maint_mode)
22	ROX	Reserved field. (Access type is pmc_quiesce_req)
23	ROX	OTHER_THREAD_ACTIVE: any other thread is active, hang control wise
24:26	ROX	HANG_FSM: hang recovery FSM state: good bad worse lost
27	RO	constant=0b0
28	ROX	HANG_HIST0: intelligent hang detected as core or ambiguous hang since last sp_cancel_lost
29	ROX	HANG_HIST1: intelligent hang detected as nest or ambiguous hang since last sp_cancel_lost
30	ROX	HANG_HIST2: hang_state bad was entered since last sp_cancel_lost
31	ROX	HANG_HIST3: hang_state lost was entered since last sp_cancel_lost
32	RO	constant=0b0
33:40	ROX	HR_COMP_CNT: hang recovery completion counter
41	ROX	SMT_DEAD_STOP: SMT dead stop
42	ROX	STOP_FETCH: stop fetch
43	ROX	STOP_DISPATCH: stop dispatch



Bits	SCOM	Field Mnemonic: Description
44	ROX	STOP_COMPLETION: stop completion
45	ROX	HOLD_DECODE: hold decode
46	ROX	Reserved field. (Access type is ext_intr_pending)
47	ROX	Reserved field. (Access type is isu_isu_empty_internal)
48	ROX	THREAD_ENABLED: this thread was enabled by PMC when reading status
49:52	ROX	POW_STATUS_THREAD_STATE: Thread state: quiesce => 0b1000 starting => 0b0100 run => 0b0010 stopping => 0b0001 Values: QUIESCE=>0b1000 STARTING=>0b0100 RUN=>0b0010 STOPPING=>0b0001
53	RO	constant=0b0 Values: QUIESCE=>0b1000 STARTING=>0b0100 RUN=>0b0010 STOPPING=>0b0001
54	ROX	MAINT_SINGLE_MODE: maintenance single instruction mode
55	RO	constant=0b0
56	ROX	Reserved field. (Access type is core_step_or_resume_pending)
57:63	RO	constant=0b0000000

Register Name	<i>Hang Recovery Control Register</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL7.HANG_CONTROL
Address	0000000010013073 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	CORE_HANG_LIMIT: core hang limit hang_ctrl(0 to 7); init = 0x9F = 3 hang pulses
8:15	RW	NEST_HANG_LIMIT: GPS hang limit hang_ctrl(8 to 15); init = 0x2D = 100 hang pulses

Registers Specification

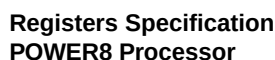
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Bits	SCOM	Field Mnemonic: Description
16:18	RW	FLUSH_TIMEOUT_MODE: flush timeout mode ntc_mode_none => 0b000 ntc_stephang_mode => 0b001 ntc_chkstp_mode => 0b010 ntc_attn_mode => 0b100 ntc_quiesce_mode => 0b011 Values: NTC_MODE_NONE=>0b000 NTC_STEPHANG_MODE=>0b001 NTC_CHKSTP_MODE=>0b010 NTC_ATTN_MODE=>0b100 NTC_QUIESCE_MODE=>0b011
19:28	RW	FLUSH_LIMIT: ntc flush counter timeout limit
29	RW	NTC_TIMED_OUT_MODE: enablentc timeout counter action
30	RW	RETURN_GOOD_ON_COMP: return good on completion without waiting for a hang_pulse after seen completion
31	RW	ANY_GROUP_MODE: any group mode
32:39	RW	COMP_CNT_LIMIT_LT: completion count mode
40	RW	EN_RAND_NTC_FLUSH: enable random ntc flushes using random_pulse
41:42	RW	Reserved field. (Access type is hr_spare)
43:50	RW	ACTIVE_MASK_LT: active mask latch for hang condition enable/disable
51:58	RW	TLBIE_STALL_LIMIT: tlbie stall limit hang_ctrl(51 to 58); init = 0x99 = 50 hang pulses
59:63	RO	constant=0b00000

Register Name	<i>Power Management Status Register For Debug</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL7.POW_STATUS
Address	0000000010013074 (SCOM)
Attributes	
Description	(0:1 - Thread State, 2:3- Power State, 6:8 - SMT Mode, 9:15 - IRQ Nodoe/ext/decr/debug/hdec/pmon/sp_att, 16:19 - Sreset_type, 20 - Sreset Pending, 21 - DBG Fetch Stop, 22 - Async Pending, 23:25 - PMC Pm_state, 26:29 - Quiesce Arbitration State, 30:33 - PMC To Pow Spare)

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	POW_STATUS_THREAD_STATE: Thread state: quiesce => 0b1000 starting => 0b0100 run => 0b0010 stopping => 0b0001 Values: QUIESCE=>0b1000 STARTING=>0b0100 RUN=>0b0010 STOPPING=>0b0001

Bits	SCOM	Field Mnemonic: Description
4:5	ROX	PMC_POW_STATE: 00 - run, 01 - doze, 10 - nap, 11 - sleep/winkle Values: RUN=>0b00 DOZE=>0b01 NAP=>0b10 SLEEP=>0b11
6:8	ROX	PMC_SMT_MODE: 00 - power_on_ST, 01 - ST, 10 - SMT2, 11 - SMT4 Values: POWER_ON_ST=>0b000 ST=>0b001 SMT2_SH=>0b010 SMT2_SP=>0b011 SMT4=>0b100 SMT8=>0b101
9	ROX	HMI_INTR: hardware maintenance interrupt
10	ROX	Reserved field. (Access type is ext_intr)
11	ROX	DECR_INTR: decrementer interrupt
12	ROX	Reserved field. (Access type is debug_intr)
13	ROX	HDEC_INTR: hypervisor decrementer interrupt
14	ROX	Reserved field. (Access type is pmu_intr)
15	ROX	SP_ATTN_INTR: special attention interrupt
16:18	ROX	SRESET_TYPE: one of the switches and ldi al to set to force sreset through scan sreset_null => 0b000 sreset_req_and_thr_en => 0b001 sreset_req_and_thr_disa => 0b010 decr_intr_and_thr_disa => 0b011 ext_intr_and_thr_disa => 0b100 hmi_intr_and_thr_disa => 0b101 sdi_intr_and_thr_disa => 0b110 awake_from_sleep => 0b111 Values: SRESET_NULL=>0b000 SRESET_REQ_AND_THR_EN=>0b001 SRESET_REQ_AND_THR_DISA=>0b010 DECR_INTR_AND_THR_DISA=>0b011 EXT_INTR_AND_THR_DISA=>0b100 HMI_INTR_AND_THR_DISA=>0b101 SDI_INTR_AND_THR_DISA=>0b110 AWAKE_FROM_SLEEP=>0b111
19	ROX	Reserved field. (Access type is sreset_type) Values: SRESET_NULL=>0b000 SRESET_REQ_AND_THR_EN=>0b001 SRESET_REQ_AND_THR_DISA=>0b010 DECR_INTR_AND_THR_DISA=>0b011 EXT_INTR_AND_THR_DISA=>0b100 HMI_INTR_AND_THR_DISA=>0b101 SDI_INTR_AND_THR_DISA=>0b110 AWAKE_FROM_SLEEP=>0b111
20	ROX	SRESET_PENDING: one of the switches and ldi al to set to force sreset through scan
21	ROX	DBG_FETCH_STOP: pause fetching for debug workaround
22	ROX	ASYNC_PENDING: asynchronous interrupt pending



Register Name	<i>SPATTN Register</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL7.SPATTN
Address	0000000010013075 (SCOM1) 0000000010013076 (SCOM2) 0000000010013077 (SCOM)
Attributes	
Description	

Register Name	SPATTN_MASK Register
Mnemonic	EXP.EC.PC.PC_NE.TCTL7.SPATTN_MASK
Address	0000000010013078 (SCOM)
Attributes	
Description	

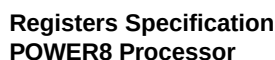


Bits	SCOM	Field Mnemonic: Description
2	RW	SPATTN_CORE_CHECKSTOP_RECOVERY_HANDSHAKE_MSK: Mask of core checkstop recovery handshake, alt: DABR SoftStop caused core quiesce
3	RW	SPATTN_CIABR QUIESCED_MSK: Mask of CIABR Quiesce caused core quiesce
4	RW	SPATTN_RECOVERY_BREAKPOINT_MSK: Mask of Attention from Core RECOVERY macro caused special attention
5	RW	SPATTN_NTC_ATTN_MSK: Mask of ntc_flush timeout
6	RW	SPATTN_THERM_MAX_MSK: Mask of edge detection on connected thermal maximum. External leveled signal detected
7	RW	SPATTN_SPR_INSTR_STOP_MSK: Mask of instruction Stop Request from Hypervisor via SPR
8:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>SDI Register</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL7.SDI
Address	0000000010013079 (SCOM1) 000000001001307A (SCOM2) 000000001001307B (SCOM)
Attributes	
Description	

Bits	SCOM1	SCOM2	SCOM	Field Mnemonic: Description
0	WOX_AND	WOX_OR	RWX	SDI_SW_USE_1: sw_use_1 - Available for use by Service Processor to get attention of the hypervisor
1	WOX_AND	WOX_OR	RWX	SDI_SW_USE_2: sw_use_2 - Available for use by Service Processor to get attention of the hypervisor
2	WOX_AND	WOX_OR	RWX	SDI_SW_USE_3: sw_use_3 - Available for use by Service Processor to get attention of the hypervisor
3	WOX_AND	WOX_OR	RWX	SDI_HANG_RECV_OR_CHSW QUIESCE_TIMEOUT: Hang Recovery or chsw Quiesce Timeout
4	WOX_AND	WOX_OR	RWX	SDI_EXT_TRIGGER: RAS trigger
5	WOX_AND	WOX_OR	RWX	SDI_COREHANG: Thread Hang with CORE Source indication (modeable)
6	WOX_AND	WOX_OR	RWX	SDI_AMBIHANG: Thread Hang with AMBIGUOUS Source indication (modeable)
7	WOX_AND	WOX_OR	RWX	SDI_NESTHANG: Thread Hang with NEST Source indication (modeable)
8:63	RO	RO	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>SDI_MASK Register</i>
Mnemonic	EXP.EC.PC.PC_NE.TCTL7.SDI_MASK
Address	000000001001307C (SCOM)
Attributes	
Description	



Register Name	PC_NE Error Report Hold_out Register7
Mnemonic	EXP.EC.PC.PC_NE.PCNE_REG7_HOLD_OUT
Address	000000001001307D (SCOM)
Attributes	
Description	

[illegible]



Register Name	Core Fault Isolation Register
Mnemonic	EXP.EC.PC.PC_NE.FIR.CORE_FIR
Address	0000000010013100 (SCOM) 0000000010013101 (SCOM1) 0000000010013102 (SCOM2)
Attributes	Secure=true
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	IFU_SRAM_PARITY_ERR: SRAM recoverable error (ICACHE parity error, etc.)
1	RWX	WOX_AND	WOX_OR	IF_SETDELETE_ERR: set deleted
2	RWX	WOX_AND	WOX_OR	IF_RFILE_REC_ERR: RegFile recoverable error
3	RWX	WOX_AND	WOX_OR	IF_RFILE_CHKSTOP_ERR: RegFile core check stop
4	RWX	WOX_AND	WOX_OR	IF_LOG_REC_ERR: logic recoverable error
5	RWX	WOX_AND	WOX_OR	IF_LOG_CHKSTOP_ERR: logic core check stop
6	RWX	WOX_AND	WOX_OR	IF_NOT_MT_REC_ERR: recoverable if not in MT window
7	RWX	WOX_AND	WOX_OR	IF_CHKSTOP_ERR: system check stop
8	RWX	WOX_AND	WOX_OR	RECOV_FIR_CHKSTOP_ERR: recovery core check stop
9	RWX	WOX_AND	WOX_OR	SD_RFILE_REC_ERR: RegFile recoverable error
10	RWX	WOX_AND	WOX_OR	SD_RFILE_CHKSTOP_ERR: RegFile core check stop (mapper error)
11	RWX	WOX_AND	WOX_OR	SD_LOG_REC_ERR: logic recoverable error
12	RWX	WOX_AND	WOX_OR	SD_LOG_CHKSTOP_ERR: logic core check stop
13	RWX	WOX_AND	WOX_OR	SD_NOT_MT_REC_ERR: recoverable if not in MT window
14	RWX	WOX_AND	WOX_OR	SD_MCHK_AND_ME_EQ_0: MCHK received while ME=0 non recoverable
15	RWX	WOX_AND	WOX_OR	SD_PC_L2_UE_ERR: UE from L2
16	RWX	WOX_AND	WOX_OR	ISU_L2_UE_OVER_TH_ERR: Number of UEs from L2 above threshold
17	RWX	WOX_AND	WOX_OR	SD_PC_CI_UE: UE on CI load
18	RWX	WOX_AND	WOX_OR	UNUSED_18: reserved
19	RWX	WOX_AND	WOX_OR	FX_GPR_REC_ERR: GPR recoverable error
20	RWX	WOX_AND	WOX_OR	SD_PC_SYS_XSTOP: reserved
21	RWX	WOX_AND	WOX_OR	FX_LOG_CHKSTOP_ERR: logic core check stop
22	RWX	WOX_AND	WOX_OR	FX_NOT_MT_REC_ERR: recoverable if not in MT window
23	RWX	WOX_AND	WOX_OR	VS_VRF_REC_ERR: VRF recoverable error
24	RWX	WOX_AND	WOX_OR	VS_LOG_REC_ERR: logic recoverable error
25	RWX	WOX_AND	WOX_OR	VS_LOG_CHKSTOP_ERR: logic core check stop
26	RWX	WOX_AND	WOX_OR	RECOV_IN_MAINT_ERR: 26 = recov_in_maint
27	RWX	WOX_AND	WOX_OR	DU_LOG_REC_ERR: logic recoverable error
28	RWX	WOX_AND	WOX_OR	RECOV_DIS_SYS_XSTOP: logic core check stop
29	RWX	WOX_AND	WOX_OR	LSU_SRAM_PARITY_ERR: SRAM recoverable error (DCACHE parity error, etc.)
30	RWX	WOX_AND	WOX_OR	LS_SETDELETE_ERR: set deleted

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
31	RWX	WOX_AND	WOX_OR	LS_RFILE_REC_ERR: RegFile recoverable error
32	RWX	WOX_AND	WOX_OR	LS_RFILE_CHKSTOP_ERR: RegFile core check stop
33	RWX	WOX_AND	WOX_OR	LS_TLB_MULTIHIT_ERR: special recovery error TLB multi-hit error occurred
34	RWX	WOX_AND	WOX_OR	LS_SLB_MULTIHIT_ERR: special recovery error SLBFEE multi-hit error occurred
35	RWX	WOX_AND	WOX_OR	LS_DERAT_MULTIHIT_ERR: special recovery error ERAT multi-hit error occurred
36	RWX	WOX_AND	WOX_OR	FORWARD_PROGRESS_ERR: forward progress error
37	RWX	WOX_AND	WOX_OR	LS_LOG_REC_ERR: logic recoverable error
38	RWX	WOX_AND	WOX_OR	LS_LOG_CHKSTOP_ERR: logic core check stop
39	RWX	WOX_AND	WOX_OR	LS_NOT_MT_REC_ERR: recoverable if not in MT window
40	RWX	WOX_AND	WOX_OR	LS_NOT_CI_REC_ERR: recoverable if not in CI window
41	RWX	WOX_AND	WOX_OR	LS_CHKSTOP_ERR: system check stop
42	RWX	WOX_AND	WOX_OR	UNUSED_42: UE from GPR/VRF recovery process
43	RWX	WOX_AND	WOX_OR	THREAD_HANG_REC_ERR: thread hang recoverable error
44	RWX	WOX_AND	WOX_OR	FIR_LOG_RECOV_ERR: logic recoverable error
45	RWX	WOX_AND	WOX_OR	PC_LOG_CHKSTOP_ERR: PC logic core check stop
46	RWX	WOX_AND	WOX_OR	UNUSED_46: reserved
47	RWX	WOX_AND	WOX_OR	TFC_FIR_TFMR_P_ERR: TFMR Parity Error (timing facility may be corrupt)
48	RWX	WOX_AND	WOX_OR	SPRD_FIR_HYP_RES_P_ERR: Hypervisor Resource error - core check stop
49	RWX	WOX_AND	WOX_OR	TFC_FIR_P_ERR: TFAC parity error
50	RWX	WOX_AND	WOX_OR	TFC_FIR_CONTROL_ERR: TFAC control error
51	RWX	WOX_AND	WOX_OR	PC_FIRM_AND_SEL_ERR: TFAC firmware error and select error
52	RWX	WOX_AND	WOX_OR	CORE_HUNG: Hang recovery failed (core check stop)
53	RWX	WOX_AND	WOX_OR	CORE_HANG_DETECT: Internal hang detected (core hang)
54	RWX	WOX_AND	WOX_OR	AMBI_HANG_DETECT: Hang detected unknown source
55	RWX	WOX_AND	WOX_OR	NEST_HANG_DETECT: External Hang detected
56	RWX	WOX_AND	WOX_OR	UNUSED_56: reserved
57	RWX	WOX_AND	WOX_OR	UNUSED_57: reserved
58	RWX	WOX_AND	WOX_OR	UNUSED_58: reserved
59	RWX	WOX_AND	WOX_OR	PC_SCOM_ERR: SCOM satellite error detected
60	RWX	WOX_AND	WOX_OR	DBG_FIR_CHECKSTOP_ON_TRIGGER: debug Trigger Error inject
61	RWX	WOX_AND	WOX_OR	SP_INJ_REC_ERR: SCOM or Firmware recoverable Error Inject
62	RWX	WOX_AND	WOX_OR	SP_INJ_XSTOP_ERR: Firmware Xstop Error Inject
63	RWX	WOX_AND	WOX_OR	SPRD_PHY_P_ERR_INJ: Phyp Xstop via SPRC / SPRD



Register Name	Core FIR Mask Register
Mnemonic	EXP.EC.PC.PC_NE.FIR.CORE_FIRMASK
Address	0000000010013103 (SCOM) 0000000010013104 (SCOM1) 0000000010013105 (SCOM2)
Attributes	Secure=true
Description	

Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
0	RW	WO_AND	WO_OR	MASK_IFU_SRAM_PARITY_ERR: SRAM recoverable error (ICACHE parity error, etc.)
1	RW	WO_AND	WO_OR	MASK_IF_SETDELETE_ERR: set deleted
2	RW	WO_AND	WO_OR	MASK_IF_RFILE_REC_ERR: RegFile recoverable error
3	RW	WO_AND	WO_OR	MASK_IF_RFILE_CHKSTOP_ERR: RegFile core check stop
4	RW	WO_AND	WO_OR	MASK_IF_LOG_REC_ERR: logic recoverable error
5	RW	WO_AND	WO_OR	MASK_IF_LOG_CHKSTOP_ERR: logic core check stop
6	RW	WO_AND	WO_OR	MASK_IF_NOT_MT_REC_ERR: recoverable if not in MT window
7	RW	WO_AND	WO_OR	MASK_IF_CHKSTOP_ERR: system check stop
8	RW	WO_AND	WO_OR	MASK_RECOV_FIR_CHKSTOP_ERR: recovery core check stop
9	RW	WO_AND	WO_OR	MASK_SD_RFILE_REC_ERR: RegFile recoverable error
10	RW	WO_AND	WO_OR	MASK_SD_RFILE_CHKSTOP_ERR: RegFile core check stop (mapper error)
11	RW	WO_AND	WO_OR	MASK_SD_LOG_REC_ERR: logic recoverable error
12	RW	WO_AND	WO_OR	MASK_SD_LOG_CHKSTOP_ERR: logic core check stop
13	RW	WO_AND	WO_OR	MASK_SD_NOT_MT_REC_ERR: recoverable if not in MT window
14	RW	WO_AND	WO_OR	MASK_SD_MCHK_AND_ME_EQ_0: MCHK received while ME=0+E332 non recoverable
15	RW	WO_AND	WO_OR	MASK_SD_PC_L2_UE_ERR: UE from L2
16	RW	WO_AND	WO_OR	MASK_ISU_L2_UE_OVER_TH_ERR: Number of UEs from L2 above threshold
17	RW	WO_AND	WO_OR	MASK_SD_PC_CI_UE: UE on CI load
18	RW	WO_AND	WO_OR	MASK_UNUSED_18: reserved
19	RW	WO_AND	WO_OR	MASK_FX_GPR_REC_ERR: GPR recoverable error
20	RW	WO_AND	WO_OR	MASK_SD_PC_SYS_XSTOP: reserved
21	RW	WO_AND	WO_OR	MASK_FX_LOG_CHKSTOP_ERR: logic core check stop
22	RW	WO_AND	WO_OR	MASK_FX_NOT_MT_REC_ERR: recoverable if not in MT window
23	RW	WO_AND	WO_OR	MASK_VS_VRF_REC_ERR: VRF recoverable error
24	RW	WO_AND	WO_OR	MASK_VS_LOG_REC_ERR: logic recoverable error
25	RW	WO_AND	WO_OR	MASK_VS_LOG_CHKSTOP_ERR: logic core check stop
26	RW	WO_AND	WO_OR	MASK_RECOV_IN_MAINT: recov_in_maint
27	RW	WO_AND	WO_OR	MASK_DU_LOG_REC_ERR: logic recoverable error
28	RW	WO_AND	WO_OR	MASK_RECOV_DIS_SYS_XSTOP: logic core check stop

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Bits	SCOM	SCOM1	SCOM2	Field Mnemonic: Description
29	RW	WO_AND	WO_OR	MASK_LSU_SRAM_PARITY_ERR: SRAM recoverable error (DCACHE parity error, etc.)
30	RW	WO_AND	WO_OR	MASK_LS_SETDELETE_ERR: set deleted
31	RW	WO_AND	WO_OR	MASK_LS_RFILE_REC_ERR: RegFile recoverable error
32	RW	WO_AND	WO_OR	MASK_LS_RFILE_CHKSTOP_ERR: RegFile core check stop
33	RW	WO_AND	WO_OR	MASK_LS_TLB_MULTIHIT_ERR: special recovery error TLB multi-hit error occurred
34	RW	WO_AND	WO_OR	MASK_LS_SLB_MULTIHIT_ERR: special recovery error SLBFEE multi-hit error occurred
35	RW	WO_AND	WO_OR	MASK_LS_DERAT_MULTIHIT_ERR: special recovery error ERAT multi-hit error occurred
36	RW	WO_AND	WO_OR	MASK_FORWARD_PROGRESS_ERR: reserved
37	RW	WO_AND	WO_OR	MASK_LS_LOG_REC_ERR: logic recoverable error
38	RW	WO_AND	WO_OR	MASK_LS_LOG_CHKSTOP_ERR: logic core check stop
39	RW	WO_AND	WO_OR	MASK_LS_NOT_MT_REC_ERR: recoverable if not in MT window
40	RW	WO_AND	WO_OR	MASK_LS_NOT_CI_REC_ERR: recoverable if not in CI window
41	RW	WO_AND	WO_OR	MASK_LS_CHKSTOP_ERR: system check stop
42	RW	WO_AND	WO_OR	MASK_UNUSED_42: UE from GPR/VRF recovery process
43	RW	WO_AND	WO_OR	MASK_THREAD_HANG_REC_ERR: thread hang recoverable error
44	RW	WO_AND	WO_OR	MASK_FIR_LOG_RECOV_ERR: logic recoverable error
45	RW	WO_AND	WO_OR	MASK_PC_LOG_CHKSTOP_ERR: PC logic core check stop
46	RW	WO_AND	WO_OR	MASK_UNUSED_46: PC recoverable if not in MT window
47	RW	WO_AND	WO_OR	MASK_TFC_FIR_TFMR_P_ERR: TFMR Parity Error (timing facility may be corrupt)
48	RW	WO_AND	WO_OR	MASK_SPRD_FIR_HYP_RES_P_ERR: Hypervisor Resource error - core check stop
49	RW	WO_AND	WO_OR	MASK_TFC_FIR_P_ERR: TFAC parity error
50	RW	WO_AND	WO_OR	MASK_TFC_FIR_CONTROL_ERR: TFAC control error
51	RW	WO_AND	WO_OR	MASK_PC_FIRM_AND_SEL_ERR: TFAC firmware error and select error
52	RW	WO_AND	WO_OR	MASK_CORE_HUNG: Hang recovery failed (core check stop)
53	RW	WO_AND	WO_OR	MASK_CORE_HANG_DETECT: Internal hang detected (core hang)
54	RW	WO_AND	WO_OR	MASK_AMBI_HANG_DETECT: Hang detected unknown source
55	RW	WO_AND	WO_OR	MASK_NEST_HANG_DETECT: External Hang detected
56	RW	WO_AND	WO_OR	MASK_UNUSED_56: Thermal alert
57	RW	WO_AND	WO_OR	MASK_UNUSED_57: Xstop from thermal
58	RW	WO_AND	WO_OR	MASK_UNUSED_58: Xstop from Chiplet
59	RW	WO_AND	WO_OR	MASK_PC_SCOM_ERR: SCOM satellite error detected
60	RW	WO_AND	WO_OR	MASK_DBG_FIR_CHECKSTOP_ON_TRIGGER: debug Trigger Error inject
61	RW	WO_AND	WO_OR	MASK_SP_INJ_REC_ERR: SCOM or Firmware recoverable Error Inject
62	RW	WO_AND	WO_OR	MASK_SP_INJ_XSTOP_ERR: Firmware Xstop Error Inject
63	RW	WO_AND	WO_OR	MASK_SPRD_PHYP_ERR_INJ: Hypervisor Xstop via SPRC / SPRD



Register Name	<i>Core FIR Action 0 Register</i>
Mnemonic	EXP.EC.PC.PC_NE.FIR.CORE_ACTION0
Address	0000000010013106 (SCOM)
Attributes	Secure=true
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	ACT0_IFU_SRAM_PARITY_ERR: SRAM recoverable error (ICACHE parity error, etc.)
1	RW	ACT0_IF_SETDELETE_ERR: set deleted
2	RW	ACT0_IF_RFILE_REC_ERR: RegFile recoverable error
3	RW	ACT0_IF_RFILE_CHKSTOP_ERR: RegFile core check stop
4	RW	ACT0_IF_LOG_REC_ERR: logic recoverable error
5	RW	ACT0_IF_LOG_CHKSTOP_ERR: logic core check stop
6	RW	ACT0_IF_NOT_MT_REC_ERR: recoverable if not in MT window
7	RW	ACT0_IF_CHKSTOP_ERR: system check stop
8	RW	ACT0_RECOV_FIR_CHKSTOP_ERR: recovery core check stop
9	RW	ACT0_SD_RFILE_REC_ERR: RegFile recoverable error
10	RW	ACT0_SD_RFILE_CHKSTOP_ERR: RegFile core check stop (mapper error)
11	RW	ACT0_SD_LOG_REC_ERR: logic recoverable error
12	RW	ACT0_SD_LOG_CHKSTOP_ERR: logic core check stop
13	RW	ACT0_SD_NOT_MT_REC_ERR: recoverable if not in MT window
14	RW	ACT0_SD_MCHK_AND_ME_EQ_0: MCHK received while ME=0+E134 non recoverable
15	RW	ACT0_SD_PC_L2_UE_ERR: UE from L2
16	RW	ACT0_ISU_L2_UE_OVER_TH_ERR: Number of UEs from L2 above threshold
17	RW	ACT0_SD_PC_CI_UE: UE on CI load
18	RW	ACT0_UNUSED_18: reserved
19	RW	ACT0_FX_GPR_REC_ERR: GPR recoverable error
20	RW	ACT0_SD_PC_SYS_XSTOP: reserved
21	RW	ACT0_FX_LOG_CHKSTOP_ERR: logic core check stop
22	RW	ACT0_FX_NOT_MT_REC_ERR: recoverable if not in MT window
23	RW	ACT0_VS_VRF_REC_ERR: VRF recoverable error
24	RW	ACT0_VS_LOG_REC_ERR: logic recoverable error
25	RW	ACT0_VS_LOG_CHKSTOP_ERR: logic core check stop
26	RW	ACT0_RECOV_IN_MAINT: recov_in_maint
27	RW	ACT0_DU_LOG_REC_ERR: logic recoverable error
28	RW	ACT0_RECOV_DIS_SYS_XSTOP: logic core check stop
29	RW	ACT0_LSU_SRAM_PARITY_ERR: SRAM recoverable error (DCACHE parity error, etc.)
30	RW	ACT0_LS_SETDELETE_ERR: set deleted
31	RW	ACT0_LS_RFILE_REC_ERR: RegFile recoverable error

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Bits	SCOM	Field Mnemonic: Description
32	RW	ACT0_LS_RFILE_CHKSTOP_ERR: RegFile core check stop
33	RW	ACT0_LS_TLB_MULTIHIT_ERR: special recovery error TLB multi-hit error occurred
34	RW	ACT0_LS_SLB_MULTIHIT_ERR: special recovery error SLBFEE multi-hit error occurred
35	RW	ACT0_LS_DERAT_MULTIHIT_ERR: special recovery error ERAT multi-hit error occurred
36	RW	ACT0_FORWARD_PROGRESS_ERR: reserved
37	RW	ACT0_LS_LOG_REC_ERR: logic recoverable error
38	RW	ACT0_LS_LOG_CHKSTOP_ERR: logic core check stop
39	RW	ACT0_LS_NOT_MT_REC_ERR: recoverable if not in MT window
40	RW	ACT0_LS_NOT_CI_REC_ERR: recoverable if not in CI window
41	RW	ACT0_LS_CHKSTOP_ERR: system check stop
42	RW	ACT0_UNUSED_42: UE from GPR/VRF recovery process
43	RW	ACT0_THREAD_HANG_REC_ERR: thread hang recoverable error
44	RW	ACT0_FIR_LOG_RECOV_ERR: logic recoverable error
45	RW	ACT0_PC_LOG_CHKSTOP_ERR: PC logic core check stop
46	RW	ACT0_UNUSED_46: PC recoverable if not in MT window
47	RW	ACT0_TFC_FIR_TFMR_P_ERR: TFMR Parity Error (timing facility may be corrupt)
48	RW	ACT0_SPRD_FIR_HYP_RES_P_ERR: Hypervisor Resource error - core check stop
49	RW	ACT0_TFC_FIR_P_ERR: TFAC parity error
50	RW	ACT0_TFC_FIR_CONTROL_ERR: TFAC control error
51	RW	ACT0_PC_FIRM_AND_SEL_ERR: TFAC firmware error and select error
52	RW	ACT0_CORE_HUNG: Hang recovery failed (core check stop)
53	RW	ACT0_CORE_HANG_DETECT: Internal hang detected (core hang)
54	RW	ACT0_AMBI_HANG_DETECT: Hang detected unknown source
55	RW	ACT0_NEST_HANG_DETECT: External Hang detected
56	RW	ACT0_UNUSED_56: Thermal alert
57	RW	ACT0_UNUSED_57: Xstop from thermal
58	RW	ACT0_UNUSED_58: Xstop from Chiplet
59	RW	ACT0_PC_SCOM_ERR: SCOM satellite error detected
60	RW	ACT0_DBG_FIR_CHECKSTOP_ON_TRIGGER: debug Trigger Error inject
61	RW	ACT0_SP_INJ_REC_ERR: SCOM or Firmware recoverable Error Inject
62	RW	ACT0_SP_INJ_XSTOP_ERR: Firmware Xstop Error Inject
63	RW	ACT0_SPRD_PHYP_ERR_INJ: Hypervisor Xstop via SPRC / SPRD

Register Name	Core FIR Action 1 Register
Mnemonic	EXP.EC.PC.PC_NE.FIR.CORE_ACTION1
Address	0000000010013107 (SCOM)
Attributes	Secure=true
Description	



Bits	SCOM	Field Mnemonic: Description
0	RW	ACT1_IFU_SRAM_PARITY_ERR: SRAM recoverable error (ICACHE parity error, etc.)
1	RW	ACT1_IF_SETDELETE_ERR: set deleted
2	RW	ACT1_IF_RFILE_REC_ERR: RegFile recoverable error
3	RW	ACT1_IF_RFILE_CHKSTOP_ERR: RegFile core check stop
4	RW	ACT1_IF_LOG_REC_ERR: logic recoverable error
5	RW	ACT1_IF_LOG_CHKSTOP_ERR: logic core check stop
6	RW	ACT1_IF_NOT_MT_REC_ERR: recoverable if not in MT window
7	RW	ACT1_IF_CHKSTOP_ERR: system check stop
8	RW	ACT1_RECOV_FIR_CHKSTOP_ERR: recovery core check stop
9	RW	ACT1_SD_RFILE_REC_ERR: RegFile recoverable error
10	RW	ACT1_SD_RFILE_CHKSTOP_ERR: RegFile core check stop (mapper error)
11	RW	ACT1_SD_LOG_REC_ERR: logic recoverable error
12	RW	ACT1_SD_LOG_CHKSTOP_ERR: logic core check stop
13	RW	ACT1_SD_NOT_MT_REC_ERR: recoverable if not in MT window
14	RW	ACT1_SD_MCHK_AND_ME_EQ_0: MCHK received while ME=0 non recoverable
15	RW	ACT1_SD_PC_L2_UE_ERR: UE from L2
16	RW	ACT1_ISU_L2_UE_OVER_TH_ERR: Number of UEs from L2 above threshold
17	RW	ACT1_SD_PC_CI_UE: UE on CI load
18	RW	ACT1_UNUSED_18: reserved
19	RW	ACT1_FX_GPR_REC_ERR: GPR recoverable error
20	RW	ACT1_SD_PC_SYS_XSTOP: reserved
21	RW	ACT1_FX_LOG_CHKSTOP_ERR: logic core check stop
22	RW	ACT1_FX_NOT_MT_REC_ERR: recoverable if not in MT window
23	RW	ACT1_VS_VRF_REC_ERR: VRF recoverable error
24	RW	ACT1_VS_LOG_REC_ERR: logic recoverable error
25	RW	ACT1_VS_LOG_CHKSTOP_ERR: logic core check stop
26	RW	ACT1_RECOV_IN_MAINT: recov_in_maint
27	RW	ACT1_DU_LOG_REC_ERR: logic recoverable error
28	RW	ACT1_RECOV_DIS_SYS_XSTOP: logic core check stop
29	RW	ACT1_LSU_SRAM_PARITY_ERR: SRAM recoverable error (DCACHE parity error, etc.)
30	RW	ACT1_LS_SETDELETE_ERR: set deleted
31	RW	ACT1_LS_RFILE_REC_ERR: RegFile recoverable error
32	RW	ACT1_LS_RFILE_CHKSTOP_ERR: RegFile core check stop
33	RW	ACT1_LS_TLB_MULTIHIT_ERR: special recovery error TLB multi-hit error occurred
34	RW	ACT1_LS_SLB_MULTIHIT_ERR: special recovery error SLBFEE multi-hit error occurred
35	RW	ACT1_LS_DERAT_MULTIHIT_ERR: special recovery error ERAT multi-hit error occurred
36	RW	ACT1_FORWARD_PROGRESS_ERR: reserved
37	RW	ACT1_LS_LOG_REC_ERR: logic recoverable error
38	RW	ACT1_LS_LOG_CHKSTOP_ERR: logic core check stop

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Bits	SCOM	Field Mnemonic: Description
39	RW	ACT1_LS_NOT_MT_REC_ERR: recoverable if not in MT window
40	RW	ACT1_LS_NOT_CI_REC_ERR: recoverable if not in CI window
41	RW	ACT1_LS_CHKSTOP_ERR: system check stop
42	RW	ACT1_UNUSED_42: UE from GPR/VRF recovery process
43	RW	ACT1_THREAD_HANG_REC_ERR: thread hang recoverable error
44	RW	ACT1_FIR_LOG_RECOV_ERR: logic recoverable error
45	RW	ACT1_PC_LOG_CHKSTOP_ERR: PC logic core check stop
46	RW	ACT1_UNUSED_46: PC recoverable if not in MT window
47	RW	ACT1_TFC_FIR_TFMR_P_ERR: TFMR Parity Error (timing facility may be corrupt)
48	RW	ACT1_SPRD_FIR_HYP_RES_P_ERR: Hypervisor Resource error - core check stop
49	RW	ACT1_TFC_FIR_P_ERR: TFAC parity error
50	RW	ACT1_TFC_FIR_CONTROL_ERR: TFAC control error
51	RW	ACT1_PC_FIRM_AND_SEL_ERR: TFAC firmware error and select error
52	RW	ACT1_CORE_HUNG: Hang recovery failed (core check stop)
53	RW	ACT1_CORE_HANG_DETECT: Internal hang detected (core hang)
54	RW	ACT1_AMBI_HANG_DETECT: Hang detected unknown source
55	RW	ACT1_NEST_HANG_DETECT: External Hang detected
56	RW	ACT1_UNUSED_56: Thermal alert
57	RW	ACT1_UNUSED_57: Xstop from thermal
58	RW	ACT1_UNUSED_58: Xstop from Chiplet
59	RW	ACT1_PC_SCOM_ERR: SCOM satellite error detected
60	RW	ACT1_DBG_FIR_CHECKSTOP_ON_TRIGGER: debug Trigger Error inject
61	RW	ACT1_SP_INJ_REC_ERR: SCOM or Firmware recoverable Error Inject
62	RW	ACT1_SP_INJ_XSTOP_ERR: Firmware Xstop Error Inject
63	RW	ACT1_SPRD_PHPY_ERR_INJ: Hypervisor Xstop via SPRC / SPRD

Register Name	Core Who-s-on-first Register
Mnemonic	EXP.EC.PC.PC_NE.FIR.CORE_WOF
Address	0000000010013108 (SCOM)
Attributes	Secure=true
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX_WCLRR EG	WOF_IFU_SRAM_PARITY_ERR: SRAM recoverable error (ICACHE parity error, etc.)
1	RWX_WCLRR EG	WOF_IF_SETDELETE_ERR: set deleted
2	RWX_WCLRR EG	WOF_IF_RFILE_REC_ERR: RegFile recoverable error



Bits	SCOM	Field Mnemonic: Description
3	RWX_WCLRR EG	WOF_IF_RFILE_CHKSTOP_ERR: RegFile core check stop
4	RWX_WCLRR EG	WOF_IF_LOG_REC_ERR: logic recoverable error
5	RWX_WCLRR EG	WOF_IF_LOG_CHKSTOP_ERR: logic core check stop
6	RWX_WCLRR EG	WOF_IF_NOT_MT_REC_ERR: recoverable if not in MT window
7	RWX_WCLRR EG	WOF_IF_CHKSTOP_ERR: system check stop
8	RWX_WCLRR EG	WOF_RECOV_FIR_CHKSTOP_ERR: recovery core check stop
9	RWX_WCLRR EG	WOF_SD_RFILE_REC_ERR: RegFile recoverable error
10	RWX_WCLRR EG	WOF_SD_RFILE_CHKSTOP_ERR: RegFile core check stop (mapper error)
11	RWX_WCLRR EG	WOF_SD_LOG_REC_ERR: logic recoverable error
12	RWX_WCLRR EG	WOF_SD_LOG_CHKSTOP_ERR: logic core check stop
13	RWX_WCLRR EG	WOF_SD_NOT_MT_REC_ERR: recoverable if not in MT window
14	RWX_WCLRR EG	WOF_SD_MCHK_AND_ME_EQ_0: MCHK received while ME=0 non recoverable
15	RWX_WCLRR EG	WOF_SD_PC_L2_UE_ERR: UE from L2
16	RWX_WCLRR EG	WOF_ISU_L2_UE_OVER_TH_ERR: Number of UEs from L2 above threshold
17	RWX_WCLRR EG	WOF_SD_PC_CI_UE: UE on CI load
18	RWX_WCLRR EG	WOF_UNUSED_18: reserved
19	RWX_WCLRR EG	WOF_FX_GPR_REC_ERR: GPR recoverable error
20	RWX_WCLRR EG	WOF_SD_PC_SYS_XSTOP: reserved
21	RWX_WCLRR EG	WOF_FX_LOG_CHKSTOP_ERR: logic core check stop
22	RWX_WCLRR EG	WOF_FX_NOT_MT_REC_ERR: recoverable if not in MT window
23	RWX_WCLRR EG	WOF_VS_VRF_REC_ERR: VRF recoverable error
24	RWX_WCLRR EG	WOF_VS_LOG_REC_ERR: logic recoverable error
25	RWX_WCLRR EG	WOF_VS_LOG_CHKSTOP_ERR: logic core check stop
26	RWX_WCLRR EG	WOF_RECOV_IN_MAINT: recov_in_maint

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Bits	SCOM	Field Mnemonic: Description
27	RWX_WCLRR EG	WOF_DU_LOG_REC_ERR: logic recoverable error
28	RWX_WCLRR EG	WOF_RECOV_DIS_SYS_XSTOP: logic core check stop
29	RWX_WCLRR EG	WOF_LSU_SRAM_PARITY_ERR: SRAM recoverable error (DCACHE parity error, etc.)
30	RWX_WCLRR EG	WOF_LS_SETDELETE_ERR: set deleted
31	RWX_WCLRR EG	WOF_LS_RFILE_REC_ERR: RegFile recoverable error
32	RWX_WCLRR EG	WOF_LS_RFILE_CHKSTOP_ERR: RegFile core check stop
33	RWX_WCLRR EG	WOF_LS_TLB_MULTIHIT_ERR: special recovery error TLB multi-hit error occurred
34	RWX_WCLRR EG	WOF_LS_SLB_MULTIHIT_ERR: special recovery error SLBFEE multi-hit error occurred
35	RWX_WCLRR EG	WOF_LS_DERAT_MULTIHIT_ERR: special recovery error ERAT multi-hit error occurred
36	RWX_WCLRR EG	WOF_FORWARD_PROGRESS_ERR: reserved
37	RWX_WCLRR EG	WOF_LS_LOG_REC_ERR: logic recoverable error
38	RWX_WCLRR EG	WOF_LS_LOG_CHKSTOP_ERR: logic core check stop
39	RWX_WCLRR EG	WOF_LS_NOT_MT_REC_ERR: recoverable if not in MT window
40	RWX_WCLRR EG	WOF_LS_NOT_CI_REC_ERR: recoverable if not in CI window
41	RWX_WCLRR EG	WOF_LS_CHKSTOP_ERR: system check stop
42	RWX_WCLRR EG	WOF_UNUSED_42: UE from GPR/VRF recovery process
43	RWX_WCLRR EG	WOF_THREAD_HANG_REC_ERR: thread hang recoverable error
44	RWX_WCLRR EG	WOF_FIR_LOG_RECOV_ERR: logic recoverable error
45	RWX_WCLRR EG	WOF_PC_LOG_CHKSTOP_ERR: PC logic core check stop
46	RWX_WCLRR EG	WOF_UNUSED_46: PC recoverable if not in MT window
47	RWX_WCLRR EG	WOF_TFC_FIR_TFMR_P_ERR: TFMR Parity Error (timing facility may be corrupt)
48	RWX_WCLRR EG	WOF_SPRD_FIR_HYP_RES_P_ERR: Hypervisor Resource error - core check stop
49	RWX_WCLRR EG	WOF_TFC_FIR_P_ERR: TFAC parity error
50	RWX_WCLRR EG	WOF_TFC_FIR_CONTROL_ERR: TFAC control error



Bits	SCOM	Field Mnemonic: Description
51	RWX_WCLRR EG	WOF_PC_FIRM_AND_SEL_ERR: TFAC firmware error and select error
52	RWX_WCLRR EG	WOF_CORE_HUNG: Hang recovery failed (core check stop)
53	RWX_WCLRR EG	WOF_CORE_HANG_DETECT: Internal hang detected (core hang)
54	RWX_WCLRR EG	WOF_AMBI_HANG_DETECT: Hang detected unknown source
55	RWX_WCLRR EG	WOF_NEST_HANG_DETECT: External Hang detected
56	RWX_WCLRR EG	WOF_UNUSED_56: Thermal alert
57	RWX_WCLRR EG	WOF_UNUSED_57: Xstop from thermal
58	RWX_WCLRR EG	WOF_UNUSED_58: Xstop from Chiplet
59	RWX_WCLRR EG	WOF_PC_SCOM_ERR: SCOM satellite error detected
60	RWX_WCLRR EG	WOF_DBG_FIR_CHECKSTOP_ON_TRIGGER: debug Trigger Error inject
61	RWX_WCLRR EG	WOF_SP_INJ_REC_ERR: SCOM or Firmware recoverable Error Inject
62	RWX_WCLRR EG	WOF_SP_INJ_XSTOP_ERR: Firmware Xstop Error Inject
63	RWX_WCLRR EG	WOF_SPRD_PHYP_ERR_INJ: Hypervisor Xstop via SPRC / SPRD

Register Name	<i>RANDOM LFSR To Support Random Pulse Generation In Thread Control</i>
Mnemonic	EXP.EC.PC.PC_NE.FIR.FIR_RANDOMLFSR
Address	0000000010013109 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RO	constant=0b00000000
8:31	RWX	RAND_LFSR_LT: pre-set for random pulse generation
32:63	RO	constant=0b00000000000000000000000000000000

Register Name	<i>Error Injection Control Register</i>
Mnemonic	EXP.EC.PC.PC_NE.FIR.FIR_ERRINJREG
Address	000000001001310A (SCOM)
Attributes	Secure=true
Description	

Registers Specification

POWER8 Processor

Bits	SCOM	Field Mnemonic: Description
0	RW	ERR_INJ_TO_LSU: Error Injection
1	RW	ERR_INJ_TO_IFU: Error Injection
2	RW	ERR_INJ_TO_ISU: Error Injection
3	RW	ERR_INJ_TO_FXU: Error Injection
4	RW	ERR_INJ_TO_VSU: Error Injection
5	RW	ERR_INJ_TO_PC: Error Injection
6	RW	ERROR_PULSE_OR_LEVEL: 0 inject is a pulse, 1 inject is a level
7	RW	CLEAR_STICKY_LEVEL: Clear sticky latch used for level
8	RW	ERR_INJ_SCOM_WRITE: SCOM write
9	RW	ERR_INJ_TRIGGER: Trigger 0
10	RW	ERR_INJ_TRIGGER1: Trigger 1
11	RW	ERR_INJ_TOD_TAP: TOD-tap
12:13	RW	ERR_INJ_BLOCK_LT: block select 00 - disable block by HV mode 01 - block if any thread is in HV mode 10 - block if all threads are in HV mode
14	RW	ERR_INJ_DELAY_AFTER_BLOCK: inject is delayed for 32 cycle after block
15	RW	ERR_INJ_RECOVERY_BLK: injection is blocked during recovery active
16	RW	ERR_INJ_RECOVERY_BLK_EXTEND: extend recovery block till forward progress
17:20	RW	ERR_INJ_TAP_SEL_LT: tap select 0000 => .5 ms 0001 => 1.0 ms 0010 => 2.0 ms 0011 => 4.1 ms 0100 => 8.2 ms 0101 => 16.4 ms 0110 => 32.8 ms 0111 => 65.5 ms 1000 => 131.0 ms 1001 => 262.1 ms 1010 => 524.3 ms 1011 => 1.0 s 1100 => 2.0 s 1101 => 4.2 s 1110 => 8.4 s 1111 => 16.8 s
21:23	RW	ERR_INJ_HYP_BLOCK: 0xx => ignore HV and PR bits 1HP => block inject if MSR(HV) = H and MSR(PR) = P for any active thread

Register Name	<i>Recovery Threshold And Random Control</i>
Mnemonic	EXP.EC.PC.PC_NE.FIR.RECOV_THRESHOLD
Address	000000001001310B (SCOM)
Attributes	Secure=true
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	Reserved field. (Access type is threshold_limit)
8:9	RW	THRESHOLD_RESET: 00 disable 01 reset after 1 HP 02 reset after 2 HP
10:25	RW	Reserved field. (Access type is min_period)
26:49	RW	Reserved field. (Access type is random_mask)

Register Name	<i>SCOM Mode Register To Support P7 Recovery Macro</i>
Mnemonic	EXP.EC.PC.PC_NE.FIR.FIR_MODEREG
Address	000000001001310C (SCOM)
Attributes	Secure=true
Description	



Bits	SCOM	Field Mnemonic: Description
0	RW	BREAKPOINT_DONE: breakpoint done set by SCOM sent to RECOVERY
1	RWX	BREAKPOINT_REQ: set by RECOVERY READ by SCOM
2	RW	SPARE_MODE_TO_VSU_LSU: spare mode enable set by SCOM sent to LSU
3	RW	SPARE_MUX_SELECT: spare MUX select set by SCOM sent to LSU
4	RW	RESET_RECOV_THOLD: reset thold register in recovery by SCOM

Register Name	<i>Threshold For Determining That Recovery Is Not Making Forward Progress</i>
Mnemonic	EXP.EC.PC.PC_NE.FIR.RCVY_THOLD_VAL
Address	000000001001310D (SCOM)
Attributes	
Description	

[illegible]

Register Name	<i>Thread Active Indications</i>
Mnemonic	EXP.EC.PC.PC_NE.FIR.THREAD_ACTIVE
Address	000000001001310E (SCOM)
Attributes	
Description	

[illegible]

Register Name	<i>Reset Keeper On Error Report Macros</i>
Mnemonic	EXP.EC.PC.PC_NE.FIR.RESET_KEEPER
Address	000000001001310F (SCOM)
Attributes	
Description	

[illegible]

Registers Specification

POWER8 Processor

Register Name	<i>PC_NE Error Report Hold_out Register8</i>
Mnemonic	EXP.EC.PC.PC_NE.PCNE_REG8_HOLD_OUT
Address	0000000010013110 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is fir_fir_err_inj_rec_ug_hold_out)
1	ROX	Reserved field. (Access type is fir_fir_err_inj_xstp_ug_hold_out)
2	ROX	Reserved field. (Access type is fir_phyp_err_inj_ug_hold_out)
3	ROX	Reserved field. (Access type is fir_isu_l2_ue_over_th_ug_hold_out)
4	ROX	Reserved field. (Access type is fir_ram_instr_reg_access_ug_hold_out)
5	ROX	Reserved field. (Access type is fir_ram_mode_user_ug_hold_out)
6	ROX	Reserved field. (Access type is fir_recov_err_during_ram_mode_ug_hold_out)
7	ROX	Reserved field. (Access type is fir_recov_err_during_smt_mode_change_ug_hold_out)
8	ROX	Reserved field. (Access type is vsu_wb_fp_residue_errorlat_free_hold_out)
9	ROX	Reserved field. (Access type is vsu_ex1_p0_ecc_errorlat_free_hold_out)
10	ROX	Reserved field. (Access type is vsu_ex1_p1_ecc_errorlat_free_hold_out)
11	ROX	Reserved field. (Access type is vsu_wb_ecc_ue_errorlat_free_hold_out)
12	ROX	Reserved field. (Access type is vsu_tl_scr_p_errorlat_free_hold_out)
13	ROX	Reserved field. (Access type is vsu_sw7_read_illegal_data_pickup_errorlat_free_hold_out)
14:19	RO	constant=0b000000
20	ROX	Reserved field. (Access type is vsu_p0_finish_conflict_errorlat_free_hold_out)
21	ROX	Reserved field. (Access type is vsu_p1_finish_conflict_errorlat_free_hold_out)
22	ROX	Reserved field. (Access type is vsu_rf1_p0_illegal_address_errorlat_free_hold_out)
23	ROX	Reserved field. (Access type is vsu_rf1_p1_illegal_address_errorlat_free_hold_out)
24	ROX	Reserved field. (Access type is vsu_load_swap_conflict_errorlat_free_hold_out)
25	ROX	Reserved field. (Access type is vsu_p0_illegal_instruction_errorlat_free_hold_out)
26	ROX	Reserved field. (Access type is vsu_p1_illegal_instruction_errorlat_free_hold_out)
27	ROX	Reserved field. (Access type is vsu_xfr_p0_illegal_rtag_errorlat_free_hold_out)
28	ROX	Reserved field. (Access type is vsu_xfr_p1_illegal_rtag_errorlat_free_hold_out)
29	ROX	Reserved field. (Access type is vsu_rf2_cy_ex_dd_dq_collision_errorlat_free_hold_out)
30:32	RO	constant=0b000
33	ROX	Reserved field. (Access type is recov_abist_hold_out)
34	ROX	Reserved field. (Access type is recov_ecc_refresh_state_hold_out)
35	ROX	Reserved field. (Access type is recov_fwd_prog_hold_out)
36	ROX	Reserved field. (Access type is recov_recov_disabled_cg_hold_out)
37	ROX	Reserved field. (Access type is recov_recovery_state_hold_out)
38	RW	Reserved field. (Access type is recov_thread_change_hold_out;)
39	ROX	Reserved field. (Access type is pmc_smt_change_timeout_hold_out)



Bits	SCOM	Field Mnemonic: Description
40	ROX	Reserved field. (Access type is pmc_quiesced_timeout_hold_out)
41	ROX	Reserved field. (Access type is pmc_core_wakeup_timeout_hold_out)
42	ROX	Reserved field. (Access type is pmc_core_inv_timeout_hold_out)
43	ROX	Reserved field. (Access type is pmc_sm_smtch_parity_hold_out)
44	ROX	Reserved field. (Access type is pmc_core_pm_sm_parity_hold_out)
45	ROX	Reserved field. (Access type is pmc_smtch_disable_hold_out)
46	ROX	Reserved field. (Access type is du_pc_cntl_err_hold_out)
47	ROX	Reserved field. (Access type is du_pc_expr_err_hold_out)
48	ROX	Reserved field. (Access type is du_pc_resi_err_hold_out)
49	ROX	Reserved field. (Access type is fir_tm_debug_ug_hold_out)
50	ROX	Reserved field. (Access type is fir_xstop_on_trigger_ug_hold_out)
51:52	ROX	Reserved field. (Access type is ne_scom_error_hold_out)
53	ROX	Reserved field. (Access type is fir_force_recov_ts_ug_hold_out)
54:63	RO	constant=0b0000000000

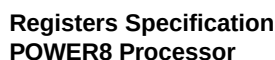
Register Name	<i>Debug Select For Ne,recov,pmc</i>
Mnemonic	EXP.EC.PC.PC_NE.PCNE_DEBUG_SELO
Address	0000000010013111 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:17	WO	Reserved field. (Access type is ne_debug_sel0)

Register Name	<i>Debug Select For Tctl0-3</i>
Mnemonic	EXP.EC.PC.PC_NE.PCNE_DEBUG_SEL1
Address	0000000010013112 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	WO	Reserved field. (Access type is ne_debug_sel1)

Register Name	<i>Debug Select For Tctl4-7</i>
Mnemonic	EXP.EC.PC.PC_NE.PCNE_DEBUG_SEL2
Address	0000000010013113 (SCOM)
Attributes	
Description	





Bits	SCOM	Field Mnemonic: Description
11:15	WO_1P	MODE_TIMEFAC_ERROR_INJ: error inject into timer
16	RW	MODE_SPRC0_SEL: bit 53 to 60 will be loaded into lpar0_sprc
17	RW	MODE_SPRC1_SEL: bit 53 to 60 will be loaded into lpar1_sprc
18	RW	MODE_SPRC2_SEL: bit 53 to 60 will be loaded into lpar2_sprc
19	RW	MODE_SPRC3_SEL: bit 53 to 60 will be loaded into lpar3_sprc
20	RW	MODE_SPRC_T0_SEL: bit 53 to 60 will be loaded into thread0_sprc
21	RW	MODE_SPRC_T1_SEL: bit 53 to 60 will be loaded into thread1_sprc
22	RW	MODE_SPRC_T2_SEL: bit 53 to 60 will be loaded into thread2_sprc
23	RW	MODE_SPRC_T3_SEL: bit 53 to 60 will be loaded into thread3_sprc
24	RW	MODE_SPRC_T4_SEL: bit 53 to 60 will be loaded into thread4_sprc
25	RW	MODE_SPRC_T5_SEL: bit 53 to 60 will be loaded into thread5_sprc
26	RW	MODE_SPRC_T6_SEL: bit 53 to 60 will be loaded into thread6_sprc
27	RW	MODE_SPRC_T7_SEL: bit 53 to 60 will be loaded into thread7_sprc
28:63	RO	constant=0b00000000000000000000000000000000

Register Name	<i>Control Register</i>
Mnemonic	EXP.EC.PC.PC_NW.SPRD.CTRL
Address	0000000010013282 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b00000000000000000000000000000000
48	ROX	CTRL_T0_RUN_Q: thread 0 run_latch
49	ROX	CTRL_T1_RUN_Q: thread 1 run_latch
50	ROX	CTRL_T2_RUN_Q: thread 2 run_latch
51	ROX	CTRL_T3_RUN_Q: thread 3 run_latch
52	ROX	CTRL_T4_RUN_Q: thread 4 run_latch
53	ROX	CTRL_T5_RUN_Q: thread 5 run_latch
54	ROX	CTRL_T6_RUN_Q: thread 6 run_latch
55	ROX	CTRL_T7_RUN_Q: thread 7 run_latch
56:62	RO	constant=0b00000000
63	NCX	Reserved field. (Access type is run_q)



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Register Name	<i>Scratch Register 0</i>	
Mnemonic	EXP.EC.PC.SCR0	
Address	0000000010013283 (SCOM)	
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0:63	RW	

Register Name	<i>Scratch Register 1</i>	
Mnemonic	EXP.EC.PC.SCR1	
Address	0000000010013284 (SCOM)	
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0:63	RW	

Register Name	<i>Scratch Register 2</i>	
Mnemonic	EXP.EC.PC.SCR2	
Address	0000000010013285 (SCOM)	
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0:63	RW	

Register Name	<i>Scratch Register 3</i>	
Mnemonic	EXP.EC.PC.SCR3	
Address	0000000010013286 (SCOM)	
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0:63	RW	



Register Name		<i>Scratch Register 4</i>
Mnemonic		EXP.EC.PC.SCR4
Address		0000000010013287 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:63	RW	

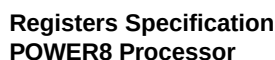
Register Name		<i>Scratch Register 5</i>
Mnemonic		EXP.EC.PC.SCR5
Address		0000000010013288 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:63	RW	

Register Name		<i>Scratch Register 6</i>
Mnemonic		EXP.EC.PC.SCR6
Address		0000000010013289 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:63	RW	

Register Name		<i>Scratch Register 7</i>
Mnemonic		EXP.EC.PC.SCR7
Address		000000001001328A (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:63	RW	

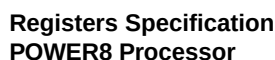
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[illegible]



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Bits	SCOM	Field Mnemonic: Description
27	RWX	DIS_LOWER_SMT_SWITCH: Disable Thread Switching
28	RWX	EN_SMT2_SHARED_MODE: When in SMT2 mode go into shared mode
29	RWX	SPARE_D: Spare
30	RWX	DIS_TRACE_SPR: Disable Trace SPR from sending In-Memory Trace control commands
31	RWX	EN_ATTN: Enable Support Processor attn instruction
32:63	RO	constant=0b00000000000000000000000000000000

Register Name	<i>Hypervisor Current State</i>
Mnemonic	EXP.EC.PC.PC_NW.SPRD.HV_STATE
Address	000000001001329D (SCOM)
Attributes	
Description	

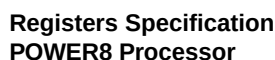
Bits	SCOM	Field Mnemonic: Description
0:47	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000
48:63	ROX	Reserved field. (Access type is hv_state)

Register Name	<i>SPURR AUTO-SCALE DETECT CYCLE COUNT SCOM</i>
Mnemonic	EXP.EC.PC.PC_NW.TFP.SPURR_FREQ_DETECT_CYC_CNT
Address	000000001001329E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	ROX	CYCLE_COUNT: cycle count used by auto frequency scale detector Represents the upper eight bits of a 13-bit cycle counter that counts the number of core clock cycles in the last interval of 16 TOD steps.
8:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>SPURR FREQUENCY SCALE SCOM</i>
Mnemonic	EXP.EC.PC.PC_NW.TFP.SPURR_FREQ_SCALE
Address	000000001001329F (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	SCALE_OVERRIDE_EN: frequency scale override enable (default=0b1) Reading this bit will return the value that was written.
1:7	RW	SCALE_FACTOR: frequency scale factor in 64ths (default=0b1000000) Reading these bits will return the value that was written.
8:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

[illegible]

Bits	SCOM	Field Mnemonic: Description
0:59	ROX	TIMEBASE: Timebase Register
60:63	RO	constant=0b0000

Bits	SCOM1	Field Mnemonic: Description
0:54	WOX	TIMEBASE: Timebase Register
55:59	N/A	not implemented
60:63	WOX	CHIP_TOD_STATUS: Chip Time of Day Status

Register Name	<i>TOD Time Of Day (mttod) Register For Sync_bit_sel=001</i>
Mnemonic	EXP.EC.PC.PC_NW.TFC.TOD_SYNC001
Address	00000000100132A1 (SCOM1)
Attributes	
Description	Note: The TOD_SYNCxxx Registers Cannot Be Tested Together By Regchk In One Run.



Bits	SCOM1	Field Mnemonic: Description
0:53	WOX	TIMEBASE: Timebase Register
54:59	N/A	not implemented
60:63	WOX	CHIP_TOD_STATUS: Chip Time of Day Status

Register Name	<i>TOD Time Of Day (mttod) For Sync_bit_sel=010</i>
Mnemonic	EXP.EC.PC.PC_NW.TFC.TOD_SYNC010
Address	00000000100132A1 (SCOM1)
Attributes	
Description	Note: The TOD_SYNCxxx Registers Cannot Be Tested Together By Regchk In One Run.

Bits	SCOM1	Field Mnemonic: Description
0:52	WOX	TIMEBASE: Timebase Register
53:59	N/A	not implemented
60:63	WOX	CHIP_TOD_STATUS: Chip Time of Day Status

Register Name	<i>TOD Time Of Day (mttod) For Sync_bit_sel=011</i>
Mnemonic	EXP.EC.PC.PC_NW.TFC.TOD_SYNC011
Address	00000000100132A1 (SCOM1)
Attributes	
Description	Note: The TOD_SYNCxxx Registers Cannot Be Tested Together By Regchk In One Run.

Bits	SCOM1	Field Mnemonic: Description
0:51	WOX	TIMEBASE: Timebase Register
52:59	N/A	not implemented
60:63	WOX	CHIP_TOD_STATUS: Chip Time of Day Status

Register Name	<i>TOD Time Of Day (mttod) For Sync_bit_sel=100</i>
Mnemonic	EXP.EC.PC.PC_NW.TFC.TOD_SYNC100
Address	00000000100132A1 (SCOM1)
Attributes	
Description	Note: The TOD_SYNCxxx Registers Cannot Be Tested Together By Regchk In One Run.

Bits	SCOM1	Field Mnemonic: Description
0:50	WOX	TIMEBASE: Timebase Register
51:59	N/A	not implemented
60:63	WOX	CHIP_TOD_STATUS: Chip Time of Day Status

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Register Name	<i>TOD Time Of Day (mttod) For Sync_bit_sel=101</i>
Mnemonic	EXP.EC.PC.PC_NW.TFC.TOD_SYNC101
Address	00000000100132A1 (SCOM1)
Attributes	
Description	Note: The TOD_SYNCxxx Registers Cannot Be Tested Together By Regchk In One Run.

Bits	SCOM1	Field Mnemonic: Description
0:49	WOX	TIMEBASE: Timebase Register
50:59	N/A	not implemented
60:63	WOX	CHIP_TOD_STATUS: Chip Time of Day Status

Register Name	<i>TOD Time Of Day (mttod) For Sync_bit_sel=110</i>
Mnemonic	EXP.EC.PC.PC_NW.TFC.TOD_SYNC110
Address	00000000100132A1 (SCOM1)
Attributes	
Description	Note: The TOD_SYNCxxx Registers Cannot Be Tested Together By Regchk In One Run.

Bits	SCOM1	Field Mnemonic: Description
0:48	WOX	TIMEBASE: Timebase Register
49:59	N/A	not implemented
60:63	WOX	CHIP_TOD_STATUS: Chip Time of Day Status

Register Name	<i>TOD Time Of Day (mttod) For Sync_bit_sel=111</i>
Mnemonic	EXP.EC.PC.PC_NW.TFC.TOD_SYNC111
Address	00000000100132A1 (SCOM1)
Attributes	
Description	Note: The TOD_SYNCxxx Registers Cannot Be Tested Together By Regchk In One Run.

Bits	SCOM1	Field Mnemonic: Description
0:47	WOX	TIMEBASE: Timebase Register
48:59	N/A	not implemented
60:63	WOX	CHIP_TOD_STATUS: Chip Time of Day Status

Register Name	<i>POWER MANAGEMENT EVENT SELECTS</i>
Mnemonic	EXP.EC.PC.PC_NW.TFP.PWM_EVENTS
Address	00000000100132A2 (SCOM)
Attributes	
Description	



Bits	SCOM	Field Mnemonic: Description
0:31	RO	constant=0b00000000000000000000000000000000
32	RW	PWM_EVENTS_RESERVED_32: Reserved
33:39	RW	FREQ_SCALE_A_THRESHOLD: Frequency scale lower threshold A (default = 0b1000000)
40	RW	PWM_EVENTS_RESERVED_40: Reserved
41:47	RW	FREQ_SCALE_B_THRESHOLD: Frequency scale upper threshold B (default = 0b1000000)
48	RW	PWM_EVENTS_RESERVED_48: Reserved
49:51	RW	PSTATE_A_THRESHOLD: P-state lower threshold A
52	RW	PWM_EVENTS_RESERVED_52: Reserved
53:55	RW	PSTATE_B_THRESHOLD: P-state upper threshold B
56	RW	PWM_EVENTS_RESERVED_56: Reserved
57	RW	PWM_EVENTS_RESERVED_57: Reserved
58:59	RW	EVENT_MUX_SELECTS: Event mux select 00: Frequency threshold compares A and B (against scale used by SPURR before PMCR fraction) 01: P-state threshold compares A and B (against value in PMCR) 10: PMCM threshold compare (from PMCR) Max Psav Mode (from PMCR) 11: PMCM threshold compare (from PMCR) PMCM compare (actual)
60	RW	PWM_EVENTS_RESERVED_60: Reserved
61	RW	PWM_EVENTS_RESERVED_61: Reserved
62:63	RW	PMCM_THRESHOLD: PMCM threshold

Register Name	<i>Processor Core Performance Throttling Mode Register</i>
Mnemonic	EXP.EC.PC.PC_NW.PROCESSOR_CORE_PFTH_MODEREG
Address	00000000100132A7 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX	PFTH_CNTR_DIS: Disable PM Instrumentation Counters.
1	RWX	PFTH_CHARAC_MODE: Enable Characterization mode.
2	RWX	PFTH_CNTR_RUN_LATCH_GATE_DIS: Ignore Run Latch for PM Instrumentation Counters.
3:10	ROX	SPRD_PFTH_TX_RUN_LATCHES: Run latches for Threads 0 to 3
11:18	ROX	TX_THREADS_STOPPED: Hold or IPC Instruction count values
19:63	RO	constant=0b00000000000000000000000000000000

Register Name	<i>PC_NW Error Report Hold_out Register0</i>
Mnemonic	EXP.EC.PC.PC_NW.PCNW_REG0_HOLD_OUT
Address	00000000100132A9 (SCOM)
Attributes	
Description	

Registers Specification

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Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is tfd_sprd_hdec_residue_nopsav_hold_out)
1:2	ROX	Reserved field. (Access type is tfc_sprd_control_tb41_hold_out)
3:9	ROX	Reserved field. (Access type is tfc_sprd_firmware_control_tb41_hold_out)
10:20	ROX	Reserved field. (Access type is tfc_sprd_parity_tb41_hold_out)
21:25	ROX	Reserved field. (Access type is tfp_sprd_parity_nopsav_hold_out)
26:29	ROX	Reserved field. (Access type is tfp_sprd_spurr_scale_limit_scale_hold_out)
30:45	ROX	Reserved field. (Access type is tfr_sprd_parity_nopsav_hold_out)
46:53	ROX	Reserved field. (Access type is tfr_sprd_tx_pur_overflow_oflow_hold_out)
54:61	ROX	Reserved field. (Access type is tfr_sprd_tx_spur_overflow_oflow_hold_out)
62:63	ROX	Reserved field. (Access type is tfd_sprd_dec_residue_nopsav_hold_out)

Register Name	<i>PC_NW Error Report Hold_out Register1</i>
Mnemonic	EXP.EC.PC.PC_NW.PCNW_REG1_HOLD_OUT
Address	00000000100132AA (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:5	ROX	Reserved field. (Access type is tfd_sprd_dec_residue_nopsav_hold_out)
6	ROX	Reserved field. (Access type is sprd_ctrl_par_hold_out)
7	ROX	Reserved field. (Access type is sprd_fir_checkstop_inj_q_hold_out)
8	ROX	Reserved field. (Access type is sprd_hid0_par_hold_out)
9	ROX	Reserved field. (Access type is sprd_hmeer_par_hold_out)
10	ROX	Reserved field. (Access type is sprd_mode_par_hold_out)
11	ROX	Reserved field. (Access type is sprd_pcr_lpar0_par_hold_out)
12	ROX	Reserved field. (Access type is sprd_pcr_lpar1_par_hold_out)
13	ROX	Reserved field. (Access type is sprd_pcr_lpar2_par_hold_out)
14	ROX	Reserved field. (Access type is sprd_pcr_lpar3_par_hold_out)
15	ROX	Reserved field. (Access type is sprd_spr_nw_scom_hold_out)
16:23	ROX	Reserved field. (Access type is tfp_sprd_pur_accum_oflow_hold_out)
24	ROX	Reserved field. (Access type is sprd_trace0_scom_hold_out)
25	ROX	Reserved field. (Access type is sprd_trace1_scom_hold_out)
26	ROX	Reserved field. (Access type is sprd_trace2_scom_hold_out)
27	ROX	Reserved field. (Access type is sprd_trace3_scom_hold_out)



Register Name	<i>RW-Accessible Via SCOM</i>
Mnemonic	EXP.EC.PC.PC_NW.SPRD.SCOM_SPRC_OCC
Address	00000000100132AB (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:53	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000
54:60	RW	Reserved field. (Access type is SCOM_SPRC_OCC_address)
61:63	RO	constant=0b000

Register Name	Performance Throttling Mode Register
Mnemonic	EXP.EC.PC.PC_NW.SPRD.PFTH_THROT_REG
Address	00000000100132AD (SCOM)
Attributes	
Description	

[illegible]

Register Name	<i>Debug Mux Selects</i>
Mnemonic	EXP.EC.PC.PC_NW.SPRD.PCNW_DBGBUS_SEL
Address	00000000100132AE (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:1	WOX	Reserved field. (Access type is dbgbus_TA0_unit_sel_00_43)



Register Name	<i>SCOM-writeable PMU CONTROL REGISTER</i>
Mnemonic	EXP.EC.PC.PC_S.PMUT0.PMU_SCOM
Address	00000000100132C1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:8	RW	Reserved field. (Access type is idle_delay)
9:17	RW	Reserved field. (Access type is completion_delay)
18	RW	Reserved field. (Access type is sample_override)
19:23	RW	Reserved field. (Access type is spare_ctrl)

Register Name	<i>SCOM-writeable PMU CONTROL REGISTER</i>
Mnemonic	EXP.EC.PC.PC_S.PMUT1.PMU_SCOM
Address	00000000100132C2 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:8	RW	Reserved field. (Access type is idle_delay)
9:17	RW	Reserved field. (Access type is completion_delay)
18	RW	Reserved field. (Access type is sample_override)
19:23	RW	Reserved field. (Access type is spare_ctrl)

Register Name	<i>SCOM-writeable PMU CONTROL REGISTER</i>
Mnemonic	EXP.EC.PC.PC_S.PMUT2.PMU_SCOM
Address	00000000100132C3 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:8	RW	Reserved field. (Access type is idle_delay)
9:17	RW	Reserved field. (Access type is completion_delay)
18	RW	Reserved field. (Access type is sample_override)
19:23	RW	Reserved field. (Access type is spare_ctrl)

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Register Name	SCOM-writeable PMU CONTROL REGISTER
Mnemonic	EXP.EC.PC.PC_S.PMUT3.PMU_SCOM
Address	00000000100132C4 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:8	RW	Reserved field. (Access type is idle_delay)
9:17	RW	Reserved field. (Access type is completion_delay)
18	RW	Reserved field. (Access type is sample_override)
19:23	RW	Reserved field. (Access type is spare_ctrl)

Register Name	SCOM-writeable PMU CONTROL REGISTER
Mnemonic	EXP.EC.PC.PC_S.PMUT4.PMU_SCOM
Address	00000000100132C5 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:8	RW	Reserved field. (Access type is idle_delay)
9:17	RW	Reserved field. (Access type is completion_delay)
18	RW	Reserved field. (Access type is sample_override)
19:23	RW	Reserved field. (Access type is spare_ctrl)

Register Name	SCOM-writeable PMU CONTROL REGISTER
Mnemonic	EXP.EC.PC.PC_S.PMUT5.PMU_SCOM
Address	00000000100132C6 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:8	RW	Reserved field. (Access type is idle_delay)
9:17	RW	Reserved field. (Access type is completion_delay)
18	RW	Reserved field. (Access type is sample_override)
19:23	RW	Reserved field. (Access type is spare_ctrl)



Register Name	<i>SCOM-writeable PMU CONTROL REGISTER</i>
Mnemonic	EXP.EC.PC.PC_S.PMUT6.PMU_SCOM
Address	00000000100132C7 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:8	RW	Reserved field. (Access type is idle_delay)
9:17	RW	Reserved field. (Access type is completion_delay)
18	RW	Reserved field. (Access type is sample_override)
19:23	RW	Reserved field. (Access type is spare_ctrl)

Register Name	<i>SCOM-writeable PMU CONTROL REGISTER</i>
Mnemonic	EXP.EC.PC.PC_S.PMUT7.PMU_SCOM
Address	00000000100132C8 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:8	RW	Reserved field. (Access type is idle_delay)
9:17	RW	Reserved field. (Access type is completion_delay)
18	RW	Reserved field. (Access type is sample_override)
19:23	RW	Reserved field. (Access type is spare_ctrl)

Register Name	<i>Sier Mask SCOM Register</i>
Mnemonic	EXP.EC.PC.PC_S.PMUC.SIER_MASK
Address	00000000100132C9 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	RW	Reserved field. (Access type is sier_mask_tbd)

Register Name	<i>SRC Mask SCOM Register</i>
Mnemonic	EXP.EC.PC.PC_S.PMUC.SRC_MASK
Address	00000000100132CA (SCOM)
Attributes	
Description	

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Bits	SCOM	Field Mnemonic: Description
0:63	RW	Reserved field. (Access type is src_mask_tbd)

Register Name	<i>PC_S Error Report Hold_out Register0</i>
Mnemonic	EXP.EC.PC.PC_S.PCS_REG0_HOLD_OUT
Address	00000000100132CB (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:3	ROX	Reserved field. (Access type is itrace_step_check_hold_out)
4	ROX	Reserved field. (Access type is spr_s_scom_hold_out)
5	ROX	Reserved field. (Access type is trace4_scom_hold_out)
6	ROX	Reserved field. (Access type is trace5_scom_hold_out)
7:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>Rmsc Page Size</i>
Mnemonic	EXP.EC.PC.PC_S.SPR_S.RMSC_PAGE_SIZE
Address	00000000100132CC (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:62	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000
63	WOX	Reserved field. (Access type is rmsc_page_size)

Register Name	<i>Hbi Invalidate Erat</i>
Mnemonic	EXP.EC.PC.PC_S.SPR_S.HBI_INVALIDATE_ERAT
Address	00000000100132CD (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:62	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000
63	WOX_1P	Reserved field. (Access type is invalidate_erat)



Register Name	Core Fuses
Mnemonic	EXP.EC.PC.PC_S.SPR_S.CORE_FUSES
Address	00000000100132CE (SCOM)
Attributes	
Description	

[illegible]

Register Name	IMA Mask Register
Mnemonic	EXP.EC.PC.PC_S.IMA_EVENT_MASK
Address	00000000100132CF (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX	Reserved field. (Access type is ECONL_0)
1	RWX	Reserved field. (Access type is ECRL_0)
2	RWX	Reserved field. (Access type is ECH_0)
3	RWX	Reserved field. (Access type is ECP_0)
4	RWX	Reserved field. (Access type is ECS_0)
5	RWX	Reserved field. (Access type is ECA_0)
6	RWX	Reserved field. (Access type is ECTA0_0)
7	RWX	Reserved field. (Access type is ECTA1_0)
8	RWX	Reserved field. (Access type is ECUS0_0)
9	RWX	Reserved field. (Access type is ECUS1_0)
10	RWX	Reserved field. (Access type is ECONL_1)
11	RWX	Reserved field. (Access type is ECRL_1)
12	RWX	Reserved field. (Access type is ECH_1)
13	RWX	Reserved field. (Access type is ECP_1)
14	RWX	Reserved field. (Access type is ECS_1)
15	RWX	Reserved field. (Access type is ECA_1)
16	RWX	Reserved field. (Access type is ECTA0_1)
17	RWX	Reserved field. (Access type is ECTA1_1)
18	RWX	Reserved field. (Access type is ECUS0_1)
19	RWX	Reserved field. (Access type is ECUS1_1)

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Bits	SCOM	Field Mnemonic: Description
20	RWX	Reserved field. (Access type is ECONL_2)
21	RWX	Reserved field. (Access type is ECRL_2)
22	RWX	Reserved field. (Access type is ECH_2)
23	RWX	Reserved field. (Access type is ECP_2)
24	RWX	Reserved field. (Access type is ECS_2)
25	RWX	Reserved field. (Access type is ECA_2)
26	RWX	Reserved field. (Access type is ECTA0_2)
27	RWX	Reserved field. (Access type is ECTA1_2)
28	RWX	Reserved field. (Access type is ECUS0_2)
29	RWX	Reserved field. (Access type is ECUS1_2)
30:32	RWX	Reserved field. (Access type is IC_Tap)
33	RWX	Reserved field. (Access type is Dis_collection_wrap)
34:63	RO	constant=0b00000000000000000000000000000000

Register Name	SCOMC For PMU Indirect SCOM Access
Mnemonic	EXP.EC.PC.PC_S.SPR_S.PMU_SCOMC_REG
Address	00000000100132D0 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX	Reserved field. (Access type is pmc1)
1	RWX	Reserved field. (Access type is pmc2)
2	RWX	Reserved field. (Access type is pmc3)
3	RWX	Reserved field. (Access type is pmc4)
4	RWX	Reserved field. (Access type is pmc5)
5	RWX	Reserved field. (Access type is pmc6)
6	RWX	Reserved field. (Access type is mmcr0)
7	RWX	Reserved field. (Access type is mmcrh)
8	RWX	Reserved field. (Access type is mmcr0)
9	RWX	Reserved field. (Access type is mmcr1)
10	RWX	Reserved field. (Access type is mmcr2)
11	RWX	Reserved field. (Access type is mmcr3)
12	RWX	Reserved field. (Access type is mmcrs)
13	RWX	Reserved field. (Access type is sier)
14:16	RWX	Reserved field. (Access type is thread_id)
17:63	RO	constant=0b00000000000000000000000000000000



Register Name	SCOMC For PMU Indirect SCOM Access
Mnemonic	EXP.EC.PC.PC_S.SPR_S.PCS_DBGBUS_SEL
Address	00000000100132D2 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:2	WOX	DBGBUS_TA4_UNIT_SEL_00_43: unit mux selects for dbg1:debug_bus_00_43 to Trace Array 4 Values: IFU_DBGBUS0_00_43=>0b000 IFU_DBGBUS1_00_43=>0b001 IFU_DBGBUS2_00_43=>0b010 IFU_DBGBUS3_00_43=>0b011 LSU_DBGBUS0_00_43=>0b100 LSU_DBGBUS1_00_43=>0b101 LSU_DBGBUS2_00_43=>0b110 LSU_DBGBUS3_00_43=>0b111
3:5	WOX	DBGBUS_TA4_UNIT_SEL_44_87: unit mux selects for dbg1:debug_bus_44_87 to Trace Array 4 Values: IFU_DBGBUS0_44_87=>0b000 IFU_DBGBUS1_44_87=>0b001 IFU_DBGBUS2_44_87=>0b010 IFU_DBGBUS3_44_87=>0b011 LSU_DBGBUS0_44_87=>0b100 LSU_DBGBUS1_44_87=>0b101 LSU_DBGBUS2_44_87=>0b110 LSU_DBGBUS3_44_87=>0b111
6:8	WOX	DBGBUS_TA5_UNIT_SEL_00_43: unit mux selects for dbg1:debug_bus_00_43 to Trace Array 5 Values: IFU_DBGBUS0_00_43=>0b000 IFU_DBGBUS1_00_43=>0b001 IFU_DBGBUS2_00_43=>0b010 IFU_DBGBUS3_00_43=>0b011 LSU_DBGBUS0_00_43=>0b100 LSU_DBGBUS1_00_43=>0b101 LSU_DBGBUS2_00_43=>0b110 LSU_DBGBUS3_00_43=>0b111
9:11	WOX	DBGBUS_TA5_UNIT_SEL_44_87: unit mux selects for dbg1:debug_bus_44_87 to Trace Array 5 Values: IFU_DBGBUS0_44_87=>0b000 IFU_DBGBUS1_44_87=>0b001 IFU_DBGBUS2_44_87=>0b010 IFU_DBGBUS3_44_87=>0b011 LSU_DBGBUS0_44_87=>0b100 LSU_DBGBUS1_44_87=>0b101 LSU_DBGBUS2_44_87=>0b110 LSU_DBGBUS3_44_87=>0b111
12	WOX	DBGBUS_L2TA1_ENABLE: enable debug bus to l2 trace 1

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Bits	SCOM	Field Mnemonic: Description
13:15	WOX	DBGBUS_L2TA1_UNIT_SEL_00_43: unit mux selects for dbgm1:debug_bus_00_43 to L2 Trace Array 1 Values: IFU_DBGBUS0_00_43=>0b000 IFU_DBGBUS1_00_43=>0b001 IFU_DBGBUS2_00_43=>0b010 IFU_DBGBUS3_00_43=>0b011 LSU_DBGBUS0_00_43=>0b100 LSU_DBGBUS1_00_43=>0b101 LSU_DBGBUS2_00_43=>0b110 LSU_DBGBUS3_00_43=>0b111
16:18	WOX	DBGBUS_L2TA1_UNIT_SEL_44_87: unit mux selects for dbgm1:debug_bus_44_87 to L2 Trace Array 1 Values: IFU_DBGBUS0_44_87=>0b000 IFU_DBGBUS1_44_87=>0b001 IFU_DBGBUS2_44_87=>0b010 IFU_DBGBUS3_44_87=>0b011 LSU_DBGBUS0_44_87=>0b100 LSU_DBGBUS1_44_87=>0b101 LSU_DBGBUS2_44_87=>0b110 LSU_DBGBUS3_44_87=>0b111
19	WOX	DBGBUS_L2TA2_ENABLE: enable debug bus to l2 trace 1
20:22	WOX	DBGBUS_L2TA2_UNIT_SEL_00_43: unit mux selects for dbgm1:debug_bus_00_43 to L2 Trace Array 2 Values: IFU_DBGBUS0_00_43=>0b000 IFU_DBGBUS1_00_43=>0b001 IFU_DBGBUS2_00_43=>0b010 IFU_DBGBUS3_00_43=>0b011 LSU_DBGBUS0_00_43=>0b100 LSU_DBGBUS1_00_43=>0b101 LSU_DBGBUS2_00_43=>0b110 LSU_DBGBUS3_00_43=>0b111
23:25	WOX	DBGBUS_L2TA2_UNIT_SEL_44_87: unit mux selects for dbgm1:debug_bus_44_87 to L2 Trace Array 2 Values: IFU_DBGBUS0_44_87=>0b000 IFU_DBGBUS1_44_87=>0b001 IFU_DBGBUS2_44_87=>0b010 IFU_DBGBUS3_44_87=>0b011 LSU_DBGBUS0_44_87=>0b100 LSU_DBGBUS1_44_87=>0b101 LSU_DBGBUS2_44_87=>0b110 LSU_DBGBUS3_44_87=>0b111
26:63	N/A	not implemented Values: IFU_DBGBUS0_44_87=>0b000 IFU_DBGBUS1_44_87=>0b001 IFU_DBGBUS2_44_87=>0b010 IFU_DBGBUS3_44_87=>0b011 LSU_DBGBUS0_44_87=>0b100 LSU_DBGBUS1_44_87=>0b101 LSU_DBGBUS2_44_87=>0b110 LSU_DBGBUS3_44_87=>0b111



Register Name	<i>TOD_STEP_CHECK Register</i>	
Mnemonic	EXP.EC.PC.PC_S.ITRACE.TOD_STEP_CHECK	
Address	00000000100132D3 (SCOM)	
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0:14	RW	
15:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>SCOMC For PMU Indirect SCOM Access</i>	
Mnemonic	EXP.EC.PC.PC_S.SPR_S.PMU_INDIRECT_SCOMC_EN_REG	
Address	00000000100132D4 (SCOM)	
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0	RWX	Reserved field. (Access type is enable_indirect_pmu_scom)
1:63	RO	constant=0b0000000000000000000000000000000000000000000000000000000000000000

Register Name	<i>PC_S Error Report Hold_out Register1</i>	
Mnemonic	EXP.EC.PC.PC_S.PCS_REG1_HOLD_OUT	
Address	00000000100132D5 (SCOM)	
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is pmut0_mult_mrk_evaluate_status_hold_out)
1	ROX	Reserved field. (Access type is pmut0_multiple_marked_instr_ris_hold_out)
2	ROX	Reserved field. (Access type is pmut0_multiple_marked_instr_resbru_hold_out)
3	ROX	Reserved field. (Access type is pmut0_multiple_marked_instr_reslsu_hold_out)
4	ROX	Reserved field. (Access type is pmut1_mult_mrk_evaluate_status_hold_out)
5	ROX	Reserved field. (Access type is pmut1_multiple_marked_instr_ris_hold_out)
6	ROX	Reserved field. (Access type is pmut1_multiple_marked_instr_resbru_hold_out)
7	ROX	Reserved field. (Access type is pmut1_multiple_marked_instr_reslsu_hold_out)
8	ROX	Reserved field. (Access type is pmut2_mult_mrk_evaluate_status_hold_out)
9	ROX	Reserved field. (Access type is pmut2_multiple_marked_instr_ris_hold_out)
10	ROX	Reserved field. (Access type is pmut2_multiple_marked_instr_resbru_hold_out)
11	ROX	Reserved field. (Access type is pmut2_multiple_marked_instr_reslsu_hold_out)
12	ROX	Reserved field. (Access type is pmut3_mult_mrk_evaluate_status_hold_out)

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Bits	SCOM	Field Mnemonic: Description
13	ROX	Reserved field. (Access type is pmut3_multiple_marked_instr_ris_hold_out)
14	ROX	Reserved field. (Access type is pmut3_multiple_marked_instr_resbru_hold_out)
15	ROX	Reserved field. (Access type is pmut3_multiple_marked_instr_reslsu_hold_out)
16	ROX	Reserved field. (Access type is pmut4_mult_mrk_evaluate_status_hold_out)
17	ROX	Reserved field. (Access type is pmut4_multiple_marked_instr_ris_hold_out)
18	ROX	Reserved field. (Access type is pmut4_multiple_marked_instr_resbru_hold_out)
19	ROX	Reserved field. (Access type is pmut4_multiple_marked_instr_reslsu_hold_out)
20	ROX	Reserved field. (Access type is pmut5_mult_mrk_evaluate_status_hold_out)
21	ROX	Reserved field. (Access type is pmut5_multiple_marked_instr_ris_hold_out)
22	ROX	Reserved field. (Access type is pmut5_multiple_marked_instr_resbru_hold_out)
23	ROX	Reserved field. (Access type is pmut5_multiple_marked_instr_reslsu_hold_out)
24	ROX	Reserved field. (Access type is pmut6_mult_mrk_evaluate_status_hold_out)
25	ROX	Reserved field. (Access type is pmut6_multiple_marked_instr_ris_hold_out)
26	ROX	Reserved field. (Access type is pmut6_multiple_marked_instr_resbru_hold_out)
27	ROX	Reserved field. (Access type is pmut6_multiple_marked_instr_reslsu_hold_out)
28	ROX	Reserved field. (Access type is pmut7_mult_mrk_evaluate_status_hold_out)
29	ROX	Reserved field. (Access type is pmut7_multiple_marked_instr_ris_hold_out)
30	ROX	Reserved field. (Access type is pmut7_multiple_marked_instr_resbru_hold_out)
31	ROX	Reserved field. (Access type is pmut7_multiple_marked_instr_reslsu_hold_out)
32:63	RO	constant=0b00000000000000000000000000000000

Register Name	<i>Fxu Error Report Hold_out Register0</i>
Mnemonic	EXP.EC.FX.FXU_REG0_HOLD_OUT
Address	0000000010013300 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is FX0_ERPT_GPR_ECC_HOLD_OUT)
1	ROX	Reserved field. (Access type is FX1_ERPT_GPR_ECC_HOLD_OUT)
2:5	ROX	Reserved field. (Access type is GROUP1_CKP_ERRORS_HOLD_OUT)
6:11	ROX	Reserved field. (Access type is GROUP2_CKP_ERRORS_HOLD_OUT)
12:14	ROX	Reserved field. (Access type is GROUP3_CKP_ERRORS_HOLD_OUT)
15	ROX	Reserved field. (Access type is GROUP4_0_CKP_ERRORS_HOLD_OUT)



Register Name	<i>Fxu Error Report Hold_out Register1</i>
Mnemonic	EXP.EC.FX.FXU_REG1_HOLD_OUT
Address	0000000010013301 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:8	ROX	Reserved field. (Access type is GROUP4_1_CKP_ERRORS_HOLD_OUT)
9:10	ROX	Reserved field. (Access type is GROUP5_CKP_ERRORS_HOLD_OUT)
11:12	ROX	Reserved field. (Access type is GROUP6_CKP_ERRORS_HOLD_OUT)
13:15	ROX	Reserved field. (Access type is GROUP1_0_REC_ERRORS_HOLD_OUT)

Register Name	<i>Fxu Error Report Hold_out Register2</i>
Mnemonic	EXP.EC.FX.FXU_REG2_HOLD_OUT
Address	0000000010013302 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:2	ROX	Reserved field. (Access type is GROUP1_1_REC_ERRORS_HOLD_OUT)
3:8	ROX	Reserved field. (Access type is GROUP2_REC_ERRORS_HOLD_OUT)
9:13	ROX	Reserved field. (Access type is GROUP3_REC_ERRORS_HOLD_OUT)
14:15	ROX	Reserved field. (Access type is GROUP4_0_REC_ERRORS_HOLD_OUT)

Register Name	<i>Fxu Error Report Hold_out Register3</i>
Mnemonic	EXP.EC.FX.FXU_REG3_HOLD_OUT
Address	0000000010013303 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:8	ROX	Reserved field. (Access type is GROUP4_1_REC_ERRORS_HOLD_OUT)
9:15	ROX	Reserved field. (Access type is GROUP5_0_REC_ERRORS_HOLD_OUT)

Register Name	<i>Fxu Error Report Hold_out Register4</i>
Mnemonic	EXP.EC.FX.FXU_REG4_HOLD_OUT
Address	0000000010013304 (SCOM)
Attributes	
Description	

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Bits	SCOM	Field Mnemonic: Description
0:1	ROX	Reserved field. (Access type is GROUP5_1_REC_ERRORS_HOLD_OUT)
2:4	ROX	Reserved field. (Access type is GROUP6_REC_ERRORS_HOLD_OUT)
5	ROX	Reserved field. (Access type is GROUP7_REC_ERRORS_HOLD_OUT)
6:10	ROX	Reserved field. (Access type is GROUP8_REC_ERRORS_HOLD_OUT)
11:15	RO	constant=0b00000

Register Name	<i>ISU Error Report Hold_out Register 0</i>
Mnemonic	EXP.EC.SD.ISU_REG0_HOLD_OUT
Address	0000000010013340 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is SDCX_SDCO_T0_HEIR_CHKSTOP_hold_out)
1	ROX	Reserved field. (Access type is SDCX_SDCO_T0_HSRR1_CHKSTOP_hold_out)
2	ROX	Reserved field. (Access type is SDCX_SDCO_T0_MSR_CHKSTOP_hold_out)
3	ROX	Reserved field. (Access type is SDCX_SDCO_T0_SRR1_CHKSTOP_hold_out)
4	ROX	Reserved field. (Access type is SDCX_SDCO_T0_VRSAVE_BKUP_CHKSTOP_hold_out)
5	ROX	Reserved field. (Access type is SDCX_SDCO_T0_VRSAVE_CHKSTOP_hold_out)
6	ROX	Reserved field. (Access type is SDCX_SDCO_T0_FSCR_CHKSTOP_hold_out)
7	ROX	Reserved field. (Access type is SDCX_SDCO_T0_HFSCR_CHKSTOP_hold_out)
8	ROX	Reserved field. (Access type is SDCX_SDCO_T0_TEXASR_CHKSTOP_hold_out)
9	ROX	Reserved field. (Access type is SDCX_SDCO_T0_BESCR_CHKSTOP_hold_out)
10:11	RO	constant=0b00
12	ROX	Reserved field. (Access type is SDCX_SDCU_T0_MCHK_AND_ME_EQ_0_hold_out)
13	RO	constant=0b0
14	ROX	Reserved field. (Access type is SDCR_ERR_INJ_HOLD_OUT)
15	ROX	Reserved field. (Access type is SDCR_ERR_INJ_RECOV_HOLD_OUT)

Register Name	<i>ISU Error Report Hold_out Register 1</i>
Mnemonic	EXP.EC.SD.ISU_REG1_HOLD_OUT
Address	0000000010013341 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is SDCX_SDCO_T1_HEIR_CHKSTOP_hold_out)
1	ROX	Reserved field. (Access type is SDCX_SDCO_T1_HSRR1_CHKSTOP_hold_out)
2	ROX	Reserved field. (Access type is SDCX_SDCO_T1_MSR_CHKSTOP_hold_out)



Bits	SCOM	Field Mnemonic: Description
3	ROX	Reserved field. (Access type is SDCX_SDCO_T1_SRR1_CHKSTOP_hold_out)
4	ROX	Reserved field. (Access type is SDCX_SDCO_T1_VRSAVE_BKUP_CHKSTOP_hold_out)
5	ROX	Reserved field. (Access type is SDCX_SDCO_T1_VRSAVE_CHKSTOP_hold_out)
6	ROX	Reserved field. (Access type is SDCX_SDCO_T1_FSCR_CHKSTOP_hold_out)
7	ROX	Reserved field. (Access type is SDCX_SDCO_T1_HFSCR_CHKSTOP_hold_out)
8	ROX	Reserved field. (Access type is SDCX_SDCO_T1_TEXASR_CHKSTOP_hold_out)
9	ROX	Reserved field. (Access type is SDCX_SDCO_T1_BESCR_CHKSTOP_hold_out)
10:11	RO	constant=0b00
12	ROX	Reserved field. (Access type is SDCX_SDCU_T1_MCHK_AND_ME_EQ_0_hold_out)
13	ROX	Reserved field. (Access type is SDCC_T0_HEAD_TAIL_XSTOP_HOLD_OUT)
14	ROX	Reserved field. (Access type is SDCC_T1_HEAD_TAIL_XSTOP_HOLD_OUT)
15	ROX	Reserved field. (Access type is SDCC_T2_HEAD_TAIL_XSTOP_HOLD_OUT)

Register Name	<i>ISU Error Report Hold_out Register 2</i>
Mnemonic	EXP.EC.SD.ISU_REG2_HOLD_OUT
Address	0000000010013342 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is SDCX_SDCO_T2_HEIR_CHKSTOP_hold_out)
1	ROX	Reserved field. (Access type is SDCX_SDCO_T2_HSRR1_CHKSTOP_hold_out)
2	ROX	Reserved field. (Access type is SDCX_SDCO_T2_MSR_CHKSTOP_hold_out)
3	ROX	Reserved field. (Access type is SDCX_SDCO_T2_SRR1_CHKSTOP_hold_out)
4	ROX	Reserved field. (Access type is SDCX_SDCO_T2_VRSAVE_BKUP_CHKSTOP_hold_out)
5	ROX	Reserved field. (Access type is SDCX_SDCO_T2_VRSAVE_CHKSTOP_hold_out)
6	ROX	Reserved field. (Access type is SDCX_SDCO_T2_FSCR_CHKSTOP_hold_out)
7	ROX	Reserved field. (Access type is SDCX_SDCO_T2_HFSCR_CHKSTOP_hold_out)
8	ROX	Reserved field. (Access type is SDCX_SDCO_T2_TEXASR_CHKSTOP_hold_out)
9	ROX	Reserved field. (Access type is SDCX_SDCO_T2_BESCR_CHKSTOP_hold_out)
10:11	RO	constant=0b00
12	ROX	Reserved field. (Access type is SDCX_SDCU_T2_MCHK_AND_ME_EQ_0_hold_out)
13	ROX	Reserved field. (Access type is SDCC_T3_HEAD_TAIL_XSTOP_HOLD_OUT)
14	ROX	Reserved field. (Access type is SDCC_T4_HEAD_TAIL_XSTOP_HOLD_OUT)
15	ROX	Reserved field. (Access type is SDCC_T5_HEAD_TAIL_XSTOP_HOLD_OUT)

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Register Name	<i>ISU Error Report Hold_out Register 3</i>
Mnemonic	EXP.EC.SD.ISU_REG3_HOLD_OUT
Address	0000000010013343 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is SDCX_SDCO_T3_HEIR_CHKSTOP_hold_out)
1	ROX	Reserved field. (Access type is SDCX_SDCO_T3_HSRR1_CHKSTOP_hold_out)
2	ROX	Reserved field. (Access type is SDCX_SDCO_T3_MSR_CHKSTOP_hold_out)
3	ROX	Reserved field. (Access type is SDCX_SDCO_T3_SRR1_CHKSTOP_hold_out)
4	ROX	Reserved field. (Access type is SDCX_SDCO_T3_VRSAVE_BKUP_CHKSTOP_hold_out)
5	ROX	Reserved field. (Access type is SDCX_SDCO_T3_VRSAVE_CHKSTOP_hold_out)
6	ROX	Reserved field. (Access type is SDCX_SDCO_T3_FSCR_CHKSTOP_hold_out)
7	ROX	Reserved field. (Access type is SDCX_SDCO_T3_HFSCR_CHKSTOP_hold_out)
8	ROX	Reserved field. (Access type is SDCX_SDCO_T3_TEXASR_CHKSTOP_hold_out)
9	ROX	Reserved field. (Access type is SDCX_SDCO_T3_BESCR_CHKSTOP_hold_out)
10:11	RO	constant=0b00
12	ROX	Reserved field. (Access type is SDCX_SDCU_T3_MCHK_AND_ME_EQ_0_hold_out)
13	ROX	Reserved field. (Access type is SDCC_T6_HEAD_TAIL_XSTOP_HOLD_OUT)
14	ROX	Reserved field. (Access type is SDCC_T7_HEAD_TAIL_XSTOP_HOLD_OUT)
15	ROX	Reserved field. (Access type is SDCEA_REGFILE_XSTOP_HOLD_OUT)

Register Name	<i>ISU Error Report Hold_out Register 4</i>
Mnemonic	EXP.EC.SD.ISU_REG4_HOLD_OUT
Address	0000000010013344 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is SDCX_SDCO_T4_HEIR_CHKSTOP_hold_out)
1	ROX	Reserved field. (Access type is SDCX_SDCO_T4_HSRR1_CHKSTOP_hold_out)
2	ROX	Reserved field. (Access type is SDCX_SDCO_T4_MSR_CHKSTOP_hold_out)
3	ROX	Reserved field. (Access type is SDCX_SDCO_T4_SRR1_CHKSTOP_hold_out)
4	ROX	Reserved field. (Access type is SDCX_SDCO_T4_VRSAVE_BKUP_CHKSTOP_hold_out)
5	ROX	Reserved field. (Access type is SDCX_SDCO_T4_VRSAVE_CHKSTOP_hold_out)
6	ROX	Reserved field. (Access type is SDCX_SDCO_T4_FSCR_CHKSTOP_hold_out)
7	ROX	Reserved field. (Access type is SDCX_SDCO_T4_HFSCR_CHKSTOP_hold_out)
8	ROX	Reserved field. (Access type is SDCX_SDCO_T4_TEXASR_CHKSTOP_hold_out)
9	ROX	Reserved field. (Access type is SDCX_SDCO_T4_BESCR_CHKSTOP_hold_out)



Bits	SCOM	Field Mnemonic: Description
10:11	RO	constant=0b00
12	ROX	Reserved field. (Access type is SDCX_SDCU_T4_MCHK_AND_ME_EQ_0_hold_out)
13	ROX	Reserved field. (Access type is SDCEB_REGFILE_XSTOP_HOLD_OUT)
14	ROX	Reserved field. (Access type is SDCEB_REGFILE_HOLD_OUT)
15	ROX	Reserved field. (Access type is SDCED_REGFILE_HOLD_OUT)

Register Name	<i>ISU Error Report Hold_out Register 5</i>
Mnemonic	EXP.EC.SD.ISU_REG5_HOLD_OUT
Address	0000000010013345 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is SDCX_SDCO_T5_HEIR_CHKSTOP_hold_out)
1	ROX	Reserved field. (Access type is SDCX_SDCO_T5_HSRR1_CHKSTOP_hold_out)
2	ROX	Reserved field. (Access type is SDCX_SDCO_T5_MSR_CHKSTOP_hold_out)
3	ROX	Reserved field. (Access type is SDCX_SDCO_T5_SRR1_CHKSTOP_hold_out)
4	ROX	Reserved field. (Access type is SDCX_SDCO_T5_VRSAVE_BKUP_CHKSTOP_hold_out)
5	ROX	Reserved field. (Access type is SDCX_SDCO_T5_VRSAVE_CHKSTOP_hold_out)
6	ROX	Reserved field. (Access type is SDCX_SDCO_T5_FSCR_CHKSTOP_hold_out)
7	ROX	Reserved field. (Access type is SDCX_SDCO_T5_HFSCR_CHKSTOP_hold_out)
8	ROX	Reserved field. (Access type is SDCX_SDCO_T5_TEXASR_CHKSTOP_hold_out)
9	ROX	Reserved field. (Access type is SDCX_SDCO_T5_BESCR_CHKSTOP_hold_out)
10:11	RO	constant=0b00
12	ROX	Reserved field. (Access type is SDCX_SDCU_T5_MCHK_AND_ME_EQ_0_hold_out)
13	ROX	Reserved field. (Access type is SDCK_ALLOC_XSTOP_HOLD_OUT)
14	ROX	Reserved field. (Access type is SDCK_T0_VLD_BITS_XSTOP_HOLD_OUT)
15	ROX	Reserved field. (Access type is SDCK_T1_VLD_BITS_XSTOP_HOLD_OUT)

Register Name	<i>ISU Error Report Hold_out Register 6</i>
Mnemonic	EXP.EC.SD.ISU_REG6_HOLD_OUT
Address	0000000010013346 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is SDCX_SDCO_T6_HEIR_CHKSTOP_hold_out)
1	ROX	Reserved field. (Access type is SDCX_SDCO_T6_HSRR1_CHKSTOP_hold_out)
2	ROX	Reserved field. (Access type is SDCX_SDCO_T6_MSR_CHKSTOP_hold_out)



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Bits	SCOM	Field Mnemonic: Description
3	ROX	Reserved field. (Access type is SDCX_SDCO_T6_SRR1_CHKSTOP_hold_out)
4	ROX	Reserved field. (Access type is SDCX_SDCO_T6_VRSAVE_BKUP_CHKSTOP_hold_out)
5	ROX	Reserved field. (Access type is SDCX_SDCO_T6_VRSAVE_CHKSTOP_hold_out)
6	ROX	Reserved field. (Access type is SDCX_SDCO_T6_FSCR_CHKSTOP_hold_out)
7	ROX	Reserved field. (Access type is SDCX_SDCO_T6_HFSCR_CHKSTOP_hold_out)
8	ROX	Reserved field. (Access type is SDCX_SDCO_T6_TEXASR_CHKSTOP_hold_out)
9	ROX	Reserved field. (Access type is SDCX_SDCO_T6_BESCR_CHKSTOP_hold_out)
10:11	RO	constant=0b00
12	ROX	Reserved field. (Access type is SDCX_SDCU_T6_MCHK_AND_ME_EQ_0_hold_out)
13	ROX	Reserved field. (Access type is SDCK_T2_VLD_BITS_XSTOP_HOLD_OUT)
14	ROX	Reserved field. (Access type is SDCK_T3_VLD_BITS_XSTOP_HOLD_OUT)
15	ROX	Reserved field. (Access type is SDCK_T4_VLD_BITS_XSTOP_HOLD_OUT)

Register Name	<i>ISU Error Report Hold_out Register 7</i>
Mnemonic	EXP.EC.SD.ISU_REG7_HOLD_OUT
Address	0000000010013347 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is SDCX_SDCO_T7_HEIR_CHKSTOP_hold_out)
1	ROX	Reserved field. (Access type is SDCX_SDCO_T7_HSRR1_CHKSTOP_hold_out)
2	ROX	Reserved field. (Access type is SDCX_SDCO_T7_MSR_CHKSTOP_hold_out)
3	ROX	Reserved field. (Access type is SDCX_SDCO_T7_SRR1_CHKSTOP_hold_out)
4	ROX	Reserved field. (Access type is SDCX_SDCO_T7_VRSAVE_BKUP_CHKSTOP_hold_out)
5	ROX	Reserved field. (Access type is SDCX_SDCO_T7_VRSAVE_CHKSTOP_hold_out)
6	ROX	Reserved field. (Access type is SDCX_SDCO_T7_FSCR_CHKSTOP_hold_out)
7	ROX	Reserved field. (Access type is SDCX_SDCO_T7_HFSCR_CHKSTOP_hold_out)
8	ROX	Reserved field. (Access type is SDCX_SDCO_T7_TEXASR_CHKSTOP_hold_out)
9	ROX	Reserved field. (Access type is SDCX_SDCO_T7_BESCR_CHKSTOP_hold_out)
10:11	RO	constant=0b00
12	ROX	Reserved field. (Access type is SDCX_SDCU_T7_MCHK_AND_ME_EQ_0_hold_out)
13	ROX	Reserved field. (Access type is SDCK_T5_VLD_BITS_XSTOP_HOLD_OUT)
14	ROX	Reserved field. (Access type is SDCK_T6_VLD_BITS_XSTOP_HOLD_OUT)
15	ROX	Reserved field. (Access type is SDCK_T7_VLD_BITS_XSTOP_HOLD_OUT)

Register Name	<i>ISU Error Report Hold_out Register 8</i>
Mnemonic	EXP.EC.SD.ISU_REG8_HOLD_OUT
Address	0000000010013348 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is SDCU_RAM_XSTOP_HOLD_OUT)
1	ROX	Reserved field. (Access type is SDCU_XSTOP_HOLD_OUT)
2	ROX	Reserved field. (Access type is SDCV_T0_FLUSH_XSTOP_HOLD_OUT)
3	ROX	Reserved field. (Access type is SDCV_T1_FLUSH_XSTOP_HOLD_OUT)
4	ROX	Reserved field. (Access type is SDCV_T2_FLUSH_XSTOP_HOLD_OUT)
5	ROX	Reserved field. (Access type is SDCV_T3_FLUSH_XSTOP_HOLD_OUT)
6	ROX	Reserved field. (Access type is SDCV_T4_FLUSH_XSTOP_HOLD_OUT)
7	ROX	Reserved field. (Access type is SDCV_T5_FLUSH_XSTOP_HOLD_OUT)
8	ROX	Reserved field. (Access type is SDCV_T6_FLUSH_XSTOP_HOLD_OUT)
9	ROX	Reserved field. (Access type is SDCV_T7_FLUSH_XSTOP_HOLD_OUT)
10	ROX	Reserved field. (Access type is SDXID0_REGFILE_HOLD_OUT)
11	ROX	Reserved field. (Access type is SDXID1_REGFILE_HOLD_OUT)
12	ROX	Reserved field. (Access type is SDXIG0_RD_ADDR_HOLD_OUT)
13	ROX	Reserved field. (Access type is SDXIG0_REGFILE_HOLD_OUT)
14	ROX	Reserved field. (Access type is SDXIG0_REGFILE_XSTOP_HOLD_OUT)
15	ROX	Reserved field. (Access type is SDXIG1_RD_ADDR_HOLD_OUT)

Register Name	<i>ISU Error Report Hold_out Register 9</i>
Mnemonic	EXP.EC.SD.ISU_REG9_HOLD_OUT
Address	0000000010013349 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is SDXIG1_REGFILE_HOLD_OUT)
1	ROX	Reserved field. (Access type is SDXIG1_REGFILE_XSTOP_HOLD_OUT)
2	ROX	Reserved field. (Access type is SDXIP0_REGFILE_HOLD_OUT)
3	ROX	Reserved field. (Access type is SDXIP1_REGFILE_HOLD_OUT)
4	ROX	Reserved field. (Access type is SDXIR_LS0_EREJ_HOLD_OUT)
5	ROX	Reserved field. (Access type is SDXIR_LS1_EREJ_HOLD_OUT)
6	ROX	Reserved field. (Access type is SDXIR_LU0_EREJ_HOLD_OUT)
7	ROX	Reserved field. (Access type is SDXIR_LU1_EREJ_HOLD_OUT)
8	ROX	Reserved field. (Access type is SDXM_REGFILE_HOLD_OUT)

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Bits	SCOM	Field Mnemonic: Description
9	ROX	Reserved field. (Access type is SDXM_REGFILE_XSTOP_HOLD_OUT)
10	ROX	Reserved field. (Access type is SDXSC_XSTOP_HOLD_OUT)
11	ROX	Reserved field. (Access type is SDXSS_XSTOP_HOLD_OUT)
12	ROX	Reserved field. (Access type is WAT_INJECT_INT_HOLD_OUT)
13	ROX	Reserved field. (Access type is WAT_INJECT_INT_RECOV_HOLD_OUT)

Register Name	<i>ISU Debug Bus Controls</i>	
Mnemonic	EXP.EC.SD.ISU_DEBUG_CTRL	
Address	000000001001334A (SCOM)	
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0:15	RW	Reserved field. (Access type is isu_hld_out_reg10)

Register Name	<i>IFU Legacy Tcc_err_reset</i>	
Mnemonic	EXP.EC.IFU.TCC_CERR_RESET	
Address	0000000010013380 (SCOM)	
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0	NCX	Reserved field. (Access type is tcc_cerr_reset)

Register Name	<i>IFU Error Report Hold_out Register0</i>	
Mnemonic	EXP.EC.IFU.IFU_REG0_HOLD_OUT	
Address	0000000010013381 (SCOM)	
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	Reserved field. (Access type is ifu_err_hold_out0)

Register Name	<i>IFU Error Report Hold_out Register1</i>	
Mnemonic	EXP.EC.IFU.IFU_REG1_HOLD_OUT	
Address	0000000010013382 (SCOM)	
Attributes		
Description		



Bits	SCOM	Field Mnemonic: Description
0:15	ROX	Reserved field. (Access type is ifu_err_hold_out1)

Register Name	<i>IFU Error Report Hold_out Register2</i>
Mnemonic	EXP.EC.IFU.IFU_REG2_HOLD_OUT
Address	0000000010013383 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	Reserved field. (Access type is ifu_err_hold_out2)

Register Name	<i>IFU Error Report Hold_out Register3</i>
Mnemonic	EXP.EC.IFU.IFU_REG3_HOLD_OUT
Address	0000000010013384 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	Reserved field. (Access type is ifu_err_hold_out3)

Register Name	<i>IFU Error Report Hold_out Register4</i>
Mnemonic	EXP.EC.IFU.IFU_REG4_HOLD_OUT
Address	0000000010013385 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is ifu_err_hold_out4)

Register Name	<i>IDU Muxing For Out1a Bus</i>
Mnemonic	EXP.EC.IFU.I.IFFDM.IFFDM_IFDMX_OUT1A
Address	0000000010013386 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	IFFDM_IFDMX_DBGCTL_OUT1: Values: 12MODE=>0b0 OUT1=>0b1

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Bits	SCOM	Field Mnemonic: Description
1:3	RW	IFFDM_IFDMX_DBGCTL_OUT1_DBMUX0_00: Values: IFUMC=>0b000 IFDIC=>0b001 IFDDC=>0b010 IFDICMERGED=>0b011 IFDD0=>0b100 IFDTC=>0b101
4:6	RW	IFFDM_IFDMX_DBGCTL_OUT1_DBMUX0_01: Values: IFDTC=>0b000 IFUMC=>0b001 IFDIC=>0b010 IFDICMERGE=>0b011 IFDDC=>0b100 IFDD0=>0b101
7:9	RW	IFFDM_IFDMX_DBGCTL_OUT1_DBMUX0_02: Values: IFUMC=>0b000 IFDD0=>0b001 IFDIC=>0b010 IFDTC=>0b011 IFDDC=>0b100
10:12	RW	IFFDM_IFDMX_DBGCTL_OUT1_DBMUX0_03: Values: IFDIC=>0b000 IFUMC=>0b001 IFDIX=>0b010 IFDD1=>0b011 IFDAC=>0b100 IFDD0=>0b101
13:15	RW	IFFDM_IFDMX_DBGCTL_OUT1_DBMUX0_04: Values: IFDIC=>0b000 IFUMC=>0b001 IFDD4=>0b010 IFDTC=>0b011 IFDAC=>0b100 IFDD0=>0b101 IFDIX=>0b110

Register Name	<i>IDU Muxing For Out1b Bus</i>
Mnemonic	EXP.EC.IFU.I.IFFDM.IFFDM_IFDMX_OUT1B
Address	0000000010013387 (SCOM)
Attributes	
Description	



Bits	SCOM	Field Mnemonic: Description
0:2	RW	IFFDM_IFDMX_DBGCTL_OUT1_DBMUX0_05: Values: IFDDC=>0b000 IFUMC=>0b001 IFDAC=>0b010 IFDIC=>0b011 IFDIX=>0b100 IFDD6=>0b101 IFDD3=>0b110
3:5	RW	IFFDM_IFDMX_DBGCTL_OUT1_DBMUX0_06: Values: IFDD3=>0b000 IFDAC24TO31=>0b001 IFDAC0TO7=>0b010 IFDD6=>0b011 IFUMC=>0b100 IFDIC=>0b101 IFDIX=>0b110
6:8	RW	IFFDM_IFDMX_DBGCTL_OUT1_DBMUX0_07: Values: IFDD3=>0b000 IFDAC=>0b001 IFDACMERGED=>0b010 IFDTC=>0b011 IFDIC=>0b100 IFDD6=>0b101 IFUMC=>0b110 IFDIX=>0b111
9:11	RW	IFFDM_IFDMX_DBGCTL_OUT1_DBMUX0_08: Values: IFDIX=>0b000 IFURM=>0b001 IFDAD=>0b010 IFDD3=>0b011 IFDAC=>0b100 IFDD6=>0b101 IFDIC=>0b110
12:14	RW	IFFDM_IFDMX_DBGCTL_OUT1_DBMUX0_09: Values: IFDD3=>0b000 IFDAD=>0b001 IFDAC=>0b010 IFDDC=>0b011 IFDD6=>0b100
15	RW	IFFDM_IFDMX_DBGCTL_OUT1B_Q_UNUSED: iffdm_ifdmx_out1b_q_unused

Register Name	IDU Muxing For Out2a Bus
Mnemonic	EXP.EC.IFU.I.IFFDM.IFFDM_IFDMX_OUT2A
Address	0000000010013388 (SCOM)
Attributes	
Description	

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Bits	SCOM	Field Mnemonic: Description
0:1	RW	IFFDM_IFDMX_DBGCTL_OUT1_DBMUX0_10: Values: IFDAD=>0b00 IFDD0=>0b01 IFDD0MERGED=>0b10 IFDDC=>0b11
2:3	RW	IFFDM_IFDMX_DBGCTL_OUT2: Values: OUT2_12MODE=>0b00 OUT2=>0b01 PRECISE_FLUSH=>0b10
4	RW	IFFDM_IFDMX_DBGCTL_OUT2_12MODE_07: Values: OUT2_12MODE_07=>0b1 OUT2_12MODE_OFF=>0b0
5:6	RW	IFFDM_IFDMX_DBGCTL_OUT2_DBMUX0_00: Values: IFDD7=>0b00 IFDTC=>0b01 IFDD6=>0b10 IFDD0=>0b11
7:8	RW	IFFDM_IFDMX_DBGCTL_OUT2_DBMUX0_01: Values: IFDD6=>0b00 IFDTC=>0b01 IFDD7=>0b10 IFDD0=>0b11
9:11	RW	IFFDM_IFDMX_DBGCTL_OUT2_DBMUX0_02: Values: IFDIX=>0b000 IFDD0=>0b001 IFDD7=>0b010 IFDD6=>0b011 IFDTC=>0b100
12:13	RW	IFFDM_IFDMX_DBGCTL_OUT2_DBMUX0_03: Values: IFDD7=>0b00 IFDD6=>0b01 IFDD0=>0b10 IFDIX=>0b11
14:15	RW	IFFDM_IFDMX_DBGCTL_OUT2_DBMUX0_04: Values: IFDD7=>0b00 IFDD7MERGE=>0b01 IFDIX=>0b10 IFDD0=>0b11

Register Name	<i>IDU Muxing For Out2b Bus</i>
Mnemonic	EXP.EC.IFU.I.IFFDM.IFFDM_IFDMX_OUT2B
Address	0000000010013389 (SCOM)
Attributes	
Description	



Bits	SCOM	Field Mnemonic: Description
0:1	RW	IFFDM_IFDMX_DBGCTL_OUT2_DBMUX0_05: Values: IFDD1_IFDD2=>0b00 IFDAC=>0b01 IFDIX=>0b10 IFDD7=>0b11
2:3	RW	IFFDM_IFDMX_DBGCTL_OUT2_DBMUX0_06: Values: IFDD4_IFDD5=>0b00 IFDAC=>0b01 IFDD7=>0b10 IFDIX=>0b11
4:5	RW	IFFDM_IFDMX_DBGCTL_OUT2_DBMUX0_07: Values: IFDIX=>0b00 IFDAC=>0b01 IFDD7=>0b10
6	RW	IFFDM_IFDMX_DBGCTL_OUT2_DBMUX0_08: Values: IFDAD=>0b0 IFDAC=>0b1
7	RW	IFFDM_IFDMX_DBGCTL_OUT2_DBMUX0_10: Values: IFDAD=>0b0 IFDADMERGED=>0b1
8	RW	IFFDM_IFDMX_DBGCTL_DEBUG_ENABLE: Values: IFDMX_ENABLE=>0b1 IFDMX_DISABLE=>0b0
9	RW	IFFDM_IFDIX_DBGCTL_DEBUG_ENABLE: Values: IFDIX_ENABLE=>0b1 IFDIX_DISABLE=>0b0
10	RW	IFFDM_IFDIC_DBGCTL_DEBUG_ENABLE: Values: IFDIC_ENABLE=>0b1 IFDIC_DISABLE=>0b0
11	RW	IFFDM_IFDMX_DBGCTL_OUT2_SWITCH_9_10: Values: IFDMX_OUT2_SWITCH_9_10=>0b1 IFDMX_OUT2_SWITCH_OFF=>0b0
12:15	RW	IFFDM_IFDMX_OUT2B_Q_UNUSED: iffdm_ifdmx_Out2b_q_unused(0 to 3)

Register Name	IFU Dbg0 Lev1 Muxing 15bits Of 26
Mnemonic	EXP.EC.IFU.I.IFFDM.IFFDM_DBG0A_LEV1_CTL
Address	000000001001338A (SCOM)
Attributes	
Description	

Registers Specification

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Bits	SCOM	Field Mnemonic: Description
0:2	RW	DBG0_LEV1_CTL_SLAT_Q_0_2: Values: DBG0_LEV1_IFD0=>0b000 DBG0_LEV1_IFBSC=>0b001 DBG0_LEV1_IFBBC=>0b010 DBG0_LEV1_IFFAC0=>0b011 DBG0_LEV1_IFFAC1=>0b100
3:5	RW	DBG0_LEV1_CTL_SLAT_Q_3_5: Values: DBG0_LEV1_IFD0=>0b000 DBG0_LEV1_IFBSC=>0b001 DBG0_LEV1_IFBBC=>0b010 DBG0_LEV1_IFFAC0=>0b011 DBG0_LEV1_IFFAC1=>0b100
6:8	RW	DBG0_LEV1_CTL_SLAT_Q_6_8: Values: DBG0_LEV1_IFD0=>0b000 DBG0_LEV1_IFBSC=>0b001 DBG0_LEV1_IFBBC=>0b010 DBG0_LEV1_IFFAC0=>0b011 DBG0_LEV1_IFFAC1=>0b100
9:11	RW	DBG0_LEV1_CTL_SLAT_Q_9_11: Values: DBG0_LEV1_IFD0=>0b000 DBG0_LEV1_IFBSC=>0b001 DBG0_LEV1_IFBBC=>0b010 DBG0_LEV1_IFFAC0=>0b011 DBG0_LEV1_IFFAC1=>0b100
12:14	RW	DBG0_LEV1_CTL_SLAT_Q_12_14: Values: DBG0_LEV1_IFD0=>0b000 DBG0_LEV1_IFBSC=>0b001 DBG0_LEV1_IFBBC=>0b010 DBG0_LEV1_IFFAC0=>0b011 DBG0_LEV1_IFFAC1=>0b100
15	RW	IFFDM_DBG0_LEV1_CTL_Q_UNUSED: dbg0_lev1_ctl_slate_q(15)

Register Name	<i>IFU Dbg0 Lev1 Muxing Bits(16:26) And 1st Capture Enables</i>
Mnemonic	EXP.EC.IFU.I.IFFDM.IFFDM_DBG0B_LEV1_CTL
Address	000000001001338B (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:2	RW	DBG0_LEV1_CTL_SLAT_Q_15_17: Values: DBG0_LEV1_IFD0=>0b000 DBG0_LEV1_IFBSC=>0b001 DBG0_LEV1_IFBBC=>0b010 DBG0_LEV1_IFFAC0=>0b011 DBG0_LEV1_IFFAC1=>0b100

Bits	SCOM	Field Mnemonic: Description
3:5	RW	DBG0_LEV1_CTL_SLAT_Q_18_20: Values: DBG0_LEV1_IFD0=>0b000 DBG0_LEV1_IFBSC=>0b001 DBG0_LEV1_IFBBC=>0b010 DBG0_LEV1_IFFAC0=>0b011 DBG0_LEV1_IFFAC1=>0b100
6:8	RW	DBG0_LEV1_CTL_SLAT_Q_21_23: Values: DBG0_LEV1_IFD0=>0b000 DBG0_LEV1_IFBSC=>0b001 DBG0_LEV1_IFBBC=>0b010 DBG0_LEV1_IFFAC0=>0b011 DBG0_LEV1_IFFAC1=>0b100
9:11	RW	DBG0_LEV1_CTL_SLAT_Q_24_26: Values: DBG0_LEV1_IFD0=>0b000 DBG0_LEV1_IFBSC=>0b001 DBG0_LEV1_IFBBC=>0b010 DBG0_LEV1_IFFAC0=>0b011 DBG0_LEV1_IFFAC1=>0b100
12	RW	FIRST_CAPTURE_Q: Values: FIRST_CAP_ON=>0b1 FIRST_CAP_OFF=>0b0
13	RW	FIRST_CAPTURE_1ST_BUS_Q: Values: FIRST_CAP_1ST_BUS_ON=>0b1 FIRST_CAP_1ST_BUS_OFF=>0b0
14	RW	FIRST_CAPTURE_TOP_2ND_BUS_Q: Values: FIRST_CAP_TOP_2ND_BUS_ON=>0b1 FIRST_CAP_TOP_2ND_BUS_OFF=>0b0
15	RW	FIRST_CAPTURE_BOT_2ND_BUS_Q: Values: FIRST_CAP_BOT_2ND_BUS_ON=>0b1 FIRST_CAP_BOT_2ND_BUS_OFF=>0b0

Register Name	<i>IFU Dbg1 Lev1 Muxing Bits(0:14) And Brucru Enable</i>
Mnemonic	EXP.EC.IFU.I.IFFDM.IFFDM_DBG1A_LEV1_CTL
Address	000000001001338C (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:2	RW	DBG1_LEV1_CTL_SLAT_Q_0_2: Values: DBG1_LEV1_IFD1=>0b000 DBG1_LEV1_IFBSC=>0b001 DBG1_LEV1_IFBBC=>0b010 DBG1_LEV1_IFFAC0=>0b011 DBG1_LEV1_IFFAC1=>0b100

Registers Specification

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Bits	SCOM	Field Mnemonic: Description
3:5	RW	DBG1_LEV1_CTL_SLAT_Q_3_5: Values: DBG1_LEV1_IFD1=>0b000 DBG1_LEV1_IFBSC=>0b001 DBG1_LEV1_IFBBC=>0b010 DBG1_LEV1_IFFAC0=>0b011 DBG1_LEV1_IFFAC1=>0b100
6:8	RW	DBG1_LEV1_CTL_SLAT_Q_6_8: Values: DBG1_LEV1_IFD1=>0b000 DBG1_LEV1_IFBSC=>0b001 DBG1_LEV1_IFBBC=>0b010 DBG1_LEV1_IFFAC0=>0b011 DBG1_LEV1_IFFAC1=>0b100
9:11	RW	DBG1_LEV1_CTL_SLAT_Q_9_11: Values: DBG1_LEV1_IFD1=>0b000 DBG1_LEV1_IFBSC=>0b001 DBG1_LEV1_IFBBC=>0b010 DBG1_LEV1_IFFAC0=>0b011 DBG1_LEV1_IFFAC1=>0b100 DBG1_LEV1_1ST_CAP=>0b101
12:14	RW	DBG1_LEV1_CTL_SLAT_Q_12_14: Values: DBG1_LEV1_IFD1=>0b000 DBG1_LEV1_IFBSC=>0b001 DBG1_LEV1_IFBBC=>0b010 DBG1_LEV1_IFFAC0=>0b011 DBG1_LEV1_IFFAC1=>0b100
15	RW	IFFDM_BRUCRU_DBGCTL_ENABLE: Values: BRUCRU_EN=>0b1 BRUCRU_DIS=>0b0

Register Name	<i>IFU Dbg1 Lev1 Muxing Bits(15:26) And Enables For Dbg0 dbg1 Lev1 Muxes</i>
Mnemonic	EXP.EC.IFU.I.IFFDM.IFFDM_DBG1B_LEV1_CTL
Address	000000001001338D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:2	RW	DBG1_LEV1_CTL_SLAT_Q_15_17: Values: DBG1_LEV1_IFD1=>0b000 DBG1_LEV1_IFBSC=>0b001 DBG1_LEV1_IFBBC=>0b010 DBG1_LEV1_IFFAC0=>0b011 DBG1_LEV1_IFFAC1=>0b100

Bits	SCOM	Field Mnemonic: Description
3:5	RW	DBG1_LEV1_CTL_SLAT_Q_18_20: Values: DBG1_LEV1_IFD1=>0b000 DBG1_LEV1_IFBSC=>0b001 DBG1_LEV1_IFBBC=>0b010 DBG1_LEV1_IFFAC0=>0b011 DBG1_LEV1_IFFAC1=>0b100 DBG1_LEV1_1ST_CAP=>0b101
6:8	RW	DBG1_LEV1_CTL_SLAT_Q_21_23: Values: DBG1_LEV1_IFD1=>0b000 DBG1_LEV1_IFBSC=>0b001 DBG1_LEV1_IFBBC=>0b010 DBG1_LEV1_IFFAC0=>0b011 DBG1_LEV1_IFFAC1=>0b100 DBG1_LEV1_PRECISE_FLUSH=>0b110
9:11	RW	DBG1_LEV1_CTL_SLAT_Q_24_26: Values: DBG1_LEV1_IFD1=>0b000 DBG1_LEV1_IFBSC=>0b001 DBG1_LEV1_IFBBC=>0b010 DBG1_LEV1_IFFAC0=>0b011 DBG1_LEV1_IFFAC1=>0b100 DBG1_LEV1_PRECISE_FLUSH=>0b110
12	RW	ENB_DEBUG0_LEV1_MUX_Q: Values: ENB_DEBUG0_LEV1=>0b1 DIS_DEBUG0_LEV1=>0b0
13	RW	ENB_DEBUG1_LEV1_MUX_Q: Values: ENB_DEBUG1_LEV1=>0b1 DIS_DEBUG1_LEV1=>0b0
14:15	RW	IFFDM_DBG1B_LEV1_CTL_Q_UNUSED: iffdm_dbg1b_lev1_ctl_q_unused(0 to 1)

Register Name	<i>IFU Dbg0 Lev2 Muxing Bits (0:15)</i>
Mnemonic	EXP.EC.IFU.I.IFFDM.IFFDM_DBG0_LEV2_CTL
Address	000000001001338E (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:1	RW	DBG0_LEV2_CTL_SLAT_Q_0_1: Values: DBG0_LEV2_IFFBC=>0b00 DBG0_LEV2_IFFEC=>0b01 DBG0_LEV2_IFFPF=>0b10 DBG0_LEV2_FR_LEV1=>0b11

Registers Specification

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Bits	SCOM	Field Mnemonic: Description
2:3	RW	DBG0_LEV2_CTL_SLAT_Q_2_3: Values: DBG0_LEV2_IFFBC=>0b00 DBG0_LEV2_IFFEC=>0b01 DBG0_LEV2_IFFPF=>0b10 DBG0_LEV2_FR_LEV1=>0b11
4:5	RW	DBG0_LEV2_CTL_SLAT_Q_4_5: Values: DBG0_LEV2_IFFBC=>0b00 DBG0_LEV2_IFFEC=>0b01 DBG0_LEV2_IFFPF=>0b10 DBG0_LEV2_FR_LEV1=>0b11
6:7	RW	DBG0_LEV2_CTL_SLAT_Q_6_7: Values: DBG0_LEV2_IFFBC=>0b00 DBG0_LEV2_IFFEC=>0b01 DBG0_LEV2_IFFPF=>0b10 DBG0_LEV2_FR_LEV1=>0b11
8:9	RW	DBG0_LEV2_CTL_SLAT_Q_8_9: Values: DBG0_LEV2_IFFBC=>0b00 DBG0_LEV2_IFFEC=>0b01 DBG0_LEV2_IFFPF=>0b10 DBG0_LEV2_FR_LEV1=>0b11
10:11	RW	DBG0_LEV2_CTL_SLAT_Q_10_11: Values: DBG0_LEV2_IFFBC=>0b00 DBG0_LEV2_IFFEC=>0b01 DBG0_LEV2_IFFPF=>0b10 DBG0_LEV2_FR_LEV1=>0b11
12:13	RW	DBG0_LEV2_CTL_SLAT_Q_12_13: Values: DBG0_LEV2_IFFBC=>0b00 DBG0_LEV2_IFFEC=>0b01 DBG0_LEV2_IFFPF=>0b10 DBG0_LEV2_FR_LEV1=>0b11
14:15	RW	DBG0_LEV2_CTL_SLAT_Q_14_15: Values: DBG0_LEV2_IFFBC=>0b00 DBG0_LEV2_IFFEC=>0b01 DBG0_LEV2_IFFPF=>0b10 DBG0_LEV2_FR_LEV1=>0b11

Register Name	<i>IFU Dbg0 Lev2 Muxing Bits(16:17) And Dbg1 Lev2 Muxing Bits(0:13)</i>
Mnemonic	EXP.EC.IFU.I.IFFDM.IFFDM_DBG1_LEV2_CTL
Address	000000001001338F (SCOM)
Attributes	
Description	



Bits	SCOM	Field Mnemonic: Description
0:1	RW	DBG0_LEV2_CTL_SLAT_Q_16_17: dbg0_lev2_ctl_slat_q(16 to 17) Values: DBG0_LEV2_IFFBC=>0b00 DBG0_LEV2_IFFEC=>0b01 DBG0_LEV2_IFFPF=>0b10 DBG0_LEV2_FR_LEV1=>0b11
2:3	RW	DBG1_LEV2_CTL_SLAT_Q_0_1: dbg1_lev2_ctl_slat_q(0 to 1) Values: DBG1_LEV2_IFFBC=>0b00 DBG1_LEV2_IFFEC=>0b01 DBG1_LEV2_IFFPF=>0b10 DBG1_LEV2_FR_LEV1=>0b11

Registers Specification

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Bits	SCOM	Field Mnemonic: Description
4:5	RW	DBG1_LEV2_CTL_SLAT_Q_2_3: dbg1_lev2_ctl_slat_q(2 to 3) Values: DBG1_LEV2_IFFBC=>0b00 DBG1_LEV2_IFFEC=>0b01 DBG1_LEV2_IFFPF=>0b10 DBG1_LEV2_FR_LEV1=>0b11
6:7	RW	DBG1_LEV2_CTL_SLAT_Q_4_5: dbg1_lev2_ctl_slat_q(4 to 5) Values: DBG1_LEV2_IFFBC=>0b00 DBG1_LEV2_IFFEC=>0b01 DBG1_LEV2_IFFPF=>0b10 DBG1_LEV2_FR_LEV1=>0b11
8:9	RW	DBG1_LEV2_CTL_SLAT_Q_6_7: dbg1_lev2_ctl_slat_q(6 to 7) Values: DBG1_LEV2_IFFBC=>0b00 DBG1_LEV2_IFFEC=>0b01 DBG1_LEV2_IFFPF=>0b10 DBG1_LEV2_FR_LEV1=>0b11
10:11	RW	DBG1_LEV2_CTL_SLAT_Q_8_9: dbg1_lev2_ctl_slat_q(8 to 9) Values: DBG1_LEV2_IFFBC=>0b00 DBG1_LEV2_IFFEC=>0b01 DBG1_LEV2_IFFPF=>0b10 DBG1_LEV2_FR_LEV1=>0b11
12:13	RW	DBG1_LEV2_CTL_SLAT_Q_10_11: dbg1_lev2_ctl_slat_q(10 to 11) Values: DBG1_LEV2_IFFBC=>0b00 DBG1_LEV2_IFFEC=>0b01 DBG1_LEV2_IFFPF=>0b10 DBG1_LEV2_FR_LEV1=>0b11
14:15	RW	DBG1_LEV2_CTL_SLAT_Q_12_13: dbg1_lev2_ctl_slat_q(12 to 13) Values: DBG1_LEV2_IFFBC=>0b00 DBG1_LEV2_IFFEC=>0b01 DBG1_LEV2_IFFPF=>0b10 DBG1_LEV2_FR_LEV1=>0b11

Register Name	<i>IFU Dbg1 Lev2 Muxing Bits(14:17) And Dbg2 Lev2 Muxing Bits(0:11)</i>
Mnemonic	EXP.EC.IFU.I.IFFDM.IFFDM_DBG2_LEV2_CTL
Address	0000000010013390 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:1	RW	DBG1_LEV2_CTL_SLAT_Q_14_15: dbg1_lev2_ctl_slat_q(14 to 15) Values: DBG1_LEV2_IFFBC=>0b00 DBG1_LEV2_IFFEC=>0b01 DBG1_LEV2_IFFPF=>0b10 DBG1_LEV2_FR_LEV1=>0b11



Bits	SCOM	Field Mnemonic: Description
2:3	RW	DBG1_LEV2_CTL_SLAT_Q_16_17: dbg1_lev2_ctl_slat_q(16 to 17) Values: DBG1_LEV2_IFFBC=>0b00 DBG1_LEV2_IFFEC=>0b01 DBG1_LEV2_IFFPF=>0b10 DBG1_LEV2_FR_LEV1=>0b11
4:5	RW	DBG2_LEV2_CTL_SLAT_Q_0_1: dbg2_lev2_ctl_slat_q(0 to 1) Values: DBG2_LEV2_IFFBC=>0b00 DBG2_LEV2_IFFEC=>0b01 DBG2_LEV2_IFFPF=>0b10 DBG2_LEV2_DBG0_LEV1=>0b11
6:7	RW	DBG2_LEV2_CTL_SLAT_Q_2_3: dbg2_lev2_ctl_slat_q(2 to 3) Values: DBG2_LEV2_IFFBC=>0b00 DBG2_LEV2_IFFEC=>0b01 DBG2_LEV2_IFFPF=>0b10 DBG2_LEV2_DBG0_LEV1=>0b11
8:9	RW	DBG2_LEV2_CTL_SLAT_Q_4_5: dbg2_lev2_ctl_slat_q(4 to 5) Values: DBG2_LEV2_IFFBC=>0b00 DBG2_LEV2_IFFEC=>0b01 DBG2_LEV2_IFFPF=>0b10 DBG2_LEV2_DBG0_LEV1=>0b11
10:11	RW	DBG2_LEV2_CTL_SLAT_Q_6_7: dbg2_lev2_ctl_slat_q(6 to 7) Values: DBG2_LEV2_IFFBC=>0b00 DBG2_LEV2_IFFEC=>0b01 DBG2_LEV2_IFFPF=>0b10 DBG2_LEV2_DBG0_LEV1=>0b11
12:13	RW	DBG2_LEV2_CTL_SLAT_Q_8_9: dbg2_lev2_ctl_slat_q(8 to 9) Values: DBG2_LEV2_IFFBC=>0b00 DBG2_LEV2_IFFEC=>0b01 DBG2_LEV2_IFFPF=>0b10 DBG2_LEV2_DBG0_LEV1=>0b11
14:15	RW	DBG2_LEV2_CTL_SLAT_Q_10_11: dbg2_lev2_ctl_slat_q(10 to 11) Values: DBG2_LEV2_IFFBC=>0b00 DBG2_LEV2_IFFEC=>0b01 DBG2_LEV2_IFFPF=>0b10 DBG2_LEV2_DBG0_LEV1=>0b11

Register Name	<i>IFU Dbg2 Lev2 Muxing Bits(12:17) And Dbg3 Lev2 Muxing Bits(0:9)</i>
Mnemonic	EXP.EC.IFU.I.IFFDM.IFFDM_DBG3_LEV2_CTL
Address	0000000010013391 (SCOM)
Attributes	
Description	

Registers Specification

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Bits	SCOM	Field Mnemonic: Description
0:1	RW	DBG2_LEV2_CTL_SLAT_Q_12_13: dbg2_lev2_ctl_slat_q(12 to 13) Values: DBG2_LEV2_IFFBC=>0b00 DBG2_LEV2_IFFEC=>0b01 DBG2_LEV2_IFFPF=>0b10 DBG2_LEV2_DBG0_LEV1=>0b11
2:3	RW	DBG2_LEV2_CTL_SLAT_Q_14_15: dbg2_lev2_ctl_slat_q(14 to 15) Values: DBG2_LEV2_IFFBC=>0b00 DBG2_LEV2_IFFEC=>0b01 DBG2_LEV2_IFFPF=>0b10 DBG2_LEV2_DBG0_LEV1=>0b11
4:5	RW	DBG2_LEV2_CTL_SLAT_Q_16_17: dbg2_lev2_ctl_slat_q(16 to 17) Values: DBG2_LEV2_IFFBC=>0b00 DBG2_LEV2_IFFEC=>0b01 DBG2_LEV2_IFFPF=>0b10 DBG2_LEV2_DBG0_LEV1=>0b11
6:7	RW	DBG3_LEV2_CTL_SLAT_Q_0_1: dbg3_lev2_ctl_slat_q(0 to 1) Values: DBG3_LEV2_IFFBC=>0b00 DBG3_LEV2_IFFEC=>0b01 DBG3_LEV2_IFFPF=>0b10 DBG3_LEV2_DBG1_LEV1=>0b11
8:9	RW	DBG3_LEV2_CTL_SLAT_Q_2_3: dbg3_lev2_ctl_slat_q(2 to 3) Values: DBG3_LEV2_IFFBC=>0b00 DBG3_LEV2_IFFEC=>0b01 DBG3_LEV2_IFFPF=>0b10 DBG3_LEV2_DBG1_LEV1=>0b11
10:11	RW	DBG3_LEV2_CTL_SLAT_Q_4_5: dbg3_lev2_ctl_slat_q(4 to 5) Values: DBG3_LEV2_IFFBC=>0b00 DBG3_LEV2_IFFEC=>0b01 DBG3_LEV2_IFFPF=>0b10 DBG3_LEV2_DBG1_LEV1=>0b11
12:13	RW	DBG3_LEV2_CTL_SLAT_Q_6_7: dbg3_lev2_ctl_slat_q(6 to 7) Values: DBG3_LEV2_IFFBC=>0b00 DBG3_LEV2_IFFEC=>0b01 DBG3_LEV2_IFFPF=>0b10 DBG3_LEV2_DBG1_LEV1=>0b11
14:15	RW	DBG3_LEV2_CTL_SLAT_Q_8_9: dbg3_lev2_ctl_slat_q(8 to 9) Values: DBG3_LEV2_IFFBC=>0b00 DBG3_LEV2_IFFEC=>0b01 DBG3_LEV2_IFFPF=>0b10 DBG3_LEV2_DBG1_LEV1=>0b11

Register Name		<i>IFU Dbg3 Lev2 Muxing Bits (10:17) And Dbg[0-3] Bits72to87_ctl</i>
Mnemonic		EXP.EC.IFU.I.IFFDM.IFFDM_DBG3A_LEV2_CTL
Address		0000000010013392 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:1	RW	DBG3_LEV2_CTL_SLAT_Q_10_11: dbg3_lev2_ctl_slats_q(10 to 11) Values: DBG3_LEV2_IFFBC=>0b00 DBG3_LEV2_IFFEC=>0b01 DBG3_LEV2_IFFPF=>0b10 DBG3_LEV2_DBG1_LEV1=>0b11
2:3	RW	DBG3_LEV2_CTL_SLAT_Q_12_13: dbg3_lev2_ctl_slats_q(12 to 13) Values: DBG3_LEV2_IFFBC=>0b00 DBG3_LEV2_IFFEC=>0b01 DBG3_LEV2_IFFPF=>0b10 DBG3_LEV2_DBG1_LEV1=>0b11
4:5	RW	DBG3_LEV2_CTL_SLAT_Q_14_15: dbg3_lev2_ctl_slats_q(14 to 15) Values: DBG3_LEV2_IFFBC=>0b00 DBG3_LEV2_IFFEC=>0b01 DBG3_LEV2_IFFPF=>0b10 DBG3_LEV2_DBG1_LEV1=>0b11
6:7	RW	DBG3_LEV2_CTL_SLAT_Q_16_17: dbg3_lev2_ctl_slats_q(16 to 17) Values: DBG3_LEV2_IFFBC=>0b00 DBG3_LEV2_IFFEC=>0b01 DBG3_LEV2_IFFPF=>0b10 DBG3_LEV2_DBG1_LEV1=>0b11
8:9	RW	DBG0_LEV2_BITS72TO87_CTL_SLAT_Q: dbg0_lev2_bits72to87_ctl_slats_q(0 to 1) Values: DBG0_LEV2_LEV1_IFAR=>0b00 DBG0_LEV2_GETS_PREFLSH=>0b01 DBG0_LEV2_DBG0_LEV1=>0b11
10:11	RW	DBG1_LEV2_BITS72TO87_CTL_SLAT_Q: dbg1_lev2_bits72to87_ctl_slats_q(0 to 1) Values: DBG1_LEV2_LEV1_IFAR=>0b00 DBG1_LEV2_GETS_PREFLSH=>0b01 DBG1_LEV2_1STCAP_OR_LEV1=>0b11
12:13	RW	DBG2_LEV2_BITS72TO87_CTL_SLAT_Q: dbg2_lev2_bits72to87_ctl_slats_q(0 to 1) Values: DBG2_LEV2_IFAR_IFFBC=>0b00 DBG2_LEV2_DBG0_LEV1=>0b11
14:15	RW	DBG3_LEV2_BITS72TO87_CTL_SLAT_Q: dbg3_lev2_bits72to87_ctl_slats_q(0 to 1) Values: DBG3_LEV2_IFFBC=>0b00 DBG3_LEV2_DBG1_LEV1=>0b11

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Register Name		IFU Macro Enables
Mnemonic		EXP.EC.IFU.I.IFFDM.IFFDM_MACRO_ENB
Address		0000000010013393 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0	RW	IFFDM_IFFBC_DBCTL_FORCE_DEBUG_SMT_MODE: iffdm_iffbc_dbctl_force_debug_smt_mode Values: IFFBC_FORCE_SMT_MODE=>0b1 OFF=>0b0
1:2	RW	IFFDM_IFFBC_DBCTL_DB_SMT_MODE_ON_FORCE: iffdm_iffbc_dbctl_db_smt_mode_on_force(0 to 1) Values: IFFBC_SMT4=>0b10 IFFBC_SMT8=>0b11 IFFBC_SMT12=>0b01 OFF=>0b00
3:4	RW	IFFDM_IFFBC_DBCTL_DBG_BUS_MODE: iffdm_iffbc_dbctl_dbg_bus_mode(0 to 1) Values: IFFBC_SMT4_EATIBUF_O_SMT8IBUFF=>0b00 IFFBC_SMT8_EAT=>0b11 IFFBC_SMT8_ASSORT=>0b01
5	RW	IFFDM_IFFBC_DBCTL_DBG_BUS_MOVE_BITS: iffdm_iffbc_dbctl_dbg_bus_move_bits Values: IFFBC_MOVE_BITS=>0b1 OFF=>0b0
6	RW	IFFDM_IFFBC_DBCTL_DBG_ENABLE_ALL_CLKS: iffdm_iffbc_dbctl_dbg_enable_all_clks Values: IFFBC_EN_CLKS=>0b1 IFFBC_DIS_CLKS=>0b0
7	RW	IFFDM_IFFPF_DBGCTL_ENABLE: iffdm_iffpf_dbgctl_enable Values: IFFPF_EN=>0b1 OFF=>0b0
8:9	RW	IFFDM_IFFPF_DBGCTL_CONFIG: iffdm_iffpf_dbgctl_config(0 to 1) Values: IFFPF_MODE_0_OR_4=>0b00 IFFPF_MODE_1_OR_5=>0b01 IFFPF_MODE_2_OR_6=>0b10 IFFPF_MODE_3_OR_7=>0b11
10	RW	IFFDM_EAT_DBGCTL_ENABLE: iffdm_eat_dbgctl_enable Values: EAT_EN=>0b1 OFF=>0b0
11:15	RW	IFFDM_EAT_DBGCTL_CONFIG: iffdm_eat_dbgctl_config(0 to 4) Values: IFFAC_MODE0_BUS01=>0b00000 IFFAC_MODE1_BUS1=>0b01010 IFFAC_MODE2_BUS1=>0b00100 IFFAC_MODE3_BUS1=>0b01110 IFFAC_MODE4_BUS1=>0b01000 IFFAC_MODE5_BUS1=>0b10010 IFFAC_DEFAULT=>0b00001



Register Name	<i>IFU SIAR</i>	
Mnemonic	EXP.EC.IFU.I.IFFDM.IFFDM_SIAR_ADDR	
Address	0000000010013394 (SCOM)	
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0:2	RWX	IFFDM_IFFSA_RW_SIARADDR_TID: iffdm_iffsa_siaraddr_tid
3:4	RWX	IFFDM_IFFSA_R_SIARDATA_SEL: iffdm_iffsa_siardata_sel

Register Name	<i>IFU SIARN</i>	
Mnemonic	EXP.EC.IFU.I.IFFDM.IFFDM_SIAR_DATA	
Address	0000000010013395 (SCOM)	
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	IFFDM_SIARN_DATA: iffdm_siarn_data(0 to 15)

Register Name	<i>LSU Error Report Hold_out Register0</i>	
Mnemonic	EXP.EC.LS.LSU_REG0_HOLD_OUT	
Address	00000000100133C0 (SCOM)	
Attributes		
Description		

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is lsexec0_extend_reject_no_dly5_hold_out)
1	ROX	Reserved field. (Access type is lsexec1_extend_reject_no_dly5_hold_out)
2	ROX	Reserved field. (Access type is lsexec2_extend_reject_no_dly5_hold_out)
3	ROX	Reserved field. (Access type is lsexec3_extend_reject_no_dly5_hold_out)
4	ROX	Reserved field. (Access type is lspintr_lsintc_dawr_parity_hold_out)
5	ROX	Reserved field. (Access type is lsslbb_multiple_request_sys_hold_out)
6	ROX	Reserved field. (Access type is lslmq_lslmqc0_res_n_ci_gpr_hold_out)
7	ROX	Reserved field. (Access type is lssrqf_fx0_res_st_data_v_mapper_hold_out)
8	ROX	Reserved field. (Access type is lsertd0_erat_res_multi_hit_hold_out)
9	ROX	Reserved field. (Access type is ltblw_tblw_arb_hold_out)
10:12	RO	constant=0b000
13	ROX	Reserved field. (Access type is lserrd_res_ls0_ldir_sv_par_hold_out)
14	ROX	Reserved field. (Access type is lserrd_lu0_fmt_setp_par_hold_out)
15	ROX	Reserved field. (Access type is lserrd_addc_ls0_fmt_control_error_hold_out)

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Register Name	<i>LSU Error Report Hold_out Register1</i>
Mnemonic	EXP.EC.LS.LSU_REG1_HOLD_OUT
Address	00000000100133C1 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is lsexec0_fin_reject_on_hold_out)
1	ROX	Reserved field. (Access type is lsexec1_fin_reject_on_hold_out)
2	ROX	Reserved field. (Access type is lsexec2_fin_reject_on_hold_out)
3	ROX	Reserved field. (Access type is lsexec3_fin_reject_on_hold_out)
4	ROX	Reserved field. (Access type is lspintr_lsintc_dawrx_parity_hold_out)
5	ROX	Reserved field. (Access type is lsslbc_ert2_multi_busy_on_hold_out)
6	ROX	Reserved field. (Access type is lslmq_lslmqc1_res_n_ci_gpr_hold_out)
7	ROX	Reserved field. (Access type is lssrqf_fx1_res_st_data_v_mapper_hold_out)
8	ROX	Reserved field. (Access type is lsertd1_erat_res_multi_hit_hold_out)
9	ROX	Reserved field. (Access type is ltblw_tblw_chkstp_hold_out)
10:12	RO	constant=0b000
13	ROX	Reserved field. (Access type is lserrd_res_ls0_ldir_tagbit_hold_out)
14	ROX	Reserved field. (Access type is lserrd_lu0_fmt_xer_wr_loads_stor_hold_out)
15	ROX	Reserved field. (Access type is lserrd_addc_ls1_fmt_control_error_hold_out)

Register Name	<i>LSU Error Report Hold_out Register2</i>
Mnemonic	EXP.EC.LS.LSU_REG2_HOLD_OUT
Address	00000000100133C2 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is lsexec0_fx_op_reject_hold_out)
1	ROX	Reserved field. (Access type is lsexec1_fx_op_reject_hold_out)
2	ROX	Reserved field. (Access type is lsexec2_fx_op_reject_hold_out)
3	ROX	Reserved field. (Access type is lsexec3_fx_op_reject_hold_out)
4	ROX	Reserved field. (Access type is lspintr_lsintc_fin_sigpdar_mtmfsdar_hold_out)
5	ROX	Reserved field. (Access type is lsslbc_ert2_multi_grant_on_hold_out)
6	ROX	Reserved field. (Access type is lslmq_lslmqc2_res_n_ci_gpr_hold_out)
7	ROX	Reserved field. (Access type is lssrqf_ls0_fmt_issue_mapper_hold_out)
8	ROX	Reserved field. (Access type is lsertd2_erat_res_multi_hit_hold_out)
9	ROX	Reserved field. (Access type is ltblb_tlb_pty_hold_out)



Bits	SCOM	Field Mnemonic: Description
10:12	RO	constant=0b000
13	ROX	Reserved field. (Access type is lserrd_res_ls1_ldir_ra_par_hold_out)
14	ROX	Reserved field. (Access type is lserrd_lu1_dcac_res_dwe_perr_hold_out)
15	ROX	Reserved field. (Access type is lserrd_addc_lu0_fmt_control_error_hold_out)

Register Name	<i>LSU Error Report Hold_out Register3</i>
Mnemonic	EXP.EC.LS.LSU_REG3_HOLD_OUT
Address	00000000100133C3 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is lsexec0_res_reject_on_hold_out)
1	ROX	Reserved field. (Access type is lsexec1_res_reject_on_hold_out)
2	ROX	Reserved field. (Access type is lsexec2_res_reject_on_hold_out)
3	ROX	Reserved field. (Access type is lsexec3_res_reject_on_hold_out)
4	ROX	Reserved field. (Access type is lspintr_lsintc_hid_parity_hold_out)
5	ROX	Reserved field. (Access type is lsslbc_multi_busy_on_hold_out)
6	ROX	Reserved field. (Access type is lsImq_lsmqc3_res_n_ci_gpr_hold_out)
7	ROX	Reserved field. (Access type is lssrqf_ls1_fmt_issue_mapper_hold_out)
8	ROX	Reserved field. (Access type is lsertd3_erat_res_multi_hit_hold_out)
9	ROX	Reserved field. (Access type is lsxpip_amrd_pty_hold_out)
10:12	RO	constant=0b000
13	ROX	Reserved field. (Access type is lserrd_res_ls1_ldir_sv_par_hold_out)
14	ROX	Reserved field. (Access type is lserrd_lu1_dcac_res_dwo_perr_hold_out)
15	ROX	Reserved field. (Access type is lserrd_addc_lu1_fmt_control_error_hold_out)

Register Name	<i>LSU Error Report Hold_out Register4</i>
Mnemonic	EXP.EC.LS.LSU_REG4_HOLD_OUT
Address	00000000100133C4 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is lsexec0_issue_thread_not_enable_hold_out)
1	ROX	Reserved field. (Access type is lsexec1_issue_thread_not_enable_hold_out)
2	ROX	Reserved field. (Access type is lsexec2_issue_thread_not_enable_hold_out)
3	ROX	Reserved field. (Access type is lsexec3_issue_thread_not_enable_hold_out)
4	ROX	Reserved field. (Access type is lspintr_lsintc_intd_parity_hold_out)



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Bits	SCOM	Field Mnemonic: Description
5	ROX	Reserved field. (Access type is lsslbc_multi_erat_write_hold_out)
6	ROX	Reserved field. (Access type is lsImq_lsmqe_ctle_2_sect_hold_out)
7	ROX	Reserved field. (Access type is lssrqf_sdqr0_fwd_fmt_perr_hold_out)
8	ROX	Reserved field. (Access type is lsertd0_erat_res_pty_hold_out)
9	ROX	Reserved field. (Access type is lsxpip_amrs_pty_hold_out)
10:12	RO	constant=0b000
13	ROX	Reserved field. (Access type is lserrd_res_ls1_ldir_tagbit_hold_out)
14	ROX	Reserved field. (Access type is lserrd_lu1_fmt_setp_par_hold_out)
15	ROX	Reserved field. (Access type is lserrd_ci_rec_hold_out)

Register Name	LSU Error Report Hold_out Register5
Mnemonic	EXP.EC.LS.LSU_REG5_HOLD_OUT
Address	00000000100133C5 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is lsexec0_pipe_overlap_hold_out)
1	ROX	Reserved field. (Access type is lsexec1_pipe_overlap_hold_out)
2	ROX	Reserved field. (Access type is lsexec2_pipe_overlap_hold_out)
3	ROX	Reserved field. (Access type is lsexec3_pipe_overlap_hold_out)
4	ROX	Reserved field. (Access type is lspintr_lsintc_slb_multihit_hold_out)
5	ROX	Reserved field. (Access type is lsslbc_multi_grant_on_hold_out)
6	ROX	Reserved field. (Access type is lsImq_lsmqe_ctle_inv_rd_hold_out)
7	ROX	Reserved field. (Access type is lssrqf_sdqr1_fwd_fmt_perr_hold_out)
8	ROX	Reserved field. (Access type is lsertd1_erat_res_pty_hold_out)
9	ROX	Reserved field. (Access type is lsIrqm_fin_hdwr_chkr_lrq_overflow_hold_out)
10:12	RO	constant=0b000
13	ROX	Reserved field. (Access type is lserrd_res_lu0_ldir_ra_par_hold_out)
14	ROX	Reserved field. (Access type is lserrd_lu1_fmt_xer_wr_loads_stor_hold_out)
15	ROX	Reserved field. (Access type is lserrd_dynam_set_deleted_hold_out)

Register Name	LSU Error Report Hold_out Register6
Mnemonic	EXP.EC.LS.LSU_REG6_HOLD_OUT
Address	00000000100133C6 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is lsexec0_res_hyperv_trap_hold_out)
1	ROX	Reserved field. (Access type is lsexec1_res_hyperv_trap_hold_out)
2	ROX	Reserved field. (Access type is lsexec2_res_hyperv_trap_hold_out)
3	ROX	Reserved field. (Access type is lsexec3_res_hyperv_trap_hold_out)
4	ROX	Reserved field. (Access type is lspintr_lsintc_slb_p_hold_out)
5	ROX	Reserved field. (Access type is lsslb_multi_pgsl_on_hold_out)
6	ROX	Reserved field. (Access type is lsmq_lsmqe_ctle_sl_no_entry_hold_out)
7	ROX	Reserved field. (Access type is lssrqf_sdqr2_fwd_fmt_perr_hold_out)
8	ROX	Reserved field. (Access type is lsertd2_erat_res_pty_hold_out)
9	ROX	Reserved field. (Access type is lsrqm_fin_ld_crosses_cache_line_hold_out)
10:12	RO	constant=0b000
13	ROX	Reserved field. (Access type is lserrd_res_lu0_ldir_sv_par_hold_out)
14	ROX	Reserved field. (Access type is lserrd_lxx_dcac_res_dwe_perr_hold_out_0)
15	ROX	Reserved field. (Access type is lserrd_ls0_dcac_res_dwe_perr_hold_out)

Register Name	<i>LSU Error Report Hold_out Register7</i>
Mnemonic	EXP.EC.LS.LSU_REG7_HOLD_OUT
Address	00000000100133C7 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is lsexec0_fin_spr_wr_not_block_hold_out)
1	ROX	Reserved field. (Access type is lsexec1_fin_spr_wr_not_block_hold_out)
2	ROX	Reserved field. (Access type is lsexec2_gpr_vsr_v_on_hold_out)
3	ROX	Reserved field. (Access type is lsexec3_gpr_vsr_v_on_hold_out)
4	ROX	Reserved field. (Access type is lspintr_lsintc_tlb_multihit_hold_out)
5	ROX	Reserved field. (Access type is lsslb_tlb_l_illegal_enc_hold_out)
6	ROX	Reserved field. (Access type is lsmq_lsmqe_ctle_bad_mc_rld_dtype_hold_out)
7	ROX	Reserved field. (Access type is lssrqf_sdqr3_fwd_fmt_perr_hold_out)
8	ROX	Reserved field. (Access type is lsertd3_erat_res_pty_hold_out)
9	ROX	Reserved field. (Access type is lsrqm_fin_lrq_multi_write_hold_out)
10:12	RO	constant=0b000
13	ROX	Reserved field. (Access type is lserrd_res_lu1_ldir_ra_par_hold_out)
14	ROX	Reserved field. (Access type is lserrd_lxx_dcac_res_dwe_perr_hold_out_1)
15	ROX	Reserved field. (Access type is lserrd_ls0_dcac_res_dwo_perr_hold_out)

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Register Name	<i>LSU Error Report Hold_out Register8</i>
Mnemonic	EXP.EC.LS.LSU_REG8_HOLD_OUT
Address	00000000100133C8 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:1	RO	constant=0b00
2	ROX	Reserved field. (Access type is lsexec2_xer_vsr_v_on_hold_out)
3	ROX	Reserved field. (Access type is lsexec3_xer_vsr_v_on_hold_out)
4	ROX	Reserved field. (Access type is lsprq_lsprqc_both_ports_writing_same_entry_core_hold_out)
5	ROX	Reserved field. (Access type is lsprqm_dscr_or_mppr_spr_parity_sys_hold_out)
6	RO	constant=0b0
7	ROX	Reserved field. (Access type is lssrqf_srqm_perr_rc3_hold_out)
8	ROX	Reserved field. (Access type is lsemqc_emq_control_hold_out)
9	ROX	Reserved field. (Access type is lsirqm_lrq_sync_fsm_too_many_syncs_pending_hold_out)
10:12	RO	constant=0b000
13	ROX	Reserved field. (Access type is lserrd_res_lu1_ldir_sv_par_hold_out)
14	ROX	Reserved field. (Access type is lserrd_lxx_dcac_res_dwe_perr_hold_out_2)
15	ROX	Reserved field. (Access type is lserrd_ls0_fmt_destined_to_vsu_hold_out)

Register Name	<i>LSU Error Report Hold_out Register9</i>
Mnemonic	EXP.EC.LS.LSU_REG9_HOLD_OUT
Address	00000000100133C9 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is lssrqs_concurrent_deallocates_hold_out)
1	ROX	Reserved field. (Access type is lsflsh_fp2_ffn_and_not_uc_hold_out)
2	ROX	Reserved field. (Access type is lsexec2_res_st_data_ci_gpr_hold_out)
3	ROX	Reserved field. (Access type is lsexec3_res_st_data_ci_gpr_hold_out)
4	ROX	Reserved field. (Access type is lsprq_lsprqc_both_ports_writing_same_entry_sys_hold_out)
5	ROX	Reserved field. (Access type is lsprqm_micro_partition_prefetch_overflow_error)
6	RO	constant=0b0
7	ROX	Reserved field. (Access type is lssrqf_st_drain_data_perr_hold_out)
8	ROX	Reserved field. (Access type is lsemqi_sec_erat_multihit_hold_out)
9:12	RO	constant=0b0000
13	ROX	Reserved field. (Access type is lserrd_res_lxx_ldir_mv_par_hold_out)
14	ROX	Reserved field. (Access type is lserrd_lxx_dcac_res_dwe_perr_hold_out_3)



Bits	SCOM	Field Mnemonic: Description
15	ROX	Reserved field. (Access type is lserrd_ls0_fmt_setp_par_hold_out)

Register Name	<i>LSU Error Report Hold_out Register10</i>
Mnemonic	EXP.EC.LS.LSU_REG10_HOLD_OUT
Address	00000000100133CA (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is lssrqs_unexpected_comp_v_hold_out)
1	ROX	Reserved field. (Access type is lsflsh_fp2_flush_next_ucode_hold_out)
2:3	RO	constant=0b00
4	ROX	Reserved field. (Access type is lsprq_lsprqc_prqn_alloc_and_hw_alloc_active_core_hold_out)
5	ROX	Reserved field. (Access type is lswdrd_rc5_wdrx_mhit_hold_out)
6	RO	constant=0b0
7	ROX	Reserved field. (Access type is lssrqf_vs0_st_data_v_mapper_hold_out)
8:12	RO	constant=0b00000
13	ROX	Reserved field. (Access type is lserrd_tl2e_ert2_pty_hold_out)
14	ROX	Reserved field. (Access type is lserrd_lxx_dcac_res_dwo_perr_hold_out_0)
15	ROX	Reserved field. (Access type is lserrd_ls1_dcac_res_dwe_perr_hold_out)

Register Name	<i>LSU Error Report Hold_out Register11</i>
Mnemonic	EXP.EC.LS.LSU_REG11_HOLD_OUT
Address	00000000100133CB (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is lssrqs_unexpected_ifu_finish_hold_out)
1	ROX	Reserved field. (Access type is lsflsh_fp2_invalid_flush_case_hold_out)
2:3	RO	constant=0b00
4	ROX	Reserved field. (Access type is lsprq_lsprqc_prqn_alloc_and_hw_alloc_active_sys_hold_out)
5	ROX	Reserved field. (Access type is lswdrd_rc5_wdrx_perr_sum_hold_out)
6	RO	constant=0b0
7	ROX	Reserved field. (Access type is lssrqf_vs1_st_data_v_mapper_hold_out)
8:12	RO	constant=0b00000
13	ROX	Reserved field. (Access type is lssetc_rc5_setp_rd4_p_error_sum_hold_out)
14	ROX	Reserved field. (Access type is lserrd_lxx_dcac_res_dwo_perr_hold_out_1)
15	ROX	Reserved field. (Access type is lserrd_ls1_dcac_res_dwo_perr_hold_out)

Register Name	<i>LSU Error Report Hold_out Register12</i>
Mnemonic	EXP.EC.LS.LSU_REG12_HOLD_OUT
Address	00000000100133CC (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is Issrqs_unexpected_l2_buffer_decrement_hold_out)
1	ROX	Reserved field. (Access type is Isflsh_fp2_slc_lq_finish_flush_next_hold_out)
2:3	RO	constant=0b00
4	ROX	Reserved field. (Access type is Isprq_Isprqs_multiple_alloc_go_core_hold_out)
5	ROX	Reserved field. (Access type is Issrq_n_srqs_srqr_rc4_perr_hold_out)
6:13	RO	constant=0b00000000
14	ROX	Reserved field. (Access type is Iserrd_lxx_dcac_res_dwo_perr_hold_out_2)
15	ROX	Reserved field. (Access type is Iserrd_ls1_fmt_destined_to_vsu_hold_out)

Register Name	<i>LSU Error Report Hold_out Register13</i>
Mnemonic	EXP.EC.LS.LSU_REG13_HOLD_OUT
Address	00000000100133CD (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is Issrqs_unexpected_ncu_buffer_decrement_hold_out)
1:3	RO	constant=0b000
4	ROX	Reserved field. (Access type is Isprq_Isprqs_multiple_alloc_go_sys_hold_out)
5:13	RO	constant=0b000000000
14	ROX	Reserved field. (Access type is Iserrd_lxx_dcac_res_dwo_perr_hold_out_3)
15	ROX	Reserved field. (Access type is Iserrd_ls1_fmt_setp_par_hold_out)

Register Name	<i>LSU Error Report Hold_out Register14</i>
Mnemonic	EXP.EC.LS.LSU_REG14_HOLD_OUT
Address	00000000100133CE (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is Issrqs_unexpected_nest_ack_hold_out)
1:3	RO	constant=0b000



Bits	SCOM	Field Mnemonic: Description
4	ROX	Reserved field. (Access type is Isxreg_Isxreg_any_xreg_pty_hold_out)
5:13	RO	constant=0b0000000000
14	ROX	Reserved field. (Access type is Iserrd_mt_rec_hold_out)
15	ROX	Reserved field. (Access type is Iserrd_lu0_dcac_res_dwe_perr_hold_out)

Register Name	<i>LSU Error Report Hold_out Register15</i>
Mnemonic	EXP.EC.LS.LSU_REG15_HOLD_OUT
Address	00000000100133CF (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is Issrqs_unexpected_steal_grant_hold_out)
1:13	RO	constant=0b00000000000000
14	ROX	Reserved field. (Access type is Iserrd_res_ls0_ldir_ra_par_hold_out)
15	ROX	Reserved field. (Access type is Iserrd_lu0_dcac_res_dwo_perr_hold_out)

Register Name	<i>RAM Instruction Mode Register</i>
Mnemonic	EXP.EC.PC.PC_NE.FIR.RAM_MODE_REG
Address	0000000010013C00 (SCOM)
Attributes	Secure=true
Description	

Bits	SCOM	Field Mnemonic: Description
0	RWX	RAM_MODE_ENABLE: RAM mode enable
1	RWX	HV_MODE_THR0_ZERO: HV mode bit thread0 forced to zero
2	RWX	HV_MODE_THR0_ONE: HV mode bit thread0 forced to one
3	RWX	HV_MODE_THR1_ZERO: HV mode bit thread1 forced to zero
4	RWX	HV_MODE_THR1_ONE: HV mode bit thread1 forced to one
5	RWX	HV_MODE_THR2_ZERO: HV mode bit thread2 forced to zero
6	RWX	HV_MODE_THR2_ONE: HV mode bit thread2 forced to one
7	RWX	HV_MODE_THR3_ZERO: HV mode bit thread3 forced to zero
8	RWX	HV_MODE_THR3_ONE: HV mode bit thread3 forced to one
9	RWX	HV_MODE_THR4_ZERO: HV mode bit thread4 forced to zero
10	RWX	HV_MODE_THR4_ONE: HV mode bit thread4 forced to one
11	RWX	HV_MODE_THR5_ZERO: HV mode bit thread5 forced to zero
12	RWX	HV_MODE_THR5_ONE: HV mode bit thread5 forced to one
13	RWX	HV_MODE_THR6_ZERO: HV mode bit thread6 forced to zero
14	RWX	HV_MODE_THR6_ONE: HV mode bit thread6 forced to one

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Bits	SCOM	Field Mnemonic: Description
15	RWX	HV_MODE_THR7_ZERO: HV mode bit thread7 forced to zero
16	RWX	HV_MODE_THR7_ONE: HV mode bit thread7 forced to one

Register Name	<i>RAM Instruction Control Register</i>
Mnemonic	EXP.EC.PC.PC_NE.FIR.RAM_CTRL_REG
Address	0000000010013C01 (SCOM)
Attributes	Secure=true
Description	

Bits	SCOM	Field Mnemonic: Description
0:2	RWX	RAM_THREAD_SELECT: RAM thread select
3:34	RWX	RAM_INSTR: RAM instruction

Register Name	<i>RAM Instruction Status Register</i>
Mnemonic	EXP.EC.PC.PC_NE.FIR.RAM_STATUS_REG
Address	0000000010013C02 (SCOM)
Attributes	Secure=true
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	RAM_CONTROL_RECOV: RAM_SCOM_during_recovery
1	ROX	RAM_STATUS: RAM Instruction completed
2	ROX	RAM_EXCEPTION: RAM Exception reported
3	ROX	LSU_EMPTY: Isu empty after RAM

Register Name	<i>RAM Instruction Control Register</i>
Mnemonic	EXP.EC.PC.PC_NE.FIR.TRUSTED_BOOT_EN_REG
Address	0000000010013C03 (SCOM)
Attributes	Secure=true
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	Reserved field. (Access type is trusted_boot_en)

Register Name		Activity Sampling Modes
Mnemonic		EXP.TP.ECO_DOM.OHA.OHA_ACTIVITY_SAMPLE_MODE_REG
Address		0000000010020000 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0	RW	ENABLE_ACTIVITY_SAMPLING: enable activity sampling, which is based on the TOD timer and the delay specified by ppt_trace_timer_match_val
1	RW	ENABLE_PPT_TRACE: If 0, the PPT feature is disabled. If 1, the PPT feature is enabled. To de-assert enable_ppt_trace the following steps need to be done: - All of the ppt trigger enables must be de-asserted (ppt_timer_timeout_enable, ppt_lpar_change_enable, ppt_global_actual_change_enable, ppt_local_voltage_change_enable, ppt_ivrm_bypass_change_enable, ppt_idle_entry_enable, ppt_idle_exit_enable) - Wait for at least 16 us to allow any ongoing PPT generation to complete or poll OHA_RO_STATUS_REG.ppt_fsm_l until ppt_fsm_l = 000. - De-assert enable_ppt_trace.
2	RW	L2_ACT_COUNT_IS_FREE_RUNNING: L2 activity count is free-running if 1, no other side effects
3	RW	L3_ACT_COUNT_IS_FREE_RUNNING: L3 activity count is free-running if 1, no other side effects
4	RW	ACTIVITY_SAMPLE_L2L3_ENABLE: if 1 then L2/L3 activity values are included into the activity proxy calculation. NOTE: either this dial or core_activity_sample_enable needs to be asserted when enable_activity_sampling is asserted. Further this dial activates the activity accumulators for I2 and I3 regardless of the setting of enable_activity_sampling.
5	RW	CORE_ACTIVITY_SAMPLE_ENABLE: if 1 enable core activity sampling and take values into account for activity proxy calculation. NOTE: either this dial core core_activity_sample_enable needs to be asserted
6	RW	DISABLE_ACTIVITY_PROXY_RESET: if 1, no reset takes place for activity proxy calculation accumulator (even if the switch enable_reset_of_counters_while_sleeping is on). Setting this bit to 1 requires the enable_reset_of_counters_while_sleeping also to be 0 to allow for a real free running activity proxy.
7:11	RW	POWER_PROXY_ACTIVITY_RANGE_SELECT_VCS: if 00000 16 LSBs out of the activity_proxy_VCS, if 10100 16 MSBs out of the activity_proxy_VCS
12:16	RW	POWER_PROXY_ACTIVITY_RANGE_SELECT_VDD: if 00000 16 LSBs out of the activity_proxy_VDD, if 10100 16 MSBs out of the activity_proxy_VDD
17:20	RW	MEMORY_ACTIVITY_RANGE_SELECT: if 0000 16 LSBs out of the memory_activity, if 1000 16 MSBs out of the Memory_activity
21:23	RW	AVG_FREQ_COUNTER_SCALER: Values 0,...,7 indicate to scale (divide) the 32bit Average frequency counter, in order that the scaled count will fit into 16 bits for the OHA_PROXY_LEGACY_REG. The mapping to the 16 bits OHA_PROXY_LEGACY_REG are as below If 000: bit 14 to 29 (divide by 2 ²) If 001: bit 12 to 27 (divide by 2 ⁴) If 010: bit 10 to 25 (divide by 2 ⁶) If 011: bit 8 to 23 (divide by 2 ⁸) If 100: bit 6 to 21 (divide by 2 ¹⁰) If 101: bit 4 to 19 (divide by 2 ¹²) If 110: bit 2 to 17 (divide by 2 ¹⁴) If 111: bit 0 to 15 (divide by 2 ¹⁶)
24:34	RW	PPT_TRACE_TIMER_MATCH_VAL: The Power Proxy Trace timer can be programmed with this dial to expire within a range of 32us to 64ms. The delay is 32us * ppt_trace_timer_match_val
35	RW	DISABLE_PPT_INT_TIMER_RESET: If 0, then the PPT interval field represents a time interval (timer difference to last PPT record), whereas when this switch is set the PPT interval field represents a timestamp (monotonically increasing).

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Bits	SCOM	Field Mnemonic: Description
36:37	RW	PPT_INT_TIMER_SELECT: the dial PPT_int_timer_select selects the time ticks for the PPT interval timer (0=25us, 1=0.5us, 2=1us, and 3=2us)
38	RW	DISABLE_PPT_CYCLE_COUNTER_RESET: If 0, then the PPT cycle counter records CPU / 2 clock cycles over the Power proxy sampling interval. If 1, then the PPT cycle counter is a free-running counter.
39:41	RW	PPT_CYCLE_COUNTER_SCALER: Values 0,...,7 indicate to scale (divide) the 28bit PPT cycle counter, in order that the scaled count will fit into 16 bits for the Power Proxy Trace record. The mapping to the 16 bit power proxy trace record are as below If 000: bit 12 to 27 If 001: bit 11 to 26 (divide by 2) If 010: bit 10 to 25 (divide by 4) If 011: bit 8 to 23 (divide by 16) If 100: bit 6 to 21 (divide by 64) If 101: bit 4 to 19 (divide by 256) If 110: bit 2 to 17 (divide by 1024) If 111: bit 0 to 15 (divide by 4096)
42:47	RW	PPT_SQUASH_TIMER_MATCH_VAL: This field sets the interval of the Power Proxy Trace squash timer, designed to reduce trace flurries. The squash timer starts whenever a Power Proxy Trace record is generated in response to an enabled event. Any other enabled events that occur before the squash timer times out are ignored, unless the event has priority (see the *_priority bits). A value of 0 disables the squash timer, effectively allowing all enabled events to cause a trace record whenever they occur. Each LSB of this timer represents 8us, giving a range of 8 - 504 us.
48	RW	PPT_TIMER_TIMEOUT_ENABLE: This bit enables a Power Proxy Trace record in the event of a trace timer timeout.
49	RW	PPT_LPAR_CHANGE_ENABLE: This bit enables a Power Proxy Trace record in the event of change to PMCR.lpar_id.
50	RW	PPT_GLOBAL_ACTUAL_CHANGE_ENABLE: This bit enables a Power Proxy Trace record in the event of Global Pstate Actual change
51	RW	PPT_LOCAL_VOLTAGE_CHANGE_ENABLE: This bit enables a Power Proxy Trace record in the event of a local voltage change under control of the iVRM
52	RW	PPT_IVRM_BYPASS_CHANGE_ENABLE: This bit enables a Power Proxy Trace record in the event of a change of the bypass mode of the iVRM
53	RW	PPT_IDLE_ENTRY_ENABLE: This bit enables a Power Proxy Trace record in the event of entry into an architected idle state.
54	RW	PPT_IDLE_EXIT_ENABLE: This bit enables a Power Proxy Trace record in the event of exit from an architected idle state.
55	RW	PPT_TIMER_TIMEOUT_PRIORITY: If set, then the named event is exempt from being squashed by the Power Proxy Trace squash timer.
56	RW	PPT_LPAR_CHANGE_PRIORITY: If set, then the named event is exempt from being squashed by the Power Proxy Trace squash timer.
57	RW	PPT_GLOBAL_ACTUAL_CHANGE_PRIORITY: If set, then the named event is exempt from being squashed by the Power Proxy Trace squash timer.
58	RW	PPT_LOCAL_VOLTAGE_CHANGE_PRIORITY: If set, then the named event is exempt from being squashed by the Power Proxy Trace squash timer.
59	RW	PPT_IVRM_BYPASS_CHANGE_PRIORITY: If set, then the named event is exempt from being squashed by the Power Proxy Trace squash timer.
60	RW	PPT_IDLE_ENTRY_PRIORITY: If set, then the named event is exempt from being squashed by the Power Proxy Trace squash timer.
61	RW	PPT_IDLE_EXIT_PRIORITY: If set, then the named event is exempt from being squashed by the Power Proxy Trace squash timer.

Bits	SCOM	Field Mnemonic: Description
62	RW	PPT_LEGACY_MODE: This bit enables the legacy mode in which firmware can do a direct SCOM read of a single register (OHA_PROXY_LEGACY_REG) containing the activity proxies and average frequency counter. No data will be sent to CHTM

Register Name	<i>OHA Activity Counts VCS</i>
Mnemonic	EXP.TP.ECO_DOM.OHA.OHA_VCS_ACTIVITY_CNT_REG
Address	0000000010020001 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:23	ROX	L2_ACTIVITY_COUNT_24BIT_VCS: L2 activity count
24:47	ROX	L3_ACTIVITY_COUNT_24BIT_VCS: L3 activity count

Register Name	<i>OHA Activity Counts VDD</i>
Mnemonic	EXP.TP.ECO_DOM.OHA.OHA_VDD_ACTIVITY_CNT_REG
Address	0000000010020002 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:23	ROX	L2_ACTIVITY_COUNT_24BIT_VDD: L2 activity count
24:47	ROX	L3_ACTIVITY_COUNT_24BIT_VDD: L3 activity count

Register Name	<i>Idle Detect Settings And Actions</i>
Mnemonic	EXP.TP.ECO_DOM.OHA.OHA_LOW_ACTIVITY_DETECT_MODE_REG
Address	0000000010020003 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	LOW_ACTIVITY_DETECT_SAMPLE_ENABLE: enables OHA to run timer and send sample pulse to core
1:8	RW	LOW_ACTIVITY_DETECT_TIMER_SELECT_FOR_ENTRY: index of timer to define the interval for LAD entry. low_activity_detect_timer_select_for_entry defines a bit index of a 24bit counter which counts in 256* OHA clock cycles. A value of 0 results in the longest time and a value of 23 results in the shortest time
9:16	RW	LOW_ACTIVITY_DETECT_TIMER_SELECT_FOR_EXIT: index of timer to define the interval for LAD exit. low_activity_detect_timer_select_for_exit defines a bit index of a 24bit counter which counts in 256* OHA clock cycles. A value of 0 results in the longest time and a value of 23 results in the shortest time
17:20	RW	LOW_ACTIVITY_DETECT_THRESHOLD_RANGE: valid values are 0,1,2,....,12 for shift of internal 28 bit run counter with the goal to reduce this to a 16 bit value. afterward the 16 bit threshold (see below) is compared to the 16 bit result

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Bits	SCOM	Field Mnemonic: Description
21:36	RW	LOW_ACTIVITY_DETECT_THRESHOLD_ENTRY: if shifted run count is below this threshold, we define, that the core is idling and OHA will enter low activity detect mode
37:52	RW	LOW_ACTIVITY_DETECT_THRESHOLD_EXIT: if shifted run count is below this threshold, we define, that the core is not idling any more and OHA will exit low activity detect mode

Register Name	<i>Activity Proxies And Frequency To Be Read Out By OCC</i>
Mnemonic	EXP.TP.ECO_DOM.OHA.OHA_ACTIVITY_AND_FREQU_REG
Address	0000000010020004 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	ROX	LOW_ACTIVITY_DETECT_ENGAGED: if asserted, OHA has detected, that the core activity (runcyles) is below the threshold

Register Name	<i>OHA Counters For Debugging</i>
Mnemonic	EXP.TP.ECO_DOM.OHA.OHA_COUNTER_REG
Address	0000000010020005 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	BASE_COUNTER: TODO: change to display 2nd TOD timer!
16:31	ROX	IDLE_DETEC_TIMER: Low Activity Detect Timer: for debugging
32:47	ROX	TOD_COUNT_MSBS: 16 MSBs of 21 Bit TOD counter for debugging
48	ROX	PPT_CYCLE_COUNT_OVFL: asserted if ppt_cycle_counter overflows
49	ROX	PPT_PARITY_ERROR: asserted when there is a parity error at the ppt_bar_reg

Register Name	<i>OHA Effective Frequency And Memory Activity</i>
Mnemonic	EXP.TP.ECO_DOM.OHA.OHA_PROXY_REG
Address	0000000010020006 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	AVERAGE_FREQUENCY: 32 bit average frequency: number of cycles during the last TOD timer interval T=tod_pulse_count_match_val/32MHz interval for frequency measurement. Each new TOD timer interval start will trigger the capture in this DIAL. In LPFT-Mode this DIAL will be reset (all 0) as long the signal tp_cplt_avgfreq_req from PMX is de-asserted. Once a TOD timer interval is completed this DIAL contains again the cycle count of the previous cycle. count.
32:55	ROX	SPECIAL_MEMORY_ACTIVITY_CNT: Memory Activity Counter - Partition 0 (which is the 11th counter that is shifted from the core to OHA)

Register Name	<i>Activity Proxies And Frequency To Be Read Out By OCC When In Legacy Mode (not Using The New Trace Facility).</i>
Mnemonic	EXP.TP.ECO_DOM.OHA.OHA_PROXY_LEGACY_REG
Address	0000000010020007 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:15	ROX	APROXY_VDD: VDD activity proxy
16:31	ROX	APROXY_VCS: VCS activity proxy
32:47	ROX	MEMORY_ACTIVITY_CNT: Memory Activity Counter - Partition 0 (which is the 11th counter that is shifted from the core to OHA)
48:63	ROX	SCALED_AVERAGE_FREQUENCY: Scaled average frequency (cycle count, DIAL OHA_PROXY_REG.average_frequency) over the sampling interval. The scaling is defined with the DIAL OHA_ACTIVITY_SAMPLE_MODE_REG.avg_freq_counter_scaler

Register Name	<i>Frequency Control Modes And Power Shifting</i>
Mnemonic	EXP.TP.ECO_DOM.OHA.OHA_SKITTER_CTRL_MODE_REG
Address	0000000010020008 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:2	RW	START_SKITTER_MUX_SEL: Selects from which source the start_skitter output is driven 0=start_in 1=Reserved for PMX_OHA_START_SKITTER_PLS from PCBS-PM Start (pulse) - not implemented in PCBS in P8 2=Reserved - zero output 3=Reserved - zero output 4=Reserved - zero output 5=Reserved for Wakeup started - not implemented in P8 All other settings result in an all zero output
3:5	RW	STOP_SKITTER_MUX_SEL: Selects from which source the start_skitter output is driven 0=stop_in 1=Reserved - zero output 2=Reserved for PMX_OHA_STOP_SKITTER_PLS from PCBS-PM Stop (pulse) - not implemented in PCBS in P8 3=OHA Skitter Timer 4=Reserved - zero output 5=Reserved for Wakeup started - not implemented in P8 6=Reserved for Wakeup done - not implemented in P8 All other settings result in an all zero output

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Bits	SCOM	Field Mnemonic: Description
6:8	RW	SKITTER_TIMER_START_MUX_SEL: Selects from which source the start_skitter output is driven 0=start_in 1=PMX_OHA_START_SKITTER_PLS from PCBS-PM Start (pulse) - not implemented in PCBS in P8 2=PMX_OHA_STOP_SKITTER_PLS from PCBS-PM Stop (pulse) - not implemented in PCBS in P8 3=OHA Skitter Timer 4=Reserved - zero output 5=Reserved for Wakeup started - not implemented in P8 6=Reserved for Wakeup done - not implemented in P8 All other settings result in an all zero output
9	RW	DISABLE_SKITTER_QUALIFICATION_MODE: If set to 1 the qualification latch is not used for skitter triggering and the MUXes will get the unqualified signals
10	RW	SKITTER_TIMER_ENABLE_FREERUN_MODE: If set to 1 the skitter timer runs at cache_nclk speed otherwise at cache_nclk/64k
11:14	RW	SKITTER_TIMER_RANGE_SELECT: Selects bit 0 to bit 15 of the skitter timer to generate the pulse for the stop_skitter output

Register Name	CPM Mode Register
Mnemonic	EXP.TP.ECO_DOM.OHA.OHA_CPM_CTRL_REG
Address	000000001002000A (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:1	RW	CPM_BIT_SEL: (NEW for P7 Plus!) selects bit 0 (for value 0) to bit 3 (for value 3) of the ANDed CPM bits that gets routed into bit3 of the error report macro. Note that bit4 of the 5-bit CPM output cannot be used as an error source.
2:4	RW	CPM_BIT_SEL_TRIG_0: Selects bit 0 (for value 0) to bit 7 (for value 7) of the ANDed CPM bits that gets used as a trigger(0) in the TPC_DBG macro
5:7	RW	CPM_BIT_SEL_TRIG_1: Selects bit 0 (for value 0) to bit 7 (for value 7) of the ANDed CPM bits that gets used as a trigger(1) in the TPC_DBG macro
8:15	RW	SCOM_MARKER: Defines the marker bits for debug trace
16:17	RW	CPM_MARK_SELECT: 00: encoded CPM data (0:7) 01: core throttled indication encoded CPM data (1:7) 10: 8-bit SCOM marker (0:7) 11: marker 0:3 encoded CPM data(3:6)
18	RW	CPM_HTM_MODE: Bit to select if PPT (Power Proxy Trace) data or CPM Data will be send to HTM 0: PPT-HTM-Mode (default) 1: CPM-HTM-Mode
19:26	RW	CPM_SCOM_MASK: 8-bit SCOM Mask ANDed to indicate which bit change edge positions should be used for HTM (applied to both CPM inputs)
27:28	RW	CPM_SCOM_MODE: 2 SCOM Mode bits indicate whether a change in (throttle OR suppress) or a change in Marker value (respectively) should be ignored for generating an HTM trace record, in addition to a change in the masked CPM value
29	RW	CPM_DATA_MODE: Bit to select if the ANDed encoded CPM data0/1 or only encoded CPM data0 will form the encoded CPM data 0: ANDed encoded CPM data0/1 (default) 1: encoded CPM data0



Register Name	<i>Read-Only Status Register</i>
Mnemonic	EXP.TP.ECO_DOM.OHA.OHA_RO_STATUS_REG
Address	000000001002000B (SCOM) 000000001002000C (PCB1)
Attributes	
Description	

Bits	SCOM	PCB1	Field Mnemonic: Description
0	ROX	ROX	LOW_ACTIVITY_DETECT_BIT: if run count is below threshold, this bit is 1 and indicates low processor utilization
1	ROX	ROX	SPECIAL_WAKEUP_COMPLETED: (NEW since P7 Plus!) if 1 this indicates, that OHA has reached its final special wakeup state
2:4	ROX	ROX	ARCHITECTED_IDLE_STATE_FROM_CORE: idle state of core (000=non-idle, 101=nap, 110=sleep, 111=winkle)
5	ROX	ROX	CORE_ACCESS_IMPOSSIBLE: this status bit will be asserted when the AISS-FSM is leaving the do_nothing state and has the SLEEP or WINKLE idle-state as target. This will indicate that soon fences are raised or clocks are stopped and prevent core register access.
6	ROX	ROX	ECO_ACCESS_IMPOSSIBLE: this status bit will be asserted when the AISS-FSM is leaving the do_nothing state and has the WINKLE idle-state as target. This will indicate that soon fences are raised or clocks are stopped and prevent eco register access.
7:12	ROX	ROX	SPARE_6BIT: unused
13:19	ROX	ROX	CURRENT_AISS_FSM_STATE_VECTOR: state machine vector for monitoring the architected idle state sequencer
20:22	ROX	ROX	EFF_IDLE_STATE: effective idle state that OHA has reached last (same encoding than the dial architected_idle_state_from_core)
23	ROX	ROX	SPARE_1BIT: dummy bit for byte alignment of bit 24-31
24:31	ROX	ROX	PC_TC_DEEP_IDLE_THREAD_STATE: Architected power management state of each individual thread is not preserved in CORE when the processor core loses state due to power off whether it was Deep Sleep OR Deep Winkle This state is now stored in OHA pc_tc_deep_idle_thread_state (0 to 7) bit state meaning 1 sleep 0 winkle
32:43	ROX	ROX	LPAR_ID: lpar_id send via serial link pc_tc_pmcr(52 to 63) to OHA for PPT
44:47	ROX	ROX	PPT_FSM_L: state vector to monitor the PPT-FSM

Register Name	<i>General OHA Modes And Debug Switches</i>
Mnemonic	EXP.TP.ECO_DOM.OHA.OHA_MODE_REG
Address	000000001002000D (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	ENABLE_IGNORE_RECOV_ERRORS: if asserted the AISS ignores recoverable errors
1	RW	ENABLE_ARCH_IDLE_MODE_SEQUENCER: if 1 then enable OHA to enter doze, nap, sleep or winkle (otherwise, the sequencer can only exit from an idle state, that is, it can wake up from Nap, which is required for IPL)

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Bits	SCOM	Field Mnemonic: Description
2	RW	TREAT_SLEEP_AS_NAP: if 1 a sleep request from core is treated as a nap request
3	RW	TREAT_WINKLE_AS_SLEEP: (NEW for P7 Plus!) if 1 a winkle request from core is treated as a sleep request. Note that the dial treat_sleep_as_nap, if set in addition to this dial, will cause the original winkle request to be translated into a nap.
4	RW	ENABLE_PSTATE_TRACING: enables to trace Pstates for debug trace instead of the AISS FSM state
5	RW	ENABLE_SUPPRESS_PURGES_AND_PCB_FENCE: if asserted, purge requests and the PCB fence will not occur in case of an xstop when OHA is about to go to sleep
6	RW	IDLE_STATE_OVERRIDE_EN: (NEW for P7 Plus!) if 1, OHA ignores the idle request by the PC and uses the dial idle_state_override_value instead. The following protocol need to be followed: - assert a special wakeup - check for special wakeup complete - setup the idle_state_override_value - assert idle_state_override_en - deassert special wakeup ... this will trigger the specified idle entry
7:9	RW	IDLE_STATE_OVERRIDE_VALUE: (NEW for P7 Plus!) idle state override value, 000=non-idle, 110=sleep, 111=winkle . 101=nap is not supported
10	RW	DISABLE_AISS_CORE_HANDSHAKE: (NEW for P7 Plus!) if this dial is asserted, the AISS ignores the interrupt pending signal from the core. Note that asserting this dial and deasserting the dial enable_arch_idle_mode_sequencer causes the AISS to be completely switched off (for enter and exit!)
11:14	RW	AISS_HANG_DETECT_TIMER_SEL: this dial selects the AISS hang timeout: 0=1ms, 2=2ms, 9=512ms, other values are illegal
15	RW	ENABLE_L2_PURGE_ABORT: enables the generation of tc_l2_purge_abort_pls if set to 1
16	RW	ENABLE_L3_PURGE_ABORT: enables the generation of tc_l3_purge_abort_pls if set to 1
17:30	RW	TOD_PULSE_COUNT_MATCH_VAL: select how many TOD pulses to count for averaging the chiplet frequency. This 14bit value is compared with the 14 MSBs of the tod_avg_count. This defines a time interval length from 32us to 524ms for clock-cycle counting. If set to zero TOD pulse counting is disabled.
31:32	RW	TRACE_DEBUG_MODE_SELECT: input select of trace debug bus(bit 10 to 38). Tracemode0=00 (Idle states), Tracemode1=01 (activity proxy), Tracemode2=10 (corecounter), Tracemode3 = 11 (avg frequency)
33	RW	LPFT_MODE: if asserted enables local pstate frequency target mode. The cycle count value (based on the dial ppt_trace_timer_match_val and tod_pulse_count_match_val) will be sent to pcbslpm via serial 4Bit IF .

Register Name		<i>OHA Error And Error Mask Register</i>
Mnemonic		EXP.TP.ECO_DOM.OHA.OHA_ERROR_AND_ERROR_MASK_REG
Address		000000001002000E (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0:7	RW	OHA_ERROR_MASK: Error mask for OHA/DPLL error reporting registers Error mask for OHA/DPLL error reporting registers
8:15	ROX	OHA_CHIPLET_ERRORS: Errors that are held in the c_err_rpt macro (to be sent to the chiplet FIR, if enabled) Errors that are held in the c_err_rpt macro (to be sent to the chiplet FIR, if enabled)



Register Name		<i>Frequencies And Some Settings For Architected Idle Modes</i>
Mnemonic		EXP.TP.ECO_DOM.OHA.OHA_ARCH_IDLE_STATE_REG
Address		0000000010020011 (SCOM)
Attributes		
Description		
Bits	SCOM	Field Mnemonic: Description
0	RW	AISS_THOLD_SEQUENCE_SELECT: arch. idle state sequence: if 0 all tholds (L2, L3 and core) are switched on at the same time, otherwise the tholds are sequenced (in sequ. mode for legacy sleep and P7P sleep the order to thold_ctrl is 000 -> 001 -> 101 -> 111 for enter and 111-> 101 -> 001 -> 000 for exit whereas for P7p sleep the order is 000 -> 100 -> 110 for enter and 110 -> 010 -> 000 for exit). The order of switching does not matter, since all the units are still quiesced and the processor bus is fenced while this switching happens. arch. idle state sequence: if 0 all tholds (L2, L3 and core) are switched on at the same time, otherwise the tholds are sequenced (in sequ. mode for legacy sleep and P7P sleep the order to thold_ctrl is 000 -> 001 -> 101 -> 111 for enter and 111-> 101 -> 001 -> 000 for exit whereas for P7p sleep the order is 000 -> 100 -> 110 for enter and 110 -> 010 -> 000 for exit). The order of switching does not matter, since all the units are still quiesced and the processor bus is fenced while this switching happens.
1	RW	DISABLE_WAITING_ON_L3: wakeup from sleep sequence: if 1 the OHA idle state sequencer does not wait for the L3 ready signal when going from sleep to non-idle state wakeup from sleep sequence: if 1 the OHA idle state sequencer does not wait for the L3 ready signal when going from sleep to non-idle state
2:3	RW	IDLE_SEQ_TIMER_SELECT: selects one of 4 MSBs of 9 bit counter as completion condition for counter (256, 128, 64 and 32 cache nclk cycles are the delays for settings 0,1, and 2, default is 2). Note to software: this value should not be changed in the running system (in which we expect idle state requests coming from the core), but it should remain constant after OHA initialization. Note2: the value 3 is illegal and not supported by the hardware. Note that in master_p7plus_mode_enable mode, this dial needs to be set to 0. selects one of 4 MSBs of 9 bit counter as completion condition for counter (256, 128, 64 and 32 cache nclk cycles are the delays for settings 0,1, and 2, default is 2). Note to software: this value should not be changed in the running system (in which we expect idle state requests coming from the core), but it should remain constant after OHA initialization. Note2: the value 3 is illegal and not supported by the hardware. Note that in master_p7plus_mode_enable mode, this dial needs to be set to 0.
4	RW	ALLOW_AISS_INTERRUPTS: if 0 (which is the default), a wakeup event can not interrupt the idle state sequence when going from non-idle to an idle state like nap or sleep if 0 (which is the default), a wakeup event can not interrupt the idle state sequence when going from non-idle to an idle state like nap or sleep
5	RW	ENABLE_RESET_OF_COUNTERS_WHILE_SLEEPWINKLE: (Dial RENAMED for P7 Plus!) if 1, all internal counts like the base counter, activity proxy, power proxy etc. are forced to 0 while we are in sleep or winkle mode. Note that this bit needs to be set to 1 for P7 DD2.0 hardware and higher to fix HW071431 (Dial RENAMED for P7 Plus!) if 1, all internal counts like the base counter, activity proxy, power proxy etc. are forced to 0 while we are in sleep or winkle mode. Note that this bit needs to be set to 1 for P7 DD2.0 hardware and higher to fix HW071431
6	RW	SELECT_P7P_SEQ_WAIT_TIME: (NEW for P7 Plus!) E1430 uses 64 cache_nclk cycles for wait times. Set to 1 to select 256 cache_nclk cycles as a backup plan if something unexpected in the design. (NEW for P7 Plus!) E1430 uses 64 cache_nclk cycles for wait times. Set to 1 to select 256 cache_nclk cycles as a backup plan if something unexpected in the design.

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Bits	SCOM	Field Mnemonic: Description
7	RW	DISABLE_AUTO_SLEEP_ENTRY: (NEW for P7 Plus!) Disables automated OHA Sleep sequencing for bug workaround. If asserted, immediately after receiving a sleep request from the core, the architected idle state sequencer triggers an interrupt (to ask the PORE for help) and then waits for an AISS reset (cf. reset_idle_state_sequencer). NOTE that this also bypasses the PM sequencer in the PCB-Slave macro. OHA_AISS_IO_REG will be then be used manually by PORE. (NEW for P7 Plus!) Disables automated OHA Sleep sequencing for bug workaround. If asserted, immediately after receiving a sleep request from the core, the architected idle state sequencer triggers an interrupt (to ask the PORE for help) and then waits for an AISS reset (cf. reset_idle_state_sequencer). NOTE that this also bypasses the PM sequencer in the PCB-Slave macro. OHA_AISS_IO_REG will be then be used manually by PORE.
8	RW	DISABLE_AUTO_WINKLE_ENTRY: (NEW for P7 Plus!) Disables automated OHA Winkle sequencing for bug workaround. For workarounds if asserted, immediately after receiving a winkle request from the core, the architected idle state sequencer triggers an interrupt (to ask the PORE for help) and then waits for an AISS reset (cf. reset_idle_state_sequencer). NOTE that this also bypasses the PM sequencer in the PCB-Slave macro. OHA_AISS_IO_REG will then be used manually by PORE. (NEW for P7 Plus!) Disables automated OHA Winkle sequencing for bug workaround. For workarounds if asserted, immediately after receiving a winkle request from the core, the architected idle state sequencer triggers an interrupt (to ask the PORE for help) and then waits for an AISS reset (cf. reset_idle_state_sequencer). NOTE that this also bypasses the PM sequencer in the PCB-Slave macro. OHA_AISS_IO_REG will then be used manually by PORE.
9	NCX	RESET_IDLE_STATE_SEQUENCER: a 1 generates a pulse to reset the idle state sequencer, there is no need to perform a 2nd write with a value of 0 a 1 generates a pulse to reset the idle state sequencer, there is no need to perform a 2nd write with a value of 0

Register Name	Configuration For PMU
Mnemonic	EXP.TP.ECO_DOM.OHA.OHA_PMU_CONFIG_REG
Address	0000000010020012 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:7	RW	PMU_PSTATE_THRESHOLD_A: FUNCTION DROPPED: Pstate compare value for event A
8:15	RW	PMU_PSTATE_THRESHOLD_B: FUNCTION DROPPED: Pstate compare value for event B
16:18	RW	PMU_CONFIGURATION: MUX selects (cf. workbook)

Register Name	CPM History Reset Register
Mnemonic	EXP.TP.ECO_DOM.OHA.OHA_CPM_HIST_RESET_REG
Address	0000000010020013 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0	RW	HIST_RESET: CCB94. history reset bit. Write a 1 to this bit will cause the rising edge detection to generate a history reset pulse to the TPC_DBG
1	RW	PCONLY_SPECIAL_WAKEUP: CCB205 HW211453: Bit to trigger a lightweight pconly-special-wakeup from NAP to be able to read the EMPATH counters in PC.

Register Name	<i>Replace Architected Idle State Sequencer</i>
Mnemonic	EXP.TP.ECO_DOM.OHA.OHA_AISS_IO_REG
Address	0000000010020014 (SCOM)
Attributes	
Description	All These Bits Can Be Used To Replace The Architected Idle State Sequencer By Using Firmware Or The PORE. They Are All High-active If Not Denoted Otherwise. This Register Is Writable If Enable_arch_idle_mode_sequencer Is Zero. If Not Denoted Otherwise, All Bits Are Level Signals.

Bits	SCOM	Field Mnemonic: Description
0:1	RWX	SPARE_2BITS_B: spare_2bits_b spare_2bits_b
2:5	RWX	TC_TP_CHIPLET_PM_STATE: PM state send to PCB slave (bit 0=doze, bit 1=nap, bit 2=sleep, 3=winkle) PM state send to PCB slave (bit 0=doze, bit 1=nap, bit 2=sleep, 3=winkle)
6	RWX	TC_PB_SLEEP: Async. disconnect of the processor bus in P7 legacy mode only Async. disconnect of the processor bus in P7 legacy mode only
7:9	RWX	TC_TC_PM_THOLD_CTRL: Requested state to clock control (bit 0 = core, bit 1 = L2, bit 2 = L3) Requested state to clock control (bit 0 = core, bit 1 = L2, bit 2 = L3)
10	RWX	TC_L3_FENCE_LCO: LCO fence for the L3 LCO fence for the L3
11	RWX	TC_NCU_FENCE: Fence the NCU Fence the NCU
12	RWX	CHKSW_HW237039DIS: needs to be 1 to disable HW237039 needs to be 1 to disable HW237039
13	RWX	TC_L3_INIT_DRAM: Initialize eDRAM Initialize eDRAM
14	RWX	TC_PB_PURGE: Request to purge the processor bus Request to purge the processor bus
15	RWX	TC_PC_PM_WAKE_UP: Wakeup signal to the core Wakeup signal to the core
16	RWX	SPARE_ENTRY_FOR_CONFIG_BIT: for future extensions for future extensions
17	RWX	RESET_OF_COUNTERS_WHILE_SLEEPWINKLE: During sleep mode, all internal counters and activity values in OHA are reset. A falling edge of this dial will cause a reset of the core activity values. During sleep mode, all internal counters and activity values in OHA are reset. A falling edge of this dial will cause a reset of the core activity values.
18	RWX	TC_CHTM_PURGE: Purge CHTM (is a level now despite of output signal name in VHDL!) Purge CHTM (is a level now despite of output signal name in VHDL!)
19	RWX	TC_TP_TERMINATE_PCB: Sends request to PCB slave to terminate current PCB transaction and fence off PCB bus Sends request to PCB slave to terminate current PCB transaction and fence off PCB bus
20	RWX	TC_OHA_THERM_PURGE_LVL: fences thermal macro fences thermal macro
21	RWX	PSCOM_CORE_FENCE_LVL: fences off core PSCOM rings fences off core PSCOM rings
22	RWX	PB_ECO_FENCE_LVL: fences off PB (stop coherency traffic from entering core domain) fences off PB (stop coherency traffic from entering core domain)

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Bits	SCOM	Field Mnemonic: Description
23	RWX	CORE2CACHE_FENCE_REQ: requests PCBS to assert the core2cache fence (level) requests PCBS to assert the core2cache fence (level)
24	RWX	CACHE2CORE_FENCE_REQ: requests PCBS to assert the cache2core fence (level) requests PCBS to assert the cache2core fence (level)
25	RWX	PERVASIVE_ECO_FENCE_REQ: spare spare
26	RWX	TC_OHA_PMX_FENCE_REQ_LVL_L: fences off fences off
27	RWX	UPDATEOHA_FREQ: Trigger PCB interrupt to PMC to get a frequency update (pulse) Trigger PCB interrupt to PMC to get a frequency update (pulse)
28	RWX	REQ_IDLE_STATE_CHANGE: Trigger PCB interrupt to PMC to start PMC idle state actions (pulse). Note that this bit should not be used in P7+ since the request can not be configured with a PCB register. FW should use the PMC register PMC_REQUEST_OVERWRITE_REG to inject idle requests rather than triggering those in OHA. Trigger PCB interrupt to PMC to start PMC idle state actions (pulse). Note that this bit should not be used in P7+ since the request can not be configured with a PCB register. FW should use the PMC register PMC_REQUEST_OVERWRITE_REG to inject idle requests rather than triggering those in OHA.
29	RWX	TC_L2_PURGE: Purge request to L2 (pulse) Purge request to L2 (pulse)
30	RWX	TC_L3_PURGE: Purge request to L3 (pulse) Purge request to L3 (pulse)
31	RWX	TC_NCU_PURGE: Purge request to NCU (pulse) Purge request to NCU (pulse)
32	RWX	TC_L2_PURGE_ABORT: Purge abort to L2 (pulse) Purge abort to L2 (pulse)
33	RWX	TC_L3_PURGE_ABORT: Purge abort to L3 (pulse) Purge abort to L3 (pulse)
34:36	ROX	PC_TC_PM_STATE: PM state from core: 000=run, 101=nap, 110=sleep, and 111=winkle PM state from core: 000=run, 101=nap, 110=sleep, and 111=winkle
37	ROX	L2_PURGE_IS_DONE: L2 purge is done (sticky level, reset, when purge is requested) L2 purge is done (sticky level, reset, when purge is requested)
38:40	ROX	L3_NCU_CHTM_PURGE_DONE: bit 0 = L2 purge is done, bit 1 = NCU purge is done, bit 2 = CHTM purge is done (sticky level, reset, when purge is requested) bit 0 = L2 purge is done, bit 1 = NCU purge is done, bit 2 = CHTM purge is done (sticky level, reset, when purge is requested)
41	ROX	tc_tc_xstop_err chiplet xstop error is pending
42	ROX	tc_tc_recov_err chiplet recoverable error is pending
43	ROX	PB_TC_PURGE_ACTIVE_LVL: PB purge is active PB purge is active
44	ROX	L3_TC_DRAM_READY_LVL: L3 reinit is done (sticky level, reset, when dram init is requested) L3 reinit is done (sticky level, reset, when dram init is requested)
45	ROX	core_fsm_non_idle if asserted, OHA is currently shifting out data from the core (Note: in this mode, the core clocks should not be stopped)
46	ROX	tc_pscom_core_fence_done PSCOM has fenced off the core rings, if asserted



Bits	SCOM	Field Mnemonic: Description
47	ROX	tc_pmx_oha_fence_done PMX has fenced off the core rings, if asserted
48	ROX	L2_PURGE_ABORT_STICKY: This status bit is asserted once the l2-purge is aborted and de-asserted once the AISS is leaving the DO_NOTHING-state This status bit is asserted once the l2-purge is aborted and de-asserted once the AISS is leaving the DO_NOTHING-state
49	ROX	L3_PURGE_ABORT_STICKY: This status bit is asserted once the l3-purge is aborted and deasserted once the AISS is leaving the DO_NOTHING-state This status bit is asserted once the l3-purge is aborted and deasserted once the AISS is leaving the DO_NOTHING-state

Register Name	<i>New For POWER8 Processor: Power Proxy Trace Setup</i>
Mnemonic	EXP.TP.ECO_DOM.OHA.OHA_PPT_BAR_REG
Address	0000000010020015 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:45	RW	PPT_BAR: Base address register for CHTM interface (bits 14..59 of the 50-bit processor bus address). Bits 60..63 of the address are implied as 0 (for 16-byte aligned accesses).
46:52	RW	PPT_SIZE_MASK: mask for 7 LSBs of CHTM address: a 1 enables that the associated bit from the 7 bit PPT address counter is used for the final address, whereas a 0 defines that the bit is defined by the the associated bit in ppt_bar[39..45]
53:55	RW	PPT_ADDRESS_SCOPE: Starting processor bus scope for CHTM interface. Bit 4..6 of Word0 (Beat0)

Register Name	<i>Configuration Of CC Counters</i>
Mnemonic	EXP.TP.ECO_DOM.SYNC_CONFIG
Address	0000000010030000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	ISLE_XSTOP_MASK_B: mask for clockstop of all island clocks on xstop from chiplet
1	RW	PCB_XSTOP_MASK_B: mask for clockstop of all island clocks on xstop from pcb
2	RW	CLKSTP_SYNC_EN: stop clocks aligned to sync pulse
3	RW	EDRAM_XSTOP_MASK_B: mask for clockstop of edram clock on any xstop
4	RW	PLL_XSTOP_MASK_B: mask for clockstop of pll clock on any xstop
5	RW	LOCAL_XSTOP_MASK_B: mask for clockstop of all island clocks on local xstop from chiplet
6	RW	DISABLE_PCB_ITR: disable interrupt generation within CC
7	RW	USE_SYNC_FOR_SCAN: if set, use opcg initial alignment for scan requests
8	RW	KEEP_EDRAM_ON_XSTOP: keep edram enabled when a checkstop occurs
9	RW	TRIGGER_OPCG_ON_XSTOP: trigger opcg on xstop instead of performing clockstop
10	RW	SEL_EXT_OPCG_TRIGGER: select external OPCG trigger (set OPCG in slave mode)

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Bits	PCB	Field Mnemonic: Description
11	RW	LISTEN_TO_SYNC_PULSE: enable phase counter synchronization by sync_pulse signal
12	RW	SYNC_CLK_START_ENABLE: enable clk start driven by tc_sync_clk_stop (falling edge)
13	RW	SYNC_CLK_STOP_ENABLE: enable clk stop driven by tc_sync_clk_stop (rising edge)
14	RWX_WOR	CHIP_PROTECTION_ENABLE: Memory buffer only - can only be set, but not cleared via PCB. When this bit is SET, no clock starts are possible
15	RW	SPARE15: spare
16	RW	SPARE16: spare
17	RW	SPARE17: spare
18	RW	SPARE18: spare
19	RW	SPARE19: spare
20	RW	SPARE20: spare

Register Name	Counter Offset
Mnemonic	EXP.TP.ECO_DOM.PHASE_SHADOW
Address	0000000010030001 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RWX	PHASE_COUNT_SHADOW_Q: offset for sync counter
6	RO	constant=0b0

Register Name	OPCG Control Register 0
Mnemonic	EXP.TP.ECO_DOM.OPCG_REG0
Address	0000000010030002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	RUNN_MODE: runn-mode if 1 or BIST mode if 0
1	RWX	OPCG_GO: opcg go (start sequence)
2	RWX	RUN_SCAN0: run scan0 (will override all BIST mode settings but the scan_ratio)
3	RW	SCAN0_MODE: set PRPGs in scan0_mode but do not run automatic scan0 sequence
4:8	RW	SCAN_RATIO: scan_ratio (n=0-15: (n+1):1, 16: 24:1, 17: 32:1, 18: 48:1, 19: 64:1, 20: 128:1)
9	RW	INOP_FORCE_SG: Set SG high during INOP
10:13	RW	INOP_ALIGN: INOP phase alignment (0: none, 1: 2:1, 2: 3:1, 3: 4:1, 4: 6:1, 5: 8:1, 6: 12:1, 7: 16:1, 8: 24:1)
14:20	RW	INOP_WAIT: INOP cycle delay (1-127)
21:24	RWX	SNOP_ALIGN: BIST mode: SNOP phase alignment (like INOP), runn-mode: loopcnt(0:3)
25:27	RWX	SNOP_WAIT: BIST mode: SNOP cycle delay (0-7), runn-mode: loopcnt(4:6)



Bits	PCB	Field Mnemonic: Description
28:31	RWX	ENOP_ALIGN: BIST mode: ENOP phase alignment (like INOP), runn-mode: loopcnt(7:10)
32:34	RWX	ENOP_WAIT: BIST mode: ENOP cycle delay (0-7), runn-mode: loopcnt(11:13)
35	RWX	ENOP_FORCE_SG: BIST mode: Set SG high during ENOP, runn-mode: loopcnt(14)
36:63	RWX	LOOP_COUNT: BIST mode: loop count ($l = 1-2^{28}$ (about 5 minutes LBIST)), runn-mode: loopcnt(15:42)

Register Name	OPCG Control Register 1
Mnemonic	EXP.TP.ECO_DOM.OPCG_REG1
Address	0000000010030003 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	FUNC_CAPT_COUNT: BIST mode: capture cycles (1-12) encoded as capture cycle - 1
4:8	RW	FUNC_CAPT_SEQ01_01F: BIST mode: capture cycle 1 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
9:13	RW	FUNC_CAPT_SEQ02_02F: BIST mode: capture cycle 2 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
14:18	RW	FUNC_CAPT_SEQ03_03F: BIST mode: capture cycle 3 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
19:23	RW	FUNC_CAPT_SEQ04_04F: BIST mode: capture cycle 4 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
24:28	RW	FUNC_CAPT_SEQ05_05F: BIST mode: capture cycle 5 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
29:33	RW	FUNC_CAPT_SEQ06_06F: BIST mode: capture cycle 6 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
34:38	RW	FUNC_CAPT_SEQ07_07F: BIST mode: capture cycle 7 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
39:43	RW	FUNC_CAPT_SEQ08_08F: BIST mode: capture cycle 8 for fast domain or single mesh support(sl, nsl, ary, sg, fce)
44:48	RW	FUNC_CAPT_SEQ09_01F: BIST mode: capture cycle 1 for slow domain or cycle 9 for single mesh support(sl, nsl, ary, sg, fce)
49:53	RW	FUNC_CAPT_SEQ10_02F: BIST mode: capture cycle 2 for slow domain or cycle 10 for single mesh support(sl, nsl, ary, sg, fce)
54:58	RW	FUNC_CAPT_SEQ11_03F: BIST mode: capture cycle 3 for slow domain or cycle 11 for single mesh support(sl, nsl, ary, sg, fce)
59:63	RW	FUNC_CAPT_SEQ12_04F: BIST mode: capture cycle 4 for slow domain or cycle 12 for single mesh support(sl, nsl, ary, sg, fce)

Register Name	OPCG Control Register 2
Mnemonic	EXP.TP.ECO_DOM.OPCG_REG2
Address	0000000010030004 (PCB)
Attributes	
Description	

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Bits	PCB	Field Mnemonic: Description
0:11	RW	SCAN_COUNT: BIST mode: Channel scan count (s = 0-4095) runn-mode: start_abist match value(0:11)
12:23	RW	MISR_A_VAL: BIST mode: a value for MISR aperture, runn-mode: start_abist match value(12:23)
24:35	RW	MISR_B_VAL: BIST mode: b value for MISR aperture, runn-mode: start_abist match value(24:35)
36:47	RW	MISR_INIT_WAIT: BIST mode: delay MISR aperture, MISRs get active after this number of loops
48	RW	OPCG_SUPPRESS_EVEN_CLK: OPCG will only create even and not odd clocks. Used for runn to create only one clock in fast domain. Default is 0
49:51	RW	OPCG_PAD_VALUE: After setting all DC signals, wait this many number of cycle x 16 before applying tholds
52	RW	USE_F_AND_FDIV2: BIST mode: if 1, use 8 f and 4 f/2 pattern concurrently, else use 1-12 local mesh patterns
53	RW	USE_ARY_CLK_DURING_FILL: BIST mode: Fire nsl_ary_clock during NSL-fill runn-mode: stop run-n on xstop
54	RW	SG_HIGH_DURING_FILL: BIST mode: Hold SG high during NSL-fill and SNOP runn-mode: OPCG engine controls start_abist (overrides GP0 setting)
55	RW	RTIM_THOLD_FORCE: force rtim_thold low when not in test_dc mode (must be 0 at all time)
56	RW	LBIST_SKITTER_CTL: BIST mode: 0: enable skitter during lbist_ip, 1: enable skitter when misr_active
57	RW	MISR_MODE: BIST mode: MISR aperture mode (0: a-1 to b-1, 1: start to a and b to end)
58	RW	INFINITE_MODE: infinite mode
59:63	RW	NSL_FILL_COUNT: BIST mode: NSL-fill count (0-31)

Register Name	<i>Opkg Start Register</i>
Mnemonic	EXP.TP.ECO_DOM.OPCG_REG3
Address	0000000010030005 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	OPCG_GO2: opcg go for broadcast sequences (start sequence)
1	RW	RUN_OPCG_ON_UPDATE_DR: start opcg engine when scan updated (update_dr) received (set pulse)
2	RW	RUN_OPCG_ON_CAPTURE_DR: start opcg engine when scan updated (capture_dr) received (set pulse)
3:4	RW	ALIGN_SOURCE_SELECT: 0: use inopa setting from opcg_reg0, 1: use rising edge of sync pulse, 2: use input from unit (for AVP)
5:7	RW	PRPG_WEIGHTING: prpg_activate: 1/2, 1/4, 1/8, 1/16, 1/2, 3/4, 7/8, 15/16
8:19	RWX	PRPG_VALUE: set to 0 for prpg always on, else seed
20	RW	EXTEND_INOPW_ENOPW: extend I/ENOPW: add 256 cycles if i/enop > 0, else 257 + max i/enop
21	RW	EXTEND_SNOPW: add 256 cycles if snop > 0, else 257 + max snop
22	RW	FORCE_SG_HIGH_DURING_SNOP: force sg high during snop
23:31	RW	CHKSW: reserved for debug witches (keep 0 unless chksw required)
32:43	RW	PRPG_A_VAL: a value for PRPG aperture
44:55	RW	PRPG_B_VAL: b value for PRPG aperture
56	RW	PRPG_MODE: PRPG aperture mode (0: a-1 to b-1, 1: start to a and b to end)



Bits	PCB	Field Mnemonic: Description
57	RW	SCAN_CLK_USE_EVEN: Generate scan clock in odd cycle instead of even. Default is 0
58:63	RW	SPARE3: spares

Register Name	<i>Start/stop Of Clocks</i>
Mnemonic	EXP.TP.ECO_DOM.CLK_REGION
Address	0000000010030006 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RWX	CLOCK_CMD: command for clock control: 00 NOP 01 START 10 STOP 11 PULSE (one pulse)
2:3	RO	constant=0b00
4	RWX	CLOCK_REGION_PERV: for clock region perv (Pervasive)
5	RWX	CLOCK_REGION_FASTUNIT0: for clock region pc
6	RWX	CLOCK_REGION_FASTUNIT1: for clock region l2
7	RWX	CLOCK_REGION_UNIT2: for clock region l3np (l3/nc/pb)
8	RWX	CLOCK_REGION_UNIT3: for clock region unit3 region is UNUSED
9	RWX	CLOCK_REGION_UNIT4: for clock region unit4 region is UNUSED
10	RWX	CLOCK_REGION_UNIT5: for clock region refr
11	RWX	CLOCK_REGION_PLL: for clock region dpll
12:19	RO	constant=0b00000000
20	RWX	SEL_THOLD_SL: select sl tholds
21	RWX	SEL_THOLD_NSL: select nsl tholds
22	RWX	SEL_THOLD_ARY: select array thold

Register Name	<i>Scan Region And Type</i>
Mnemonic	EXP.TP.ECO_DOM.SCANSELQ
Address	0000000010030007 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b000
3	RW_WCLRPA RT	SCANSEL_CLK_VITL: scan clock region vitl (Vital = Clock)
4	RWX	SCANSEL_CLK_PERV: scan clock region perv (Pervasive)
5	RWX	SCANSEL_CLK_FASTUNIT0: scan clock region pc
6	RWX	SCANSEL_CLK_FASTUNIT1: scan clock region l2
7	RWX	SCANSEL_CLK_UNIT2: scan clock region l3np (l3/nc/pb)

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Bits	PCB	Field Mnemonic: Description
8	RWX	SCANSEL_CLK_UNIT3: scan clock region unit3 region is UNUSED
9	RWX	SCANSEL_CLK_UNIT4: scan clock region unit4 region is UNUSED
10	RWX	SCANSEL_CLK_UNIT5: scan clock region refr
11	RWX	SCANSEL_CLK_PLL: scan clock region dpll
12:19	RO	constant=0b00000000
20	RW	SCANSEL_FUNC: scan chain func (functional)
21	RW	SCANSEL_CFG: scan chain mode (boot config and debug config)
22	RW	SCANSEL_CCFG_GPTR: scan chain ccfg / gptra (Pervasive: CC config, Others: GPTR)
23	RW	SCANSEL_REGF: scan chain regf (register files)
24	RW	SCANSEL_LBIST: scan chain lbist (LBIST)
25	RW	SCANSEL_ABIST: scan chain abist (ABIST)
26	RW	SCANSEL_REPR: scan chain repr (Array Repair)
27	RW	SCANSEL_TIME: scan chain time (Array Timing)
28	RW	SCANSEL_BNDY_FARY: scan chain bndy (Boundary IO's)
29	RW	SCANSEL_FARR: scan chain farr (fast array unload)
30	RW	SCANSEL_CMSK: scan chain cmsk (lbist channel mask)

Register Name	<i>Clocks Running</i>
Mnemonic	EXP.TP.ECO_DOM.CLOCK_STAT
Address	0000000010030008 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	CLOCK_STATUS_PERV_FUNC_SL: status of perv func_sl_thold 0=run, 1=stop
1	ROX	CLOCK_STATUS_PERV_FUNC_NSL: status of perv func_nsl_thold 0=run, 1=stop
2	ROX	CLOCK_STATUS_PERV_ARY_NSL: status of perv ary_nsl_thold 0=run, 1=stop
3	ROX	CLOCK_STATUS_FASTUNIT0_ODD_FUNC_SL: status of pc_odd func_sl_thold 0=run, 1=stop
4	ROX	CLOCK_STATUS_FASTUNIT0_EVEN_FUNC_SL: status of pc_even func_sl_thold 0=run, 1=stop
5	ROX	CLOCK_STATUS_FASTUNIT0_ODD_FUNC_NSL: status of pc_odd func_nsl_thold 0=run, 1=stop
6	ROX	CLOCK_STATUS_FASTUNIT0_EVEN_FUNC_NSL: status of pc_even func_nsl_thold 0=run, 1=stop
7	ROX	CLOCK_STATUS_FASTUNIT0_ODD_ARY_NSL: status of pc_odd ary_nsl_thold 0=run, 1=stop
8	ROX	CLOCK_STATUS_FASTUNIT0_EVEN_ARY_NSL: status of pc_even ary_nsl_thold 0=run, 1=stop
9	ROX	CLOCK_STATUS_FASTUNIT1_ODD_FUNC_SL: status of l2_odd func_sl_thold 0=run, 1=stop
10	ROX	CLOCK_STATUS_FASTUNIT1_EVEN_FUNC_SL: status of l2_even func_sl_thold 0=run, 1=stop
11	ROX	CLOCK_STATUS_FASTUNIT1_ODD_FUNC_NSL: status of l2_odd func_nsl_thold 0=run, 1=stop
12	ROX	CLOCK_STATUS_FASTUNIT1_EVEN_FUNC_NSL: status of l2_even func_nsl_thold 0=run, 1=stop
13	ROX	CLOCK_STATUS_FASTUNIT1_ODD_ARY_NSL: status of l2_odd ary_nsl_thold 0=run, 1=stop
14	ROX	CLOCK_STATUS_FASTUNIT1_EVEN_ARY_NSL: status of l2_even ary_nsl_thold 0=run, 1=stop



Bits	PCB	Field Mnemonic: Description
15	ROX	CLOCK_STATUS_UNIT2_FUNC_SL: status of l3np (l3/nc/pb) func_sl_thold 0=run, 1=stop
16	ROX	CLOCK_STATUS_UNIT2_FUNC_NSL: status of l3np (l3/nc/pb) func_nsl_thold 0=run, 1=stop
17	ROX	CLOCK_STATUS_UNIT2_ARY_NSL: status of l3np (l3/nc/pb) ary_nsl_thold 0=run, 1=stop
18	ROX	CLOCK_STATUS_UNIT3_FUNC_SL: status of unit3 func_sl_thold 0=run, 1=stop region is UNUSED
19	ROX	CLOCK_STATUS_UNIT3_FUNC_NSL: status of unit3 func_nsl_thold 0=run, 1=stop region is UNUSED
20	ROX	CLOCK_STATUS_UNIT3_ARY_NSL: status of unit3 ary_nsl_thold 0=run, 1=stop region is UNUSED
21	ROX	CLOCK_STATUS_UNIT4_FUNC_SL: status of unit4 func_sl_thold 0=run, 1=stop region is UNUSED
22	ROX	CLOCK_STATUS_UNIT4_FUNC_NSL: status of unit4 func_nsl_thold 0=run, 1=stop region is UNUSED
23	ROX	CLOCK_STATUS_UNIT4_ARY_NSL: status of unit4 ary_nsl_thold 0=run, 1=stop region is UNUSED
24	ROX	CLOCK_STATUS_UNIT5_FUNC_SL: status of refr func_sl_thold 0=run, 1=stop
25	ROX	CLOCK_STATUS_UNIT5_FUNC_NSL: status of refr func_nsl_thold 0=run, 1=stop
26	ROX	CLOCK_STATUS_UNIT5_ARY_NSL: status of refr ary_nsl_thold 0=run, 1=stop
27	ROX	CLOCK_STATUS_PLL_FUNC_SL: status of dpll func_sl_thold 0=run, 1=stop
28	ROX	CLOCK_STATUS_PLL_FUNC_NSL: status of dpll func_nsl_thold 0=run, 1=stop
29	ROX	CLOCK_STATUS_PLL_ARY_NSL: status of dpll ary_nsl_thold 0=run, 1=stop
30:63	RO	constant=0b1111111111111111111111111111111111111111111111111111111111111111

Register Name	<i>Error Status Of CC</i>
Mnemonic	EXP.TP.ECO_DOM.ERROR_STATUS
Address	0000000010030009 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	PCB_WRITE_NOT_ALLOWED: PCB access error: write not allowed
1	RWX	PCB_READ_NOT_ALLOWED: PCB access error: read not allowed
2	RWX	PCB_PARITY_ERR_ON_CMD: PCB access error: parity error on PCB command
3	RWX	PCB_ADDRESS_NOT_VALID: PCB access error: address not valid
4	RWX	PCB_PARITY_ADDR_ERR: PCB access error: parity error on address
5	RWX	PCB_PARITY_DATA_ERR: PCB access error: parity error on data
6	RWX	PCB_PROTECTED_ACCESS_INVALID: PCB access error: protection violation
7	RWX	PCB_PARITY_SPCIF_ERR: parity error from special packet interface
8	RWX	PCB_WRITE_AND_OPCG: PCB write while opcg in progress
9	RWX	CLOCK_CMD_CONFLICT: clock command conflict: previous one was not yet completed (includes those triggered by tc_sync_clk_stop)
10	RWX	SCAN_COLLISION: scan collision - high when scan protection error occurred
11	RWX	OPCG_TRIGGER_ERROR: opcg triggered while in progress
12	RWX	OPCG_PARITY_ERROR: opcg state machine parity error - during test its OK, but in system its a error
13	RWX	PHASE_CNT_CORRUPTED: phase hold counter corruption detected

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Bits	PCB	Field Mnemonic: Description
14:15	RWX	CC_PAR_ERR: parity error in CC registers (1. opcg & sync config parity error, 2. clock mux parity error)
16	RWX	GPIO_PAR_ERR: parity error in GP0 register
17	RWX	SECURITY_VIOLATION: security_violation - when Chip protection is active and you try a clock start, pulse, which is invalid at this time

Register Name	<i>CC Protect Mode Register</i>
Mnemonic	EXP.TP.ECO_DOM.CC_PROTECT_MODE_REG
Address	00000000100303FE (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	CC_READ_PROTECT_ENABLE: Enable read protection
1	RW	CC_WRITE_PROTECT_ENABLE: Enable write protection

Register Name	<i>Atomic Lock Register</i>
Mnemonic	EXP.TP.ECO_DOM.CC_ATOMIC_LOCK_REG
Address	00000000100303FF (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	CC_ATOMIC_LOCK_ENABLE: Enable atomic lock
1:4	ROX	CC_ATOMIC_ID: Atomic ID

Register Name	<i>Global Checkstop FIR</i>
Mnemonic	EXP.TP.ECO_DOM.XFIR
Address	0000000010040000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	XFIR_IN0: summary bit(any xstop)
1	RWX	XFIR_IN1: xstop from other chiplets
2	RWX	XFIR_IN2: Unused
3	RWX	XFIR_IN3: xstop from pervasive unit
4	RWX	XFIR_IN4: xstop from core unit(pc)
5	RWX	XFIR_IN5: xstop from I2
6	RWX	XFIR_IN6: xstop from I3



Bits	PCB	Field Mnemonic: Description
7	RWX	XFIR_IN7: xstop from from non-cacheable unit (NCU)
8:25	RWX	XFIR_IN8: unused
26	RWX	XFIR_IN26: xstop on debug trigger

Register Name	<i>Global Recoverable FIR</i>
Mnemonic	EXP.TP.ECO_DOM.RFIR
Address	0000000010040001 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	RFIR_IN0: local (core) checkstop from core pervasive (informational)
1	ROX	LFIR_RECOV_ERR: recov from pervasive unit
2	ROX	RFIR_IN4: recov from core unit(pc)
3	ROX	RFIR_IN5: recov from I2
4	ROX	RFIR_IN6: recov from I3
5	ROX	RFIR_IN7: recov from from non-cacheable unit (NCU)
6:23	ROX	RFIR_IN8: unused

Register Name	<i>FIR Mask</i>
Mnemonic	EXP.TP.ECO_DOM.FIR_MASK
Address	0000000010040002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	FIR_MASK_IN0: mask for xfir summary bit(any xstop)
1	RW	FIR_MASK_IN1: mask for xfir from other chiplets
2	RW	FIR_MASK_IN2: Unused
3	RW	FIR_MASK_IN3: mask for xfir from pervasive unit
4	RW	FIR_MASK_IN4: mask for core unit(pc) XFIR and RFIR
5	RW	FIR_MASK_IN5: mask for I2 XFIR and RFIR
6	RW	FIR_MASK_IN6: mask for I3 XFIR and RFIR
7	RW	FIR_MASK_IN7: mask for from non-cacheable unit (NCU) XFIR and RFIR
8:25	RW	FIR_MASK_IN8: unused
26	RW	FIR_MASK_IN26: mask for debug trigger and local xstop to recoverable error

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Register Name	<i>Special Attention</i>
Mnemonic	EXP.TP.ECO_DOM.SPATTN
Address	0000000010040004 (PCB) 0000000010040005 (PCB1) 0000000010040006 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0:7	ROX	NCX	NCX	SPATTN_IN0: Special Attention from Core, Thread 0...7
8:9	ROX	NCX	NCX	SPATTN_IN8: unused special attentions

Register Name	<i>Special Attention Mask</i>
Mnemonic	EXP.TP.ECO_DOM.SPA_MASK
Address	0000000010040007 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:9	RW	SPA_MASK_IN: special attention mask

Register Name	<i>Mode Register</i>
Mnemonic	EXP.TP.ECO_DOM.EPS.FIR.MODE_REG
Address	0000000010040008 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	MODE_IN0: Enable Clockstop on Checkstop
1	RW	MODE_IN1: Enable Clockstop on Recoverable
2	RW	MODE_IN2: Enable Clockstop on Spattn
3	RW	MODE_IN3: Core-only Spattn
4	RW	MODE_IN4: Stop Chip TOD on Checkstop
5	RW	MODE_IN5: Stop Chip TOD on Recoverable
6	RW	MODE_IN6: Disable propagation of checkstop to other chips
7	RW	MODE_IN7: turns xstop on trig into clkstp on trig
8	RW	MODE_IN8: enable xstop on special attention
9	RW	MODE_IN9: mask_direct/local_error
10	RW	MODE_IN10: mask_xstop_to_pcb
11	RW	MODE_IN11: mask external xstop
12:15	RW	MODE_IN: unused

Register Name	<i>Local FIR</i>
Mnemonic	EXP.TP.ECO_DOM.LOCAL_FIR
Address	000000001004000A (PCB) 000000001004000B (PCB1) 000000001004000C (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_IN0: CFIR internal parity error
1	RWX	WOX_AND	WOX_OR	FIR_IN1: local errors from GPIO (PCB error)
2	RWX	WOX_AND	WOX_OR	FIR_IN2: local errors from CC (PCB error)
3	RWX	WOX_AND	WOX_OR	FIR_IN3: local errors from CC (OPCG, parity, scan collision, ...)
4	RWX	WOX_AND	WOX_OR	FIR_IN4: local errors from PSC (PCB error)
5	RWX	WOX_AND	WOX_OR	FIR_IN5: local errors from PSC (parity error)
6	RWX	WOX_AND	WOX_OR	FIR_IN6: local errors from Thermal (parity error)
7	RWX	WOX_AND	WOX_OR	FIR_IN7: local errors from Thermal (PCB error)
8	RWX	WOX_AND	WOX_OR	FIR_IN8: local errors from Thermal (Trip error critical)
9	RWX	WOX_AND	WOX_OR	FIR_IN9: local errors from Thermal (Trip error fatal)
10	RWX	WOX_AND	WOX_OR	FIR_IN10: local errors from Trace Array (error)
11	RWX	WOX_AND	WOX_OR	FIR_IN11: local errors from Trace Array (scom error)
12:13	RWX	WOX_AND	WOX_OR	FIR_IN12: local errors from tral (error)
14	RWX	WOX_AND	WOX_OR	FIR_IN14: local errors from OHA (recov error)
15	RWX	WOX_AND	WOX_OR	FIR_IN15: local errors from OHA (xstop error)
16	RWX	WOX_AND	WOX_OR	FIR_IN16: local errors from skewadj
17	RWX	WOX_AND	WOX_OR	FIR_IN17: local errors from dcadj
18:39	RWX	WOX_AND	WOX_OR	FIR_IN18: unused local errors
40	RWX	WOX_AND	WOX_OR	FIR_IN40: malfunction alert (local xstop in another chiplet)

Register Name	<i>Local FIR Mask</i>			
Mnemonic	EXP.TP.ECO_DOM.EPS.FIR.LOCAL_FIR_MASK			
Address	000000001004000D (PCB) 000000001004000E (PCB1) 000000001004000F (PCB2)			
Attributes				
Description				
Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0:40	RW	WO_AND	WO_OR	LFIR_MASK_IN: mask for LEM error collection vector

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Register Name	<i>Local FIR Action0</i>
Mnemonic	EXP.TP.ECO_DOM.EPS.FIR.LOCAL_FIR_ACTION0
Address	0000000010040010 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:40	RW	FIR_ACTION0_IN: action0 mask

Register Name	<i>Local FIR Action1</i>
Mnemonic	EXP.TP.ECO_DOM.EPS.FIR.LOCAL_FIR_ACTION1
Address	0000000010040011 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:40	RW	FIR_ACTION1_IN: action1 mask

Register Name	<i>Write Configuration Data To Cpm 0-3.0-11: CPM0, 12-23: CPM1, 24-35: CPM2</i>
Mnemonic	EXP.TP.ECO_DOM.EPS.THERM.CPM_CONFIG_WRITE_REG0
Address	0000000010050000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:11	WOX	CPM0_CONFIG_DATA: Address ending in: 0x00 contains CPM0 CONFIG_DATA 0x01 contains CPM0 ENCODED value indicating location of edge in 12-bit sampler 15 means all ones 0 means 0b100000000000 1 means 0b110000000000 2 means 0b111000000000 3 means 0b111100000000 4 means 0b111110000000 5 means 0b111111000000 6 means 0b111111100000 7 means 0b111111110000 8 means 0b111111111000 9 means 0b111111111100 10 means 0b111111111110 11 means 0b111111111111 0x02 contains CPM0 RAW value of the actual 12-bit sampler
12:15	N/A	not implemented



Bits	PCB	Field Mnemonic: Description
16:27	WOX	CPM1_CONFIG_DATA: Address ending in: 0x00 contains CPM1_CONFIG_DATA 0x01 contains CPM1_ENCODED value indicating location of edge in 12-bit sampler 15 means all ones 0 means 0b100000000000 1 means 0b110000000000..... 11 means 0b111111111111 0x02 contains CPM1_RAW value of the actual 12-bit sampler CPM1 is only available in EX core chiplets
28:31	N/A	not implemented
32:43	WOX	CPM2_CONFIG_DATA: Address ending in: 0x00 contains CPM2_CONFIG_DATA 0x01 contains CPM2_ENCODED value indicating location of edge in 12-bit sampler 15 means all ones 0 means 0b100000000000 1 means 0b110000000000..... 11 means 0b111111111111 0x02 contains CPM2_RAW value of the actual 12-bit sampler CPM2 is only available in EX core chiplets
44:63	N/A	not implemented

Register Name	<i>DTS Thermal Sensor Loop1 Results</i>
Mnemonic	EXP.TP.ECO_DOM.EPS.THERM.DTS_RESULT0
Address	0000000010050000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:15	ROX	DTS_0_RESULT: Calibrated DTS Result of sensor with id 0.
16:31	ROX	DTS_1_RESULT: Calibrated DTS Result of sensor with id 1.
32:47	ROX	DTS_2_RESULT: Calibrated DTS Result of sensor with id 2.
48:63	RO	constant=0b0000000000000000

Register Name	<i>Write Configuration Data To Cpm 4-7.0-11: CPM4,</i>
Mnemonic	EXP.TP.ECO_DOM.EPS.THERM.CPM_CONFIG_WRITE_REG1
Address	0000000010050001 (PCB)
Attributes	
Description	

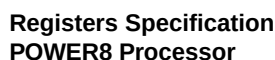
Bits	PCB	Field Mnemonic: Description
0:11	WOX	CPM0_CONFIG_DATA: Address ending in: 0x00 contains CPM0_CONFIG_DATA 0x01 contains CPM0_ENCODED value indicating location of edge in 12-bit sampler 15 means all ones 0 means 0b100000000000 1 means 0b110000000000 2 means 0b111000000000 3 means 0b111100000000 4 means 0b111110000000 5 means 0b111111000000 6 means 0b111111100000 7 means 0b111111110000 8 means 0b111111111000 9 means 0b111111111100 10 means 0b111111111110 11 means 0b111111111111 0x02 contains CPM0_RAW value of the actual 12-bit sampler
12:63	N/A	not implemented

[illegible]

Register Name		DTS Trace Results
Mnemonic		EXP.TP.ECO_DOM.EPS.THERM.DTS_TRC_RESULT
Address		0000000010050003 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:43	ROX	TIMESTAMP_COUNTER_VALUE: Time stamp counter value during DTS trace mode.
44	ROX	TIMESTAMP_COUNTER_OVERFLOW_ERR: Over flow error bit of the time stamp counter value during DTS trace mode.
45:47	RO	constant=0b000
48:63	ROX	DTS_1_RESULT: Calibrated DTS Result of sensor with id 1.



Register Name		<i>RAW CPM Results, CPM1-4 Is Only Available On EX Chiplets. Bit 0 - 11: CPM0, Bit 16 - 27: CPM1, Bit 32 - 43: CPM2,</i>
Mnemonic		EXP.TP.ECO_DOM.EPS.THERM.RAW_CPM_RESULT0
Address		0000000010050005 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:11	ROX	CPM0_CONFIG_DATA: Address ending in: 0x00 contains CPM0 CONFIG_DATA 0x01 contains CPM0 ENCODED value indicating location of edge in 12-bit sampler 15 means all ones 0 means 0b100000000000 1 means 0b110000000000 2 means 0b111000000000 3 means 0b111100000000 4 means 0b111110000000 5 means 0b111111000000 6 means 0b111111100000 7 means 0b111111110000 8 means 0b111111111000 9 means 0b111111111100 10 means 0b111111111110 11 means 0b111111111111 0x02 contains CPM0 RAW value of the actual 12-bit sampler
12:15	RO	constant=0b0000
16:27	ROX	CPM1_CONFIG_DATA: Address ending in: 0x00 contains CPM1 CONFIG_DATA 0x01 contains CPM1 ENCODED value indicating location of edge in 12-bit sampler 15 means all ones 0 means 0b100000000000 1 means 0b110000000000..... 11 means 0b111111111111 0x02 contains CPM1 RAW value of the actual 12-bit sampler CPM1 is only available in EX core chiplets
28:31	RO	constant=0b0000
32:43	ROX	CPM2_CONFIG_DATA: Address ending in: 0x00 contains CPM2 CONFIG_DATA 0x01 contains CPM2 ENCODED value indicating location of edge in 12-bit sampler 15 means all ones 0 means 0b100000000000 1 means 0b110000000000..... 11 means 0b111111111111 0x02 contains CPM2 RAW value of the actual 12-bit sampler CPM2 is only available in EX core chiplets
44:63	RO	constant=0b00000000000000000000



Register Name	RAW CPM Results, CPM4 Is Only Available On EX Chiplets. Bit 0 - 11: CPM4,
Mnemonic	EXP.TP.ECO_DOM.EPS.THERM.RAW_CPM_RESULT1
Address	0000000010050006 (PCB)
Attributes	
Description	

[illegible]

Register Name	<i>Encoded CPM Results</i>
Mnemonic	EXP.TP.ECO_DOM.EPS.THERM.ENC_CPM_RESULT0
Address	0000000010050008 (PCB)
Attributes	
Description	DTS1-4 And CPM1-4 Is Only Available On EX Chiplets Bit 0 - 15: Temperature Result DTS0, Bit 16 - 31: Temperature Result DTS1(available Only On EX Chiplets), Bit 32 - 47: Temperature Result DTS2(available Only On EX Chiplets), Bit 48 - 51: Encoded Data CPM0, Bit 52 - 55: Encoded Data CPM1(available Only On EX Chiplets), Bit 56 - 59: Encoded Data CPM2(available Only On EX Chiplets)

Bits	PCB	Field Mnemonic: Description
0:15	ROX	DTS_0_RESULT: Calibrated DTS Result of sensor with id 0.
16:31	ROX	DTS_1_RESULT: Calibrated DTS Result of sensor with id 1.
32:47	ROX	DTS_2_RESULT: Calibrated DTS Result of sensor with id 2.

Bits	PCB	Field Mnemonic: Description
48:51	ROX	CPM0_CONFIG_DATA: Address ending in: 0x00 contains CPM0 CONFIG_DATA 0x01 contains CPM0 ENCODED value indicating location of edge in 12-bit sampler 15 means all ones 0 means 0b100000000000 1 means 0b110000000000 2 means 0b111000000000 3 means 0b111100000000 4 means 0b111110000000 5 means 0b111111000000 6 means 0b111111100000 7 means 0b111111110000 8 means 0b111111111000 9 means 0b111111111100 10 means 0b111111111110 11 means 0b111111111111 0x02 contains CPM0 RAW value of the actual 12-bit sampler
52:55	ROX	CPM1_CONFIG_DATA: Address ending in: 0x00 contains CPM1 CONFIG_DATA 0x01 contains CPM1 ENCODED value indicating location of edge in 12-bit sampler 15 means all ones 0 means 0b100000000000 1 means 0b110000000000..... 11 means 0b111111111111 0x02 contains CPM1 RAW value of the actual 12-bit sampler CPM1 is only available in EX core chiplets
56:59	ROX	CPM2_CONFIG_DATA: Address ending in: 0x00 contains CPM2 CONFIG_DATA 0x01 contains CPM2 ENCODED value indicating location of edge in 12-bit sampler 15 means all ones 0 means 0b100000000000 1 means 0b110000000000..... 11 means 0b111111111111 0x02 contains CPM2 RAW value of the actual 12-bit sampler CPM2 is only available in EX core chiplets
60:63	RO	constant=0b0000

Register Name	Encoded CPM Results
Mnemonic	EXP.TP.ECO_DOM.EPS.THERM.ENC_CPM_RESULT1
Address	0000000010050009 (PCB)
Attributes	
Description	DTS4 And CPM 4 Is Only Available On EX Chiplets Bit 0 - 15: Temperature Result DTS4(available Only On EX Chiplets), Bit 40 - 43: Encoded Data CPM4(available Only On EX Chiplets)

Bits	PCB	Field Mnemonic: Description
0:15	ROX	DTS_4_RESULT: Calibrated DTS Result of sensor with id 4.
16:47	RO	constant=0b00000000000000000000000000000000

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Bits	PCB	Field Mnemonic: Description
48:51	ROX	CPM0_CONFIG_DATA: Address ending in: 0x00 contains CPM0 CONFIG_DATA 0x01 contains CPM0 ENCODED value indicating location of edge in 12-bit sampler 15 means all ones 0 means 0b100000000000 1 means 0b110000000000 2 means 0b111000000000 3 means 0b111100000000 4 means 0b111110000000 5 means 0b111111000000 6 means 0b111111100000 7 means 0b111111110000 8 means 0b111111111000 9 means 0b111111111100 10 means 0b111111111110 11 means 0b111111111111 0x02 contains CPM0 RAW value of the actual 12-bit sampler
52:63	RO	constant=0b000000000000

Register Name	CPM & DTS Enables and Cntl's
Mnemonic	EXP.TP.ECO_DOM.EPS.THERM.THERM_MODE_REG
Address	000000001005000F (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	Reserved field. (Access type is therm_dis_cpm_bubble_corr)
1	RW	THERM_FORCE_THRES_ACT: force tpc_therm_thres_mac clock gating off and activates clocks
2:4	RW	THERM_THRES_TRIP_ENA: therm_thres_trip compare enables 1xx: trip0 - warning x1x: trip1 - critical xx1: trip2 - fatal
5	RW	THERM_DTS_SAMPLE_ENA: 0: no dts sampling, 1: dts sampling is enabled and below counter compare match can occur.

Bits	PCB	Field Mnemonic: Description
6:9	RW	THERM_SAMPLE_PULSE_CNT: A 16 MHz sample pulse is fed into an 18-bit counter, with the therm_sample_pulse_cnt it is possible to select a high-order bit of the counter to enable a resolutions of sampling dtss between 2.5 us and 80 ms. An edge detection circuit detects the rising edge of the selected counter bit and this triggers a dts sample 0000: 16 ms 0001: 8 ms 0010: 4 ms 0011: 2 ms 0100: 1 ms 0101: 0.5 ms 0110: 250 us 0111: 125 us 1000: 62 .5us 1001: 31.3 us 1010: 15.6 us 1011: 7.8 us 1100: 3.9 us 1101: 2 us 1110: 1 us 1111: 0.5 us
10:11	RW	THERM_THRES_MODE_ENA: Forces maximum or minimum mode in threshold unit: 00: is off 11: is illegal 10: maximum mode 01: minimum mode
12	RW	DTS_TRIGGER_MODE: unused
13	RW	DTS_TRIGGER_SEL: unused
14:15	RW	THERM_MODE_UNUSED: unused
16:19	RW	THERM_DTS_READ_SEL: selects which dts result will be provided with pcb read addr_v(4): 0000: DTS 0 0001: DTS 1 0010: DTS 2 0100: DTS 4 1111: Worst Case Sensor
20:22	RW	THERM_DTS_ENABLE_L1: loop1 dts enables: 1xx: DTS 0 available x1x: DTS 1 available xx1: DTS 2 available
23	RO	constant=0b0
24	RW	THERM_DTS_ENABLE_L2: loop2 dts enables: 1: DTS 4 available
25:34	RO	constant=0b0000000000
35:37	RW	THERM_CPM_ENABLE_L1: loop1 cpm enables
38	RO	constant=0b0
39	RW	THERM_CPM_ENABLE_L2: loop2 cpm enables

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Register Name	Skitter Control Register
Mnemonic	EXP.TP.ECO_DOM.EPS.THERM.SKITTER_MODE_REG
Address	0000000010050010 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	SKITTER_HOLD_SAMPLE: forces skitter to hold current sample
1	RW	DISABLE_SKITTER_STICKINESS: if '0' accumulation mode, '1' samples new value each cycle and resets sticky value
2:3	RW	SKITTER_MODE_UNUSED1: unused
4:5	RW	SKITTER_HOLD_DBGTRIG_SEL: bit0: hold_on_trigger0 bit1: _on_trigger1
6:7	RW	SKITTER_RESET_TRIG_SEL: bit0: reset_sticky_on_trigger0 bit1: reset_sticky_on_trigger1
8:9	RW	SKITTER_SAMPLE_GUTS: selects guts to measure: 00: guts1 01: guts2 10: guts3 11: guts4
10:43	RO	constant=0b00000000000000000000000000000000
44	ROX	SKITTER_HOLD_SAMPLE_WITH_TRIGGER: forces skitter to hold current sample on dbg trigger, this has highest priority
45	ROX	SKITTER_DATA_V_LT: if '1' the data requested by a skitter force read register has finished and data is present in skitter data register in the collector macro. The data be read by any combination of V25/V26/V27 pcb reads

Register Name	Error Injection Control Register
Mnemonic	EXP.TP.ECO_DOM.EPS.THERM.INJECT_REG
Address	0000000010050011 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	THERM_INJECT_TRIP: 00: no injection 01: warning trip level injection 10: critical trip level injection 11: fatal trip level injection
2:3	RW	THERM_INJECT_MODE: 00: no injection 01: injection on the next dts sample 10: solid injection for the next dts samples till bit setting changes 11: not used

Register Name	<i>Control / Force Reset Register</i>
Mnemonic	EXP.TP.ECO_DOM.EPS.THERM.CONTROL_REG
Address	0000000010050012 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	WO_1P	Reserved field. (Access type is reset_trip_history)
1	WO_1P	Reserved field. (Access type is reset_sample_pulse_cnt)
2	WO_1P	Reserved field. (Access type is f_reset_cpm_rd)
3	WO_1P	Reserved field. (Access type is f_reset_cpm_wr)
4	WO_1P	Reserved field. (Access type is reset_sample_dts)
5	WO_1P	Reserved field. (Access type is force_sample_dts)
6	WO_1P	Reserved field. (Access type is force_sample_dts_interruptible)
7	WO_1P	Reserved field. (Access type is force_reset_thres_l1results)
8	WO_1P	Reserved field. (Access type is force_reset_thres_l2results)
9	WO_1P	Reserved field. (Access type is force_reset_thres_l3results)
10	WO_1P	Reserved field. (Access type is force_measure_volt_interruptible)
11	WO_1P	Reserved field. (Access type is force_reset_measure_volt)
12	WO_1P	Reserved field. (Access type is force_shift_sensor)

Register Name	<i>Thermal Error Status Register</i>
Mnemonic	EXP.TP.ECO_DOM.EPS.THERM.ERR_STATUS_REG
Address	0000000010050013 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field. (Access type is serial_shiftcnt_modereg_parity_err_hold)
1	ROX	Reserved field. (Access type is therm_modereg_parity_err_hold)
2	ROX	Reserved field. (Access type is skitter_modereg_parity_err_hold)
3	ROX	Reserved field. (Access type is skitter_forcereg_parity_err_hold)
4	ROX	Reserved field. (Access type is scan_init_version_reg_parity_err_hold)
5	ROX	Reserved field. (Access type is volt_modereg_parity_err_hold)
6	ROX	Reserved field. (Access type is skitter_clksrcreg_parity_err_hold)
7	ROX	Reserved field. (Access type is count_state_err_hold)
8	ROX	Reserved field. (Access type is run_state_err_hold)
9	ROX	Reserved field. (Access type is thres_therm_state_err_hold)
10	ROX	Reserved field. (Access type is thres_therm_overflow_err_hold)
11	ROX	Reserved field. (Access type is shifter_parity_err_hold)

Registers Specification

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Bits	PCB	Field Mnemonic: Description
12	ROX	Reserved field. (Access type is shifter_valid_err_hold)
13	ROX	Reserved field. (Access type is timeout_err_hold)
14	ROX	Reserved field. (Access type is f_skitter_err_hold)
15	ROX	Reserved field. (Access type is pcb_err_hold_out)
16	ROX	SERIAL_SHIFTCNT_MODEREG_PARITY_ERR_MASK: serial shift count parity error mask
17	ROX	THERM_MODEREG_PARITY_ERR_MASK: therm mode reg parity error mask
18	ROX	SKITTER_MODEREG_PARITY_ERR_MASK: skitter mode register parity error mask
19	ROX	SKITTER_FORCEREG_PARITY_ERR_MASK: skitter force register parity error mask
20	ROX	SCAN_INIT_VERSION_REG_PARITY_ERR_MASK: scan init version register parity error mask
21	ROX	VOLT_MODEREG_PARITY_ERR_MASK: volt mode reg parity error mask
22	RO	constant=0b0
23	ROX	COUNT_STATE_ERR_MASK: count state machine error mask
24	ROX	RUN_STATE_ERR_MASK: run state machine error mask
25	ROX	THRES_STATE_ERR_MASK: thres state machine error mask
26	ROX	OVERFLOW_ERR_MASK: DTS calibration calculation overflow error mask
27	ROX	SHIFTER_PARITY_ERR_MASK: Shifter parity error mask
28	ROX	SHIFTER_VALID_ERR_MASK: Shifter valid error mask
29	ROX	TIMEOUT_ERR_MASK: Timeout error mask
30	ROX	F_SKITTER_READ_ERR_MASK: force skitter read one hot error mask
31	ROX	PCB_ERR_MASK: pervasive control bus error mask
32:39	RO	constant=0b00000000
40:43	ROX	Reserved field. (Access type is count_state_lt)
44:46	ROX	Reserved field. (Access type is run_state_lt)
47	ROX	Reserved field. (Access type is shift_dts_lt)
48	ROX	Reserved field. (Access type is shift_volt_lt)
49:50	ROX	Reserved field. (Access type is read_state_lt)
51:54	ROX	Reserved field. (Access type is write_state_lt)
55	ROX	Reserved field. (Access type is sample_dts_lt)
56	ROX	Reserved field. (Access type is measure_volt_lt)
57	ROX	Reserved field. (Access type is read_cpm_lt)
58	ROX	Reserved field. (Access type is write_cpm_lt)
59	ROX	Reserved field. (Access type is unused)
60:63	RO	constant=0b0000



Register Name	<i>Skitter Force Read Register</i>	
Mnemonic	EXP.TP.ECO_DOM.EPS.THERM.SKITTER_FORCE_REG	
Address	0000000010050014 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	RW	F_SKITTER_READ: Forces the read of that particular skitter

Register Name	<i>Skitter Clock Src Control Register</i>	
Mnemonic	EXP.TP.ECO_DOM.EPS.THERM.SKITTER_CLKSRC_REG	
Address	0000000010050016 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RW	SKITTER0_CLKSRC: selects clock to measure: 000: local mesh clock 001: external pin skitter_c1_1_in 010: local d1clk only if d_mode = 1 011: external pin skitter_c1_2_in 100: local lclk only if d_mode = 1 101: external pin skitter_c1_3_in 110: unused 111: external pin skitter_c1_4_in
3:35	RO	constant=0b00000000000000000000000000000000

Register Name	<i>Skitter Data Register Read Bit0:63</i>	
Mnemonic	EXP.TP.ECO_DOM.EPS.THERM.SKITTER_DATA0	
Address	0000000010050019 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:63	ROX	

Register Name	<i>Skitter Data Register Read Bit32:95</i>	
Mnemonic	EXP.TP.ECO_DOM.EPS.THERM.SKITTER_DATA1	
Address	000000001005001A (PCB)	
Attributes		
Description		

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Bits	PCB	Field Mnemonic: Description
0:63	ROX	

Register Name	<i>Skitter Data Register Read Bit64:127</i>
Mnemonic	EXP.TP.ECO_DOM.EPS.THERM.SKITTER_DATA2
Address	000000001005001B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:63	ROX	

Register Name	<i>Timestamp Counter Read</i>
Mnemonic	EXP.TP.ECO_DOM.EPS.THERM.TIMESTAMP_COUNTER_READ
Address	000000001005001C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:43	ROX	TIMESTAMP_COUNTER_VALUE: Time stamp counter value during DTS trace mode.
44	ROX	TIMESTAMP_COUNTER_OVERFLOW_ERR: Over flow error bit of the time stamp counter value during DTS trace mode.

6. POWER8: EX Chiplet PCB Slave

The POWER8 Processor registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.ASSIST_INTERRUPT_REG	0x00000000110F0011	983
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.ATOMIC_LOCK_REG	0x00000000110F03FF	1031
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.ATTN_INTERRUPT_REG	0x00000000110F001A	986
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.CLK_ADJ_REG	0x00000000110F0015	985
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.CLK_ADJ_SET	0x00000000110F0016	985
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.ERROR_REG	0x00000000110F001F	987
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.GP3_REG	0x00000000110F0012	660
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.HANG_PULSE_0_REG	0x00000000110F0020	988
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.HANG_PULSE_1_REG	0x00000000110F0021	989
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.HANG_PULSE_2_REG	0x00000000110F0022	989
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.HANG_PULSE_3_REG	0x00000000110F0023	989
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.HANG_PULSE_4_REG	0x00000000110F0024	989
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.HANG_PULSE_5_REG	0x00000000110F0025	990
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.HANG_PULSE_6_REG	0x00000000110F0026	990
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.HEARTBEAT_REG	0x00000000110F0018	985
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.MULTICAST_GROUP_1	0x00000000110F0001	982
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.MULTICAST_GROUP_2	0x00000000110F0002	982
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.MULTICAST_GROUP_3	0x00000000110F0003	982
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.MULTICAST_GROUP_4	0x00000000110F0004	983
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.PLL_LOCK_REG	0x00000000110F0019	986
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.PRE_COUNTER_REG	0x00000000110F0028	990
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.PRIMARY_ADDRESS_REG	0x00000000110F0000	982
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.PROTECT_MODE_REG	0x00000000110F03FE	1030
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.RECOV_INTERRUPT_REG	0x00000000110F001B	986
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.SLAVE_CONFIG_REG	0x00000000110F001E	987
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.TIMEOUT_REG	0x00000000110F0010	983
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.VITAL_SCAN_OUT	0x00000000110F0017	985
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.XSTOP_INTERRUPT_REG	0x00000000110F001C	986
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.COREPFPDDLY_REG	0x00000000110F012D	1006
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.COREPFPUDLY_REG	0x00000000110F012C	1006
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.COREPFVRET_REG	0x00000000110F0130	1007
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.DPLL_CPM_PARM_REG	0x00000000110F0152	1009
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.ECOPFPDDLY_REG	0x00000000110F014D	1007
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.ECOPFPUDLY_REG	0x00000000110F014C	1007
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.ECOPFVRET_REG	0x00000000110F0150	1008
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.FREQ_CTRL_REG	0x00000000110F0151	1008
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.IDLEFSMGOTOCMD_REG	0x00000000110F0114	1005
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBSPM_MODE_REG	0x00000000110F0156	1016
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_DPLL_STATUS_REG	0x00000000110F0161	1022
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR1_REG	0x00000000110F0170	1029
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR2_REG	0x00000000110F0171	1030



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Mnemonic	Address	Page
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_CONTROL_STATUS_REG	0x00000000110F0154	1010
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_PFETSTR_SENSE_REG	0x00000000110F0157	1017
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VALUE_SETTING_REG	0x00000000110F0155	1014
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG0	0x00000000110F0162	1023
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG1	0x00000000110F0163	1023
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_CONTROL_REG	0x00000000110F0168	1028
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_STATUS_REG	0x00000000110F0169	1028
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_OCC_HEARTBEAT_REG	0x00000000110F0164	1025
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_PMC_VF_CTRL_REG	0x00000000110F015A	1020
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_BOUNDS_REG	0x00000000110F015D	1021
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_CONTROL_REG	0x00000000110F0159	1019
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_IDLE_CONTROL_REG	0x00000000110F0158	1018
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_STATUS_REG	0x00000000110F0153	1009
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_INDEX_BOUND_REG	0x00000000110F015C	1020
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_STEP_TARGET_REG	0x00000000110F0160	1022
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_CTRL_REG	0x00000000110F015E	1021
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_REG	0x00000000110F015F	1021
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG0	0x00000000110F0165	1025
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG1	0x00000000110F0166	1026
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_STATUS_REG	0x00000000110F0167	1027
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_UNDERVOLTING_REG	0x00000000110F015B	1020
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PFSENSE_REG	0x00000000110F0107	996
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PFVSCNTLSTAT_REG	0x00000000110F010E	1001
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PFVDDCNTLSTAT_REG	0x00000000110F0106	995
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PMERRMASK_REG	0x00000000110F010A	999
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PMERRSUM_REG	0x00000000110F0108	997
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PMERR_REG	0x00000000110F0109	997
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PMGPO_REG	0x00000000110F0100	991
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PMGPI_REG	0x00000000110F0103	993
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PMSPCWKUPFSP_REG	0x00000000110F010B	1000
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PMSPCWKUPOCC_REG	0x00000000110F010C	1000
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PMSPCWKUPPHYP_REG	0x00000000110F010D	1001
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PMSTATEHISTFSP_REG	0x00000000110F0111	1003
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PMSTATEHISTOCC_REG	0x00000000110F0112	1004



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EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPERF_REG	0x00000000110F0113	1004
EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPHYP_REG	0x00000000110F0110	1003
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.ASSIST_INTERRUPT_REG	0x00000000120F0011	1032
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.ATOMIC_LOCK_REG	0x00000000120F03FF	1081
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.ATTN_INTERRUPT_REG	0x00000000120F001A	1035
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.CLK_ADJ_REG	0x00000000120F0015	1034
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.CLK_ADJ_SET	0x00000000120F0016	1034
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.ERROR_REG	0x00000000120F001F	1036
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.GP3_REG	0x00000000120F0012	661
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.HANG_PULSE_0_REG	0x00000000120F0020	1037
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.HANG_PULSE_1_REG	0x00000000120F0021	1038
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.HANG_PULSE_2_REG	0x00000000120F0022	1038
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.HANG_PULSE_3_REG	0x00000000120F0023	1038
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.HANG_PULSE_4_REG	0x00000000120F0024	1038
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.HANG_PULSE_5_REG	0x00000000120F0025	1039
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.HANG_PULSE_6_REG	0x00000000120F0026	1039
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.HEARTBEAT_REG	0x00000000120F0018	1034
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.MULTICAST_GROUP_1	0x00000000120F0001	1031
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.MULTICAST_GROUP_2	0x00000000120F0002	1031
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.MULTICAST_GROUP_3	0x00000000120F0003	1032
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.MULTICAST_GROUP_4	0x00000000120F0004	1032
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.PLL_LOCK_REG	0x00000000120F0019	1035
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.PRE_COUNTER_REG	0x00000000120F0028	1039
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.PRIMARY_ADDRESS_REG	0x00000000120F0000	1031
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.PROTECT_MODE_REG	0x00000000120F03FE	1080
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.RECOV_INTERRUPT_REG	0x00000000120F001B	1035
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.SLAVE_CONFIG_REG	0x00000000120F001E	1036
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.TIMEOUT_REG	0x00000000120F0010	1032
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.VITAL_SCAN_OUT	0x00000000120F0017	1034
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.XSTOP_INTERRUPT_REG	0x00000000120F001C	1035
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.COREPFPDDLY_REG	0x00000000120F012D	1055
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.COREPFPUDLY_REG	0x00000000120F012C	1055
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.COREPFVRET_REG	0x00000000120F0130	1056
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.DPLL_CPM_PARM_REG	0x00000000120F0152	1058
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.ECOPFPDDLY_REG	0x00000000120F014D	1056
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.ECOPFPUDLY_REG	0x00000000120F014C	1056
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.ECOPFVRET_REG	0x00000000120F0150	1057
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.FREQ_CTRL_REG	0x00000000120F0151	1057
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.IDLEFSMGOTOCMD_REG	0x00000000120F0114	1054
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBSPM_MODE_REG	0x00000000120F0156	1065
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_DPLL_STATUS_REG	0x00000000120F0161	1071
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR1_REG	0x00000000120F0170	1079
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR2_REG	0x00000000120F0171	1080
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_CONTROL_STATUS_REG	0x00000000120F0154	1059
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_PFETSTR_SENSE_REG	0x00000000120F0157	1066



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Mnemonic	Address	Page
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VALUE_SETTING_REG	0x00000000120F0155	1063
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG0	0x00000000120F0162	1072
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG1	0x00000000120F0163	1072
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_CONTROL_REG	0x00000000120F0168	1078
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_STATUS_REG	0x00000000120F0169	1078
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_OCC_HEARTBEAT_REG	0x00000000120F0164	1074
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_PMC_VF_CTRL_REG	0x00000000120F015A	1069
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_BOUNDS_REG	0x00000000120F015D	1070
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_CONTROL_REG	0x00000000120F0159	1068
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_IDLE_CONTROL_REG	0x00000000120F0158	1067
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_STATUS_REG	0x00000000120F0153	1058
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_INDEX_BOUND_REG	0x00000000120F015C	1069
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_STEP_TARGET_REG	0x00000000120F0160	1071
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_CTRL_REG	0x00000000120F015E	1070
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_REG	0x00000000120F015F	1070
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG0	0x00000000120F0165	1074
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG1	0x00000000120F0166	1075
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_STATUS_REG	0x00000000120F0167	1076
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_UNDERVOLTING_REG	0x00000000120F015B	1069
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PFSENSE_REG	0x00000000120F0107	1045
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PFVSCNTLSTAT_REG	0x00000000120F010E	1050
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PFVDDCNTLSTAT_REG	0x00000000120F0106	1044
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PMERRMASK_REG	0x00000000120F010A	1048
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PMERRSUM_REG	0x00000000120F0108	1046
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PMERR_REG	0x00000000120F0109	1046
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PMGPO_REG	0x00000000120F0100	1040
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PMGPI_REG	0x00000000120F0103	1042
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PMSPCWKUPFSP_REG	0x00000000120F010B	1049
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PMSPCWKUPOCC_REG	0x00000000120F010C	1049
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PMSPCWKUPPHYP_REG	0x00000000120F010D	1050
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PMSTATEHISTFSP_REG	0x00000000120F0111	1052
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PMSTATEHISTOCC_REG	0x00000000120F0112	1053
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPERF_REG	0x00000000120F0113	1053
EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPHYP_REG	0x00000000120F0110	1052
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.ASSIST_INTERRUPT_REG	0x00000000130F0011	1082
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.ATOMIC_LOCK_REG	0x00000000130F03FF	1130



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EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.ATTN_INTERRUPT_REG	0x00000000130F001A	1085
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.CLK_ADJ_REG	0x00000000130F0015	1084
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.CLK_ADJ_SET	0x00000000130F0016	1084
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.ERROR_REG	0x00000000130F001F	1086
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.GP3_REG	0x00000000130F0012	662
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.HANG_PULSE_0_REG	0x00000000130F0020	1087
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.HANG_PULSE_1_REG	0x00000000130F0021	1088
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.HANG_PULSE_2_REG	0x00000000130F0022	1088
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.HANG_PULSE_3_REG	0x00000000130F0023	1088
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.HANG_PULSE_4_REG	0x00000000130F0024	1088
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.HANG_PULSE_5_REG	0x00000000130F0025	1089
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.HANG_PULSE_6_REG	0x00000000130F0026	1089
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.HEARTBEAT_REG	0x00000000130F0018	1084
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.MULTICAST_GROUP_1	0x00000000130F0001	1081
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.MULTICAST_GROUP_2	0x00000000130F0002	1081
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.MULTICAST_GROUP_3	0x00000000130F0003	1082
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.MULTICAST_GROUP_4	0x00000000130F0004	1082
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.PLL_LOCK_REG	0x00000000130F0019	1085
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.PRE_COUNTER_REG	0x00000000130F0028	1089
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.PRIMARY_ADDRESS_REG	0x00000000130F0000	1081
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.PROTECT_MODE_REG	0x00000000130F03FE	1129
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.RECOV_INTERRUPT_REG	0x00000000130F001B	1085
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.SLAVE_CONFIG_REG	0x00000000130F001E	1086
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.TIMEOUT_REG	0x00000000130F0010	1082
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.VITAL_SCAN_OUT	0x00000000130F0017	1084
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.XSTOP_INTERRUPT_REG	0x00000000130F001C	1085
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.COREPFPDDL_REG	0x00000000130F012D	1105
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.COREPFPUDLY_REG	0x00000000130F012C	1105
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.COREPFPVRET_REG	0x00000000130F0130	1106
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.DPLL_CPM_PARM_REG	0x00000000130F0152	1108
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.ECOPFPDDL_REG	0x00000000130F014D	1106
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.ECOPFPUDLY_REG	0x00000000130F014C	1106
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.ECOPFVRET_REG	0x00000000130F0150	1107
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.FREQ_CTRL_REG	0x00000000130F0151	1107
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.IDLEFSMGOTOCMD_REG	0x00000000130F0114	1104
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBSPM_MODE_REG	0x00000000130F0156	1115
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_DPLL_STATUS_REG	0x00000000130F0161	1121
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR1_REG	0x00000000130F0170	1128
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR2_REG	0x00000000130F0171	1129
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_CONTROL_STATUS_REG	0x00000000130F0154	1109
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_PFETSTR_SENSE_REG	0x00000000130F0157	1116
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VALUE_SETTING_REG	0x00000000130F0155	1113
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG0	0x00000000130F0162	1122
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG1	0x00000000130F0163	1122



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EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUEN CY_TARGET_CONTROL_REG	0x00000000130F0168	1127
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUEN CY_TARGET_STATUS_REG	0x00000000130F0169	1127
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_OCC_HEARTBEAT_REG	0x00000000130F0164	1124
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_PMC_VF_CTRL_REG	0x00000000130F015A	1119
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_ BOUNDS_REG	0x00000000130F015D	1120
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_ CONTROL_REG	0x00000000130F0159	1118
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_I DLE_CONTROL_REG	0x00000000130F0158	1117
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_ STATUS_REG	0x00000000130F0153	1108
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_INDEX_BOUND_ REG	0x00000000130F015C	1119
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_STEP_TARGET_ REG	0x00000000130F0160	1121
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_CTRL_R EG	0x00000000130F015E	1120
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_REG	0x00000000130F015F	1120
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CON TROL_REG0	0x00000000130F0165	1124
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CON TROL_REG1	0x00000000130F0166	1125
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_STA TUS_REG	0x00000000130F0167	1126
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_UNDERVOLTING_REG	0x00000000130F015B	1119
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PFSENSE_REG	0x00000000130F0107	1095
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PFVCSNTLSTAT_REG	0x00000000130F010E	1100
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PFVDDCNTLSTAT_REG	0x00000000130F0106	1094
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PMERRMASK_REG	0x00000000130F010A	1098
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PMERRSUM_REG	0x00000000130F0108	1096
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PMERR_REG	0x00000000130F0109	1096
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PMGPO_REG	0x00000000130F0100	1090
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PMGPI_REG	0x00000000130F0103	1092
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PMSPCWKUPFSP_REG	0x00000000130F010B	1099
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PMSPCWKUPOCC_REG	0x00000000130F010C	1099
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PMSPCWKUPPHYP_REG	0x00000000130F010D	1100
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PMSTATEHISTFSP_REG	0x00000000130F0111	1102
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PMSTATEHISTOCC_REG	0x00000000130F0112	1103
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPERF_REG	0x00000000130F0113	1103
EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPHYP_REG	0x00000000130F0110	1102
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.ASSIST_INTERRUPT_REG	0x00000000140F0011	1131
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.ATOMIC_LOCK_REG	0x00000000140F03FF	1180
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.ATTN_INTERRUPT_REG	0x00000000140F001A	1134
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.CLK_ADJ_REG	0x00000000140F0015	1133
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.CLK_ADJ_SET	0x00000000140F0016	1133
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.ERROR_REG	0x00000000140F001F	1135
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.GP3_REG	0x00000000140F0012	663



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EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.HANG_PULSE_0_REG	0x00000000140F0020	1136
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.HANG_PULSE_1_REG	0x00000000140F0021	1137
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.HANG_PULSE_2_REG	0x00000000140F0022	1137
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.HANG_PULSE_3_REG	0x00000000140F0023	1137
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.HANG_PULSE_4_REG	0x00000000140F0024	1137
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.HANG_PULSE_5_REG	0x00000000140F0025	1138
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.HANG_PULSE_6_REG	0x00000000140F0026	1138
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.HEARTBEAT_REG	0x00000000140F0018	1133
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.MULTICAST_GROUP_1	0x00000000140F0001	1130
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.MULTICAST_GROUP_2	0x00000000140F0002	1130
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.MULTICAST_GROUP_3	0x00000000140F0003	1131
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.MULTICAST_GROUP_4	0x00000000140F0004	1131
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.PLL_LOCK_REG	0x00000000140F0019	1134
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.PRE_COUNTER_REG	0x00000000140F0028	1138
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.PRIMARY_ADDRESS_REG	0x00000000140F0000	1130
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.PROTECT_MODE_REG	0x00000000140F03FE	1179
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.RECOV_INTERRUPT_REG	0x00000000140F001B	1134
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.SLAVE_CONFIG_REG	0x00000000140F001E	1135
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.TIMEOUT_REG	0x00000000140F0010	1131
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.VITAL_SCAN_OUT	0x00000000140F0017	1133
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.XSTOP_INTERRUPT_REG	0x00000000140F001C	1134
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.COREPFPPDLY_REG	0x00000000140F012D	1154
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.COREPFPUPLY_REG	0x00000000140F012C	1154
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.COREPFVRET_REG	0x00000000140F0130	1155
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.DPLL_CPM_PARM_REG	0x00000000140F0152	1157
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.ECOPFPDLY_REG	0x00000000140F014D	1155
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.ECOPFPUDLY_REG	0x00000000140F014C	1155
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.ECOPFVRET_REG	0x00000000140F0150	1156
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.FREQ_CTRL_REG	0x00000000140F0151	1156
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.IDLEFSMGOTOCMD_REG	0x00000000140F0114	1153
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBSPM_MODE_REG	0x00000000140F0156	1164
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_DPLL_STATUS_REG	0x00000000140F0161	1170
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR1_REG	0x00000000140F0170	1178
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR2_REG	0x00000000140F0171	1179
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_CONTROL_STATUS_REG	0x00000000140F0154	1158
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_PFETSTR_SENSE_REG	0x00000000140F0157	1165
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VALUE_SETTING_REG	0x00000000140F0155	1162
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG0	0x00000000140F0162	1171
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG1	0x00000000140F0163	1171
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_CONTROL_REG	0x00000000140F0168	1177
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_STATUS_REG	0x00000000140F0169	1177
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_OCC_HEARTBEAT_REG	0x00000000140F0164	1173



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EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_PMC_VF_CTRL_REG	0x00000000140F015A	1168
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_BOUNDS_REG	0x00000000140F015D	1169
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_CONTROL_REG	0x00000000140F0159	1167
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_IDLE_CONTROL_REG	0x00000000140F0158	1166
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_STATUS_REG	0x00000000140F0153	1157
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_INDEX_BOUND_REG	0x00000000140F015C	1168
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_STEP_TARGET_REG	0x00000000140F0160	1170
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_CTRL_REG	0x00000000140F015E	1169
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_REG	0x00000000140F015F	1169
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG0	0x00000000140F0165	1173
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG1	0x00000000140F0166	1174
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_STATUS_REG	0x00000000140F0167	1175
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_UNDERVOLTING_REG	0x00000000140F015B	1168
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PFSENSE_REG	0x00000000140F0107	1144
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PFVCSCTLSTAT_REG	0x00000000140F010E	1149
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PFVDDCNTLSTAT_REG	0x00000000140F0106	1143
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PMERRMASK_REG	0x00000000140F010A	1147
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PMERRSUM_REG	0x00000000140F0108	1145
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PMERR_REG	0x00000000140F0109	1145
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PMGPO_REG	0x00000000140F0100	1139
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PMGPI_REG	0x00000000140F0103	1141
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PMSPCWKUPFSP_REG	0x00000000140F010B	1148
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PMSPCWKUPOCC_REG	0x00000000140F010C	1148
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PMSPCWKUPPHYP_REG	0x00000000140F010D	1149
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PMSTATEHISTFSP_REG	0x00000000140F0111	1151
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PMSTATEHISTOCC_REG	0x00000000140F0112	1152
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPERF_REG	0x00000000140F0113	1152
EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPHYP_REG	0x00000000140F0110	1151
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.ASSIST_INTERRUPT_REG	0x00000000150F0011	1181
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.ATOMIC_LOCK_REG	0x00000000150F03FF	1230
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.ATTN_INTERRUPT_REG	0x00000000150F001A	1184
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.CLK_ADJ_REG	0x00000000150F0015	1183
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.CLK_ADJ_SET	0x00000000150F0016	1183
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.ERROR_REG	0x00000000150F001F	1185
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.GP3_REG	0x00000000150F0012	664
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.HANG_PULSE_0_REG	0x00000000150F0020	1186
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.HANG_PULSE_1_REG	0x00000000150F0021	1187
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.HANG_PULSE_2_REG	0x00000000150F0022	1187
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.HANG_PULSE_3_REG	0x00000000150F0023	1187
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.HANG_PULSE_4_REG	0x00000000150F0024	1187



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EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.HANG_PULSE_5_REG	0x00000000150F0025	1188
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.HANG_PULSE_6_REG	0x00000000150F0026	1188
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.HEARTBEAT_REG	0x00000000150F0018	1183
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.MULTICAST_GROUP_1	0x00000000150F0001	1180
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.MULTICAST_GROUP_2	0x00000000150F0002	1180
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.MULTICAST_GROUP_3	0x00000000150F0003	1181
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.MULTICAST_GROUP_4	0x00000000150F0004	1181
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.PLL_LOCK_REG	0x00000000150F0019	1184
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.PRE_COUNTER_REG	0x00000000150F0028	1188
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.PRIMARY_ADDRESS_REG	0x00000000150F0000	1180
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.PROTECT_MODE_REG	0x00000000150F03FE	1229
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.RECOV_INTERRUPT_REG	0x00000000150F001B	1184
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.SLAVE_CONFIG_REG	0x00000000150F001E	1185
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.TIMEOUT_REG	0x00000000150F0010	1181
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.VITAL_SCAN_OUT	0x00000000150F0017	1183
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.XSTOP_INTERRUPT_REG	0x00000000150F001C	1184
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.COREPFPDDLY_REG	0x00000000150F012D	1204
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.COREPFPUDLY_REG	0x00000000150F012C	1204
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.COREPFVRET_REG	0x00000000150F0130	1205
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.DPLL_CPM_PARM_REG	0x00000000150F0152	1207
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.ECOPFPDDLY_REG	0x00000000150F014D	1205
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.ECOPFPUDLY_REG	0x00000000150F014C	1205
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.ECOPFVRET_REG	0x00000000150F0150	1206
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.FREQ_CTRL_REG	0x00000000150F0151	1206
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.IDLEFSMGOTOCMD_REG	0x00000000150F0114	1203
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBSPM_MODE_REG	0x00000000150F0156	1214
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_DPLL_STATUS_REG	0x00000000150F0161	1220
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR1_REG	0x00000000150F0170	1228
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR2_REG	0x00000000150F0171	1229
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_CONTROL_STATUS_REG	0x00000000150F0154	1208
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_PFETSTR_SENSE_REG	0x00000000150F0157	1215
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VALUE_SETTING_REG	0x00000000150F0155	1212
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG0	0x00000000150F0162	1221
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG1	0x00000000150F0163	1221
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_CONTROL_REG	0x00000000150F0168	1227
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_STATUS_REG	0x00000000150F0169	1227
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_OCC_HEARTBEAT_REG	0x00000000150F0164	1223
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_PMC_VF_CTRL_REG	0x00000000150F015A	1218
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_BOUNDS_REG	0x00000000150F015D	1219
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_CONTROL_REG	0x00000000150F0159	1217



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EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_IDLE_CONTROL_REG	0x00000000150F0158	1216
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_STATUS_REG	0x00000000150F0153	1207
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_INDEX_BOUND_REG	0x00000000150F015C	1218
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_STEP_TARGET_REG	0x00000000150F0160	1220
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_CTRL_REG	0x00000000150F015E	1219
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_REG	0x00000000150F015F	1219
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG0	0x00000000150F0165	1223
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG1	0x00000000150F0166	1224
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_STATUS_REG	0x00000000150F0167	1225
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_UNDERVOLTING_REG	0x00000000150F015B	1218
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PFSENSE_REG	0x00000000150F0107	1194
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PFVCS_CNTL_STAT_REG	0x00000000150F010E	1199
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PFVDD_CNTL_STAT_REG	0x00000000150F0106	1193
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PMERRMASK_REG	0x00000000150F010A	1197
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PMERRSUM_REG	0x00000000150F0108	1195
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PMERR_REG	0x00000000150F0109	1195
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PMGPO_REG	0x00000000150F0100	1189
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PMGPI_REG	0x00000000150F0103	1191
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PMSPCWKUPFSP_REG	0x00000000150F010B	1198
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PMSPCWKUPOCC_REG	0x00000000150F010C	1198
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PMSPCWKUPPHYP_REG	0x00000000150F010D	1199
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PMSTATEHISTFSP_REG	0x00000000150F0111	1201
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PMSTATEHISTOCC_REG	0x00000000150F0112	1202
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPERF_REG	0x00000000150F0113	1202
EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPHYP_REG	0x00000000150F0110	1201
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.ASSIST_INTERRUPT_REG	0x00000000160F0011	1231
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.ATOMIC_LOCK_REG	0x00000000160F03FF	1280
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.ATTN_INTERRUPT_REG	0x00000000160F001A	1234
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.CLK_ADJ_REG	0x00000000160F0015	1233
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.CLK_ADJ_SET	0x00000000160F0016	1233
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.ERROR_REG	0x00000000160F001F	1235
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.GP3_REG	0x00000000160F0012	664
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.HANG_PULSE_0_REG	0x00000000160F0020	1236
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.HANG_PULSE_1_REG	0x00000000160F0021	1237
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.HANG_PULSE_2_REG	0x00000000160F0022	1237
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.HANG_PULSE_3_REG	0x00000000160F0023	1237
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.HANG_PULSE_4_REG	0x00000000160F0024	1237
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.HANG_PULSE_5_REG	0x00000000160F0025	1238
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.HANG_PULSE_6_REG	0x00000000160F0026	1238
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.HEARTBEAT_REG	0x00000000160F0018	1233
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.MULTICAST_GROUP_1	0x00000000160F0001	1230



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EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.MULTICAST_GROUP_2	0x00000000160F0002	1230
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.MULTICAST_GROUP_3	0x00000000160F0003	1231
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.MULTICAST_GROUP_4	0x00000000160F0004	1231
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.PLL_LOCK_REG	0x00000000160F0019	1234
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.PRE_COUNTER_REG	0x00000000160F0028	1238
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.PRIMARY_ADDRESS_REG	0x00000000160F0000	1230
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.PROTECT_MODE_REG	0x00000000160F03FE	1279
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.RECOV_INTERRUPT_REG	0x00000000160F001B	1234
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.SLAVE_CONFIG_REG	0x00000000160F001E	1235
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.TIMEOUT_REG	0x00000000160F0010	1231
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.VITAL_SCAN_OUT	0x00000000160F0017	1233
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.XSTOP_INTERRUPT_REG	0x00000000160F001C	1234
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.COREPFPDDLY_REG	0x00000000160F012D	1254
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.COREPFPUDLY_REG	0x00000000160F012C	1254
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.COREPFVRET_REG	0x00000000160F0130	1255
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.DPLL_CPM_PARM_REG	0x00000000160F0152	1257
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.ECOPFPDDLY_REG	0x00000000160F014D	1255
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.ECOPFPUDLY_REG	0x00000000160F014C	1255
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.ECOPFVRET_REG	0x00000000160F0150	1256
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.FREQ_CTRL_REG	0x00000000160F0151	1256
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.IDLEFSMGOTOCMD_REG	0x00000000160F0114	1253
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBSPM_MODE_REG	0x00000000160F0156	1264
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_DPLL_STATUS_REG	0x00000000160F0161	1270
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR1_REG	0x00000000160F0170	1278
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR2_REG	0x00000000160F0171	1279
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_CONTROL_STATUS_REG	0x00000000160F0154	1258
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_PFETSTR_SENSE_REG	0x00000000160F0157	1265
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VALUE_SETTING_REG	0x00000000160F0155	1262
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG0	0x00000000160F0162	1271
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG1	0x00000000160F0163	1271
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_CONTROL_REG	0x00000000160F0168	1277
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_STATUS_REG	0x00000000160F0169	1277
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_OCC_HEARTBEAT_REG	0x00000000160F0164	1273
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_PMC_VF_CTRL_REG	0x00000000160F015A	1268
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_BOUNDS_REG	0x00000000160F015D	1269
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_CONTROL_REG	0x00000000160F0159	1267
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_IDLE_CONTROL_REG	0x00000000160F0158	1266
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_STATUS_REG	0x00000000160F0153	1257



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EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_INDEX_BOUND_REG	0x00000000160F015C	1268
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_STEP_TARGET_REG	0x00000000160F0160	1270
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_CTRL_REG	0x00000000160F015E	1269
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_REG	0x00000000160F015F	1269
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG0	0x00000000160F0165	1273
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG1	0x00000000160F0166	1274
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_STATUS_REG	0x00000000160F0167	1275
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_UNDERVOLTING_REG	0x00000000160F015B	1268
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PFSENSE_REG	0x00000000160F0107	1244
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PFVSCNTLSTAT_REG	0x00000000160F010E	1249
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PFVDDCNTLSTAT_REG	0x00000000160F0106	1243
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PMERRMASK_REG	0x00000000160F010A	1247
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PMERRSUM_REG	0x00000000160F0108	1245
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PMERR_REG	0x00000000160F0109	1245
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PMGPO_REG	0x00000000160F0100	1239
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PMGPI_REG	0x00000000160F0103	1241
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PMSPCWKUPFSP_REG	0x00000000160F010B	1248
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PMSPCWKUPOCC_REG	0x00000000160F010C	1248
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PMSPCWKUPPHYP_REG	0x00000000160F010D	1249
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PMSTATEHISTFSP_REG	0x00000000160F0111	1251
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PMSTATEHISTOCC_REG	0x00000000160F0112	1252
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPERF_REG	0x00000000160F0113	1252
EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPHYP_REG	0x00000000160F0110	1251
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.ASSIST_INTERRUPT_REG	0x00000000190F0011	1281
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.ATOMIC_LOCK_REG	0x00000000190F03FF	1329
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.ATTN_INTERRUPT_REG	0x00000000190F001A	1284
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.CLK_ADJ_REG	0x00000000190F0015	1283
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.CLK_ADJ_SET	0x00000000190F0016	1283
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.ERROR_REG	0x00000000190F001F	1285
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.GP3_REG	0x00000000190F0012	665
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.HANG_PULSE_0_REG	0x00000000190F0020	1286
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.HANG_PULSE_1_REG	0x00000000190F0021	1287
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.HANG_PULSE_2_REG	0x00000000190F0022	1287
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.HANG_PULSE_3_REG	0x00000000190F0023	1287
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.HANG_PULSE_4_REG	0x00000000190F0024	1287
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.HANG_PULSE_5_REG	0x00000000190F0025	1288
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.HANG_PULSE_6_REG	0x00000000190F0026	1288
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.HEARTBEAT_REG	0x00000000190F0018	1283
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.MULTICAST_GROUP_1	0x00000000190F0001	1280
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.MULTICAST_GROUP_2	0x00000000190F0002	1280
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.MULTICAST_GROUP_3	0x00000000190F0003	1281
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.MULTICAST_GROUP_4	0x00000000190F0004	1281
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.PLL_LOCK_REG	0x00000000190F0019	1284



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EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.PRE_COUNTER_REG	0x00000000190F0028	1288
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.PRIMARY_ADDRESS_REG	0x00000000190F0000	1280
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.PROTECT_MODE_REG	0x00000000190F03FE	1328
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.RECOV_INTERRUPT_REG	0x00000000190F001B	1284
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.SLAVE_CONFIG_REG	0x00000000190F001E	1285
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.TIMEOUT_REG	0x00000000190F0010	1281
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.VITAL_SCAN_OUT	0x00000000190F0017	1283
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.XSTOP_INTERRUPT_REG	0x00000000190F001C	1284
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.COREPFPDDLY_REG	0x00000000190F012D	1304
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.COREPFPUDLY_REG	0x00000000190F012C	1304
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.COREPFVRET_REG	0x00000000190F0130	1305
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.DPLL_CPM_PARM_REG	0x00000000190F0152	1307
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.ECOPFPDDLY_REG	0x00000000190F014D	1305
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.ECOPFPUDLY_REG	0x00000000190F014C	1305
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.ECOPFVRET_REG	0x00000000190F0150	1306
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.FREQ_CTRL_REG	0x00000000190F0151	1306
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.IDLEFSMGOTOCMD_REG	0x00000000190F0114	1303
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBSPM_MODE_REG	0x00000000190F0156	1314
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_DPLL_STATUS_REG	0x00000000190F0161	1320
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR1_REG	0x00000000190F0170	1327
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR2_REG	0x00000000190F0171	1328
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_CONTROL_STATUS_REG	0x00000000190F0154	1308
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_PFETSTR_SENSE_REG	0x00000000190F0157	1315
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VALUE_SETTING_REG	0x00000000190F0155	1312
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG0	0x00000000190F0162	1321
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG1	0x00000000190F0163	1321
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_CONTROL_REG	0x00000000190F0168	1326
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_STATUS_REG	0x00000000190F0169	1326
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_OCC_HEARTBEAT_REG	0x00000000190F0164	1323
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_PMC_VF_CTRL_REG	0x00000000190F015A	1318
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_BOUNDS_REG	0x00000000190F015D	1319
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_CONTROL_REG	0x00000000190F0159	1317
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_IDLE_CONTROL_REG	0x00000000190F0158	1316
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_STATUS_REG	0x00000000190F0153	1307
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_INDEX_BOUND_REG	0x00000000190F015C	1318
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_STEP_TARGET_REG	0x00000000190F0160	1320
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_CTRL_REG	0x00000000190F015E	1319



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EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_REG	0x00000000190F015F	1319
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CON TROL_REG0	0x00000000190F0165	1323
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CON TROL_REG1	0x00000000190F0166	1324
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_STA TUS_REG	0x00000000190F0167	1325
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_UNDERVOLTING_REG	0x00000000190F015B	1318
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PFSENSE_REG	0x00000000190F0107	1294
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PFVCSCTLSTAT_REG	0x00000000190F010E	1299
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PFVDDCNTLSTAT_REG	0x00000000190F0106	1293
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PMERRMASK_REG	0x00000000190F010A	1297
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PMERRSUM_REG	0x00000000190F0108	1295
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PMERR_REG	0x00000000190F0109	1295
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PMGPO_REG	0x00000000190F0100	1289
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PMGPI_REG	0x00000000190F0103	1291
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PMSPCWKUPFSP_REG	0x00000000190F010B	1298
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PMSPCWKUPOCC_REG	0x00000000190F010C	1298
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PMSPCWKUPPHYP_REG	0x00000000190F010D	1299
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PMSTATEHISTFSP_REG	0x00000000190F0111	1301
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PMSTATEHISTOCC_REG	0x00000000190F0112	1302
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPERF_REG	0x00000000190F0113	1302
EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPHYP_REG	0x00000000190F0110	1301
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.ASSIST_INTERRUPT_REG	0x000000001A0F0011	1330
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.ATOMIC_LOCK_REG	0x000000001A0F03FF	1378
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.ATTN_INTERRUPT_REG	0x000000001A0F001A	1333
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.CLK_ADJ_REG	0x000000001A0F0015	1332
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.CLK_ADJ_SET	0x000000001A0F0016	1332
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.ERROR_REG	0x000000001A0F001F	1334
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.GP3_REG	0x000000001A0F0012	666
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.HANG_PULSE_0_REG	0x000000001A0F0020	1335
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.HANG_PULSE_1_REG	0x000000001A0F0021	1336
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.HANG_PULSE_2_REG	0x000000001A0F0022	1336
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.HANG_PULSE_3_REG	0x000000001A0F0023	1336
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.HANG_PULSE_4_REG	0x000000001A0F0024	1336
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.HANG_PULSE_5_REG	0x000000001A0F0025	1337
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.HANG_PULSE_6_REG	0x000000001A0F0026	1337
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.HEARTBEAT_REG	0x000000001A0F0018	1332
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.MULTICAST_GROUP_1	0x000000001A0F0001	1329
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.MULTICAST_GROUP_2	0x000000001A0F0002	1329
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.MULTICAST_GROUP_3	0x000000001A0F0003	1330
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.MULTICAST_GROUP_4	0x000000001A0F0004	1330
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.PLL_LOCK_REG	0x000000001A0F0019	1333
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.PRE_COUNTER_REG	0x000000001A0F0028	1337
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.PRIMARY_ADDRESS_REG	0x000000001A0F0000	1329
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.PROTECT_MODE_REG	0x000000001A0F03FE	1378
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.RECOV_INTERRUPT_REG	0x000000001A0F001B	1333
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.SLAVE_CONFIG_REG	0x000000001A0F001E	1334



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EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.TIMEOUT_REG	0x000000001A0F0010	1330
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.VITAL_SCAN_OUT	0x000000001A0F0017	1332
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.XSTOP_INTERRUPT_REG	0x000000001A0F001C	1333
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.COREPFPDDLY_REG	0x000000001A0F012D	1353
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.COREPFPUDLY_REG	0x000000001A0F012C	1353
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.COREPFVRET_REG	0x000000001A0F0130	1354
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.DPLL_CPM_PARM_REG	0x000000001A0F0152	1356
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.ECOPFPDDLY_REG	0x000000001A0F014D	1354
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.ECOPFPUDLY_REG	0x000000001A0F014C	1354
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.ECOPFVRET_REG	0x000000001A0F0150	1355
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.FREQ_CTRL_REG	0x000000001A0F0151	1355
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.IDLEFSMGOTOCMD_REG	0x000000001A0F0114	1352
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBSPM_MODE_REG	0x000000001A0F0156	1363
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_DPLL_STATUS_REG	0x000000001A0F0161	1369
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR1_REG	0x000000001A0F0170	1377
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR2_REG	0x000000001A0F0171	1377
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_CONTROL_STATUS_REG	0x000000001A0F0154	1357
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_PFETSTR_SENSE_REG	0x000000001A0F0157	1364
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VALUE_SETTING_REG	0x000000001A0F0155	1361
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG0	0x000000001A0F0162	1370
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG1	0x000000001A0F0163	1370
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_CONTROL_REG	0x000000001A0F0168	1375
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_STATUS_REG	0x000000001A0F0169	1376
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_OCC_HEARTBEAT_REG	0x000000001A0F0164	1372
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_PMC_VF_CTRL_REG	0x000000001A0F015A	1367
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_BOUNDS_REG	0x000000001A0F015D	1368
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_CONTROL_REG	0x000000001A0F0159	1366
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_IDLE_CONTROL_REG	0x000000001A0F0158	1365
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_STATUS_REG	0x000000001A0F0153	1356
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_INDEX_BOUND_REG	0x000000001A0F015C	1367
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_STEP_TARGET_REG	0x000000001A0F0160	1369
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_CTRL_REG	0x000000001A0F015E	1368
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_REG	0x000000001A0F015F	1368
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG0	0x000000001A0F0165	1373
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG1	0x000000001A0F0166	1373



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EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_STATUS_REG	0x000000001A0F0167	1375
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_UNDERVOLTING_REG	0x000000001A0F015B	1367
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PFSENSE_REG	0x000000001A0F0107	1343
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PFVCSCTLSTAT_REG	0x000000001A0F010E	1348
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PFVDDCNTLSTAT_REG	0x000000001A0F0106	1342
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PMERRMASK_REG	0x000000001A0F010A	1346
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PMERRSUM_REG	0x000000001A0F0108	1344
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PMERR_REG	0x000000001A0F0109	1344
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PMGPO_REG	0x000000001A0F0100	1338
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PMGPI_REG	0x000000001A0F0103	1340
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PMSPCWKUPFSP_REG	0x000000001A0F010B	1347
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PMSPCWKUPOCC_REG	0x000000001A0F010C	1347
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PMSPCWKUPPHYP_REG	0x000000001A0F010D	1348
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PMSTATEHISTFSP_REG	0x000000001A0F0111	1350
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PMSTATEHISTOCC_REG	0x000000001A0F0112	1351
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPERF_REG	0x000000001A0F0113	1351
EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPHYP_REG	0x000000001A0F0110	1350
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.ASSIST_INTERRUPT_REG	0x000000001B0F0011	1380
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.ATOMIC_LOCK_REG	0x000000001B0F03FF	1428
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.ATTN_INTERRUPT_REG	0x000000001B0F001A	1382
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.CLK_ADJ_REG	0x000000001B0F0015	1381
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.CLK_ADJ_SET	0x000000001B0F0016	1381
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.ERROR_REG	0x000000001B0F001F	1383
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.GP3_REG	0x000000001B0F0012	667
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.HANG_PULSE_0_REG	0x000000001B0F0020	1385
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.HANG_PULSE_1_REG	0x000000001B0F0021	1385
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.HANG_PULSE_2_REG	0x000000001B0F0022	1385
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.HANG_PULSE_3_REG	0x000000001B0F0023	1385
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.HANG_PULSE_4_REG	0x000000001B0F0024	1386
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.HANG_PULSE_5_REG	0x000000001B0F0025	1386
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.HANG_PULSE_6_REG	0x000000001B0F0026	1386
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.HEARTBEAT_REG	0x000000001B0F0018	1382
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.MULTICAST_GROUP_1	0x000000001B0F0001	1379
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.MULTICAST_GROUP_2	0x000000001B0F0002	1379
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.MULTICAST_GROUP_3	0x000000001B0F0003	1379
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.MULTICAST_GROUP_4	0x000000001B0F0004	1379
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.PLL_LOCK_REG	0x000000001B0F0019	1382
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.PRE_COUNTER_REG	0x000000001B0F0028	1387
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.PRIMARY_ADDRESS_REG	0x000000001B0F0000	1378
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.PROTECT_MODE_REG	0x000000001B0F03FE	1427
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.RECOV_INTERRUPT_REG	0x000000001B0F001B	1382
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.SLAVE_CONFIG_REG	0x000000001B0F001E	1383
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.TIMEOUT_REG	0x000000001B0F0010	1380
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.VITAL_SCAN_OUT	0x000000001B0F0017	1381
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.XSTOP_INTERRUPT_REG	0x000000001B0F001C	1383
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.COREPFPDDL_REG	0x000000001B0F012D	1402
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.COREPFPUDLY_REG	0x000000001B0F012C	1402



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EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.COREPFVRET_REG	0x000000001B0F0130	1403
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.DPLL_CPM_PARM_REG	0x000000001B0F0152	1405
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.ECOPFPDDLY_REG	0x000000001B0F014D	1404
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.ECOPFPUDLY_REG	0x000000001B0F014C	1403
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.ECOPFVRET_REG	0x000000001B0F0150	1404
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.FREQ_CTRL_REG	0x000000001B0F0151	1404
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.IDLEFSMGOTOCMD_REG	0x000000001B0F0114	1401
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBSPM_MODE_REG	0x000000001B0F0156	1412
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_DPLL_STATUS_REG	0x000000001B0F0161	1418
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR1_REG	0x000000001B0F0170	1426
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR2_REG	0x000000001B0F0171	1427
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_CONTROL_STATUS_REG	0x000000001B0F0154	1406
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_PFETSTR_SENSE_REG	0x000000001B0F0157	1413
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VALUE_SETTING_REG	0x000000001B0F0155	1410
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG0	0x000000001B0F0162	1419
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG1	0x000000001B0F0163	1419
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_CONTROL_REG	0x000000001B0F0168	1425
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_STATUS_REG	0x000000001B0F0169	1425
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_OCC_HEARTBEAT_REG	0x000000001B0F0164	1421
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_PMC_VF_CTRL_REG	0x000000001B0F015A	1416
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_BOUNDS_REG	0x000000001B0F015D	1417
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_CONTROL_REG	0x000000001B0F0159	1415
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_IDLE_CONTROL_REG	0x000000001B0F0158	1414
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_STATUS_REG	0x000000001B0F0153	1406
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_INDEX_BOUND_REG	0x000000001B0F015C	1416
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_STEP_TARGET_REG	0x000000001B0F0160	1418
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_CTRL_REG	0x000000001B0F015E	1417
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_REG	0x000000001B0F015F	1417
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG0	0x000000001B0F0165	1421
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG1	0x000000001B0F0166	1422
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_STATUS_REG	0x000000001B0F0167	1423
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_UNDERVOLTING_REG	0x000000001B0F015B	1416
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PFSENSE_REG	0x000000001B0F0107	1393
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PFVCSCNTLSTAT_REG	0x000000001B0F010E	1397



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EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PFVDDCNTLSTAT_REG	0x000000001B0F0106	1391
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PMERRMASK_REG	0x000000001B0F010A	1395
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PMERRSUM_REG	0x000000001B0F0108	1393
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PMERR_REG	0x000000001B0F0109	1393
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PMGPO_REG	0x000000001B0F0100	1387
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PMGPI_REG	0x000000001B0F0103	1389
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PMSPCWKUPFSP_REG	0x000000001B0F010B	1396
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PMSPCWKUPOCC_REG	0x000000001B0F010C	1397
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PMSPCWKUPPHYP_REG	0x000000001B0F010D	1397
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PMSTATEHISTFSP_REG	0x000000001B0F0111	1399
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PMSTATEHISTOCC_REG	0x000000001B0F0112	1400
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPERF_REG	0x000000001B0F0113	1401
EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPHYP_REG	0x000000001B0F0110	1399
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.ASSIST_INTERRUPT_REG	0x000000001C0F0011	1429
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.ATOMIC_LOCK_REG	0x000000001C0F03FF	1478
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.ATTN_INTERRUPT_REG	0x000000001C0F001A	1432
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.CLK_ADJ_REG	0x000000001C0F0015	1431
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.CLK_ADJ_SET	0x000000001C0F0016	1431
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.ERROR_REG	0x000000001C0F001F	1433
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.GP3_REG	0x000000001C0F0012	668
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.HANG_PULSE_0_REG	0x000000001C0F0020	1434
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.HANG_PULSE_1_REG	0x000000001C0F0021	1435
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.HANG_PULSE_2_REG	0x000000001C0F0022	1435
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.HANG_PULSE_3_REG	0x000000001C0F0023	1435
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.HANG_PULSE_4_REG	0x000000001C0F0024	1435
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.HANG_PULSE_5_REG	0x000000001C0F0025	1436
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.HANG_PULSE_6_REG	0x000000001C0F0026	1436
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.HEARTBEAT_REG	0x000000001C0F0018	1431
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.MULTICAST_GROUP_1	0x000000001C0F0001	1428
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.MULTICAST_GROUP_2	0x000000001C0F0002	1428
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.MULTICAST_GROUP_3	0x000000001C0F0003	1429
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.MULTICAST_GROUP_4	0x000000001C0F0004	1429
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.PLL_LOCK_REG	0x000000001C0F0019	1432
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.PRE_COUNTER_REG	0x000000001C0F0028	1436
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.PRIMARY_ADDRESS_REG	0x000000001C0F0000	1428
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.PROTECT_MODE_REG	0x000000001C0F03FE	1477
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.RECOV_INTERRUPT_REG	0x000000001C0F001B	1432
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.SLAVE_CONFIG_REG	0x000000001C0F001E	1433
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.TIMEOUT_REG	0x000000001C0F0010	1429
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.VITAL_SCAN_OUT	0x000000001C0F0017	1431
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.XSTOP_INTERRUPT_REG	0x000000001C0F001C	1432
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.COREPFPDDL_REG	0x000000001C0F012D	1452
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.COREPFPUDLY_REG	0x000000001C0F012C	1452
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.COREPFVRET_REG	0x000000001C0F0130	1453
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.DPLL_CPM_PARM_REG	0x000000001C0F0152	1455
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.ECOPFPDDL_REG	0x000000001C0F014D	1453
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.ECOPFPUDLY_REG	0x000000001C0F014C	1453
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.ECOPFVRET_REG	0x000000001C0F0150	1454



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EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.FREQ_CTRL_REG	0x000000001C0F0151	1454
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.IDLEFSMGOTOCMD_REG	0x000000001C0F0114	1451
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBSPM_MODE_REG	0x000000001C0F0156	1462
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_DPLL_STATUS_REG	0x000000001C0F0161	1468
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR1_REG	0x000000001C0F0170	1476
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR2_REG	0x000000001C0F0171	1477
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_CONTROL_STATUS_REG	0x000000001C0F0154	1456
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_PFETSTR_SENSE_REG	0x000000001C0F0157	1463
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VALUE_SETTING_REG	0x000000001C0F0155	1460
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG0	0x000000001C0F0162	1469
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG1	0x000000001C0F0163	1469
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_CONTROL_REG	0x000000001C0F0168	1475
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_STATUS_REG	0x000000001C0F0169	1475
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_OCC_HEARTBEAT_REG	0x000000001C0F0164	1471
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_PMC_VF_CTRL_REG	0x000000001C0F015A	1466
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_BOUNDS_REG	0x000000001C0F015D	1467
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_CONTROL_REG	0x000000001C0F0159	1465
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_IDLE_CONTROL_REG	0x000000001C0F0158	1464
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_STATUS_REG	0x000000001C0F0153	1455
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_INDEX_BOUND_REG	0x000000001C0F015C	1466
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_STEP_TARGET_REG	0x000000001C0F0160	1468
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_CTRL_REG	0x000000001C0F015E	1467
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_REG	0x000000001C0F015F	1467
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG0	0x000000001C0F0165	1471
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG1	0x000000001C0F0166	1472
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_STATUS_REG	0x000000001C0F0167	1473
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_UNDERVOLTING_REG	0x000000001C0F015B	1466
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PFSENSE_REG	0x000000001C0F0107	1442
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PFVCSCTLSTAT_REG	0x000000001C0F010E	1447
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PFVDDCNTLSTAT_REG	0x000000001C0F0106	1441
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PMERRMASK_REG	0x000000001C0F010A	1445
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PMERRSUM_REG	0x000000001C0F0108	1443
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PMERR_REG	0x000000001C0F0109	1443
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PMGPO_REG	0x000000001C0F0100	1437



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EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PMGP1_REG	0x000000001C0F0103	1439
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PMSPCWKUPFSP_REG	0x000000001C0F010B	1446
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PMSPCWKUPOCC_REG	0x000000001C0F010C	1446
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PMSPCWKUPPHYP_REG	0x000000001C0F010D	1447
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PMSTATEHISTFSP_REG	0x000000001C0F0111	1449
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PMSTATEHISTOCC_REG	0x000000001C0F0112	1450
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPERF_REG	0x000000001C0F0113	1450
EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPHYP_REG	0x000000001C0F0110	1449
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.ASSIST_INTERRUPT_REG	0x000000001D0F0011	1479
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.ATOMIC_LOCK_REG	0x000000001D0F03FF	1528
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.ATTN_INTERRUPT_REG	0x000000001D0F001A	1482
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.CLK_ADJ_REG	0x000000001D0F0015	1481
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.CLK_ADJ_SET	0x000000001D0F0016	1481
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.ERROR_REG	0x000000001D0F001F	1483
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.GP3_REG	0x000000001D0F0012	669
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.HANG_PULSE_0_REG	0x000000001D0F0020	1484
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.HANG_PULSE_1_REG	0x000000001D0F0021	1485
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.HANG_PULSE_2_REG	0x000000001D0F0022	1485
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.HANG_PULSE_3_REG	0x000000001D0F0023	1485
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.HANG_PULSE_4_REG	0x000000001D0F0024	1485
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.HANG_PULSE_5_REG	0x000000001D0F0025	1486
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.HANG_PULSE_6_REG	0x000000001D0F0026	1486
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.HEARTBEAT_REG	0x000000001D0F0018	1481
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.MULTICAST_GROUP_1	0x000000001D0F0001	1478
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.MULTICAST_GROUP_2	0x000000001D0F0002	1478
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.MULTICAST_GROUP_3	0x000000001D0F0003	1479
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.MULTICAST_GROUP_4	0x000000001D0F0004	1479
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.PLL_LOCK_REG	0x000000001D0F0019	1482
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.PRE_COUNTER_REG	0x000000001D0F0028	1486
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.PRIMARY_ADDRESS_REG	0x000000001D0F0000	1478
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.PROTECT_MODE_REG	0x000000001D0F03FE	1527
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.RECOV_INTERRUPT_REG	0x000000001D0F001B	1482
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.SLAVE_CONFIG_REG	0x000000001D0F001E	1483
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.TIMEOUT_REG	0x000000001D0F0010	1479
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.VITAL_SCAN_OUT	0x000000001D0F0017	1481
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.XSTOP_INTERRUPT_REG	0x000000001D0F001C	1482
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.COREPFPDDLY_REG	0x000000001D0F012D	1502
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.COREPFPUDLY_REG	0x000000001D0F012C	1502
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.COREPFVRET_REG	0x000000001D0F0130	1503
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.DPLL_CPM_PARM_REG	0x000000001D0F0152	1505
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.ECOPFPDDLY_REG	0x000000001D0F014D	1503
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.ECOPFPUDLY_REG	0x000000001D0F014C	1503
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.ECOPFVRET_REG	0x000000001D0F0150	1504
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.FREQ_CTRL_REG	0x000000001D0F0151	1504
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.IDLEFSMGOTOCMD_REG	0x000000001D0F0114	1501
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBSPM_MODE_REG	0x000000001D0F0156	1512
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_DPLL_STATUS_REG	0x000000001D0F0161	1518
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR1_REG	0x000000001D0F0170	1526



Mnemonic	Address	Page
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR2_REG	0x000000001D0F0171	1527
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_CONTROL_STATUS_REG	0x000000001D0F0154	1506
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_PFETSTR_SENSE_REG	0x000000001D0F0157	1513
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VALUE_SETTING_REG	0x000000001D0F0155	1510
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG0	0x000000001D0F0162	1519
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG1	0x000000001D0F0163	1519
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_CONTROL_REG	0x000000001D0F0168	1525
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_STATUS_REG	0x000000001D0F0169	1525
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_OCC_HEARTBEAT_REG	0x000000001D0F0164	1521
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_PMC_VF_CTRL_REG	0x000000001D0F015A	1516
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_BOUNDS_REG	0x000000001D0F015D	1517
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_CONTROL_REG	0x000000001D0F0159	1515
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_IDLE_CONTROL_REG	0x000000001D0F0158	1514
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_STATUS_REG	0x000000001D0F0153	1505
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_INDEX_BOUND_REG	0x000000001D0F015C	1516
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_STEP_TARGET_REG	0x000000001D0F0160	1518
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_CTRL_REG	0x000000001D0F015E	1517
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_REG	0x000000001D0F015F	1517
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG0	0x000000001D0F0165	1521
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG1	0x000000001D0F0166	1522
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_STATUS_REG	0x000000001D0F0167	1523
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_UNDERVOLTING_REG	0x000000001D0F015B	1516
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PFSENSE_REG	0x000000001D0F0107	1492
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PFVSCNTLSTAT_REG	0x000000001D0F010E	1497
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PFVDDCNTLSTAT_REG	0x000000001D0F0106	1491
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PMERRMASK_REG	0x000000001D0F010A	1495
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PMERRSUM_REG	0x000000001D0F0108	1493
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PMERR_REG	0x000000001D0F0109	1493
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PMGPO_REG	0x000000001D0F0100	1487
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PMGPI_REG	0x000000001D0F0103	1489
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PMSPCWKUPFSP_REG	0x000000001D0F010B	1496
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PMSPCWKUPOCC_REG	0x000000001D0F010C	1496
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PMSPCWKUPPHYP_REG	0x000000001D0F010D	1497
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PMSTATEHISTFSP_REG	0x000000001D0F0111	1499



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Mnemonic	Address	Page
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PMSTATEHISTOCC_REG	0x000000001D0F0112	1500
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPERF_REG	0x000000001D0F0113	1500
EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPHYP_REG	0x000000001D0F0110	1499
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.ASSIST_INTERRUPT_REG	0x000000001E0F0011	1529
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.ATOMIC_LOCK_REG	0x000000001E0F03FF	1578
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.ATTN_INTERRUPT_REG	0x000000001E0F001A	1532
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.CLK_ADJ_REG	0x000000001E0F0015	1531
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.CLK_ADJ_SET	0x000000001E0F0016	1531
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.ERROR_REG	0x000000001E0F001F	1533
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.GP3_REG	0x000000001E0F0012	670
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.HANG_PULSE_0_REG	0x000000001E0F0020	1534
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.HANG_PULSE_1_REG	0x000000001E0F0021	1535
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.HANG_PULSE_2_REG	0x000000001E0F0022	1535
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.HANG_PULSE_3_REG	0x000000001E0F0023	1535
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.HANG_PULSE_4_REG	0x000000001E0F0024	1535
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.HANG_PULSE_5_REG	0x000000001E0F0025	1536
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.HANG_PULSE_6_REG	0x000000001E0F0026	1536
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.HEARTBEAT_REG	0x000000001E0F0018	1531
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.MULTICAST_GROUP_1	0x000000001E0F0001	1528
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.MULTICAST_GROUP_2	0x000000001E0F0002	1528
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.MULTICAST_GROUP_3	0x000000001E0F0003	1529
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.MULTICAST_GROUP_4	0x000000001E0F0004	1529
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.PLL_LOCK_REG	0x000000001E0F0019	1532
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.PRE_COUNTER_REG	0x000000001E0F0028	1536
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.PRIMARY_ADDRESS_REG	0x000000001E0F0000	1528
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.PROTECT_MODE_REG	0x000000001E0F03FE	1577
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.RECOV_INTERRUPT_REG	0x000000001E0F001B	1532
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.SLAVE_CONFIG_REG	0x000000001E0F001E	1533
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.TIMEOUT_REG	0x000000001E0F0010	1529
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.VITAL_SCAN_OUT	0x000000001E0F0017	1531
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.XSTOP_INTERRUPT_REG	0x000000001E0F001C	1532
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.COREPFPDLY_REG	0x000000001E0F012D	1552
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.COREPFPUDLY_REG	0x000000001E0F012C	1552
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.COREPFVRET_REG	0x000000001E0F0130	1553
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.DPLL_CPM_PARM_REG	0x000000001E0F0152	1555
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.ECOPFPDLY_REG	0x000000001E0F014D	1553
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.ECOPFPUDLY_REG	0x000000001E0F014C	1553
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.ECOPFVRET_REG	0x000000001E0F0150	1554
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.FREQ_CTRL_REG	0x000000001E0F0151	1554
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.IDLEFSMGOTOCMD_REG	0x000000001E0F0114	1551
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBSPM_MODE_REG	0x000000001E0F0156	1562
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_DPLL_STATUS_REG	0x000000001E0F0161	1568
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR1_REG	0x000000001E0F0170	1576
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR2_REG	0x000000001E0F0171	1577
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_CONTROL_STATUS_REG	0x000000001E0F0154	1556
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_PFETSTR_SENSE_REG	0x000000001E0F0157	1563



Mnemonic	Address	Page
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VALUE_SETTING_REG	0x000000001E0F0155	1560
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG0	0x000000001E0F0162	1569
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG1	0x000000001E0F0163	1569
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_CONTROL_REG	0x000000001E0F0168	1575
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_STATUS_REG	0x000000001E0F0169	1575
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_OCC_HEARTBEAT_REG	0x000000001E0F0164	1571
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_PMC_VF_CTRL_REG	0x000000001E0F015A	1566
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_BOUNDS_REG	0x000000001E0F015D	1567
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_CONTROL_REG	0x000000001E0F0159	1565
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_IDLE_CONTROL_REG	0x000000001E0F0158	1564
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_STATUS_REG	0x000000001E0F0153	1555
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_INDEX_BOUND_REG	0x000000001E0F015C	1566
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_STEP_TARGET_REG	0x000000001E0F0160	1568
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_CTRL_REG	0x000000001E0F015E	1567
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_REG	0x000000001E0F015F	1567
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG0	0x000000001E0F0165	1571
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG1	0x000000001E0F0166	1572
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_STATUS_REG	0x000000001E0F0167	1573
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_UNDERVOLTING_REG	0x000000001E0F015B	1566
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PFSENSE_REG	0x000000001E0F0107	1542
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PFVCSCNTLSTAT_REG	0x000000001E0F010E	1547
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PFVDDCNTLSTAT_REG	0x000000001E0F0106	1541
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PMERRMASK_REG	0x000000001E0F010A	1545
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PMERRSUM_REG	0x000000001E0F0108	1543
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PMERR_REG	0x000000001E0F0109	1543
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PMGPO_REG	0x000000001E0F0100	1537
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PMGPI_REG	0x000000001E0F0103	1539
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PMSPCWKUPFSP_REG	0x000000001E0F010B	1546
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PMSPCWKUPOCC_REG	0x000000001E0F010C	1546
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PMSPCWKUPPHYP_REG	0x000000001E0F010D	1547
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PMSTATEHISTFSP_REG	0x000000001E0F0111	1549
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PMSTATEHISTOCC_REG	0x000000001E0F0112	1550
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPERF_REG	0x000000001E0F0113	1550
EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPHYP_REG	0x000000001E0F0110	1549

The POWER8 Processor registers are listed in the following tables.

Register Name		<i>Contains The Slave's Primary Address</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.PRIMARY_ADDRESS_REG
Address		00000000110F0000 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:5	RO	Reserved field (Access type is primary_address)

Register Name		<i>Multicast Group 1</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.MULTICAST_GROUP_1
Address		00000000110F0001 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST1_GROUP: multicast group1 setting

Register Name		<i>Multicast Group 2</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.MULTICAST_GROUP_2
Address		00000000110F0002 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST2_GROUP: multicast group2 setting

Register Name		<i>Multicast Group 3</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.MULTICAST_GROUP_3
Address		00000000110F0003 (PCB)
Attributes		
Description		



Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST3_GROUP: multicast group3 setting

Register Name	<i>Multicast Group 4</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.MULTICAST_GROUP_4
Address	00000000110F0004 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST4_GROUP: multicast group4 setting

Register Name	<i>Timeout Select Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.TIMEOUT_REG
Address	00000000110F0010 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	Reserved field (Access type is int_timeout)

Register Name	<i>Assist Interrupt Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.ASSIST_INTERRUPT_REG
Address	00000000110F0011 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is attn)
1	ROX	Reserved field (Access type is recov)
2	ROX	Reserved field (Access type is xstop)

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Register Name	GP3 Register (NA In PERV CPLT)
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.GP3_REG
Address	00000000110F0012 (PCB) 00000000110F0013 (PCB1) 00000000110F0014 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset
2	RWX	RWX_WAND	RWX_WOR	GLSMUX_RESET: Glsmux reset for test purpose and stuck active mesh protection. Notice no clocks in the EX if this bit is set.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Put the DPLL in test mode.
4	RWX	RWX_WAND	RWX_WOR	PLL_RST: Put PLL in reset state.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYP: Enable PLL bypass.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pcb_access)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	PM_PI_DECODE: Test override for power management. EX chiplet only.
22	RWX	RWX_WAND	RWX_WOR	RESCLK_DIS: Resonant clocking disable.
23:25	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave will report 'Chiplet Offline'.
27	RWX	RWX_WAND	RWX_WOR	TP_LVLTRANS_FENCE: Electrical winkel fence. Mainly used by power management.
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.
29:31	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)



Register Name	<i>Skew Adjust Data</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.CLK_ADJ_REG	
Address	00000000110F0015 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:15	ROX	

Register Name	<i>Clk Ajust Config</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.CLK_ADJ_SET	
Address	00000000110F0016 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:31	RW	CLK_ADJ_SET_REG: Clk adj config

Register Name	<i>Vital Scan Out</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.VITAL_SCAN_OUT	
Address	00000000110F0017 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	

Register Name	<i>Chiplet Heartbeat Register</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.HEARTBEAT_REG	
Address	00000000110F0018 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	HEARTBEAT_DEAD: Chiplet heartbeat not detected

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Register Name	<i>Lock Indications From PLLs</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.PLL_LOCK_REG
Address	00000000110F0019 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	ROX	Reserved field (Access type is lock)

Register Name	<i>Attn Interrupt</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.ATTN_INTERRUPT_REG
Address	00000000110F001A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is attn)

Register Name	<i>Recov Interrupt</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.RECOV_INTERRUPT_REG
Address	00000000110F001B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is recov)

Register Name	<i>Xstop Interrupt</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.XSTOP_INTERRUPT_REG
Address	00000000110F001C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is xstop)



Register Name	<i>Slave Config Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.SLAVE_CONFIG_REG
Address	00000000110F001E (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	CFG_DISABLE_PERV_THOLD_CHECK: Disable pervasive thold check
1	RW	CFG_DISABLE_MALF_PULSE_GEN: Disable pulse generation for malf alert. Switch back to level
2	RW	CFG_STOP_HANG_CNT_SYS_XSTP: Disable hang counter stop for system xstop
3	RW	CFG_DISABLE_CL_ATOMIC_LOCK: Disable atomic lock for chiplet accesses
4	RW	CFG_DISABLE_HEARTBEAT: Disable check for voltage and gridclock in the chiplet
5	RW	CFG_ZERO_DATA: Sent zero data on any error
6:7	RW	
8:12	RW	ERROR_MASK: mask bits for slave error reporting
13:15	RW	

Register Name	<i>Error Capture Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.ERROR_REG
Address	00000000110F001F (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX_WCLEA R	CE_ERROR: Correctable error on pcb bus
1:3	RWX_WCLEA R	CHIPLET_ERRORS: Errors reported by chiplet 000 = no error 001 = XSCOM command blocked due pending errors 010 chiplet offline 011 partial good 100 invalid address / address error / bad access type 101 clock error 110 parity error / received unexpected packet / wrong packet number 111 timeout This register is for debug purposes only. It only holds meaningful data if it is cleared after each error.
4	RWX_WCLEA R	PARITY_ERROR: Parity error on PCB Interface
5	RWX_WCLEA R	DATA_BUFFER_ERROR: Parity error in data buffer
6	RWX_WCLEA R	ADDR_BUFFER_ERROR: Parity error in address buffer
7	RWX_WCLEA R	PCB_FSM_ERROR: Invalid state error in PCB FSM
8	RWX_WCLEA R	CL_FSM_ERROR: Invalid state error in Chiplet FSM
9	RWX_WCLEA R	INT_RX_FSM_ERROR: Invalid state error in interrupt RX FSM
10	RWX_WCLEA R	INT_TX_FSM_ERROR: Invalid state error in interrupt TX FSM

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Bits	PCB	Field Mnemonic: Description
11	RWX_WCLEAR	INT_TYPE_ERROR: Invalid interrupt type
12	RWX_WCLEAR	CL_DATA_ERROR: Parity error on Chiplet Interface
13	RWX_WCLEAR	INFO_ERROR: Parity error on Chiplet info lines
14	RWX_WCLEAR	UNUSED_0:
15	RWX_WCLEAR	CHIPLET_ATOMIC_LOCK_ERROR: Chiplet atomic lock error
16	RWX_WCLEAR	PCB_INTERFACE_ERROR: Error of pcb interface component for the internal endpoint
17	RWX_WCLEAR	CHIPLET_OFFLINE: Heartbeat check indicated that chiplet is offline
18	RWX_WCLEAR	CHIPLET_GRID_SKITTER: Heartbeat check indicated skitter on the chiplet grid
19	RWX_WCLEAR	GP3_REG_PARITY_ERROR: gp3 register parity bad
20	RWX_WCLEAR	ADDRESS_REG_PARITY_ERROR: address register parity bad
21	RWX_WCLEAR	TIMEOUT_REG_PARITY_ERROR: timeout select register parity bad
22	RWX_WCLEAR	CONFIG_REG_PARITY_ERROR: slave config register parity bad
23	RWX_WCLEAR	CLK_ADJ_REG_PARITY_ERROR: clk adj register parity bad
24	RWX_WCLEAR	DIV_REG_PARITY_ERROR: div register parity bad
25:28	RWX_WCLEAR	PLL_UNLOCK_ERROR: unlock from chiplet pll

Register Name		Hang Pulse Generation Register 0.
Mnemonic		EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.HANG_PULSE_0_REG
Address		00000000110F0020 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_0: Value of hang pulse 0. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_0: If set to '1', hang pulses are suppressed in case of a xstop



Register Name	<i>Hang Pulse Generation Register 1.</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.HANG_PULSE_1_REG
Address	00000000110F0021 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_1: Value of hang pulse 1. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_1: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 2.</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.HANG_PULSE_2_REG
Address	00000000110F0022 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_2: Value of hang pulse 2. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_2: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 3.</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.HANG_PULSE_3_REG
Address	00000000110F0023 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_3: Value of hang pulse 3. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_3: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 4.</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.HANG_PULSE_4_REG
Address	00000000110F0024 (PCB)
Attributes	
Description	

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Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_4: Value of hang pulse 4. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_4: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 5</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.HANG_PULSE_5_REG
Address	00000000110F0025 (PCB)
Attributes	
Description	This hang counter is exclusively used to generate the malfunction alert pulse.

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_5: Value of hang pulse 5. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_5: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 6</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.HANG_PULSE_6_REG
Address	00000000110F0026 (PCB)
Attributes	
Description	This hang counter is exclusively used for heartbeat generation.

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_6: Value of hang pulse 6. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_6: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Divider For Hang Counter Clock</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.PRE_COUNTER_REG
Address	00000000110F0028 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PRE_COUNTER: Divider for hang counter clock. Divides clock by n+1 (default: n=0)



Register Name		PowerManagement GP0		
Mnemonic		EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PMGP0_REG		
Address		00000000110F0100 (PCB) 00000000110F0101 (PCB1) 00000000110F0102 (PCB2)		
Attributes				
Description				
Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PM_DISABLE: Master Switch for the PowerManagement Macro
1	RWX	WOX_AND	WOX_OR	PMGP0_SPARE_BIT1: spare bit
2	RWX	WOX_AND	WOX_OR	TP_TC_RESTART_CORE_DOMAIN: Kicks off small sequencer in OHA to get chiplet clocks back running for fast sleep without involving PORE. From GP-reg and overridden by PowMan State Machine.
3	RWX	WOX_AND	WOX_OR	DPLL_THOLD: Thold for the DPLL clock domain in the chiplet
4	RWX	WOX_AND	WOX_OR	PERV_THOLD: Thold for the Pervasive clock domain in the chiplet
5	RO	RO	RO	Reserved.
6	RO	RO	RO	Reserved.
7	RWX	WOX_AND	WOX_OR	PM_DPLL_TIMER_ENA: Select a timer instead of the DPLL lock bit for criteria to switch to DPLL. The time is defined by thold_timer_sel.
8	RWX	WOX_AND	WOX_OR	DPLL_LOCK_SENSE: DPLL lock sensitivity control (0=faster lock time, 1=slower lock time)
9	RWX	WOX_AND	WOX_OR	PMGP0_SPARE2: spare bit
10	RWX	WOX_AND	WOX_OR	DPLL_RESET: Reset to DPLL
11	RWX	WOX_AND	WOX_OR	PMGP0_SPARE_BIT11: Spare bit
12:19	RWX	WOX_AND	WOX_OR	DPLL_TESTOUT_CTL: DPLL testout control
20	RWX	WOX_AND	WOX_OR	TP_TC_CACHE2CORE_FENCE: Fence from cache to core domain in EX chiplet
21	RWX	WOX_AND	WOX_OR	TP_TC_CORE2CACHE_FENCE: Fence from core to cache domain in EX chiplet
22	RWX	WOX_AND	WOX_OR	TP_TC_PERVASIVE_ECO_FENCE: Pervasive ECO fence
23	RWX	WOX_AND	WOX_OR	CHKSW_HW257424_DISABLE: Debug switch for interrupt retry exhausted bug (0=fix enabled, 1=fix disabled)
24:26	RWX	WOX_AND	WOX_OR	TP_CLK_ASYNC_RESET_DC: Clk async reset for three glitchless muxes, and the two clock dividers (bit 0 = master GLM, bit 1 = ECO Div2 and ECO GLM, bit 2= core Div1 and core GLM)
27:29	RWX	WOX_AND	WOX_OR	TP_CLKGLM_SEL_DC: Glitchless Mux Select for primary chiplet clock source (feeding both core and eco clock muxes) 000 = refclk, 001 = DPLL. 100 = Use constant selected by bit 34, else refclk
30	RWX	WOX_AND	WOX_OR	TP_CLKGLM_ECO_SEL_DC: Glitchless Mux Select for eco domain (cache_nclk) grid. 0= follow primary source chosen by previous field: 1 = Use constant selected by bit 34
31	ROX	NC	NC	SPECIAL_WKUP_DONE: Indicates that special wakeup is done, if asserted
32:33	RWX	WOX_AND	WOX_OR	TP_CLKGLM_CORE_SEL_DC: Glitchless Mux Select for core domain (nclk grid) mux. 0b00=primary GLS mux output, 0b10=constant input, 0b01=refclk. Valid transitions are 0b01 <-> 0b00 <-> 0b10, 0b11 is illegal

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
34	RWX	WOX_AND	WOX_OR	TP_CLKGLM_CONST_DC: Constant input available to all three ClkGlm
35:36	RWX	WOX_AND	WOX_OR	THOLD_TIMER_SEL: Selection for the thold transition timer in the IDLE state machine. 0b00=1024 cycles delay, 0b01=512 cycles delay, 0b10=256 cycles delay, 0b11= 128 cycles delay
37	RWX	WOX_AND	WOX_OR	BLOCK_ALL_WAKEUP_SOURCES: Setting this bit will make the PM Slave ignore any Wakeup events (ext. interrupt, malfunction alert, any special wakeup bit). This bit is intended to enable firmware concurrent patch capability. Note: This does NOT block the interrupt from being presented to the processor core. The following procedure is required on changes: 1. Firmware may only set this bit after first setting special wakeup and polling for special wakeup complete (OHA and PCB-slave both in running state with AISS and PM FSMs idle). 2. Firmware may only clear this bit if all special wakeup bits are first cleared.
38	RWX	WOX_AND	WOX_OR	TP_TC_DPLL_TESTMODE_DC: ADPLL test mode
39	RWX	WOX_AND	WOX_OR	PM_SLV_WINKLE_FENCE: Fence off the powered off chiplet in winkle. - Logical fence/hold for pcb_slave and pcb_slave_pm. For electrical fence see bit 23.
40	RWX	WOX_AND	WOX_OR	L3_ENABLE_SWITCH: Setting this bit activates l3_edram_enable if allowed by system configuration GP3(28). Resetting this bit deactivates l3_edram_enable.
41	RWX	WOX_AND	WOX_OR	TP_CPLT_IVRM_REFBYPASS_DC: Signal to iVRM (used to be controlled by scan-only block inside EX, but needs to be driven by VIO domain)
42	RWX	WOX_AND	WOX_OR	CHKSW_HW241939_DISABLE: if this bit is set to 1, the fix for HW241939 (pfet enable SCOM-ability) is disabled
43	RWX	WOX_AND	WOX_OR	CHKSW_HW273115_DISABLE: if this bit is set to 1, the fix for HW273115 (Pga ACK noack issue when the babystepper is in the winkle state) is disabled
44	RWX	WOX_AND	WOX_OR	CHKSW_HW245103_DISABLE: if this bit is set to 1, the fix for HW245103 resonant clocking CSB and SW -bit ordering change is disabled
45	RWX	WOX_AND	WOX_OR	CHKSW_HW257534_DISABLE: if this bit is set to 1, the fix for HW257534 (fencing of errors) is disabled
46	RWX	WOX_AND	WOX_OR	CHKSW_HW259509_ENABLE: if this bit is set to 0, the fix for HW259509 (Pstate change hanging, because of DPLL flock timer in a hung state) is disabled
47	RWX	WOX_AND	WOX_OR	CHKSW_HW260345_DISABLE: if set to 1, this bit disables the HW260345 fix (fix was to make sure that we enter bypass mode for iVRM safe mode without a glitch that could cause Vcs in regulation and Vdd in bypass)
48:49	ROX	NC	NC	WAKEUP_INT_TYPE: (Known to be unreliable and not supported, informational usage only) Type of the last wakeup event that caused an exit from sleep or winkle (excluding nap!), regardless of present state. 0b01: External interrupt. 0b10: Malfunction Alert. 0b11: Special Wakeup. 0b00: chiplet has never fully entered and exited a chiplet-level idle state since IPL of the system. (Note this does not necessarily get updated when the processor core enters an idle state, only if the PCB-Slave enters and then exits the idle state for this chiplet).
50	ROX	NC	NC	DPLL_LOCK: DPLL lock indicator
51	ROX	NC	NC	SPECIAL_WKUP_ALL_SOURCES_ORED: logical OR of all special wakeup sources
52	ROX	NC	NC	REGULAR_WKUP_AVAILABLE: logical OR of external interrupt and malfunction alert



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
53	RWX	WOX_AND	WOX_OR	BLOCK_REG_WKUP_SOURCES: blocks ext. int. and malf. Alert from waking up PCBS (no block possible for PC!)

Register Name	PowerManagement GP1
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PMGP1_REG
Address	00000000110F0103 (PCB) 00000000110F0104 (PCB1) 00000000110F0105 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	SLEEP_POWER_DOWN_EN: Sleep Power Down Enable: When set to 1, causes hardware to automatically reduce voltage to the Core domain when entering Sleep mode. The voltage value for power down is chosen by sleep_power_off_sel (bit 2). When set to 0, a request is sent to the PORE engine for assistance entering Sleep.
1	RWX	WOX_AND	WOX_OR	SLEEP_POWER_UP_EN: Sleep Power Up Enable: When set to 1, enables automated hardware restoration of voltage via PFETs and, if enabled, iVRMs when exiting Sleep mode. If this bit is set to 0 the hardware rely on external means (PORE or equivalent) to restore voltage.
2	RWX	WOX_AND	WOX_OR	SLEEP_POWER_OFF_SEL: Sleep Power Off Select: Selects which voltage level to place the Core domain PFETs upon Sleep entry. 0 = Vret (Fast Sleep Mode), 1 = Voff (Deep Sleep Mode). Depending on the setting of pmicr_latency_en, this bit is controlled with a PCB-write (0) or by the PMICR in the core (1).
3	RWX	WOX_AND	WOX_OR	WINKLE_POWER_DOWN_EN: Winkle Power Down Enable: When set to 1, causes hardware to automatically reduce voltage to the entire Chiplet (both Core and ECO Domains) when entering Winkle mode. The voltage value for power down is chosen by winkle_power_off_sel (bit 5). When set to 0, a request is sent to the PORE engine for assistance entering Winkle.
4	RWX	WOX_AND	WOX_OR	WINKLE_POWER_UP_EN: Winkle Power Up Enable: When set to 1, enables automated hardware PFET enablement when exiting Winkle mode. If this bit is set to 0 the hardware rely on external means (PORE or equivalent) to cause the PFETs to be re-enabled.
5	RWX	WOX_AND	WOX_OR	WINKLE_POWER_OFF_SEL: Winkle Power Off Select: Selects which voltage level to place the Core and ECO domain PFETs upon Winkle entry. 0 = Vret (Fast Winkle Mode), 1 = Voff (Deep Winkle Mode). Depending on the setting of pmicr_latency_en, this bit is controlled with a PCB-write (0) or by the PMICR in the core (1).
6	RWX	WOX_AND	WOX_OR	OHA_WKUP_OVERRIDE_EN: Needs to be 0 for normal operation. If set to 1, the two following dials are used to override the regular and special wakeup signal from PCBS to OHA
7	RWX	WOX_AND	WOX_OR	OHA_PM_WKUP_OVERRIDE: Enablement by 'oha_wkup_override_en' forces the regular wakeup signal to OHA to the value of this bit regardless of presence of an interrupt source.
8	RWX	WOX_AND	WOX_OR	OHA_SPC_WKUP_OVERRIDE: Enablement by 'oha_wkup_override_en' forces the special wakeup signal to OHA to the value of this bit, regardless of the firmware settings.

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
9	RWX	WOX_AND	WOX_OR	ENDP_RESET_PM_ONLY: If asserted, an endpoint reset of all power management-related functions (not the regular PCB slave) is performed. Intended usage is for recovery.
10	RWX	WOX_AND	WOX_OR	DPLL_FREQ_OVERRIDE_ENABLE: override Fmax/Fmin only, if '1', using register FREQ_CTRL_REG
11	RWX	WOX_AND	WOX_OR	PM_SPR_OVERRIDE_EN: PM SPR Override Enable The PPMCR (0xNNNN) and PPMICR (0XXXXX) accesses the register resources that make up the PMCR SPR used by hypervisor to management Pstates. Thus, PCB updates to it are disabled in hardware to prevent collisions. This bit allows ownership of the PMCR to be switched from hypervisor to OCC. This switch is immediate in hardware, thus, firmware must ensure the ownership switch is otherwise communicated. 0 = Disables the writing of the PPMCR (0xNNNN) from the PCB and allows SPR 884 writes (mtspr) to update the register resource. 1 = Enables the writing of the PPMCR (0xNNNN) from the PCB.
12	RWX	WOX_AND	WOX_OR	FORCE_SAFE_MODE: Force Safe Mode 0 = Allow other enabled features to determine the operational Pstate. 1 = Forces the minimum of POHBR[psafe] and PPMSR[global_pstate_actual] Pstate for the core chiplet as the operational frequency.
13	RWX	WOX_AND	WOX_OR	IVRM_SAFE_MODE_EN: Internal VRM Safe Mode Enable 0 = Disable the iVRM safe mode, thus, no automatic actions occur, if an iVRM error happens. 1 = if the iVRMs are enabled (PIVRMCSR[ivrm_en] is set) and Pstates are enabled and if the error defined by dial pcbs_ivrm_gross_or_fine_err occurs, then the railstepper is forced into bypass mode to prevent a voltage-frequency hazard
14	RWX	WOX_AND	WOX_OR	IVRM_SAFE_MODE_FORCE_ACTIVE: Internal VRM Safe Mode Force Dial 0 = the hardware decides whether to activate the iVRM safe mode or not 1 = the iVRM safe mode is forced regardless (this makes only sense if ivrm_fsm_enable=1 and Pstates are enabled)
15	RWX	WOX_AND	WOX_OR	PMICR_LATENCY_EN: Selects how the sleep/winkle latency (which is deep/fast) is controlled. If asserted the PMICR controls the winkle/sleep_power_off_sel in PMGP1, otherwise those bits are controlled via SCOM by OCC.
16	RWX	WOX_AND	WOX_OR	ENABLE_OCC_CTRL_FOR_LOCAL_PSTATE_EFF_REQ: controls, if the HW (for value 0) or OCC (value 1) is in control of the Local Pstate Effective register in PPSTR
17	RWX	WOX_AND	WOX_OR	SERIALIZE_PFET_POWERDOWN: if asserted, the pFET sequencer will sequence the core and the ECO domain one after the other when powering down
18	RWX	WOX_AND	WOX_OR	SERIALIZE_PFET_POWERUP: if asserted, the pFET sequencer will sequence the ECO and the core domain one after the other when powering up
19	RWX	WOX_AND	WOX_OR	DISABLE_FORCE_DEEP_TO_FAST_SLEEP: 0: (normal operation) - If PCB Slave reports a recoverable error or a checkstop, a DEEP sleep operation is forced to FAST. The entries in sleep/winkle_power_off_sel remain unchanged. 1: force to FAST is disabled.



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
20	RWX	WOX_AND	WOX_OR	DISABLE_FORCE_DEEP_TO_FAST_WINKLE: 0: (normal operation) - If PCB Slave reports a recoverable error or a checkstop, a DEEP winkle operation is forced to FAST. The entries in sleep/winkle_power_off_sel remain unchanged. 1: force to FAST is disabled.

Register Name	PFET Control/Status Register For Core And ECO Vdd
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PFVDDCNTLSTAT_REG
Address	00000000110F0106 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	CORE_VDD_PFET_FORCE_STATE: Core Domain PFET Force State Provides a means for firmware to force the core domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 4:5 = 00 (both core_vdd_pfet_val_override AND core_vdd_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
2:3	RW	ECO_VDD_PFET_FORCE_STATE: ECO Domain PFET Force State Provides a means for firmware to force the ECO domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 6:7 = 00 (both eco_vdd_pfet_val_override AND eco_vdd_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
4	RW	CORE_VDD_PFET_VAL_OVERRIDE: Core Domain PFET Value Override 0 = Override is disabled
5	RW	CORE_VDD_PFET_SEL_OVERRIDE: Core Domain PFET Stage Select Override 0 = Override is disabled
6	RW	ECO_VDD_PFET_VAL_OVERRIDE: ECO Domain PFET Value Override 0 = Override is disabled
7	RW	ECO_VDD_PFET_SEL_OVERRIDE: ECO Domain PFET Stage Select Override 0 = Override is disabled
8	RW	CORE_VDD_PFET_ENABLE_REGULATION_FINGER: Core Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the core_vdd_pfet_enable_value.
9	RW	ECO_VDD_PFET_ENABLE_REGULATION_FINGER: ECO Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the eco_vdd_pfet_enable_value.

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Bits	PCB	Field Mnemonic: Description
10:21	RW	CORE_VDD_PFET_ENABLE_VALUE: Core PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the Core Domain PFET Enables directly. If core_vdd_pfet_val_override = 1, a write to this field sets the state of the core PFET Enables until core_vdd_pfet_val_override is cleared. If core_vdd_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the core_vdd_pfet_valN_slav registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
22:25	RW	CORE_VDD_PFET_SEL_VALUE: Core PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure core_vdd_pfet_valN_slav(0:11) where N is 0 to 11 if core_vdd_pfet_sel_override = 1. If core_vdd_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
26:37	RW	ECO_VDD_PFET_ENABLE_VALUE: ECO PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the ECO PFET Enables directly. If ECO_vdd_pfet_val_override = 1, a write to this field sets the state of the ECO PFET Enables until ECO_vdd_pfet_val_override is cleared. If eco_vdd_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the eco_vdd_pfet_valN_slav registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
38:41	RW	ECO_VDD_PFET_SEL_VALUE: ECO PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure eco_vdd_pfet_valN_slav(0:11) where N is 0 to 11 if eco_vdd_pfet_sel_override = 1. If eco_vdd_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
42:45	ROX	CORE_VDD_PG_STATE: Core power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
46:49	ROX	CORE_VDD_PG_SEL: For debug, contains the actual index n into Core Domain PFET Value [n] SLAT Register set that contains the Core PFET Enable Value currently enabled.
50:53	ROX	ECO_VDD_PG_STATE: ECO Domain power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
54:57	ROX	ECO_VDD_PG_SEL: For debug, contains the actual index n into ECO Domain PFET Value [n] SLAT Register set that contains the ECO PFET Enable Value currently enabled.

Register Name	PFET Sense Register	
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PFSENSE_REG	
Address	00000000110F0107 (PCB)	
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:11	ROX	TP_CORE_VDD_PFET_ENABLE_SENSE: Not used any more.
12:23	ROX	TP_ECO_VDD_PFET_ENABLE_SENSE: Not used any more.



Bits	PCB	Field Mnemonic: Description
24:35	ROX	TP_CORE_VCS_PFET_ENABLE_SENSE: Not used any more.
36:47	ROX	TP_ECO_VCS_PFET_ENABLE_SENSE: Not used any more.

Register Name	<i>PM Error Summary Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PMERRSUM_REG
Address	00000000110F0108 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	PM_ERROR: PM Error is present. Intended for use by special PCB multicast to see error state of all chiplets with a single read (via 510F0108 to read all chiplets)

Register Name	<i>PM Error Register:</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PMERR_REG
Address	00000000110F0109 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_HANG_ERR: Hang during Unassisted Sleep Entry: SLEEP_ENTRY_NOTIFY_PMC state
1	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ASSIST_HANG_ERR: Hang during Assisted Sleep Entry: SLEEP_ENTRY_NOTIFY_PMC_ASSIST state
2	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ERR: Hang during Unassisted Sleep Exit: SLEEP_EXIT_NOTIFY_PMC state
3	ROX	PCBS_SLEEP_EXIT_INVOKE_PORE_ERR: Hang during Assisted Deep Sleep Exit: SLEEP_EXIT_INVOKE_PORE state
4	ROX	PCBS_WINKLE_ENTRY_NOTIFY_PMC_ERR: Hang during Unassisted Winkle Entry: WINKLE_ENTRY_NOTIFY_PMC state
5	ROX	PCBS_WINKLE_ENTRY_SEND_INT_ASSIST_ERR: Hang during Assisted Winkle Entry: WINKLE_ENTRY_SEND_INT_ASSIST state
6	ROX	PCBS_WINKLE_EXIT_NOTIFY_PMC_ERR: Hang during Unassisted Winkle Exit: WINKLE_EXIT_NOTIFY_PMC state
7	ROX	PCBS_WAIT_DPLL_LOCK_ERR: Hang during Unassisted Exit waiting on DPLL: WAIT_DPLL_LOCK state
8	ROX	PCBS_SPARE8_ERR: spare bit, always 0
9	ROX	PCBS_WINKLE_EXIT_SEND_INT_ASSIST_ERR: Hang during Assisted Winkle Exit: WINKLE_EXIT_SEND_INT_ASSIST state
10	ROX	PCBS_WINKLE_EXIT_SEND_INT_POWUP_ASSIST_ERR: Hang during Assisted Winkle Exit: WINKLE_EXIT_SEND_INT_POWUP_ASSIST state
11	ROX	PCBS_WRITE_FSM_GOTO_REG_IN_INVALID_STATE_ERR: write to FSM goto register in invalid state
12	ROX	PCBS_WRITE_PMGP0_IN_INVALID_STATE_ERR: write to PMGP0 in invalid state

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Bits	PCB	Field Mnemonic: Description
13	ROX	PCBS_FREQ_OVERFLOW_IN_PSTATE_MODE_ERR: frequency of DPLL in Pstate mode overflows (Fnom + desired Pstate > 511)
14	ROX	PCBS_ECO_RS_BYPASS_CONFUSION_ERR: ECO railstepper tried to exit Vcs bypass and enter Vdd bypass in one Pstate step (it is not clear, in which order this strange operation should be performed - most likely it should never happen to avoid that Vcs is greater than Vdd)
15	ROX	PCBS_CORE_RS_BYPASS_CONFUSION_ERR: same as previous error, but for core railstepper (it is not clear, in which order this strange operation should be performed - most likely it should never happen to avoid that Vcs is greater than Vdd)
16	ROX	PCBS_READ_LPST_IN_PSTATE_MODE_ERR: read LPST-array while iVRM FSMs are enabled (dial ivrm_fsm_enable asserted)
17	ROX	PCBS_LPST_READ_CORR_ERR: correctable error occurred when reading the LPST
18	ROX	PCBS_LPST_READ_UNCORR_ERR: uncorrectable error occurred when reading the LPST
19	ROX	PCBS_PFET_STRENGTH_OVERFLOW_ERR: overflow occurred when calculating the pFET strength (in final rounding step!)
20	ROX	PCBS_VDS_LOOKUP_ERR: Vds entry not found in lookup table (when performing the linear search!)
21	ROX	PCBS_IDLE_INTERRUPT_TIMEOUT_ERR: idle interrupt timeout in PCB interrupt controller
22	ROX	PCBS_PSTATE_INTERRUPT_TIMEOUT_ERR: PState interrupt timeout in PCB interrupt controller
23	ROX	PCBS_GLOBAL_ACTUAL_SYNC_INTERRUPT_TIMEOUT_ERR: GlobalActualSync Interrupt timeout in PCB interrupt controller
24	ROX	PCBS_PMAX_SYNC_INTERRUPT_TIMEOUT_ERR: PmaxSync Interrupt timeout in PCB interrupt controller
25	ROX	PCBS_GLOBAL_ACTUAL_PSTATE_PROTOCOL_ERR: a write to global actual Pstate register has occurred before the global actual Pstate interrupt has left PCBS
26	ROX	PCBS_PMAX_PROTOCOL_ERR: a write to the Pmax/Pmin register has occurred before the Pmax sync interrupt has left PCB
27	ROX	PCBS_IVRM_GROSS_OR_FINE_ERR: iVRM gross or fine error (details to be found in PCBS_ivrm_Control_Status_Reg)
28	ROX	PCBS_IVRM_RANGE_ERR: iVRM range error (summary bit, details to be found in PCBS_ivrm_Control_Status_Reg)
29	ROX	PCBS_DPLL_CPM_FMIN_ERR: DPLL CPM Fmin error
30	ROX	PCBS_DPLL_DCO_FULL_ERR: DPLL DCO full
31	ROX	PCBS_DPLL_DCO_EMPTY_ERR: DPLL DCO empty
32	ROX	PCBS_DPLL_INT_ERR: DPLL internal error
33	ROX	PCBS_FMIN_AND_NOT_CPMBIT_ERR: dpll_fmin_and_not_cpmbit (ref. to dial cpm_fmin_clip_error_sel on how to configure this)
34	ROX	PCBS_DPLL_FASTER_THAN_FMAX_PLUS_DELTA1_ERR: dpll_faster_than_fmax_plus_delta1 (for characterization, delta1 is configurable with pll_char_delta1)
35	ROX	PCBS_DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2_ERR: dpll_slower_than_fmin_minus_delta2 (for characterization, delta2 is configurable with pll_char_delta2)
36	ROX	PCBS_RESCLK_CSB_INSTR_VECTOR_CHG_IN_INVALID_STATE_ERR: RESCLK CSB instruction vector change while FSMs none idle
37	ROX	PCBS_RESCLK_BAND_BOUNDARY_CHG_IN_INVALID_STATE_ERR: RESCLK Band boundaries change while FSMs none idle
38	ROX	PCBS_OCC_HEARTBEAT_LOSS_ERR: OCC heartbeat loss
39	ROX	PCBS_SPARE39_ERR: spare bit, always 0
40	ROX	PCBS_SPARE40_ERR: spare bit, always 0



Bits	PCB	Field Mnemonic: Description
41	ROX	PCBS_SPARE41_ERR: spare bit, always 0
42	ROX	PCBS_SPARE42_ERR: spare bit, always 0

Register Name	<i>PM Error Mask Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PMERRMASK_REG
Address	00000000110F010A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_HANG_ERR_MASK: Mask for this error: 1=masked, 0=not masked
1	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ASSIST_HANG_ERR_MASK: Mask for this error: 1=masked, 0=not masked
2	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
3	RW	PCBS_SLEEP_EXIT_INVOKE_PORE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
4	RW	PCBS_WINKLE_ENTRY_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
5	RW	PCBS_WINKLE_ENTRY_SEND_INT_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
6	RW	PCBS_WINKLE_EXIT_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
7	RW	PCBS_WAIT_DPLL_LOCK_ERR_MASK: Mask for this error: 1=masked, 0=not masked
8	RW	PCBS_SPARE8_ERR_MASK: Mask for this error: 1=masked, 0=not masked
9	RW	PCBS_WINKLE_EXIT_SEND_INT_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
10	RW	PCBS_WINKLE_EXIT_SEND_INT_POWUP_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
11	RW	PCBS_WRITE_FSM_GOTO_REG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
12	RW	PCBS_WRITE_PMGPO_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
13	RW	PCBS_FREQ_OVERFLOW_IN_PSTATE_MODE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
14	RW	PCBS_ECO_RS_BYPASS_CONFUSION_ERR_MASK: Mask for this error: 1=masked, 0=not masked
15	RW	PCBS_CORE_RS_BYPASS_CONFUSION_ERR_MASK: Mask for this error: 1=masked, 0=not masked
16	RW	PCBS_READ_LPST_IN_PSTATE_MODE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
17	RW	PCBS_LPST_READ_CORR_ERR_MASK: Mask for this error: 1=masked, 0=not masked
18	RW	PCBS_LPST_READ_UNCORR_ERR_MASK: Mask for this error: 1=masked, 0=not masked
19	RW	PCBS_PFET_STRENGTH_OVERFLOW_ERR_MASK: Mask for this error: 1=masked, 0=not masked
20	RW	PCBS_VDS_LOOKUP_ERR_MASK: Mask for this error: 1=masked, 0=not masked
21	RW	PCBS_IDLE_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
22	RW	PCBS_PSTATE_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
23	RW	PCBS_GLOBAL_ACTUAL_SYNC_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
24	RW	PCBS_PMAX_SYNC_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked

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Bits	PCB	Field Mnemonic: Description
25	RW	PCBS_GLOBAL_ACTUAL_PSTATE_PROTOCOL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
26	RW	PCBS_PMAX_PROTOCOL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
27	RW	PCBS_IVRM_GROSS_OR_FINE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
28	RW	PCBS_IVRM_RANGE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
29	RW	PCBS_DPLL_CPM_FMIN_ERR_MASK: Mask for this error: 1=masked, 0=not masked
30	RW	PCBS_DPLL_DCO_FULL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
31	RW	PCBS_DPLL_DCO_EMPTY_ERR_MASK: Mask for this error: 1=masked, 0=not masked
32	RW	PCBS_DPLL_INT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
33	RW	PCBS_FMIN_AND_NOT_CPMBIT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
34	RW	PCBS_DPLL_FASTER_THAN_FMAX_PLUS_DELTA1_ERR_MASK: Mask for this error: 1=masked, 0=not masked
35	RW	PCBS_DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2_ERR_MASK: Mask for this error: 1=masked, 0=not masked
36	RW	PCBS_RESCLK_CSB_INSTR_VECTOR_CHG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
37	RW	PCBS_RESCLK_BAND_BOUNDARY_CHG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
38	RW	PCBS_OCC_HEARTBEAT_LOSS_ERR_MASK: Mask for this error: 1=masked, 0=not masked
39	RW	PCBS_SPARE39_ERR_MASK: Mask for this error: 1=masked, 0=not masked
40	RW	PCBS_SPARE40_ERR_MASK: Mask for this error: 1=masked, 0=not masked
41	RW	PCBS_SPARE41_ERR_MASK: Mask for this error: 1=masked, 0=not masked
42	RW	PCBS_SPARE42_ERR_MASK: Mask for this error: 1=masked, 0=not masked

Register Name		<i>PM Special Wakeup FSP</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PMSPCWKUPFSP_REG
Address		00000000110F010B (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RW	FSP_SPECIAL_WAKEUP: Chiplet Special Wakeup for FSP Firmware use. NOTE: protocol is required when setting this bit

Register Name		<i>PM Special Wakeup OCC</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PMSPCWKUPOCC_REG
Address		00000000110F010C (PCB)
Attributes		
Description		



Bits	PCB	Field Mnemonic: Description
0	RW	OCC_SPECIAL_WAKEUP: Chiplet Special Wakeup for OCC Firmware use. NOTE: protocol is required when setting this bit

Register Name	<i>PM Special Wakeup Hypervisor</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PMSPCWKUPPHYP_REG
Address	00000000110F010D (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	PHYP_SPECIAL_WAKEUP: Chiplet Special Wakeup for hypervisor Firmware use. NOTE: protocol is required when setting this bit

Register Name	<i>PFET Control/Status Register For Core And ECO Vcs</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PFVCSCTLSTAT_REG
Address	00000000110F010E (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	CORE_VCS_PFET_FORCE_STATE: Core Domain PFET Force State Provides a means for firmware to force the core domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 4:5 = 00 (both core_vcs_pfet_val_override AND core_vcs_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
2:3	RW	ECO_VCS_PFET_FORCE_STATE: ECO Domain PFET Force State Provides a means for firmware to force the ECO domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 6:7 = 00 (both eco_vcs_pfet_val_override AND eco_vcs_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
4	RW	CORE_VCS_PFET_VAL_OVERRIDE: Core Domain PFET Value Override 0 = Override is disabled
5	RW	CORE_VCS_PFET_SEL_OVERRIDE: Core Domain PFET Stage Select Override 0 = Override is disabled
6	RW	ECO_VCS_PFET_VAL_OVERRIDE: ECO Domain PFET Value Override 0 = Override is disabled
7	RW	ECO_VCS_PFET_SEL_OVERRIDE: ECO Domain PFET Stage Select Override 0 = Override is disabled

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Bits	PCB	Field Mnemonic: Description
8	RW	CORE_VCS_PFET_ENABLE_REGULATION_FINGER: Core Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the core_vcs_pfet_enable_value.
9	RW	ECO_VCS_PFET_ENABLE_REGULATION_FINGER: ECO Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the eco_vcs_pfet_enable_value.
10:21	RW	CORE_VCS_PFET_ENABLE_VALUE: Core PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the Core Domain PFET Enables directly. If core_vcs_pfet_val_override = 1, a write to this field sets the state of the core PFET Enables until core_vcs_pfet_val_override is cleared. If core_vcs_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the core_vcs_pfet_valN_slav registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
22:25	RW	CORE_VCS_PFET_SEL_VALUE: Core PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure core_vcs_pfet_valN_slav(0:11) where N is 0 to 11 if core_vcs_pfet_sel_override = 1. If core_vcs_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
26:37	RW	ECO_VCS_PFET_ENABLE_VALUE: ECO PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the ECO PFET Enables directly. If ECO_vcs_pfet_val_override = 1, a write to this field sets the state of the ECO PFET Enables until ECO_vcs_pfet_val_override is cleared. If eco_vcs_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the eco_vcs_pfet_valN_slav registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
38:41	RW	ECO_VCS_PFET_SEL_VALUE: ECO PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure eco_vcs_pfet_valN_slav(0:11) where N is 0 to 11 if eco_vcs_pfet_sel_override = 1. If eco_vcs_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
42:45	ROX	CORE_VCS_PG_STATE: Core power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
46:49	ROX	CORE_VCS_PG_SEL: For debug, contains the actual index n into Core Domain PFET Value [n] SLAT Register set that contains the Core PFET Enable Value currently enabled.
50:53	ROX	ECO_VCS_PG_STATE: ECO Domain power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
54:57	ROX	ECO_VCS_PG_SEL: For debug, contains the actual index n into ECO Domain PFET Value [n] SLAT Register set that contains the ECO PFET Enable Value currently enabled.



Register Name	<i>PM State History Register For Hypervisor</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPHYP_REG
Address	00000000110F0110 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	PHYP_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPART	PHYP_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPART	PHYP_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPART	PHYP_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPART	PHYP_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPART	PHYP_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For FSP</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PMSTATEHISTFSP_REG
Address	00000000110F0111 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	FSP_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPART	FSP_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPART	FSP_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPART	FSP_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.



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Bits	PCB	Field Mnemonic: Description
6	ROX_CLRPAR T	FSP_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	FSP_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For OCC</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PMSTATEHISTOCC_REG
Address	00000000110F0112 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	OCC_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	OCC_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	OCC_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	OCC_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	OCC_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	OCC_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For PerfMon</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPERF_REG
Address	00000000110F0113 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	PERF_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	PERF_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	PERF_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	PERF_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	PERF_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	PERF_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM FSM Reset And Babystepper Idle Injects</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.IDLEFSMGOTOCMD_REG
Address	00000000110F0114 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	WO_1P	idle_fsm_goto_cmd ' A write to this reg will proceed the IDLE FSM from WAIT_FOR_PORE_DONE, SLEEP_EXIT_WAIT_FOR_PORE_FAST_EXIT_DONE, or WINKLE_EXIT_WAIT_FOR_PORE_FAST_EXIT_DONE to the following states: ' 0b01: goto IDLE state ' 0b10: goto SLEEP_EXIT_CORE_MESHLET_ON state ' 0b11: goto WINKLE_EXIT_NOTIFY_PMC state ' '
2	RWX	babystp_trigger_sleep_entry ' A write to this reg with a 1 in this field will cause the babystepper to run the sleep entry sequence. This step is needed for an assisted entry into sleep, before the power is actually turned off since the babystepper needs to know about the sleep state. For an unassisted entry, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished entering its sleep mode. '
3	RWX	babystp_trigger_winkle_entry ' A write to this reg with a 1 in this field will cause the babystepper to run the winkle entry sequence. This step is needed for an assisted entry into winkle before the power is actually turned off since the babystepper needs to know about the winkle state. For an unassisted entry, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished entering its winkle mode. '
4	RWX	babystp_trigger_wakeup ' A write to this reg with a 1 in this field will cause the babystepper to run the wakeup sequence from sleep/winkle depending on the babystepper state of sleep or winkle. This step is needed for an assisted exit from winkle before the power is actually turned off since the babystepper needs to know about the wakeup state. For an unassisted exit, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished waking up from sleep or winkle. '

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Register Name	Core PFET Power Up Delay
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.COREPFPUDLY_REG
Address	00000000110F012C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_POWUP_DLY0: Delay used after transitioning to Core Domain power up sequence stage0. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	CORE_POWUP_DLY1: Delay used after transitioning to Core domain power up sequence stage1.
8:19	RW	CORE_POWER_UP_DELAY_SEL: Vector select for which delay to use for the respective power-up stage. Bit mapping: 8 -> core_*_pfet_enable(0) 9 -> core_*_pfet_enable(1) ... 19 -> core_*_pfet_enable(11) Bit meaning: 0 = Use core_powup_dly0 1 = Use core_powup_dly1

Register Name	Core PFET Power Down Delay
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.COREPFPDDLY_REG
Address	00000000110F012D (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_POWDN_DLY0: Delay used after transitioning to Core domain power dn sequence stage1. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	CORE_POWDN_DLY1: Delay used after transitioning to Core domain power dn sequence stage1. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
8:19	RW	CORE_POWER_DN_DELAY_SEL: Vector select for which delay to use for the respective power-dn stage. Bit mapping: 8 -> core_*_pfet_enable(0) 9 -> core_*_pfet_enable(1) ... 19 -> core_*_pfet_enable(11) Bit meaning: 0 = Use core_powdn_dly0 1 = Use core_powdn_dly1



Register Name	Core PFET Vretention	
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.COREPFVRET_REG	
Address	00000000110F0130 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_VRET_SEL: Pointer to the stage representing the Vretention value for the core PFETs. Power down sequences will stop after enabling this stage.
4:7	RW	CORE_VOFF_SEL: Pointer to the stage representing the Voff value for the core PFETs. Power down sequences will stop after enabling this stage.

Register Name	ECO PFET Power Up Delay	
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.ECOPFPUDLY_REG	
Address	00000000110F014C (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_POWUP_DLY0: Delay used after transitioning to ECO domain power up sequence stage0 in terms of refclk period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	ECO_POWUP_DLY1: Delay used after transitioning to ECO domain power up sequence stage1.
8:19	RW	ECO_POWER_UP_DELAY_SEL: Vector select for which delay to use for the respective power-up stage. Bit mapping: 8 -> eco_*_pfet_enable(0) 9 -> eco_*_pfet_enable(1) ... 19 -> eco_*_pfet_enable(11) Bit meaning: 0 = Use eco_powup_dly0 1 = Use eco_powup_dly1

Register Name	ECO PFET Power Down Delay	
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.ECOPFPDDLY_REG	
Address	00000000110F014D (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_POWDN_DLY0: UNUSED/SPARE
4:7	RW	ECO_POWDN_DLY1: Delay used after transitioning to ECO Domain power dn sequence stage1. The delays in this register are in terms of refclk period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.

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Bits	PCB	Field Mnemonic: Description
8:19	RW	ECO_POWER_DN_DELAY_SEL: Vector select for which delay to use for the respective power-down stage. Bit mapping: 8 -> eco_*_pfet_enable(0) 9 -> eco_*_pfet_enable(1) ... 19 -> eco_*_pfet_enable(11) Bit meaning: 0 = Use eco_powdn_dly0 1 = Use eco_powdn_dly1

Register Name		<i>ECO PFET Vretention</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.ECOPFVRET_REG
Address		00000000110F0150 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_VRET_SEL: Pointer to the stage representing the Vretention value for the ECO PFETs. Power down sequences will stop after enabling this stage.
4:7	RW	ECO_VOFF_SEL: Pointer to the stage representing the Voff value for the ECO PFETs. Power down sequences will stop after enabling this stage.

Register Name		<i>Frequency Control Register With Overrides For DPLL.</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.FREQ_CTRL_REG
Address		00000000110F0151 (PCB)
Attributes		
Description		Note that overrides to Dpll_fmax are only applied, if Dpll_freq_override_enable = 1. A read of all these dials always returns the currently established DPLL frequencies (regardless of any other mode settings).

Bits	PCB	Field Mnemonic: Description
0:8	RWX	DPLL_FMIN: minimum DPLL frequency in CPM-DPLL mode that is set at IPL time A read always returns the currently established value A write is not conditioned on any other dial setting.
9:17	RWX	DPLL_FMAX: DPLL maximum frequency and frequin (these two values are the same in the POWER8 processor) without applying bias values: A read always returns the currently established value A write is conditioned on the setting of dpll_freq_override_enable. If dpll_freq_override_enable is asserted, a write causes this field to update. Otherwise the hardware (that is, PStates) are controlling the update of this value.
18:21	RW	DPLL_FMAX_BIAS: Bias for the maximum DPLL frequency intended to be used in CPM-DPLL mode to control explicitly the hard limit for the maximum DPLL frequency. Note that this signed value gets added to the value of dpll_fmax and the result is established as the effective DPLL Fmax input. Thus, in non-CPM mode it is recommended to set this dial to 0. Note also that this dial MUST be zero in non-CPM mode
22:30	RW	FREQU_AT_PSTATE0: DPLL frequency for Pstate 0



Register Name	<i>DPLL Mode Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.DPLL_CPM_PARM_REG
Address	00000000110F0152 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	LF_SLEWRATEXPI: out of lock slew rate for DPLL
8	RW	LF_USE_CPMXPI: use CPM instead of PFD as loop filter input, if '1' (instead of using both)
9	RW	FF_USE_CPMXPI: use the CPM inputs for the frequency filter, if '1'
10	RW	CPM_FILTER_ENABLE: enables the CPM filter
11	RW	FF_BYPASSXPI: enables frequency filter bypass
12	RW	DCO_OVERRIDE: enables overrides for DCO testing/characterization
13	RW	DCO_INCR: enables increment for DCO testing/characterization, increments only on a rising edge
14	RW	DCO_DECR: enables decrement for DCO testing/characterization, decrements only on a rising edge
15:23	RW	DPLL_LOCK_TIMER_REPLACEMENT_VALUE: if dpll_lock_replacement_timer_mode_en is set, this dial specifies the delay in us, after which it is assumed, that the DPLL has reached a frequency lock condition. Note that values less than 3 will cause in undefined HW behavior (0 will cause hangs!). If dpll_lock_replacement_timer_mode_en is zero, this dial specifies the delay in pcb_nclk cycles after which the hardware monitors the DPLL frequout output (if dpll_freqout_mode_en is set) or the DPLL flock output (if dpll_flock_mode_en is set). Note that in this case, the value of this dial needs to be greater or equal to 150 (decimal).
24:31	RW	PRE_VRET_PSTATE: Pstate that is stepped to before switching to Vretention defined in PCBS_iVRM_Control_Status_Reg
32	RW	OVERRIDE_PCBS_DPLL_SYNCHRONIZER: Bypasses the 'ping-pong' synchronization logic between the DPLL and the PCBS-PM. NEVER SET TO 1 UNLESS YOU KNOW WHAT YOU ARE DOING!
33:36	RW	DPLL_CHAR_DELTA1: Delta in DPLL ticks for characterization (cf. dial dpll_faster_than_fmax_plus_delta1)
37:40	RW	DPLL_CHAR_DELTA2: Delta in DPLL ticks for characterization (cf. dial dpll_faster_than_fmin_minus_delta2)

Register Name	<i>Read Access To The Power Management Status</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_STATUS_REG
Address	00000000110F0153 (PCB)
Attributes	
Description	The PPMSR provides read access to the power management status that is also shadowed to pc and visible to hypervisor in the PMSR (with some delay due to the shadowing process).

Bits	PCB	Field Mnemonic: Description
0:7	ROX	global_pstate_actual ' Actual Global Pstate Pstate or Pglobal_actual' " Reads from this field return the presently established global PState value.' " Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent '

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Bits	PCB	Field Mnemonic: Description
8:15	ROX	LOCAL_PSTATE_ACTUAL: ' Actual Local PState or Plocal_actual' " 'Reads from this field return the presently established local PState value. This value will always be less than or equal to global_pstate_actual.' " 'Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent' "
16:23	ROX	pv_min Minimum Pstate set by the platform.
24:31	ROX	pvf_max Maximum Pstate set by the platform.
32	ROX	spr_em_disabled ' SPR Energy Management Disabled' 'Read from this field indicate whether the platform has disabled the ' 'PMCR and PMICR SPRs to control the chiplet PState. '
33	ROX	Psafe_mode_active Read from this field indicate whether the chiplet has been put into a safe mode with Psafe enabled to a OCC heartbeat loss or other externally forced reasons (0=regular mode, 1=safe mode is active)
34	ROX	iVRM_safe_mode_active Read from this field indicate whether the chiplet has been put the iVRM safe mode (forcing the bypass mode for all iVRMs)
35	ROX	ivrm_enable Read from this field indicate whether the chiplet internal voltage regulation macro is enabled for localized voltage control (0=disabled, 1=enabled) based on ANDing the power on signals to the iVRMs
36	ROX	all_fsms_in_safe_state For recovery: if this bit is asserted, all Pstate and iVRM control FSMs are in a stable, safe state that allows the recovery routine to proceed with resetting the PCBS PM without the risk of interrupt a critical action
37:40	ROX	pmsr_spares spare bits

Register Name	Access To Chiplet Level Controls Of The Internal VRM Rail Set
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_CONTROL_STATUS_REG
Address	00000000110F0154 (PCB)
Attributes	
Description	The PIVRMCSR provides access to chiplet level controls of the internal VRM rail set (VDD and VCS) across both the core and ECO domains. The following is valid only for bits 4 to 7: when in automatic iVRM mode (ivrm_fsm_enable=1), these bits provide access to the values established by the automatic hardware mechanism. When in iVRM override mode (ivrm_fsm_enable=0), these bits allow firmware direct control of the values driving the internal VRMs.

Bits	PCB	Field Mnemonic: Description
0	RW	IVRM_FSM_ENABLE: Internal master VRM FSM Enable 0 = Disable Internal VRM FSMs and enable to control the iVRMs with the available override registers (SCOMable) as a backup mode or for setup (override mode) 1 = Enable Internal VRM FSM sequencers (requires that Pstates are enabled with enable_Pstate_mode=1 as well) (automatic mode)
1	RW	USE_IVRM_FOR_VRET: Internal VRM Enabled for Vretention 0 = Disable Internal VRM for Vretention 1 = Enable Internal VRM for Vretention
2	RW	BINSEARCH_CAL_ENA: trigger binary search (level signal)

Bits	PCB	Field Mnemonic: Description
3	RW	PVREF_EN: Internal VRM Power Voltage Reference Forced Enable 0 = Allow hardware to enable/disable pvref circuit 1 = Force enablement of the pvref circuit
4	RWX	IVRM_CORE_VDD_BYPASS_B: Internal VRM Core VDD Bypass (negative active) 0 = VDD Internal Core VRMs in bypass 1 = VDD internal Core VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
5	RWX	IVRM_CORE_VDD_POWERON: Internal VRM Core VDD Poweron 0 = Core VDD Internal VRMs powered off 1 = Core VDD internal VRMs powered on if this bit is not set (=0), the Core VDD internal VRM powered off internally. If this bit is set (=1), the Core VDD internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
6	RWX	IVRM_CORE_VCS_BYPASS_B: Internal VRM Core VCS Bypass (negative active) 0 = VCS Internal Core VRMs in bypass 1 = VCS internal Core VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VCS internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VCS internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
7	RWX	IVRM_CORE_VCS_POWERON: Internal VRM Core VCS Poweron 0 = Core VCS Internal VRMs powered off 1 = Core VCS internal VRMs powered on if this bit is not set (=0), the Core VCS internal VRM powered off internally. If this bit is set (=1), the Core VCS internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
8	RWX	IVRM_ECO_VDD_BYPASS_B: Internal VRM ECO VDD Bypass (negative active) 0 = VDD Internal ECO VRMs in bypass 1 = VDD internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
9	RWX	IVRM_ECO_VDD_POWERON: Internal VRM ECO VDD Bypass (negative active) 0 = VDD Internal ECO VRMs in bypass 1 = VDD internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.

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Bits	PCB	Field Mnemonic: Description
10	RWX	IVRM_ECO_VCS_BYPASS_B: Internal VRM ECO VCS Bypass (negative active) 0 = VCS Internal ECO VRMs in bypass 1 = VCS internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VCS internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VCS internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
11	RWX	IVRM_ECO_VCS_POWERON: Internal VRM ECO VCS Poweron 0 = ECO VCS Internal VRMs powered off 1 = ECO VCS internal VRMs powered on if this bit is not set (=0), the ECO VCS internal VRM powered off internally. If this bit is set (=1), the ECO VCS internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
12:18	RWX	IVRM_VRET_VDD: if use_ivrm_for_Vret is asserted, this dial is used to control the Vdd retention voltage. Note: this field will establish the Core VDD rail for Sleep and both the Core and ECO rail for Winkle. - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
19:25	RWX	IVRM_VRET_VCS: if use_ivrm_for_Vret is asserted, this dial is used to control the Vcs retention voltage. Note: this field will establish the Core VDD rail for Sleep and both the Core and ECO rail for Winkle. - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
26:30	RWX	IVRM_VRET_CORE_VDD_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the Core Vdd iVRM PFET strength for the retention voltage
31:35	RWX	IVRM_VRET_CORE_VCS_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the Core Vcs iVRM PFET strength for the retention voltage
36:40	RWX	IVRM_VRET_ECO_VDD_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the ECO Vdd iVRM PFET strength for the retention voltage
41:45	RWX	IVRM_VRET_ECO_VCS_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the ECO Vcs iVRM PFET strength for the retention voltage
46	RW	PVREF_FAIL: voltage reference fail input to iVRMs
47	ROX	IVRM_PREF_ERROR_GROSS: Voltage Reference Gross Error 0 = Gross Error not detected 1 = Gross Error detected
48	ROX	IVRM_PREF_ERROR_FINE: Voltage Reference Fine Error 0 = Fine Error not detected 1 = Fine Error detected
49	ROX	IVRM_CORE_VDD_RANGE_HI: Core VDD Internal VRM Range Hi Indicator 0 = Core VDD Internal VRM Hi indicator signal not asserted 1 = Core VDD internal VRMs Hi indicator signal asserted
50	ROX	IVRM_CORE_VDD_RANGE_LO: Core VDD Internal VRM Range Low Indicator 0 = Core VDD Internal VRM Low indicator signal not asserted 1 = Core VDD internal VRMs Low indicator signal asserted



Bits	PCB	Field Mnemonic: Description
51	ROX	IVRM_ECO_VDD_RANGE_HI: ECO VDD Internal VRM Range Hi Indicator 0 = ECO VDD Internal VRM Hi indicator signal not asserted 1 = ECO VDD internal VRMs Hi indicator signal asserted
52	ROX	IVRM_ECO_VDD_RANGE_LO: ECO VDD Internal VRM Range Low Indicator 0 = ECO VDD Internal VRM Low indicator signal not asserted 1 = ECO VDD internal VRMs Low indicator signal asserted
53	ROX	IVRM_CORE_VCS_RANGE_HI: Core VCS Internal VRM Range Hi Indicator 0 = Core VCS Internal VRM Hi indicator signal not asserted 1 = Core VCS internal VRMs Hi indicator signal asserted
54	ROX	IVRM_CORE_VCS_RANGE_LO: Core VCS Internal VRM Range Low Indicator 0 = Core VCS Internal VRM Low indicator signal not asserted 1 = Core VCS internal VRMs Low indicator signal asserted
55	ROX	IVRM_ECO_VCS_RANGE_HI: ECO VCS Internal VRM Range Hi Indicator 0 = ECO VCS Internal VRM Hi indicator signal not asserted 1 = ECO VCS internal VRMs Hi indicator signal asserted
56	ROX	IVRM_ECO_VCS_RANGE_LO: ECO VCS Internal VRM Range Low Indicator 0 = ECO VCS Internal VRM Low indicator signal not asserted 1 = ECO VCS internal VRMs Low indicator signal asserted
57	ROX	BINSEARCH_CAL_DONE: binary search done signal
58	RWX	IVRM_CORE_VDD_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
59	RWX	IVRM_CORE_VCS_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
60	RWX	IVRM_ECO_VDD_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
61	RWX	IVRM_ECO_VCS_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
62	RW	IVRM_POWER_DOWN_DISABLE: If this bit is 1, the iVRM poweron signal is left asserted. Power off of the iVRMs is then blocked

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Register Name	Access To VID Values And PFET Strength Valid Signal Settings
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VALUE_SETTING_REG
Address	00000000110F0155 (PCB)
Attributes	
Description	The PIVRMVSR allows access to VID values and PFET strength valid signal settings presented to the internal VRM rail set (VDD and VCS) across both the core and ECO domains. When In Ivrsm_fsm_enable = "auto" mode, this register provides access to the values established by the automatic hardware mechanism. When Ivrsm_fsm_enable = "override" mode, this register allows firmware direct control of the values driving the internal VRMs Which, if the VRMs are not in bypass, will move the voltage settings.

Bits	PCB	Field Mnemonic: Description
0:7	RWX	IVRM_CORE_VDD_IVID: When read, returns the value presently being driving to the Core VDD iVRM. If ivrm_fsm_enable =0 (override_mode), then writes to this field will drive a new VID value to the Core VDD iVRM. If ivrm_fsm_enable = 1, writes to this field are not performed. 0 = Reserved 1:7 = ivid_vdd - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
8:15	RWX	IVRM_CORE_VCS_IVID: When read, returns the value presently being driving to the Core VCS iVRM. If ivrm_fsm_enable =0 (override_mode), then writes to this field will drive a new VID value to the Core VCS iVRM. If ivrm_fsm_enable = 1, writes to this field are not performed. 0 = Reserved 1:7 = ivid_vdd - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
16:23	RWX	IVRM_ECO_VDD_IVID: When read, returns the value presently being driving to the Core VDD iVRM. If ivrm_fsm_enable =0 (override_mode), then writes to this field will drive a new VID value to the ECO VDD iVRM. If ivrm_fsm_enable = 1, writes to this field are not performed. 0 = Reserved 1:7 = ivid_vdd - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
24:31	RWX	IVRM_ECO_VCS_IVID: When read, returns the value presently being driving to the ECO VCS iVRM. If ivrm_fsm_enable =0 (override_mode), then writes to this field will drive a new VID value to the ECO VCS iVRM, If ivrm_fsm_enable = 0, writes to this field are not performed. 0 = Reserved 1:7 = ivid_vdd - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
32:36	RWX	IVRM_CORE_VDD_PFET_STRENGTH: When read, returns the value presently being driving to the core VCS iVRM. If ivrm_fsm_enable =0 (override_mode), then writes to this field will drive a new strength value to the core VCS iVRM, If ivrm_fsm_enable = 0, writes to this field are not performed.

Bits	PCB	Field Mnemonic: Description
37:41	RWX	IVRM_CORE_VCS_PFET_STRENGTH: This register is assigned to the signals tcex##_tp_ivrm_core_vcs_sense & tcex##_tp_ivrm_core_vdd_sense & tcex##_tp_ivrm_eco_vcs_sense & tcex##_tp_ivrm_eco_vdd_sense & 0b0 Note that all other sense signals are spares now and tied to 0. OUTDATED TEXT: When read, returns the value presently being driving to the core VDD iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the core VDD iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
42:46	RWX	IVRM_ECO_VDD_PFET_STRENGTH: When read, returns the value presently being driving to the ECO VCS iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the ECO VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
47:51	RWX	IVRM_ECO_VCS_PFET_STRENGTH: When read, returns the value presently being driving to the ECO VDD iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the ECO VDD iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
52	RWX	IVRM_VDD_CORE_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the Core VDD iVRM. If ivrm_fsm_enable = 1 AND ivrm_control_mode = 1 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the Core VDD iVRM, If ivrm_fsm_enable = 0 OR ivrm_control_mode = 0, writes to this field are not performed.
53	RWX	IVRM_VCS_CORE_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the Core VCS iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the Core VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
54	RWX	IVRM_VDD_ECO_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the ECO VDD iVRM. If ivrm_fsm_enable = 1 AND ivrm_control_mode = 1 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the ECO VDD iVRM, If ivrm_fsm_enable = 0 OR ivrm_control_mode = 0, writes to this field are not performed.
55	RWX	IVRM_VCS_ECO_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the ECO VCS iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the ECO VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
56	RWX	CORE_VDD_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
57	RWX	CORE_VCS_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
58	RWX	ECO_VDD_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
59	RWX	ECO_VCS_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.

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Register Name		General PCBS Modes And Chicken Switches
Mnemonic		EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBSPM_MODE_REG
Address		00000000110F0156 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RW	ENABLE_PSTATE_MODE: if asserted, Pstate requests (from overrides or PMCR) will be honored, otherwise, the hardware does not do anything. Note to firmware: this is the master switch for Pstates and should be asserted after all sub-modes (that is, lvrn_fsm_en) are setup to avoid enabling unintentional modes during the mode setup.
1	RW	GLOBAL_PSTATE_CHANGE_FOR_IDLE_STATE_ENABLED: if asserted, a global Pstate change to the Nap/Sleep/Winkle-Pstate is requested, when the Nap/Sleep/Winkle state is entered and the individual enable bits in the PIMCR are asserted
2	RW	ENABLE_GLOBAL_PSTATE_REQ: if '1' then enable PMC interrupt with global Pstate change request, otherwise, disable global requests
3	RW	ENABLE_WINKLE_WITH_CPM_MODE: if '1', PCBS automatically changes the DPLL mode to mode 1, when entering winkle, but changes the mode back to CPM mode when exiting. Needed for CPM-DPLL control loop enablement.
4	RW	ENABLE_CLIPPING_OF_GLOBAL_PSTATE_REQ: if '1', PCBS automatically clips global Pstate requests with Pvf_max in PPMBR and sets the 'donate' bit in the interrupt accordingly
5	RW	CHKSW_HW214553: if deasserted, HW214553 (frequin issue in resclk mode) is fixed, if asserted, the fix is not active
6	RW	ENABLE_PMC_PMAX_SYNC_NOTIFICATION: if asserted, the PCBS-PM will send a 'Pmax_sync' interrupt, once the synchronization criterion is met
7	RW	DPLL_LOCK_REPLACEMENT_TIMER_MODE_EN: Select a timer instead of the DPLL lock bit as target frequency reached criterion. This timer has to be setup by the dial dpll_lock_timer_replacement_value. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
8	RW	DPLL_FREQOUT_MODE_EN: Looks at the DPLL frequout to find out, if the target frequency has been reached. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
9	RW	DPLL_FLOCK_MODE_EN: Looks at the real DPLL flock output to find out, if the target frequency has been reached. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
10	RW	ENABLE_SENSE_DELAY_CHARACTERIZATION: If this switch is 0, the sense latches are updated every cycle. If this switch is 1, the sense delay measurement mode is enabled, that starts a sense delay timer, whenever one of the registers that drive the inputs of the iVRMs/pFETs is written via PCB and that triggers a sense register freeze operation, when the sense delay timer reaches the value sense_delay_timer_val. With this mode, the sense delays can be measured in multiples of the PCB-slave clock speed.
11:17	RW	SENSE_DELAY_TIMER_VAL: See the description of enable_sense_delay_characterization for details.
18:19	RW	CPM_FMIN_CLIP_ERROR_SEL: This dial selects, which of the following conditions will cause the FIR bit dpll_fmin_and_not_cpmbit to be set to detect, that the DPLL runs at Fmin, but is still clipped by the CPMs. 0b00 = function is disabled 0b01 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit2 = 0 0b10 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit1 = 0 0b11 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit0 = 0
20:23	RW	DBG_TRACE_SEL: This dial selects the group of signals to be traced for debug in the lab. Details to be found in the Section 'Trace Bus'



Bits	PCB	Field Mnemonic: Description
24:25	RW	TRACE_DATA_SEL: This dial selects the group of signals to be traced for debug in the lab. Details to be found in the Section 'Trace Bus'
26:29	RW	TP_CPLT_IVRM_VPP_TUNE: Tune bits to be set going to the iVRMs

Register Name	<i>PIVRMPS Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_PFETSTR_SENSE_REG
Address	00000000110F0157 (PCB)
Attributes	
Description	This PIVRMPS is used to check that the pFET sense outputs correspond to the driven values (mainly for test).

Bits	PCB	Field Mnemonic: Description
0:4	ROX	IVRM_CORE_VDD_PFETSTR_SNS: Not used any more.
5:9	ROX	IVRM_CORE_VCS_PFETSTR_SNS: This register is assigned to the signals tcex##_tp_ivrm_core_vcs_sense & tcex##_tp_ivrm_core_vdd_sense & tcex##_tp_ivrm_eco_vcs_sense & tcex##_tp_ivrm_eco_vdd_sense & 0b0
10:14	ROX	IVRM_ECO_VDD_PFETSTR_SNS: Not used any more.
15:19	ROX	IVRM_ECO_VCS_PFETSTR_SNS: Not used any more.
20	ROX	IVRM_VDD_CORE_PFETSTR_VALID_SNS: Not used any more.
21	ROX	IVRM_VCS_CORE_PFETSTR_VALID_SNS: Not used any more.
22	ROX	IVRM_VDD_ECO_PFETSTR_VALID_SNS: Not used any more.
23	ROX	IVRM_VCS_ECO_PFETSTR_VALID_SNS: Not used any more.
24	ROX	CORE_VDD_BYPASS_B_SENSE: Not used any more.
25	ROX	CORE_VCS_BYPASS_B_SENSE: Not used any more.
26	ROX	ECO_VDD_BYPASS_B_SENSE: Not used any more.
27	ROX	ECO_VCS_BYPASS_B_SENSE: Not used any more.
28	ROX	CORE_VDD_POWERON_SENSE: Not used any more.
29	ROX	CORE_VCS_POWERON_SENSE: Not used any more.
30	ROX	ECO_VDD_POWERON_SENSE: Not used any more.
31	ROX	ECO_VCS_POWERON_SENSE: Not used any more.
32	ROX	CORE_VDD_VPUMP_EN_SENSE: Not used any more.
33	ROX	CORE_VCS_VPUMP_EN_SENSE: Not used any more.
34	ROX	ECO_VDD_VPUMP_EN_SENSE: Not used any more.
35	ROX	ECO_VCS_VPUMP_EN_SENSE: Not used any more.
36	ROX	CORE_VDD_PFET_LOW_VOUT_SNS: Not used any more.
37	ROX	CORE_VCS_PFET_LOW_VOUT_SNS: Not used any more.
38	ROX	ECO_VDD_PFET_LOW_VOUT_SNS: Not used any more.
39	ROX	ECO_VCS_PFET_LOW_VOUT_SNS: Not used any more.

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Register Name	<i>PPMICR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_IDLE_CONTROL_REG
Address	00000000110F0158 (PCB)
Attributes	
Description	Used to read the PMICR register typically owned (written) by the hypervisor. Writes are conditioned on the setting of the dial Pm_spr_override_en. If Pm_spr_override_en is set, firmware needs to make sure that the special wakeup state of this chiplet is reached before changing any of the latency fields in this register. Otherwise the hardware behavior is undefined.

Bits	PCB	Field Mnemonic: Description
0:7	ROX	NAP_PSTATE_REQ: Nap Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
8	ROX	NAP_PSTATE_EN: Nap PState Enable 1 = Enable the Nap Pstate (NPS) Request, Nap Global Enable and Nap Latency functions 0 = Disables the Nap Pstate (NPS) Request, Nap Global Enable and Nap Latency functions Reads from the field return the value last written.
9	ROX	NAP_GLOBAL_EN: Nap Global Enable 1 = Upon the execution of a Nap instruction , the Nap Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a Nap instruction , the Nap Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.
10:11	ROX	NAP_LATENCY: Nap Latency not supported for POWER8 processor
12:15	ROX	RESERVED_PPMICR_0: reserved
16:23	ROX	SLEEP_PSTATE_REQ: sleep Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
24	ROX	SLEEP_PSTATE_EN: sleep PState Enable 1 = Enable the sleep Pstate (NPS) Request, sleep Global Enable and sleep Latency functions 0 = Disables the sleep Pstate (NPS) Request, sleep Global Enable and sleep Latency functions Reads from the field return the value last written.
25	ROX	SLEEP_GLOBAL_EN: sleep Global Enable 1 = Upon the execution of a sleep instruction , the sleep Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a sleep instruction , the sleep Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.



Bits	PCB	Field Mnemonic: Description
26:27	ROX	SLEEP_LATENCY: sleep Latency 00 = Cease instructions and honors Pstate change but does not perform additional state changing actions (unsupported in POWER8, maps to 0b10) 01 = Indicates to the platform that a sub-state that would have the lowest latency is enabled (unsupported in POWER8, maps to 0b10) 10 = Indicates to the platform that a sub-state that might have a medium exit latency is enabled (POWER8: Fast Sleep) 11 = Indicates to the platform that a sub-state that might have higher exit latency is enabled (POWER8: Deep Sleep)
28:31	ROX	RESERVED_PPMICR_1: reserved
32:39	ROX	WINKLE_PSTATE_REQ: winkle Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
40	ROX	WINKLE_PSTATE_EN: winkle PState Enable 1 = Enable the winkle Pstate (NPS) Request, winkle Global Enable and winkle Latency functions 0 = Disables the winkle Pstate (NPS) Request, winkle Global Enable and winkle Latency functions Reads from the field return the value last written.
41	ROX	WINKLE_GLOBAL_EN: winkle Global Enable 1 = Upon the execution of a winkle instruction , the winkle Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a winkle instruction , the winkle Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.
42:43	ROX	WINKLE_LATENCY: winkle Latency 00 = Cease instructions and honors Pstate change but does not perform additional state changing actions (unsupported in POWER8, maps to 0b10) 01 = Indicates to the platform that a sub-state that would have the lowest latency is enabled (unsupported in POWER8, maps to 0b10) 10 = Indicates to the platform that a sub-state that might have a medium exit latency is enabled (POWER8: Fast Winkle) 11 = Indicates to the platform that a sub-state that might have higher exit latency is enabled (POWER8: Deep Winkle)
44:47	ROX	RESERVED_PPMICR_2: reserved

Register Name	<i>PPMCR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_CONTROL_REG
Address	00000000110F0159 (PCB)
Attributes	
Description	The PPMCR provides read access to the PMCR register shadow in PCBS typically owned (written) by the hypervisor. Writes are conditioned on the setting of PMGP1[pm_spr_override_en].

Bits	PCB	Field Mnemonic: Description
0:7	RWX	GLOBAL_PSTATE_REQ: global Pstate request from hypervisor (or OCC)
8:15	RWX	LOCAL_PSTATE_REQ: local Pstate request from hypervisor or OCC
16	RWX	AUTO_OVERRIDE0_PSTATE_LIMIT_EN: automatic override Pstate 0 (for low activity detection) is enabled, if asserted

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Bits	PCB	Field Mnemonic: Description
17	RWX	AUTO_OVERRIDE1_PSTATE_LIMIT_EN: automatic override Pstate 1 (reserved for future use) is enabled, if asserted
18:23	RWX	RESERVED_PPMCR: reserved
24:31	RWX	AUTO_OVERRIDE_PSTATE0: automatic override Pstate 0 (for low activity detection)
32:39	RWX	AUTO_OVERRIDE_PSTATE1: automatic override Pstate 1 (reserved for future use)

Register Name	<i>Control Register That Is Written By PMC Sequencer</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_PMC_VF_CTRL_REG
Address	00000000110F015A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PGLOBAL_ACTUAL: global actual Pstate
8:15	RW	MAXREGVCS: maximum regulation point for Vcs, Bit 0 is reserved, bits 1 to 7 are in iVID format
16:23	RW	MAXREGVDD: maximum regulation point for Vdd, Bit 0 is reserved, bits 1 to 7 are in iVID format
24:31	RW	EVIDVCS_EFF: eff. external voltage ID for Vcs in iVID format, Bit 0 is reserved
32:39	RW	EVIDVDD_EFF: eff. external voltage ID for Vdd in iVID format, Bit 0 is reserved

Register Name	<i>Undervolting Register For PCBS</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_UNDERVOLTING_REG
Address	00000000110F015B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PUV_MIN: minimum Pstate for which undervolting is allowed
8:15	RW	PUV_MAX: maximum Pstate for which undervolting is allowed
16:21	RW	KUV: this value indicates how many Pstate ticks a voltage request is undervolted (clipped with Puv_min). Note that the Kuv value is signed

Register Name	<i>PPSIBR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_INDEX_BOUND_REG
Address	00000000110F015C (PCB)
Attributes	
Description	The PPSIBR enables setting the minimum and maximum Pstate that is supported as a pointer into the local Pstate table (which has entries from 0 to 127).

Bits	PCB	Field Mnemonic: Description
0:7	RW	LPSI_MIN: this Pstate index is the index that corresponds to array entry 0. Note that the index domain is obtained by adding 128 to a Pstate, thus, the value is unsigned.
8:14	RW	LPSI_ENTRIES_MINUS_1: this dial contains the value of the number of entries in the Pstate table minus 1

Register Name	<i>PPMBR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_BOUNDS_REG
Address	00000000110F015D (PCB)
Attributes	
Description	The PPMBR enables setting the Pstate bounds that are managed by the OCC. If Dial Enable_pmc_pmax_sync_notification is set, firmware must wait after each write to this register until PMC has received the Pmax Sync Interrupt. If a write happens to this register, while the previously scheduled Pmax Sync Interrupt has not yet left PCBS, the error TBD will be set.

Bits	PCB	Field Mnemonic: Description
0:7	RW	PMIN_CLIP: minimum Pstate allowed for this chiplet
8:15	RW	PMAX_CLIP: maximum Pstate allowed for this chiplet (has to be greater or equal to Pmin_clip)

Register Name	<i>PPTCR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_CTRL_REG
Address	00000000110F015E (PCB)
Attributes	
Description	The PPTCR controls the address for writing the local Pstate table array (all 96 words are accessible). Note that the protocol requires this register to be set up with the Pstate address first, if a read or a write of the Pstate array is intended, to make sure that the initial address is set correctly. The register PPTR must always be written or read afterward. Note that any access to the PPTR auto-increments this register.

Bits	PCB	Field Mnemonic: Description
0:6	RWX	PSTATE_TABLE_ADDRESS: This is the address of the Pstate table in PCBS, which is auto-incremented after any access to the PTLR.

Register Name	<i>PPTR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_REG
Address	00000000110F015F (PCB)
Attributes	
Description	The PPTR controls the data to be written into the Pstate table and returns the data for a read of the Pstate table. Note that the protocol requires for a write to set this register up after setting up pptcr first (if the user does not rely on the auto-increment function of the address). For a read of the pstate table, this register must be read after setting up PPTCR first as well (again if the auto-increment feature of the address is not used). Any access to this register auto-increments the pstate_table_address by 1. Note also that the read functionality of this register is only functional if PIVRMCSR[ivrm_fsm_enable] = 0. The write functionality works in any case.

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Bits	PCB	Field Mnemonic: Description
0:63	RW	pstate_data This is the field for data bits 0 to 63

Register Name	PPSTR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_STEP_TARGET_REG
Address	00000000110F0160 (PCB)
Attributes	
Description	The PPSTR provides read access to several intermediate values in the Pstate computation pipeline. Writes are conditioned on the setting of PMGP0[enable_OCC_ctrl_for_local_Pstate_eff_req].

Bits	PCB	Field Mnemonic: Description
0:7	RWX	LOCAL_PSTATE_EFF_REQ: this field represents the effective local Pstate request right before the clipping with Pmin and Pmax if enable_OCC_ctrl_for_local_Pstate_eff_req=0 then the hardware controls this dial, that updates every cycle if enable_OCC_ctrl_for_local_Pstate_eff_req=1 then OCC is in control and can write this field to control the effective local Pstate request that will eventually propagate through the downstream logic and determine the Local PState Actual. Note: if no write to this register is performed, the currently established value is maintained stable forever.
8:15	ROX	LOCAL_PSTATE_TARGET: This field is the target Pstate of a complete Pstate change that is performed in smaller steps
16:23	ROX	LOCAL_CORE_PSTATE_STEP_TARGET: this field represents the intermediate value that is about to be established as the next Local Pstate Actual after completing one step in the process of the transition towards the 'local_Pstate_target' the new voltage, frequency, and clock resonance setting
24:31	ROX	LOCAL_ECO_PSTATE_STEP_TARGET: this field represents the intermediate value that is about to be established as the next Local Pstate Actual after completing one step in the process of the transition towards the 'local_Pstate_target' the new voltage, frequency, and clock resonance setting

Register Name	Read-Only Status Register For DPLL And For Debugging (PDSR)
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_DPLL_STATUS_REG
Address	00000000110F0161 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:14	ROX	DPLL_FF_FREQOUT: frequout output from DPLL (current frequency - bits 2 to 10 correspond to the same scale as the 9 bits of frequin (which need to be multiplied with our frequency step to get the real frequency), the remaining bits just provide a higher accuracy)
15	ROX	DPLL_FREQU_CHANGE: DPLL Frequency change (pin of DPLL without filter)
16	ROX	DPLL_STATUS_SPARE_BIT1: Spare bit.
17	ROX	PMAX_SYNC_PENDING: gets asserted, if the logic has a Pmax sync interrupt outstanding that will be eventually sent to PMC when the Pmax sync criterion is met
18	ROX	GA_ACK_PENDING: gets asserted, if the logic has a global actual Pstate update acknowledgment interrupt outstanding that will be eventually sent to PMC when the GA ack criterion is met
19:26	ROX	CAPPED_GLOBAL_PSTATE_REQ: corresponds to the capped global Pstate request that is presented as Pstate interrupt and send to PMC



Bits	PCB	Field Mnemonic: Description
27	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT2: DPLL runs at Fmax and CPM bit 2 is set. Note that this bit and the following 2 bits indicate, that the CPMs would allow the DPLL to run faster than Fmax.
28	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT3: DPLL runs at Fmax and CPM bit 3 is set
29	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT4: DPLL runs at Fmax and CPM bit 4 is set
30	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT2: DPLL runs at Fmin and CPM bit2 is zero. Note that this bit and the following 2 bits indicate, that the CPMs indicate, that the DPLL should run slower than the currently established Fmin.
31	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT1: DPLL runs at Fmin and CPM bit1 is zero
32	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT0: DPLL runs at Fmin and CPM bit0 is zero
33	ROX_CLRPAR T	DPLL_FASTER_THAN_FMAX_PLUS_DELTA1: The DPLL indicated that it ran once faster than Fmax+dpll_char_delta1
34	ROX_CLRPAR T	DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2: The DPLL indicated that it ran once slower than Fmin-dpll_char_delta2
35:48	ROX	DPLL_MAX_FREQOUT_AFTER_LAST_READ: This dial indicates the maximum DPLL frequout value after the last read of this register (only 14 MSBs)
49:62	ROX	DPLL_MIN_FREQOUT_AFTER_LAST_READ: This dial indicates the minimum DPLL frequout value after the last read of this register (only 14 MSBs)

Register Name	<i>The PIVRMVCR0 Controls The Voltage Stepping Delays</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG0
Address	00000000110F0162 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	IVRM_REQ_PSTATE_STEPDELAY_RISING: Requested Internal Pstate Baby Step Delay - Rising Step. Delay before allowing the next step for a rising Pstate Transition. This dial and ivrm_req_Pstate_stepdelay_lowering allow for differing delays for the two directional transitions if necessary. In 100ns units as established by scan dial ivrm_100ns_value
8:15	RW	IVRM_REQ_PSTATE_STEPDELAY_LOWERING: Requested Internal Pstate Baby Step Delay - Lowering Step. Delay before allowing the next step for a lower Pstate Transition. This dial and ivrm_req_Pstate_stepdelay_rising allow for differing delays for the two directional transitions if necessary. In 100ns units as established by scan dial ivrm_100ns_value

Register Name	<i>The PIVRMVCR1 Controls The Voltage Stepping Delays</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG1
Address	00000000110F0163 (PCB)
Attributes	
Description	

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Bits	PCB	Field Mnemonic: Description
0:7	RW	IVRM_STABILIZE_DELAY_RUN: Stabilization Delay - Run Time Delay to allow a rail to stabilize upon a baby step while the region is operational. In 100ns units as established by scan dial ivrm_100ns_value
8:15	RW	IVRM_STABILIZE_DELAY_IDLE: Stabilization Delay - Idle Transition Delay to allow a rail to stabilize upon a baby step during an idle transition where the activity in the region is quiesced. In 100ns units as established by scan dial ivrm_100ns_value
16:23	RW	IVRM_PFSTR_PROP_DELAY: PFET Strength Propagation Delay Time from PFET Strength values being launched till PFET Strength Valid is asserted. In order to ensure like rails across domains (Core VDD<>ECO VDD, Core VCS<>ECO VCS) are in sync during operational mode, this time value applies to all rails across the domains. This parameter allows for PFET Strength values to settle before PFET Strength Valid is sampled in the Uregs. The value set must the maximum delay for the worst rail timing and must allow for any metastability settling (for example, normally 2-3 cycles for single signals in an asynch handshake interface)
24:31	RW	IVRM_PFSTRVALID_PROP_DELAY: PFETStrength Valid Propagation Delay Time from ivrm_pfstr_prop_delay expiring to where PFET Strength Valid is deasserted. The value is the maximum of a) the minimum pulse width required for PFETStrength Valid and b) the propagation of PFETStrength Valid through (or enough of) the daisy chain. In order to ensure like rails across domains (Core VDD<>ECO VDD, Core VCS<>ECO VCS) are in sync during operational mode, this time value applies to all rails across the domains and thus must be the set to the value of the worst (slowest) rail. The minimum pulse width cannot be violated. The propagation delay can be tuned for more aggressive timing (for example, deassert before the actual propagation is complete). Measured in prv_nclk cycles. The min delay is 2 cycles. Additional delay can be configured with the following settings. 0x00 = No additional delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_clinks
32:39	RW	IVRM_VPUMP_POWERON_TIME: iVRM (VRreg and UReg) - Vpump Power On Time Time necessary for the distributed internal VRM macro circuits to power on. Same delay is required for power on voltage pump circuit. Both delays are in the 8us range. In 100ns units as established by scan dial ivrm_100ns_value
40:47	RW	IVRM_BYPASS_DELAY: iVRM Bypass Propagation Delay Delay time for bypass_b signal propagation. Measured in prv_nclk cycles Target: 50ns 0x00 = No delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks
48:55	RW	PFET_VPUMP_ENABLE_DELAY: PFET and Vpump Enable Propagation Delay Delay time for PFET enable and vpump enable signal propagation. Target: 130ns Measured in prv_nclk cycles 0x00 = No delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks
56:62	RW	IVRM_VID_VOUT_THRESHOLD: VID threshold If the output voltage (Vout) is targeting a value below this threshold the slow PFET can backed off from its normal drive strength so as to reduce the ripple at these lower voltage conditions

Register Name	POHR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_OCC_HEARTBEAT_REG
Address	00000000110F0164 (PCB)
Attributes	
Description	Controls the behavior of the OCC heartbeat function.

Bits	PCB	Field Mnemonic: Description
0:7	RW	occ_heartbeat_time 'OCC Heartbeat Time Value' " 'This field defines the number of ~64us hang timer pulses in which a a PCB read or write of the heartbeat trigger register (of which the offset is specified by dial occ_heartbeat_reg_addr_offset) is not detected that will constitute the loss of the OCC heartbeat. If occ_heartbeat_en is set and upon this loss detection, POHBR[psafe] is forced and, if enabled, the error TBD is activated ' " '0x00 - unsupported, causes undefined behavior' '0x01 - 64us +0/-1us' '0x02 - 128us +0/-1us' '...' '0xFF - 16320us +0/-1us 16.3ms' " 'Upon the 64us hang pulse, the decremter ticks. if the decremter reaches x00, the heartbeat loss event is triggered.' " '
8	RW	occ_heartbeat_enable 'OCC Heartbeat Timer Enable' " '0 = Disable the OCC Heartbeat function. Lack of accesses to the register defined by the dial occ_heartbeat_reg_addr_offset does not result in heartbeat loss events to be triggered (no FIRs set nor Safe mode entry).' " '1 = Enable the OCC Heartbeat function. '
9:16	RW	occ_heartbeat_reg_addr_offset This dial allows to configure the address offset within the PCBS power management entity of the register, that will regularly reset the heartbeat timer (which is called heartbeat trigger register). The address offset is 0x100 plus the value of this dial.
17:24	RW	Psafe 'Pstate Safe' " 'This field establishes the Pstate that the core chiplet will take on if: 'psafe <= PMSR[global_actual_pstate]' 'AND any of the following conditions are true:' 'Loss of OCC Heartbeat if occ_heartbeat_en is set' 'PMGPO[force_safe_mode] is set' " 'If psafe > PMSR[global_actual_pstate], the global_actual_pstate is forced.' " 'The value of Psafe needs to be at or below the nominal Pstate to make sure safe operation of all chiplets. '

Register Name	PRCCR0 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG 0
Address	00000000110F0165 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function.

Bits	PCB	Field Mnemonic: Description
0	ROX	RESCLK_DIS: Resonant Clock Enable Master enable of all resonant clocking functions. This dial can be set by setting GP3(22) and can not be set in this PCBS_resonant_Clock_Control_Reg0. 1 = Resonant Clock function is disabled. Default values (0) for resclk_value, resclk_core_sync_value, csb_eco_sync_value 0 = Resonant Clock Control hardware is enabled (the mode is defined by dial resclk_control_mode)

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Bits	PCB	Field Mnemonic: Description
1	RW	RESCLK_CONTROL_MODE: Resonant Clock Control Mode Defines the control means enabled when resclk_dis is not set. 0 = Pstate band hardware mechanism enabled 1 = Manual mode enabled (Firmware mode) If this bit is set to 0, the hardware control mechanism that manages the transition across the Resonant Bands is enabled. If this bit is set to 1, the automatic Pstate band hardware mechanism is disabled and the Firmware is in control of all values of the dial resclk_value, resclk_core_sync_value, csb_eco_sync_value. Firmware must ensure that frequency changes will not cross resonant bands or machine failures may result. resclk_value represents the values for clock sector buffer strength, inductor switch strength and high inductor enable. Firmware must ensure the correct stepping in/out the different bands and propagation of the values (resclk_value) to the core/eco (resclk_core_sync_value / csb_eco_sync_value).
2:4	RW	RESCLK_SYNC_PW: Resonant Clock Sync Pulse Width Number of nest/4 cycles to assert the clock sync signal. This value must be high enough to ensure capture and propagation across the asynchronous chiplet boundary.
5:11	RW	RES_SYNC_DELAY_CNT: Resonant Clock Sync Delay Number of nest/4 cycles wait after the launch of the resclk_value (csb and inductor) before launching the sync to allow these to be captured. This value must be high enough to ensure full propagation to the input of the clock sector buffers and inductor switches.
12:26	RW	RES_CSB_STR_INSTR_LO: Resonant Clock Sector Buffer Strength Instruction - Low Band Mask value that determines whether, during a fixed 15 step sequence, the res_csb_str(0:3) is to be decremented/incremented in entering/exiting the Low Band. During resonant clock Entry, res_csb_str(0:3) decremented by the value pattern from 0 down to 14. During resonant clock Exit, res_csb_str(0:3) incremented by the value pattern from 14 up to 0.
27:41	RW	RES_CSB_STR_INSTR_HI: Resonant Clock Sector Buffer Strength Instruction - High Band Mask value that determines whether, during a fixed 15 step sequence, the res_csb_str(0:3) is to be decremented/incremented in entering/exiting the High Band. During resonant clock Entry, res_csb_str(0:3) decremented by the value pattern from 0 down to 14. During resonant clock Exit, res_csb_str(0:3) incremented by the value pattern from 14 up to 0.

Register Name	PRCCR1 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG 1
Address	00000000110F0166 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function. Writes are conditioned.

Bits	PCB	Field Mnemonic: Description
0:7	RW	FULL_CSB_PS: Full Clock Sector Buffer Pstate Pstate defining the maximum point where the clock sector buffer must be driven to full strength. This allow clocks to be distributed at low Vmin levels. FW needs to make sure that no overlaps occur with bands 2 or 3.
8:15	RW	RES_LOW_LOWER_PS: Low Frequency Resonant Lower (LFRLow) Pstate Pstate defining the lower frequency of the Low Resonant Frequency Band. FW needs to make sure that no overlap occurs with band 0.
16:23	RW	RES_LOW_UPPER_PS: Low Frequency Resonant Upper (LFRUpper) Pstate Pstate defining the upper frequency of the Low Resonant Frequency Band. Note that if an overlap occurs with band 3, the hardware behavior is undefined.
24:31	RW	RES_HIGH_LOWER_PS: High Frequency Resonant Lower (HFRLow) Pstate Pstate defining the lower frequency of the High Resonant Frequency Band. Note that if an overlap occurs with band 2, the hardware behavior is undefined.

Bits	PCB	Field Mnemonic: Description
32:39	RW	RES_HIGH_UPPER_PS: High Frequency Resonant Upper (LFRUpper) Pstate Pstate defining the upper frequency of the High Resonant Frequency Band. This value needs to be greater or equal to high_res_lower_ps.
40:43	RW	NONRES_CSB_VALUE_TI: Clock Sector Buffer Table Index for non-resonant state Table Index into Clock Sector Buffer Table for the nominal, non-resonant state.
44:47	RW	FULL_CSB_VALUE_TI: Clock Sector Buffer Table Index for full CSB value Table Index into Clock Sector Buffer Table for the full CSB strength value.
48:56	RWX	RESCLK_VALUE: Output register driving the 9 bit resclk_value In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current resclk_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. The value in this register represents the following concatenation: csb_str_value(0:3) sw_str(0:3) hi_induct_en.
57	RWX	RESCLK_CORE_SYNC_VALUE: Output register driving the resclk_core_sync signal In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current resclk_core_sync_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. This bit is supposed to be used in order to create a SCOM-controlled pulse to force an update of the resclk propagation registers. A 1 enables the synchronous update, a 0 disables it. Suggested use of this bit is to set it to 1 and then set it back to 0 to create a (long) update pulse.
58	RWX	CSB_ECO_SYNC_VALUE: Output register driving the csb_eco_sync signal In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current csb_eco_sync_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. This bit is supposed to be used in order enable the ECO domain to participate in clock sector buffer strength changes, when switching from nominal strength to full CSB strength. A 1 enables the ECO domain, a 0 disables it from seeing a CSB strength update.

Register Name	PRCCR1 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_STATUS_REG
Address	00000000110F0167 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function.

Bits	PCB	Field Mnemonic: Description
0	ROX	RESCLK_STATE: Resonant Clock State 0 = Resonant Clocking inactive 1 = Resonant Clocking active Valid if resclk_inprogress = 0. Hardware sets this bit to the right value at the completion of the transition into and out of resonance mode.

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Bits	PCB	Field Mnemonic: Description
1	ROX	RES_HI_INDUCT_EN: Resonant High Inductor Enable Valid if resclk_inprogress = 0. This dial provides the current value being propagated. 0 = Resonant Clock mode not active 1 = Resonant Clock mode active
2	ROX	RESCLK_INPROGRESS: Resonant Clock Transition in Progress This bit is set by hardware while a transition is in progress and will be reset by hardware when the operation is complete.
3	ROX	RESCLK_FULL_CSB: Full CSB Clock State 0 = Full CSB Clocking inactive 1 = Full CSB Clocking active Valid if resclk_inprogress = 0. Hardware sets this bit to the right value at the completion of the transition into and out of full CSB mode respectively.

Register Name	<i>PLPFTCR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_CONTROL_REG
Address	00000000110F0168 (PCB)
Attributes	
Description	The PLPFTCR enables firmware to configure the modes that are used for the PCBS Local Pstate Frequency Target Status Register.

Bits	PCB	Field Mnemonic: Description
0:2	RW	DELAY_TIME: This field encodes the delay between the time a Local Actual Pstate change modifies the input to the DPLL and the time frequency acquisition begins to allow the hardware to ignore the frequency transition of the DPLL in order to get better frequency measurements. This field encodes a delay of ~1us to ~128us in power of 2 selects. The delay is defined by $2^{\text{delay\_time}}$ in us. Note that the hardware uses multiples of the slow hang pulse that is running at 1us.
3	RW	RECORD_TRANSITIONS: This bit indicates whether the LPFTSR records events that correspond to Local Actual Pstate changes (and therefore may include DPLL slewing effects.) One usage model would set the periodic sample_time defined by the dial OHA_MODE_REG[tod_pulse_count_match_val] to a time less than the worst-case DPLL slew time but then ignore Pstate transitions because they might include DPLL slew effects.
4:18	RW	MULTIPLIER: This 15-bit unsigned constant is multiplied by the DPLL frequency code (9 bits) implied by the Local Actual Pstate to yield the 24-bit frequency target measured in PCBS-PM clock cycles (core clock / 2). Assuming times in seconds and frequencies in Hz, firmware should set this constant to: $(\text{DPLL\_Frequency\_Code\_Step\_Hz} * \text{Sample\_Time\_Seconds}) / 2$
19	RW	ENABLE_LPFT_FUNCTION: This is the enable bit to enable the local Pstate frequency target function. A '1' enables the function, a '0' disables it (the value can be changed at any time).

Register Name	<i>PLPFTSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_STATUS_REG
Address	00000000110F0169 (PCB)
Attributes	
Description	Allows firmware to observe local actual Pstate realized frequencies.

Bits	PCB	Field Mnemonic: Description
0	ROX_CLRPART	VALID: If this bit is set then all of the remaining fields of this register are valid. This bit is cleared whenever the register is read or after a local actual Pstate change occurs, and is will be set whenever the hardware completes a valid sample. If firmware reads this register and the valid bit is not set, then it indicates that the Local Pstate target frequency acquisition logic has not been able to complete a frequency acquisition for any Local Actual Pstate change since the last time the LPFTSR was read. This could be due to either of the following factors: 1. Firmware is sampling the LPFTSR faster than the time implied by the sample time defined in OHA by the dial OHA_MODE_REG[tod_pulse_count_match_val] field
1	ROX	CPM_DPLL: If the valid bit is set, then if cpm_dpll is set it indicates that the event recorded by this register was due to a Local Actual Pstate implemented by the DPLL running in CPM-DPLL mode, otherwise the value of this bit is undefined. If the valid bit is not set, this bit is undefined.
2	ROX	IVRM: If the valid bit is set, then if ivrm is set it indicates that the event recorded by this register was due to a Local Actual Pstate whose voltage was set locally by the iVRM operating entirely in regulation mode. If the valid bit is not set, this bit is undefined.
3	ROX	TRANSITION: If the valid bit is set, then if transition is set it indicates that during the observation period a Local Pstate Actual change has occurred, and any performance delta may be due to DPLL frequency slewing. If the valid bit is not set, this bit is undefined
4	ROX	STABLE: If stable is set it indicates that the DPLL input frequency has been stable since the last time the PLPFTSR was read. This bit is set whenever the PLPFTSR is read, and cleared whenever the Fmax input of the DPLL changes. This bit is always valid, regardless of the state of the valid bit. If the PLPFTSR is read on the same cycle a frequency changes then the stable bit is cleared. This bit helps firmware better understand how to interpret the information contained in the PLPFTSR. (Note that this bit should have an attribute ROX_SETPART, but this is not supported by regchk.)
5:28	ROX	DELTA: If the valid bit is set then this is the 24-bit signed difference Measured Cycles - Target Cycles for the event captured by this register. If the valid bit is not set, this dial is undefined.
29:52	ROX	CUMULATIVE: This field records the 24-bit cumulative (signed) delta for all valid samples taken since this field was cleared. Writing any value to this register clears this field. Note that it should have an attribute WOX_CLRPART, but this is not supported by regchk/figtree.
53:60	ROX	PSTATE: If the valid bit is set then this is the Local Actual Pstate of the frequency acquisition that had the minimum (signed) delta of any valid sample taken since the last time the LPFTSR was read. If the valid bit is not set, then this field is undefined.

Register Name	PFSMM1/2 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR1_REG
Address	00000000110F0170 (PCB)
Attributes	
Description	The PFSMM1/2 facilitates debug by providing insight into the internal FSM states of the PCB-slave power-management unit. For expert use only. Coding according to VHDL design.

Bits	PCB	Field Mnemonic: Description
0:6	ROX	BABYSTEP_MAIN_FSM: Main Babystep FSM (mfsm_lt)
7:11	ROX	BABYSTEP_SLAVE_FSM: Babystep Slave FSM (sfsm_lt)
12:16	ROX	CORE_RAILSTEPPER_MAIN_FSM: Main Core Railstepper FSM (mrsfsm_lt)
17:21	ROX	ECO_RAILSTEPPER_MAIN_FSM: Main ECO Railstepper FSM (mrsfsm_lt)

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Bits	PCB	Field Mnemonic: Description
22:25	ROX	CORE_RAILSTEPPER_SUB_FSM: Core Railstepper Sub-FSM (srsfsm_lt)
26:29	ROX	ECO_RAILSTEPPER_SUB_FSM: ECO Railstepper Sub-FSM (srsfsm_lt)
30:34	ROX	CORE_RAILSTEPPER_BYP_FSM: Core Railstepper Bypass FSM (byp_fsm_lt)
35:39	ROX	ECO_RAILSTEPPER_BYP_FSM: ECO Railstepper Bypass FSM (byp_fsm_lt)
40:45	ROX	IVRM_CORE_VDD_SEQUENCER_FSM: Core iVRM Sequencer for Vdd (ivrm_fsm_lt)
46:51	ROX	IVRM_CORE_VCS_SEQUENCER_FSM: Core iVRM Sequencer for Vcs (ivrm_fsm_lt)
52:57	ROX	IVRM_ECO_VDD_SEQUENCER_FSM: ECO iVRM Sequencer for Vdd (ivrm_fsm_lt)
58:63	ROX	IVRM_ECO_VCS_SEQUENCER_FSM: ECO iVRM Sequencer for Vcs (ivrm_fsm_lt)

Register Name	<i>Refer To The Description Of PFSMM1.</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR2_REG
Address	00000000110F0171 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:6	ROX	RESCLK_BAND_FSM: Band Sequencer for resonant clocking (band_fsm_lt)
7:10	ROX	RESCLK_LOWRES_FSM: Low Resonant Clocking sequencer (lowres_fsm_lt)
11:14	ROX	RESCLK_HIGHRES_FSM: High Resonant Clocking sequencer (highres_fsm_lt)
15:18	ROX	RESCLK_FULLCSB_FSM: Full-CSB Resonant Clocking sequencer (fullcsb_fsm_lt)
19:22	ROX	RESCLK_UPDATE_FSM: Resonant Clocking Update sequencer (update_fsm_lt)
23:29	ROX	IDLE_TRANSITION_FSM: Idle State Sequence FSM (ifsm_lt)
30:37	ROX	Peco_step_target_uv Current ECO Step Target Pstate (different from Plocal_actual for undervolting)
38:45	ROX	Pcore_step_target_uv Current core Step Target Pstate (different from Plocal_actual for sleep and undervolting)

Register Name	<i>Protect Mode Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.PROTECT_MODE_REG
Address	00000000110F03FE (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	READ_PROTECT_ENABLE: Enable read protection
1	RW	WRITE_PROTECT_ENABLE: Enable write protection

Register Name	<i>Atomic Lock Register</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX01.TP_PCB_SLAVE_INST.ATOMIC_LOCK_REG	
Address	00000000110F03FF (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	RW	ATOMIC_LOCK_ENABLE: Enable atomic lock
1:4	ROX	ATOMIC_ID: Atomic ID

Register Name	<i>Contains The Slave's Primary Address</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.PRIMARY_ADDRESS_REG	
Address	00000000120F0000 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RO	Reserved field (Access type is primary_address)

Register Name	<i>Multicast Group 1</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.MULTICAST_GROUP_1	
Address	00000000120F0001 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST1_GROUP: multicast group1 setting

Register Name	<i>Multicast Group 2</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.MULTICAST_GROUP_2	
Address	00000000120F0002 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST2_GROUP: multicast group2 setting

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Register Name	<i>Multicast Group 3</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.MULTICAST_GROUP_3
Address	00000000120F0003 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST3_GROUP: multicast group3 setting

Register Name	<i>Multicast Group 4</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.MULTICAST_GROUP_4
Address	00000000120F0004 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST4_GROUP: multicast group4 setting

Register Name	<i>Timeout Select Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.TIMEOUT_REG
Address	00000000120F0010 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	Reserved field (Access type is int_timeout)

Register Name	<i>Assist Interrupt Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.ASSIST_INTERRUPT_REG
Address	00000000120F0011 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is attn)
1	ROX	Reserved field (Access type is recov)
2	ROX	Reserved field (Access type is xstop)



Register Name	GP3 Register (NA In PERV CPLT)
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.GP3_REG
Address	00000000120F0012 (PCB) 00000000120F0013 (PCB1) 00000000120F0014 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset
2	RWX	RWX_WAND	RWX_WOR	GLSMUX_RESET: Glsmux reset for test purpose and stuck active mesh protection. Notice no clocks in the EX if this bit is set.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Put the DPLL in test mode.
4	RWX	RWX_WAND	RWX_WOR	PLL_RST: Put PLL in reset state.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYP: Enable PLL bypass.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pcb_access)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	PM_PI_DECODE: Test override for power management. EX chiplet only.
22	RWX	RWX_WAND	RWX_WOR	RESCLK_DIS: Resonant clocking disable.
23:25	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave will report 'Chiplet Offline'.
27	RWX	RWX_WAND	RWX_WOR	TP_LVLTRANS_FENCE: Electrical winkel fence. Mainly used by power management.
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.
29:31	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)

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Register Name	<i>Skew Adjust Data</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.CLK_ADJ_REG
Address	00000000120F0015 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:15	ROX	

Register Name	<i>Clk Ajust Config</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.CLK_ADJ_SET
Address	00000000120F0016 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:31	RW	CLK_ADJ_SET_REG: Clk adj config

Register Name	<i>Vital Scan Out</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.VITAL_SCAN_OUT
Address	00000000120F0017 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	

Register Name	<i>Chiplet Heartbeat Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.HEARTBEAT_REG
Address	00000000120F0018 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	HEARTBEAT_DEAD: Chiplet heartbeat not detected



Register Name	<i>Lock Indications From PLLs</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.PLL_LOCK_REG	
Address	00000000120F0019 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:3	ROX	Reserved field (Access type is lock)

Register Name	<i>Attn Interrupt</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.ATTN_INTERRUPT_REG	
Address	00000000120F001A (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is attn)

Register Name	<i>Recov Interrupt</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.RECOV_INTERRUPT_REG	
Address	00000000120F001B (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is recov)

Register Name	<i>Xstop Interrupt</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.XSTOP_INTERRUPT_REG	
Address	00000000120F001C (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is xstop)

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Register Name	<i>Slave Config Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.SLAVE_CONFIG_REG
Address	00000000120F001E (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	CFG_DISABLE_PERV_THOLD_CHECK: Disable pervasive thold check
1	RW	CFG_DISABLE_MALF_PULSE_GEN: Disable pulse generation for malf alert. Switch back to level
2	RW	CFG_STOP_HANG_CNT_SYS_XSTP: Disable hang counter stop for system xstop
3	RW	CFG_DISABLE_CL_ATOMIC_LOCK: Disable atomic lock for chiplet accesses
4	RW	CFG_DISABLE_HEARTBEAT: Disable check for voltage and gridclock in the chiplet
5	RW	CFG_ZERO_DATA: Sent zero data on any error
6:7	RW	
8:12	RW	ERROR_MASK: mask bits for slave error reporting
13:15	RW	

Register Name	<i>Error Capture Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.ERROR_REG
Address	00000000120F001F (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX_WCLEA R	CE_ERROR: Correctable error on pcb bus
1:3	RWX_WCLEA R	CHIPLET_ERRORS: Errors reported by chiplet 000 = no error 001 = XSCOM command blocked due pending errors 010 chiplet offline 011 partial good 100 invalid address / address error / bad access type 101 clock error 110 parity error / received unexpected packet / wrong packet number 111 timeout This register is for debug purposes only. It only holds meaningful data if it is cleared after each error.
4	RWX_WCLEA R	PARITY_ERROR: Parity error on PCB Interface
5	RWX_WCLEA R	DATA_BUFFER_ERROR: Parity error in data buffer
6	RWX_WCLEA R	ADDR_BUFFER_ERROR: Parity error in address buffer
7	RWX_WCLEA R	PCB_FSM_ERROR: Invalid state error in PCB FSM
8	RWX_WCLEA R	CL_FSM_ERROR: Invalid state error in Chiplet FSM
9	RWX_WCLEA R	INT_RX_FSM_ERROR: Invalid state error in interrupt RX FSM
10	RWX_WCLEA R	INT_TX_FSM_ERROR: Invalid state error in interrupt TX FSM



Bits	PCB	Field Mnemonic: Description
11	RWX_WCLEAR	INT_TYPE_ERROR: Invalid interrupt type
12	RWX_WCLEAR	CL_DATA_ERROR: Parity error on Chiplet Interface
13	RWX_WCLEAR	INFO_ERROR: Parity error on Chiplet info lines
14	RWX_WCLEAR	UNUSED_0:
15	RWX_WCLEAR	CHIPLET_ATOMIC_LOCK_ERROR: Chiplet atomic lock error
16	RWX_WCLEAR	PCB_INTERFACE_ERROR: Error of pcb interface component for the internal endpoint
17	RWX_WCLEAR	CHIPLET_OFFLINE: Heartbeat check indicated that chiplet is offline
18	RWX_WCLEAR	CHIPLET_GRID_SKITTER: Heartbeat check indicated skitter on the chiplet grid
19	RWX_WCLEAR	GP3_REG_PARITY_ERROR: gp3 register parity bad
20	RWX_WCLEAR	ADDRESS_REG_PARITY_ERROR: address register parity bad
21	RWX_WCLEAR	TIMEOUT_REG_PARITY_ERROR: timeout select register parity bad
22	RWX_WCLEAR	CONFIG_REG_PARITY_ERROR: slave config register parity bad
23	RWX_WCLEAR	CLK_ADJ_REG_PARITY_ERROR: clk adj register parity bad
24	RWX_WCLEAR	DIV_REG_PARITY_ERROR: div register parity bad
25:28	RWX_WCLEAR	PLL_UNLOCK_ERROR: unlock from chiplet pll

Register Name		<i>Hang Pulse Generation Register 0.</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.HANG_PULSE_0_REG
Address		00000000120F0020 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_0: Value of hang pulse 0. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_0: If set to '1', hang pulses are suppressed in case of a xstop

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Register Name	<i>Hang Pulse Generation Register 1.</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.HANG_PULSE_1_REG
Address	00000000120F0021 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_1: Value of hang pulse 1. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_1: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 2.</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.HANG_PULSE_2_REG
Address	00000000120F0022 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_2: Value of hang pulse 2. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_2: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 3.</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.HANG_PULSE_3_REG
Address	00000000120F0023 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_3: Value of hang pulse 3. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_3: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 4.</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.HANG_PULSE_4_REG
Address	00000000120F0024 (PCB)
Attributes	
Description	



Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_4: Value of hang pulse 4. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_4: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 5</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.HANG_PULSE_5_REG
Address	00000000120F0025 (PCB)
Attributes	
Description	This hang counter is exclusively used to generate the malfunction alert pulse.

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_5: Value of hang pulse 5. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_5: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 6</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.HANG_PULSE_6_REG
Address	00000000120F0026 (PCB)
Attributes	
Description	This hang counter is exclusively used for heartbeat generation..

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_6: Value of hang pulse 6. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_6: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Divider For Hang Counter Clock</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.PRE_COUNTER_REG
Address	00000000120F0028 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PRE_COUNTER: Divider for hang counter clock. Divides clock by n+1 (default: n=0)

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Register Name		PowerManagement GP0		
Mnemonic		EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PMGP0_REG		
Address		00000000120F0100 (PCB) 00000000120F0101 (PCB1) 00000000120F0102 (PCB2)		
Attributes				
Description				
Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PM_DISABLE: Master Switch for the PowerManagement Macro
1	RWX	WOX_AND	WOX_OR	PMGP0_SPARE_BIT1: spare bit
2	RWX	WOX_AND	WOX_OR	TP_TC_RESTART_CORE_DOMAIN: Kicks off small sequencer in OHA to get chiplet clocks back running for fast sleep without involving PORE. From GP-reg and overridden by PowMan State Machine.
3	RWX	WOX_AND	WOX_OR	DPLL_THOLD: Thold for the DPLL clock domain in the chiplet
4	RWX	WOX_AND	WOX_OR	PERV_THOLD: Thold for the Pervasive clock domain in the chiplet
5	RO	RO	RO	Reserved.
6	RO	RO	RO	Reserved.
7	RWX	WOX_AND	WOX_OR	PM_DPLL_TIMER_ENA: Select a timer instead of the DPLL lock bit for criteria to switch to DPLL. The time is defined by thold_timer_sel.
8	RWX	WOX_AND	WOX_OR	DPLL_LOCK_SENSE: DPLL lock sensitivity control (0=faster lock time, 1=slower lock time)
9	RWX	WOX_AND	WOX_OR	PMGP0_SPARE2: spare bit
10	RWX	WOX_AND	WOX_OR	DPLL_RESET: Reset to DPLL
11	RWX	WOX_AND	WOX_OR	PMGP0_SPARE_BIT11: Spare bit
12:19	RWX	WOX_AND	WOX_OR	DPLL_TESTOUT_CTL: DPLL testout control
20	RWX	WOX_AND	WOX_OR	TP_TC_CACHE2CORE_FENCE: Fence from cache to core domain in EX chiplet
21	RWX	WOX_AND	WOX_OR	TP_TC_CORE2CACHE_FENCE: Fence from core to cache domain in EX chiplet
22	RWX	WOX_AND	WOX_OR	TP_TC_PERVASIVE_ECO_FENCE: Pervasive ECO fence
23	RWX	WOX_AND	WOX_OR	CHKSW_HW257424_DISABLE: Chicken switch for interrupt retry exhausted bug (0=fix enabled, 1=fix disabled)
24:26	RWX	WOX_AND	WOX_OR	TP_CLK_ASYNC_RESET_DC: Clk async reset for three glitchless muxes, and the two clock dividers (bit 0 = master GLM, bit 1 = ECO Div2 and ECO GLM, bit 2= core Div1 and core GLM)
27:29	RWX	WOX_AND	WOX_OR	TP_CLKGLM_SEL_DC: Glitchless Mux Select for primary chiplet clock source (feeding both core and eco clock muxes) 000 = refclk, 001 = DPLL. 100 = Use constant selected by bit 34, else refclk
30	RWX	WOX_AND	WOX_OR	TP_CLKGLM_ECO_SEL_DC: Glitchless Mux Select for eco domain (cache_nclk) grid. 0= follow primary source chosen by previous field: 1 = Use constant selected by bit 34
31	ROX	NC	NC	SPECIAL_WKUP_DONE: Indicates that special wakeup is done, if asserted
32:33	RWX	WOX_AND	WOX_OR	TP_CLKGLM_CORE_SEL_DC: Glitchless Mux Select for core domain (nclk grid) mux. 0b00=primary GLS mux output, 0b10=constant input, 0b01=refclk. Valid transitions are 0b01 <-> 0b00 <-> 0b10, 0b11 is illegal



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
34	RWX	WOX_AND	WOX_OR	TP_CLKGLM_CONST_DC: Constant input available to all three ClkGlm
35:36	RWX	WOX_AND	WOX_OR	THOLD_TIMER_SEL: Selection for the thold transition timer in the IDLE state machine. 0b00=1024 cycles delay, 0b01=512 cycles delay, 0b10=256 cycles delay, 0b11= 128 cycles delay
37	RWX	WOX_AND	WOX_OR	BLOCK_ALL_WAKEUP_SOURCES: Setting this bit will make the PM Slave ignore any Wakeup events (ext. interrupt, malfunction alert, any special wakeup bit). This bit is intended to enable firmware concurrent patch capability. Note: This does NOT block the interrupt from being presented to the processor core. The following procedure is required on changes: 1. Firmware may only set this bit after first setting special wakeup and polling for special wakeup complete (OHA and PCB-slave both in running state with AISS and PM FSMs idle). 2. Firmware may only clear this bit if all special wakeup bits are first cleared.
38	RWX	WOX_AND	WOX_OR	TP_TC_DPLL_TESTMODE_DC: ADPLL test mode
39	RWX	WOX_AND	WOX_OR	PM_SLV_WINKLE_FENCE: Fence off the powered off chiplet in winkle. - Logical fence/hold for pcb_slave and pcb_slave_pm. For electrical fence see bit 23.
40	RWX	WOX_AND	WOX_OR	L3_ENABLE_SWITCH: Setting this bit activates l3_edram_enable if allowed by system configuration GP3(28). Resetting this bit deactivates l3_edram_enable.
41	RWX	WOX_AND	WOX_OR	TP_CPLT_IVRM_REFBYPASS_DC: Signal to iVRM (used to be controlled by scan-only block inside EX, but needs to be driven by VIO domain)
42	RWX	WOX_AND	WOX_OR	CHKSW_HW241939_DISABLE: if this bit is set to 1, the fix for HW241939 (pfet enable SCOM-ability) is disabled
43	RWX	WOX_AND	WOX_OR	CHKSW_HW273115_DISABLE: if this bit is set to 1, the fix for HW273115 (Pga ACK noack issue when the babystepper is in the winkle state) is disabled
44	RWX	WOX_AND	WOX_OR	CHKSW_HW245103_DISABLE: if this bit is set to 1, the fix for HW245103 resonant clocking CSB and SW -bit ordering change is disabled
45	RWX	WOX_AND	WOX_OR	CHKSW_HW257534_DISABLE: if this bit is set to 1, the fix for HW257534 (fencing of errors) is disabled
46	RWX	WOX_AND	WOX_OR	CHKSW_HW259509_ENABLE: if this bit is set to 0, the fix for HW259509 (Pstate change hanging, because of DPLL flock timer in a hung state) is disabled
47	RWX	WOX_AND	WOX_OR	CHKSW_HW260345_DISABLE: if set to 1, this bit disables the HW260345 fix (fix was to make sure that we enter bypass mode for iVRM safe mode without a glitch that could cause Vcs in regulation and Vdd in bypass)
48:49	ROX	NC	NC	WAKEUP_INT_TYPE: (Known to be unreliable and not supported, informational usage only) Type of the last wakeup event that caused an exit from sleep or winkle (excluding nap!), regardless of present state. 0b01: External interrupt. 0b10: Malfunction Alert. 0b11: Special Wakeup. 0b00: chiplet has never fully entered and exited a chiplet-level idle state since IPL of the system. (Note this does not necessarily get updated when the processor core enters an idle state, only if the PCB-Slave enters and then exits the idle state for this chiplet).
50	ROX	NC	NC	DPLL_LOCK: DPLL lock indicator
51	ROX	NC	NC	SPECIAL_WKUP_ALL_SOURCES_ORED: logical OR of all special wakeup sources
52	ROX	NC	NC	REGULAR_WKUP_AVAILABLE: logical OR of external interrupt and malfunction alert

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
53	RWX	WOX_AND	WOX_OR	BLOCK_REG_WKUP_SOURCES: blocks ext. int. and malf. Alert from waking up PCBS (no block possible for PC!)

Register Name	<i>PowerManagement GP1</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PMGP1_REG
Address	00000000120F0103 (PCB) 00000000120F0104 (PCB1) 00000000120F0105 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	SLEEP_POWER_DOWN_EN: Sleep Power Down Enable: When set to 1, causes hardware to automatically reduce voltage to the Core domain when entering Sleep mode. The voltage value for power down is chosen by sleep_power_off_sel (bit 2). When set to 0, a request is sent to the PORE engine for assistance entering Sleep.
1	RWX	WOX_AND	WOX_OR	SLEEP_POWER_UP_EN: Sleep Power Up Enable: When set to 1, enables automated hardware restoration of voltage via PFETs and, if enabled, iVRMs when exiting Sleep mode. If this bit is set to 0 the hardware rely on external means (PORE or equivalent) to restore voltage.
2	RWX	WOX_AND	WOX_OR	SLEEP_POWER_OFF_SEL: Sleep Power Off Select: Selects which voltage level to place the Core domain PFETs upon Sleep entry. 0 = Vret (Fast Sleep Mode), 1 = Voff (Deep Sleep Mode). Depending on the setting of pmicr_latency_en, this bit is controlled with a PCB-write (0) or by the PMICR in the core (1).
3	RWX	WOX_AND	WOX_OR	WINKLE_POWER_DOWN_EN: Winkle Power Down Enable: When set to 1, causes hardware to automatically reduce voltage to the entire Chiplet (both Core and ECO Domains) when entering Winkle mode. The voltage value for power down is chosen by winkle_power_off_sel (bit 5). When set to 0, a request is sent to the PORE engine for assistance entering Winkle.
4	RWX	WOX_AND	WOX_OR	WINKLE_POWER_UP_EN: Winkle Power Up Enable: When set to 1, enables automated hardware PFET enablement when exiting Winkle mode. If this bit is set to 0 the hardware rely on external means (PORE or equivalent) to cause the PFETs to be re-enabled.
5	RWX	WOX_AND	WOX_OR	WINKLE_POWER_OFF_SEL: Winkle Power Off Select: Selects which voltage level to place the Core and ECO domain PFETs upon Winkle entry. 0 = Vret (Fast Winkle Mode), 1 = Voff (Deep Winkle Mode). Depending on the setting of pmicr_latency_en, this bit is controlled with a PCB-write (0) or by the PMICR in the core (1).
6	RWX	WOX_AND	WOX_OR	OHA_WKUP_OVERRIDE_EN: Needs to be 0 for normal operation. If set to 1, the two following dials are used to override the regular and special wakeup signal from PCBS to OHA
7	RWX	WOX_AND	WOX_OR	OHA_PM_WKUP_OVERRIDE: Enablement by 'oha_wkup_override_en' forces the regular wakeup signal to OHA to the value of this bit regardless of presence of an interrupt source.
8	RWX	WOX_AND	WOX_OR	OHA_SPC_WKUP_OVERRIDE: Enablement by 'oha_wkup_override_en' forces the special wakeup signal to OHA to the value of this bit, regardless of the firmware settings.

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
9	RWX	WOX_AND	WOX_OR	ENDP_RESET_PM_ONLY: If asserted, an endpoint reset of all power management-related functions (not the regular PCB slave) is performed. Intended usage is for recovery.
10	RWX	WOX_AND	WOX_OR	DPLL_FREQ_OVERRIDE_ENABLE: override Fmax/Fmin only, if '1', using register FREQ_CTRL_REG
11	RWX	WOX_AND	WOX_OR	PM_SPR_OVERRIDE_EN: PM SPR Override Enable The PPMCR (0xNNNN) and PPMICR (0XXXXX) accesses the register resources that make up the PMCR SPR used by the hypervisor to management Pstates. Thus, PCB updates to it are disabled in hardware to prevent collisions. This bit allows ownership of the PMCR to be switched from the hypervisor to OCC. This switch is immediate in hardware, thus, firmware must ensure the ownership switch is otherwise communicated. 0 = Disables the writing of the PPMCR (0xNNNN) from the PCB and allows SPR 884 writes (mtspr) to update the register resource. 1 = Enables the writing of the PPMCR (0xNNNN) from the PCB.
12	RWX	WOX_AND	WOX_OR	FORCE_SAFE_MODE: Force Safe Mode 0 = Allow other enabled features to determine the operational Pstate. 1 = Forces the minimum of POHBR[psafe] and PPMCR[global_pstate_actual] Pstate for the core chiplet as the operational frequency.
13	RWX	WOX_AND	WOX_OR	IVRM_SAFE_MODE_EN: Internal VRM Safe Mode Enable 0 = Disable the iVRM safe mode, thus, no automatic actions occur, if an iVRM error happens. 1 = if the iVRMs are enabled (PIVRMCSR[ivm_en] is set) and Pstates are enabled and if the error defined by dial pcbs_ivrm_gross_or_fine_err occurs, then the railstepper is forced into bypass mode to prevent a voltage-frequency hazard
14	RWX	WOX_AND	WOX_OR	IVRM_SAFE_MODE_FORCE_ACTIVE: Internal VRM Safe Mode Force Dial 0 = the hardware decides whether to activate the iVRM safe mode or not 1 = the iVRM safe mode is forced regardless (this makes only sense if ivrm_fsm_enable=1 and Pstates are enabled)
15	RWX	WOX_AND	WOX_OR	PMICR_LATENCY_EN: Selects how the sleep/winkle latency (which is deep/fast) is controlled. If asserted the PMICR controls the winkle/sleep_power_off_sel in PMGP1, otherwise those bits are controlled via SCOM by OCC.
16	RWX	WOX_AND	WOX_OR	ENABLE_OCC_CTRL_FOR_LOCAL_PSTATE_EFF_REQ: controls, if the HW (for value 0) or OCC (value 1) is in control of the Local Pstate Effective register in PPSTR
17	RWX	WOX_AND	WOX_OR	SERIALIZE_PFET_POWERDOWN: if asserted, the pFET sequencer will sequence the core and the ECO domain one after the other when powering down
18	RWX	WOX_AND	WOX_OR	SERIALIZE_PFET_POWERUP: if asserted, the pFET sequencer will sequence the ECO and the core domain one after the other when powering up
19	RWX	WOX_AND	WOX_OR	DISABLE_FORCE_DEEP_TO_FAST_SLEEP: 0: (normal operation) - If PCB Slave reports a recoverable error or a checkstop, a DEEP sleep operation is forced to FAST. The entries in sleep/winkle_power_off_sel remain unchanged. 1: force to FAST is disabled.

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
20	RWX	WOX_AND	WOX_OR	DISABLE_FORCE_DEEP_TO_FAST_WINKLE: 0: (normal operation) - If PCB Slave reports a recoverable error or a checkstop, a DEEP winkle operation is forced to FAST. The entries in sleep/winkle_power_off_sel remain unchanged. 1: force to FAST is disabled.

Register Name	<i>PFET Control/Status Register For Core And ECO Vdd</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PFVDDCNTLSTAT_REG
Address	00000000120F0106 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	CORE_VDD_PFET_FORCE_STATE: Core Domain PFET Force State Provides a means for firmware to force the core domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 4:5 = 00 (both core_vdd_pfet_val_override AND core_vdd_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
2:3	RW	ECO_VDD_PFET_FORCE_STATE: ECO Domain PFET Force State Provides a means for firmware to force the ECO domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 6:7 = 00 (both eco_vdd_pfet_val_override AND eco_vdd_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
4	RW	CORE_VDD_PFET_VAL_OVERRIDE: Core Domain PFET Value Override 0 = Override is disabled
5	RW	CORE_VDD_PFET_SEL_OVERRIDE: Core Domain PFET Stage Select Override 0 = Override is disabled
6	RW	ECO_VDD_PFET_VAL_OVERRIDE: ECO Domain PFET Value Override 0 = Override is disabled
7	RW	ECO_VDD_PFET_SEL_OVERRIDE: ECO Domain PFET Stage Select Override 0 = Override is disabled
8	RW	CORE_VDD_PFET_ENABLE_REGULATION_FINGER: Core Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the core_vdd_pfet_enable_value.
9	RW	ECO_VDD_PFET_ENABLE_REGULATION_FINGER: ECO Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the eco_vdd_pfet_enable_value.



Bits	PCB	Field Mnemonic: Description
10:21	RW	CORE_VDD_PFET_ENABLE_VALUE: Core PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the Core Domain PFET Enables directly. If core_vdd_pfet_val_override = 1, a write to this field sets the state of the core PFET Enables until core_vdd_pfet_val_override is cleared. If core_vdd_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the core_vdd_pfet_valN_slat registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
22:25	RW	CORE_VDD_PFET_SEL_VALUE: Core PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure core_vdd_pfet_valN_slate(0:11) where N is 0 to 11 if core_vdd_pfet_sel_override = 1. If core_vdd_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
26:37	RW	ECO_VDD_PFET_ENABLE_VALUE: ECO PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the ECO PFET Enables directly. If ECO_vdd_pfet_val_override = 1, a write to this field sets the state of the ECO PFET Enables until ECO_vdd_pfet_val_override is cleared. If eco_vdd_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the eco_vdd_pfet_valN_slat registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
38:41	RW	ECO_VDD_PFET_SEL_VALUE: ECO PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure eco_vdd_pfet_valN_slate(0:11) where N is 0 to 11 if eco_vdd_pfet_sel_override = 1. If eco_vdd_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
42:45	ROX	CORE_VDD_PG_STATE: Core power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
46:49	ROX	CORE_VDD_PG_SEL: For debug, contains the actual index n into Core Domain PFET Value [n] SLAT Register set that contains the Core PFET Enable Value currently enabled.
50:53	ROX	ECO_VDD_PG_STATE: ECO Domain power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
54:57	ROX	ECO_VDD_PG_SEL: For debug, contains the actual index n into ECO Domain PFET Value [n] SLAT Register set that contains the ECO PFET Enable Value currently enabled.

Register Name	PFET Sense Register	
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PFSENSE_REG	
Address	00000000120F0107 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:11	ROX	TP_CORE_VDD_PFET_ENABLE_SENSE: Not used any more.
12:23	ROX	TP_ECO_VDD_PFET_ENABLE_SENSE: Not used any more.

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Bits	PCB	Field Mnemonic: Description
24:35	ROX	TP_CORE_VCS_PFET_ENABLE_SENSE: Not used any more.
36:47	ROX	TP_ECO_VCS_PFET_ENABLE_SENSE: Not used any more.

Register Name	<i>PM Error Summary Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PMERRSUM_REG
Address	00000000120F0108 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	PM_ERROR: PM Error is present. Intended for use by special PCB multicast to see error state of all chiplets with a single read (via 510F0108 to read all chiplets)

Register Name	<i>PM Error Register:</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PMERR_REG
Address	00000000120F0109 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_HANG_ERR: Hang during Unassisted Sleep Entry: SLEEP_ENTRY_NOTIFY_PMC state
1	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ASSIST_HANG_ERR: Hang during Assisted Sleep Entry: SLEEP_ENTRY_NOTIFY_PMC_ASSIST state
2	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ERR: Hang during Unassisted Sleep Exit: SLEEP_EXIT_NOTIFY_PMC state
3	ROX	PCBS_SLEEP_EXIT_INVOKE_PORE_ERR: Hang during Assisted Deep Sleep Exit: SLEEP_EXIT_INVOKE_PORE state
4	ROX	PCBS_WINKLE_ENTRY_NOTIFY_PMC_ERR: Hang during Unassisted Winkle Entry: WINKLE_ENTRY_NOTIFY_PMC state
5	ROX	PCBS_WINKLE_ENTRY_SEND_INT_ASSIST_ERR: Hang during Assisted Winkle Entry: WINKLE_ENTRY_SEND_INT_ASSIST state
6	ROX	PCBS_WINKLE_EXIT_NOTIFY_PMC_ERR: Hang during Unassisted Winkle Exit: WINKLE_EXIT_NOTIFY_PMC state
7	ROX	PCBS_WAIT_DPLL_LOCK_ERR: Hang during Unassisted Exit waiting on DPLL: WAIT_DPLL_LOCK state
8	ROX	PCBS_SPARE8_ERR: spare bit, always 0
9	ROX	PCBS_WINKLE_EXIT_SEND_INT_ASSIST_ERR: Hang during Assisted Winkle Exit: WINKLE_EXIT_SEND_INT_ASSIST state
10	ROX	PCBS_WINKLE_EXIT_SEND_INT_POWUP_ASSIST_ERR: Hang during Assisted Winkle Exit: WINKLE_EXIT_SEND_INT_POWUP_ASSIST state
11	ROX	PCBS_WRITE_FSM_GOTO_REG_IN_INVALID_STATE_ERR: write to FSM goto register in invalid state
12	ROX	PCBS_WRITE_PMGP0_IN_INVALID_STATE_ERR: write to PMGP0 in invalid state



Bits	PCB	Field Mnemonic: Description
13	ROX	PCBS_FREQ_OVERFLOW_IN_PSTATE_MODE_ERR: frequency of DPLL in Pstate mode overflows (Fnom + desired Pstate > 511)
14	ROX	PCBS_ECO_RS_BYPASS_CONFUSION_ERR: ECO railstepper tried to exit Vcs bypass and enter Vdd bypass in one Pstate step (it is not clear, in which order this strange operation should be performed - most likely it should never happen to avoid that Vcs is greater than Vdd)
15	ROX	PCBS_CORE_RS_BYPASS_CONFUSION_ERR: same as previous error, but for core railstepper (it is not clear, in which order this strange operation should be performed - most likely it should never happen to avoid that Vcs is greater than Vdd)
16	ROX	PCBS_READ_LPST_IN_PSTATE_MODE_ERR: read LPST-array while iVRM FSMs are enabled (dial ivrm_fsm_enable asserted)
17	ROX	PCBS_LPST_READ_CORR_ERR: correctable error occurred when reading the LPST
18	ROX	PCBS_LPST_READ_UNCORR_ERR: uncorrectable error occurred when reading the LPST
19	ROX	PCBS_PFET_STRENGTH_OVERFLOW_ERR: overflow occurred when calculating the pFET strength (in final rounding step!)
20	ROX	PCBS_VDS_LOOKUP_ERR: Vds entry not found in lookup table (when performing the linear search!)
21	ROX	PCBS_IDLE_INTERRUPT_TIMEOUT_ERR: idle interrupt timeout in PCB interrupt controller
22	ROX	PCBS_PSTATE_INTERRUPT_TIMEOUT_ERR: PState interrupt timeout in PCB interrupt controller
23	ROX	PCBS_GLOBAL_ACTUAL_SYNC_INTERRUPT_TIMEOUT_ERR: GlobalActualSync Interrupt timeout in PCB interrupt controller
24	ROX	PCBS_PMAX_SYNC_INTERRUPT_TIMEOUT_ERR: PmaxSync Interrupt timeout in PCB interrupt controller
25	ROX	PCBS_GLOBAL_ACTUAL_PSTATE_PROTOCOL_ERR: a write to global actual Pstate register has occurred before the global actual Pstate interrupt has left PCBS
26	ROX	PCBS_PMAX_PROTOCOL_ERR: a write to the Pmax/Pmin register has occurred before the Pmax sync interrupt has left PCB
27	ROX	PCBS_IVRM_GROSS_OR_FINE_ERR: iVRM gross or fine error (details to be found in PCBS_ivrm_Control_Status_Reg)
28	ROX	PCBS_IVRM_RANGE_ERR: iVRM range error (summary bit, details to be found in PCBS_ivrm_Control_Status_Reg)
29	ROX	PCBS_DPLL_CPM_FMIN_ERR: DPLL CPM Fmin error
30	ROX	PCBS_DPLL_DCO_FULL_ERR: DPLL DCO full
31	ROX	PCBS_DPLL_DCO_EMPTY_ERR: DPLL DCO empty
32	ROX	PCBS_DPLL_INT_ERR: DPLL internal error
33	ROX	PCBS_FMIN_AND_NOT_CPMBIT_ERR: dpll_fmin_and_not_cpmbit (ref. to dial cpm_fmin_clip_error_sel on how to configure this)
34	ROX	PCBS_DPLL_FASTER_THAN_FMAX_PLUS_DELTA1_ERR: dpll_faster_than_fmax_plus_delta1 (for characterization, delta1 is configurable with pll_char_delta1)
35	ROX	PCBS_DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2_ERR: dpll_slower_than_fmin_minus_delta2 (for characterization, delta2 is configurable with pll_char_delta2)
36	ROX	PCBS_RESCLK_CSB_INSTR_VECTOR_CHG_IN_INVALID_STATE_ERR: RESCLK CSB instruction vector change while FSMs none idle
37	ROX	PCBS_RESCLK_BAND_BOUNDARY_CHG_IN_INVALID_STATE_ERR: RESCLK Band boundaries change while FSMs none idle
38	ROX	PCBS_OCC_HEARTBEAT_LOSS_ERR: OCC heartbeat loss
39	ROX	PCBS_SPARE39_ERR: spare bit, always 0
40	ROX	PCBS_SPARE40_ERR: spare bit, always 0



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Bits	PCB	Field Mnemonic: Description
41	ROX	PCBS_SPARE41_ERR: spare bit, always 0
42	ROX	PCBS_SPARE42_ERR: spare bit, always 0

Register Name	<i>PM Error Mask Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PMERRMASK_REG
Address	00000000120F010A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_HANG_ERR_MASK: Mask for this error: 1=masked, 0=not masked
1	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ASSIST_HANG_ERR_MASK: Mask for this error: 1=masked, 0=not masked
2	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
3	RW	PCBS_SLEEP_EXIT_INVOKE_PORE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
4	RW	PCBS_WINKLE_ENTRY_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
5	RW	PCBS_WINKLE_ENTRY_SEND_INT_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
6	RW	PCBS_WINKLE_EXIT_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
7	RW	PCBS_WAIT_DPLL_LOCK_ERR_MASK: Mask for this error: 1=masked, 0=not masked
8	RW	PCBS_SPARE8_ERR_MASK: Mask for this error: 1=masked, 0=not masked
9	RW	PCBS_WINKLE_EXIT_SEND_INT_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
10	RW	PCBS_WINKLE_EXIT_SEND_INT_POWUP_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
11	RW	PCBS_WRITE_FSM_GOTO_REG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
12	RW	PCBS_WRITE_PMGPO_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
13	RW	PCBS_FREQ_OVERFLOW_IN_PSTATE_MODE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
14	RW	PCBS_ECO_RS_BYPASS_CONFUSION_ERR_MASK: Mask for this error: 1=masked, 0=not masked
15	RW	PCBS_CORE_RS_BYPASS_CONFUSION_ERR_MASK: Mask for this error: 1=masked, 0=not masked
16	RW	PCBS_READ_LPST_IN_PSTATE_MODE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
17	RW	PCBS_LPST_READ_CORR_ERR_MASK: Mask for this error: 1=masked, 0=not masked
18	RW	PCBS_LPST_READ_UNCORR_ERR_MASK: Mask for this error: 1=masked, 0=not masked
19	RW	PCBS_PFET_STRENGTH_OVERFLOW_ERR_MASK: Mask for this error: 1=masked, 0=not masked
20	RW	PCBS_VDS_LOOKUP_ERR_MASK: Mask for this error: 1=masked, 0=not masked
21	RW	PCBS_IDLE_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
22	RW	PCBS_PSTATE_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
23	RW	PCBS_GLOBAL_ACTUAL_SYNC_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
24	RW	PCBS_PMAX_SYNC_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked



Bits	PCB	Field Mnemonic: Description
25	RW	PCBS_GLOBAL_ACTUAL_PSTATE_PROTOCOL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
26	RW	PCBS_PMAX_PROTOCOL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
27	RW	PCBS_IVRM_GROSS_OR_FINE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
28	RW	PCBS_IVRM_RANGE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
29	RW	PCBS_DPLL_CPM_FMIN_ERR_MASK: Mask for this error: 1=masked, 0=not masked
30	RW	PCBS_DPLL_DCO_FULL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
31	RW	PCBS_DPLL_DCO_EMPTY_ERR_MASK: Mask for this error: 1=masked, 0=not masked
32	RW	PCBS_DPLL_INT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
33	RW	PCBS_FMIN_AND_NOT_CPMBIT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
34	RW	PCBS_DPLL_FASTER_THAN_FMAX_PLUS_DELTA1_ERR_MASK: Mask for this error: 1=masked, 0=not masked
35	RW	PCBS_DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2_ERR_MASK: Mask for this error: 1=masked, 0=not masked
36	RW	PCBS_RESCLK_CSB_INSTR_VECTOR_CHG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
37	RW	PCBS_RESCLK_BAND_BOUNDARY_CHG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
38	RW	PCBS_OCC_HEARTBEAT_LOSS_ERR_MASK: Mask for this error: 1=masked, 0=not masked
39	RW	PCBS_SPARE39_ERR_MASK: Mask for this error: 1=masked, 0=not masked
40	RW	PCBS_SPARE40_ERR_MASK: Mask for this error: 1=masked, 0=not masked
41	RW	PCBS_SPARE41_ERR_MASK: Mask for this error: 1=masked, 0=not masked
42	RW	PCBS_SPARE42_ERR_MASK: Mask for this error: 1=masked, 0=not masked

Register Name		<i>PM Special Wakeup FSP</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PMSPCWKUPFSP_REG
Address		00000000120F010B (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RW	FSP_SPECIAL_WAKEUP: Chiplet Special Wakeup for FSP Firmware use. NOTE: protocol is required when setting this bit

Register Name		<i>PM Special Wakeup OCC</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PMSPCWKUPOCC_REG
Address		00000000120F010C (PCB)
Attributes		
Description		

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Bits	PCB	Field Mnemonic: Description
0	RW	OCC_SPECIAL_WAKEUP: Chiplet Special Wakeup for OCC Firmware use. NOTE: protocol is required when setting this bit

Register Name	<i>PM Special Wakeup Hypervisor</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PMSPCWKUPPHYP_REG
Address	00000000120F010D (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	PHYP_SPECIAL_WAKEUP: Chiplet Special Wakeup for hypervisor Firmware use. NOTE: protocol is required when setting this bit

Register Name	<i>PFET Control/Status Register For Core And ECO Vcs</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PFVCSCTLSTAT_REG
Address	00000000120F010E (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	CORE_VCS_PFET_FORCE_STATE: Core Domain PFET Force State Provides a means for firmware to force the core domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 4:5 = 00 (both core_vcs_pfet_val_override AND core_vcs_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
2:3	RW	ECO_VCS_PFET_FORCE_STATE: ECO Domain PFET Force State Provides a means for firmware to force the ECO domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 6:7 = 00 (both eco_vcs_pfet_val_override AND eco_vcs_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
4	RW	CORE_VCS_PFET_VAL_OVERRIDE: Core Domain PFET Value Override 0 = Override is disabled
5	RW	CORE_VCS_PFET_SEL_OVERRIDE: Core Domain PFET Stage Select Override 0 = Override is disabled
6	RW	ECO_VCS_PFET_VAL_OVERRIDE: ECO Domain PFET Value Override 0 = Override is disabled
7	RW	ECO_VCS_PFET_SEL_OVERRIDE: ECO Domain PFET Stage Select Override 0 = Override is disabled



Bits	PCB	Field Mnemonic: Description
8	RW	CORE_VCS_PFET_ENABLE_REGULATION_FINGER: Core Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the core_vcs_pfet_enable_value.
9	RW	ECO_VCS_PFET_ENABLE_REGULATION_FINGER: ECO Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the eco_vcs_pfet_enable_value.
10:21	RW	CORE_VCS_PFET_ENABLE_VALUE: Core PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the Core Domain PFET Enables directly. If core_vcs_pfet_val_override = 1, a write to this field sets the state of the core PFET Enables until core_vcs_pfet_val_override is cleared. If core_vcs_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the core_vcs_pfet_valN_slav registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
22:25	RW	CORE_VCS_PFET_SEL_VALUE: Core PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure core_vcs_pfet_valN_slav(0:11) where N is 0 to 11 if core_vcs_pfet_sel_override = 1. If core_vcs_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
26:37	RW	ECO_VCS_PFET_ENABLE_VALUE: ECO PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the ECO PFET Enables directly. If ECO_vcs_pfet_val_override = 1, a write to this field sets the state of the ECO PFET Enables until ECO_vcs_pfet_val_override is cleared. If eco_vcs_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the eco_vcs_pfet_valN_slav registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
38:41	RW	ECO_VCS_PFET_SEL_VALUE: ECO PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure eco_vcs_pfet_valN_slav(0:11) where N is 0 to 11 if eco_vcs_pfet_sel_override = 1. If eco_vcs_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
42:45	ROX	CORE_VCS_PG_STATE: Core power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
46:49	ROX	CORE_VCS_PG_SEL: For debug, contains the actual index n into Core Domain PFET Value [n] SLAT Register set that contains the Core PFET Enable Value currently enabled.
50:53	ROX	ECO_VCS_PG_STATE: ECO Domain power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
54:57	ROX	ECO_VCS_PG_SEL: For debug, contains the actual index n into ECO Domain PFET Value [n] SLAT Register set that contains the ECO PFET Enable Value currently enabled.

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Register Name	<i>PM State History Register For Hypervisor</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPHYP_REG
Address	00000000120F0110 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	PHYP_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	PHYP_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	PHYP_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	PHYP_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	PHYP_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	PHYP_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For FSP</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PMSTATEHISTFSP_REG
Address	00000000120F0111 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	FSP_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	FSP_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	FSP_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	FSP_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.



Bits	PCB	Field Mnemonic: Description
6	ROX_CLRPAR T	FSP_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	FSP_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For OCC</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PMSTATEHISTOCC_REG
Address	00000000120F0112 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	OCC_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	OCC_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	OCC_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	OCC_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	OCC_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	OCC_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For PerfMon</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPERF_REG
Address	00000000120F0113 (PCB)
Attributes	
Description	

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Bits	PCB	Field Mnemonic: Description
0:2	ROX	PERF_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	PERF_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	PERF_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	PERF_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	PERF_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	PERF_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM FSM Reset And Babystepper Idle Injects</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.IDLEFSMGOTOCMD_REG
Address	00000000120F0114 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	WO_1P	idle_fsm_goto_cmd ' A write to this reg will proceed the IDLE FSM from WAIT_FOR_PORE_DONE, SLEEP_EXIT_WAIT_FOR_PORE_FAST_EXIT_DONE, or WINKLE_EXIT_WAIT_FOR_PORE_FAST_EXIT_DONE to the following states: ' 0b01: goto IDLE state ' 0b10: goto SLEEP_EXIT_CORE_MESHLET_ON state ' 0b11: goto WINKLE_EXIT_NOTIFY_PMC state ' '
2	RWX	babystp_trigger_sleep_entry ' A write to this reg with a 1 in this field will cause the babystepper to run the sleep entry sequence. This step is needed for an assisted entry into sleep, before the power is actually turned off since the babystepper needs to know about the sleep state. For an unassisted entry, writing this register must not be performed. ' ' 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished entering its sleep mode. '
3	RWX	babystp_trigger_winkle_entry ' A write to this reg with a 1 in this field will cause the babystepper to run the winkle entry sequence. This step is needed for an assisted entry into winkle before the power is actually turned off since the babystepper needs to know about the winkle state. For an unassisted entry, writing this register must not be performed. ' ' 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished entering its winkle mode. '
4	RWX	babystp_trigger_wakeup ' A write to this reg with a 1 in this field will cause the babystepper to run the wakeup sequence from sleep/winkle depending on the babystepper state of sleep or winkle. This step is needed for an assisted exit from winkle before the power is actually turned off since the babystepper needs to know about the wakeup state. For an unassisted exit, writing this register must not be performed. ' ' 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished waking up from sleep or winkle. '



Register Name	Core PFET Power Up Delay
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.COREPFPUDLY_REG
Address	00000000120F012C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_POWUP_DLY0: Delay used after transitioning to Core Domain power up sequence stage0. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	CORE_POWUP_DLY1: Delay used after transitioning to Core domain power up sequence stage1.
8:19	RW	CORE_POWER_UP_DELAY_SEL: Vector select for which delay to use for the respective power-up stage. Bit mapping: 8 -> core_*_pfet_enable(0) 9 -> core_*_pfet_enable(1) ... 19 -> core_*_pfet_enable(11) Bit meaning: 0 = Use core_powup_dly0 1 = Use core_powup_dly1

Register Name	Core PFET Power Down Delay
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.COREPFPDDLY_REG
Address	00000000120F012D (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_POWDN_DLY0: Delay used after transitioning to Core domain power dn sequence stage1. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	CORE_POWDN_DLY1: Delay used after transitioning to Core domain power dn sequence stage1. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
8:19	RW	CORE_POWER_DN_DELAY_SEL: Vector select for which delay to use for the respective power-dn stage. Bit mapping: 8 -> core_*_pfet_enable(0) 9 -> core_*_pfet_enable(1) ... 19 -> core_*_pfet_enable(11) Bit meaning: 0 = Use core_powdn_dly0 1 = Use core_powdn_dly1

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Register Name	Core PFET Vretention
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.COREPFVRET_REG
Address	00000000120F0130 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_VRET_SEL: Pointer to the stage representing the Vretention value for the core PFETs. Power down sequences will stop after enabling this stage.
4:7	RW	CORE_VOFF_SEL: Pointer to the stage representing the Voff value for the core PFETs. Power down sequences will stop after enabling this stage.

Register Name	ECO PFET Power Up Delay
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.ECOPFPUDLY_REG
Address	00000000120F014C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_POWUP_DLY0: Delay used after transitioning to ECO domain power up sequence stage0 in terms of refclk period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	ECO_POWUP_DLY1: Delay used after transitioning to ECO domain power up sequence stage1.
8:19	RW	ECO_POWER_UP_DELAY_SEL: Vector select for which delay to use for the respective power-up stage. Bit mapping: 8 -> eco_*_pfet_enable(0) 9 -> eco_*_pfet_enable(1) ... 19 -> eco_*_pfet_enable(11) Bit meaning: 0 = Use eco_powup_dly0 1 = Use eco_powup_dly1

Register Name	ECO PFET Power Down Delay
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.ECOPFPDDLY_REG
Address	00000000120F014D (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_POWDN_DLY0: UNUSED/SPARE
4:7	RW	ECO_POWDN_DLY1: Delay used after transitioning to ECO Domain power dn sequence stage1. The delays in this register are in terms of refclk period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.

Bits	PCB	Field Mnemonic: Description
8:19	RW	ECO_POWER_DN_DELAY_SEL: Vector select for which delay to use for the respective power-down stage. Bit mapping: 8 -> eco_*_pfet_enable(0) 9 -> eco_*_pfet_enable(1) ... 19 -> eco_*_pfet_enable(11) Bit meaning: 0 = Use eco_powdn_dly0 1 = Use eco_powdn_dly1

Register Name		<i>ECO PFET Vretention</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.ECOPFVRET_REG
Address		00000000120F0150 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_VRET_SEL: Pointer to the stage representing the Vretention value for the ECO PFETs. Power down sequences will stop after enabling this stage.
4:7	RW	ECO_VOFF_SEL: Pointer to the stage representing the Voff value for the ECO PFETs. Power down sequences will stop after enabling this stage.

Register Name		<i>Frequency Control Register With Overrides For DPLL</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.FREQ_CTRL_REG
Address		00000000120F0151 (PCB)
Attributes		
Description		Frequency control register with overrides for DPLL. Note that overrides to Dpll_fmax are only applied, if Dpll_freq_override_enable = 1. A read of all these dials always returns the currently established DPLL frequencies (regardless of any other mode settings).

Bits	PCB	Field Mnemonic: Description
0:8	RWX	DPLL_FMIN: minimum DPLL frequency in CPM-DPLL mode that is set at IPL time A read always returns the currently established value A write is not conditioned on any other dial setting.
9:17	RWX	DPLL_FMAX: DPLL maximum frequency and frequin (these two values are the same in POWER8 processor) without applying bias values: A read always returns the currently established value A write is conditioned on the setting of dpll_freq_override_enable. If dpll_freq_override_enable is asserted, a write causes this field to update. Otherwise the hardware (that is, PStates) are controlling the update of this value.
18:21	RW	DPLL_FMAX_BIAS: Bias for the maximum DPLL frequency intended to be used in CPM-DPLL mode to control explicitly the hard limit for the maximum DPLL frequency. Note that this signed value gets added to the value of dpll_fmax and the result is established as the effective DPLL Fmax input. Thus, in non-CPM mode it is recommended to set this dial to 0. Note also that this dial MUST be zero in non-CPM mode
22:30	RW	FREQU_AT_PSTATE0: DPLL frequency for Pstate 0

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Register Name	<i>DPLL Mode Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.DPLL_CPM_PARM_REG
Address	00000000120F0152 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	LF_SLEWRATEXPI: out of lock slew rate for DPLL
8	RW	LF_USE_CPMXPI: use CPM instead of PFD as loop filter input, if '1' (instead of using both)
9	RW	FF_USE_CPMXPI: use the CPM inputs for the frequency filter, if '1'
10	RW	CPM_FILTER_ENABLE: enables the CPM filter
11	RW	FF_BYPASSXPI: enables frequency filter bypass
12	RW	DCO_OVERRIDE: enables overrides for DCO testing/characterization
13	RW	DCO_INCR: enables increment for DCO testing/characterization, increments only on a rising edge
14	RW	DCO_DECR: enables decrement for DCO testing/characterization, decrements only on a rising edge
15:23	RW	DPLL_LOCK_TIMER_REPLACEMENT_VALUE: if dpll_lock_replacement_timer_mode_en is set, this dial specifies the delay in us, after which it is assumed, that the DPLL has reached a frequency lock condition. Note that values less than 3 will cause in undefined HW behavior (0 will cause HANGs!). if dpll_lock_replacement_timer_mode_en is zero, this dial specifies the delay in pcb_nclk cycles after which the hardware monitors the DPLL frequout output (if dpll_freqout_mode_en is set) or the DPLL flock output (if dpll_flock_mode_en is set). Note that in this case, the value of this dial needs to be greater or equal to 150 (decimal).
24:31	RW	PRE_VRET_PSTATE: Pstate that is stepped to before switching to Vretention defined in PCBS_iVRM_Control_Status_Reg
32	RW	OVERRIDE_PCBS_DPLL_SYNCHRONIZER: Bypasses the 'ping-pong' synchronization logic between the DPLL and the PCBS-PM. NEVER SET TO 1 UNLESS YOU KNOW WHAT YOU ARE DOING!
33:36	RW	DPLL_CHAR_DELTA1: Delta in DPLL ticks for characterization (cf. dial dpll_faster_than_fmax_plus_delta1)
37:40	RW	DPLL_CHAR_DELTA2: Delta in DPLL ticks for characterization (cf. dial dpll_faster_than_fmin_minus_delta2)

Register Name	<i>PPMSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_STATUS_REG
Address	00000000120F0153 (PCB)
Attributes	
Description	The PPMSR provides read access to the power management status that is also shadowed to PC and visible to the hypervisor in the PMSR (with some delay due to the shadowing process).

Bits	PCB	Field Mnemonic: Description
0:7	ROX	global_pstate_actual ' Actual Global Pstate Pstate or Pglobal_actual' " 'Reads from this field return the presently established global PState value.' " 'Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent '

Bits	PCB	Field Mnemonic: Description
8:15	ROX	LOCAL_PSTATE_ACTUAL: ' Actual Local PState or Plocal_actual' " 'Reads from this field return the presently established local PState value. This value will always be less than or equal to global_pstate_actual.' " 'Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent' "
16:23	ROX	pv_min Minimum Pstate set by the platform.
24:31	ROX	pvf_max Maximum Pstate set by the platform.
32	ROX	spr_em_disabled ' SPR Energy Management Disabled' 'Read from this field indicate whether the platform has disabled the 'PMCR and PMICR SPRs to control the chiplet PState. '
33	ROX	Psafe_mode_active Read from this field indicate whether the chiplet has been put into a safe mode with Psafe enabled to a OCC heartbeat loss or other externally forced reasons (0=regular mode, 1=safe mode is active)
34	ROX	iVRM_safe_mode_active Read from this field indicate whether the chiplet has been put the iVRM safe mode (forcing the bypass mode for all iVRMs)
35	ROX	ivrm_enable Read from this field indicate whether the chiplet internal voltage regulation macro is enabled for localized voltage control (0=disabled, 1=enabled) based on ANDing the poweron signals to the iVRMs
36	ROX	all_fsms_in_safe_state For recovery: if this bit is asserted, all Pstate and iVRM control FSMs are in a stable, safe state that allows the recovery routine to proceed with resetting the PCBS PM without the risk of interrupt a critical action
37:40	ROX	pmsr_spares spare bits

Register Name	<i>PIVRMCSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_CONTROL_STATUS_REG
Address	00000000120F0154 (PCB)
Attributes	
Description	The PIVRMCSR provides access to chiplet-level controls of the internal VRM rail set (VDD and VCS) across both the core and ECO domains. The following is valid only for bits 4 to 7: When in automatic iVRM mode (ivrm_fsm_enable = 1), these bits provide access to the values established by the automatic hardware mechanism. When In iVRM Override Mode (ivrm_fsm_enable = 0), these bits allow firmware direct control of the values driving the internal VRMs

Bits	PCB	Field Mnemonic: Description
0	RW	IVRM_FSM_ENABLE: Internal master VRM FSM Enable 0 = Disable Internal VRM FSMs and enable to control the iVRMs with the available override registers (SCOMable) as a backup mode or for setup (override mode) 1 = Enable Internal VRM FSM sequencers (requires that Pstates are enabled with enable_Pstate_mode=1 as well) (automatic mode)
1	RW	USE_IVRM_FOR_VRET: Internal VRM Enabled for Vretention 0 = Disable Internal VRM for Vretention 1 = Enable Internal VRM for Vretention
2	RW	BINSEARCH_CAL_ENA: trigger binary search (level signal)

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Bits	PCB	Field Mnemonic: Description
3	RW	PVREF_EN: Internal VRM Power Voltage Reference Forced Enable 0 = Allow hardware to enable/disable pvref circuit 1 = Force enablement of the pvref circuit
4	RWX	IVRM_CORE_VDD_BYPASS_B: Internal VRM Core VDD Bypass (negative active) 0 = VDD Internal Core VRMs in bypass 1 = VDD internal Core VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
5	RWX	IVRM_CORE_VDD_POWERON: Internal VRM Core VDD Poweron 0 = Core VDD Internal VRMs powered off 1 = Core VDD internal VRMs powered on if this bit is not set (=0), the Core VDD internal VRM powered off internally. If this bit is set (=1), the Core VDD internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
6	RWX	IVRM_CORE_VCS_BYPASS_B: Internal VRM Core VCS Bypass (negative active) 0 = VCS Internal Core VRMs in bypass 1 = VCS internal Core VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VCS internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VCS internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
7	RWX	IVRM_CORE_VCS_POWERON: Internal VRM Core VCS Poweron 0 = Core VCS Internal VRMs powered off 1 = Core VCS internal VRMs powered on if this bit is not set (=0), the Core VCS internal VRM powered off internally. If this bit is set (=1), the Core VCS internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
8	RWX	IVRM_ECO_VDD_BYPASS_B: Internal VRM ECO VDD Bypass (negative active) 0 = VDD Internal ECO VRMs in bypass 1 = VDD internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
9	RWX	IVRM_ECO_VDD_POWERON: Internal VRM ECO VDD Bypass (negative active) 0 = VDD Internal ECO VRMs in bypass 1 = VDD internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.

Bits	PCB	Field Mnemonic: Description
10	RWX	IVRM_ECO_VCS_BYPASS_B: Internal VRM ECO VCS Bypass (negative active) 0 = VCS Internal ECO VRMs in bypass 1 = VCS internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VCS internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VCS internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
11	RWX	IVRM_ECO_VCS_POWERON: Internal VRM ECO VCS Poweron 0 = ECO VCS Internal VRMs powered off 1 = ECO VCS internal VRMs powered on if this bit is not set (=0), the ECO VCS internal VRM powered off internally. If this bit is set (=1), the ECO VCS internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
12:18	RWX	IVRM_VRET_VDD: if use_ivrm_for_Vret is asserted, this dial is used to control the Vdd retention voltage. Note: this field will establish the Core VDD rail for Sleep and both the Core and ECO rail for Winkle. - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
19:25	RWX	IVRM_VRET_VCS: if use_ivrm_for_Vret is asserted, this dial is used to control the Vcs retention voltage. Note: this field will establish the Core VDD rail for Sleep and both the Core and ECO rail for Winkle. - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
26:30	RWX	IVRM_VRET_CORE_VDD_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the Core Vdd iVRM PFET strength for the retention voltage
31:35	RWX	IVRM_VRET_CORE_VCS_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the Core Vcs iVRM PFET strength for the retention voltage
36:40	RWX	IVRM_VRET_ECO_VDD_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the ECO Vdd iVRM PFET strength for the retention voltage
41:45	RWX	IVRM_VRET_ECO_VCS_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the ECO Vcs iVRM PFET strength for the retention voltage
46	RW	PVREF_FAIL: voltage reference fail input to iVRMs
47	ROX	IVRM_PREF_ERROR_GROSS: Voltage Reference Gross Error 0 = Gross Error not detected 1 = Gross Error detected
48	ROX	IVRM_PREF_ERROR_FINE: Voltage Reference Fine Error 0 = Fine Error not detected 1 = Fine Error detected
49	ROX	IVRM_CORE_VDD_RANGE_HI: Core VDD Internal VRM Range Hi Indicator 0 = Core VDD Internal VRM Hi indicator signal not asserted 1 = Core VDD internal VRMs Hi indicator signal asserted
50	ROX	IVRM_CORE_VDD_RANGE_LO: Core VDD Internal VRM Range Low Indicator 0 = Core VDD Internal VRM Low indicator signal not asserted 1 = Core VDD internal VRMs Low indicator signal asserted

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Bits	PCB	Field Mnemonic: Description
51	ROX	IVRM_ECO_VDD_RANGE_HI: ECO VDD Internal VRM Range Hi Indicator 0 = ECO VDD Internal VRM Hi indicator signal not asserted 1 = ECO VDD internal VRMs Hi indicator signal asserted
52	ROX	IVRM_ECO_VDD_RANGE_LO: ECO VDD Internal VRM Range Low Indicator 0 = ECO VDD Internal VRM Low indicator signal not asserted 1 = ECO VDD internal VRMs Low indicator signal asserted
53	ROX	IVRM_CORE_VCS_RANGE_HI: Core VCS Internal VRM Range Hi Indicator 0 = Core VCS Internal VRM Hi indicator signal not asserted 1 = Core VCS internal VRMs Hi indicator signal asserted
54	ROX	IVRM_CORE_VCS_RANGE_LO: Core VCS Internal VRM Range Low Indicator 0 = Core VCS Internal VRM Low indicator signal not asserted 1 = Core VCS internal VRMs Low indicator signal asserted
55	ROX	IVRM_ECO_VCS_RANGE_HI: ECO VCS Internal VRM Range Hi Indicator 0 = ECO VCS Internal VRM Hi indicator signal not asserted 1 = ECO VCS internal VRMs Hi indicator signal asserted
56	ROX	IVRM_ECO_VCS_RANGE_LO: ECO VCS Internal VRM Range Low Indicator 0 = ECO VCS Internal VRM Low indicator signal not asserted 1 = ECO VCS internal VRMs Low indicator signal asserted
57	ROX	BINSEARCH_CAL_DONE: binary search done signal
58	RWX	IVRM_CORE_VDD_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
59	RWX	IVRM_CORE_VCS_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
60	RWX	IVRM_ECO_VDD_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
61	RWX	IVRM_ECO_VCS_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
62	RW	IVRM_POWER_DOWN_DISABLE: If this bit is 1, the iVRM poweron signal is left asserted. Power off of the iVRMs is then blocked



Register Name	PIVRMVSR
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VALUE_SETTING_REG
Address	00000000120F0155 (PCB)
Attributes	
Description	The PIVRMVSR allows access to VID values and PFET strength valid signal settings presented to the internal VRM rail set (VDD and VCS) across both the core and ECO domains. When in <code>ivrm_fsm_enable = "auto"</code> mode, this register provides access to the values established by the automatic hardware mechanism. When <code>ivrm_fsm_enable = "override"</code> mode, this register allows firmware direct control of the values driving the internal VRMs which, if the VRMs are not in bypass, will move the voltage settings.

Bits	PCB	Field Mnemonic: Description
0:7	RWX	IVRM_CORE_VDD_IVID: When read, returns the value presently being driving to the Core VDD iVRM. If <code>ivrm_fsm_enable = 0 (override_mode)</code> , then writes to this field will drive a new VID value to the Core VDD iVRM. If <code>ivrm_fsm_enable = 1</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
8:15	RWX	IVRM_CORE_VCS_IVID: When read, returns the value presently being driving to the Core VCS iVRM. If <code>ivrm_fsm_enable = 0 (override_mode)</code> , then writes to this field will drive a new VID value to the Core VCS iVRM. If <code>ivrm_fsm_enable = 1</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
16:23	RWX	IVRM_ECO_VDD_IVID: When read, returns the value presently being driving to the Core VDD iVRM. If <code>ivrm_fsm_enable = 0 (override_mode)</code> , then writes to this field will drive a new VID value to the ECO VDD iVRM. If <code>ivrm_fsm_enable = 1</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
24:31	RWX	IVRM_ECO_VCS_IVID: When read, returns the value presently being driving to the ECO VCS iVRM. If <code>ivrm_fsm_enable = 0 (override_mode)</code> , then writes to this field will drive a new VID value to the ECO VCS iVRM. If <code>ivrm_fsm_enable = 0</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
32:36	RWX	IVRM_CORE_VDD_PFET_STRENGTH: When read, returns the value presently being driving to the core VCS iVRM. If <code>ivrm_fsm_enable = 0 (override_mode)</code> , then writes to this field will drive a new strength value to the core VCS iVRM. If <code>ivrm_fsm_enable = 0</code> , writes to this field are not performed.

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Bits	PCB	Field Mnemonic: Description
37:41	RWX	IVRM_CORE_VCS_PFET_STRENGTH: This register is assigned to the signals tcex##_tp_ivrm_core_vcs_sense & tcex##_tp_ivrm_core_vdd_sense & tcex##_tp_ivrm_eco_vcs_sense & tcex##_tp_ivrm_eco_vdd_sense & 0b0 Note that all other sense signals are spares now and tied to 0. OUTDATED TEXT: When read, returns the value presently being driving to the core VDD iVRM. If ivrm_fsm_enable =0 (override_mode), then writes to this field will drive a new strength value to the core VDD iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
42:46	RWX	IVRM_ECO_VDD_PFET_STRENGTH: When read, returns the value presently being driving to the ECO VCS iVRM. If ivrm_fsm_enable =0 (override_mode), then writes to this field will drive a new strength value to the ECO VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
47:51	RWX	IVRM_ECO_VCS_PFET_STRENGTH: When read, returns the value presently being driving to the ECO VDD iVRM. If ivrm_fsm_enable =0 (override_mode), then writes to this field will drive a new strength value to the ECO VDD iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
52	RWX	IVRM_VDD_CORE_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the Core VDD iVRM. If ivrm_fsm_enable =1 AND ivrm_control_mode = 1 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the Core VDD iVRM, If ivrm_fsm_enable = 0 OR ivrm_control_mode = 0, writes to this field are not performed.
53	RWX	IVRM_VCS_CORE_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the Core VCS iVRM. If ivrm_fsm_enable =0 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the Core VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
54	RWX	IVRM_VDD_ECO_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the ECO VDD iVRM. If ivrm_fsm_enable =1 AND ivrm_control_mode = 1 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the ECO VDD iVRM, If ivrm_fsm_enable = 0 OR ivrm_control_mode = 0, writes to this field are not performed.
55	RWX	IVRM_VCS_ECO_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the ECO VCS iVRM. If ivrm_fsm_enable =0 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the ECO VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
56	RWX	CORE_VDD_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable =0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
57	RWX	CORE_VCS_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable =0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
58	RWX	ECO_VDD_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable =0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
59	RWX	ECO_VCS_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable =0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.

Register Name		<i>General PCBS Modes And Chicken Switches</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBSPM_MODE_REG
Address		00000000120F0156 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RW	ENABLE_PSTATE_MODE: if asserted, Pstate requests (from overrides or PMCR) will be honored, otherwise, the hardware does not do anything. Note to firmware: this is the master switch for Pstates and should be asserted after all sub-modes (that is, lvrn_fsm_en) are setup to avoid enabling unintentional modes during the mode setup.
1	RW	GLOBAL_PSTATE_CHANGE_FOR_IDLE_STATE_ENABLED: if asserted, a global Pstate change to the Nap/Sleep/Winkle-Pstate is requested, when the Nap/Sleep/Winkle state is entered and the individual enable bits in the PIMCR are asserted
2	RW	ENABLE_GLOBAL_PSTATE_REQ: if '1' then enable PMC interrupt with global Pstate change request, otherwise, disable global requests
3	RW	ENABLE_WINKLE_WITH_CPM_MODE: if '1', PCBS automatically changes the DPLL mode to mode 1, when entering winkle, but changes the mode back to CPM mode when exiting. Needed for CPM-DPLL control loop enablement.
4	RW	ENABLE_CLIPPING_OF_GLOBAL_PSTATE_REQ: if '1', PCBS automatically clips global Pstate requests with Pvf_max in PPMBR and sets the 'donate' bit in the interrupt accordingly
5	RW	CHKSW_HW214553: if deasserted, HW214553 (frequin issue in resclk mode) is fixed, if asserted, the fix is not active
6	RW	ENABLE_PMC_PMAX_SYNC_NOTIFICATION: if asserted, the PCBS-PM will send a 'Pmax_sync' interrupt, once the synchronization criterion is met
7	RW	DPLL_LOCK_REPLACEMENT_TIMER_MODE_EN: Select a timer instead of the DPLL lock bit as target frequency reached criterion. This timer has to be setup by the dial dpll_lock_timer_replacement_value. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
8	RW	DPLL_FREQOUT_MODE_EN: Looks at the DPLL frequout to find out, if the target frequency has been reached. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
9	RW	DPLL_FLOCK_MODE_EN: Looks at the real DPLL flock output to find out, if the target frequency has been reached. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
10	RW	ENABLE_SENSE_DELAY_CHARACTERIZATION: If this switch is 0, the sense latches are updated every cycle. If this switch is 1, the sense delay measurement mode is enabled, that starts a sense delay timer, whenever one of the registers that drive the inputs of the iVRMs/pFETs is written via PCB and that triggers a sense register freeze operation, when the sense delay timer reaches the value sense_delay_timer_val. With this mode, the sense delays can be measured in multiples of the PCB-slave clock speed.
11:17	RW	SENSE_DELAY_TIMER_VAL: See the description of enable_sense_delay_characterization for details.
18:19	RW	CPM_FMIN_CLIP_ERROR_SEL: This dial selects, which of the following conditions will cause the FIR bit dpll_fmin_and_not_cpmbit to be set to detect, that the DPLL runs at Fmin, but is still clipped by the CPMs. 0b00 = function is disabled 0b01 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit2 = 0 0b10 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit1 = 0 0b11 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit0 = 0
20:23	RW	DBG_TRACE_SEL: This dial selects the group of signals to be traced for debug in the lab. Details to be found in the Section 'Trace Bus'

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Bits	PCB	Field Mnemonic: Description
24:25	RW	TRACE_DATA_SEL: This dial selects the group of signals to be traced for debug in the lab. Details to be found in the Section 'Trace Bus'
26:29	RW	TP_CPLT_IVRM_VPP_TUNE: Tune bits to be set going to the iVRMs

Register Name	<i>PIVRMPS Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_PFETSTR_SENSE_REG
Address	00000000120F0157 (PCB)
Attributes	
Description	This PIVRMPS Is used to check that the pFET sense outputs correspond to the driven values (mainly for test).

Bits	PCB	Field Mnemonic: Description
0:4	ROX	IVRM_CORE_VDD_PFETSTR_SNS: Not used any more.
5:9	ROX	IVRM_CORE_VCS_PFETSTR_SNS: This register is assigned to the signals tcex##_tp_ivrm_core_vcs_sense & tcex##_tp_ivrm_core_vdd_sense & tcex##_tp_ivrm_eco_vcs_sense & tcex##_tp_ivrm_eco_vdd_sense & 0b0
10:14	ROX	IVRM_ECO_VDD_PFETSTR_SNS: Not used any more.
15:19	ROX	IVRM_ECO_VCS_PFETSTR_SNS: Not used any more.
20	ROX	IVRM_VDD_CORE_PFETSTR_VALID_SNS: Not used any more.
21	ROX	IVRM_VCS_CORE_PFETSTR_VALID_SNS: Not used any more.
22	ROX	IVRM_VDD_ECO_PFETSTR_VALID_SNS: Not used any more.
23	ROX	IVRM_VCS_ECO_PFETSTR_VALID_SNS: Not used any more.
24	ROX	CORE_VDD_BYPASS_B_SENSE: Not used any more.
25	ROX	CORE_VCS_BYPASS_B_SENSE: Not used any more.
26	ROX	ECO_VDD_BYPASS_B_SENSE: Not used any more.
27	ROX	ECO_VCS_BYPASS_B_SENSE: Not used any more.
28	ROX	CORE_VDD_POWERON_SENSE: Not used any more.
29	ROX	CORE_VCS_POWERON_SENSE: Not used any more.
30	ROX	ECO_VDD_POWERON_SENSE: Not used any more.
31	ROX	ECO_VCS_POWERON_SENSE: Not used any more.
32	ROX	CORE_VDD_VPUMP_EN_SENSE: Not used any more.
33	ROX	CORE_VCS_VPUMP_EN_SENSE: Not used any more.
34	ROX	ECO_VDD_VPUMP_EN_SENSE: Not used any more.
35	ROX	ECO_VCS_VPUMP_EN_SENSE: Not used any more.
36	ROX	CORE_VDD_PFET_LOW_VOUT_SNS: Not used any more.
37	ROX	CORE_VCS_PFET_LOW_VOUT_SNS: Not used any more.
38	ROX	ECO_VDD_PFET_LOW_VOUT_SNS: Not used any more.
39	ROX	ECO_VCS_PFET_LOW_VOUT_SNS: Not used any more.



Register Name	PPMICR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_IDLE_CONTROL_REG
Address	00000000120F0158 (PCB)
Attributes	
Description	The PPMICR is used to to read the PMICR register typically owned (written) by the hypervisor. Writes are conditioned on the setting of the dial Pm_spr_override_en. If Pm_spr_override_en is set, firmware needs to make sure that the special wakeup state of this chiplet is reached before changing any of the latency fields in this register. Otherwise, the hardware behavior is undefined.

Bits	PCB	Field Mnemonic: Description
0:7	ROX	NAP_PSTATE_REQ: Nap Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
8	ROX	NAP_PSTATE_EN: Nap PState Enable 1 = Enable the Nap Pstate (NPS) Request, Nap Global Enable and Nap Latency functions 0 = Disables the Nap Pstate (NPS) Request, Nap Global Enable and Nap Latency functions Reads from the field return the value last written.
9	ROX	NAP_GLOBAL_EN: Nap Global Enable 1 = Upon the execution of a Nap instruction , the Nap Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a Nap instruction , the Nap Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.
10:11	ROX	NAP_LATENCY: Nap Latency not supported for POWER8 processor
12:15	ROX	RESERVED_PPMICR_0: reserved
16:23	ROX	SLEEP_PSTATE_REQ: sleep Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
24	ROX	SLEEP_PSTATE_EN: sleep PState Enable 1 = Enable the sleep Pstate (NPS) Request, sleep Global Enable and sleep Latency functions 0 = Disables the sleep Pstate (NPS) Request, sleep Global Enable and sleep Latency functions Reads from the field return the value last written.
25	ROX	SLEEP_GLOBAL_EN: sleep Global Enable 1 = Upon the execution of a sleep instruction , the sleep Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a sleep instruction , the sleep Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.

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Bits	PCB	Field Mnemonic: Description
26:27	ROX	SLEEP_LATENCY: sleep Latency 00 = Cease instructions and honors Pstate change but does not perform additional state changing actions (unsupported in POWER8, maps to 0b10) 01 = Indicates to the platform that a sub-state that would have the lowest latency is enabled (unsupported in POWER8, maps to 0b10) 10 = Indicates to the platform that a sub-state that might have a medium exit latency is enabled (POWER8: Fast Sleep) 11 = Indicates to the platform that a sub-state that might have higher exit latency is enabled (POWER8: Deep Sleep)
28:31	ROX	RESERVED_PPMICR_1: reserved
32:39	ROX	WINKLE_PSTATE_REQ: winkle Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
40	ROX	WINKLE_PSTATE_EN: winkle PState Enable 1 = Enable the winkle Pstate (NPS) Request, winkle Global Enable and winkle Latency functions 0 = Disables the winkle Pstate (NPS) Request, winkle Global Enable and winkle Latency functions Reads from the field return the value last written.
41	ROX	WINKLE_GLOBAL_EN: winkle Global Enable 1 = Upon the execution of a winkle instruction , the winkle Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a winkle instruction , the winkle Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.
42:43	ROX	WINKLE_LATENCY: winkle Latency 00 = Cease instructions and honors Pstate change but does not perform additional state changing actions (unsupported in POWER8, maps to 0b10) 01 = Indicates to the platform that a sub-state that would have the lowest latency is enabled (unsupported in POWER8, maps to 0b10) 10 = Indicates to the platform that a sub-state that might have a medium exit latency is enabled (POWER8: Fast Winkle) 11 = Indicates to the platform that a sub-state that might have higher exit latency is enabled (POWER8: Deep Winkle)
44:47	ROX	RESERVED_PPMICR_2: reserved

Register Name	PPMCR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_CONTROL_REG
Address	00000000120F0159 (PCB)
Attributes	
Description	The PPMCR provides read access to the PMCR register shadow in the PCBS typically owned (written) by the hypervisor. Writes are conditioned on the setting of PMGP1[pm_spr_override_en].

Bits	PCB	Field Mnemonic: Description
0:7	RWX	GLOBAL_PSTATE_REQ: global Pstate request from hypervisor (or OCC)
8:15	RWX	LOCAL_PSTATE_REQ: local Pstate request from hypervisor or OCC
16	RWX	AUTO_OVERRIDE0_PSTATE_LIMIT_EN: automatic override Pstate 0 (for low activity detection) is enabled, if asserted



Bits	PCB	Field Mnemonic: Description
17	RWX	AUTO_OVERRIDE1_PSTATE_LIMIT_EN: automatic override Pstate 1 (reserved for future use) is enabled, if asserted
18:23	RWX	RESERVED_PPMCR: reserved
24:31	RWX	AUTO_OVERRIDE_PSTATE0: automatic override Pstate 0 (for low activity detection)
32:39	RWX	AUTO_OVERRIDE_PSTATE1: automatic override Pstate 1 (reserved for future use)

Register Name	<i>Control Register That Is Written By PMC Sequencer</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_PMC_VF_CTRL_REG
Address	00000000120F015A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PGLOBAL_ACTUAL: global actual Pstate
8:15	RW	MAXREGVCS: maximum regulation point for Vcs, Bit 0 is reserved, bits 1 to 7 are in iVID format
16:23	RW	MAXREGVDD: maximum regulation point for Vdd, Bit 0 is reserved, bits 1 to 7 are in iVID format
24:31	RW	EVIDVCS_EFF: eff. external voltage ID for Vcs in iVID format, Bit 0 is reserved
32:39	RW	EVIDVDD_EFF: eff. external voltage ID for Vdd in iVID format, Bit 0 is reserved

Register Name	<i>Undervolting Register For PCBS</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_UNDERVOLTING_REG
Address	00000000120F015B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PUV_MIN: minimum Pstate for which undervolting is allowed
8:15	RW	PUV_MAX: maximum Pstate for which undervolting is allowed
16:21	RW	KUV: this value indicates how many Pstate ticks a voltage request is undervolted (clipped with Puv_min). Note that the Kuv value is signed

Register Name	<i>PPSIBR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_INDEX_BOUND_REG
Address	00000000120F015C (PCB)
Attributes	
Description	The PPSIBR enables setting the minimum and maximum Pstate that is supported as a pointer into the local Pstate table (which has entries from 0 to 127).

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Bits	PCB	Field Mnemonic: Description
0:7	RW	LPSI_MIN: this Pstate index is the index that corresponds to array entry 0. Note that the index domain is obtained by adding 128 to a Pstate, thus, the value is unsigned.
8:14	RW	LPSI_ENTRIES_MINUS_1: this dial contains the value of the number of entries in the Pstate table minus 1

Register Name	<i>PPMBR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_BOUNDS_REG
Address	00000000120F015D (PCB)
Attributes	
Description	The PPMBR enables setting the Pstate bounds that are managed by the OCC. If dial Enable_pmc_pmax_sync_notification is set, firmware must wait after each write to this register until the PMC has received the Pmax Sync Interrupt. If a write happens to this register while the previously scheduled Pmax Sync Interrupt has not yet left PCBS, the error TBD will be set.

Bits	PCB	Field Mnemonic: Description
0:7	RW	PMIN_CLIP: minimum Pstate allowed for this chiplet
8:15	RW	PMAX_CLIP: maximum Pstate allowed for this chiplet (has to be greater or equal to Pmin_clip)

Register Name	<i>PPTCR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_CTRL_REG
Address	00000000120F015E (PCB)
Attributes	
Description	The PPTCR controls the address for writing the local Pstate table array (all 96 words are accessible). Note that the protocol requires this register to be set up with the Pstate address first, if a read or a write of the Pstate array is intended, to make sure that the initial address is set correctly. The register PPTR must always be written or read afterward. Note that any access to the PPTR auto-increments this register.

Bits	PCB	Field Mnemonic: Description
0:6	RWX	PSTATE_TABLE_ADDRESS: This is the address of the Pstate table in PCBS, which is auto-incremented after any access to the PTLR.

Register Name	<i>PPTR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_REG
Address	00000000120F015F (PCB)
Attributes	
Description	The PPTR controls the data to be written into the Pstate Table and returns the data for a read of the Pstate table. Note that the protocol requires for a write to set this register up after first setting up PPTCR (if the user does not rely on the auto-increment function of the address). For a read of the Pstate table, this register must be read after first setting up PPTCR as well (again if the auto-increment feature of the address is not used). Any access to this register auto-increments the Pstate_table_address by 1. Note also that the read functionality of this register is only functional if PIVRMCSR[ivrm_fsm_enable] = 0. The write functionality works in any case.

Bits	PCB	Field Mnemonic: Description
0:63	RW	pstate_data This is the field for data bits 0 to 63

Register Name	<i>PPSTR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_STEP_TARGET_REG
Address	00000000120F0160 (PCB)
Attributes	
Description	The PPSTR provides read access to several intermediate values in the Pstate computation pipeline. Writes are conditioned on the setting of PMGP0[enable_OCC_ctrl_for_local_Pstate_eff_req].

Bits	PCB	Field Mnemonic: Description
0:7	RWX	LOCAL_PSTATE_EFF_REQ: this field represents the effective local Pstate request right before the clipping with Pmin and Pmax if enable_OCC_ctrl_for_local_Pstate_eff_req=0 then the hardware controls this dial, that updates every cycle if enable_OCC_ctrl_for_local_Pstate_eff_req=1 then OCC is in control and can write this field to control the effective local Pstate request that will eventually propagate through the downstream logic and determine the Local PState Actual. Note: if no write to this register is performed, the currently established value is maintained stable forever.
8:15	ROX	LOCAL_PSTATE_TARGET: This field is the target Pstate of a complete Pstate change that is performed in smaller steps
16:23	ROX	LOCAL_CORE_PSTATE_STEP_TARGET: this field represents the intermediate value that is about to be established as the next Local Pstate Actual after completing one step in the process of the transition towards the 'local_Pstate_target' the new voltage, frequency, and clock resonance setting
24:31	ROX	LOCAL_ECO_PSTATE_STEP_TARGET: this field represents the intermediate value that is about to be established as the next Local Pstate Actual after completing one step in the process of the transition towards the 'local_Pstate_target' the new voltage, frequency, and clock resonance setting

Register Name	<i>Read-Only Status Register For DPLL And For Debugging (PDSR)</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_DPLL_STATUS_REG
Address	00000000120F0161 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:14	ROX	DPLL_FF_FREQOUT: frequout output from DPLL (current frequency - bits 2 to 10 correspond to the same scale as the 9 bits of frequin (which need to be multiplied with our frequency step to get the real frequency), the remaining bits just provide a higher accuracy)
15	ROX	DPLL_FREQU_CHANGE: DPLL Frequency change (pin of DPLL without filter)
16	ROX	DPLL_STATUS_SPARE_BIT1: Spare bit.
17	ROX	PMAX_SYNC_PENDING: gets asserted, if the logic has a Pmax sync interrupt outstanding that will be eventually sent to PMC when the Pmax sync criterion is met
18	ROX	GA_ACK_PENDING: gets asserted, if the logic has a global actual Pstate update acknowledgment interrupt outstanding that will be eventually sent to PMC when the GA ack criterion is met
19:26	ROX	CAPPED_GLOBAL_PSTATE_REQ: corresponds to the capped global Pstate request that is presented as Pstate interrupt and send to PMC

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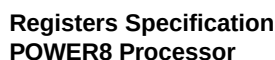
Bits	PCB	Field Mnemonic: Description
27	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT2: DPLL runs at Fmax and CPM bit 2 is set. Note that this bit and the following 2 bits indicate, that the CPMs would allow the DPLL to run faster than Fmax.
28	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT3: DPLL runs at Fmax and CPM bit 3 is set
29	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT4: DPLL runs at Fmax and CPM bit 4 is set
30	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT2: DPLL runs at Fmin and CPM bit2 is zero. Note that this bit and the following 2 bits indicate, that the CPMs indicate, that the DPLL should run slower than the currently established Fmin.
31	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT1: DPLL runs at Fmin and CPM bit1 is zero
32	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT0: DPLL runs at Fmin and CPM bit0 is zero
33	ROX_CLRPAR T	DPLL_FASTER_THAN_FMAX_PLUS_DELTA1: The DPLL indicated that it ran once faster than Fmax+dppl_char_delta1
34	ROX_CLRPAR T	DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2: The DPLL indicated that it ran once slower than Fmin-dppl_char_delta2
35:48	ROX	DPLL_MAX_FREQOUT_AFTER_LAST_READ: This dial indicates the maximum DPLL frequout value after the last read of this register (only 14 MSBs)
49:62	ROX	DPLL_MIN_FREQOUT_AFTER_LAST_READ: This dial indicates the minimum DPLL frequout value after the last read of this register (only 14 MSBs)

Register Name	<i>The PIVRMVCR0 Controls The Voltage Stepping Delays</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG0
Address	00000000120F0162 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	IVRM_REQ_PSTATE_STEPDELAY_RISING: Requested Internal Pstate Baby Step Delay - Rising Step. Delay before allowing the next step for a rising Pstate Transition. This dial and ivrm_req_Pstate_stepdelay_lowering allow for differing delays for the two directional transitions if necessary. In 100ns units as established by scan dial ivrm_100ns_value
8:15	RW	IVRM_REQ_PSTATE_STEPDELAY_LOWERING: Requested Internal Pstate Baby Step Delay - Lowering Step. Delay before allowing the next step for a lower Pstate Transition. This dial and ivrm_req_Pstate_stepdelay_rising allow for differing delays for the two directional transitions if necessary. In 100ns units as established by scan dial ivrm_100ns_value

Register Name	<i>The PIVRMVCR1 Controls The Voltage Stepping Delays</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG1
Address	00000000120F0163 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	IVRM_STABILIZE_DELAY_RUN: Stabilization Delay - Run Time Delay to allow a rail to stabilize upon a baby step while the region is operational. In 100ns units as established by scan dial ivrm_100ns_value
8:15	RW	IVRM_STABILIZE_DELAY_IDLE: Stabilization Delay - Idle Transition Delay to allow a rail to stabilize upon a baby step during an idle transition where the activity in the region is quiesced. In 100ns units as established by scan dial ivrm_100ns_value
16:23	RW	IVRM_PFSTR_PROP_DELAY: PFET Strength Propagation Delay Time from PFET Strength values being launched till PFET Strength Valid is asserted. In order to ensure like rails across domains (Core VDD<>ECO VDD, Core VCS<>ECO VCS) are in sync during operational mode, this time value applies to all rails across the domains. This parameter allows for PFET Strength values to settle before PFET Strength Valid is sampled in the Uregs. The value set must be the maximum delay for the worst rail timing and must allow for any metastability settling (for example, normally 2-3 cycles for single signals in an asynch handshake interface)
24:31	RW	IVRM_PFSTRVALID_PROP_DELAY: PFETStrength Valid Propagation Delay Time from ivrm_pfstr_prop_delay expiring to where PFET Strength Valid is deasserted. The value is the maximum of a) the minimum pulse width required for PFETStrength Valid and b) the propagation of PFETStrength Valid through (or enough of) the daisy chain. In order to ensure like rails across domains (Core VDD<>ECO VDD, Core VCS<>ECO VCS) are in sync during operational mode, this time value applies to all rails across the domains and thus must be the set to the value of the worst (slowest) rail. The minimum pulse width cannot be violated. The propagation delay can be tuned for more aggressive timing (for example, deassert before the actual propagation is complete). Measured in prv_nclk cycles. The min delay is 2 cycles. Additional delay can be configured with the following settings 0x00 = No additional delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks
32:39	RW	IVRM_VPUMP_POWERON_TIME: iVRM (VRreg and UReg) - Vpump Power On Time Time necessary for the distributed internal VRM macro circuits to power on. Same delay is required for power on voltage pump circuit. Both delays are in the 8us range. In 100ns units as established by scan dial ivrm_100ns_value
40:47	RW	IVRM_BYPASS_DELAY: iVRM Bypass Propagation Delay Delay time for bypass_b signal propagation. Measured in prv_nclk cycles Target: 50ns 0x00 = No delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks



Register Name	PRCCR0 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG0
Address	00000000120F0165 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function.

Bits	PCB	Field Mnemonic: Description
0	ROX	RESCLK_DIS: Resonant Clock Enable Master enable of all resonant clocking functions. This dial can be set by setting GP3(22) and can not be set in this PCBS_resonant_Clock_Control_Reg0. 1 = Resonant Clock function is disabled. Default values (0) for resclk_value, resclk_core_sync_value, csb_eco_sync_value 0 = Resonant Clock Control hardware is enabled (the mode is defined by dial resclk_control_mode)
1	RW	RESCLK_CONTROL_MODE: Resonant Clock Control Mode Defines the control means enabled when resclk_dis is not set. 0 = Pstate band hardware mechanism enabled 1 = Manual mode enabled (Firmware mode) If this bit is set to 0, the hardware control mechanism that manages the transition across the Resonant Bands is enabled. If this bit is set to 1, the automatic Pstate band hardware mechanism is disabled and the Firmware is in control of all values of the dial resclk_value, resclk_core_sync_value, csb_eco_sync_value. Firmware must ensure that frequency changes will not cross resonant bands or machine failures may result. resclk_value represents the values for clock sector buffer strength, inductor switch strength and high inductor enable. Firmware must ensure the correct stepping in/out the different bands and propagation of the values (resclk_value) to the core/eco (resclk_core_sync_value / csb_eco_sync_value).
2:4	RW	RESCLK_SYNC_PW: Resonant Clock Sync Pulse Width Number of nest/4 cycles to assert the clock sync signal. This value must be high enough to ensure capture and propagation across the asynchronous chiplet boundary.
5:11	RW	RES_SYNC_DELAY_CNT: Resonant Clock Sync Delay Number of nest/4 cycles wait after the launch of the resclk_value (csb and inductor) before launching the sync to allow these to be captured. This value must be high enough to ensure full propagation to the input of the clock sector buffers and inductor switches.
12:26	RW	RES_CSB_STR_INSTR_LO: Resonant Clock Sector Buffer Strength Instruction - Low Band Mask value that determines whether, during a fixed 15 step sequence, the res_csb_str(0:3) is to be decremented/incremented in entering/exiting the Low Band. During resonant clock Entry, res_csb_str(0:3) decremented by the value pattern from 0 down to 14. During resonant clock Exit, res_csb_str(0:3) incremented by the value pattern from 14 up to 0.
27:41	RW	RES_CSB_STR_INSTR_HI: Resonant Clock Sector Buffer Strength Instruction - High Band Mask value that determines whether, during a fixed 15 step sequence, the res_csb_str(0:3) is to be decremented/incremented in entering/exiting the High Band. During resonant clock Entry, res_csb_str(0:3) decremented by the value pattern from 0 down to 14. During resonant clock Exit, res_csb_str(0:3) incremented by the value pattern from 14 up to 0.

Register Name		PRCCR1 Register
Mnemonic		EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG 1
Address		00000000120F0166 (PCB)
Attributes		
Description		Controls the behavior of the resonant clocking function. Writes are conditioned.
Bits	PCB	Field Mnemonic: Description
0:7	RW	FULL_CSB_PS: Full Clock Sector Buffer Pstate Pstate defining the maximum point where the clock sector buffer must be driven to full strength. This allow clocks to be distributed at low Vmin levels. FW needs to make sure that no overlaps occur with bands 2 or 3.
8:15	RW	RES_LOW_LOWER_PS: Low Frequency Resonant Lower (LFRLow) Pstate Pstate defining the lower frequency of the Low Resonant Frequency Band. FW needs to make sure that no overlap occurs with band 0.

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Bits	PCB	Field Mnemonic: Description
16:23	RW	RES_LOW_UPPER_PS: Low Frequency Resonant Upper (LFRUpper) Pstate Pstate defining the upper frequency of the Low Resonant Frequency Band. Note that if an overlap occurs with band 3, the hardware behavior is undefined.
24:31	RW	RES_HIGH_LOWER_PS: High Frequency Resonant Lower (HFRLow) Pstate Pstate defining the lower frequency of the High Resonant Frequency Band. Note that if an overlap occurs with band 2, the hardware behavior is undefined.
32:39	RW	RES_HIGH_UPPER_PS: High Frequency Resonant Upper (LFRUpper) Pstate Pstate defining the upper frequency of the High Resonant Frequency Band. This value needs to be greater or equal to high_res_lower_ps.
40:43	RW	NONRES_CSB_VALUE_TI: Clock Sector Buffer Table Index for non-resonant state Table Index into Clock Sector Buffer Table for the nominal, non-resonant state.
44:47	RW	FULL_CSB_VALUE_TI: Clock Sector Buffer Table Index for full CSB value Table Index into Clock Sector Buffer Table for the full CSB strength value.
48:56	RWX	RESCLK_VALUE: Output register driving the 9 bit resclk_value In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current resclk_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. The value in this register represents the following concatenation: csb_str_value(0:3) sw_str(0:3) hi_induct_en.
57	RWX	RESCLK_CORE_SYNC_VALUE: Output register driving the resclk_core_sync signal In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current resclk_core_sync_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. This bit is supposed to be used in order to create a SCOM-controlled pulse to force an update of the resclk propagation registers. A 1 enables the synchronous update, a 0 disables it. Suggested use of this bit is to set it to 1 and then set it back to 0 to create a (long) update pulse.
58	RWX	CSB_ECO_SYNC_VALUE: Output register driving the csb_eco_sync signal In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current csb_eco_sync_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. This bit is supposed to be used in order enable the ECO domain to participate in clock sector buffer strength changes, when switching from nominal strength to full CSB strength. A 1 enables the ECO domain, a 0 disables it from seeing a CSB strength update.

Register Name	PRCCR1 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_STATUS_REG
Address	00000000120F0167 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function.



Bits	PCB	Field Mnemonic: Description
0	ROX	RESCLK_STATE: Resonant Clock State 0 = Resonant Clocking inactive 1 = Resonant Clocking active Valid if resclk_inprogress = 0. Hardware sets this bit to the right value at the completion of the transition into and out of resonance mode.

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Bits	PCB	Field Mnemonic: Description
1	ROX	RES_HI_INDUCT_EN: Resonant High Inductor Enable Valid if resclk_inprogress = 0. This dial provides the current value being propagated. 0 = Resonant Clock mode not active 1 = Resonant Clock mode active
2	ROX	RESCLK_INPROGRESS: Resonant Clock Transition in Progress This bit is set by hardware while a transition is in progress and will be reset by hardware when the operation is complete.
3	ROX	RESCLK_FULL_CSB: Full CSB Clock State 0 = Full CSB Clocking inactive 1 = Full CSB Clocking active Valid if resclk_inprogress = 0. Hardware sets this bit to the right value at the completion of the transition into and out of full CSB mode respectively.

Register Name	<i>PLPFTCR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_CONTROL_REG
Address	00000000120F0168 (PCB)
Attributes	
Description	The PLPFTCR allows firmware to configure the modes that are used for the PCBS Local Pstate Frequency Target Status Register.

Bits	PCB	Field Mnemonic: Description
0:2	RW	DELAY_TIME: This field encodes the delay between the time a Local Actual Pstate change modifies the input to the DPLL and the time frequency acquisition begins to allow the hardware to ignore the frequency transition of the DPLL in order to get better frequency measurements. This field encodes a delay of ~1us to ~128us in power of 2 selects. The delay is defined by $2^{\text{delay\_time}}$ in us. Note that the hardware uses multiples of the slow hang pulse that is running at 1us.
3	RW	RECORD_TRANSITIONS: This bit indicates whether the LPFTSR records events that correspond to Local Actual Pstate changes (and therefore may include DPLL slewing effects.) One usage model would set the periodic sample_time defined by the dial OHA_MODE_REG[tod_pulse_count_match_val] to a time less than the worst-case DPLL slew time but then ignore Pstate transitions because they might include DPLL slew effects.
4:18	RW	MULTIPLIER: This 15-bit unsigned constant is multiplied by the DPLL frequency code (9 bits) implied by the Local Actual Pstate to yield the 24-bit frequency target measured in PCBS-PM clock cycles (core clock / 2). Assuming times in seconds and frequencies in Hz, firmware should set this constant to: $(\text{DPLL\_Frequency\_Code\_Step\_Hz} * \text{Sample\_Time\_Seconds}) / 2$
19	RW	ENABLE_LPFT_FUNCTION: This is the enable bit to enable the local Pstate frequency target function. A '1' enables the function, a '0' disables it (the value can be changed at any time).

Register Name	<i>PLPFTSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_STATUS_REG
Address	00000000120F0169 (PCB)
Attributes	
Description	The PLPFTSR allows firmware to observe local actual Pstate realized frequencies.

Bits	PCB	Field Mnemonic: Description
0	ROX_CLRPART	VALID: If this bit is set then all of the remaining fields of this register are valid. This bit is cleared whenever the register is read or after a local actual Pstate change occurs, and is will be set whenever the hardware completes a valid sample. If firmware reads this register and the valid bit is not set, then it indicates that the Local Pstate target frequency acquisition logic has not been able to complete a frequency acquisition for any Local Actual Pstate change since the last time the LPFTSR was read. This could be due to either of the following factors: 1. Firmware is sampling the LPFTSR faster than the time implied by the sample time defined in OHA by the dial OHA_MODE_REG[tod_pulse_count_match_val] field
1	ROX	CPM_DPLL: If the valid bit is set, then if cpm_dpll is set it indicates that the event recorded by this register was due to a Local Actual Pstate implemented by the DPLL running in CPM-DPLL mode, otherwise the value of this bit is undefined. If the valid bit is not set, this bit is undefined.
2	ROX	IVRM: If the valid bit is set, then if ivrm is set it indicates that the event recorded by this register was due to a Local Actual Pstate whose voltage was set locally by the iVRM operating entirely in regulation mode. If the valid bit is not set, this bit is undefined.
3	ROX	TRANSITION: If the valid bit is set, then if transition is set it indicates that during the observation period a Local Pstate Actual change has occurred, and any performance delta may be due to DPLL frequency slewing. If the valid bit is not set, this bit is undefined
4	ROX	STABLE: If stable is set it indicates that the DPLL input frequency has been stable since the last time the PLPFTSR was read. This bit is set whenever the PLPFTSR is read, and cleared whenever the Fmax input of the DPLL changes. This bit is always valid, regardless of the state of the valid bit. If the PLPFTSR is read on the same cycle a frequency changes then the stable bit is cleared. This bit helps firmware better understand how to interpret the information contained in the PLPFTSR. (Note that this bit should have an attribute ROX_SETPART, but this is not supported by regchk.)
5:28	ROX	DELTA: If the valid bit is set then this is the 24-bit signed difference Measured Cycles - Target Cycles for the event captured by this register. If the valid bit is not set, this dial is undefined.
29:52	ROX	CUMULATIVE: This field records the 24-bit cumulative (signed) delta for all valid samples taken since this field was cleared. Writing any value to this register clears this field. Note that it should have an attribute WOX_CLRPART, but this is not supported by regchk/figtree.
53:60	ROX	PSTATE: If the valid bit is set then this is the Local Actual Pstate of the frequency acquisition that had the minimum (signed) delta of any valid sample taken since the last time the LPFTSR was read. If the valid bit is not set, then this field is undefined.

Register Name	PFSMM1/2 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR1_REG
Address	00000000120F0170 (PCB)
Attributes	
Description	The PFSMM1/2 facilitates debug by providing insight into the internal FSM states of the PCB-slave power-management unit. For expert use only. Coding according to VHDL design.

Bits	PCB	Field Mnemonic: Description
0:6	ROX	BABYSTEP_MAIN_FSM: Main Babystep FSM (mfsm_lt)
7:11	ROX	BABYSTEP_SLAVE_FSM: Babystep Slave FSM (sfsm_lt)
12:16	ROX	CORE_RAILSTEPPER_MAIN_FSM: Main Core Railstepper FSM (mrsfsm_lt)
17:21	ROX	ECO_RAILSTEPPER_MAIN_FSM: Main ECO Railstepper FSM (mrsfsm_lt)

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Bits	PCB	Field Mnemonic: Description
22:25	ROX	CORE_RAILSTEPPER_SUB_FSM: Core Railstepper Sub-FSM (srsfsm_lt)
26:29	ROX	ECO_RAILSTEPPER_SUB_FSM: ECO Railstepper Sub-FSM (srsfsm_lt)
30:34	ROX	CORE_RAILSTEPPER_BYP_FSM: Core Railstepper Bypass FSM (byp_fsm_lt)
35:39	ROX	ECO_RAILSTEPPER_BYP_FSM: ECO Railstepper Bypass FSM (byp_fsm_lt)
40:45	ROX	IVRM_CORE_VDD_SEQUENCER_FSM: Core iVRM Sequencer for Vdd (ivrm_fsm_lt)
46:51	ROX	IVRM_CORE_VCS_SEQUENCER_FSM: Core iVRM Sequencer for Vcs (ivrm_fsm_lt)
52:57	ROX	IVRM_ECO_VDD_SEQUENCER_FSM: ECO iVRM Sequencer for Vdd (ivrm_fsm_lt)
58:63	ROX	IVRM_ECO_VCS_SEQUENCER_FSM: ECO iVRM Sequencer for Vcs (ivrm_fsm_lt)

Register Name	<i>Refer To The Description Of PFSMM1.</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR2_REG
Address	00000000120F0171 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:6	ROX	RESCLK_BAND_FSM: Band Sequencer for resonant clocking (band_fsm_lt)
7:10	ROX	RESCLK_LOWRES_FSM: Low Resonant Clocking sequencer (lowres_fsm_lt)
11:14	ROX	RESCLK_HIGHRES_FSM: High Resonant Clocking sequencer (highres_fsm_lt)
15:18	ROX	RESCLK_FULLCSB_FSM: Full-CSB Resonant Clocking sequencer (fullcsb_fsm_lt)
19:22	ROX	RESCLK_UPDATE_FSM: Resonant Clocking Update sequencer (update_fsm_lt)
23:29	ROX	IDLE_TRANSITION_FSM: Idle State Sequence FSM (ifsm_lt)
30:37	ROX	Peco_step_target_uv Current ECO Step Target Pstate (different from Plocal_actual for undervolting)
38:45	ROX	Pcore_step_target_uv Current core Step Target Pstate (different from Plocal_actual for sleep and undervolting)

Register Name	<i>Protect Mode Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.PROTECT_MODE_REG
Address	00000000120F03FE (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	READ_PROTECT_ENABLE: Enable read protection
1	RW	WRITE_PROTECT_ENABLE: Enable write protection



Register Name	<i>Atomic Lock Register</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX02.TP_PCB_SLAVE_INST.ATOMIC_LOCK_REG	
Address	00000000120F03FF (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	RW	ATOMIC_LOCK_ENABLE: Enable atomic lock
1:4	ROX	ATOMIC_ID: Atomic ID

Register Name	<i>Contains The Slave's Primary Address</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.PRIMARY_ADDRESS_REG	
Address	00000000130F0000 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RO	Reserved field (Access type is primary_address)

Register Name	<i>Multicast Group 1</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.MULTICAST_GROUP_1	
Address	00000000130F0001 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST1_GROUP: multicast group1 setting

Register Name	<i>Multicast Group 2</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.MULTICAST_GROUP_2	
Address	00000000130F0002 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST2_GROUP: multicast group2 setting

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Register Name	<i>Multicast Group 3</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.MULTICAST_GROUP_3
Address	00000000130F0003 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST3_GROUP: multicast group3 setting

Register Name	<i>Multicast Group 4</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.MULTICAST_GROUP_4
Address	00000000130F0004 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST4_GROUP: multicast group4 setting

Register Name	<i>Timeout Select Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.TIMEOUT_REG
Address	00000000130F0010 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	Reserved field (Access type is int_timeout)

Register Name	<i>Assist Interrupt Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.ASSIST_INTERRUPT_REG
Address	00000000130F0011 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is attn)
1	ROX	Reserved field (Access type is recov)
2	ROX	Reserved field (Access type is xstop)



Register Name	GP3 Register (NA In PERV CPLT)
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.GP3_REG
Address	00000000130F0012 (PCB) 00000000130F0013 (PCB1) 00000000130F0014 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset
2	RWX	RWX_WAND	RWX_WOR	GLSMUX_RESET: Glsmux reset for test purpose and stuck active mesh protection. Notice no clocks in the EX if this bit is set.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Put the DPLL in test mode.
4	RWX	RWX_WAND	RWX_WOR	PLL_RST: Put PLL in reset state.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYP: Enable PLL bypass.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pcb_access)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	PM_PI_DECODE: Test override for power management. EX chiplet only.
22	RWX	RWX_WAND	RWX_WOR	RESCLK_DIS: Resonant clocking disable.
23:25	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave will report 'Chiplet Offline'.
27	RWX	RWX_WAND	RWX_WOR	TP_LVLTRANS_FENCE: Electrical winkel fence. Mainly used by power management.
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.
29:31	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)

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Register Name	<i>Skew Adjust Data</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.CLK_ADJ_REG
Address	00000000130F0015 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:15	ROX	

Register Name	<i>Clk Ajust Config</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.CLK_ADJ_SET
Address	00000000130F0016 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:31	RW	CLK_ADJ_SET_REG: Clk adj config

Register Name	<i>Vital Scan Out</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.VITAL_SCAN_OUT
Address	00000000130F0017 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	

Register Name	<i>Chiplet Heartbeat Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.HEARTBEAT_REG
Address	00000000130F0018 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	HEARTBEAT_DEAD: Chiplet heartbeat not detected



Register Name	<i>Lock Indications From PLLs</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.PLL_LOCK_REG	
Address	00000000130F0019 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:3	ROX	Reserved field (Access type is lock)

Register Name	<i>Attn Interrupt</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.ATTN_INTERRUPT_REG	
Address	00000000130F001A (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is attn)

Register Name	<i>Recov Interrupt</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.RECOV_INTERRUPT_REG	
Address	00000000130F001B (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is recov)

Register Name	<i>Xstop Interrupt</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.XSTOP_INTERRUPT_REG	
Address	00000000130F001C (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is xstop)

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Register Name	<i>Slave Config Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.SLAVE_CONFIG_REG
Address	00000000130F001E (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	CFG_DISABLE_PERV_THOLD_CHECK: Disable pervasive thold check
1	RW	CFG_DISABLE_MALF_PULSE_GEN: Disable pulse generation for malf alert. Switch back to level
2	RW	CFG_STOP_HANG_CNT_SYS_XSTP: Disable hang counter stop for system xstop
3	RW	CFG_DISABLE_CL_ATOMIC_LOCK: Disable atomic lock for chiplet accesses
4	RW	CFG_DISABLE_HEARTBEAT: Disable check for voltage and gridclock in the chiplet
5	RW	CFG_ZERO_DATA: Sent zero data on any error
6:7	RW	
8:12	RW	ERROR_MASK: mask bits for slave error reporting
13:15	RW	

Register Name	<i>Error Capture Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.ERROR_REG
Address	00000000130F001F (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX_WCLEA R	CE_ERROR: Correctable error on pcb bus
1:3	RWX_WCLEA R	CHIPLET_ERRORS: Errors reported by chiplet 000 = no error 001 = XSCOM command blocked due pending errors 010 chiplet offline 011 partial good 100 invalid address / address error / bad access type 101 clock error 110 parity error / received unexpected packet / wrong packet number 111 timeout This register is for debug purposes only. It only holds meaningful data if it is cleared after each error.
4	RWX_WCLEA R	PARITY_ERROR: Parity error on PCB Interface
5	RWX_WCLEA R	DATA_BUFFER_ERROR: Parity error in data buffer
6	RWX_WCLEA R	ADDR_BUFFER_ERROR: Parity error in address buffer
7	RWX_WCLEA R	PCB_FSM_ERROR: Invalid state error in PCB FSM
8	RWX_WCLEA R	CL_FSM_ERROR: Invalid state error in Chiplet FSM
9	RWX_WCLEA R	INT_RX_FSM_ERROR: Invalid state error in interrupt RX FSM
10	RWX_WCLEA R	INT_TX_FSM_ERROR: Invalid state error in interrupt TX FSM



Bits	PCB	Field Mnemonic: Description
11	RWX_WCLEAR	INT_TYPE_ERROR: Invalid interrupt type
12	RWX_WCLEAR	CL_DATA_ERROR: Parity error on Chiplet Interface
13	RWX_WCLEAR	INFO_ERROR: Parity error on Chiplet info lines
14	RWX_WCLEAR	UNUSED_0:
15	RWX_WCLEAR	CHIPLET_ATOMIC_LOCK_ERROR: Chiplet atomic lock error
16	RWX_WCLEAR	PCB_INTERFACE_ERROR: Error of pcb interface component for the internal endpoint
17	RWX_WCLEAR	CHIPLET_OFFLINE: Heartbeat check indicated that chiplet is offline
18	RWX_WCLEAR	CHIPLET_GRID_SKITTER: Heartbeat check indicated skitter on the chiplet grid
19	RWX_WCLEAR	GP3_REG_PARITY_ERROR: gp3 register parity bad
20	RWX_WCLEAR	ADDRESS_REG_PARITY_ERROR: address register parity bad
21	RWX_WCLEAR	TIMEOUT_REG_PARITY_ERROR: timeout select register parity bad
22	RWX_WCLEAR	CONFIG_REG_PARITY_ERROR: slave config register parity bad
23	RWX_WCLEAR	CLK_ADJ_REG_PARITY_ERROR: clk adj register parity bad
24	RWX_WCLEAR	DIV_REG_PARITY_ERROR: div register parity bad
25:28	RWX_WCLEAR	PLL_UNLOCK_ERROR: unlock from chiplet pll

Register Name		Hang Pulse Generation Register 0.
Mnemonic		EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.HANG_PULSE_0_REG
Address		00000000130F0020 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_0: Value of hang pulse 0. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_0: If set to '1', hang pulses are suppressed in case of a xstop

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Register Name	<i>Hang Pulse Generation Register 1.</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.HANG_PULSE_1_REG
Address	00000000130F0021 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_1: Value of hang pulse 1. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_1: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 2.</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.HANG_PULSE_2_REG
Address	00000000130F0022 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_2: Value of hang pulse 2. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_2: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 3.</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.HANG_PULSE_3_REG
Address	00000000130F0023 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_3: Value of hang pulse 3. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_3: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 4.</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.HANG_PULSE_4_REG
Address	00000000130F0024 (PCB)
Attributes	
Description	



Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_4: Value of hang pulse 4. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_4: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 5</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.HANG_PULSE_5_REG
Address	00000000130F0025 (PCB)
Attributes	
Description	This hang counter is exclusively used to generate the malfunction alert pulse.

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_5: Value of hang pulse 5. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_5: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 6</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.HANG_PULSE_6_REG
Address	00000000130F0026 (PCB)
Attributes	
Description	This hang counter is exclusively used for heartbeat generation.

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_6: Value of hang pulse 6. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_6: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Divider For Hang Counter Clock</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.PRE_COUNTER_REG
Address	00000000130F0028 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PRE_COUNTER: Divider for hang counter clock. Divides clock by n+1 (default: n=0)

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Register Name		PowerManagement GP0		
Mnemonic		EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PMGP0_REG		
Address		00000000130F0100 (PCB) 00000000130F0101 (PCB1) 00000000130F0102 (PCB2)		
Attributes				
Description				
Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PM_DISABLE: Master Switch for the PowerManagement Macro
1	RWX	WOX_AND	WOX_OR	PMGP0_SPARE_BIT1: spare bit
2	RWX	WOX_AND	WOX_OR	TP_TC_RESTART_CORE_DOMAIN: Kicks off small sequencer in OHA to get chiplet clocks back running for fast sleep without involving PORE. From GP-reg and overridden by PowMan State Machine.
3	RWX	WOX_AND	WOX_OR	DPLL_THOLD: Thold for the DPLL clock domain in the chiplet
4	RWX	WOX_AND	WOX_OR	PERV_THOLD: Thold for the Pervasive clock domain in the chiplet
5	RO	RO	RO	Reserved.
6	RO	RO	RO	Reserved.
7	RWX	WOX_AND	WOX_OR	PM_DPLL_TIMER_ENA: Select a timer instead of the DPLL lock bit for criteria to switch to DPLL. The time is defined by thold_timer_sel.
8	RWX	WOX_AND	WOX_OR	DPLL_LOCK_SENSE: DPLL lock sensitivity control (0=faster lock time, 1=slower lock time)
9	RWX	WOX_AND	WOX_OR	PMGP0_SPARE2: spare bit
10	RWX	WOX_AND	WOX_OR	DPLL_RESET: Reset to DPLL
11	RWX	WOX_AND	WOX_OR	PMGP0_SPARE_BIT11: Spare bit
12:19	RWX	WOX_AND	WOX_OR	DPLL_TESTOUT_CTL: DPLL testout control
20	RWX	WOX_AND	WOX_OR	TP_TC_CACHE2CORE_FENCE: Fence from cache to core domain in EX chiplet
21	RWX	WOX_AND	WOX_OR	TP_TC_CORE2CACHE_FENCE: Fence from core to cache domain in EX chiplet
22	RWX	WOX_AND	WOX_OR	TP_TC_PERVASIVE_ECO_FENCE: Pervasive ECO fence
23	RWX	WOX_AND	WOX_OR	CHKSW_HW257424_DISABLE: Chicken switch for interrupt retry exhausted bug (0=fix enabled, 1=fix disabled)
24:26	RWX	WOX_AND	WOX_OR	TP_CLK_ASYNC_RESET_DC: Clk async reset for three glitchless muxes, and the two clock dividers (bit 0 = master GLM, bit 1 = ECO Div2 and ECO GLM, bit 2= core Div1 and core GLM)
27:29	RWX	WOX_AND	WOX_OR	TP_CLKGLM_SEL_DC: Glitchless Mux Select for primary chiplet clock source (feeding both core and eco clock muxes) 000 = refclk, 001 = DPLL. 100 = Use constant selected by bit 34, else refclk
30	RWX	WOX_AND	WOX_OR	TP_CLKGLM_ECO_SEL_DC: Glitchless Mux Select for eco domain (cache_nclk) grid. 0= follow primary source chosen by previous field: 1 = Use constant selected by bit 34
31	ROX	NC	NC	SPECIAL_WKUP_DONE: Indicates that special wakeup is done, if asserted
32:33	RWX	WOX_AND	WOX_OR	TP_CLKGLM_CORE_SEL_DC: Glitchless Mux Select for core domain (nclk grid) mux. 0b00=primary GLS mux output, 0b10=constant input, 0b01=refclk. Valid transitions are 0b01 <-> 0b00 <-> 0b10, 0b11 is illegal



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
34	RWX	WOX_AND	WOX_OR	TP_CLKGLM_CONST_DC: Constant input available to all three ClkGlm
35:36	RWX	WOX_AND	WOX_OR	THOLD_TIMER_SEL: Selection for the thold transition timer in the IDLE state machine. 0b00=1024 cycles delay, 0b01=512 cycles delay, 0b10=256 cycles delay, 0b11= 128 cycles delay
37	RWX	WOX_AND	WOX_OR	BLOCK_ALL_WAKEUP_SOURCES: Setting this bit will make the PM Slave ignore any Wakeup events (ext. interrupt, malfunction alert, any special wakeup bit). This bit is intended to enable firmware concurrent patch capability. Note: This does NOT block the interrupt from being presented to the processor core. The following procedure is required on changes: 1. Firmware may only set this bit after first setting special wakeup and polling for special wakeup complete (OHA and PCB-slave both in running state with AISS and PM FSMs idle). 2. Firmware may only clear this bit if all special wakeup bits are first cleared.
38	RWX	WOX_AND	WOX_OR	TP_TC_DPLL_TESTMODE_DC: ADPLL test mode
39	RWX	WOX_AND	WOX_OR	PM_SLV_WINKLE_FENCE: Fence off the powered off chiplet in winkle. - Logical fence/hold for pcb_slave and pcb_slave_pm. For electrical fence see bit 23.
40	RWX	WOX_AND	WOX_OR	L3_ENABLE_SWITCH: Setting this bit activates l3_edram_enable if allowed by system configuration GP3(28). Resetting this bit deactivates l3_edram_enable.
41	RWX	WOX_AND	WOX_OR	TP_CPLT_IVRM_REFBYPASS_DC: Signal to iVRM (used to be controlled by scan-only block inside EX, but needs to be driven by VIO domain)
42	RWX	WOX_AND	WOX_OR	CHKSW_HW241939_DISABLE: if this bit is set to 1, the fix for HW241939 (pfet enable SCOM-ability) is disabled
43	RWX	WOX_AND	WOX_OR	CHKSW_HW273115_DISABLE: if this bit is set to 1, the fix for HW273115 (Pga ACK noack issue when the babystepper is in the winkle state) is disabled
44	RWX	WOX_AND	WOX_OR	CHKSW_HW245103_DISABLE: if this bit is set to 1, the fix for HW245103 resonant clocking CSB and SW -bit ordering change is disabled
45	RWX	WOX_AND	WOX_OR	CHKSW_HW257534_DISABLE: if this bit is set to 1, the fix for HW257534 (fencing of errors) is disabled
46	RWX	WOX_AND	WOX_OR	CHKSW_HW259509_ENABLE: if this bit is set to 0, the fix for HW259509 (Pstate change hanging, because of DPLL flock timer in a hung state) is disabled
47	RWX	WOX_AND	WOX_OR	CHKSW_HW260345_DISABLE: if set to 1, this bit disables the HW260345 fix (fix was to make sure that we enter bypass mode for iVRM safe mode without a glitch that could cause Vcs in regulation and Vdd in bypass)
48:49	ROX	NC	NC	WAKEUP_INT_TYPE: (Known to be unreliable and not supported, informational usage only) Type of the last wakeup event that caused an exit from sleep or winkle (excluding nap!), regardless of present state. 0b01: External interrupt. 0b10: Malfunction Alert. 0b11: Special Wakeup. 0b00: chiplet has never fully entered and exited a chiplet-level idle state since IPL of the system. (Note this does not necessarily get updated when the processor core enters an idle state, only if the PCB-Slave enters and then exits the idle state for this chiplet).
50	ROX	NC	NC	DPLL_LOCK: DPLL lock indicator
51	ROX	NC	NC	SPECIAL_WKUP_ALL_SOURCES_ORED: logical OR of all special wakeup sources
52	ROX	NC	NC	REGULAR_WKUP_AVAILABLE: logical OR of external interrupt and malfunction alert

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
53	RWX	WOX_AND	WOX_OR	BLOCK_REG_WKUP_SOURCES: blocks ext. int. and malf. Alert from waking up PCBS (no block possible for PC!)

Register Name	<i>PowerManagement GP1</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PMGP1_REG
Address	00000000130F0103 (PCB) 00000000130F0104 (PCB1) 00000000130F0105 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	SLEEP_POWER_DOWN_EN: Sleep Power Down Enable: When set to 1, causes hardware to automatically reduce voltage to the Core domain when entering Sleep mode. The voltage value for power down is chosen by sleep_power_off_sel (bit 2). When set to 0, a request is sent to the PORE engine for assistance entering Sleep.
1	RWX	WOX_AND	WOX_OR	SLEEP_POWER_UP_EN: Sleep Power Up Enable: When set to 1, enables automated hardware restoration of voltage via PFETs and, if enabled, iVRMs when exiting Sleep mode. If this bit is set to 0 the hardware rely on external means (PORE or equivalent) to restore voltage.
2	RWX	WOX_AND	WOX_OR	SLEEP_POWER_OFF_SEL: Sleep Power Off Select: Selects which voltage level to place the Core domain PFETs upon Sleep entry. 0 = Vret (Fast Sleep Mode), 1 = Voff (Deep Sleep Mode). Depending on the setting of pmicr_latency_en, this bit is controlled with a PCB-write (0) or by the PMICR in the core (1).
3	RWX	WOX_AND	WOX_OR	WINKLE_POWER_DOWN_EN: Winkle Power Down Enable: When set to 1, causes hardware to automatically reduce voltage to the entire Chiplet (both Core and ECO Domains) when entering Winkle mode. The voltage value for power down is chosen by winkle_power_off_sel (bit 5). When set to 0, a request is sent to the PORE engine for assistance entering Winkle.
4	RWX	WOX_AND	WOX_OR	WINKLE_POWER_UP_EN: Winkle Power Up Enable: When set to 1, enables automated hardware PFET enablement when exiting Winkle mode. If this bit is set to 0 the hardware rely on external means (PORE or equivalent) to cause the PFETs to be re-enabled.
5	RWX	WOX_AND	WOX_OR	WINKLE_POWER_OFF_SEL: Winkle Power Off Select: Selects which voltage level to place the Core and ECO domain PFETs upon Winkle entry. 0 = Vret (Fast Winkle Mode), 1 = Voff (Deep Winkle Mode). Depending on the setting of pmicr_latency_en, this bit is controlled with a PCB-write (0) or by the PMICR in the core (1).
6	RWX	WOX_AND	WOX_OR	OHA_WKUP_OVERRIDE_EN: Needs to be 0 for normal operation. If set to 1, the two following dials are used to override the regular and special wakeup signal from PCBS to OHA
7	RWX	WOX_AND	WOX_OR	OHA_PM_WKUP_OVERRIDE: Enablement by 'oha_wkup_override_en' forces the regular wakeup signal to OHA to the value of this bit regardless of presence of an interrupt source.
8	RWX	WOX_AND	WOX_OR	OHA_SPC_WKUP_OVERRIDE: Enablement by 'oha_wkup_override_en' forces the special wakeup signal to OHA to the value of this bit, regardless of the firmware settings.

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
9	RWX	WOX_AND	WOX_OR	ENDP_RESET_PM_ONLY: If asserted, an endpoint reset of all power management-related functions (not the regular PCB slave) is performed. Intended usage is for recovery.
10	RWX	WOX_AND	WOX_OR	DPLL_FREQ_OVERRIDE_ENABLE: override Fmax/Fmin only, if '1', using register FREQ_CTRL_REG
11	RWX	WOX_AND	WOX_OR	PM_SPR_OVERRIDE_EN: PM SPR Override Enable The PPMCR (0xNNNN) and PPMICR (0XXXXX) accesses the register resources that make up the PMCR SPR used by hypervisor to management Pstates. Thus, PCB updates to it are disabled in hardware to prevent collisions. This bit allows ownership of the PMCR to be switched from hypervisor to OCC. This switch is immediate in hardware, thus, firmware must ensure the ownership switch is otherwise communicated. 0 = Disables the writing of the PPMCR (0xNNNN) from the PCB and allows SPR 884 writes (mtspr) to update the register resource. 1 = Enables the writing of the PPMCR (0xNNNN) from the PCB.
12	RWX	WOX_AND	WOX_OR	FORCE_SAFE_MODE: Force Safe Mode 0 = Allow other enabled features to determine the operational Pstate. 1 = Forces the minimum of POHBR[psafe] and PPMISR[global_pstate_actual] Pstate for the core chiplet as the operational frequency.
13	RWX	WOX_AND	WOX_OR	IVRM_SAFE_MODE_EN: Internal VRM Safe Mode Enable 0 = Disable the iVRM safe mode, thus, no automatic actions occur, if an iVRM error happens. 1 = if the iVRMs are enabled (PIVRMCSR[ivrn_en] is set) and Pstates are enabled and if the error defined by dial pcbs_ivrm_gross_or_fine_err occurs, then the railstepper is forced into bypass mode to prevent a voltage-frequency hazard
14	RWX	WOX_AND	WOX_OR	IVRM_SAFE_MODE_FORCE_ACTIVE: Internal VRM Safe Mode Force Dial 0 = the hardware decides whether to activate the iVRM safe mode or not 1 = the iVRM safe mode is forced regardless (this makes only sense if ivrm_fsm_enable=1 and Pstates are enabled)
15	RWX	WOX_AND	WOX_OR	PMICR_LATENCY_EN: Selects how the sleep/winkle latency (which is deep/fast) is controlled. If asserted the PMICR controls the winkle/sleep_power_off_sel in PMGP1, otherwise those bits are controlled via SCOM by OCC.
16	RWX	WOX_AND	WOX_OR	ENABLE_OCC_CTRL_FOR_LOCAL_PSTATE_EFF_REQ: controls, if the HW (for value 0) or OCC (value 1) is in control of the Local Pstate Effective register in PPSTR
17	RWX	WOX_AND	WOX_OR	SERIALIZE_PFET_POWERDOWN: if asserted, the pFET sequencer will sequence the core and the ECO domain one after the other when powering down
18	RWX	WOX_AND	WOX_OR	SERIALIZE_PFET_POWERUP: if asserted, the pFET sequencer will sequence the ECO and the core domain one after the other when powering up
19	RWX	WOX_AND	WOX_OR	DISABLE_FORCE_DEEP_TO_FAST_SLEEP: 0: (normal operation) - If PCB Slave reports a recoverable error or a checkstop, a DEEP sleep operation is forced to FAST. The entries in sleep/winkle_power_off_sel remain unchanged. 1: force to FAST is disabled.

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
20	RWX	WOX_AND	WOX_OR	DISABLE_FORCE_DEEP_TO_FAST_WINKLE: 0: (normal operation) - If PCB Slave reports a recoverable error or a checkstop, a DEEP winkle operation is forced to FAST. The entries in sleep/winkle_power_off_sel remain unchanged. 1: force to FAST is disabled.

Register Name	PFET Control/Status Register For Core And ECO Vdd
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PFVDDCNTLSTAT_REG
Address	00000000130F0106 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	CORE_VDD_PFET_FORCE_STATE: Core Domain PFET Force State Provides a means for firmware to force the core domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 4:5 = 00 (both core_vdd_pfet_val_override AND core_vdd_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
2:3	RW	ECO_VDD_PFET_FORCE_STATE: ECO Domain PFET Force State Provides a means for firmware to force the ECO domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 6:7 = 00 (both eco_vdd_pfet_val_override AND eco_vdd_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
4	RW	CORE_VDD_PFET_VAL_OVERRIDE: Core Domain PFET Value Override 0 = Override is disabled
5	RW	CORE_VDD_PFET_SEL_OVERRIDE: Core Domain PFET Stage Select Override 0 = Override is disabled
6	RW	ECO_VDD_PFET_VAL_OVERRIDE: ECO Domain PFET Value Override 0 = Override is disabled
7	RW	ECO_VDD_PFET_SEL_OVERRIDE: ECO Domain PFET Stage Select Override 0 = Override is disabled
8	RW	CORE_VDD_PFET_ENABLE_REGULATION_FINGER: Core Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the core_vdd_pfet_enable_value.
9	RW	ECO_VDD_PFET_ENABLE_REGULATION_FINGER: ECO Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the eco_vdd_pfet_enable_value.



Bits	PCB	Field Mnemonic: Description
10:21	RW	CORE_VDD_PFET_ENABLE_VALUE: Core PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the Core Domain PFET Enables directly. If core_vdd_pfet_val_override = 1, a write to this field sets the state of the core PFET Enables until core_vdd_pfet_val_override is cleared. If core_vdd_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the core_vdd_pfet_valN_slat registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
22:25	RW	CORE_VDD_PFET_SEL_VALUE: Core PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure core_vdd_pfet_valN_slate(0:11) where N is 0 to 11 if core_vdd_pfet_sel_override = 1. If core_vdd_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
26:37	RW	ECO_VDD_PFET_ENABLE_VALUE: ECO PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the ECO PFET Enables directly. If ECO_vdd_pfet_val_override = 1, a write to this field sets the state of the ECO PFET Enables until ECO_vdd_pfet_val_override is cleared. If eco_vdd_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the eco_vdd_pfet_valN_slat registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
38:41	RW	ECO_VDD_PFET_SEL_VALUE: ECO PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure eco_vdd_pfet_valN_slate(0:11) where N is 0 to 11 if eco_vdd_pfet_sel_override = 1. If eco_vdd_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
42:45	ROX	CORE_VDD_PG_STATE: Core power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
46:49	ROX	CORE_VDD_PG_SEL: For debug, contains the actual index n into Core Domain PFET Value [n] SLAT Register set that contains the Core PFET Enable Value currently enabled.
50:53	ROX	ECO_VDD_PG_STATE: ECO Domain power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
54:57	ROX	ECO_VDD_PG_SEL: For debug, contains the actual index n into ECO Domain PFET Value [n] SLAT Register set that contains the ECO PFET Enable Value currently enabled.

Register Name	PFET Sense Register	
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PFSENSE_REG	
Address	00000000130F0107 (PCB)	
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:11	ROX	TP_CORE_VDD_PFET_ENABLE_SENSE: Not used any more.
12:23	ROX	TP_ECO_VDD_PFET_ENABLE_SENSE: Not used any more.



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Bits	PCB	Field Mnemonic: Description
24:35	ROX	TP_CORE_VCS_PFET_ENABLE_SENSE: Not used any more.
36:47	ROX	TP_ECO_VCS_PFET_ENABLE_SENSE: Not used any more.

Register Name	<i>PM Error Summary Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PMERRSUM_REG
Address	00000000130F0108 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	PM_ERROR: PM Error is present. Intended for use by special PCB multicast to see error state of all chiplets with a single read (via 510F0108 to read all chiplets)

Register Name	<i>PM Error Register:</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PMERR_REG
Address	00000000130F0109 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_HANG_ERR: Hang during Unassisted Sleep Entry: SLEEP_ENTRY_NOTIFY_PMC state
1	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ASSIST_HANG_ERR: Hang during Assisted Sleep Entry: SLEEP_ENTRY_NOTIFY_PMC_ASSIST state
2	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ERR: Hang during Unassisted Sleep Exit: SLEEP_EXIT_NOTIFY_PMC state
3	ROX	PCBS_SLEEP_EXIT_INVOKE_PORE_ERR: Hang during Assisted Deep Sleep Exit: SLEEP_EXIT_INVOKE_PORE state
4	ROX	PCBS_WINKLE_ENTRY_NOTIFY_PMC_ERR: Hang during Unassisted Winkle Entry: WINKLE_ENTRY_NOTIFY_PMC state
5	ROX	PCBS_WINKLE_ENTRY_SEND_INT_ASSIST_ERR: Hang during Assisted Winkle Entry: WINKLE_ENTRY_SEND_INT_ASSIST state
6	ROX	PCBS_WINKLE_EXIT_NOTIFY_PMC_ERR: Hang during Unassisted Winkle Exit: WINKLE_EXIT_NOTIFY_PMC state
7	ROX	PCBS_WAIT_DPLL_LOCK_ERR: Hang during Unassisted Exit waiting on DPLL: WAIT_DPLL_LOCK state
8	ROX	PCBS_SPARE8_ERR: spare bit, always 0
9	ROX	PCBS_WINKLE_EXIT_SEND_INT_ASSIST_ERR: Hang during Assisted Winkle Exit: WINKLE_EXIT_SEND_INT_ASSIST state
10	ROX	PCBS_WINKLE_EXIT_SEND_INT_POWUP_ASSIST_ERR: Hang during Assisted Winkle Exit: WINKLE_EXIT_SEND_INT_POWUP_ASSIST state
11	ROX	PCBS_WRITE_FSM_GOTO_REG_IN_INVALID_STATE_ERR: write to FSM goto register in invalid state
12	ROX	PCBS_WRITE_PMGP0_IN_INVALID_STATE_ERR: write to PMGP0 in invalid state



Bits	PCB	Field Mnemonic: Description
13	ROX	PCBS_FREQ_OVERFLOW_IN_PSTATE_MODE_ERR: frequency of DPLL in Pstate mode overflows (Fnom + desired Pstate > 511)
14	ROX	PCBS_ECO_RS_BYPASS_CONFUSION_ERR: ECO railstepper tried to exit Vcs bypass and enter Vdd bypass in one Pstate step (it is not clear, in which order this strange operation should be performed - most likely it should never happen to avoid that Vcs is greater than Vdd)
15	ROX	PCBS_CORE_RS_BYPASS_CONFUSION_ERR: same as previous error, but for core railstepper (it is not clear, in which order this strange operation should be performed - most likely it should never happen to avoid that Vcs is greater than Vdd)
16	ROX	PCBS_READ_LPST_IN_PSTATE_MODE_ERR: read LPST-array while iVRM FSMs are enabled (dial ivrm_fsm_enable asserted)
17	ROX	PCBS_LPST_READ_CORR_ERR: correctable error occurred when reading the LPST
18	ROX	PCBS_LPST_READ_UNCORR_ERR: uncorrectable error occurred when reading the LPST
19	ROX	PCBS_PFET_STRENGTH_OVERFLOW_ERR: overflow occurred when calculating the pFET strength (in final rounding step!)
20	ROX	PCBS_VDS_LOOKUP_ERR: Vds entry not found in lookup table (when performing the linear search!)
21	ROX	PCBS_IDLE_INTERRUPT_TIMEOUT_ERR: idle interrupt timeout in PCB interrupt controller
22	ROX	PCBS_PSTATE_INTERRUPT_TIMEOUT_ERR: PState interrupt timeout in PCB interrupt controller
23	ROX	PCBS_GLOBAL_ACTUAL_SYNC_INTERRUPT_TIMEOUT_ERR: GlobalActualSync Interrupt timeout in PCB interrupt controller
24	ROX	PCBS_PMAX_SYNC_INTERRUPT_TIMEOUT_ERR: PmaxSync Interrupt timeout in PCB interrupt controller
25	ROX	PCBS_GLOBAL_ACTUAL_PSTATE_PROTOCOL_ERR: a write to global actual Pstate register has occurred before the global actual Pstate interrupt has left PCBS
26	ROX	PCBS_PMAX_PROTOCOL_ERR: a write to the Pmax/Pmin register has occurred before the Pmax sync interrupt has left PCB
27	ROX	PCBS_IVRM_GROSS_OR_FINE_ERR: iVRM gross or fine error (details to be found in PCBS_ivrm_Control_Status_Reg)
28	ROX	PCBS_IVRM_RANGE_ERR: iVRM range error (summary bit, details to be found in PCBS_ivrm_Control_Status_Reg)
29	ROX	PCBS_DPLL_CPM_FMIN_ERR: DPLL CPM Fmin error
30	ROX	PCBS_DPLL_DCO_FULL_ERR: DPLL DCO full
31	ROX	PCBS_DPLL_DCO_EMPTY_ERR: DPLL DCO empty
32	ROX	PCBS_DPLL_INT_ERR: DPLL internal error
33	ROX	PCBS_FMIN_AND_NOT_CPMBIT_ERR: dpll_fmin_and_not_cpmbit (ref. to dial cpm_fmin_clip_error_sel on how to configure this)
34	ROX	PCBS_DPLL_FASTER_THAN_FMAX_PLUS_DELTA1_ERR: dpll_faster_than_fmax_plus_delta1 (for characterization, delta1 is configurable with pll_char_delta1)
35	ROX	PCBS_DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2_ERR: dpll_slower_than_fmin_minus_delta2 (for characterization, delta2 is configurable with pll_char_delta2)
36	ROX	PCBS_RESCLK_CSB_INSTR_VECTOR_CHG_IN_INVALID_STATE_ERR: RESCLK CSB instruction vector change while FSMs none idle
37	ROX	PCBS_RESCLK_BAND_BOUNDARY_CHG_IN_INVALID_STATE_ERR: RESCLK Band boundaries change while FSMs none idle
38	ROX	PCBS_OCC_HEARTBEAT_LOSS_ERR: OCC heartbeat loss
39	ROX	PCBS_SPARE39_ERR: spare bit, always 0
40	ROX	PCBS_SPARE40_ERR: spare bit, always 0



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Bits	PCB	Field Mnemonic: Description
41	ROX	PCBS_SPARE41_ERR: spare bit, always 0
42	ROX	PCBS_SPARE42_ERR: spare bit, always 0

Register Name	<i>PM Error Mask Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PMERRMASK_REG
Address	00000000130F010A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_HANG_ERR_MASK: Mask for this error: 1=masked, 0=not masked
1	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ASSIST_HANG_ERR_MASK: Mask for this error: 1=masked, 0=not masked
2	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
3	RW	PCBS_SLEEP_EXIT_INVOKE_PORE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
4	RW	PCBS_WINKLE_ENTRY_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
5	RW	PCBS_WINKLE_ENTRY_SEND_INT_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
6	RW	PCBS_WINKLE_EXIT_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
7	RW	PCBS_WAIT_DPLL_LOCK_ERR_MASK: Mask for this error: 1=masked, 0=not masked
8	RW	PCBS_SPARE8_ERR_MASK: Mask for this error: 1=masked, 0=not masked
9	RW	PCBS_WINKLE_EXIT_SEND_INT_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
10	RW	PCBS_WINKLE_EXIT_SEND_INT_POWUP_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
11	RW	PCBS_WRITE_FSM_GOTO_REG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
12	RW	PCBS_WRITE_PMGPO_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
13	RW	PCBS_FREQ_OVERFLOW_IN_PSTATE_MODE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
14	RW	PCBS_ECO_RS_BYPASS_CONFUSION_ERR_MASK: Mask for this error: 1=masked, 0=not masked
15	RW	PCBS_CORE_RS_BYPASS_CONFUSION_ERR_MASK: Mask for this error: 1=masked, 0=not masked
16	RW	PCBS_READ_LPST_IN_PSTATE_MODE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
17	RW	PCBS_LPST_READ_CORR_ERR_MASK: Mask for this error: 1=masked, 0=not masked
18	RW	PCBS_LPST_READ_UNCORR_ERR_MASK: Mask for this error: 1=masked, 0=not masked
19	RW	PCBS_PFET_STRENGTH_OVERFLOW_ERR_MASK: Mask for this error: 1=masked, 0=not masked
20	RW	PCBS_VDS_LOOKUP_ERR_MASK: Mask for this error: 1=masked, 0=not masked
21	RW	PCBS_IDLE_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
22	RW	PCBS_PSTATE_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
23	RW	PCBS_GLOBAL_ACTUAL_SYNC_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
24	RW	PCBS_PMAX_SYNC_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked



Bits	PCB	Field Mnemonic: Description
25	RW	PCBS_GLOBAL_ACTUAL_PSTATE_PROTOCOL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
26	RW	PCBS_PMAX_PROTOCOL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
27	RW	PCBS_IVRM_GROSS_OR_FINE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
28	RW	PCBS_IVRM_RANGE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
29	RW	PCBS_DPLL_CPM_FMIN_ERR_MASK: Mask for this error: 1=masked, 0=not masked
30	RW	PCBS_DPLL_DCO_FULL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
31	RW	PCBS_DPLL_DCO_EMPTY_ERR_MASK: Mask for this error: 1=masked, 0=not masked
32	RW	PCBS_DPLL_INT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
33	RW	PCBS_FMIN_AND_NOT_CPMBIT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
34	RW	PCBS_DPLL_FASTER_THAN_FMAX_PLUS_DELTA1_ERR_MASK: Mask for this error: 1=masked, 0=not masked
35	RW	PCBS_DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2_ERR_MASK: Mask for this error: 1=masked, 0=not masked
36	RW	PCBS_RESCLK_CSB_INSTR_VECTOR_CHG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
37	RW	PCBS_RESCLK_BAND_BOUNDARY_CHG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
38	RW	PCBS_OCC_HEARTBEAT_LOSS_ERR_MASK: Mask for this error: 1=masked, 0=not masked
39	RW	PCBS_SPARE39_ERR_MASK: Mask for this error: 1=masked, 0=not masked
40	RW	PCBS_SPARE40_ERR_MASK: Mask for this error: 1=masked, 0=not masked
41	RW	PCBS_SPARE41_ERR_MASK: Mask for this error: 1=masked, 0=not masked
42	RW	PCBS_SPARE42_ERR_MASK: Mask for this error: 1=masked, 0=not masked

Register Name		<i>PM Special Wakeup FSP</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PMSPCWKUPFSP_REG
Address		00000000130F010B (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RW	FSP_SPECIAL_WAKEUP: Chiplet Special Wakeup for FSP Firmware use. NOTE: protocol is required when setting this bit

Register Name		<i>PM Special Wakeup OCC</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PMSPCWKUPOCC_REG
Address		00000000130F010C (PCB)
Attributes		
Description		

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Bits	PCB	Field Mnemonic: Description
0	RW	OCC_SPECIAL_WAKEUP: Chiplet Special Wakeup for OCC Firmware use. NOTE: protocol is required when setting this bit

Register Name	<i>PM Special Wakeup Hypervisor</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PMSPCWKUPPHYP_REG
Address	00000000130F010D (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	PHYP_SPECIAL_WAKEUP: Chiplet Special Wakeup for hypervisor Firmware use. NOTE: protocol is required when setting this bit

Register Name	<i>PFET Control/Status Register For Core And ECO Vcs</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PFVCSCTLSTAT_REG
Address	00000000130F010E (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	CORE_VCS_PFET_FORCE_STATE: Core Domain PFET Force State Provides a means for firmware to force the core domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 4:5 = 00 (both core_vcs_pfet_val_override AND core_vcs_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
2:3	RW	ECO_VCS_PFET_FORCE_STATE: ECO Domain PFET Force State Provides a means for firmware to force the ECO domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 6:7 = 00 (both eco_vcs_pfet_val_override AND eco_vcs_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
4	RW	CORE_VCS_PFET_VAL_OVERRIDE: Core Domain PFET Value Override 0 = Override is disabled
5	RW	CORE_VCS_PFET_SEL_OVERRIDE: Core Domain PFET Stage Select Override 0 = Override is disabled
6	RW	ECO_VCS_PFET_VAL_OVERRIDE: ECO Domain PFET Value Override 0 = Override is disabled
7	RW	ECO_VCS_PFET_SEL_OVERRIDE: ECO Domain PFET Stage Select Override 0 = Override is disabled

Bits	PCB	Field Mnemonic: Description
8	RW	CORE_VCS_PFET_ENABLE_REGULATION_FINGER: Core Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the core_vcs_pfet_enable_value.
9	RW	ECO_VCS_PFET_ENABLE_REGULATION_FINGER: ECO Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the eco_vcs_pfet_enable_value.
10:21	RW	CORE_VCS_PFET_ENABLE_VALUE: Core PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the Core Domain PFET Enables directly. If core_vcs_pfet_val_override = 1, a write to this field sets the state of the core PFET Enables until core_vcs_pfet_val_override is cleared. If core_vcs_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the core_vcs_pfet_valN_slat registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
22:25	RW	CORE_VCS_PFET_SEL_VALUE: Core PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure core_vcs_pfet_valN_slate(0:11) where N is 0 to 11 if core_vcs_pfet_sel_override = 1. If core_vcs_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
26:37	RW	ECO_VCS_PFET_ENABLE_VALUE: ECO PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the ECO PFET Enables directly. If ECO_vcs_pfet_val_override = 1, a write to this field sets the state of the ECO PFET Enables until ECO_vcs_pfet_val_override is cleared. If eco_vcs_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the eco_vcs_pfet_valN_slat registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
38:41	RW	ECO_VCS_PFET_SEL_VALUE: ECO PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure eco_vcs_pfet_valN_slate(0:11) where N is 0 to 11 if eco_vcs_pfet_sel_override = 1. If eco_vcs_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
42:45	ROX	CORE_VCS_PG_STATE: Core power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
46:49	ROX	CORE_VCS_PG_SEL: For debug, contains the actual index n into Core Domain PFET Value [n] SLAT Register set that contains the Core PFET Enable Value currently enabled.
50:53	ROX	ECO_VCS_PG_STATE: ECO Domain power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
54:57	ROX	ECO_VCS_PG_SEL: For debug, contains the actual index n into ECO Domain PFET Value [n] SLAT Register set that contains the ECO PFET Enable Value currently enabled.

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Register Name	<i>PM State History Register For Hypervisor</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPHYP_REG
Address	00000000130F0110 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	PHYP_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPART	PHYP_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPART	PHYP_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPART	PHYP_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPART	PHYP_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPART	PHYP_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For FSP</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PMSTATEHISTFSP_REG
Address	00000000130F0111 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	FSP_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPART	FSP_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPART	FSP_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPART	FSP_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.



Bits	PCB	Field Mnemonic: Description
6	ROX_CLRPAR T	FSP_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	FSP_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For OCC</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PMSTATEHISTOCC_REG
Address	00000000130F0112 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	OCC_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	OCC_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	OCC_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	OCC_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	OCC_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	OCC_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For PerfMon</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPERF_REG
Address	00000000130F0113 (PCB)
Attributes	
Description	

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Bits	PCB	Field Mnemonic: Description
0:2	ROX	PERF_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	PERF_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	PERF_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	PERF_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	PERF_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	PERF_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM FSM Reset And Babystepper Idle Injects</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.IDLEFSMGOTOCMD_REG
Address	00000000130F0114 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	WO_1P	idle_fsm_goto_cmd ' A write to this reg will proceed the IDLE FSM from WAIT_FOR_PORE_DONE, SLEEP_EXIT_WAIT_FOR_PORE_FAST_EXIT_DONE, or WINKLE_EXIT_WAIT_FOR_PORE_FAST_EXIT_DONE to the following states: ' 0b01: goto IDLE state ' 0b10: goto SLEEP_EXIT_CORE_MESHLET_ON state ' 0b11: goto WINKLE_EXIT_NOTIFY_PMC state ' "
2	RWX	babystp_trigger_sleep_entry ' A write to this reg with a 1 in this field will cause the babystepper to run the sleep entry sequence. This step is needed for an assisted entry into sleep, before the power is actually turned off since the babystepper needs to know about the sleep state. For an unassisted entry, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished entering its sleep mode. ' "
3	RWX	babystp_trigger_winkle_entry ' A write to this reg with a 1 in this field will cause the babystepper to run the winkle entry sequence. This step is needed for an assisted entry into winkle before the power is actually turned off since the babystepper needs to know about the winkle state. For an unassisted entry, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished entering its winkle mode. ' "
4	RWX	babystp_trigger_wakeup ' A write to this reg with a 1 in this field will cause the babystepper to run the wakeup sequence from sleep/winkle depending on the babystepper state of sleep or winkle. This step is needed for an assisted exit from winkle before the power is actually turned off since the babystepper needs to know about the wakeup state. For an unassisted exit, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished waking up from sleep or winkle. ' "



Register Name	<i>Core PFET Power Up Delay</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.COREPFPUDLY_REG
Address	00000000130F012C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_POWUP_DLY0: Delay used after transitioning to Core Domain power up sequence stage0. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	CORE_POWUP_DLY1: Delay used after transitioning to Core domain power up sequence stage1.
8:19	RW	CORE_POWER_UP_DELAY_SEL: Vector select for which delay to use for the respective power-up stage. Bit mapping: 8 -> core_*_pfet_enable(0) 9 -> core_*_pfet_enable(1) ... 19 -> core_*_pfet_enable(11) Bit meaning: 0 = Use core_powup_dly0 1 = Use core_powup_dly1

Register Name	<i>Core PFET Power Down Delay</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.COREPFPDDLY_REG
Address	00000000130F012D (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_POWDN_DLY0: Delay used after transitioning to Core domain power dn sequence stage1. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	CORE_POWDN_DLY1: Delay used after transitioning to Core domain power dn sequence stage1. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
8:19	RW	CORE_POWER_DN_DELAY_SEL: Vector select for which delay to use for the respective power-dn stage. Bit mapping: 8 -> core_*_pfet_enable(0) 9 -> core_*_pfet_enable(1) ... 19 -> core_*_pfet_enable(11) Bit meaning: 0 = Use core_powdn_dly0 1 = Use core_powdn_dly1

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Register Name	Core PFET Vretention
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.COREPFVRET_REG
Address	00000000130F0130 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_VRET_SEL: Pointer to the stage representing the Vretention value for the core PFETs. Power down sequences will stop after enabling this stage.
4:7	RW	CORE_VOFF_SEL: Pointer to the stage representing the Voff value for the core PFETs. Power down sequences will stop after enabling this stage.

Register Name	ECO PFET Power Up Delay
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.ECOPFPUDLY_REG
Address	00000000130F014C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_POWUP_DLY0: Delay used after transitioning to ECO domain power up sequence stage0 in terms of refclk period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	ECO_POWUP_DLY1: Delay used after transitioning to ECO domain power up sequence stage1.
8:19	RW	ECO_POWER_UP_DELAY_SEL: Vector select for which delay to use for the respective power-up stage. Bit mapping: 8 -> eco_*_pfet_enable(0) 9 -> eco_*_pfet_enable(1) ... 19 -> eco_*_pfet_enable(11) Bit meaning: 0 = Use eco_powup_dly0 1 = Use eco_powup_dly1

Register Name	ECO PFET Power Down Delay
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.ECOPFPDDLY_REG
Address	00000000130F014D (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_POWDN_DLY0: UNUSED/SPARE
4:7	RW	ECO_POWDN_DLY1: Delay used after transitioning to ECO Domain power dn sequence stage1. The delays in this register are in terms of refclk period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.

Bits	PCB	Field Mnemonic: Description
8:19	RW	ECO_POWER_DN_DELAY_SEL: Vector select for which delay to use for the respective power-down stage. Bit mapping: 8 -> eco_*_pfet_enable(0) 9 -> eco_*_pfet_enable(1) ... 19 -> eco_*_pfet_enable(11) Bit meaning: 0 = Use eco_powdn_dly0 1 = Use eco_powdn_dly1

Register Name		<i>ECO PFET Vretention</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.ECOPFVRET_REG
Address		00000000130F0150 (PCB)
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_VRET_SEL: Pointer to the stage representing the Vretention value for the ECO PFETs. Power down sequences will stop after enabling this stage.
4:7	RW	ECO_VOFF_SEL: Pointer to the stage representing the Voff value for the ECO PFETs. Power down sequences will stop after enabling this stage.

Register Name		<i>Frequency Control Register With Overrides For DPLL.</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.FREQ_CTRL_REG
Address		00000000130F0151 (PCB)
Attributes		
Description		Note that overrides to Dpll_fmax are only applied if Dpll_freq_override_enable = 1. A read of all these dials always returns the currently established DPLL frequencies (regardless of any other mode settings).

Bits	PCB	Field Mnemonic: Description
0:8	RWX	DPLL_FMIN: minimum DPLL frequency in CPM-DPLL mode that is set at IPL time A read always returns the currently established value A write is not conditioned on any other dial setting.
9:17	RWX	DPLL_FMAX: DPLL maximum frequency and frequin (these two values are the same in POWER8 processor) without applying bias values: A read always returns the currently established value A write is conditioned on the setting of dpll_freq_override_enable. If dpll_freq_override_enable is asserted, a write causes this field to update. Otherwise the hardware (that is, PStates) are controlling the update of this value.
18:21	RO	Reserved.
22:30	RW	FREQU_AT_PSTATE0: DPLL frequency for Pstate 0

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Register Name	<i>DPLL Mode Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.DPLL_CPM_PARM_REG
Address	00000000130F0152 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	LF_SLEWRATEXPI: out of lock slew rate for DPLL
8	RW	LF_USE_CPMXPI: use CPM instead of PFD as loop filter input, if '1' (instead of using both)
9	RW	FF_USE_CPMXPI: use the CPM inputs for the frequency filter, if '1'
10	RW	CPM_FILTER_ENABLE: enables the CPM filter
11	RW	FF_BYPASSXPI: enables frequency filter bypass
12	RW	DCO_OVERRIDE: enables overrides for DCO testing/characterization
13	RW	DCO_INCR: enables increment for DCO testing/characterization, increments only on a rising edge
14	RW	DCO_DECR: enables decrement for DCO testing/characterization, decrements only on a rising edge
15:23	RW	DPLL_LOCK_TIMER_REPLACEMENT_VALUE: if dpll_lock_replacement_timer_mode_en is set, this dial specifies the delay in us, after which it is assumed, that the DPLL has reached a frequency lock condition. Note that values less than 3 will cause in undefined HW behavior (0 will cause HANGs!). if dpll_lock_replacement_timer_mode_en is zero, this dial specifies the delay in pcb_nclk cycles after which the hardware monitors the DPLL frequout output (if dpll_freqout_mode_en is set) or the DPLL flock output (if dpll_flock_mode_en is set). Note that in this case, the value of this dial needs to be greater or equal to 150 (decimal).
24:31	RW	PRE_VRET_PSTATE: Pstate that is stepped to before switching to Vretention defined in PCBS_iVRM_Control_Status_Reg
32	RW	OVERRIDE_PCBS_DPLL_SYNCHRONIZER: Bypasses the 'ping-pong' synchronization logic between the DPLL and the PCBS-PM. NEVER SET TO 1 UNLESS YOU KNOW WHAT YOU ARE DOING!
33:36	RW	DPLL_CHAR_DELTA1: Delta in DPLL ticks for characterization (cf. dial dpll_faster_than_fmax_plus_delta1)
37:40	RW	DPLL_CHAR_DELTA2: Delta in DPLL ticks for characterization (cf. dial dpll_faster_than_fmin_minus_delta2)

Register Name	<i>PPMSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_STATUS_REG
Address	00000000130F0153 (PCB)
Attributes	
Description	The PPMSR provides read access to the power management status that is also shadowed to the PC and visible to the hypervisor in the PMSR (with some delay due to the shadowing process).

Bits	PCB	Field Mnemonic: Description
0:7	ROX	global_pstate_actual ' Actual Global Pstate Pstate or Pglobal_actual' " 'Reads from this field return the presently established global PState value.' " 'Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent '

Bits	PCB	Field Mnemonic: Description
8:15	ROX	LOCAL_PSTATE_ACTUAL: ' Actual Local PState or Plocal_actual' " 'Reads from this field return the presently established local PState value. This value will always be less than or equal to global_pstate_actual.' " 'Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent' "
16:23	ROX	pv_min Minimum Pstate set by the platform.
24:31	ROX	pvf_max Maximum Pstate set by the platform.
32	ROX	spr_em_disabled ' SPR Energy Management Disabled' 'Read from this field indicate whether the platform has disabled the ' 'PMCR and PMICR SPRs to control the chiplet PState. '
33	ROX	Psafe_mode_active Read from this field indicate whether the chiplet has been put into a safe mode with Psafe enabled to a OCC heartbeat loss or other externally forced reasons (0=regular mode, 1=safe mode is active)
34	ROX	iVRM_safe_mode_active Read from this field indicate whether the chiplet has been put the iVRM safe mode (forcing the bypass mode for all iVRMs)
35	ROX	ivrm_enable Read from this field indicate whether the chiplet internal voltage regulation macro is enabled for localized voltage control (0=disabled, 1=enabled) based on ANDing the poweron signals to the iVRMs
36	ROX	all_fsms_in_safe_state For recovery: if this bit is asserted, all Pstate and iVRM control FSMs are in a stable, safe state that allows the recovery routine to proceed with resetting the PCBS PM without the risk of interrupt a critical action
37:40	ROX	pmsr_spares spare bits

Register Name	<i>PIVRMCSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_CONTROL_STATUS_REG
Address	00000000130F0154 (PCB)
Attributes	
Description	The PIVRMCSR provides access to chiplet-level controls of the internal VRM rail set (VDD and VCS) across both the core and ECO domains. The following is valid only for bits 4 to 7: When in automatic iVRM mode (ivrm_fsm_enable = 1), these bits provide access to the values established by the automatic hardware mechanism. When in iVRM override mode (ivrm_fsm_enable = 0), these bits allow firmware direct control of the values driving the internal VRMs.

Bits	PCB	Field Mnemonic: Description
0	RW	IVRM_FSM_ENABLE: Internal master VRM FSM Enable 0 = Disable Internal VRM FSMs and enable to control the iVRMs with the available override registers (SCOMable) as a backup mode or for setup (override mode) 1 = Enable Internal VRM FSM sequencers (requires that Pstates are enabled with enable_Pstate_mode=1 as well) (automatic mode)
1	RW	USE_IVRM_FOR_VRET: Internal VRM Enabled for Vretention 0 = Disable Internal VRM for Vretention 1 = Enable Internal VRM for Vretention
2	RW	BINSEARCH_CAL_ENA: trigger binary search (level signal)

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Bits	PCB	Field Mnemonic: Description
3	RW	PVREF_EN: Internal VRM Power Voltage Reference Forced Enable 0 = Allow hardware to enable/disable pvref circuit 1 = Force enablement of the pvref circuit
4	RWX	IVRM_CORE_VDD_BYPASS_B: Internal VRM Core VDD Bypass (negative active) 0 = VDD Internal Core VRMs in bypass 1 = VDD internal Core VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
5	RWX	IVRM_CORE_VDD_POWERON: Internal VRM Core VDD Poweron 0 = Core VDD Internal VRMs powered off 1 = Core VDD internal VRMs powered on if this bit is not set (=0), the Core VDD internal VRM powered off internally. If this bit is set (=1), the Core VDD internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
6	RWX	IVRM_CORE_VCS_BYPASS_B: Internal VRM Core VCS Bypass (negative active) 0 = VCS Internal Core VRMs in bypass 1 = VCS internal Core VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VCS internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VCS internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
7	RWX	IVRM_CORE_VCS_POWERON: Internal VRM Core VCS Poweron 0 = Core VCS Internal VRMs powered off 1 = Core VCS internal VRMs powered on if this bit is not set (=0), the Core VCS internal VRM powered off internally. If this bit is set (=1), the Core VCS internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
8	RWX	IVRM_ECO_VDD_BYPASS_B: Internal VRM ECO VDD Bypass (negative active) 0 = VDD Internal ECO VRMs in bypass 1 = VDD internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
9	RWX	IVRM_ECO_VDD_POWERON: Internal VRM ECO VDD Bypass (negative active) 0 = VDD Internal ECO VRMs in bypass 1 = VDD internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.

Bits	PCB	Field Mnemonic: Description
10	RWX	IVRM_ECO_VCS_BYPASS_B: Internal VRM ECO VCS Bypass (negative active) 0 = VCS Internal ECO VRMs in bypass 1 = VCS internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VCS internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VCS internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
11	RWX	IVRM_ECO_VCS_POWERON: Internal VRM ECO VCS Poweron 0 = ECO VCS Internal VRMs powered off 1 = ECO VCS internal VRMs powered on if this bit is not set (=0), the ECO VCS internal VRM powered off internally. If this bit is set (=1), the ECO VCS internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
12:18	RWX	IVRM_VRET_VDD: if use_ivrm_for_Vret is asserted, this dial is used to control the Vdd retention voltage. Note: this field will establish the Core VDD rail for Sleep and both the Core and ECO rail for Winkle. - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
19:25	RWX	IVRM_VRET_VCS: if use_ivrm_for_Vret is asserted, this dial is used to control the Vcs retention voltage. Note: this field will establish the Core VDD rail for Sleep and both the Core and ECO rail for Winkle. - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
26:30	RWX	IVRM_VRET_CORE_VDD_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the Core Vdd iVRM PFET strength for the retention voltage
31:35	RWX	IVRM_VRET_CORE_VCS_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the Core Vcs iVRM PFET strength for the retention voltage
36:40	RWX	IVRM_VRET_ECO_VDD_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the ECO Vdd iVRM PFET strength for the retention voltage
41:45	RWX	IVRM_VRET_ECO_VCS_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the ECO Vcs iVRM PFET strength for the retention voltage
46	RW	PVREF_FAIL: voltage reference fail input to iVRMs
47	ROX	IVRM_PREF_ERROR_GROSS: Voltage Reference Gross Error 0 = Gross Error not detected 1 = Gross Error detected
48	ROX	IVRM_PREF_ERROR_FINE: Voltage Reference Fine Error 0 = Fine Error not detected 1 = Fine Error detected
49	ROX	IVRM_CORE_VDD_RANGE_HI: Core VDD Internal VRM Range Hi Indicator 0 = Core VDD Internal VRM Hi indicator signal not asserted 1 = Core VDD internal VRMs Hi indicator signal asserted
50	ROX	IVRM_CORE_VDD_RANGE_LO: Core VDD Internal VRM Range Low Indicator 0 = Core VDD Internal VRM Low indicator signal not asserted 1 = Core VDD internal VRMs Low indicator signal asserted

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Bits	PCB	Field Mnemonic: Description
51	ROX	IVRM_ECO_VDD_RANGE_HI: ECO VDD Internal VRM Range Hi Indicator 0 = ECO VDD Internal VRM Hi indicator signal not asserted 1 = ECO VDD internal VRMs Hi indicator signal asserted
52	ROX	IVRM_ECO_VDD_RANGE_LO: ECO VDD Internal VRM Range Low Indicator 0 = ECO VDD Internal VRM Low indicator signal not asserted 1 = ECO VDD internal VRMs Low indicator signal asserted
53	ROX	IVRM_CORE_VCS_RANGE_HI: Core VCS Internal VRM Range Hi Indicator 0 = Core VCS Internal VRM Hi indicator signal not asserted 1 = Core VCS internal VRMs Hi indicator signal asserted
54	ROX	IVRM_CORE_VCS_RANGE_LO: Core VCS Internal VRM Range Low Indicator 0 = Core VCS Internal VRM Low indicator signal not asserted 1 = Core VCS internal VRMs Low indicator signal asserted
55	ROX	IVRM_ECO_VCS_RANGE_HI: ECO VCS Internal VRM Range Hi Indicator 0 = ECO VCS Internal VRM Hi indicator signal not asserted 1 = ECO VCS internal VRMs Hi indicator signal asserted
56	ROX	IVRM_ECO_VCS_RANGE_LO: ECO VCS Internal VRM Range Low Indicator 0 = ECO VCS Internal VRM Low indicator signal not asserted 1 = ECO VCS internal VRMs Low indicator signal asserted
57	ROX	BINSEARCH_CAL_DONE: binary search done signal
58	RWX	IVRM_CORE_VDD_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
59	RWX	IVRM_CORE_VCS_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
60	RWX	IVRM_ECO_VDD_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
61	RWX	IVRM_ECO_VCS_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
62	RW	IVRM_POWER_DOWN_DISABLE: If this bit is 1, the iVRM poweron signal is left asserted. Power off of the iVRMs is then blocked



Register Name	PIVRMVSR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VALUE_SETTING_REG
Address	00000000130F0155 (PCB)
Attributes	
Description	The PIVRMVSR allows access to VID values and PFET strength valid signal settings presented to the internal VRM rail set (VDD and VCS) across both the core and ECO domains. When In Ivrsm_fsm_enable = "auto" mode, this register provides access to the values established by the automatic hardware mechanism. When Ivrsm_fsm_enable = "override" mode, this register allows firmware direct control of the values driving the internal VRMs which, if the VRMs are not in bypass, will move the voltage settings.

Bits	PCB	Field Mnemonic: Description
0:7	RWX	IVRM_CORE_VDD_IVID: When read, returns the value presently being driving to the Core VDD iVRM. If Ivrsm_fsm_enable = 0 (override_mode), then writes to this field will drive a new VID value to the Core VDD iVRM. If Ivrsm_fsm_enable = 1, writes to this field are not performed. 0 = Reserved 1:7 = ivid_vdd - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
8:15	RWX	IVRM_CORE_VCS_IVID: When read, returns the value presently being driving to the Core VCS iVRM. If Ivrsm_fsm_enable = 0 (override_mode), then writes to this field will drive a new VID value to the Core VCS iVRM. If Ivrsm_fsm_enable = 1, writes to this field are not performed. 0 = Reserved 1:7 = ivid_vdd - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
16:23	RWX	IVRM_ECO_VDD_IVID: When read, returns the value presently being driving to the Core VDD iVRM. If Ivrsm_fsm_enable = 0 (override_mode), then writes to this field will drive a new VID value to the ECO VDD iVRM. If Ivrsm_fsm_enable = 1, writes to this field are not performed. 0 = Reserved 1:7 = ivid_vdd - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
24:31	RWX	IVRM_ECO_VCS_IVID: When read, returns the value presently being driving to the ECO VCS iVRM. If Ivrsm_fsm_enable = 0 (override_mode), then writes to this field will drive a new VID value to the ECO VCS iVRM. If Ivrsm_fsm_enable = 0, writes to this field are not performed. 0 = Reserved 1:7 = ivid_vdd - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
32:36	RWX	IVRM_CORE_VDD_PFET_STRENGTH: When read, returns the value presently being driving to the core VCS iVRM. If Ivrsm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the core VCS iVRM. If Ivrsm_fsm_enable = 0, writes to this field are not performed.

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Bits	PCB	Field Mnemonic: Description
37:41	RWX	IVRM_CORE_VCS_PFET_STRENGTH: This register is assigned to the signals tcex##_tp_ivrm_core_vcs_sense & tcex##_tp_ivrm_core_vdd_sense & tcex##_tp_ivrm_eco_vcs_sense & tcex##_tp_ivrm_eco_vdd_sense & 0b0 Note that all other sense signals are spares now and tied to 0. OUTDATED TEXT: When read, returns the value presently being driving to the core VDD iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the core VDD iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
42:46	RWX	IVRM_ECO_VDD_PFET_STRENGTH: When read, returns the value presently being driving to the ECO VCS iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the ECO VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
47:51	RWX	IVRM_ECO_VCS_PFET_STRENGTH: When read, returns the value presently being driving to the ECO VDD iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the ECO VDD iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
52	RWX	IVRM_VDD_CORE_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the Core VDD iVRM. If ivrm_fsm_enable = 1 AND ivrm_control_mode = 1 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the Core VDD iVRM, If ivrm_fsm_enable = 0 OR ivrm_control_mode = 0, writes to this field are not performed.
53	RWX	IVRM_VCS_CORE_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the Core VCS iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the Core VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
54	RWX	IVRM_VDD_ECO_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the ECO VDD iVRM. If ivrm_fsm_enable = 1 AND ivrm_control_mode = 1 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the ECO VDD iVRM, If ivrm_fsm_enable = 0 OR ivrm_control_mode = 0, writes to this field are not performed.
55	RWX	IVRM_VCS_ECO_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the ECO VCS iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the ECO VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
56	RWX	CORE_VDD_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
57	RWX	CORE_VCS_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
58	RWX	ECO_VDD_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
59	RWX	ECO_VCS_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.

Register Name		<i>General PCBS Modes And Chicken Switches</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBSPM_MODE_REG
Address		00000000130F0156 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RW	ENABLE_PSTATE_MODE: if asserted, Pstate requests (from overrides or PMCR) will be honored, otherwise, the hardware does not do anything. Note to firmware: this is the master switch for Pstates and should be asserted after all sub-modes (that is, lvrn_fsm_en) are setup to avoid enabling unintentional modes during the mode setup.
1	RW	GLOBAL_PSTATE_CHANGE_FOR_IDLE_STATE_ENABLED: if asserted, a global Pstate change to the Nap/Sleep/Winkle-Pstate is requested, when the Nap/Sleep/Winkle state is entered and the individual enable bits in the PIMCR are asserted
2	RW	ENABLE_GLOBAL_PSTATE_REQ: if '1' then enable PMC interrupt with global Pstate change request, otherwise, disable global requests
3	RW	ENABLE_WINKLE_WITH_CPM_MODE: if '1', PCBS automatically changes the DPLL mode to mode 1, when entering winkle, but changes the mode back to CPM mode when exiting. Needed for CPM-DPLL control loop enablement.
4	RW	ENABLE_CLIPPING_OF_GLOBAL_PSTATE_REQ: if '1', PCBS automatically clips global Pstate requests with Pvf_max in PPMBR and sets the 'donate' bit in the interrupt accordingly
5	RW	CHKSW_HW214553: if deasserted, HW214553 (frequin issue in resclk mode) is fixed, if asserted, the fix is not active
6	RW	ENABLE_PMC_PMAX_SYNC_NOTIFICATION: if asserted, the PCBS-PM will send a 'Pmax_sync' interrupt, once the synchronization criterion is met
7	RW	DPLL_LOCK_REPLACEMENT_TIMER_MODE_EN: Select a timer instead of the DPLL lock bit as target frequency reached criterion. This timer has to be setup by the dial dpll_lock_timer_replacement_value. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
8	RW	DPLL_FREQOUT_MODE_EN: Looks at the DPLL frequout to find out, if the target frequency has been reached. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
9	RW	DPLL_FLOCK_MODE_EN: Looks at the real DPLL flock output to find out, if the target frequency has been reached. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
10	RW	ENABLE_SENSE_DELAY_CHARACTERIZATION: If this switch is 0, the sense latches are updated every cycle. If this switch is 1, the sense delay measurement mode is enabled, that starts a sense delay timer, whenever one of the registers that drive the inputs of the iVRMs/pFETs is written via PCB and that triggers a sense register freeze operation, when the sense delay timer reaches the value sense_delay_timer_val. With this mode, the sense delays can be measured in multiples of the PCB-slave clock speed.
11:17	RW	SENSE_DELAY_TIMER_VAL: See the description of enable_sense_delay_characterization for details.
18:19	RW	CPM_FMIN_CLIP_ERROR_SEL: This dial selects, which of the following conditions will cause the FIR bit dpll_fmin_and_not_cpmbit to be set to detect, that the DPLL runs at Fmin, but is still clipped by the CPMs. 0b00 = function is disabled 0b01 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit2 = 0 0b10 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit1 = 0 0b11 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit0 = 0
20:23	RW	DBG_TRACE_SEL: This dial selects the group of signals to be traced for debug in the lab. Details to be found in the Section 'Trace Bus'

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Bits	PCB	Field Mnemonic: Description
24:25	RW	TRACE_DATA_SEL: This dial selects the group of signals to be traced for debug in the lab. Details to be found in the Section 'Trace Bus'
26:29	RW	TP_CPLT_IVRM_VPP_TUNE: Tune bits to be set going to the iVRMs

Register Name	<i>PIVRMPS Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_PFETSTR_SENSE_REG
Address	00000000130F0157 (PCB)
Attributes	
Description	This PIVRMPS is used to check that the pFET sense outputs correspond to the driven values (mainly for test).

Bits	PCB	Field Mnemonic: Description
0:4	ROX	IVRM_CORE_VDD_PFETSTR_SNS: Not used any more.
5:9	ROX	IVRM_CORE_VCS_PFETSTR_SNS: This register is assigned to the signals tcex##_tp_ivrm_core_vcs_sense & tcex##_tp_ivrm_core_vdd_sense & tcex##_tp_ivrm_eco_vcs_sense & tcex##_tp_ivrm_eco_vdd_sense & 0b0
10:14	ROX	IVRM_ECO_VDD_PFETSTR_SNS: Not used any more.
15:19	ROX	IVRM_ECO_VCS_PFETSTR_SNS: Not used any more.
20	ROX	IVRM_VDD_CORE_PFETSTR_VALID_SNS: Not used any more.
21	ROX	IVRM_VCS_CORE_PFETSTR_VALID_SNS: Not used any more.
22	ROX	IVRM_VDD_ECO_PFETSTR_VALID_SNS: Not used any more.
23	ROX	IVRM_VCS_ECO_PFETSTR_VALID_SNS: Not used any more.
24	ROX	CORE_VDD_BYPASS_B_SENSE: Not used any more.
25	ROX	CORE_VCS_BYPASS_B_SENSE: Not used any more.
26	ROX	ECO_VDD_BYPASS_B_SENSE: Not used any more.
27	ROX	ECO_VCS_BYPASS_B_SENSE: Not used any more.
28	ROX	CORE_VDD_POWERON_SENSE: Not used any more.
29	ROX	CORE_VCS_POWERON_SENSE: Not used any more.
30	ROX	ECO_VDD_POWERON_SENSE: Not used any more.
31	ROX	ECO_VCS_POWERON_SENSE: Not used any more.
32	ROX	CORE_VDD_VPUMP_EN_SENSE: Not used any more.
33	ROX	CORE_VCS_VPUMP_EN_SENSE: Not used any more.
34	ROX	ECO_VDD_VPUMP_EN_SENSE: Not used any more.
35	ROX	ECO_VCS_VPUMP_EN_SENSE: Not used any more.
36	ROX	CORE_VDD_PFET_LOW_VOUT_SNS: Not used any more.
37	ROX	CORE_VCS_PFET_LOW_VOUT_SNS: Not used any more.
38	ROX	ECO_VDD_PFET_LOW_VOUT_SNS: Not used any more.
39	ROX	ECO_VCS_PFET_LOW_VOUT_SNS: Not used any more.



Register Name	PPMICR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_IDLE_CONT ROL_REG
Address	00000000130F0158 (PCB)
Attributes	
Description	The PPMICR is used to to read the PMICR Register typically owned (written) by the hypervisor. Writes are conditioned on the setting of the dial Pm_spr_override_en. If Pm_spr_override_en is set, firmware needs to make sure that the special wakeup state of this chiplet is reached before changing any of the latency fields in this register. Otherwise, the hardware behavior is undefined.

Bits	PCB	Field Mnemonic: Description
0:7	ROX	NAP_PSTATE_REQ: Nap Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
8	ROX	NAP_PSTATE_EN: Nap PState Enable 1 = Enable the Nap Pstate (NPS) Request, Nap Global Enable and Nap Latency functions 0 = Disables the Nap Pstate (NPS) Request, Nap Global Enable and Nap Latency functions Reads from the field return the value last written.
9	ROX	NAP_GLOBAL_EN: Nap Global Enable 1 = Upon the execution of a Nap instruction , the Nap Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a Nap instruction , the Nap Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.
10:11	ROX	NAP_LATENCY: Nap Latency not supported for POWER8 processor
12:15	ROX	RESERVED_PPMICR_0: reserved
16:23	ROX	SLEEP_PSTATE_REQ: sleep Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
24	ROX	SLEEP_PSTATE_EN: sleep PState Enable 1 = Enable the sleep Pstate (NPS) Request, sleep Global Enable and sleep Latency functions 0 = Disables the sleep Pstate (NPS) Request, sleep Global Enable and sleep Latency functions Reads from the field return the value last written.
25	ROX	SLEEP_GLOBAL_EN: sleep Global Enable 1 = Upon the execution of a sleep instruction , the sleep Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a sleep instruction , the sleep Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.

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Bits	PCB	Field Mnemonic: Description
26:27	ROX	SLEEP_LATENCY: sleep Latency 00 = Cease instructions and honors Pstate change but does not perform additional state changing actions (unsupported in POWER8, maps to 0b10) 01 = Indicates to the platform that a sub-state that would have the lowest latency is enabled (unsupported in POWER8, maps to 0b10) 10 = Indicates to the platform that a sub-state that might have a medium exit latency is enabled (POWER8: Fast Sleep) 11 = Indicates to the platform that a sub-state that might have higher exit latency is enabled (POWER8: Deep Sleep)
28:31	ROX	RESERVED_PPMICR_1: reserved
32:39	ROX	WINKLE_PSTATE_REQ: winkle Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
40	ROX	WINKLE_PSTATE_EN: winkle PState Enable 1 = Enable the winkle Pstate (NPS) Request, winkle Global Enable and winkle Latency functions 0 = Disables the winkle Pstate (NPS) Request, winkle Global Enable and winkle Latency functions Reads from the field return the value last written.
41	ROX	WINKLE_GLOBAL_EN: winkle Global Enable 1 = Upon the execution of a winkle instruction , the winkle Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a winkle instruction , the winkle Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.
42:43	ROX	WINKLE_LATENCY: winkle Latency 00 = Cease instructions and honors Pstate change but does not perform additional state changing actions (unsupported in POWER8, maps to 0b10) 01 = Indicates to the platform that a sub-state that would have the lowest latency is enabled (unsupported in POWER8, maps to 0b10) 10 = Indicates to the platform that a sub-state that might have a medium exit latency is enabled (POWER8: Fast Winkle) 11 = Indicates to the platform that a sub-state that might have higher exit latency is enabled (POWER8: Deep Winkle)
44:47	ROX	RESERVED_PPMICR_2: reserved

Register Name	PPMCR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_CONTROL_REG
Address	00000000130F0159 (PCB)
Attributes	
Description	The PPMCR provides read access to the PMCR register shadow in PCBS typically owned (written) by the hypervisor. Writes are conditioned on the setting of PMGP1[pm_spr_override_en].

Bits	PCB	Field Mnemonic: Description
0:7	RWX	GLOBAL_PSTATE_REQ: global Pstate request from hypervisor (or OCC)
8:15	RWX	LOCAL_PSTATE_REQ: local Pstate request from hypervisor or OCC
16	RWX	AUTO_OVERRIDE0_PSTATE_LIMIT_EN: automatic override Pstate 0 (for low activity detection) is enabled, if asserted



Bits	PCB	Field Mnemonic: Description
17	RWX	AUTO_OVERRIDE1_PSTATE_LIMIT_EN: automatic override Pstate 1 (reserved for future use) is enabled, if asserted
18:23	RWX	RESERVED_PPMCR: reserved
24:31	RWX	AUTO_OVERRIDE_PSTATE0: automatic override Pstate 0 (for low activity detection)
32:39	RWX	AUTO_OVERRIDE_PSTATE1: automatic override Pstate 1 (reserved for future use)

Register Name	<i>Control Register That Is Written By PMC Sequencer</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_PMC_VF_CTRL_REG
Address	00000000130F015A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PGLOBAL_ACTUAL: global actual Pstate
8:15	RW	MAXREGVCS: maximum regulation point for Vcs, Bit 0 is reserved, bits 1 to 7 are in iVID format
16:23	RW	MAXREGVDD: maximum regulation point for Vdd, Bit 0 is reserved, bits 1 to 7 are in iVID format
24:31	RW	EVIDVCS_EFF: eff. external voltage ID for Vcs in iVID format, Bit 0 is reserved
32:39	RW	EVIDVDD_EFF: eff. external voltage ID for Vdd in iVID format, Bit 0 is reserved

Register Name	<i>Undervolting Register For PCBS</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_UNDERVOLTING_REG
Address	00000000130F015B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PUV_MIN: minimum Pstate for which undervolting is allowed
8:15	RW	PUV_MAX: maximum Pstate for which undervolting is allowed
16:21	RW	KUV: this value indicates how many Pstate ticks a voltage request is undervolted (clipped with Puv_min). Note that the Kuv value is signed

Register Name	<i>PPSIBR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_INDEX_BOUND_REG
Address	00000000130F015C (PCB)
Attributes	
Description	The PPSIBR enables setting the minimum and maximum Pstate that is supported as a pointer into the local Pstate table (which has entries from 0 to 127).

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Bits	PCB	Field Mnemonic: Description
0:7	RW	LPSI_MIN: this Pstate index is the index that corresponds to array entry 0. Note that the index domain is obtained by adding 128 to a Pstate, thus, the value is unsigned.
8:14	RW	LPSI_ENTRIES_MINUS_1: this dial contains the value of the number of entries in the Pstate table minus 1

Register Name	<i>PPMBR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_BOUNDS_REG
Address	00000000130F015D (PCB)
Attributes	
Description	The PPMBR enables setting the Pstate bounds that are managed by the OCC. If dial Enable_pmc_pmax_sync_notification is set, firmware must wait after each write to this register until PMC has received the Pmax Sync Interrupt. If a write happens to this register while the previously scheduled Pmax Sync Interrupt has not yet left the PCBS, the error TBD will be set.

Bits	PCB	Field Mnemonic: Description
0:7	RW	PMIN_CLIP: minimum Pstate allowed for this chiplet
8:15	RW	PMAX_CLIP: maximum Pstate allowed for this chiplet (has to be greater or equal to Pmin_clip)

Register Name	<i>PPTCR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_CTRL_REG
Address	00000000130F015E (PCB)
Attributes	
Description	The PPTCR controls the address for writing the local Pstate Table Array (all 96 words are accessible). Note that the protocol requires this register to be set up with the Pstate address first, if a read or a write of the Pstate array is intended, to make sure that the initial address is set correctly. The register PPTR must always be written or read afterward. Note that any access to the PPTR auto-increments this register.

Bits	PCB	Field Mnemonic: Description
0:6	RWX	PSTATE_TABLE_ADDRESS: This is the address of the Pstate table in PCBS, which is auto-incremented after any access to the PTLR.

Register Name	<i>PPTR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_REG
Address	00000000130F015F (PCB)
Attributes	
Description	The PPTR controls the data to be written into the Pstate table and returns the data for a read of the Pstate table. Note that the protocol requires for a write to set this register up after first setting up PPTCR (if the user does not rely on the auto-increment function of the address). For a read of the Pstate table, this register must be read after first setting up PPTCR as well (again if the auto-increment feature of the address is not used). Any access to this register auto-increments the Pstate_table_address by 1. Note also that the read functionality of this register is only functional if PIVRMCSR[ivrm_fsm_enable] = 0. The write functionality works in any case.



Bits	PCB	Field Mnemonic: Description
0:63	RW	pstate_data This is the field for data bits 0 to 63

Register Name	PPSTR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_STEP_TARGET_REG
Address	00000000130F0160 (PCB)
Attributes	
Description	The PPSTR provides read access to several intermediate values in the Pstate computation pipeline. Writes Are conditioned on the setting of PMGPO[enable_OCC_ctrl_for_local_Pstate_eff_req].

Bits	PCB	Field Mnemonic: Description
0:7	RWX	LOCAL_PSTATE_EFF_REQ: this field represents the effective local Pstate request right before the clipping with Pmin and Pmax if enable_OCC_ctrl_for_local_Pstate_eff_req=0 then the hardware controls this dial, that updates every cycle if enable_OCC_ctrl_for_local_Pstate_eff_req=1 then OCC is in control and can write this field to control the effective local Pstate request that will eventually propagate through the downstream logic and determine the Local PState Actual. Note: if no write to this register is performed, the currently established value is maintained stable forever.
8:15	ROX	LOCAL_PSTATE_TARGET: This field is the target Pstate of a complete Pstate change that is performed in smaller steps
16:23	ROX	LOCAL_CORE_PSTATE_STEP_TARGET: this field represents the intermediate value that is about to be established as the next Local Pstate Actual after completing one step in the process of the transition towards the 'local_Pstate_target' the new voltage, frequency, and clock resonance setting
24:31	ROX	LOCAL_ECO_PSTATE_STEP_TARGET: this field represents the intermediate value that is about to be established as the next Local Pstate Actual after completing one step in the process of the transition towards the 'local_Pstate_target' the new voltage, frequency, and clock resonance setting

Register Name	Read-Only Status Register For DPLL And For Debugging (PDSR)
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_DPLL_STATUS_REG
Address	00000000130F0161 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:14	ROX	DPLL_FF_FREQOUT: frequout output from DPLL (current frequency - bits 2 to 10 correspond to the same scale as the 9 bits of frequin (which need to be multiplied with our frequency step to get the real frequency), the remaining bits just provide a higher accuracy)
15	ROX	DPLL_FREQU_CHANGE: DPLL Frequency change (pin of DPLL without filter)
16	ROX	DPLL_STATUS_SPARE_BIT1: Spare bit.
17	ROX	PMAX_SYNC_PENDING: gets asserted, if the logic has a Pmax sync interrupt outstanding that will be eventually sent to PMC when the Pmax sync criterion is met
18	ROX	GA_ACK_PENDING: gets asserted, if the logic has a global actual Pstate update acknowledgment interrupt outstanding that will be eventually sent to PMC when the GA ack criterion is met
19:26	ROX	CAPPED_GLOBAL_PSTATE_REQ: corresponds to the capped global Pstate request that is presented as Pstate interrupt and send to PMC

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Bits	PCB	Field Mnemonic: Description
27	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT2: DPLL runs at Fmax and CPM bit 2 is set. Note that this bit and the following 2 bits indicate, that the CPMs would allow the DPLL to run faster than Fmax.
28	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT3: DPLL runs at Fmax and CPM bit 3 is set
29	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT4: DPLL runs at Fmax and CPM bit 4 is set
30	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT2: DPLL runs at Fmin and CPM bit2 is zero. Note that this bit and the following 2 bits indicate, that the CPMs indicate, that the DPLL should run slower than the currently established Fmin.
31	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT1: DPLL runs at Fmin and CPM bit1 is zero
32	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT0: DPLL runs at Fmin and CPM bit0 is zero
33	ROX_CLRPAR T	DPLL_FASTER_THAN_FMAX_PLUS_DELTA1: The DPLL indicated that it ran once faster than Fmax+dppl_char_delta1
34	ROX_CLRPAR T	DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2: The DPLL indicated that it ran once slower than Fmin-dppl_char_delta2
35:48	ROX	DPLL_MAX_FREQOUT_AFTER_LAST_READ: This dial indicates the maximum DPLL frequout value after the last read of this register (only 14 MSBs)
49:62	ROX	DPLL_MIN_FREQOUT_AFTER_LAST_READ: This dial indicates the minimum DPLL frequout value after the last read of this register (only 14 MSBs)

Register Name	<i>The PIVRMVCR0 Controls The Voltage Stepping Delays</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG0
Address	00000000130F0162 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	IVRM_REQ_PSTATE_STEPDELAY_RISING: Requested Internal Pstate Baby Step Delay - Rising Step. Delay before allowing the next step for a rising Pstate Transition. This dial and ivrm_req_Pstate_stepdelay_lowering allow for differing delays for the two directional transitions if necessary. In 100ns units as established by scan dial ivrm_100ns_value
8:15	RW	IVRM_REQ_PSTATE_STEPDELAY_LOWERING: Requested Internal Pstate Baby Step Delay - Lowering Step. Delay before allowing the next step for a lower Pstate Transition. This dial and ivrm_req_Pstate_stepdelay_rising allow for differing delays for the two directional transitions if necessary. In 100ns units as established by scan dial ivrm_100ns_value

Register Name	<i>The PIVRMVCR1 Controls The Voltage Stepping Delays</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG1
Address	00000000130F0163 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	IVRM_STABILIZE_DELAY_RUN: Stabilization Delay - Run Time Delay to allow a rail to stabilize upon a baby step while the region is operational. In 100ns units as established by scan dial ivrm_100ns_value
8:15	RW	IVRM_STABILIZE_DELAY_IDLE: Stabilization Delay - Idle Transition Delay to allow a rail to stabilize upon a baby step during an idle transition where the activity in the region is quiesced. In 100ns units as established by scan dial ivrm_100ns_value
16:23	RW	IVRM_PFSTR_PROP_DELAY: PFET Strength Propagation Delay Time from PFET Strength values being launched till PFET Strength Valid is asserted. In order to ensure like rails across domains (Core VDD<>ECO VDD, Core VCS<>ECO VCS) are in sync during operational mode, this time value applies to all rails across the domains. This parameter allows for PFET Strength values to settle before PFET Strength Valid is sampled in the Uregs. The value set must the maximum delay for the worst rail timing and must allow for any metastability settling (for example, normally 2-3 cycles for single signals in an asynch handshake interface)
24:31	RW	IVRM_PFSTRVALID_PROP_DELAY: PFETStrength Valid Propagation Delay Time from ivrm_pfstr_prop_delay expiring to where PFET Strength Valid is deasserted. The value is the maximum of a) the minimum pulse width required for PFETStrength Valid and b) the propagation of PFETStrength Valid through (or enough of) the daisy chain. In order to ensure like rails across domains (Core VDD<>ECO VDD, Core VCS<>ECO VCS) are in sync during operational mode, this time value applies to all rails across the domains and thus must be the set to the value of the worst (slowest) rail. The minimum pulse width cannot be violated. The propagation delay can be tuned for more aggressive timing (for example, deassert before the actual propagation is complete). Measured in prv_nclk cycles. The min delay is 2 cycles. Additional delay can be configured with the following settings 0x00 = No additional delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks
32:39	RW	IVRM_VPUMP_POWERON_TIME: iVRM (VRreg and UReg) - Vpump Power On Time Time necessary for the distributed internal VRM macro circuits to power on. Same delay is required for power on voltage pump circuit. Both delays are in the 8us range. In 100ns units as established by scan dial ivrm_100ns_value
40:47	RW	IVRM_BYPASS_DELAY: iVRM Bypass Propagation Delay Delay time for bypass_b signal propagation. Measured in prv_nclk cycles Target: 50ns 0x00 = No delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks
48:55	RW	PFET_VPUMP_ENABLE_DELAY: PFET and Vpump Enable Propagation Delay Delay time for PFET enable and vpump enable signal propagation. Target: 130ns Measured in prv_nclk cycles 0x00 = No delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks
56:62	RW	IVRM_VID_VOUT_THRESHOLD: VID threshold If the output voltage (Vout) is targeting a value below this threshold the slow PFET can backed off from its normal drive strength so as to reduce the ripple at these lower voltage conditions

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Register Name	POHR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_OCC_HEARTBEAT_REG
Address	00000000130F0164 (PCB)
Attributes	
Description	Controls the behavior of the OCC heartbeat function.

Bits	PCB	Field Mnemonic: Description
0:7	RW	occ_heartbeat_time 'OCC Heartbeat Time Value' " 'This field defines the number of ~64us hang timer pulses in which a a PCB read or write of the heartbeat trigger register (of which the offset is specified by dial occ_heartbeat_reg_addr_offset) is not detected that will constitute the loss of the OCC heartbeat. If occ_heartbeat_en is set and upon this loss detection, POHBR[psafe] is forced and, if enabled, the error TBD is activated ' " '0x00 - unsupported, causes undefined behavior' '0x01 - 64us +0/-1us' '0x02 - 128us +0/-1us' '...' '0xFF - 16320us +0/-1us 16.3ms' " 'Upon the 64us hang pulse, the decremter ticks. if the decremter reaches x00, the heartbeat loss event is triggered.' " ' '
8	RW	occ_heartbeat_enable 'OCC Heartbeat Timer Enable' " '0 = Disable the OCC Heartbeat function. Lack of accesses to the register defined by the dial occ_heartbeat_reg_addr_offset does not result in heartbeat loss events to be triggered (no FIRs set nor Safe mode entry).' " '1 = Enable the OCC Heartbeat function. '
9:16	RW	occ_heartbeat_reg_addr_offset This dial allows to configure the address offset within the PCBS power management entity of the register, that will regularly reset the heartbeat timer (which is called heartbeat trigger register). The address offset is 0x100 plus the value of this dial.
17:24	RW	Psafe 'Pstate Safe' " 'This field establishes the Pstate that the core chiplet will take on if: 'psafe <= PMSR[global_actual_pstate] 'AND any of the following conditions are true:' 'Loss of OCC Heartbeat if occ_heartbeat_en is set' 'PMGPO[force_safe_mode] is set' " 'If psafe > PMSR[global_actual_pstate], the global_actual_pstate is forced.' " 'The value of Psafe needs to be at or below the nominal Pstate to make sure safe operation of all chiplets. '

Register Name	PRCCR0 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG0
Address	00000000130F0165 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function.

Bits	PCB	Field Mnemonic: Description
0	ROX	RESCLK_DIS: Resonant Clock Enable Master enable of all resonant clocking functions. This dial can be set by setting GP3(22) and can not be set in this PCBS_resonant_Clock_Control_Reg0. 1 = Resonant Clock function is disabled. Default values (0) for resclk_value, resclk_core_sync_value, csb_eco_sync_value 0 = Resonant Clock Control hardware is enabled (the mode is defined by dial resclk_control_mode)

Bits	PCB	Field Mnemonic: Description
1	RW	RESCLK_CONTROL_MODE : Resonant Clock Control Mode Defines the control means enabled when resclk_dis is not set. 0 = Pstate band hardware mechanism enabled 1 = Manual mode enabled (Firmware mode) If this bit is set to 0, the hardware control mechanism that manages the transition across the Resonant Bands is enabled. If this bit is set to 1, the automatic Pstate band hardware mechanism is disabled and the Firmware is in control of all values of the dial resclk_value, resclk_core_sync_value, csb_eco_sync_value. Firmware must ensure that frequency changes will not cross resonant bands or machine failures may result. resclk_value represents the values for clock sector buffer strength, inductor switch strength and high inductor enable. Firmware must ensure the correct stepping in/out the different bands and propagation of the values (resclk_value) to the core/eco (resclk_core_sync_value / csb_eco_sync_value).
2:4	RW	RESCLK_SYNC_PW : Resonant Clock Sync Pulse Width Number of nest/4 cycles to assert the clock sync signal. This value must be high enough to ensure capture and propagation across the asynchronous chiplet boundary.
5:11	RW	RES_SYNC_DELAY_CNT : Resonant Clock Sync Delay Number of nest/4 cycles wait after the launch of the resclk_value (csb and inductor) before launching the sync to allow these to be captured. This value must be high enough to ensure full propagation to the input of the clock sector buffers and inductor switches.
12:26	RW	RES_CSB_STR_INSTR_LO : Resonant Clock Sector Buffer Strength Instruction - Low Band Mask value that determines whether, during a fixed 15 step sequence, the res_csb_str(0:3) is to be decremented/incremented in entering/exiting the Low Band. During resonant clock Entry, res_csb_str(0:3) decremented by the value pattern from 0 down to 14. During resonant clock Exit, res_csb_str(0:3) incremented by the value pattern from 14 up to 0.
27:41	RW	RES_CSB_STR_INSTR_HI : Resonant Clock Sector Buffer Strength Instruction - High Band Mask value that determines whether, during a fixed 15 step sequence, the res_csb_str(0:3) is to be decremented/incremented in entering/exiting the High Band. During resonant clock Entry, res_csb_str(0:3) decremented by the value pattern from 0 down to 14. During resonant clock Exit, res_csb_str(0:3) incremented by the value pattern from 14 up to 0.

Register Name	PRCCR1 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG 1
Address	00000000130F0166 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function. Writes are conditioned.

Bits	PCB	Field Mnemonic: Description
0:7	RW	FULL_CSB_PS : Full Clock Sector Buffer Pstate Pstate defining the maximum point where the clock sector buffer must be driven to full strength. This allow clocks to be distributed at low Vmin levels. FW needs to make sure that no overlaps occur with bands 2 or 3.
8:15	RW	RES_LOW_LOWER_PS : Low Frequency Resonant Lower (LFRLow) Pstate Pstate defining the lower frequency of the Low Resonant Frequency Band. FW needs to make sure that no overlap occurs with band 0.
16:23	RW	RES_LOW_UPPER_PS : Low Frequency Resonant Upper (LFRUpper) Pstate Pstate defining the upper frequency of the Low Resonant Frequency Band. Note that if an overlap occurs with band 3, the hardware behavior is undefined.
24:31	RW	RES_HIGH_LOWER_PS : High Frequency Resonant Lower (HFRLow) Pstate Pstate defining the lower frequency of the High Resonant Frequency Band. Note that if an overlap occurs with band 2, the hardware behavior is undefined.

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Bits	PCB	Field Mnemonic: Description
32:39	RW	RES_HIGH_UPPER_PS: High Frequency Resonant Upper (LFRUpper) Pstate Pstate defining the upper frequency of the High Resonant Frequency Band. This value needs to be greater or equal to high_res_lower_ps.
40:43	RW	NONRES_CSB_VALUE_TI: Clock Sector Buffer Table Index for non-resonant state Table Index into Clock Sector Buffer Table for the nominal, non-resonant state.
44:47	RW	FULL_CSB_VALUE_TI: Clock Sector Buffer Table Index for full CSB value Table Index into Clock Sector Buffer Table for the full CSB strength value.
48:56	RWX	RESCLK_VALUE: Output register driving the 9 bit resclk_value In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current resclk_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. The value in this register represents the following concatenation: csb_str_value(0:3) sw_str(0:3) hi_induct_en.
57	RWX	RESCLK_CORE_SYNC_VALUE: Output register driving the resclk_core_sync signal In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current resclk_core_sync_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. This bit is supposed to be used in order to create a SCOM-controlled pulse to force an update of the resclk propagation registers. A 1 enables the synchronous update, a 0 disables it. Suggested use of this bit is to set it to 1 and then set it back to 0 to create a (long) update pulse.
58	RWX	CSB_ECO_SYNC_VALUE: Output register driving the csb_eco_sync signal In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current csb_eco_sync_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. This bit is supposed to be used in order enable the ECO domain to participate in clock sector buffer strength changes, when switching from nominal strength to full CSB strength. A 1 enables the ECO domain, a 0 disables it from seeing a CSB strength update.

Register Name	PRCCR1 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_STATUS_REG
Address	00000000130F0167 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function.

Bits	PCB	Field Mnemonic: Description
0	ROX	RESCLK_STATE: Resonant Clock State 0 = Resonant Clocking inactive 1 = Resonant Clocking active Valid if resclk_inprogress = 0. Hardware sets this bit to the right value at the completion of the transition into and out of resonance mode.

Bits	PCB	Field Mnemonic: Description
1	ROX	RES_HI_INDUCT_EN: Resonant High Inductor Enable Valid if resclk_inprogress = 0. This dial provides the current value being propagated. 0 = Resonant Clock mode not active 1 = Resonant Clock mode active
2	ROX	RESCLK_INPROGRESS: Resonant Clock Transition in Progress This bit is set by hardware while a transition is in progress and will be reset by hardware when the operation is complete.
3	ROX	RESCLK_FULL_CSB: Full CSB Clock State 0 = Full CSB Clocking inactive 1 = Full CSB Clocking active Valid if resclk_inprogress = 0. Hardware sets this bit to the right value at the completion of the transition into and out of full CSB mode respectively.

Register Name	<i>PLPFTCR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_CONTROL_REG
Address	00000000130F0168 (PCB)
Attributes	
Description	The PLPFTCR enables firmware to configure the modes that are used for the PCBS Local Pstate Frequency Target Status Register.

Bits	PCB	Field Mnemonic: Description
0:2	RW	DELAY_TIME: This field encodes the delay between the time a Local Actual Pstate change modifies the input to the DPLL and the time frequency acquisition begins to allow the hardware to ignore the frequency transition of the DPLL in order to get better frequency measurements. This field encodes a delay of ~1us to ~128us in power of 2 selects. The delay is defined by $2^{**}delay\_time$ in us. Note that the hardware uses multiples of the slow hang pulse that is running at 1us.
3	RW	RECORD_TRANSITIONS: This bit indicates whether the LPFTSR records events that correspond to Local Actual Pstate changes (and therefore may include DPLL slewing effects.) One usage model would set the periodic sample_time defined by the dial OHA_MODE_REG[tod_pulse_count_match_val] to a time less than the worst-case DPLL slew time but then ignore Pstate transitions because they might include DPLL slew effects.
4:18	RW	MULTIPLIER: This 15-bit unsigned constant is multiplied by the DPLL frequency code (9 bits) implied by the Local Actual Pstate to yield the 24-bit frequency target measured in PCBS-PM clock cycles (core clock / 2). Assuming times in seconds and frequencies in Hz, firmware should set this constant to: $(DPLL\_Frequency\_Code\_Step\_Hz * Sample\_Time\_Seconds) / 2$
19	RW	ENABLE_LPFT_FUNCTION: This is the enable bit to enable the local Pstate frequency target function. A '1' enables the function, a '0' disables it (the value can be changed at any time).

Register Name	<i>PLPFTSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_STATUS_REG
Address	00000000130F0169 (PCB)
Attributes	
Description	The PLPFTSR allows firmware to observe local actual Pstate realized frequencies.

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Bits	PCB	Field Mnemonic: Description
0	ROX_CLRPART	VALID: If this bit is set then all of the remaining fields of this register are valid. This bit is cleared whenever the register is read or after a local actual Pstate change occurs, and is will be set whenever the hardware completes a valid sample. If firmware reads this register and the valid bit is not set, then it indicates that the Local Pstate target frequency acquisition logic has not been able to complete a frequency acquisition for any Local Actual Pstate change since the last time the LPFTSR was read. This could be due to either of the following factors: 1. Firmware is sampling the LPFTSR faster than the time implied by the sample time defined in OHA by the dial OHA_MODE_REG[tod_pulse_count_match_val] field
1	ROX	CPM_DPLL: If the valid bit is set, then if cpm_dpll is set it indicates that the event recorded by this register was due to a Local Actual Pstate implemented by the DPLL running in CPM-DPLL mode, otherwise the value of this bit is undefined. If the valid bit is not set, this bit is undefined.
2	ROX	IVRM: If the valid bit is set, then if ivrm is set it indicates that the event recorded by this register was due to a Local Actual Pstate whose voltage was set locally by the iVRM operating entirely in regulation mode. If the valid bit is not set, this bit is undefined.
3	ROX	TRANSITION: If the valid bit is set, then if transition is set it indicates that during the observation period a Local Pstate Actual change has occurred, and any performance delta may be due to DPLL frequency slewing. If the valid bit is not set, this bit is undefined
4	ROX	STABLE: If stable is set it indicates that the DPLL input frequency has been stable since the last time the PLPFTSR was read. This bit is set whenever the PLPFTSR is read, and cleared whenever the Fmax input of the DPLL changes. This bit is always valid, regardless of the state of the valid bit. If the PLPFTSR is read on the same cycle a frequency changes then the stable bit is cleared. This bit helps firmware better understand how to interpret the information contained in the PLPFTSR. (Note that this bit should have an attribute ROX_SETPART, but this is not supported by regchk.)
5:28	ROX	DELTA: If the valid bit is set then this is the 24-bit signed difference Measured Cycles - Target Cycles for the event captured by this register. If the valid bit is not set, this dial is undefined.
29:52	ROX	CUMULATIVE: This field records the 24-bit cumulative (signed) delta for all valid samples taken since this field was cleared. Writing any value to this register clears this field. Note that it should have an attribute WOX_CLRPART, but this is not supported by regchk/figtree.
53:60	ROX	PSTATE: If the valid bit is set then this is the Local Actual Pstate of the frequency acquisition that had the minimum (signed) delta of any valid sample taken since the last time the LPFTSR was read. If the valid bit is not set, then this field is undefined.

Register Name	PFSMM1/2 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR1_REG
Address	00000000130F0170 (PCB)
Attributes	
Description	The PFSMM1/2 facilitates debug by providing insight into the internal FSM states of the PCB-slave power-management unit. For expert use only. Coding according to VHDL design.

Bits	PCB	Field Mnemonic: Description
0:6	ROX	BABYSTEP_MAIN_FSM: Main Babystep FSM (mfsm_lt)
7:11	ROX	BABYSTEP_SLAVE_FSM: Babystep Slave FSM (sfsm_lt)
12:16	ROX	CORE_RAILSTEPPER_MAIN_FSM: Main Core Railstepper FSM (mrsfsm_lt)
17:21	ROX	ECO_RAILSTEPPER_MAIN_FSM: Main ECO Railstepper FSM (mrsfsm_lt)



Bits	PCB	Field Mnemonic: Description
22:25	ROX	CORE_RAILSTEPPER_SUB_FSM: Core Railstepper Sub-FSM (srsfsm_lt)
26:29	ROX	ECO_RAILSTEPPER_SUB_FSM: ECO Railstepper Sub-FSM (srsfsm_lt)
30:34	ROX	CORE_RAILSTEPPER_BYP_FSM: Core Railstepper Bypass FSM (byp_fsm_lt)
35:39	ROX	ECO_RAILSTEPPER_BYP_FSM: ECO Railstepper Bypass FSM (byp_fsm_lt)
40:45	ROX	IVRM_CORE_VDD_SEQUENCER_FSM: Core iVRM Sequencer for Vdd (ivrm_fsm_lt)
46:51	ROX	IVRM_CORE_VCS_SEQUENCER_FSM: Core iVRM Sequencer for Vcs (ivrm_fsm_lt)
52:57	ROX	IVRM_ECO_VDD_SEQUENCER_FSM: ECO iVRM Sequencer for Vdd (ivrm_fsm_lt)
58:63	ROX	IVRM_ECO_VCS_SEQUENCER_FSM: ECO iVRM Sequencer for Vcs (ivrm_fsm_lt)

Register Name	<i>Refer To The Description Of PFSMM1.</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR2_REG
Address	00000000130F0171 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:6	ROX	RESCLK_BAND_FSM: Band Sequencer for resonant clocking (band_fsm_lt)
7:10	ROX	RESCLK_LOWRES_FSM: Low Resonant Clocking sequencer (lowres_fsm_lt)
11:14	ROX	RESCLK_HIGHRES_FSM: High Resonant Clocking sequencer (highres_fsm_lt)
15:18	ROX	RESCLK_FULLCSB_FSM: Full-CSB Resonant Clocking sequencer (fullcsb_fsm_lt)
19:22	ROX	RESCLK_UPDATE_FSM: Resonant Clocking Update sequencer (update_fsm_lt)
23:29	ROX	IDLE_TRANSITION_FSM: Idle State Sequence FSM (ifsm_lt)
30:37	ROX	Peco_step_target_uv Current ECO Step Target Pstate (different from Plocal_actual for undervolting)
38:45	ROX	Pcore_step_target_uv Current core Step Target Pstate (different from Plocal_actual for sleep and undervolting)

Register Name	<i>Protect Mode Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.PROTECT_MODE_REG
Address	00000000130F03FE (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	READ_PROTECT_ENABLE: Enable read protection
1	RW	WRITE_PROTECT_ENABLE: Enable write protection

Register Name	<i>Atomic Lock Register</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX03.TP_PCB_SLAVE_INST.ATOMIC_LOCK_REG	
Address	00000000130F03FF (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	RW	ATOMIC_LOCK_ENABLE: Enable atomic lock
1:4	ROX	ATOMIC_ID: Atomic ID

Register Name	<i>Contains The Slave's Primary Address</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.PRIMARY_ADDRESS_REG	
Address	00000000140F0000 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RO	Reserved field (Access type is primary_address)

Register Name	<i>Multicast Group 1</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.MULTICAST_GROUP_1	
Address	00000000140F0001 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST1_GROUP: multicast group1 setting

Register Name	<i>Multicast Group 2</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.MULTICAST_GROUP_2	
Address	00000000140F0002 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST2_GROUP: multicast group2 setting



Register Name	Multicast Group 3	
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.MULTICAST_GROUP_3	
Address	00000000140F0003 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST3_GROUP: multicast group3 setting

Register Name	Multicast Group 4	
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.MULTICAST_GROUP_4	
Address	00000000140F0004 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST4_GROUP: multicast group4 setting

Register Name	Timeout Select Register	
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.TIMEOUT_REG	
Address	00000000140F0010 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:1	RW	Reserved field (Access type is int_timeout)

Register Name	Assist Interrupt Register	
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.ASSIST_INTERRUPT_REG	
Address	00000000140F0011 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is attn)
1	ROX	Reserved field (Access type is recov)
2	ROX	Reserved field (Access type is xstop)

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Register Name	GP3 Register (NA In PERV CPLT)
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.GP3_REG
Address	00000000140F0012 (PCB) 00000000140F0013 (PCB1) 00000000140F0014 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset
2	RWX	RWX_WAND	RWX_WOR	GLSMUX_RESET: Glsmux reset for test purpose and stuck active mesh protection. Notice no clocks in the EX if this bit is set.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Put the DPLL in test mode.
4	RWX	RWX_WAND	RWX_WOR	PLL_RST: Put PLL in reset state.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYP: Enable PLL bypass.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pcb_access)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	PM_PI_DECODE: Test override for power management. EX chiplet only.
22	RWX	RWX_WAND	RWX_WOR	RESCLK_DIS: Resonant clocking disable.
23:25	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave will report 'Chiplet Offline'.
27	RWX	RWX_WAND	RWX_WOR	TP_LVLTRANS_FENCE: Electrical winkel fence. Mainly used by power management.
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.
29:31	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)



Register Name	<i>Skew Adjust Data</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.CLK_ADJ_REG	
Address	00000000140F0015 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:15	ROX	

Register Name	<i>Clk Ajust Config</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.CLK_ADJ_SET	
Address	00000000140F0016 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:31	RW	CLK_ADJ_SET_REG: Clk adj config

Register Name	<i>Vital Scan Out</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.VITAL_SCAN_OUT	
Address	00000000140F0017 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	

Register Name	<i>Chiplet Heartbeat Register</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.HEARTBEAT_REG	
Address	00000000140F0018 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	HEARTBEAT_DEAD: Chiplet heartbeat not detected

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Register Name	<i>Lock Indications From PLLs</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.PLL_LOCK_REG
Address	00000000140F0019 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	ROX	Reserved field (Access type is lock)

Register Name	<i>Attn Interrupt</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.ATTN_INTERRUPT_REG
Address	00000000140F001A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is attn)

Register Name	<i>Recov Interrupt</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.RECOV_INTERRUPT_REG
Address	00000000140F001B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is recov)

Register Name	<i>Xstop Interrupt</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.XSTOP_INTERRUPT_REG
Address	00000000140F001C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is xstop)



Register Name	<i>Slave Config Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.SLAVE_CONFIG_REG
Address	00000000140F001E (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	CFG_DISABLE_PERV_THOLD_CHECK: Disable pervasive thold check
1	RW	CFG_DISABLE_MALF_PULSE_GEN: Disable pulse generation for malf alert. Switch back to level
2	RW	CFG_STOP_HANG_CNT_SYS_XSTP: Disable hang counter stop for system xstop
3	RW	CFG_DISABLE_CL_ATOMIC_LOCK: Disable atomic lock for chiplet accesses
4	RW	CFG_DISABLE_HEARTBEAT: Disable check for voltage and gridclock in the chiplet
5	RW	CFG_ZERO_DATA: Sent zero data on any error
6:7	RW	
8:12	RW	ERROR_MASK: mask bits for slave error reporting
13:15	RW	

Register Name	<i>Error Capture Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.ERROR_REG
Address	00000000140F001F (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX_WCLEA R	CE_ERROR: Correctable error on pcb bus
1:3	RWX_WCLEA R	CHIPLET_ERRORS: Errors reported by chiplet 000 = no error 001 = XSCOM command blocked due pending errors 010 chiplet offline 011 partial good 100 invalid address / address error / bad access type 101 clock error 110 parity error / received unexpected packet / wrong packet number 111 timeout This register is for debug purposes only. It only holds meaningful data if it is cleared after each error.
4	RWX_WCLEA R	PARITY_ERROR: Parity error on PCB Interface
5	RWX_WCLEA R	DATA_BUFFER_ERROR: Parity error in data buffer
6	RWX_WCLEA R	ADDR_BUFFER_ERROR: Parity error in address buffer
7	RWX_WCLEA R	PCB_FSM_ERROR: Invalid state error in PCB FSM
8	RWX_WCLEA R	CL_FSM_ERROR: Invalid state error in Chiplet FSM
9	RWX_WCLEA R	INT_RX_FSM_ERROR: Invalid state error in interrupt RX FSM
10	RWX_WCLEA R	INT_TX_FSM_ERROR: Invalid state error in interrupt TX FSM

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Bits	PCB	Field Mnemonic: Description
11	RWX_WCLEAR	INT_TYPE_ERROR: Invalid interrupt type
12	RWX_WCLEAR	CL_DATA_ERROR: Parity error on Chiplet Interface
13	RWX_WCLEAR	INFO_ERROR: Parity error on Chiplet info lines
14	RWX_WCLEAR	UNUSED_0:
15	RWX_WCLEAR	CHIPLET_ATOMIC_LOCK_ERROR: Chiplet atomic lock error
16	RWX_WCLEAR	PCB_INTERFACE_ERROR: Error of pcb interface component for the internal endpoint
17	RWX_WCLEAR	CHIPLET_OFFLINE: Heartbeat check indicated that chiplet is offline
18	RWX_WCLEAR	CHIPLET_GRID_SKITTER: Heartbeat check indicated skitter on the chiplet grid
19	RWX_WCLEAR	GP3_REG_PARITY_ERROR: gp3 register parity bad
20	RWX_WCLEAR	ADDRESS_REG_PARITY_ERROR: address register parity bad
21	RWX_WCLEAR	TIMEOUT_REG_PARITY_ERROR: timeout select register parity bad
22	RWX_WCLEAR	CONFIG_REG_PARITY_ERROR: slave config register parity bad
23	RWX_WCLEAR	CLK_ADJ_REG_PARITY_ERROR: clk adj register parity bad
24	RWX_WCLEAR	DIV_REG_PARITY_ERROR: div register parity bad
25:28	RWX_WCLEAR	PLL_UNLOCK_ERROR: unlock from chiplet pll

Register Name		Hang Pulse Generation Register 0.
Mnemonic		EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.HANG_PULSE_0_REG
Address		00000000140F0020 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_0: Value of hang pulse 0. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_0: If set to '1', hang pulses are suppressed in case of a xstop



Register Name	Hang Pulse Generation Register 1.	
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.HANG_PULSE_1_REG	
Address	00000000140F0021 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_1: Value of hang pulse 1. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_1: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	Hang Pulse Generation Register 2.	
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.HANG_PULSE_2_REG	
Address	00000000140F0022 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_2: Value of hang pulse 2. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_2: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	Hang Pulse Generation Register 3.	
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.HANG_PULSE_3_REG	
Address	00000000140F0023 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_3: Value of hang pulse 3. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_3: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	Hang Pulse Generation Register 4.	
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.HANG_PULSE_4_REG	
Address	00000000140F0024 (PCB)	
Attributes		
Description		

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Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_4: Value of hang pulse 4. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_4: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 5</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.HANG_PULSE_5_REG
Address	00000000140F0025 (PCB)
Attributes	
Description	This hang counter is used exclusively to generate the malfunction alert pulse.

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_5: Value of hang pulse 5. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_5: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 6</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.HANG_PULSE_6_REG
Address	00000000140F0026 (PCB)
Attributes	
Description	This hang counter is exclusively used for heartbeat generation.

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_6: Value of hang pulse 6. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_6: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Divider For Hang Counter Clock</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.PRE_COUNTER_REG
Address	00000000140F0028 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PRE_COUNTER: Divider for hang counter clock. Divides clock by n+1 (default: n=0)



Register Name		PowerManagement GP0		
Mnemonic		EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PMGPO_REG		
Address		00000000140F0100 (PCB) 00000000140F0101 (PCB1) 00000000140F0102 (PCB2)		
Attributes				
Description				
Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PM_DISABLE: Master Switch for the PowerManagement Macro
1	RWX	WOX_AND	WOX_OR	PMGP0_SPARE_BIT1: spare bit
2	RWX	WOX_AND	WOX_OR	TP_TC_RESTART_CORE_DOMAIN: Kicks off small sequencer in OHA to get chiplet clocks back running for fast sleep without involving PORE. From GP-reg and overridden by PowMan State Machine.
3	RWX	WOX_AND	WOX_OR	DPLL_THOLD: Thold for the DPLL clock domain in the chiplet
4	RWX	WOX_AND	WOX_OR	PERV_THOLD: Thold for the Pervasive clock domain in the chiplet
5	RO	RO	RO	Reserved.
6	RO	RO	RO	Reserved.
7	RWX	WOX_AND	WOX_OR	PM_DPLL_TIMER_ENA: Select a timer instead of the DPLL lock bit for criteria to switch to DPLL. The time is defined by thold_timer_sel.
8	RWX	WOX_AND	WOX_OR	DPLL_LOCK_SENSE: DPLL lock sensitivity control (0=faster lock time, 1=slower lock time)
9	RWX	WOX_AND	WOX_OR	PMGP0_SPARE2: spare bit
10	RWX	WOX_AND	WOX_OR	DPLL_RESET: Reset to DPLL
11	RWX	WOX_AND	WOX_OR	PMGP0_SPARE_BIT11: Spare bit
12:19	RWX	WOX_AND	WOX_OR	DPLL_TESTOUT_CTL: DPLL testout control
20	RWX	WOX_AND	WOX_OR	TP_TC_CACHE2CORE_FENCE: Fence from cache to core domain in EX chiplet
21	RWX	WOX_AND	WOX_OR	TP_TC_CORE2CACHE_FENCE: Fence from core to cache domain in EX chiplet
22	RWX	WOX_AND	WOX_OR	TP_TC_PERVASIVE_ECO_FENCE: Pervasive ECO fence
23	RWX	WOX_AND	WOX_OR	CHKSW_HW257424_DISABLE: Chicken switch for interrupt retry exhausted bug (0=fix enabled, 1=fix disabled)
24:26	RWX	WOX_AND	WOX_OR	TP_CLK_ASYNC_RESET_DC: Clk async reset for three glitchless muxes, and the two clock dividers (bit 0 = master GLM, bit 1 = ECO Div2 and ECO GLM, bit 2= core Div1 and core GLM)
27:29	RWX	WOX_AND	WOX_OR	TP_CLKGLM_SEL_DC: Glitchless Mux Select for primary chiplet clock source (feeding both core and eco clock muxes) 000 = refclk, 001 = DPLL. 100 = Use constant selected by bit 34, else refclk
30	RWX	WOX_AND	WOX_OR	TP_CLKGLM_ECO_SEL_DC: Glitchless Mux Select for eco domain (cache_nclk) grid. 0= follow primary source chosen by previous field: 1 = Use constant selected by bit 34
31	ROX	NC	NC	SPECIAL_WKUP_DONE: Indicates that special wakeup is done, if asserted
32:33	RWX	WOX_AND	WOX_OR	TP_CLKGLM_CORE_SEL_DC: Glitchless Mux Select for core domain (nclk grid) mux. 0b00=primary GLS mux output, 0b10=constant input, 0b01=refclk. Valid transitions are 0b01 <-> 0b00 <-> 0b10, 0b11 is illegal

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
34	RWX	WOX_AND	WOX_OR	TP_CLKGLM_CONST_DC: Constant input available to all three ClkGlm
35:36	RWX	WOX_AND	WOX_OR	THOLD_TIMER_SEL: Selection for the thold transition timer in the IDLE state machine. 0b00=1024 cycles delay, 0b01=512 cycles delay, 0b10=256 cycles delay, 0b11= 128 cycles delay
37	RWX	WOX_AND	WOX_OR	BLOCK_ALL_WAKEUP_SOURCES: Setting this bit will make the PM Slave ignore any Wakeup events (ext. interrupt, malfunction alert, any special wakeup bit). This bit is intended to enable firmware concurrent patch capability. Note: This does NOT block the interrupt from being presented to the processor core. The following procedure is required on changes: 1. Firmware may only set this bit after first setting special wakeup and polling for special wakeup complete (OHA and PCB-slave both in running state with AISS and PM FSMs idle). 2. Firmware may only clear this bit if all special wakeup bits are first cleared.
38	RWX	WOX_AND	WOX_OR	TP_TC_DPLL_TESTMODE_DC: ADPLL test mode
39	RWX	WOX_AND	WOX_OR	PM_SLV_WINKLE_FENCE: Fence off the powered off chiplet in winkle. - Logical fence/hold for pcb_slave and pcb_slave_pm. For electrical fence see bit 23.
40	RWX	WOX_AND	WOX_OR	L3_ENABLE_SWITCH: Setting this bit activates l3_edram_enable if allowed by system configuration GP3(28). Resetting this bit deactivates l3_edram_enable.
41	RWX	WOX_AND	WOX_OR	TP_CPLT_IVRM_REFBYPASS_DC: Signal to iVRM (used to be controlled by scan-only block inside EX, but needs to be driven by VIO domain)
42	RWX	WOX_AND	WOX_OR	CHKSW_HW241939_DISABLE: if this bit is set to 1, the fix for HW241939 (pfet enable SCOM-ability) is disabled
43	RWX	WOX_AND	WOX_OR	CHKSW_HW273115_DISABLE: if this bit is set to 1, the fix for HW273115 (Pga ACK noack issue when the babystepper is in the winkle state) is disabled
44	RWX	WOX_AND	WOX_OR	CHKSW_HW245103_DISABLE: if this bit is set to 1, the fix for HW245103 resonant clocking CSB and SW -bit ordering change is disabled
45	RWX	WOX_AND	WOX_OR	CHKSW_HW257534_DISABLE: if this bit is set to 1, the fix for HW257534 (fencing of errors) is disabled
46	RWX	WOX_AND	WOX_OR	CHKSW_HW259509_ENABLE: if this bit is set to 0, the fix for HW259509 (Pstate change hanging, because of DPLL flock timer in a hung state) is disabled
47	RWX	WOX_AND	WOX_OR	CHKSW_HW260345_DISABLE: if set to 1, this bit disables the HW260345 fix (fix was to make sure that we enter bypass mode for iVRM safe mode without a glitch that could cause Vcs in regulation and Vdd in bypass)
48:49	ROX	NC	NC	WAKEUP_INT_TYPE: (Known to be unreliable and not supported, informational usage only) Type of the last wakeup event that caused an exit from sleep or winkle (excluding nap!), regardless of present state. 0b01: External interrupt. 0b10: Malfunction Alert. 0b11: Special Wakeup. 0b00: chiplet has never fully entered and exited a chiplet-level idle state since IPL of the system. (Note this does not necessarily get updated when the processor core enters an idle state, only if the PCB-Slave enters and then exits the idle state for this chiplet).
50	ROX	NC	NC	DPLL_LOCK: DPLL lock indicator
51	ROX	NC	NC	SPECIAL_WKUP_ALL_SOURCES_ORED: logical OR of all special wakeup sources
52	ROX	NC	NC	REGULAR_WKUP_AVAILABLE: logical OR of external interrupt and malfunction alert



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
53	RWX	WOX_AND	WOX_OR	BLOCK_REG_WKUP_SOURCES: blocks ext. int. and malf. Alert from waking up PCBS (no block possible for PC!)

Register Name	PowerManagement GP1
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PMGP1_REG
Address	00000000140F0103 (PCB) 00000000140F0104 (PCB1) 00000000140F0105 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	SLEEP_POWER_DOWN_EN: Sleep Power Down Enable: When set to 1, causes hardware to automatically reduce voltage to the Core domain when entering Sleep mode. The voltage value for power down is chosen by sleep_power_off_sel (bit 2). When set to 0, a request is sent to the PORE engine for assistance entering Sleep.
1	RWX	WOX_AND	WOX_OR	SLEEP_POWER_UP_EN: Sleep Power Up Enable: When set to 1, enables automated hardware restoration of voltage via PFETs and, if enabled, iVRMs when exiting Sleep mode. If this bit is set to 0 the hardware rely on external means (PORE or equivalent) to restore voltage.
2	RWX	WOX_AND	WOX_OR	SLEEP_POWER_OFF_SEL: Sleep Power Off Select: Selects which voltage level to place the Core domain PFETs upon Sleep entry. 0 = Vret (Fast Sleep Mode), 1 = Voff (Deep Sleep Mode). Depending on the setting of pmicr_latency_en, this bit is controlled with a PCB-write (0) or by the PMICR in the core (1).
3	RWX	WOX_AND	WOX_OR	WINKLE_POWER_DOWN_EN: Winkle Power Down Enable: When set to 1, causes hardware to automatically reduce voltage to the entire Chiplet (both Core and ECO Domains) when entering Winkle mode. The voltage value for power down is chosen by winkle_power_off_sel (bit 5). When set to 0, a request is sent to the PORE engine for assistance entering Winkle.
4	RWX	WOX_AND	WOX_OR	WINKLE_POWER_UP_EN: Winkle Power Up Enable: When set to 1, enables automated hardware PFET enablement when exiting Winkle mode. If this bit is set to 0 the hardware rely on external means (PORE or equivalent) to cause the PFETs to be re-enabled.
5	RWX	WOX_AND	WOX_OR	WINKLE_POWER_OFF_SEL: Winkle Power Off Select: Selects which voltage level to place the Core and ECO domain PFETs upon Winkle entry. 0 = Vret (Fast Winkle Mode), 1 = Voff (Deep Winkle Mode). Depending on the setting of pmicr_latency_en, this bit is controlled with a PCB-write (0) or by the PMICR in the core (1).
6	RWX	WOX_AND	WOX_OR	OHA_WKUP_OVERRIDE_EN: Needs to be 0 for normal operation. If set to 1, the two following dials are used to override the regular and special wakeup signal from PCBS to OHA
7	RWX	WOX_AND	WOX_OR	OHA_PM_WKUP_OVERRIDE: Enablement by 'oha_wkup_override_en' forces the regular wakeup signal to OHA to the value of this bit regardless of presence of an interrupt source.
8	RWX	WOX_AND	WOX_OR	OHA_SPC_WKUP_OVERRIDE: Enablement by 'oha_wkup_override_en' forces the special wakeup signal to OHA to the value of this bit, regardless of the firmware settings.

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
9	RWX	WOX_AND	WOX_OR	ENDP_RESET_PM_ONLY: If asserted, an endpoint reset of all power management-related functions (not the regular PCB slave) is performed. Intended usage is for recovery.
10	RWX	WOX_AND	WOX_OR	DPLL_FREQ_OVERRIDE_ENABLE: override Fmax/Fmin only, if '1', using register FREQ_CTRL_REG
11	RWX	WOX_AND	WOX_OR	PM_SPR_OVERRIDE_EN: PM SPR Override Enable The PPMCR (0xNNNN) and PPMICR (0XXXXX) accesses the register resources that make up the PMCR SPR used by hypervisor to management Pstates. Thus, PCB updates to it are disabled in hardware to prevent collisions. This bit allows ownership of the PMCR to be switched from hypervisor to OCC. This switch is immediate in hardware, thus, firmware must ensure the ownership switch is otherwise communicated. 0 = Disables the writing of the PPMCR (0xNNNN) from the PCB and allows SPR 884 writes (mtspr) to update the register resource. 1 = Enables the writing of the PPMCR (0xNNNN) from the PCB.
12	RWX	WOX_AND	WOX_OR	FORCE_SAFE_MODE: Force Safe Mode 0 = Allow other enabled features to determine the operational Pstate. 1 = Forces the minimum of POHBR[psafe] and PPMSR[global_pstate_actual] Pstate for the core chiplet as the operational frequency.
13	RWX	WOX_AND	WOX_OR	IVRM_SAFE_MODE_EN: Internal VRM Safe Mode Enable 0 = Disable the iVRM safe mode, thus, no automatic actions occur, if an iVRM error happens. 1 = if the iVRMs are enabled (PIVRMCSR[ivrn_en] is set) and Pstates are enabled and if the error defined by dial pcbs_ivrm_gross_or_fine_err occurs, then the railstepper is forced into bypass mode to prevent a voltage-frequency hazard
14	RWX	WOX_AND	WOX_OR	IVRM_SAFE_MODE_FORCE_ACTIVE: Internal VRM Safe Mode Force Dial 0 = the hardware decides whether to activate the iVRM safe mode or not 1 = the iVRM safe mode is forced regardless (this makes only sense if ivrm_fsm_enable=1 and Pstates are enabled)
15	RWX	WOX_AND	WOX_OR	PMICR_LATENCY_EN: Selects how the sleep/winkle latency (which is deep/fast) is controlled. If asserted the PMICR controls the winkle/sleep_power_off_sel in PMGP1, otherwise those bits are controlled via SCOM by OCC.
16	RWX	WOX_AND	WOX_OR	ENABLE_OCC_CTRL_FOR_LOCAL_PSTATE_EFF_REQ: controls, if the HW (for value 0) or OCC (value 1) is in control of the Local Pstate Effective register in PPSTR
17	RWX	WOX_AND	WOX_OR	SERIALIZE_PFET_POWERDOWN: if asserted, the pFET sequencer will sequence the core and the ECO domain one after the other when powering down
18	RWX	WOX_AND	WOX_OR	SERIALIZE_PFET_POWERUP: if asserted, the pFET sequencer will sequence the ECO and the core domain one after the other when powering up
19	RWX	WOX_AND	WOX_OR	DISABLE_FORCE_DEEP_TO_FAST_SLEEP: 0: (normal operation) - If PCB Slave reports a recoverable error or a checkstop, a DEEP sleep operation is forced to FAST. The entries in sleep/winkle_power_off_sel remain unchanged. 1: force to FAST is disabled.



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
20	RWX	WOX_AND	WOX_OR	DISABLE_FORCE_DEEP_TO_FAST_WINKLE: 0: (normal operation) - If PCB Slave reports a recoverable error or a checkstop, a DEEP winkle operation is forced to FAST. The entries in sleep/winkle_power_off_sel remain unchanged. 1: force to FAST is disabled.

Register Name	<i>PFET Control/Status Register For Core And ECO Vdd</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PFVDDCNTLSTAT_REG
Address	00000000140F0106 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	CORE_VDD_PFET_FORCE_STATE: Core Domain PFET Force State Provides a means for firmware to force the core domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 4:5 = 00 (both core_vdd_pfet_val_override AND core_vdd_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
2:3	RW	ECO_VDD_PFET_FORCE_STATE: ECO Domain PFET Force State Provides a means for firmware to force the ECO domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 6:7 = 00 (both eco_vdd_pfet_val_override AND eco_vdd_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
4	RW	CORE_VDD_PFET_VAL_OVERRIDE: Core Domain PFET Value Override 0 = Override is disabled
5	RW	CORE_VDD_PFET_SEL_OVERRIDE: Core Domain PFET Stage Select Override 0 = Override is disabled
6	RW	ECO_VDD_PFET_VAL_OVERRIDE: ECO Domain PFET Value Override 0 = Override is disabled
7	RW	ECO_VDD_PFET_SEL_OVERRIDE: ECO Domain PFET Stage Select Override 0 = Override is disabled
8	RW	CORE_VDD_PFET_ENABLE_REGULATION_FINGER: Core Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the core_vdd_pfet_enable_value.
9	RW	ECO_VDD_PFET_ENABLE_REGULATION_FINGER: ECO Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the eco_vdd_pfet_enable_value.

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Bits	PCB	Field Mnemonic: Description
10:21	RW	CORE_VDD_PFET_ENABLE_VALUE: Core PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the Core Domain PFET Enables directly. If core_vdd_pfet_val_override = 1, a write to this field sets the state of the core PFET Enables until core_vdd_pfet_val_override is cleared. If core_vdd_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the core_vdd_pfet_valN_slav registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
22:25	RW	CORE_VDD_PFET_SEL_VALUE: Core PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure core_vdd_pfet_valN_slav(0:11) where N is 0 to 11 if core_vdd_pfet_sel_override = 1. If core_vdd_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
26:37	RW	ECO_VDD_PFET_ENABLE_VALUE: ECO PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the ECO PFET Enables directly. If ECO_vdd_pfet_val_override = 1, a write to this field sets the state of the ECO PFET Enables until ECO_vdd_pfet_val_override is cleared. If eco_vdd_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the eco_vdd_pfet_valN_slav registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
38:41	RW	ECO_VDD_PFET_SEL_VALUE: ECO PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure eco_vdd_pfet_valN_slav(0:11) where N is 0 to 11 if eco_vdd_pfet_sel_override = 1. If eco_vdd_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
42:45	ROX	CORE_VDD_PG_STATE: Core power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
46:49	ROX	CORE_VDD_PG_SEL: For debug, contains the actual index n into Core Domain PFET Value [n] SLAT Register set that contains the Core PFET Enable Value currently enabled.
50:53	ROX	ECO_VDD_PG_STATE: ECO Domain power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
54:57	ROX	ECO_VDD_PG_SEL: For debug, contains the actual index n into ECO Domain PFET Value [n] SLAT Register set that contains the ECO PFET Enable Value currently enabled.

Register Name	PFET Sense Register	
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PFSENSE_REG	
Address	00000000140F0107 (PCB)	
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:11	ROX	TP_CORE_VDD_PFET_ENABLE_SENSE: Not used any more.
12:23	ROX	TP_ECO_VDD_PFET_ENABLE_SENSE: Not used any more.



Bits	PCB	Field Mnemonic: Description
24:35	ROX	TP_CORE_VCS_PFET_ENABLE_SENSE: Not used any more.
36:47	ROX	TP_ECO_VCS_PFET_ENABLE_SENSE: Not used any more.

Register Name	<i>PM Error Summary Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PMERRSUM_REG
Address	00000000140F0108 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	PM_ERROR: PM Error is present. Intended for use by special PCB multicast to see error state of all chiplets with a single read (via 510F0108 to read all chiplets)

Register Name	<i>PM Error Register:</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PMERR_REG
Address	00000000140F0109 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_HANG_ERR: Hang during Unassisted Sleep Entry: SLEEP_ENTRY_NOTIFY_PMC state
1	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ASSIST_HANG_ERR: Hang during Assisted Sleep Entry: SLEEP_ENTRY_NOTIFY_PMC_ASSIST state
2	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ERR: Hang during Unassisted Sleep Exit: SLEEP_EXIT_NOTIFY_PMC state
3	ROX	PCBS_SLEEP_EXIT_INVOKE_PORE_ERR: Hang during Assisted Deep Sleep Exit: SLEEP_EXIT_INVOKE_PORE state
4	ROX	PCBS_WINKLE_ENTRY_NOTIFY_PMC_ERR: Hang during Unassisted Winkle Entry: WINKLE_ENTRY_NOTIFY_PMC state
5	ROX	PCBS_WINKLE_ENTRY_SEND_INT_ASSIST_ERR: Hang during Assisted Winkle Entry: WINKLE_ENTRY_SEND_INT_ASSIST state
6	ROX	PCBS_WINKLE_EXIT_NOTIFY_PMC_ERR: Hang during Unassisted Winkle Exit: WINKLE_EXIT_NOTIFY_PMC state
7	ROX	PCBS_WAIT_DPLL_LOCK_ERR: Hang during Unassisted Exit waiting on DPLL: WAIT_DPLL_LOCK state
8	ROX	PCBS_SPARE8_ERR: spare bit, always 0
9	ROX	PCBS_WINKLE_EXIT_SEND_INT_ASSIST_ERR: Hang during Assisted Winkle Exit: WINKLE_EXIT_SEND_INT_ASSIST state
10	ROX	PCBS_WINKLE_EXIT_SEND_INT_POWUP_ASSIST_ERR: Hang during Assisted Winkle Exit: WINKLE_EXIT_SEND_INT_POWUP_ASSIST state
11	ROX	PCBS_WRITE_FSM_GOTO_REG_IN_INVALID_STATE_ERR: write to FSM goto register in invalid state
12	ROX	PCBS_WRITE_PMGP0_IN_INVALID_STATE_ERR: write to PMGP0 in invalid state

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Bits	PCB	Field Mnemonic: Description
13	ROX	PCBS_FREQ_OVERFLOW_IN_PSTATE_MODE_ERR: frequency of DPLL in Pstate mode overflows (Fnom + desired Pstate > 511)
14	ROX	PCBS_ECO_RS_BYPASS_CONFUSION_ERR: ECO railstepper tried to exit Vcs bypass and enter Vdd bypass in one Pstate step (it is not clear, in which order this strange operation should be performed - most likely it should never happen to avoid that Vcs is greater than Vdd)
15	ROX	PCBS_CORE_RS_BYPASS_CONFUSION_ERR: same as previous error, but for core railstepper (it is not clear, in which order this strange operation should be performed - most likely it should never happen to avoid that Vcs is greater than Vdd)
16	ROX	PCBS_READ_LPST_IN_PSTATE_MODE_ERR: read LPST-array while iVRM FSMs are enabled (dial ivrm_fsm_enable asserted)
17	ROX	PCBS_LPST_READ_CORR_ERR: correctable error occurred when reading the LPST
18	ROX	PCBS_LPST_READ_UNCORR_ERR: uncorrectable error occurred when reading the LPST
19	ROX	PCBS_PFET_STRENGTH_OVERFLOW_ERR: overflow occurred when calculating the pFET strength (in final rounding step!)
20	ROX	PCBS_VDS_LOOKUP_ERR: Vds entry not found in lookup table (when performing the linear search!)
21	ROX	PCBS_IDLE_INTERRUPT_TIMEOUT_ERR: idle interrupt timeout in PCB interrupt controller
22	ROX	PCBS_PSTATE_INTERRUPT_TIMEOUT_ERR: PState interrupt timeout in PCB interrupt controller
23	ROX	PCBS_GLOBAL_ACTUAL_SYNC_INTERRUPT_TIMEOUT_ERR: GlobalActualSync Interrupt timeout in PCB interrupt controller
24	ROX	PCBS_PMAX_SYNC_INTERRUPT_TIMEOUT_ERR: PmaxSync Interrupt timeout in PCB interrupt controller
25	ROX	PCBS_GLOBAL_ACTUAL_PSTATE_PROTOCOL_ERR: a write to global actual Pstate register has occurred before the global actual Pstate interrupt has left PCBS
26	ROX	PCBS_PMAX_PROTOCOL_ERR: a write to the Pmax/Pmin register has occurred before the Pmax sync interrupt has left PCB
27	ROX	PCBS_IVRM_GROSS_OR_FINE_ERR: iVRM gross or fine error (details to be found in PCBS_ivrm_Control_Status_Reg)
28	ROX	PCBS_IVRM_RANGE_ERR: iVRM range error (summary bit, details to be found in PCBS_ivrm_Control_Status_Reg)
29	ROX	PCBS_DPLL_CPM_FMIN_ERR: DPLL CPM Fmin error
30	ROX	PCBS_DPLL_DCO_FULL_ERR: DPLL DCO full
31	ROX	PCBS_DPLL_DCO_EMPTY_ERR: DPLL DCO empty
32	ROX	PCBS_DPLL_INT_ERR: DPLL internal error
33	ROX	PCBS_FMIN_AND_NOT_CPMBIT_ERR: dpll_fmin_and_not_cpmbit (ref. to dial cpm_fmin_clip_error_sel on how to configure this)
34	ROX	PCBS_DPLL_FASTER_THAN_FMAX_PLUS_DELTA1_ERR: dpll_faster_than_fmax_plus_delta1 (for characterization, delta1 is configurable with pll_char_delta1)
35	ROX	PCBS_DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2_ERR: dpll_slower_than_fmin_minus_delta2 (for characterization, delta2 is configurable with pll_char_delta2)
36	ROX	PCBS_RESCLK_CSB_INSTR_VECTOR_CHG_IN_INVALID_STATE_ERR: RESCLK CSB instruction vector change while FSMs none idle
37	ROX	PCBS_RESCLK_BAND_BOUNDARY_CHG_IN_INVALID_STATE_ERR: RESCLK Band boundaries change while FSMs none idle
38	ROX	PCBS_OCC_HEARTBEAT_LOSS_ERR: OCC heartbeat loss
39	ROX	PCBS_SPARE39_ERR: spare bit, always 0
40	ROX	PCBS_SPARE40_ERR: spare bit, always 0



Bits	PCB	Field Mnemonic: Description
41	ROX	PCBS_SPARE41_ERR: spare bit, always 0
42	ROX	PCBS_SPARE42_ERR: spare bit, always 0

Register Name	<i>PM Error Mask Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PMERRMASK_REG
Address	00000000140F010A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_HANG_ERR_MASK: Mask for this error: 1=masked, 0=not masked
1	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ASSIST_HANG_ERR_MASK: Mask for this error: 1=masked, 0=not masked
2	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
3	RW	PCBS_SLEEP_EXIT_INVOKE_PORE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
4	RW	PCBS_WINKLE_ENTRY_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
5	RW	PCBS_WINKLE_ENTRY_SEND_INT_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
6	RW	PCBS_WINKLE_EXIT_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
7	RW	PCBS_WAIT_DPLL_LOCK_ERR_MASK: Mask for this error: 1=masked, 0=not masked
8	RW	PCBS_SPARE8_ERR_MASK: Mask for this error: 1=masked, 0=not masked
9	RW	PCBS_WINKLE_EXIT_SEND_INT_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
10	RW	PCBS_WINKLE_EXIT_SEND_INT_POWUP_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
11	RW	PCBS_WRITE_FSM_GOTO_REG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
12	RW	PCBS_WRITE_PMGPO_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
13	RW	PCBS_FREQ_OVERFLOW_IN_PSTATE_MODE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
14	RW	PCBS_ECO_RS_BYPASS_CONFUSION_ERR_MASK: Mask for this error: 1=masked, 0=not masked
15	RW	PCBS_CORE_RS_BYPASS_CONFUSION_ERR_MASK: Mask for this error: 1=masked, 0=not masked
16	RW	PCBS_READ_LPST_IN_PSTATE_MODE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
17	RW	PCBS_LPST_READ_CORR_ERR_MASK: Mask for this error: 1=masked, 0=not masked
18	RW	PCBS_LPST_READ_UNCORR_ERR_MASK: Mask for this error: 1=masked, 0=not masked
19	RW	PCBS_PFET_STRENGTH_OVERFLOW_ERR_MASK: Mask for this error: 1=masked, 0=not masked
20	RW	PCBS_VDS_LOOKUP_ERR_MASK: Mask for this error: 1=masked, 0=not masked
21	RW	PCBS_IDLE_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
22	RW	PCBS_PSTATE_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
23	RW	PCBS_GLOBAL_ACTUAL_SYNC_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
24	RW	PCBS_PMAX_SYNC_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked

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Bits	PCB	Field Mnemonic: Description
25	RW	PCBS_GLOBAL_ACTUAL_PSTATE_PROTOCOL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
26	RW	PCBS_PMAX_PROTOCOL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
27	RW	PCBS_IVRM_GROSS_OR_FINE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
28	RW	PCBS_IVRM_RANGE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
29	RW	PCBS_DPLL_CPM_FMIN_ERR_MASK: Mask for this error: 1=masked, 0=not masked
30	RW	PCBS_DPLL_DCO_FULL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
31	RW	PCBS_DPLL_DCO_EMPTY_ERR_MASK: Mask for this error: 1=masked, 0=not masked
32	RW	PCBS_DPLL_INT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
33	RW	PCBS_FMIN_AND_NOT_CPMBIT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
34	RW	PCBS_DPLL_FASTER_THAN_FMAX_PLUS_DELTA1_ERR_MASK: Mask for this error: 1=masked, 0=not masked
35	RW	PCBS_DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2_ERR_MASK: Mask for this error: 1=masked, 0=not masked
36	RW	PCBS_RESCLK_CSB_INSTR_VECTOR_CHG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
37	RW	PCBS_RESCLK_BAND_BOUNDARY_CHG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
38	RW	PCBS_OCC_HEARTBEAT_LOSS_ERR_MASK: Mask for this error: 1=masked, 0=not masked
39	RW	PCBS_SPARE39_ERR_MASK: Mask for this error: 1=masked, 0=not masked
40	RW	PCBS_SPARE40_ERR_MASK: Mask for this error: 1=masked, 0=not masked
41	RW	PCBS_SPARE41_ERR_MASK: Mask for this error: 1=masked, 0=not masked
42	RW	PCBS_SPARE42_ERR_MASK: Mask for this error: 1=masked, 0=not masked

Register Name		<i>PM Special Wakeup FSP</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PMSPCWKUPFSP_REG
Address		00000000140F010B (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RW	FSP_SPECIAL_WAKEUP: Chiplet Special Wakeup for FSP Firmware use. NOTE: protocol is required when setting this bit

Register Name		<i>PM Special Wakeup OCC</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PMSPCWKUPOCC_REG
Address		00000000140F010C (PCB)
Attributes		
Description		



Bits	PCB	Field Mnemonic: Description
0	RW	OCC_SPECIAL_WAKEUP: Chiplet Special Wakeup for OCC Firmware use. NOTE: protocol is required when setting this bit

Register Name	<i>PM Special Wakeup Hypervisor</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PMSPCWKUPPHYP_REG
Address	00000000140F010D (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	PHYP_SPECIAL_WAKEUP: Chiplet Special Wakeup for hypervisor Firmware use. NOTE: protocol is required when setting this bit

Register Name	<i>PFET Control/Status Register For Core And ECO Vcs</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PFVCSCTLSTAT_REG
Address	00000000140F010E (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	CORE_VCS_PFET_FORCE_STATE: Core Domain PFET Force State Provides a means for firmware to force the core domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 4:5 = 00 (both core_vcs_pfet_val_override AND core_vcs_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
2:3	RW	ECO_VCS_PFET_FORCE_STATE: ECO Domain PFET Force State Provides a means for firmware to force the ECO domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 6:7 = 00 (both eco_vcs_pfet_val_override AND eco_vcs_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
4	RW	CORE_VCS_PFET_VAL_OVERRIDE: Core Domain PFET Value Override 0 = Override is disabled
5	RW	CORE_VCS_PFET_SEL_OVERRIDE: Core Domain PFET Stage Select Override 0 = Override is disabled
6	RW	ECO_VCS_PFET_VAL_OVERRIDE: ECO Domain PFET Value Override 0 = Override is disabled
7	RW	ECO_VCS_PFET_SEL_OVERRIDE: ECO Domain PFET Stage Select Override 0 = Override is disabled

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Bits	PCB	Field Mnemonic: Description
8	RW	CORE_VCS_PFET_ENABLE_REGULATION_FINGER: Core Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the core_vcs_pfet_enable_value.
9	RW	ECO_VCS_PFET_ENABLE_REGULATION_FINGER: ECO Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the eco_vcs_pfet_enable_value.
10:21	RW	CORE_VCS_PFET_ENABLE_VALUE: Core PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the Core Domain PFET Enables directly. If core_vcs_pfet_val_override = 1, a write to this field sets the state of the core PFET Enables until core_vcs_pfet_val_override is cleared. If core_vcs_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the core_vcs_pfet_valN_slac registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
22:25	RW	CORE_VCS_PFET_SEL_VALUE: Core PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure core_vcs_pfet_valN_slac(0:11) where N is 0 to 11 if core_vcs_pfet_sel_override = 1. If core_vcs_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
26:37	RW	ECO_VCS_PFET_ENABLE_VALUE: ECO PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the ECO PFET Enables directly. If ECO_vcs_pfet_val_override = 1, a write to this field sets the state of the ECO PFET Enables until ECO_vcs_pfet_val_override is cleared. If eco_vcs_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the eco_vcs_pfet_valN_slac registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
38:41	RW	ECO_VCS_PFET_SEL_VALUE: ECO PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure eco_vcs_pfet_valN_slac(0:11) where N is 0 to 11 if eco_vcs_pfet_sel_override = 1. If eco_vcs_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
42:45	ROX	CORE_VCS_PG_STATE: Core power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
46:49	ROX	CORE_VCS_PG_SEL: For debug, contains the actual index n into Core Domain PFET Value [n] SLAT Register set that contains the Core PFET Enable Value currently enabled.
50:53	ROX	ECO_VCS_PG_STATE: ECO Domain power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
54:57	ROX	ECO_VCS_PG_SEL: For debug, contains the actual index n into ECO Domain PFET Value [n] SLAT Register set that contains the ECO PFET Enable Value currently enabled.



Register Name	<i>PM State History Register For Hypervisor</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPHYP_REG
Address	00000000140F0110 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	PHYP_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	PHYP_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	PHYP_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	PHYP_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	PHYP_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	PHYP_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For FSP</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PMSTATEHISTFSP_REG
Address	00000000140F0111 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	FSP_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	FSP_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	FSP_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	FSP_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.



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Bits	PCB	Field Mnemonic: Description
6	ROX_CLRPAR T	FSP_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	FSP_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For OCC</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PMSTATEHISTOCC_REG
Address	00000000140F0112 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	OCC_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	OCC_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	OCC_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	OCC_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	OCC_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	OCC_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For PerfMon</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPERF_REG
Address	00000000140F0113 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	PERF_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	PERF_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	PERF_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	PERF_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	PERF_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	PERF_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM FSM Reset And Babystepper Idle Injects</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.IDLEFSMGOTOCMD_REG
Address	00000000140F0114 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	WO_1P	idle_fsm_goto_cmd ' A write to this reg will proceed the IDLE FSM from WAIT_FOR_PORE_DONE, SLEEP_EXIT_WAIT_FOR_PORE_FAST_EXIT_DONE, or WINKLE_EXIT_WAIT_FOR_PORE_FAST_EXIT_DONE to the following states: ' 0b01: goto IDLE state ' 0b10: goto SLEEP_EXIT_CORE_MESHLET_ON state ' 0b11: goto WINKLE_EXIT_NOTIFY_PMC state ' "
2	RWX	babystp_trigger_sleep_entry ' A write to this reg with a 1 in this field will cause the babystepper to run the sleep entry sequence. This step is needed for an assisted entry into sleep, before the power is actually turned off since the babystepper needs to know about the sleep state. For an unassisted entry, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished entering its sleep mode. ' "
3	RWX	babystp_trigger_winkle_entry ' A write to this reg with a 1 in this field will cause the babystepper to run the winkle entry sequence. This step is needed for an assisted entry into winkle before the power is actually turned off since the babystepper needs to know about the winkle state. For an unassisted entry, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished entering its winkle mode. ' "
4	RWX	babystp_trigger_wakeup ' A write to this reg with a 1 in this field will cause the babystepper to run the wakeup sequence from sleep/winkle depending on the babystepper state of sleep or winkle. This step is needed for an assisted exit from winkle before the power is actually turned off since the babystepper needs to know about the wakeup state. For an unassisted exit, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished waking up from sleep or winkle. ' "

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Register Name	Core PFET Power Up Delay
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.COREPFPUDLY_REG
Address	00000000140F012C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_POWUP_DLY0: Delay used after transitioning to Core Domain power up sequence stage0. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	CORE_POWUP_DLY1: Delay used after transitioning to Core domain power up sequence stage1.
8:19	RW	CORE_POWER_UP_DELAY_SEL: Vector select for which delay to use for the respective power-up stage. Bit mapping: 8 -> core_*_pfet_enable(0) 9 -> core_*_pfet_enable(1) ... 19 -> core_*_pfet_enable(11) Bit meaning: 0 = Use core_powup_dly0 1 = Use core_powup_dly1

Register Name	Core PFET Power Down Delay
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.COREPFPDDLY_REG
Address	00000000140F012D (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_POWDN_DLY0: Delay used after transitioning to Core domain power dn sequence stage1. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	CORE_POWDN_DLY1: Delay used after transitioning to Core domain power dn sequence stage1. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
8:19	RW	CORE_POWER_DN_DELAY_SEL: Vector select for which delay to use for the respective power-dn stage. Bit mapping: 8 -> core_*_pfet_enable(0) 9 -> core_*_pfet_enable(1) ... 19 -> core_*_pfet_enable(11) Bit meaning: 0 = Use core_powdn_dly0 1 = Use core_powdn_dly1



Register Name	Core PFET Vretention	
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.COREPFVRET_REG	
Address	00000000140F0130 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_VRET_SEL: Pointer to the stage representing the Vretention value for the core PFETs. Power down sequences will stop after enabling this stage.
4:7	RW	CORE_VOFF_SEL: Pointer to the stage representing the Voff value for the core PFETs. Power down sequences will stop after enabling this stage.

Register Name	ECO PFET Power Up Delay	
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.ECOPFPUDLY_REG	
Address	00000000140F014C (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_POWUP_DLY0: Delay used after transitioning to ECO domain power up sequence stage0 in terms of refclk period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	ECO_POWUP_DLY1: Delay used after transitioning to ECO domain power up sequence stage1.
8:19	RW	ECO_POWER_UP_DELAY_SEL: Vector select for which delay to use for the respective power-up stage. Bit mapping: 8 -> eco_*_pfet_enable(0) 9 -> eco_*_pfet_enable(1) ... 19 -> eco_*_pfet_enable(11) Bit meaning: 0 = Use eco_powup_dly0 1 = Use eco_powup_dly1

Register Name	ECO PFET Power Down Delay	
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.ECOPFPDDLY_REG	
Address	00000000140F014D (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_POWDN_DLY0: UNUSED/SPARE
4:7	RW	ECO_POWDN_DLY1: Delay used after transitioning to ECO Domain power dn sequence stage1. The delays in this register are in terms of refclk period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.

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Bits	PCB	Field Mnemonic: Description
8:19	RW	ECO_POWER_DN_DELAY_SEL: Vector select for which delay to use for the respective power-down stage. Bit mapping: 8 -> eco_*_pfet_enable(0) 9 -> eco_*_pfet_enable(1) ... 19 -> eco_*_pfet_enable(11) Bit meaning: 0 = Use eco_powdn_dly0 1 = Use eco_powdn_dly1

Register Name		<i>ECO PFET Vretention</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.ECOPFVRET_REG
Address		00000000140F0150 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_VRET_SEL: Pointer to the stage representing the Vretention value for the ECO PFETs. Power down sequences will stop after enabling this stage.
4:7	RW	ECO_VOFF_SEL: Pointer to the stage representing the Voff value for the ECO PFETs. Power down sequences will stop after enabling this stage.

Register Name		<i>Frequency Control Register With Overrides For DPLL</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.FREQ_CTRL_REG
Address		00000000140F0151 (PCB)
Attributes		
Description		Note that overrides to Dpll_fmax are only applied if Dpll_freq_override_enable = 1. A read of all these dials always returns the currently established DPLL frequencies (regardless of any other mode settings).
Bits	PCB	Field Mnemonic: Description
0:8	RWX	DPLL_FMIN: minimum DPLL frequency in CPM-DPLL mode that is set at IPL time A read always returns the currently established value A write is not conditioned on any other dial setting.
9:17	RWX	DPLL_FMAX: DPLL maximum frequency and frequin (these two values are the same in POWER8 processor) without applying bias values: A read always returns the currently established value A write is conditioned on the setting of dpll_freq_override_enable. If dpll_freq_override_enable is asserted, a write causes this field to update. Otherwise the hardware (that is, PStates) are controlling the update of this value.
18:21	RO	Reserved.
22:30	RW	FREQU_AT_PSTATE0: DPLL frequency for Pstate 0



Register Name	<i>DPLL Mode Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.DPLL_CPM_PARM_REG
Address	00000000140F0152 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	LF_SLEWRATEXPI: out of lock slew rate for DPLL
8	RW	LF_USE_CPMXPI: use CPM instead of PFD as loop filter input, if '1' (instead of using both)
9	RW	FF_USE_CPMXPI: use the CPM inputs for the frequency filter, if '1'
10	RW	CPM_FILTER_ENABLE: enables the CPM filter
11	RW	FF_BYPASSXPI: enables frequency filter bypass
12	RW	DCO_OVERRIDE: enables overrides for DCO testing/characterization
13	RW	DCO_INCR: enables increment for DCO testing/characterization, increments only on a rising edge
14	RW	DCO_DECR: enables decrement for DCO testing/characterization, decrements only on a rising edge
15:23	RW	DPLL_LOCK_TIMER_REPLACEMENT_VALUE: if dpll_lock_replacement_timer_mode_en is set, this dial specifies the delay in us, after which it is assumed, that the DPLL has reached a frequency lock condition. Note that values less than 3 will cause in undefined HW behavior (0 will cause HANGs!). if dpll_lock_replacement_timer_mode_en is zero, this dial specifies the delay in pcb_nclk cycles after which the hardware monitors the DPLL frequout output (if dpll_freqout_mode_en is set) or the DPLL flock output (if dpll_flock_mode_en is set). Note that in this case, the value of this dial needs to be greater or equal to 150 (decimal).
24:31	RW	PRE_VRET_PSTATE: Pstate that is stepped to before switching to Vretention defined in PCBS_iVRM_Control_Status_Reg
32	RW	OVERRIDE_PCBS_DPLL_SYNCHRONIZER: Bypasses the 'ping-pong' synchronization logic between the DPLL and the PCBS-PM. NEVER SET TO 1 UNLESS YOU KNOW WHAT YOU ARE DOING!
33:36	RW	DPLL_CHAR_DELTA1: Delta in DPLL ticks for characterization (cf. dial dpll_faster_than_fmax_plus_delta1)
37:40	RW	DPLL_CHAR_DELTA2: Delta in DPLL ticks for characterization (cf. dial dpll_faster_than_fmin_minus_delta2)

Register Name	<i>PPMSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_STATUS_REG
Address	00000000140F0153 (PCB)
Attributes	
Description	The PPMSR provides read access to the power management status that is also shadowed to the PC and visible to the hypervisor in the PMSR (with some delay due to the shadowing process).

Bits	PCB	Field Mnemonic: Description
0:7	ROX	global_pstate_actual ' Actual Global Pstate Pstate or Pglobal_actual' " Reads from this field return the presently established global PState value.' " "Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent '

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Bits	PCB	Field Mnemonic: Description
8:15	ROX	LOCAL_PSTATE_ACTUAL: ' Actual Local PState or Plocal_actual' " 'Reads from this field return the presently established local PState value. This value will always be less than or equal to global_pstate_actual.' " 'Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent' "
16:23	ROX	pv_min Minimum Pstate set by the platform.
24:31	ROX	pvf_max Maximum Pstate set by the platform.
32	ROX	spr_em_disabled ' SPR Energy Management Disabled' 'Read from this field indicate whether the platform has disabled the ' 'PMCR and PMICR SPRs to control the chiplet PState. '
33	ROX	Psafe_mode_active Read from this field indicate whether the chiplet has been put into a safe mode with Psafe enabled to a OCC heartbeat loss or other externally forced reasons (0=regular mode, 1=safe mode is active)
34	ROX	iVRM_safe_mode_active Read from this field indicate whether the chiplet has been put the iVRM safe mode (forcing the bypass mode for all iVRMs)
35	ROX	ivrm_enable Read from this field indicate whether the chiplet internal voltage regulation macro is enabled for localized voltage control (0=disabled, 1=enabled) based on ANDing the poweron signals to the iVRMs
36	ROX	all_fsms_in_safe_state For recovery: if this bit is asserted, all Pstate and iVRM control FSMs are in a stable, safe state that allows the recovery routine to proceed with resetting the PCBS PM without the risk of interrupt a critical action
37:40	ROX	pmsr_spares spare bits

Register Name	<i>PIVRMCSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_CONTROL_STATUS_REG
Address	00000000140F0154 (PCB)
Attributes	
Description	The PIVRMCSR provides access to chiplet-level controls of the internal VRM rail set (VDD and VCS) across both the core and ECO domains. The following is valid only for bits 4 to 7: when in automatic iVRM mode (ivrm_fsm_enable=1), these bits provide access to the values established by the automatic hardware mechanism. When In iVRM override mode (ivrm_fsm_enable=0), these bits allow firmware direct control of the values driving the internal VRMs.

Bits	PCB	Field Mnemonic: Description
0	RW	IVRM_FSM_ENABLE: Internal master VRM FSM Enable 0 = Disable Internal VRM FSMs and enable to control the iVRMs with the available override registers (SCOMable) as a backup mode or for setup (override mode) 1 = Enable Internal VRM FSM sequencers (requires that Pstates are enabled with enable_Pstate_mode=1 as well) (automatic mode)
1	RW	USE_IVRM_FOR_VRET: Internal VRM Enabled for Vretention 0 = Disable Internal VRM for Vretention 1 = Enable Internal VRM for Vretention
2	RW	BINSEARCH_CAL_ENA: trigger binary search (level signal)

Bits	PCB	Field Mnemonic: Description
3	RW	PVREF_EN: Internal VRM Power Voltage Reference Forced Enable 0 = Allow hardware to enable/disable pvref circuit 1 = Force enablement of the pvref circuit
4	RWX	IVRM_CORE_VDD_BYPASS_B: Internal VRM Core VDD Bypass (negative active) 0 = VDD Internal Core VRMs in bypass 1 = VDD internal Core VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
5	RWX	IVRM_CORE_VDD_POWERON: Internal VRM Core VDD Poweron 0 = Core VDD Internal VRMs powered off 1 = Core VDD internal VRMs powered on if this bit is not set (=0), the Core VDD internal VRM powered off internally. If this bit is set (=1), the Core VDD internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
6	RWX	IVRM_CORE_VCS_BYPASS_B: Internal VRM Core VCS Bypass (negative active) 0 = VCS Internal Core VRMs in bypass 1 = VCS internal Core VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VCS internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VCS internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
7	RWX	IVRM_CORE_VCS_POWERON: Internal VRM Core VCS Poweron 0 = Core VCS Internal VRMs powered off 1 = Core VCS internal VRMs powered on if this bit is not set (=0), the Core VCS internal VRM powered off internally. If this bit is set (=1), the Core VCS internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
8	RWX	IVRM_ECO_VDD_BYPASS_B: Internal VRM ECO VDD Bypass (negative active) 0 = VDD Internal ECO VRMs in bypass 1 = VDD internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
9	RWX	IVRM_ECO_VDD_POWERON: Internal VRM ECO VDD Bypass (negative active) 0 = VDD Internal ECO VRMs in bypass 1 = VDD internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.

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Bits	PCB	Field Mnemonic: Description
10	RWX	IVRM_ECO_VCS_BYPASS_B: Internal VRM ECO VCS Bypass (negative active) 0 = VCS Internal ECO VRMs in bypass 1 = VCS internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VCS internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VCS internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
11	RWX	IVRM_ECO_VCS_POWERON: Internal VRM ECO VCS Poweron 0 = ECO VCS Internal VRMs powered off 1 = ECO VCS internal VRMs powered on if this bit is not set (=0), the ECO VCS internal VRM powered off internally. If this bit is set (=1), the ECO VCS internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
12:18	RWX	IVRM_VRET_VDD: if use_ivrm_for_Vret is asserted, this dial is used to control the Vdd retention voltage. Note: this field will establish the Core VDD rail for Sleep and both the Core and ECO rail for Winkle. - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
19:25	RWX	IVRM_VRET_VCS: if use_ivrm_for_Vret is asserted, this dial is used to control the Vcs retention voltage. Note: this field will establish the Core VDD rail for Sleep and both the Core and ECO rail for Winkle. - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
26:30	RWX	IVRM_VRET_CORE_VDD_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the Core Vdd iVRM PFET strength for the retention voltage
31:35	RWX	IVRM_VRET_CORE_VCS_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the Core Vcs iVRM PFET strength for the retention voltage
36:40	RWX	IVRM_VRET_ECO_VDD_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the ECO Vdd iVRM PFET strength for the retention voltage
41:45	RWX	IVRM_VRET_ECO_VCS_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the ECO Vcs iVRM PFET strength for the retention voltage
46	RW	PVREF_FAIL: voltage reference fail input to iVRMs
47	ROX	IVRM_PREF_ERROR_GROSS: Voltage Reference Gross Error 0 = Gross Error not detected 1 = Gross Error detected
48	ROX	IVRM_PREF_ERROR_FINE: Voltage Reference Fine Error 0 = Fine Error not detected 1 = Fine Error detected
49	ROX	IVRM_CORE_VDD_RANGE_HI: Core VDD Internal VRM Range Hi Indicator 0 = Core VDD Internal VRM Hi indicator signal not asserted 1 = Core VDD internal VRMs Hi indicator signal asserted
50	ROX	IVRM_CORE_VDD_RANGE_LO: Core VDD Internal VRM Range Low Indicator 0 = Core VDD Internal VRM Low indicator signal not asserted 1 = Core VDD internal VRMs Low indicator signal asserted

Bits	PCB	Field Mnemonic: Description
51	ROX	IVRM_ECO_VDD_RANGE_HI: ECO VDD Internal VRM Range Hi Indicator 0 = ECO VDD Internal VRM Hi indicator signal not asserted 1 = ECO VDD internal VRMs Hi indicator signal asserted
52	ROX	IVRM_ECO_VDD_RANGE_LO: ECO VDD Internal VRM Range Low Indicator 0 = ECO VDD Internal VRM Low indicator signal not asserted 1 = ECO VDD internal VRMs Low indicator signal asserted
53	ROX	IVRM_CORE_VCS_RANGE_HI: Core VCS Internal VRM Range Hi Indicator 0 = Core VCS Internal VRM Hi indicator signal not asserted 1 = Core VCS internal VRMs Hi indicator signal asserted
54	ROX	IVRM_CORE_VCS_RANGE_LO: Core VCS Internal VRM Range Low Indicator 0 = Core VCS Internal VRM Low indicator signal not asserted 1 = Core VCS internal VRMs Low indicator signal asserted
55	ROX	IVRM_ECO_VCS_RANGE_HI: ECO VCS Internal VRM Range Hi Indicator 0 = ECO VCS Internal VRM Hi indicator signal not asserted 1 = ECO VCS internal VRMs Hi indicator signal asserted
56	ROX	IVRM_ECO_VCS_RANGE_LO: ECO VCS Internal VRM Range Low Indicator 0 = ECO VCS Internal VRM Low indicator signal not asserted 1 = ECO VCS internal VRMs Low indicator signal asserted
57	ROX	BINSEARCH_CAL_DONE: binary search done signal
58	RWX	IVRM_CORE_VDD_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
59	RWX	IVRM_CORE_VCS_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
60	RWX	IVRM_ECO_VDD_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
61	RWX	IVRM_ECO_VCS_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
62	RW	IVRM_POWER_DOWN_DISABLE: If this bit is 1, the iVRM poweron signal is left asserted. Power off of the iVRMs is then blocked

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Register Name	PIVRMVSR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VALUE_SETTING_REG
Address	00000000140F0155 (PCB)
Attributes	
Description	The PIVRMVSR allows access to VID values and PFET strength valid signal settings presented to the internal VRM rail set (VDD and VCS) across both the core and ECO domains. When in <code>ivrm_fsm_enable = "auto"</code> mode, this register provides access to the values established by the automatic hardware mechanism. When <code>ivrm_fsm_enable = "override"</code> mode, this register allows firmware direct control of the values driving the internal VRMs which, if the VRMs are not in bypass, will move the voltage settings.

Bits	PCB	Field Mnemonic: Description
0:7	RWX	IVRM_CORE_VDD_IVID: When read, returns the value presently being driving to the Core VDD iVRM. If <code>ivrm_fsm_enable = 0</code> (override_mode), then writes to this field will drive a new VID value to the Core VDD iVRM. If <code>ivrm_fsm_enable = 1</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
8:15	RWX	IVRM_CORE_VCS_IVID: When read, returns the value presently being driving to the Core VCS iVRM. If <code>ivrm_fsm_enable = 0</code> (override_mode), then writes to this field will drive a new VID value to the Core VCS iVRM. If <code>ivrm_fsm_enable = 1</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
16:23	RWX	IVRM_ECO_VDD_IVID: When read, returns the value presently being driving to the Core VDD iVRM. If <code>ivrm_fsm_enable = 0</code> (override_mode), then writes to this field will drive a new VID value to the ECO VDD iVRM. If <code>ivrm_fsm_enable = 1</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
24:31	RWX	IVRM_ECO_VCS_IVID: When read, returns the value presently being driving to the ECO VCS iVRM. If <code>ivrm_fsm_enable = 0</code> (override_mode), then writes to this field will drive a new VID value to the ECO VCS iVRM, If <code>ivrm_fsm_enable = 0</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
32:36	RWX	IVRM_CORE_VDD_PFET_STRENGTH: When read, returns the value presently being driving to the core VCS iVRM. If <code>ivrm_fsm_enable = 0</code> (override_mode), then writes to this field will drive a new strength value to the core VCS iVRM, If <code>ivrm_fsm_enable = 0</code> , writes to this field are not performed.

Bits	PCB	Field Mnemonic: Description
37:41	RWX	IVRM_CORE_VCS_PFET_STRENGTH: This register is assigned to the signals tcex##_tp_ivrm_core_vcs_sense & tcex##_tp_ivrm_core_vdd_sense & tcex##_tp_ivrm_eco_vcs_sense & tcex##_tp_ivrm_eco_vdd_sense & 0b0 Note that all other sense signals are spares now and tied to 0. OUTDATED TEXT: When read, returns the value presently being driving to the core VDD iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the core VDD iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
42:46	RWX	IVRM_ECO_VDD_PFET_STRENGTH: When read, returns the value presently being driving to the ECO VCS iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the ECO VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
47:51	RWX	IVRM_ECO_VCS_PFET_STRENGTH: When read, returns the value presently being driving to the ECO VDD iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the ECO VDD iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
52	RWX	IVRM_VDD_CORE_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the Core VDD iVRM. If ivrm_fsm_enable = 1 AND ivrm_control_mode = 1 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the Core VDD iVRM, If ivrm_fsm_enable = 0 OR ivrm_control_mode = 0, writes to this field are not performed.
53	RWX	IVRM_VCS_CORE_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the Core VCS iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the Core VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
54	RWX	IVRM_VDD_ECO_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the ECO VDD iVRM. If ivrm_fsm_enable = 1 AND ivrm_control_mode = 1 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the ECO VDD iVRM, If ivrm_fsm_enable = 0 OR ivrm_control_mode = 0, writes to this field are not performed.
55	RWX	IVRM_VCS_ECO_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the ECO VCS iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the ECO VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
56	RWX	CORE_VDD_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
57	RWX	CORE_VCS_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
58	RWX	ECO_VDD_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
59	RWX	ECO_VCS_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.

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Register Name		General PCBS Modes And Chicken Switches
Mnemonic		EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBSPM_MODE_REG
Address		00000000140F0156 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RW	ENABLE_PSTATE_MODE: if asserted, Pstate requests (from overrides or PMCR) will be honored, otherwise, the hardware does not do anything. Note to firmware: this is the master switch for Pstates and should be asserted after all sub-modes (that is, lvrn_fsm_en) are setup to avoid enabling unintentional modes during the mode setup.
1	RW	GLOBAL_PSTATE_CHANGE_FOR_IDLE_STATE_ENABLED: if asserted, a global Pstate change to the Nap/Sleep/Winkle-Pstate is requested, when the Nap/Sleep/Winkle state is entered and the individual enable bits in the PIMCR are asserted
2	RW	ENABLE_GLOBAL_PSTATE_REQ: if '1' then enable PMC interrupt with global Pstate change request, otherwise, disable global requests
3	RW	ENABLE_WINKLE_WITH_CPM_MODE: if '1', PCBS automatically changes the DPLL mode to mode 1, when entering winkle, but changes the mode back to CPM mode when exiting. Needed for CPM-DPLL control loop enablement.
4	RW	ENABLE_CLIPPING_OF_GLOBAL_PSTATE_REQ: if '1', PCBS automatically clips global Pstate requests with Pvf_max in PPMBR and sets the 'donate' bit in the interrupt accordingly
5	RW	CHKSW_HW214553: if deasserted, HW214553 (frequin issue in resclk mode) is fixed, if asserted, the fix is not active
6	RW	ENABLE_PMC_PMAX_SYNC_NOTIFICATION: if asserted, the PCBS-PM will send a 'Pmax_sync' interrupt, once the synchronization criterion is met
7	RW	DPLL_LOCK_REPLACEMENT_TIMER_MODE_EN: Select a timer instead of the DPLL lock bit as target frequency reached criterion. This timer has to be setup by the dial dpll_lock_timer_replacement_value. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
8	RW	DPLL_FREQOUT_MODE_EN: Looks at the DPLL frequout to find out, if the target frequency has been reached. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
9	RW	DPLL_FLOCK_MODE_EN: Looks at the real DPLL flock output to find out, if the target frequency has been reached. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
10	RW	ENABLE_SENSE_DELAY_CHARACTERIZATION: If this switch is 0, the sense latches are updated every cycle. If this switch is 1, the sense delay measurement mode is enabled, that starts a sense delay timer, whenever one of the registers that drive the inputs of the iVRMs/pFETs is written via PCB and that triggers a sense register freeze operation, when the sense delay timer reaches the value sense_delay_timer_val. With this mode, the sense delays can be measured in multiples of the PCB-slave clock speed.
11:17	RW	SENSE_DELAY_TIMER_VAL: See the description of enable_sense_delay_characterization for details.
18:19	RW	CPM_FMIN_CLIP_ERROR_SEL: This dial selects, which of the following conditions will cause the FIR bit dpll_fmin_and_not_cpmbit to be set to detect, that the DPLL runs at Fmin, but is still clipped by the CPMs. 0b00 = function is disabled 0b01 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit2 = 0 0b10 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit1 = 0 0b11 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit0 = 0
20:23	RW	DBG_TRACE_SEL: This dial selects the group of signals to be traced for debug in the lab. Details to be found in the Section 'Trace Bus'

Bits	PCB	Field Mnemonic: Description
24:25	RW	TRACE_DATA_SEL: This dial selects the group of signals to be traced for debug in the lab. Details to be found in the Section 'Trace Bus'
26:29	RW	TP_CPLT_IVRM_VPP_TUNE: Tune bits to be set going to the iVRMs

Register Name	<i>PIVRMPS Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_PFETSTR_SENSE_REG
Address	00000000140F0157 (PCB)
Attributes	
Description	This PIVRMPS is used to check that the pFET sense outputs correspond to the driven values (mainly for test).

Bits	PCB	Field Mnemonic: Description
0:4	ROX	IVRM_CORE_VDD_PFETSTR_SNS: Not used any more.
5:9	ROX	IVRM_CORE_VCS_PFETSTR_SNS: This register is assigned to the signals tcex##_tp_ivrm_core_vcs_sense & tcex##_tp_ivrm_core_vdd_sense & tcex##_tp_ivrm_eco_vcs_sense & tcex##_tp_ivrm_eco_vdd_sense & 0b0
10:14	ROX	IVRM_ECO_VDD_PFETSTR_SNS: Not used any more.
15:19	ROX	IVRM_ECO_VCS_PFETSTR_SNS: Not used any more.
20	ROX	IVRM_VDD_CORE_PFETSTR_VALID_SNS: Not used any more.
21	ROX	IVRM_VCS_CORE_PFETSTR_VALID_SNS: Not used any more.
22	ROX	IVRM_VDD_ECO_PFETSTR_VALID_SNS: Not used any more.
23	ROX	IVRM_VCS_ECO_PFETSTR_VALID_SNS: Not used any more.
24	ROX	CORE_VDD_BYPASS_B_SENSE: Not used any more.
25	ROX	CORE_VCS_BYPASS_B_SENSE: Not used any more.
26	ROX	ECO_VDD_BYPASS_B_SENSE: Not used any more.
27	ROX	ECO_VCS_BYPASS_B_SENSE: Not used any more.
28	ROX	CORE_VDD_POWERON_SENSE: Not used any more.
29	ROX	CORE_VCS_POWERON_SENSE: Not used any more.
30	ROX	ECO_VDD_POWERON_SENSE: Not used any more.
31	ROX	ECO_VCS_POWERON_SENSE: Not used any more.
32	ROX	CORE_VDD_VPUMP_EN_SENSE: Not used any more.
33	ROX	CORE_VCS_VPUMP_EN_SENSE: Not used any more.
34	ROX	ECO_VDD_VPUMP_EN_SENSE: Not used any more.
35	ROX	ECO_VCS_VPUMP_EN_SENSE: Not used any more.
36	ROX	CORE_VDD_PFET_LOW_VOUT_SNS: Not used any more.
37	ROX	CORE_VCS_PFET_LOW_VOUT_SNS: Not used any more.
38	ROX	ECO_VDD_PFET_LOW_VOUT_SNS: Not used any more.
39	ROX	ECO_VCS_PFET_LOW_VOUT_SNS: Not used any more.

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Register Name	PPMICR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_IDLE_CONTROL_REG
Address	00000000140F0158 (PCB)
Attributes	
Description	The PPMICR is used to read the PMICR register typically owned (written) by the hypervisor. Writes are conditioned on the setting of the dial Pm_spr_override_en. If Pm_spr_override_en is set, firmware needs to make sure that the special wakeup state of this chiplet is reached before changing any of the latency fields in this register. Otherwise, the hardware behavior is undefined.

Bits	PCB	Field Mnemonic: Description
0:7	ROX	NAP_PSTATE_REQ: Nap Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
8	ROX	NAP_PSTATE_EN: Nap PState Enable 1 = Enable the Nap Pstate (NPS) Request, Nap Global Enable and Nap Latency functions 0 = Disables the Nap Pstate (NPS) Request, Nap Global Enable and Nap Latency functions Reads from the field return the value last written.
9	ROX	NAP_GLOBAL_EN: Nap Global Enable 1 = Upon the execution of a Nap instruction , the Nap Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a Nap instruction , the Nap Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.
10:11	ROX	NAP_LATENCY: Nap Latency not supported for POWER8 processor
12:15	ROX	RESERVED_PPMICR_0: reserved
16:23	ROX	SLEEP_PSTATE_REQ: sleep Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
24	ROX	SLEEP_PSTATE_EN: sleep PState Enable 1 = Enable the sleep Pstate (NPS) Request, sleep Global Enable and sleep Latency functions 0 = Disables the sleep Pstate (NPS) Request, sleep Global Enable and sleep Latency functions Reads from the field return the value last written.
25	ROX	SLEEP_GLOBAL_EN: sleep Global Enable 1 = Upon the execution of a sleep instruction , the sleep Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a sleep instruction , the sleep Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.

Bits	PCB	Field Mnemonic: Description
26:27	ROX	SLEEP_LATENCY: sleep Latency 00 = Cease instructions and honors Pstate change but does not perform additional state changing actions (unsupported in POWER8, maps to 0b10) 01 = Indicates to the platform that a sub-state that would have the lowest latency is enabled (unsupported in POWER8, maps to 0b10) 10 = Indicates to the platform that a sub-state that might have a medium exit latency is enabled (POWER8: Fast Sleep) 11 = Indicates to the platform that a sub-state that might have higher exit latency is enabled (POWER8: Deep Sleep)
28:31	ROX	RESERVED_PPMICR_1: reserved
32:39	ROX	WINKLE_PSTATE_REQ: winkle Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
40	ROX	WINKLE_PSTATE_EN: winkle PState Enable 1 = Enable the winkle Pstate (NPS) Request, winkle Global Enable and winkle Latency functions 0 = Disables the winkle Pstate (NPS) Request, winkle Global Enable and winkle Latency functions Reads from the field return the value last written.
41	ROX	WINKLE_GLOBAL_EN: winkle Global Enable 1 = Upon the execution of a winkle instruction , the winkle Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a winkle instruction , the winkle Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.
42:43	ROX	WINKLE_LATENCY: winkle Latency 00 = Cease instructions and honors Pstate change but does not perform additional state changing actions (unsupported in POWER8, maps to 0b10) 01 = Indicates to the platform that a sub-state that would have the lowest latency is enabled (unsupported in POWER8, maps to 0b10) 10 = Indicates to the platform that a sub-state that might have a medium exit latency is enabled (POWER8: Fast Winkle) 11 = Indicates to the platform that a sub-state that might have higher exit latency is enabled (POWER8: Deep Winkle)
44:47	ROX	RESERVED_PPMICR_2: reserved

Register Name	PPMCR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_CONTROL_REG
Address	00000000140F0159 (PCB)
Attributes	
Description	The PPMCR provides read access to the PMCR register shadow in the PCBS typically owned (written) by the hypervisor. Writes are conditioned on the setting of PMGP1[pm_spr_override_en].

Bits	PCB	Field Mnemonic: Description
0:7	RWX	GLOBAL_PSTATE_REQ: global Pstate request from hypervisor (or OCC)
8:15	RWX	LOCAL_PSTATE_REQ: local Pstate request from hypervisor or OCC
16	RWX	AUTO_OVERRIDE0_PSTATE_LIMIT_EN: automatic override Pstate 0 (for low activity detection) is enabled, if asserted



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Bits	PCB	Field Mnemonic: Description
17	RWX	AUTO_OVERRIDE1_PSTATE_LIMIT_EN: automatic override Pstate 1 (reserved for future use) is enabled, if asserted
18:23	RWX	RESERVED_PPMCR: reserved
24:31	RWX	AUTO_OVERRIDE_PSTATE0: automatic override Pstate 0 (for low activity detection)
32:39	RWX	AUTO_OVERRIDE_PSTATE1: automatic override Pstate 1 (reserved for future use)

Register Name	<i>Control Register That Is Written By PMC Sequencer</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_PMC_VF_CTRL_REG
Address	00000000140F015A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PGLOBAL_ACTUAL: global actual Pstate
8:15	RW	MAXREGVCS: maximum regulation point for Vcs, Bit 0 is reserved, bits 1 to 7 are in iVID format
16:23	RW	MAXREGVDD: maximum regulation point for Vdd, Bit 0 is reserved, bits 1 to 7 are in iVID format
24:31	RW	EVIDVCS_EFF: eff. external voltage ID for Vcs in iVID format, Bit 0 is reserved
32:39	RW	EVIDVDD_EFF: eff. external voltage ID for Vdd in iVID format, Bit 0 is reserved

Register Name	<i>Undervolting Register For PCBS</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_UNDERVOLTING_REG
Address	00000000140F015B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PUV_MIN: minimum Pstate for which undervolting is allowed
8:15	RW	PUV_MAX: maximum Pstate for which undervolting is allowed
16:21	RW	KUV: this value indicates how many Pstate ticks a voltage request is undervolted (clipped with Puv_min). Note that the Kuv value is signed

Register Name	<i>PPSIBR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_INDEX_BOUND_REG
Address	00000000140F015C (PCB)
Attributes	
Description	The PPSIBR enables setting the minimum and maximum Pstate that is supported as a pointer into the local Pstate table (which has entries from 0 to 127).

Bits	PCB	Field Mnemonic: Description
0:7	RW	LPSI_MIN: this Pstate index is the index that corresponds to array entry 0. Note that the index domain is obtained by adding 128 to a Pstate, thus, the value is unsigned.
8:14	RW	LPSI_ENTRIES_MINUS_1: this dial contains the value of the number of entries in the Pstate table minus 1

Register Name	<i>PPMBR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_BOUNDS_REG
Address	00000000140F015D (PCB)
Attributes	
Description	The PPMBR enables setting the Pstate bounds that are managed by the OCC. If dial Enable_pmc_pmax_sync_notification is set, firmware must wait after each write to this register until PMC has received the Pmax Sync Interrupt. If a write happens to this register while the previously scheduled Pmax Sync Interrupt has not yet left the PCBS, the error TBD will be set.

Bits	PCB	Field Mnemonic: Description
0:7	RW	PMIN_CLIP: minimum Pstate allowed for this chiplet
8:15	RW	PMAX_CLIP: maximum Pstate allowed for this chiplet (has to be greater or equal to Pmin_clip)

Register Name	<i>PPTCR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_CTRL_REG
Address	00000000140F015E (PCB)
Attributes	
Description	The PPTCR controls the address for writing the local Pstate Table Array (all 96 words are accessible). Note that the protocol requires this register to be set up with the Pstate address first, if a read or a write of the Pstate array is intended, to make sure that the initial address is set correctly. The register PPTR must always be written or read afterward. Note that any access to the PPTR auto-increments this register.

Bits	PCB	Field Mnemonic: Description
0:6	RWX	PSTATE_TABLE_ADDRESS: This is the address of the Pstate table in PCBS, which is auto-incremented after any access to the PTLR.

Register Name	<i>PPTR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_REG
Address	00000000140F015F (PCB)
Attributes	
Description	The PPTR controls the data to be written into the Pstate table and returns the data for a read of the Pstate table. Note that the protocol requires for a write to set this register up after first setting up PPTCR (if the user does not rely on the auto-increment function of the address). For a read of the Pstate table, this register must be read after first setting up PPTCR as well (again if the auto-increment feature of the address is not used). Any access to this register auto-increments the Pstate_table_address by 1. Note also that the read functionality of this register is only functional if PIVRMCSR[ivrm_fsm_enable] = 0. The write functionality works in any case.

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Bits	PCB	Field Mnemonic: Description
0:63	RW	pstate_data This is the field for data bits 0 to 63

Register Name	PPSTR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_STEP_TARGET_REG
Address	00000000140F0160 (PCB)
Attributes	
Description	The PPSTR provides read access to several intermediate values in the Pstate computation pipeline. Writes Are conditioned on the setting of PMGPO[enable_OCC_ctrl_for_local_Pstate_eff_req].

Bits	PCB	Field Mnemonic: Description
0:7	RWX	LOCAL_PSTATE_EFF_REQ: this field represents the effective local Pstate request right before the clipping with Pmin and Pmax if enable_OCC_ctrl_for_local_Pstate_eff_req=0 then the hardware controls this dial, that updates every cycle if enable_OCC_ctrl_for_local_Pstate_eff_req=1 then OCC is in control and can write this field to control the effective local Pstate request that will eventually propagate through the downstream logic and determine the Local PState Actual. Note: if no write to this register is performed, the currently established value is maintained stable forever.
8:15	ROX	LOCAL_PSTATE_TARGET: This field is the target Pstate of a complete Pstate change that is performed in smaller steps
16:23	ROX	LOCAL_CORE_PSTATE_STEP_TARGET: this field represents the intermediate value that is about to be established as the next Local Pstate Actual after completing one step in the process of the transition towards the 'local_Pstate_target' the new voltage, frequency, and clock resonance setting
24:31	ROX	LOCAL_ECO_PSTATE_STEP_TARGET: this field represents the intermediate value that is about to be established as the next Local Pstate Actual after completing one step in the process of the transition towards the 'local_Pstate_target' the new voltage, frequency, and clock resonance setting

Register Name	Read-Only Status Register For DPLL And For Debugging (PDSR)
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_DPLL_STATUS_REG
Address	00000000140F0161 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:14	ROX	DPLL_FF_FREQOUT: frequout output from DPLL (current frequency - bits 2 to 10 correspond to the same scale as the 9 bits of frequin (which need to be multiplied with our frequency step to get the real frequency), the remaining bits just provide a higher accuracy)
15	ROX	DPLL_FREQU_CHANGE: DPLL Frequency change (pin of DPLL without filter)
16	ROX	DPLL_STATUS_SPARE_BIT1: Spare bit.
17	ROX	PMAX_SYNC_PENDING: gets asserted, if the logic has a Pmax sync interrupt outstanding that will be eventually sent to PMC when the Pmax sync criterion is met
18	ROX	GA_ACK_PENDING: gets asserted, if the logic has a global actual Pstate update acknowledgment interrupt outstanding that will be eventually sent to PMC when the GA ack criterion is met
19:26	ROX	CAPPED_GLOBAL_PSTATE_REQ: corresponds to the capped global Pstate request that is presented as Pstate interrupt and send to PMC

Bits	PCB	Field Mnemonic: Description
27	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT2: DPLL runs at Fmax and CPM bit 2 is set. Note that this bit and the following 2 bits indicate, that the CPMs would allow the DPLL to run faster than Fmax.
28	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT3: DPLL runs at Fmax and CPM bit 3 is set
29	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT4: DPLL runs at Fmax and CPM bit 4 is set
30	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT2: DPLL runs at Fmin and CPM bit2 is zero. Note that this bit and the following 2 bits indicate, that the CPMs indicate, that the DPLL should run slower than the currently established Fmin.
31	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT1: DPLL runs at Fmin and CPM bit1 is zero
32	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT0: DPLL runs at Fmin and CPM bit0 is zero
33	ROX_CLRPAR T	DPLL_FASTER_THAN_FMAX_PLUS_DELTA1: The DPLL indicated that it ran once faster than Fmax+dpll_char_delta1
34	ROX_CLRPAR T	DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2: The DPLL indicated that it ran once slower than Fmin-dpll_char_delta2
35:48	ROX	DPLL_MAX_FREQOUT_AFTER_LAST_READ: This dial indicates the maximum DPLL frequout value after the last read of this register (only 14 MSBs)
49:62	ROX	DPLL_MIN_FREQOUT_AFTER_LAST_READ: This dial indicates the minimum DPLL frequout value after the last read of this register (only 14 MSBs)

Register Name	<i>The PIVRMVCR0 Controls The Voltage Stepping Delays</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG0
Address	00000000140F0162 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	IVRM_REQ_PSTATE_STEPDELAY_RISING: Requested Internal Pstate Baby Step Delay - Rising Step. Delay before allowing the next step for a rising Pstate Transition. This dial and ivrm_req_Pstate_stepdelay_lowering allow for differing delays for the two directional transitions if necessary. In 100ns units as established by scan dial ivrm_100ns_value
8:15	RW	IVRM_REQ_PSTATE_STEPDELAY_LOWERING: Requested Internal Pstate Baby Step Delay - Lowering Step. Delay before allowing the next step for a lower Pstate Transition. This dial and ivrm_req_Pstate_stepdelay_rising allow for differing delays for the two directional transitions if necessary. In 100ns units as established by scan dial ivrm_100ns_value

Register Name	<i>The PIVRMVCR1 Controls The Voltage Stepping Delays</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG1
Address	00000000140F0163 (PCB)
Attributes	
Description	

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Bits	PCB	Field Mnemonic: Description
0:7	RW	IVRM_STABILIZE_DELAY_RUN: Stabilization Delay - Run Time Delay to allow a rail to stabilize upon a baby step while the region is operational. In 100ns units as established by scan dial ivrm_100ns_value
8:15	RW	IVRM_STABILIZE_DELAY_IDLE: Stabilization Delay - Idle Transition Delay to allow a rail to stabilize upon a baby step during an idle transition where the activity in the region is quiesced. In 100ns units as established by scan dial ivrm_100ns_value
16:23	RW	IVRM_PFSTR_PROP_DELAY: PFET Strength Propagation Delay Time from PFET Strength values being launched till PFET Strength Valid is asserted. In order to ensure like rails across domains (Core VDD<>ECO VDD, Core VCS<>ECO VCS) are in sync during operational mode, this time value applies to all rails across the domains. This parameter allows for PFET Strength values to settle before PFET Strength Valid is sampled in the Uregs. The value set must the maximum delay for the worst rail timing and must allow for any metastability settling (for example, normally 2-3 cycles for single signals in an asynch handshake interface)
24:31	RW	IVRM_PFSTRVALID_PROP_DELAY: PFETStrength Valid Propagation Delay Time from ivrm_pfstr_prop_delay expiring to where PFET Strength Valid is deasserted. The value is the maximum of a) the minimum pulse width required for PFETStrength Valid and b) the propagation of PFETStrength Valid through (or enough of) the daisy chain. In order to ensure like rails across domains (Core VDD<>ECO VDD, Core VCS<>ECO VCS) are in sync during operational mode, this time value applies to all rails across the domains and thus must be the set to the value of the worst (slowest) rail. The minimum pulse width cannot be violated. The propagation delay can be tuned for more aggressive timing (for example, de-assert before the actual propagation is complete). Measured in prv_nclk cycles. The min delay is 2 cycles. Additional delay can be configured with the following settings 0x00 = No additional delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks
32:39	RW	IVRM_VPUMP_POWERON_TIME: iVRM (VRreg and UReg) - Vpump Power On Time Time necessary for the distributed internal VRM macro circuits to power on. Same delay is required for power on voltage pump circuit. Both delays are in the 8us range. In 100ns units as established by scan dial ivrm_100ns_value
40:47	RW	IVRM_BYPASS_DELAY: iVRM Bypass Propagation Delay Delay time for bypass_b signal propagation. Measured in prv_nclk cycles Target: 50ns 0x00 = No delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks

Bits	PCB	Field Mnemonic: Description
48:55	RW	PFET_VPUMP_ENABLE_DELAY: PFET and Vpump Enable Propagation Delay Delay time for PFET enable and vpump enable signal propagation. Target: 130ns Measured in prv_nclk cycles 0x00 = No delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks
56:62	RW	IVRM_VID_VOUT_THRESHOLD: VID threshold If the output voltage (Vout) is targeting a value below this threshold the slow PFET can backed off from its normal drive strength so as to reduce the ripple at these lower voltage conditions

Register Name	POHR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_OCC_HEARTBEAT_REG
Address	00000000140F0164 (PCB)
Attributes	
Description	Controls the behavior of the OCC heartbeat function.

Bits	PCB	Field Mnemonic: Description
0:7	RW	occ_heartbeat_time 'OCC Heartbeat Time Value' " 'This field defines the number of ~64us hang timer pulses in which a a PCB read or write of the heartbeat trigger register (of which the offset is specified by dial occ_heartbeat_reg_addr_offset) is not detected that will constitute the loss of the OCC heartbeat. If occ_heartbeat_en is set and upon this loss detection, POHBR[psafe] is forced and, if enabled, the error TBD is activated ' ' 0x00 - unsupported, causes undefined behavior' 0x01 - 64us +0/-1us' 0x02 - 128us +0/-1us' ...' 0xFF - 16320us +0/-1us 16.3ms' " 'Upon the 64us hang pulse, the decremter ticks. if the decremter reaches x00, the heartbeat loss event is triggered.' ' '
8	RW	occ_heartbeat_enable 'OCC Heartbeat Timer Enable' " '0 = Disable the OCC Heartbeat function. Lack of accesses to the register defined by the dial occ_heartbeat_reg_addr_offset does not result in heartbeat loss events to be triggered (no FIRs set nor Safe mode entry).' " '1 = Enable the OCC Heartbeat function.'
9:16	RW	occ_heartbeat_reg_addr_offset This dial allows to configure the address offset within the PCBS power management entity of the register, that will regularly reset the heartbeat timer (which is called heartbeat trigger register). The address offset is 0x100 plus the value of this dial.
17:24	RW	Psafe 'Pstate Safe' " 'This field establishes the Pstate that the core chiplet will take on if: 'psafe <= PMSR[global_actual_pstate] 'AND any of the following conditions are true:' 'Loss of OCC Heartbeat if occ_heartbeat_en is set' 'PMGPO[force_safe_mode] is set' " 'If psafe > PMSR[global_actual_pstate], the global_actual_pstate is forced.' " 'The value of Psafe needs to be at or below the nominal Pstate to make sure safe operation of all chiplets.'

Register Name	PRCCR0 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG 0
Address	00000000140F0165 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function.

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Bits	PCB	Field Mnemonic: Description
0	ROX	RESCLK_DIS: Resonant Clock Enable Master enable of all resonant clocking functions. This dial can be set by setting GP3(22) and can not be set in this PCBS_resonant_Clock_Control_Reg0. 1 = Resonant Clock function is disabled. Default values (0) for resclk_value, resclk_core_sync_value, csb_eco_sync_value 0 = Resonant Clock Control hardware is enabled (the mode is defined by dial resclk_control_mode)
1	RW	RESCLK_CONTROL_MODE: Resonant Clock Control Mode Defines the control means enabled when resclk_dis is not set. 0 = Pstate band hardware mechanism enabled 1 = Manual mode enabled (Firmware mode) If this bit is set to 0, the hardware control mechanism that manages the transition across the Resonant Bands is enabled. If this bit is set to 1, the automatic Pstate band hardware mechanism is disabled and the Firmware is in control of all values of the dial resclk_value, resclk_core_sync_value, csb_eco_sync_value. Firmware must ensure that frequency changes will not cross resonant bands or machine failures may result. resclk_value represents the values for clock sector buffer strength, inductor switch strength and high inductor enable. Firmware must ensure the correct stepping in/out the different bands and propagation of the values (resclk_value) to the core/eco (resclk_core_sync_value / csb_eco_sync_value).
2:4	RW	RESCLK_SYNC_PW: Resonant Clock Sync Pulse Width Number of nest/4 cycles to assert the clock sync signal. This value must be high enough to ensure capture and propagation across the asynchronous chiplet boundary.
5:11	RW	RES_SYNC_DELAY_CNT: Resonant Clock Sync Delay Number of nest/4 cycles wait after the launch of the resclk_value (csb and inductor) before launching the sync to allow these to be captured. This value must be high enough to ensure full propagation to the input of the clock sector buffers and inductor switches.
12:26	RW	RES_CSB_STR_INSTR_LO: Resonant Clock Sector Buffer Strength Instruction - Low Band Mask value that determines whether, during a fixed 15 step sequence, the res_csb_str(0:3) is to be decremented/incremented in entering/exiting the Low Band. During resonant clock Entry, res_csb_str(0:3) decremented by the value pattern from 0 down to 14. During resonant clock Exit, res_csb_str(0:3) incremented by the value pattern from 14 up to 0.
27:41	RW	RES_CSB_STR_INSTR_HI: Resonant Clock Sector Buffer Strength Instruction - High Band Mask value that determines whether, during a fixed 15 step sequence, the res_csb_str(0:3) is to be decremented/incremented in entering/exiting the High Band. During resonant clock Entry, res_csb_str(0:3) decremented by the value pattern from 0 down to 14. During resonant clock Exit, res_csb_str(0:3) incremented by the value pattern from 14 up to 0.

Register Name	PRCCR1 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG 1
Address	00000000140F0166 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function. Writes are conditioned.

Bits	PCB	Field Mnemonic: Description
0:7	RW	FULL_CSB_PS: Full Clock Sector Buffer Pstate Pstate defining the maximum point where the clock sector buffer must be driven to full strength. This allow clocks to be distributed at low Vmin levels. FW needs to make sure that no overlaps occur with bands 2 or 3.
8:15	RW	RES_LOW_LOWER_PS: Low Frequency Resonant Lower (LFRLow) Pstate Pstate defining the lower frequency of the Low Resonant Frequency Band. FW needs to make sure that no overlap occurs with band 0.



Bits	PCB	Field Mnemonic: Description
16:23	RW	RES_LOW_UPPER_PS: Low Frequency Resonant Upper (LFRUpper) Pstate Pstate defining the upper frequency of the Low Resonant Frequency Band. Note that if an overlap occurs with band 3, the hardware behavior is undefined.
24:31	RW	RES_HIGH_LOWER_PS: High Frequency Resonant Lower (HFRLow) Pstate Pstate defining the lower frequency of the High Resonant Frequency Band. Note that if an overlap occurs with band 2, the hardware behavior is undefined.
32:39	RW	RES_HIGH_UPPER_PS: High Frequency Resonant Upper (LFRUpper) Pstate Pstate defining the upper frequency of the High Resonant Frequency Band. This value needs to be greater or equal to high_res_lower_ps.
40:43	RW	NONRES_CSB_VALUE_TI: Clock Sector Buffer Table Index for non-resonant state Table Index into Clock Sector Buffer Table for the nominal, non-resonant state.
44:47	RW	FULL_CSB_VALUE_TI: Clock Sector Buffer Table Index for full CSB value Table Index into Clock Sector Buffer Table for the full CSB strength value.
48:56	RWX	RESCLK_VALUE: Output register driving the 9 bit resclk_value In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current resclk_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. The value in this register represents the following concatenation: csb_str_value(0:3) sw_str(0:3) hi_induct_en.
57	RWX	RESCLK_CORE_SYNC_VALUE: Output register driving the resclk_core_sync signal In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current resclk_core_sync_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. This bit is supposed to be used in order to create a SCOM-controlled pulse to force an update of the resclk propagation registers. A 1 enables the synchronous update, a 0 disables it. Suggested use of this bit is to set it to 1 and then set it back to 0 to create a (long) update pulse.
58	RWX	CSB_ECO_SYNC_VALUE: Output register driving the csb_eco_sync signal In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read only register to report the current csb_eco_sync_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. This bit is supposed to be used in order enable the ECO domain to participate in clock sector buffer strength changes, when switching from nominal strength to full CSB strength. A 1 enables the ECO domain, a 0 disables it from seeing a CSB strength update.

Register Name	PRCCR1 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_STATUS_REG
Address	00000000140F0167 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function.



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Bits	PCB	Field Mnemonic: Description
0	ROX	RESCLK_STATE: Resonant Clock State 0 = Resonant Clocking inactive 1 = Resonant Clocking active Valid if resclk_inprogress = 0. Hardware sets this bit to the right value at the completion of the transition into and out of resonance mode.

Bits	PCB	Field Mnemonic: Description
1	ROX	RES_HI_INDUCT_EN: Resonant High Inductor Enable Valid if resclk_inprogress = 0. This dial provides the current value being propagated. 0 = Resonant Clock mode not active 1 = Resonant Clock mode active
2	ROX	RESCLK_INPROGRESS: Resonant Clock Transition in Progress This bit is set by hardware while a transition is in progress and will be reset by hardware when the operation is complete.
3	ROX	RESCLK_FULL_CSB: Full CSB Clock State 0 = Full CSB Clocking inactive 1 = Full CSB Clocking active Valid if resclk_inprogress = 0. Hardware sets this bit to the right value at the completion of the transition into and out of full CSB mode respectively.

Register Name	<i>PLPFTCR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_CONTROL_REG
Address	00000000140F0168 (PCB)
Attributes	
Description	The PLPFTCR enables firmware to configure the modes that are used for the PCBS Local Pstate Frequency Target Status Register.

Bits	PCB	Field Mnemonic: Description
0:2	RW	DELAY_TIME: This field encodes the delay between the time a Local Actual Pstate change modifies the input to the DPLL and the time frequency acquisition begins to allow the hardware to ignore the frequency transition of the DPLL in order to get better frequency measurements. This field encodes a delay of ~1us to ~128us in power of 2 selects. The delay is defined by $2^{**}delay\_time$ in us. Note that the hardware uses multiples of the slow hang pulse that is running at 1us.
3	RW	RECORD_TRANSITIONS: This bit indicates whether the LPFTSR records events that correspond to Local Actual Pstate changes (and therefore may include DPLL slewing effects.) One usage model would set the periodic sample_time defined by the dial OHA_MODE_REG[tod_pulse_count_match_val] to a time less than the worst-case DPLL slew time but then ignore Pstate transitions because they might include DPLL slew effects.
4:18	RW	MULTIPLIER: This 15-bit unsigned constant is multiplied by the DPLL frequency code (9 bits) implied by the Local Actual Pstate to yield the 24-bit frequency target measured in PCBS-PM clock cycles (core clock / 2). Assuming times in seconds and frequencies in Hz, firmware should set this constant to: $(DPLL\_Frequency\_Code\_Step\_Hz * Sample\_Time\_Seconds) / 2$
19	RW	ENABLE_LPFT_FUNCTION: This is the enable bit to enable the local Pstate frequency target function. A '1' enables the function, a '0' disables it (the value can be changed at any time).

Register Name	<i>PLPFTSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_STATUS_REG
Address	00000000140F0169 (PCB)
Attributes	
Description	The PLPFTSR allows firmware to observe local actual Pstate realized frequencies.

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Bits	PCB	Field Mnemonic: Description
0	ROX_CLRPART	VALID: If this bit is set then all of the remaining fields of this register are valid. This bit is cleared whenever the register is read or after a local actual Pstate change occurs, and is will be set whenever the hardware completes a valid sample. If firmware reads this register and the valid bit is not set, then it indicates that the Local Pstate target frequency acquisition logic has not been able to complete a frequency acquisition for any Local Actual Pstate change since the last time the LPFTSR was read. This could be due to either of the following factors: 1. Firmware is sampling the LPFTSR faster than the time implied by the sample time defined in OHA by the dial OHA_MODE_REG[tod_pulse_count_match_val] field
1	ROX	CPM_DPLL: If the valid bit is set, then if cpm_dpll is set it indicates that the event recorded by this register was due to a Local Actual Pstate implemented by the DPLL running in CPM-DPLL mode, otherwise the value of this bit is undefined. If the valid bit is not set, this bit is undefined.
2	ROX	IVRM: If the valid bit is set, then if ivrm is set it indicates that the event recorded by this register was due to a Local Actual Pstate whose voltage was set locally by the iVRM operating entirely in regulation mode. If the valid bit is not set, this bit is undefined.
3	ROX	TRANSITION: If the valid bit is set, then if transition is set it indicates that during the observation period a Local Pstate Actual change has occurred, and any performance delta may be due to DPLL frequency slewing. If the valid bit is not set, this bit is undefined
4	ROX	STABLE: If stable is set it indicates that the DPLL input frequency has been stable since the last time the PLPFTSR was read. This bit is set whenever the PLPFTSR is read, and cleared whenever the Fmax input of the DPLL changes. This bit is always valid, regardless of the state of the valid bit. If the PLPFTSR is read on the same cycle a frequency changes then the stable bit is cleared. This bit helps firmware better understand how to interpret the information contained in the PLPFTSR. (Note that this bit should have an attribute ROX_SETPART, but this is not supported by regchk.)
5:28	ROX	DELTA: If the valid bit is set then this is the 24-bit signed difference Measured Cycles - Target Cycles for the event captured by this register. If the valid bit is not set, this dial is undefined.
29:52	ROX	CUMULATIVE: This field records the 24-bit cumulative (signed) delta for all valid samples taken since this field was cleared. Writing any value to this register clears this field. Note that it should have an attribute WOX_CLRPART, but this is not supported by regchk/figtree.
53:60	ROX	PSTATE: If the valid bit is set then this is the Local Actual Pstate of the frequency acquisition that had the minimum (signed) delta of any valid sample taken since the last time the LPFTSR was read. If the valid bit is not set, then this field is undefined.

Register Name	PFSMM1/2 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR1_REG
Address	00000000140F0170 (PCB)
Attributes	
Description	The PFSMM1/2 facilitates debug by providing insight into the internal FSM states of the PCB-slave power-management unit. For expert use only. Coding according to VHDL design.

Bits	PCB	Field Mnemonic: Description
0:6	ROX	BABYSTEP_MAIN_FSM: Main Babystep FSM (mfsm_lt)
7:11	ROX	BABYSTEP_SLAVE_FSM: Babystep Slave FSM (sfsm_lt)
12:16	ROX	CORE_RAILSTEPPER_MAIN_FSM: Main Core Railstepper FSM (mrsfsm_lt)
17:21	ROX	ECO_RAILSTEPPER_MAIN_FSM: Main ECO Railstepper FSM (mrsfsm_lt)



Bits	PCB	Field Mnemonic: Description
22:25	ROX	CORE_RAILSTEPPER_SUB_FSM: Core Railstepper Sub-FSM (srsfsm_lt)
26:29	ROX	ECO_RAILSTEPPER_SUB_FSM: ECO Railstepper Sub-FSM (srsfsm_lt)
30:34	ROX	CORE_RAILSTEPPER_BYP_FSM: Core Railstepper Bypass FSM (byp_fsm_lt)
35:39	ROX	ECO_RAILSTEPPER_BYP_FSM: ECO Railstepper Bypass FSM (byp_fsm_lt)
40:45	ROX	IVRM_CORE_VDD_SEQUENCER_FSM: Core iVRM Sequencer for Vdd (ivrm_fsm_lt)
46:51	ROX	IVRM_CORE_VCS_SEQUENCER_FSM: Core iVRM Sequencer for Vcs (ivrm_fsm_lt)
52:57	ROX	IVRM_ECO_VDD_SEQUENCER_FSM: ECO iVRM Sequencer for Vdd (ivrm_fsm_lt)
58:63	ROX	IVRM_ECO_VCS_SEQUENCER_FSM: ECO iVRM Sequencer for Vcs (ivrm_fsm_lt)

Register Name	<i>Refer To The Description Of PFSMM1.</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR2_REG
Address	00000000140F0171 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:6	ROX	RESCLK_BAND_FSM: Band Sequencer for resonant clocking (band_fsm_lt)
7:10	ROX	RESCLK_LOWRES_FSM: Low Resonant Clocking sequencer (lowres_fsm_lt)
11:14	ROX	RESCLK_HIGHRES_FSM: High Resonant Clocking sequencer (highres_fsm_lt)
15:18	ROX	RESCLK_FULLCSB_FSM: Full-CSB Resonant Clocking sequencer (fullcsb_fsm_lt)
19:22	ROX	RESCLK_UPDATE_FSM: Resonant Clocking Update sequencer (update_fsm_lt)
23:29	ROX	IDLE_TRANSITION_FSM: Idle State Sequence FSM (ifsm_lt)
30:37	ROX	Peco_step_target_uv Current ECO Step Target Pstate (different from Plocal_actual for undervolting)
38:45	ROX	Pcore_step_target_uv Current core Step Target Pstate (different from Plocal_actual for sleep and undervolting)

Register Name	<i>Protect Mode Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.PROTECT_MODE_REG
Address	00000000140F03FE (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	READ_PROTECT_ENABLE: Enable read protection
1	RW	WRITE_PROTECT_ENABLE: Enable write protection

Register Name	<i>Atomic Lock Register</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX04.TP_PCB_SLAVE_INST.ATOMIC_LOCK_REG	
Address	00000000140F03FF (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	RW	ATOMIC_LOCK_ENABLE: Enable atomic lock
1:4	ROX	ATOMIC_ID: Atomic ID

Register Name	<i>Contains The Slave's Primary Address</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.PRIMARY_ADDRESS_REG	
Address	00000000150F0000 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RO	Reserved field (Access type is primary_address)

Register Name	<i>Multicast Group 1</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.MULTICAST_GROUP_1	
Address	00000000150F0001 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST1_GROUP: multicast group1 setting

Register Name	<i>Multicast Group 2</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.MULTICAST_GROUP_2	
Address	00000000150F0002 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST2_GROUP: multicast group2 setting



Register Name	<i>Multicast Group 3</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.MULTICAST_GROUP_3	
Address	00000000150F0003 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST3_GROUP: multicast group3 setting

Register Name	<i>Multicast Group 4</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.MULTICAST_GROUP_4	
Address	00000000150F0004 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST4_GROUP: multicast group4 setting

Register Name	<i>Timeout Select Register</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.TIMEOUT_REG	
Address	00000000150F0010 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:1	RW	Reserved field (Access type is int_timeout)

Register Name	<i>Assist Interrupt Register</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.ASSIST_INTERRUPT_REG	
Address	00000000150F0011 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is attn)
1	ROX	Reserved field (Access type is recov)
2	ROX	Reserved field (Access type is xstop)

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Register Name	GP3 Register (NA In PERV CPLT)
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.GP3_REG
Address	00000000150F0012 (PCB) 00000000150F0013 (PCB1) 00000000150F0014 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset
2	RWX	RWX_WAND	RWX_WOR	GLSMUX_RESET: Glsmux reset for test purpose and stuck active mesh protection. Notice no clocks in the EX if this bit is set.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Put the DPLL in test mode.
4	RWX	RWX_WAND	RWX_WOR	PLL_RST: Put PLL in reset state.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYP: Enable PLL bypass.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pcb_access)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	PM_PI_DECODE: Test override for power management. EX chiplet only.
22	RWX	RWX_WAND	RWX_WOR	RESCLK_DIS: Resonant clocking disable.
23:25	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave will report 'Chiplet Offline'.
27	RWX	RWX_WAND	RWX_WOR	TP_LVLTRANS_FENCE: Electrical winkel fence. Mainly used by power management.
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.
29:31	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)



Register Name	<i>Skew Adjust Data</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.CLK_ADJ_REG	
Address	00000000150F0015 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:15	ROX	

Register Name	<i>Clk Ajust Config</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.CLK_ADJ_SET	
Address	00000000150F0016 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:31	RW	CLK_ADJ_SET_REG: Clk adj config

Register Name	<i>Vital Scan Out</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.VITAL_SCAN_OUT	
Address	00000000150F0017 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	

Register Name	<i>Chiplet Heartbeat Register</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.HEARTBEAT_REG	
Address	00000000150F0018 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	HEARTBEAT_DEAD: Chiplet heartbeat not detected

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Register Name	<i>Lock Indications From PLLs</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.PLL_LOCK_REG
Address	00000000150F0019 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	ROX	Reserved field (Access type is lock)

Register Name	<i>Attn Interrupt</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.ATTN_INTERRUPT_REG
Address	00000000150F001A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is attn)

Register Name	<i>Recov Interrupt</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.RECOV_INTERRUPT_REG
Address	00000000150F001B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is recov)

Register Name	<i>Xstop Interrupt</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.XSTOP_INTERRUPT_REG
Address	00000000150F001C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is xstop)

Register Name	<i>Slave Config Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.SLAVE_CONFIG_REG
Address	00000000150F001E (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	CFG_DISABLE_PERV_THOLD_CHECK: Disable pervasive thold check
1	RW	CFG_DISABLE_MALF_PULSE_GEN: Disable pulse generation for malf alert. Switch back to level
2	RW	CFG_STOP_HANG_CNT_SYS_XSTP: Disable hang counter stop for system xstop
3	RW	CFG_DISABLE_CL_ATOMIC_LOCK: Disable atomic lock for chiplet accesses
4	RW	CFG_DISABLE_HEARTBEAT: Disable check for voltage and gridclock in the chiplet
5	RW	CFG_ZERO_DATA: Sent zero data on any error
6:7	RW	
8:12	RW	ERROR_MASK: mask bits for slave error reporting
13:15	RW	

Register Name	<i>Error Capture Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.ERROR_REG
Address	00000000150F001F (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX_WCLEA R	CE_ERROR: Correctable error on pcb bus
1:3	RWX_WCLEA R	CHIPLET_ERRORS: Errors reported by chiplet 000 = no error 001 = XSCOM command blocked due pending errors 010 chiplet offline 011 partial good 100 invalid address / address error / bad access type 101 clock error 110 parity error / received unexpected packet / wrong packet number 111 timeout This register is for debug purposes only. It only holds meaningful data if it is cleared after each error.
4	RWX_WCLEA R	PARITY_ERROR: Parity error on PCB Interface
5	RWX_WCLEA R	DATA_BUFFER_ERROR: Parity error in data buffer
6	RWX_WCLEA R	ADDR_BUFFER_ERROR: Parity error in address buffer
7	RWX_WCLEA R	PCB_FSM_ERROR: Invalid state error in PCB FSM
8	RWX_WCLEA R	CL_FSM_ERROR: Invalid state error in Chiplet FSM
9	RWX_WCLEA R	INT_RX_FSM_ERROR: Invalid state error in interrupt RX FSM
10	RWX_WCLEA R	INT_TX_FSM_ERROR: Invalid state error in interrupt TX FSM

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Bits	PCB	Field Mnemonic: Description
11	RWX_WCLEAR	INT_TYPE_ERROR: Invalid interrupt type
12	RWX_WCLEAR	CL_DATA_ERROR: Parity error on Chiplet Interface
13	RWX_WCLEAR	INFO_ERROR: Parity error on Chiplet info lines
14	RWX_WCLEAR	UNUSED_0:
15	RWX_WCLEAR	CHIPLET_ATOMIC_LOCK_ERROR: Chiplet atomic lock error
16	RWX_WCLEAR	PCB_INTERFACE_ERROR: Error of pcb interface component for the internal endpoint
17	RWX_WCLEAR	CHIPLET_OFFLINE: Heartbeat check indicated that chiplet is offline
18	RWX_WCLEAR	CHIPLET_GRID_SKITTER: Heartbeat check indicated skitter on the chiplet grid
19	RWX_WCLEAR	GP3_REG_PARITY_ERROR: gp3 register parity bad
20	RWX_WCLEAR	ADDRESS_REG_PARITY_ERROR: address register parity bad
21	RWX_WCLEAR	TIMEOUT_REG_PARITY_ERROR: timeout select register parity bad
22	RWX_WCLEAR	CONFIG_REG_PARITY_ERROR: slave config register parity bad
23	RWX_WCLEAR	CLK_ADJ_REG_PARITY_ERROR: clk adj register parity bad
24	RWX_WCLEAR	DIV_REG_PARITY_ERROR: div register parity bad
25:28	RWX_WCLEAR	PLL_UNLOCK_ERROR: unlock from chiplet pll

Register Name		Hang Pulse Generation Register 0.
Mnemonic		EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.HANG_PULSE_0_REG
Address		00000000150F0020 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_0: Value of hang pulse 0. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_0: If set to '1', hang pulses are suppressed in case of a xstop



Register Name	<i>Hang Pulse Generation Register 1.</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.HANG_PULSE_1_REG	
Address	00000000150F0021 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_1: Value of hang pulse 1. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_1: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 2.</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.HANG_PULSE_2_REG	
Address	00000000150F0022 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_2: Value of hang pulse 2. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_2: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 3.</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.HANG_PULSE_3_REG	
Address	00000000150F0023 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_3: Value of hang pulse 3. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_3: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 4.</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.HANG_PULSE_4_REG	
Address	00000000150F0024 (PCB)	
Attributes		
Description		

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Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_4: Value of hang pulse 4. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_4: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 5</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.HANG_PULSE_5_REG
Address	00000000150F0025 (PCB)
Attributes	
Description	This hang counter is used exclusively to generate the malfunction alert pulse.

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_5: Value of hang pulse 5. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_5: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 6</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.HANG_PULSE_6_REG
Address	00000000150F0026 (PCB)
Attributes	
Description	This hang counter is exclusively used for heartbeat generation.

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_6: Value of hang pulse 6. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_6: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Divider For Hang Counter Clock</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.PRE_COUNTER_REG
Address	00000000150F0028 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PRE_COUNTER: Divider for hang counter clock. Divides clock by n+1 (default: n=0)



Register Name		<i>PowerManagement GP0</i>		
Mnemonic		EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PMGP0_REG		
Address		00000000150F0100 (PCB) 00000000150F0101 (PCB1) 00000000150F0102 (PCB2)		
Attributes				
Description				
Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PM_DISABLE: Master Switch for the PowerManagement Macro
1	RWX	WOX_AND	WOX_OR	PMGP0_SPARE_BIT1: spare bit
2	RWX	WOX_AND	WOX_OR	TP_TC_RESTART_CORE_DOMAIN: Kicks off small sequencer in OHA to get chiplet clocks back running for fast sleep without involving PORE. From GP-reg and overridden by PowMan State Machine.
3	RWX	WOX_AND	WOX_OR	DPLL_THOLD: Thold for the DPLL clock domain in the chiplet
4	RWX	WOX_AND	WOX_OR	PERV_THOLD: Thold for the Pervasive clock domain in the chiplet
5	RO	RO	RO	Reserved.
6	RO	RO	RO	Reserved.
7	RWX	WOX_AND	WOX_OR	PM_DPLL_TIMER_ENA: Select a timer instead of the DPLL lock bit for criteria to switch to DPLL. The time is defined by thold_timer_sel.
8	RWX	WOX_AND	WOX_OR	DPLL_LOCK_SENSE: DPLL lock sensitivity control (0=faster lock time, 1=slower lock time)
9	RWX	WOX_AND	WOX_OR	PMGP0_SPARE2: spare bit
10	RWX	WOX_AND	WOX_OR	DPLL_RESET: Reset to DPLL
11	RWX	WOX_AND	WOX_OR	PMGP0_SPARE_BIT11: Spare bit
12:19	RWX	WOX_AND	WOX_OR	DPLL_TESTOUT_CTL: DPLL testout control
20	RWX	WOX_AND	WOX_OR	TP_TC_CACHE2CORE_FENCE: Fence from cache to core domain in EX chiplet
21	RWX	WOX_AND	WOX_OR	TP_TC_CORE2CACHE_FENCE: Fence from core to cache domain in EX chiplet
22	RWX	WOX_AND	WOX_OR	TP_TC_PERVASIVE_ECO_FENCE: Pervasive ECO fence
23	RWX	WOX_AND	WOX_OR	CHKSW_HW257424_DISABLE: Chicken switch for interrupt retry exhausted bug (0=fix enabled, 1=fix disabled)
24:26	RWX	WOX_AND	WOX_OR	TP_CLK_ASYNC_RESET_DC: Clk async reset for three glitchless muxes, and the two clock dividers (bit 0 = master GLM, bit 1 = ECO Div2 and ECO GLM, bit 2= core Div1 and core GLM)
27:29	RWX	WOX_AND	WOX_OR	TP_CLKGLM_SEL_DC: Glitchless Mux Select for primary chiplet clock source (feeding both core and eco clock muxes) 000 = refclk, 001 = DPLL. 100 = Use constant selected by bit 34, else refclk
30	RWX	WOX_AND	WOX_OR	TP_CLKGLM_ECO_SEL_DC: Glitchless Mux Select for eco domain (cache_nclk) grid. 0= follow primary source chosen by previous field: 1 = Use constant selected by bit 34
31	ROX	NC	NC	SPECIAL_WKUP_DONE: Indicates that special wakeup is done, if asserted
32:33	RWX	WOX_AND	WOX_OR	TP_CLKGLM_CORE_SEL_DC: Glitchless Mux Select for core domain (nclk grid) mux. 0b00=primary GLS mux output, 0b10=constant input, 0b01=refclk. Valid transitions are 0b01 <-> 0b00 <-> 0b10, 0b11 is illegal

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
34	RWX	WOX_AND	WOX_OR	TP_CLKGLM_CONST_DC: Constant input available to all three ClkGlm
35:36	RWX	WOX_AND	WOX_OR	THOLD_TIMER_SEL: Selection for the thold transition timer in the IDLE state machine. 0b00=1024 cycles delay, 0b01=512 cycles delay, 0b10=256 cycles delay, 0b11= 128 cycles delay
37	RWX	WOX_AND	WOX_OR	BLOCK_ALL_WAKEUP_SOURCES: Setting this bit will make the PM Slave ignore any Wakeup events (ext. interrupt, malfunction alert, any special wakeup bit). This bit is intended to enable firmware concurrent patch capability. Note: This does NOT block the interrupt from being presented to the processor core. The following procedure is required on changes: 1. Firmware may only set this bit after first setting special wakeup and polling for special wakeup complete (OHA and PCB-slave both in running state with AISS and PM FSMs idle). 2. Firmware may only clear this bit if all special wakeup bits are first cleared.
38	RWX	WOX_AND	WOX_OR	TP_TC_DPLL_TESTMODE_DC: ADPLL test mode
39	RWX	WOX_AND	WOX_OR	PM_SLV_WINKLE_FENCE: Fence off the powered off chiplet in winkle. - Logical fence/hold for pcb_slave and pcb_slave_pm. For electrical fence see bit 23.
40	RWX	WOX_AND	WOX_OR	L3_ENABLE_SWITCH: Setting this bit activates l3_edram_enable if allowed by system configuration GP3(28). Resetting this bit deactivates l3_edram_enable.
41	RWX	WOX_AND	WOX_OR	TP_CPLT_IVRM_REFBYPASS_DC: Signal to iVRM (used to be controlled by scan-only block inside EX, but needs to be driven by VIO domain)
42	RWX	WOX_AND	WOX_OR	CHKSW_HW241939_DISABLE: if this bit is set to 1, the fix for HW241939 (pfet enable SCOM-ability) is disabled
43	RWX	WOX_AND	WOX_OR	CHKSW_HW273115_DISABLE: if this bit is set to 1, the fix for HW273115 (Pga ACK noack issue when the babystepper is in the winkle state) is disabled
44	RWX	WOX_AND	WOX_OR	CHKSW_HW245103_DISABLE: if this bit is set to 1, the fix for HW245103 resonant clocking CSB and SW -bit ordering change is disabled
45	RWX	WOX_AND	WOX_OR	CHKSW_HW257534_DISABLE: if this bit is set to 1, the fix for HW257534 (fencing of errors) is disabled
46	RWX	WOX_AND	WOX_OR	CHKSW_HW259509_ENABLE: if this bit is set to 0, the fix for HW259509 (Pstate change hanging, because of DPLL flock timer in a hung state) is disabled
47	RWX	WOX_AND	WOX_OR	CHKSW_HW260345_DISABLE: if set to 1, this bit disables the HW260345 fix (fix was to make sure that we enter bypass mode for iVRM safe mode without a glitch that could cause Vcs in regulation and Vdd in bypass)
48:49	ROX	NC	NC	WAKEUP_INT_TYPE: (Known to be unreliable and not supported, informational usage only) Type of the last wakeup event that caused an exit from sleep or winkle (excluding nap!), regardless of present state. 0b01: External interrupt. 0b10: Malfunction Alert. 0b11: Special Wakeup. 0b00: chiplet has never fully entered and exited a chiplet-level idle state since IPL of the system. (Note this does not necessarily get updated when the processor core enters an idle state, only if the PCB-Slave enters and then exits the idle state for this chiplet).
50	ROX	NC	NC	DPLL_LOCK: DPLL lock indicator
51	ROX	NC	NC	SPECIAL_WKUP_ALL_SOURCES_ORED: logical OR of all special wakeup sources
52	ROX	NC	NC	REGULAR_WKUP_AVAILABLE: logical OR of external interrupt and malfunction alert



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
53	RWX	WOX_AND	WOX_OR	BLOCK_REG_WKUP_SOURCES: blocks ext. int. and malf. Alert from waking up PCBS (no block possible for PC!)

Register Name	PowerManagement GP1
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PMGP1_REG
Address	00000000150F0103 (PCB) 00000000150F0104 (PCB1) 00000000150F0105 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	SLEEP_POWER_DOWN_EN: Sleep Power Down Enable: When set to 1, causes hardware to automatically reduce voltage to the Core domain when entering Sleep mode. The voltage value for power down is chosen by sleep_power_off_sel (bit 2). When set to 0, a request is sent to the PORE engine for assistance entering Sleep.
1	RWX	WOX_AND	WOX_OR	SLEEP_POWER_UP_EN: Sleep Power Up Enable: When set to 1, enables automated hardware restoration of voltage via PFETs and, if enabled, iVRMs when exiting Sleep mode. If this bit is set to 0 the hardware rely on external means (PORE or equivalent) to restore voltage.
2	RWX	WOX_AND	WOX_OR	SLEEP_POWER_OFF_SEL: Sleep Power Off Select: Selects which voltage level to place the Core domain PFETs upon Sleep entry. 0 = Vret (Fast Sleep Mode), 1 = Voff (Deep Sleep Mode). Depending on the setting of pmicr_latency_en, this bit is controlled with a PCB-write (0) or by the PMICR in the core (1).
3	RWX	WOX_AND	WOX_OR	WINKLE_POWER_DOWN_EN: Winkle Power Down Enable: When set to 1, causes hardware to automatically reduce voltage to the entire Chiplet (both Core and ECO Domains) when entering Winkle mode. The voltage value for power down is chosen by winkle_power_off_sel (bit 5). When set to 0, a request is sent to the PORE engine for assistance entering Winkle.
4	RWX	WOX_AND	WOX_OR	WINKLE_POWER_UP_EN: Winkle Power Up Enable: When set to 1, enables automated hardware PFET enablement when exiting Winkle mode. If this bit is set to 0 the hardware rely on external means (PORE or equivalent) to cause the PFETs to be re-enabled.
5	RWX	WOX_AND	WOX_OR	WINKLE_POWER_OFF_SEL: Winkle Power Off Select: Selects which voltage level to place the Core and ECO domain PFETs upon Winkle entry. 0 = Vret (Fast Winkle Mode), 1 = Voff (Deep Winkle Mode). Depending on the setting of pmicr_latency_en, this bit is controlled with a PCB-write (0) or by the PMICR in the core (1).
6	RWX	WOX_AND	WOX_OR	OHA_WKUP_OVERRIDE_EN: Needs to be 0 for normal operation. If set to 1, the two following dials are used to override the regular and special wakeup signal from PCBS to OHA
7	RWX	WOX_AND	WOX_OR	OHA_PM_WKUP_OVERRIDE: Enablement by 'oha_wkup_override_en' forces the regular wakeup signal to OHA to the value of this bit regardless of presence of an interrupt source.
8	RWX	WOX_AND	WOX_OR	OHA_SPC_WKUP_OVERRIDE: Enablement by 'oha_wkup_override_en' forces the special wakeup signal to OHA to the value of this bit, regardless of the firmware settings.

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
9	RWX	WOX_AND	WOX_OR	ENDP_RESET_PM_ONLY: If asserted, an endpoint reset of all power management-related functions (not the regular PCB slave) is performed. Intended usage is for recovery.
10	RWX	WOX_AND	WOX_OR	DPLL_FREQ_OVERRIDE_ENABLE: override Fmax/Fmin only, if '1', using register FREQ_CTRL_REG
11	RWX	WOX_AND	WOX_OR	PM_SPR_OVERRIDE_EN: PM SPR Override Enable The PPMCR (0xNNNN) and PPMICR (0XXXXX) accesses the register resources that make up the PMCR SPR used by hypervisor to management Pstates. Thus, PCB updates to it are disabled in hardware to prevent collisions. This bit allows ownership of the PMCR to be switched from hypervisor to OCC. This switch is immediate in hardware, thus, firmware must ensure the ownership switch is otherwise communicated. 0 = Disables the writing of the PPMCR (0xNNNN) from the PCB and allows SPR 884 writes (mtspr) to update the register resource. 1 = Enables the writing of the PPMCR (0xNNNN) from the PCB.
12	RWX	WOX_AND	WOX_OR	FORCE_SAFE_MODE: Force Safe Mode 0 = Allow other enabled features to determine the operational Pstate. 1 = Forces the minimum of POHBR[psafe] and PPMSR[global_pstate_actual] Pstate for the core chiplet as the operational frequency.
13	RWX	WOX_AND	WOX_OR	IVRM_SAFE_MODE_EN: Internal VRM Safe Mode Enable 0 = Disable the iVRM safe mode, thus, no automatic actions occur, if an iVRM error happens. 1 = if the iVRMs are enabled (PIVRMCSR[ivrm_en] is set) and Pstates are enabled and if the error defined by dial pcbs_ivrm_gross_or_fine_err occurs, then the railstepper is forced into bypass mode to prevent a voltage-frequency hazard
14	RWX	WOX_AND	WOX_OR	IVRM_SAFE_MODE_FORCE_ACTIVE: Internal VRM Safe Mode Force Dial 0 = the hardware decides whether to activate the iVRM safe mode or not 1 = the iVRM safe mode is forced regardless (this makes only sense if ivrm_fsm_enable=1 and Pstates are enabled)
15	RWX	WOX_AND	WOX_OR	PMICR_LATENCY_EN: Selects how the sleep/winkle latency (which is deep/fast) is controlled. If asserted the PMICR controls the winkle/sleep_power_off_sel in PMGP1, otherwise those bits are controlled via SCOM by OCC.
16	RWX	WOX_AND	WOX_OR	ENABLE_OCC_CTRL_FOR_LOCAL_PSTATE_EFF_REQ: controls, if the HW (for value 0) or OCC (value 1) is in control of the Local Pstate Effective register in PPSTR
17	RWX	WOX_AND	WOX_OR	SERIALIZE_PFET_POWERDOWN: if asserted, the pFET sequencer will sequence the core and the ECO domain one after the other when powering down
18	RWX	WOX_AND	WOX_OR	SERIALIZE_PFET_POWERUP: if asserted, the pFET sequencer will sequence the ECO and the core domain one after the other when powering up
19	RWX	WOX_AND	WOX_OR	DISABLE_FORCE_DEEP_TO_FAST_SLEEP: 0: (normal operation) - If PCB Slave reports a recoverable error or a checkstop, a DEEP sleep operation is forced to FAST. The entries in sleep/winkle_power_off_sel remain unchanged. 1: force to FAST is disabled.



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
20	RWX	WOX_AND	WOX_OR	DISABLE_FORCE_DEEP_TO_FAST_WINKLE: 0: (normal operation) - If PCB Slave reports a recoverable error or a checkstop, a DEEP winkle operation is forced to FAST. The entries in sleep/winkle_power_off_sel remain unchanged. 1: force to FAST is disabled.

Register Name	PFET Control/Status Register For Core And ECO Vdd
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PFVDDCNTLSTAT_REG
Address	00000000150F0106 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	CORE_VDD_PFET_FORCE_STATE: Core Domain PFET Force State Provides a means for firmware to force the core domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 4:5 = 00 (both core_vdd_pfet_val_override AND core_vdd_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
2:3	RW	ECO_VDD_PFET_FORCE_STATE: ECO Domain PFET Force State Provides a means for firmware to force the ECO domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 6:7 = 00 (both eco_vdd_pfet_val_override AND eco_vdd_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
4	RW	CORE_VDD_PFET_VAL_OVERRIDE: Core Domain PFET Value Override 0 = Override is disabled
5	RW	CORE_VDD_PFET_SEL_OVERRIDE: Core Domain PFET Stage Select Override 0 = Override is disabled
6	RW	ECO_VDD_PFET_VAL_OVERRIDE: ECO Domain PFET Value Override 0 = Override is disabled
7	RW	ECO_VDD_PFET_SEL_OVERRIDE: ECO Domain PFET Stage Select Override 0 = Override is disabled
8	RW	CORE_VDD_PFET_ENABLE_REGULATION_FINGER: Core Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the core_vdd_pfet_enable_value.
9	RW	ECO_VDD_PFET_ENABLE_REGULATION_FINGER: ECO Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the eco_vdd_pfet_enable_value.

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Bits	PCB	Field Mnemonic: Description
10:21	RW	CORE_VDD_PFET_ENABLE_VALUE: Core PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the Core Domain PFET Enables directly. If core_vdd_pfet_val_override = 1, a write to this field sets the state of the core PFET Enables until core_vdd_pfet_val_override is cleared. If core_vdd_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the core_vdd_pfet_valN_slac registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
22:25	RW	CORE_VDD_PFET_SEL_VALUE: Core PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure core_vdd_pfet_valN_slac(0:11) where N is 0 to 11 if core_vdd_pfet_sel_override = 1. If core_vdd_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
26:37	RW	ECO_VDD_PFET_ENABLE_VALUE: ECO PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the ECO PFET Enables directly. If ECO_vdd_pfet_val_override = 1, a write to this field sets the state of the ECO PFET Enables until ECO_vdd_pfet_val_override is cleared. If eco_vdd_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the eco_vdd_pfet_valN_slac registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
38:41	RW	ECO_VDD_PFET_SEL_VALUE: ECO PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure eco_vdd_pfet_valN_slac(0:11) where N is 0 to 11 if eco_vdd_pfet_sel_override = 1. If eco_vdd_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
42:45	ROX	CORE_VDD_PG_STATE: Core power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
46:49	ROX	CORE_VDD_PG_SEL: For debug, contains the actual index n into Core Domain PFET Value [n] SLAT Register set that contains the Core PFET Enable Value currently enabled.
50:53	ROX	ECO_VDD_PG_STATE: ECO Domain power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
54:57	ROX	ECO_VDD_PG_SEL: For debug, contains the actual index n into ECO Domain PFET Value [n] SLAT Register set that contains the ECO PFET Enable Value currently enabled.

Register Name	PFET Sense Register	
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PFSENSE_REG	
Address	00000000150F0107 (PCB)	
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:11	ROX	TP_CORE_VDD_PFET_ENABLE_SENSE: Not used any more.
12:23	ROX	TP_ECO_VDD_PFET_ENABLE_SENSE: Not used any more.



Bits	PCB	Field Mnemonic: Description
24:35	ROX	TP_CORE_VCS_PFET_ENABLE_SENSE: Not used any more.
36:47	ROX	TP_ECO_VCS_PFET_ENABLE_SENSE: Not used any more.

Register Name	<i>PM Error Summary Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PMERRSUM_REG
Address	00000000150F0108 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	PM_ERROR: PM Error is present. Intended for use by special PCB multicast to see error state of all chiplets with a single read (via 510F0108 to read all chiplets)

Register Name	<i>PM Error Register:</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PMERR_REG
Address	00000000150F0109 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_HANG_ERR: Hang during Unassisted Sleep Entry: SLEEP_ENTRY_NOTIFY_PMC state
1	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ASSIST_HANG_ERR: Hang during Assisted Sleep Entry: SLEEP_ENTRY_NOTIFY_PMC_ASSIST state
2	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ERR: Hang during Unassisted Sleep Exit: SLEEP_EXIT_NOTIFY_PMC state
3	ROX	PCBS_SLEEP_EXIT_INVOKE_PORE_ERR: Hang during Assisted Deep Sleep Exit: SLEEP_EXIT_INVOKE_PORE state
4	ROX	PCBS_WINKLE_ENTRY_NOTIFY_PMC_ERR: Hang during Unassisted Winkle Entry: WINKLE_ENTRY_NOTIFY_PMC state
5	ROX	PCBS_WINKLE_ENTRY_SEND_INT_ASSIST_ERR: Hang during Assisted Winkle Entry: WINKLE_ENTRY_SEND_INT_ASSIST state
6	ROX	PCBS_WINKLE_EXIT_NOTIFY_PMC_ERR: Hang during Unassisted Winkle Exit: WINKLE_EXIT_NOTIFY_PMC state
7	ROX	PCBS_WAIT_DPLL_LOCK_ERR: Hang during Unassisted Exit waiting on DPLL: WAIT_DPLL_LOCK state
8	ROX	PCBS_SPARE8_ERR: spare bit, always 0
9	ROX	PCBS_WINKLE_EXIT_SEND_INT_ASSIST_ERR: Hang during Assisted Winkle Exit: WINKLE_EXIT_SEND_INT_ASSIST state
10	ROX	PCBS_WINKLE_EXIT_SEND_INT_POWUP_ASSIST_ERR: Hang during Assisted Winkle Exit: WINKLE_EXIT_SEND_INT_POWUP_ASSIST state
11	ROX	PCBS_WRITE_FSM_GOTO_REG_IN_INVALID_STATE_ERR: write to FSM goto register in invalid state
12	ROX	PCBS_WRITE_PMGP0_IN_INVALID_STATE_ERR: write to PMGP0 in invalid state

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Bits	PCB	Field Mnemonic: Description
13	ROX	PCBS_FREQ_OVERFLOW_IN_PSTATE_MODE_ERR: frequency of DPLL in Pstate mode overflows (Fnom + desired Pstate > 511)
14	ROX	PCBS_ECO_RS_BYPASS_CONFUSION_ERR: ECO railstepper tried to exit Vcs bypass and enter Vdd bypass in one Pstate step (it is not clear, in which order this strange operation should be performed - most likely it should never happen to avoid that Vcs is greater than Vdd)
15	ROX	PCBS_CORE_RS_BYPASS_CONFUSION_ERR: same as previous error, but for core railstepper (it is not clear, in which order this strange operation should be performed - most likely it should never happen to avoid that Vcs is greater than Vdd)
16	ROX	PCBS_READ_LPST_IN_PSTATE_MODE_ERR: read LPST-array while iVRM FSMs are enabled (dial ivrm_fsm_enable asserted)
17	ROX	PCBS_LPST_READ_CORR_ERR: correctable error occurred when reading the LPST
18	ROX	PCBS_LPST_READ_UNCORR_ERR: uncorrectable error occurred when reading the LPST
19	ROX	PCBS_PFET_STRENGTH_OVERFLOW_ERR: overflow occurred when calculating the pFET strength (in final rounding step!)
20	ROX	PCBS_VDS_LOOKUP_ERR: Vds entry not found in lookup table (when performing the linear search!)
21	ROX	PCBS_IDLE_INTERRUPT_TIMEOUT_ERR: idle interrupt timeout in PCB interrupt controller
22	ROX	PCBS_PSTATE_INTERRUPT_TIMEOUT_ERR: PState interrupt timeout in PCB interrupt controller
23	ROX	PCBS_GLOBAL_ACTUAL_SYNC_INTERRUPT_TIMEOUT_ERR: GlobalActualSync Interrupt timeout in PCB interrupt controller
24	ROX	PCBS_PMAX_SYNC_INTERRUPT_TIMEOUT_ERR: PmaxSync Interrupt timeout in PCB interrupt controller
25	ROX	PCBS_GLOBAL_ACTUAL_PSTATE_PROTOCOL_ERR: a write to global actual Pstate register has occurred before the global actual Pstate interrupt has left PCBS
26	ROX	PCBS_PMAX_PROTOCOL_ERR: a write to the Pmax/Pmin register has occurred before the Pmax sync interrupt has left PCB
27	ROX	PCBS_IVRM_GROSS_OR_FINE_ERR: iVRM gross or fine error (details to be found in PCBS_ivrm_Control_Status_Reg)
28	ROX	PCBS_IVRM_RANGE_ERR: iVRM range error (summary bit, details to be found in PCBS_ivrm_Control_Status_Reg)
29	ROX	PCBS_DPLL_CPM_FMIN_ERR: DPLL CPM Fmin error
30	ROX	PCBS_DPLL_DCO_FULL_ERR: DPLL DCO full
31	ROX	PCBS_DPLL_DCO_EMPTY_ERR: DPLL DCO empty
32	ROX	PCBS_DPLL_INT_ERR: DPLL internal error
33	ROX	PCBS_FMIN_AND_NOT_CPMBIT_ERR: dpll_fmin_and_not_cpmbit (ref. to dial cpm_fmin_clip_error_sel on how to configure this)
34	ROX	PCBS_DPLL_FASTER_THAN_FMAX_PLUS_DELTA1_ERR: dpll_faster_than_fmax_plus_delta1 (for characterization, delta1 is configurable with pll_char_delta1)
35	ROX	PCBS_DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2_ERR: dpll_slower_than_fmin_minus_delta2 (for characterization, delta2 is configurable with pll_char_delta2)
36	ROX	PCBS_RESCLK_CSB_INSTR_VECTOR_CHG_IN_INVALID_STATE_ERR: RESCLK CSB instruction vector change while FSMs none idle
37	ROX	PCBS_RESCLK_BAND_BOUNDARY_CHG_IN_INVALID_STATE_ERR: RESCLK Band boundaries change while FSMs none idle
38	ROX	PCBS_OCC_HEARTBEAT_LOSS_ERR: OCC heartbeat loss
39	ROX	PCBS_SPARE39_ERR: spare bit, always 0
40	ROX	PCBS_SPARE40_ERR: spare bit, always 0



Bits	PCB	Field Mnemonic: Description
41	ROX	PCBS_SPARE41_ERR: spare bit, always 0
42	ROX	PCBS_SPARE42_ERR: spare bit, always 0

Register Name	<i>PM Error Mask Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PMERRMASK_REG
Address	00000000150F010A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_HANG_ERR_MASK: Mask for this error: 1=masked, 0=not masked
1	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ASSIST_HANG_ERR_MASK: Mask for this error: 1=masked, 0=not masked
2	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
3	RW	PCBS_SLEEP_EXIT_INVOKE_PORE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
4	RW	PCBS_WINKLE_ENTRY_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
5	RW	PCBS_WINKLE_ENTRY_SEND_INT_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
6	RW	PCBS_WINKLE_EXIT_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
7	RW	PCBS_WAIT_DPLL_LOCK_ERR_MASK: Mask for this error: 1=masked, 0=not masked
8	RW	PCBS_SPARE8_ERR_MASK: Mask for this error: 1=masked, 0=not masked
9	RW	PCBS_WINKLE_EXIT_SEND_INT_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
10	RW	PCBS_WINKLE_EXIT_SEND_INT_POWUP_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
11	RW	PCBS_WRITE_FSM_GOTO_REG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
12	RW	PCBS_WRITE_PMGPO_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
13	RW	PCBS_FREQ_OVERFLOW_IN_PSTATE_MODE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
14	RW	PCBS_ECO_RS_BYPASS_CONFUSION_ERR_MASK: Mask for this error: 1=masked, 0=not masked
15	RW	PCBS_CORE_RS_BYPASS_CONFUSION_ERR_MASK: Mask for this error: 1=masked, 0=not masked
16	RW	PCBS_READ_LPST_IN_PSTATE_MODE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
17	RW	PCBS_LPST_READ_CORR_ERR_MASK: Mask for this error: 1=masked, 0=not masked
18	RW	PCBS_LPST_READ_UNCORR_ERR_MASK: Mask for this error: 1=masked, 0=not masked
19	RW	PCBS_PFET_STRENGTH_OVERFLOW_ERR_MASK: Mask for this error: 1=masked, 0=not masked
20	RW	PCBS_VDS_LOOKUP_ERR_MASK: Mask for this error: 1=masked, 0=not masked
21	RW	PCBS_IDLE_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
22	RW	PCBS_PSTATE_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
23	RW	PCBS_GLOBAL_ACTUAL_SYNC_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
24	RW	PCBS_PMAX_SYNC_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked

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Bits	PCB	Field Mnemonic: Description
25	RW	PCBS_GLOBAL_ACTUAL_PSTATE_PROTOCOL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
26	RW	PCBS_PMAX_PROTOCOL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
27	RW	PCBS_IVRM_GROSS_OR_FINE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
28	RW	PCBS_IVRM_RANGE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
29	RW	PCBS_DPLL_CPM_FMIN_ERR_MASK: Mask for this error: 1=masked, 0=not masked
30	RW	PCBS_DPLL_DCO_FULL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
31	RW	PCBS_DPLL_DCO_EMPTY_ERR_MASK: Mask for this error: 1=masked, 0=not masked
32	RW	PCBS_DPLL_INT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
33	RW	PCBS_FMIN_AND_NOT_CPMBIT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
34	RW	PCBS_DPLL_FASTER_THAN_FMAX_PLUS_DELTA1_ERR_MASK: Mask for this error: 1=masked, 0=not masked
35	RW	PCBS_DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2_ERR_MASK: Mask for this error: 1=masked, 0=not masked
36	RW	PCBS_RESCLK_CSB_INSTR_VECTOR_CHG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
37	RW	PCBS_RESCLK_BAND_BOUNDARY_CHG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
38	RW	PCBS_OCC_HEARTBEAT_LOSS_ERR_MASK: Mask for this error: 1=masked, 0=not masked
39	RW	PCBS_SPARE39_ERR_MASK: Mask for this error: 1=masked, 0=not masked
40	RW	PCBS_SPARE40_ERR_MASK: Mask for this error: 1=masked, 0=not masked
41	RW	PCBS_SPARE41_ERR_MASK: Mask for this error: 1=masked, 0=not masked
42	RW	PCBS_SPARE42_ERR_MASK: Mask for this error: 1=masked, 0=not masked

Register Name		PM Special Wakeup FSP
Mnemonic		EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PMSPCWKUPFSP_REG
Address		00000000150F010B (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RW	FSP_SPECIAL_WAKEUP: Chiplet Special Wakeup for FSP Firmware use. NOTE: protocol is required when setting this bit

Register Name		PM Special Wakeup OCC
Mnemonic		EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PMSPCWKUPOCC_REG
Address		00000000150F010C (PCB)
Attributes		
Description		



Bits	PCB	Field Mnemonic: Description
0	RW	OCC_SPECIAL_WAKEUP: Chiplet Special Wakeup for OCC Firmware use. NOTE: protocol is required when setting this bit

Register Name	<i>PM Special Wakeup Hypervisor</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PMSPCWKUPPHYP_REG
Address	00000000150F010D (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	PHYP_SPECIAL_WAKEUP: Chiplet Special Wakeup for hypervisor Firmware use. NOTE: protocol is required when setting this bit

Register Name	<i>PFET Control/Status Register For Core And ECO Vcs</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PFVCSCTLSTAT_REG
Address	00000000150F010E (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	CORE_VCS_PFET_FORCE_STATE: Core Domain PFET Force State Provides a means for firmware to force the core domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 4:5 = 00 (both core_vcs_pfet_val_override AND core_vcs_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
2:3	RW	ECO_VCS_PFET_FORCE_STATE: ECO Domain PFET Force State Provides a means for firmware to force the ECO domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 6:7 = 00 (both eco_vcs_pfet_val_override AND eco_vcs_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
4	RW	CORE_VCS_PFET_VAL_OVERRIDE: Core Domain PFET Value Override 0 = Override is disabled
5	RW	CORE_VCS_PFET_SEL_OVERRIDE: Core Domain PFET Stage Select Override 0 = Override is disabled
6	RW	ECO_VCS_PFET_VAL_OVERRIDE: ECO Domain PFET Value Override 0 = Override is disabled
7	RW	ECO_VCS_PFET_SEL_OVERRIDE: ECO Domain PFET Stage Select Override 0 = Override is disabled

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Bits	PCB	Field Mnemonic: Description
8	RW	CORE_VCS_PFET_ENABLE_REGULATION_FINGER: Core Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the core_vcs_pfet_enable_value.
9	RW	ECO_VCS_PFET_ENABLE_REGULATION_FINGER: ECO Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the eco_vcs_pfet_enable_value.
10:21	RW	CORE_VCS_PFET_ENABLE_VALUE: Core PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the Core Domain PFET Enables directly. If core_vcs_pfet_val_override = 1, a write to this field sets the state of the core PFET Enables until core_vcs_pfet_val_override is cleared. If core_vcs_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the core_vcs_pfet_valN_slav registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
22:25	RW	CORE_VCS_PFET_SEL_VALUE: Core PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure core_vcs_pfet_valN_slav(0:11) where N is 0 to 11 if core_vcs_pfet_sel_override = 1. If core_vcs_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
26:37	RW	ECO_VCS_PFET_ENABLE_VALUE: ECO PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the ECO PFET Enables directly. If ECO_vcs_pfet_val_override = 1, a write to this field sets the state of the ECO PFET Enables until ECO_vcs_pfet_val_override is cleared. If eco_vcs_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the eco_vcs_pfet_valN_slav registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
38:41	RW	ECO_VCS_PFET_SEL_VALUE: ECO PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure eco_vcs_pfet_valN_slav(0:11) where N is 0 to 11 if eco_vcs_pfet_sel_override = 1. If eco_vcs_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
42:45	ROX	CORE_VCS_PG_STATE: Core power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
46:49	ROX	CORE_VCS_PG_SEL: For debug, contains the actual index n into Core Domain PFET Value [n] SLAT Register set that contains the Core PFET Enable Value currently enabled.
50:53	ROX	ECO_VCS_PG_STATE: ECO Domain power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
54:57	ROX	ECO_VCS_PG_SEL: For debug, contains the actual index n into ECO Domain PFET Value [n] SLAT Register set that contains the ECO PFET Enable Value currently enabled.



Register Name	<i>PM State History Register For Hypervisor</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPHYP_REG
Address	00000000150F0110 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	PHYP_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPART	PHYP_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPART	PHYP_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPART	PHYP_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPART	PHYP_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPART	PHYP_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For FSP</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PMSTATEHISTFSP_REG
Address	00000000150F0111 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	FSP_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPART	FSP_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPART	FSP_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPART	FSP_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.

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Bits	PCB	Field Mnemonic: Description
6	ROX_CLRPAR T	FSP_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	FSP_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For OCC</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PMSTATEHISTOCC_REG
Address	00000000150F0112 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	OCC_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	OCC_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	OCC_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	OCC_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	OCC_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	OCC_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For PerfMon</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPERF_REG
Address	00000000150F0113 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	PERF_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	PERF_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	PERF_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	PERF_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	PERF_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	PERF_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM FSM Reset And Babystepper Idle Injects</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.IDLEFSMGOTOCMD_REG
Address	00000000150F0114 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	WO_1P	idle_fsm_goto_cmd ' A write to this reg will proceed the IDLE FSM from WAIT_FOR_PORE_DONE, SLEEP_EXIT_WAIT_FOR_PORE_FAST_EXIT_DONE, or WINKLE_EXIT_WAIT_FOR_PORE_FAST_EXIT_DONE to the following states: ' 0b01: goto IDLE state ' 0b10: goto SLEEP_EXIT_CORE_MESHLET_ON state ' 0b11: goto WINKLE_EXIT_NOTIFY_PMC state ' "
2	RWX	babystp_trigger_sleep_entry ' A write to this reg with a 1 in this field will cause the babystepper to run the sleep entry sequence. This step is needed for an assisted entry into sleep, before the power is actually turned off since the babystepper needs to know about the sleep state. For an unassisted entry, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished entering its sleep mode. ' "
3	RWX	babystp_trigger_winkle_entry ' A write to this reg with a 1 in this field will cause the babystepper to run the winkle entry sequence. This step is needed for an assisted entry into winkle before the power is actually turned off since the babystepper needs to know about the winkle state. For an unassisted entry, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished entering its winkle mode. ' "
4	RWX	babystp_trigger_wakeup ' A write to this reg with a 1 in this field will cause the babystepper to run the wakeup sequence from sleep/winkle depending on the babystepper state of sleep or winkle. This step is needed for an assisted exit from winkle before the power is actually turned off since the babystepper needs to know about the wakeup state. For an unassisted exit, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished waking up from sleep or winkle. ' "

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Register Name	Core PFET Power Up Delay
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.COREPFPUDLY_REG
Address	00000000150F012C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_POWUP_DLY0: Delay used after transitioning to Core Domain power up sequence stage0. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	CORE_POWUP_DLY1: Delay used after transitioning to Core domain power up sequence stage1.
8:19	RW	CORE_POWER_UP_DELAY_SEL: Vector select for which delay to use for the respective power-up stage. Bit mapping: 8 -> core_*_pfet_enable(0) 9 -> core_*_pfet_enable(1) ... 19 -> core_*_pfet_enable(11) Bit meaning: 0 = Use core_powup_dly0 1 = Use core_powup_dly1

Register Name	Core PFET Power Down Delay
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.COREPFPDDLY_REG
Address	00000000150F012D (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_POWDN_DLY0: Delay used after transitioning to Core domain power dn sequence stage1. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	CORE_POWDN_DLY1: Delay used after transitioning to Core domain power dn sequence stage1. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
8:19	RW	CORE_POWER_DN_DELAY_SEL: Vector select for which delay to use for the respective power-dn stage. Bit mapping: 8 -> core_*_pfet_enable(0) 9 -> core_*_pfet_enable(1) ... 19 -> core_*_pfet_enable(11) Bit meaning: 0 = Use core_powdn_dly0 1 = Use core_powdn_dly1



Register Name	Core PFET Vretention	
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.COREPFVRET_REG	
Address	00000000150F0130 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_VRET_SEL: Pointer to the stage representing the Vretention value for the core PFETs. Power down sequences will stop after enabling this stage.
4:7	RW	CORE_VOFF_SEL: Pointer to the stage representing the Voff value for the core PFETs. Power down sequences will stop after enabling this stage.

Register Name	ECO PFET Power Up Delay	
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.ECOPFPUDLY_REG	
Address	00000000150F014C (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_POWUP_DLY0: Delay used after transitioning to ECO domain power up sequence stage0 in terms of refclk period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	ECO_POWUP_DLY1: Delay used after transitioning to ECO domain power up sequence stage1.
8:19	RW	ECO_POWER_UP_DELAY_SEL: Vector select for which delay to use for the respective power-up stage. Bit mapping: 8 -> eco_*_pfet_enable(0) 9 -> eco_*_pfet_enable(1) ... 19 -> eco_*_pfet_enable(11) Bit meaning: 0 = Use eco_powup_dly0 1 = Use eco_powup_dly1

Register Name	ECO PFET Power Down Delay	
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.ECOPFPDDLY_REG	
Address	00000000150F014D (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_POWDN_DLY0: UNUSED/SPARE
4:7	RW	ECO_POWDN_DLY1: Delay used after transitioning to ECO Domain power dn sequence stage1. The delays in this register are in terms of refclk period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.

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Bits	PCB	Field Mnemonic: Description
8:19	RW	ECO_POWER_DN_DELAY_SEL: Vector select for which delay to use for the respective power-down stage. Bit mapping: 8 -> eco_*_pfet_enable(0) 9 -> eco_*_pfet_enable(1) ... 19 -> eco_*_pfet_enable(11) Bit meaning: 0 = Use eco_powdn_dly0 1 = Use eco_powdn_dly1

Register Name		ECO PFET Vretention
Mnemonic		EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.ECOPFVRET_REG
Address		00000000150F0150 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_VRET_SEL: Pointer to the stage representing the Vretention value for the ECO PFETs. Power down sequences will stop after enabling this stage.
4:7	RW	ECO_VOFF_SEL: Pointer to the stage representing the Voff value for the ECO PFETs. Power down sequences will stop after enabling this stage.

Register Name		Frequency Control Register With Overrides For DPLL
Mnemonic		EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.FREQ_CTRL_REG
Address		00000000150F0151 (PCB)
Attributes		
Description		Note that overrides to Dpll_fmax are only applied if Dpll_freq_override_enable = 1. A read of all these dials always returns the currently established DPLL frequencies (regardless of any other mode settings).
Bits	PCB	Field Mnemonic: Description
0:8	RWX	DPLL_FMIN: minimum DPLL frequency in CPM-DPLL mode that is set at IPL time A read always returns the currently established value A write is not conditioned on any other dial setting.
9:17	RWX	DPLL_FMAX: DPLL maximum frequency and frequin (these two values are the same in POWER8 processor) without applying bias values: A read always returns the currently established value A write is conditioned on the setting of dpll_freq_override_enable. If dpll_freq_override_enable is asserted, a write causes this field to update. Otherwise the hardware (that is, PStates) are controlling the update of this value.
18:21	RO	Reserved.
22:30	RW	FREQU_AT_PSTATE0: DPLL frequency for Pstate 0



Register Name	<i>DPLL Mode Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.DPLL_CPM_PARM_REG
Address	00000000150F0152 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	LF_SLEWRATEXPI: out of lock slew rate for DPLL
8	RW	LF_USE_CPMXPI: use CPM instead of PFD as loop filter input, if '1' (instead of using both)
9	RW	FF_USE_CPMXPI: use the CPM inputs for the frequency filter, if '1'
10	RW	CPM_FILTER_ENABLE: enables the CPM filter
11	RW	FF_BYPASSXPI: enables frequency filter bypass
12	RW	DCO_OVERRIDE: enables overrides for DCO testing/characterization
13	RW	DCO_INCR: enables increment for DCO testing/characterization, increments only on a rising edge
14	RW	DCO_DECR: enables decrement for DCO testing/characterization, decrements only on a rising edge
15:23	RW	DPLL_LOCK_TIMER_REPLACEMENT_VALUE: if dpll_lock_replacement_timer_mode_en is set, this dial specifies the delay in us, after which it is assumed, that the DPLL has reached a frequency lock condition. Note that values less than 3 will cause in undefined HW behavior (0 will cause HANGs!). if dpll_lock_replacement_timer_mode_en is zero, this dial specifies the delay in pcb_nclk cycles after which the hardware monitors the DPLL frequout output (if dpll_freqout_mode_en is set) or the DPLL flock output (if dpll_flock_mode_en is set). Note that in this case, the value of this dial needs to be greater or equal to 150 (decimal).
24:31	RW	PRE_VRET_PSTATE: Pstate that is stepped to before switching to Vretention defined in PCBS_iVRM_Control_Status_Reg
32	RW	OVERRIDE_PCBS_DPLL_SYNCHRONIZER: Bypasses the 'ping-pong' synchronization logic between the DPLL and the PCBS-PM. NEVER SET TO 1 UNLESS YOU KNOW WHAT YOU ARE DOING!
33:36	RW	DPLL_CHAR_DELTA1: Delta in DPLL ticks for characterization (cf. dial dpll_faster_than_fmax_plus_delta1)
37:40	RW	DPLL_CHAR_DELTA2: Delta in DPLL ticks for characterization (cf. dial dpll_faster_than_fmin_minus_delta2)

Register Name	<i>PPMSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_STATUS_REG
Address	00000000150F0153 (PCB)
Attributes	
Description	The PPMSR provides read access to the power management status that is also shadowed to the PC and visible to the hypervisor in the PMSR (with some delay due to the shadowing process).

Bits	PCB	Field Mnemonic: Description
0:7	ROX	global_pstate_actual ' Actual Global Pstate Pstate or Pglobal_actual' " Reads from this field return the presently established global PState value.' " "Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent '

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Bits	PCB	Field Mnemonic: Description
8:15	ROX	LOCAL_PSTATE_ACTUAL: ' Actual Local PState or Plocal_actual' " 'Reads from this field return the presently established local PState value. This value will always be less than or equal to global_pstate_actual.' " 'Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent' "
16:23	ROX	pv_min Minimum Pstate set by the platform.
24:31	ROX	pvf_max Maximum Pstate set by the platform.
32	ROX	spr_em_disabled ' SPR Energy Management Disabled' 'Read from this field indicate whether the platform has disabled the ' 'PMCR and PMICR SPRs to control the chiplet PState. '
33	ROX	Psafe_mode_active Read from this field indicate whether the chiplet has been put into a safe mode with Psafe enabled to a OCC heartbeat loss or other externally forced reasons (0=regular mode, 1=safe mode is active)
34	ROX	iVRM_safe_mode_active Read from this field indicate whether the chiplet has been put the iVRM safe mode (forcing the bypass mode for all iVRMs)
35	ROX	ivrm_enable Read from this field indicate whether the chiplet internal voltage regulation macro is enabled for localized voltage control (0=disabled, 1=enabled) based on ANDing the poweron signals to the iVRMs
36	ROX	all_fsms_in_safe_state For recovery: if this bit is asserted, all Pstate and iVRM control FSMs are in a stable, safe state that allows the recovery routine to proceed with resetting the PCBS PM without the risk of interrupt a critical action
37:40	ROX	pmsr_spares spare bits

Register Name	<i>PIVRMCSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_CONTROL_STATUS_REG
Address	00000000150F0154 (PCB)
Attributes	
Description	The PIVRMCSR provides access to chiplet-level controls of the internal VRM rail set (VDD and VCS) across both the core and ECO domains. The following is valid only for bits 4 to 7: when in automatic iVRM mode (ivrm_fsm_enable=1), these bits provide access to the values established by the automatic hardware mechanism. When In iVRM override mode (ivrm_fsm_enable=0), these bits allow firmware direct control of the values driving the internal VRMs.

Bits	PCB	Field Mnemonic: Description
0	RW	IVRM_FSM_ENABLE: Internal master VRM FSM Enable 0 = Disable Internal VRM FSMs and enable to control the iVRMs with the available override registers (SCOMable) as a backup mode or for setup (override mode) 1 = Enable Internal VRM FSM sequencers (requires that Pstates are enabled with enable_Pstate_mode=1 as well) (automatic mode)
1	RW	USE_IVRM_FOR_VRET: Internal VRM Enabled for Vretention 0 = Disable Internal VRM for Vretention 1 = Enable Internal VRM for Vretention
2	RW	BINSEARCH_CAL_ENA: trigger binary search (level signal)

Bits	PCB	Field Mnemonic: Description
3	RW	PVREF_EN: Internal VRM Power Voltage Reference Forced Enable 0 = Allow hardware to enable/disable pvref circuit 1 = Force enablement of the pvref circuit
4	RWX	IVRM_CORE_VDD_BYPASS_B: Internal VRM Core VDD Bypass (negative active) 0 = VDD Internal Core VRMs in bypass 1 = VDD internal Core VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
5	RWX	IVRM_CORE_VDD_POWERON: Internal VRM Core VDD Poweron 0 = Core VDD Internal VRMs powered off 1 = Core VDD internal VRMs powered on if this bit is not set (=0), the Core VDD internal VRM powered off internally. If this bit is set (=1), the Core VDD internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
6	RWX	IVRM_CORE_VCS_BYPASS_B: Internal VRM Core VCS Bypass (negative active) 0 = VCS Internal Core VRMs in bypass 1 = VCS internal Core VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VCS internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VCS internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
7	RWX	IVRM_CORE_VCS_POWERON: Internal VRM Core VCS Poweron 0 = Core VCS Internal VRMs powered off 1 = Core VCS internal VRMs powered on if this bit is not set (=0), the Core VCS internal VRM powered off internally. If this bit is set (=1), the Core VCS internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
8	RWX	IVRM_ECO_VDD_BYPASS_B: Internal VRM ECO VDD Bypass (negative active) 0 = VDD Internal ECO VRMs in bypass 1 = VDD internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
9	RWX	IVRM_ECO_VDD_POWERON: Internal VRM ECO VDD Bypass (negative active) 0 = VDD Internal ECO VRMs in bypass 1 = VDD internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.

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Bits	PCB	Field Mnemonic: Description
10	RWX	IVRM_ECO_VCS_BYPASS_B: Internal VRM ECO VCS Bypass (negative active) 0 = VCS Internal ECO VRMs in bypass 1 = VCS internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VCS internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VCS internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
11	RWX	IVRM_ECO_VCS_POWERON: Internal VRM ECO VCS Poweron 0 = ECO VCS Internal VRMs powered off 1 = ECO VCS internal VRMs powered on if this bit is not set (=0), the ECO VCS internal VRM powered off internally. If this bit is set (=1), the ECO VCS internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
12:18	RWX	IVRM_VRET_VDD: if use_ivrm_for_Vret is asserted, this dial is used to control the Vdd retention voltage. Note: this field will establish the Core VDD rail for Sleep and both the Core and ECO rail for Winkle. - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
19:25	RWX	IVRM_VRET_VCS: if use_ivrm_for_Vret is asserted, this dial is used to control the Vcs retention voltage. Note: this field will establish the Core VDD rail for Sleep and both the Core and ECO rail for Winkle. - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
26:30	RWX	IVRM_VRET_CORE_VDD_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the Core Vdd iVRM PFET strength for the retention voltage
31:35	RWX	IVRM_VRET_CORE_VCS_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the Core Vcs iVRM PFET strength for the retention voltage
36:40	RWX	IVRM_VRET_ECO_VDD_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the ECO Vdd iVRM PFET strength for the retention voltage
41:45	RWX	IVRM_VRET_ECO_VCS_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the ECO Vcs iVRM PFET strength for the retention voltage
46	RW	PVREF_FAIL: voltage reference fail input to iVRMs
47	ROX	IVRM_PREF_ERROR_GROSS: Voltage Reference Gross Error 0 = Gross Error not detected 1 = Gross Error detected
48	ROX	IVRM_PREF_ERROR_FINE: Voltage Reference Fine Error 0 = Fine Error not detected 1 = Fine Error detected
49	ROX	IVRM_CORE_VDD_RANGE_HI: Core VDD Internal VRM Range Hi Indicator 0 = Core VDD Internal VRM Hi indicator signal not asserted 1 = Core VDD internal VRMs Hi indicator signal asserted
50	ROX	IVRM_CORE_VDD_RANGE_LO: Core VDD Internal VRM Range Low Indicator 0 = Core VDD Internal VRM Low indicator signal not asserted 1 = Core VDD internal VRMs Low indicator signal asserted

Bits	PCB	Field Mnemonic: Description
51	ROX	IVRM_ECO_VDD_RANGE_HI: ECO VDD Internal VRM Range Hi Indicator 0 = ECO VDD Internal VRM Hi indicator signal not asserted 1 = ECO VDD internal VRMs Hi indicator signal asserted
52	ROX	IVRM_ECO_VDD_RANGE_LO: ECO VDD Internal VRM Range Low Indicator 0 = ECO VDD Internal VRM Low indicator signal not asserted 1 = ECO VDD internal VRMs Low indicator signal asserted
53	ROX	IVRM_CORE_VCS_RANGE_HI: Core VCS Internal VRM Range Hi Indicator 0 = Core VCS Internal VRM Hi indicator signal not asserted 1 = Core VCS internal VRMs Hi indicator signal asserted
54	ROX	IVRM_CORE_VCS_RANGE_LO: Core VCS Internal VRM Range Low Indicator 0 = Core VCS Internal VRM Low indicator signal not asserted 1 = Core VCS internal VRMs Low indicator signal asserted
55	ROX	IVRM_ECO_VCS_RANGE_HI: ECO VCS Internal VRM Range Hi Indicator 0 = ECO VCS Internal VRM Hi indicator signal not asserted 1 = ECO VCS internal VRMs Hi indicator signal asserted
56	ROX	IVRM_ECO_VCS_RANGE_LO: ECO VCS Internal VRM Range Low Indicator 0 = ECO VCS Internal VRM Low indicator signal not asserted 1 = ECO VCS internal VRMs Low indicator signal asserted
57	ROX	BINSEARCH_CAL_DONE: binary search done signal
58	RWX	IVRM_CORE_VDD_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
59	RWX	IVRM_CORE_VCS_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
60	RWX	IVRM_ECO_VDD_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
61	RWX	IVRM_ECO_VCS_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
62	RW	IVRM_POWER_DOWN_DISABLE: If this bit is 1, the iVRM poweron signal is left asserted. Power off of the iVRMs is then blocked

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Register Name		<i>PIVRMVSR Register</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VALUE_SETTING_REG
Address		00000000150F0155 (PCB)
Attributes		
Description		The PIVRMVSR allows access to VID values and PFET strength valid signal settings presented to the internal VRM rail set (VDD and VCS) across both the core and ECO domains. When in <code>ivrm_fsm_enable = "auto"</code> mode, this register provides access to the values established by the automatic hardware mechanism. When <code>ivrm_fsm_enable = "override"</code> mode, this register allows firmware direct control of the values driving the internal VRMs which, if the VRMs are not in bypass, will move the voltage settings.
Bits	PCB	Field Mnemonic: Description
0:7	RWX	IVRM_CORE_VDD_IVID: When read, returns the value presently being driving to the Core VDD iVRM. If <code>ivrm_fsm_enable = 0</code> (<code>override_mode</code>), then writes to this field will drive a new VID value to the Core VDD iVRM. If <code>ivrm_fsm_enable = 1</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
8:15	RWX	IVRM_CORE_VCS_IVID: When read, returns the value presently being driving to the Core VCS iVRM. If <code>ivrm_fsm_enable = 0</code> (<code>override_mode</code>), then writes to this field will drive a new VID value to the Core VCS iVRM. If <code>ivrm_fsm_enable = 1</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
16:23	RWX	IVRM_ECO_VDD_IVID: When read, returns the value presently being driving to the Core VDD iVRM. If <code>ivrm_fsm_enable = 0</code> (<code>override_mode</code>), then writes to this field will drive a new VID value to the ECO VDD iVRM. If <code>ivrm_fsm_enable = 1</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
24:31	RWX	IVRM_ECO_VCS_IVID: When read, returns the value presently being driving to the ECO VCS iVRM. If <code>ivrm_fsm_enable = 0</code> (<code>override_mode</code>), then writes to this field will drive a new VID value to the ECO VCS iVRM, If <code>ivrm_fsm_enable = 0</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
32:36	RWX	IVRM_CORE_VDD_PFET_STRENGTH: When read, returns the value presently being driving to the core VCS iVRM. If <code>ivrm_fsm_enable = 0</code> (<code>override_mode</code>), then writes to this field will drive a new strength value to the core VCS iVRM, If <code>ivrm_fsm_enable = 0</code> , writes to this field are not performed.

Bits	PCB	Field Mnemonic: Description
37:41	RWX	IVRM_CORE_VCS_PFET_STRENGTH: This register is assigned to the signals tcex##_tp_ivrm_core_vcs_sense & tcex##_tp_ivrm_core_vdd_sense & tcex##_tp_ivrm_eco_vcs_sense & tcex##_tp_ivrm_eco_vdd_sense & 0b0 Note that all other sense signals are spares now and tied to 0. OUTDATED TEXT: When read, returns the value presently being driving to the core VDD iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the core VDD iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
42:46	RWX	IVRM_ECO_VDD_PFET_STRENGTH: When read, returns the value presently being driving to the ECO VCS iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the ECO VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
47:51	RWX	IVRM_ECO_VCS_PFET_STRENGTH: When read, returns the value presently being driving to the ECO VDD iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the ECO VDD iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
52	RWX	IVRM_VDD_CORE_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the Core VDD iVRM. If ivrm_fsm_enable = 1 AND ivrm_control_mode = 1 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the Core VDD iVRM, If ivrm_fsm_enable = 0 OR ivrm_control_mode = 0, writes to this field are not performed.
53	RWX	IVRM_VCS_CORE_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the Core VCS iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the Core VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
54	RWX	IVRM_VDD_ECO_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the ECO VDD iVRM. If ivrm_fsm_enable = 1 AND ivrm_control_mode = 1 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the ECO VDD iVRM, If ivrm_fsm_enable = 0 OR ivrm_control_mode = 0, writes to this field are not performed.
55	RWX	IVRM_VCS_ECO_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the ECO VCS iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the ECO VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
56	RWX	CORE_VDD_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
57	RWX	CORE_VCS_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
58	RWX	ECO_VDD_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
59	RWX	ECO_VCS_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.

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Register Name		General PCBS Modes And Chicken Switches
Mnemonic		EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBSPM_MODE_REG
Address		00000000150F0156 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RW	ENABLE_PSTATE_MODE: if asserted, Pstate requests (from overrides or PMCR) will be honored, otherwise, the hardware does not do anything. Note to firmware: this is the master switch for Pstates and should be asserted after all sub-modes (that is, lvrn_fsm_en) are setup to avoid enabling unintentional modes during the mode setup.
1	RW	GLOBAL_PSTATE_CHANGE_FOR_IDLE_STATE_ENABLED: if asserted, a global Pstate change to the Nap/Sleep/Winkle-Pstate is requested, when the Nap/Sleep/Winkle state is entered and the individual enable bits in the PIMCR are asserted
2	RW	ENABLE_GLOBAL_PSTATE_REQ: if '1' then enable PMC interrupt with global Pstate change request, otherwise, disable global requests
3	RW	ENABLE_WINKLE_WITH_CPM_MODE: if '1', PCBS automatically changes the DPLL mode to mode 1, when entering winkle, but changes the mode back to CPM mode when exiting. Needed for CPM-DPLL control loop enablement.
4	RW	ENABLE_CLIPPING_OF_GLOBAL_PSTATE_REQ: if '1', PCBS automatically clips global Pstate requests with Pvf_max in PPMBR and sets the 'donate' bit in the interrupt accordingly
5	RW	CHKSW_HW214553: if deasserted, HW214553 (frequin issue in resclk mode) is fixed, if asserted, the fix is not active
6	RW	ENABLE_PMC_PMAX_SYNC_NOTIFICATION: if asserted, the PCBS-PM will send a 'Pmax_sync' interrupt, once the synchronization criterion is met
7	RW	DPLL_LOCK_REPLACEMENT_TIMER_MODE_EN: Select a timer instead of the DPLL lock bit as target frequency reached criterion. This timer has to be setup by the dial dpll_lock_timer_replacement_value. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
8	RW	DPLL_FREQOUT_MODE_EN: Looks at the DPLL frequout to find out, if the target frequency has been reached. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
9	RW	DPLL_FLOCK_MODE_EN: Looks at the real DPLL flock output to find out, if the target frequency has been reached. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
10	RW	ENABLE_SENSE_DELAY_CHARACTERIZATION: If this switch is 0, the sense latches are updated every cycle. If this switch is 1, the sense delay measurement mode is enabled, that starts a sense delay timer, whenever one of the registers that drive the inputs of the iVRMs/pFETs is written via PCB and that triggers a sense register freeze operation, when the sense delay timer reaches the value sense_delay_timer_val. With this mode, the sense delays can be measured in multiples of the PCB-slave clock speed.
11:17	RW	SENSE_DELAY_TIMER_VAL: See the description of enable_sense_delay_characterization for details.
18:19	RW	CPM_FMIN_CLIP_ERROR_SEL: This dial selects, which of the following conditions will cause the FIR bit dpll_fmin_and_not_cpmbit to be set to detect, that the DPLL runs at Fmin, but is still clipped by the CPMs. 0b00 = function is disabled 0b01 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit2 = 0 0b10 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit1 = 0 0b11 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit0 = 0
20:23	RW	DBG_TRACE_SEL: This dial selects the group of signals to be traced for debug in the lab. Details to be found in the Section 'Trace Bus'

Bits	PCB	Field Mnemonic: Description
24:25	RW	TRACE_DATA_SEL: This dial selects the group of signals to be traced for debug in the lab. Details to be found in the Section 'Trace Bus'
26:29	RW	TP_CPLT_IVRM_VPP_TUNE: Tune bits to be set going to the iVRMs

Register Name	<i>PIVRMPS Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_PFETSTR_SENSE_REG
Address	00000000150F0157 (PCB)
Attributes	
Description	This PIVRMPS is used to check that the pFET sense outputs correspond to the driven values (mainly for test).

Bits	PCB	Field Mnemonic: Description
0:4	ROX	IVRM_CORE_VDD_PFETSTR_SNS: Not used any more.
5:9	ROX	IVRM_CORE_VCS_PFETSTR_SNS: This register is assigned to the signals tcex##_tp_ivrm_core_vcs_sense & tcex##_tp_ivrm_core_vdd_sense & tcex##_tp_ivrm_eco_vcs_sense & tcex##_tp_ivrm_eco_vdd_sense & 0b0
10:14	ROX	IVRM_ECO_VDD_PFETSTR_SNS: Not used any more.
15:19	ROX	IVRM_ECO_VCS_PFETSTR_SNS: Not used any more.
20	ROX	IVRM_VDD_CORE_PFETSTR_VALID_SNS: Not used any more.
21	ROX	IVRM_VCS_CORE_PFETSTR_VALID_SNS: Not used any more.
22	ROX	IVRM_VDD_ECO_PFETSTR_VALID_SNS: Not used any more.
23	ROX	IVRM_VCS_ECO_PFETSTR_VALID_SNS: Not used any more.
24	ROX	CORE_VDD_BYPASS_B_SENSE: Not used any more.
25	ROX	CORE_VCS_BYPASS_B_SENSE: Not used any more.
26	ROX	ECO_VDD_BYPASS_B_SENSE: Not used any more.
27	ROX	ECO_VCS_BYPASS_B_SENSE: Not used any more.
28	ROX	CORE_VDD_POWERON_SENSE: Not used any more.
29	ROX	CORE_VCS_POWERON_SENSE: Not used any more.
30	ROX	ECO_VDD_POWERON_SENSE: Not used any more.
31	ROX	ECO_VCS_POWERON_SENSE: Not used any more.
32	ROX	CORE_VDD_VPUMP_EN_SENSE: Not used any more.
33	ROX	CORE_VCS_VPUMP_EN_SENSE: Not used any more.
34	ROX	ECO_VDD_VPUMP_EN_SENSE: Not used any more.
35	ROX	ECO_VCS_VPUMP_EN_SENSE: Not used any more.
36	ROX	CORE_VDD_PFET_LOW_VOUT_SNS: Not used any more.
37	ROX	CORE_VCS_PFET_LOW_VOUT_SNS: Not used any more.
38	ROX	ECO_VDD_PFET_LOW_VOUT_SNS: Not used any more.
39	ROX	ECO_VCS_PFET_LOW_VOUT_SNS: Not used any more.

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Register Name	PPMICR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_IDLE_CONTROL_REG
Address	00000000150F0158 (PCB)
Attributes	
Description	The PPMICR is used to read the PMICR register typically owned (written) by the hypervisor. Writes are conditioned on the setting of the dial Pm_spr_override_en. If Pm_spr_override_en is set, firmware needs to make sure that the special wakeup state of this chiplet is reached before changing any of the latency fields in this register. Otherwise, the hardware behavior is undefined.

Bits	PCB	Field Mnemonic: Description
0:7	ROX	NAP_PSTATE_REQ: Nap Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
8	ROX	NAP_PSTATE_EN: Nap PState Enable 1 = Enable the Nap Pstate (NPS) Request, Nap Global Enable and Nap Latency functions 0 = Disables the Nap Pstate (NPS) Request, Nap Global Enable and Nap Latency functions Reads from the field return the value last written.
9	ROX	NAP_GLOBAL_EN: Nap Global Enable 1 = Upon the execution of a Nap instruction , the Nap Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a Nap instruction , the Nap Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.
10:11	ROX	NAP_LATENCY: Nap Latency not supported for POWER8 processor
12:15	ROX	RESERVED_PPMICR_0: reserved
16:23	ROX	SLEEP_PSTATE_REQ: sleep Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
24	ROX	SLEEP_PSTATE_EN: sleep PState Enable 1 = Enable the sleep Pstate (NPS) Request, sleep Global Enable and sleep Latency functions 0 = Disables the sleep Pstate (NPS) Request, sleep Global Enable and sleep Latency functions Reads from the field return the value last written.
25	ROX	SLEEP_GLOBAL_EN: sleep Global Enable 1 = Upon the execution of a sleep instruction , the sleep Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a sleep instruction , the sleep Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.

Bits	PCB	Field Mnemonic: Description
26:27	ROX	SLEEP_LATENCY: sleep Latency 00 = Cease instructions and honors Pstate change but does not perform additional state changing actions (unsupported in POWER8, maps to 0b10) 01 = Indicates to the platform that a sub-state that would have the lowest latency is enabled (unsupported in POWER8, maps to 0b10) 10 = Indicates to the platform that a sub-state that might have a medium exit latency is enabled (POWER8: Fast Sleep) 11 = Indicates to the platform that a sub-state that might have higher exit latency is enabled (POWER8: Deep Sleep)
28:31	ROX	RESERVED_PPMICR_1: reserved
32:39	ROX	WINKLE_PSTATE_REQ: winkle Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
40	ROX	WINKLE_PSTATE_EN: winkle PState Enable 1 = Enable the winkle Pstate (NPS) Request, winkle Global Enable and winkle Latency functions 0 = Disables the winkle Pstate (NPS) Request, winkle Global Enable and winkle Latency functions Reads from the field return the value last written.
41	ROX	WINKLE_GLOBAL_EN: winkle Global Enable 1 = Upon the execution of a winkle instruction , the winkle Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a winkle instruction , the winkle Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.
42:43	ROX	WINKLE_LATENCY: winkle Latency 00 = Cease instructions and honors Pstate change but does not perform additional state changing actions (unsupported in POWER8, maps to 0b10) 01 = Indicates to the platform that a sub-state that would have the lowest latency is enabled (unsupported in POWER8, maps to 0b10) 10 = Indicates to the platform that a sub-state that might have a medium exit latency is enabled (POWER8: Fast Winkle) 11 = Indicates to the platform that a sub-state that might have higher exit latency is enabled (POWER8: Deep Winkle)
44:47	ROX	RESERVED_PPMICR_2: reserved

Register Name	PPMCR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_CONTROL_REG
Address	00000000150F0159 (PCB)
Attributes	
Description	The PPMCR provides read access to the PMCR register shadow in the PCBS typically owned (written) by the hypervisor. Writes are conditioned on the setting of PMGP1[pm_spr_override_en].

Bits	PCB	Field Mnemonic: Description
0:7	RWX	GLOBAL_PSTATE_REQ: global Pstate request from hypervisor (or OCC)
8:15	RWX	LOCAL_PSTATE_REQ: local Pstate request from hypervisor or OCC
16	RWX	AUTO_OVERRIDE0_PSTATE_LIMIT_EN: automatic override Pstate 0 (for low activity detection) is enabled, if asserted



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Bits	PCB	Field Mnemonic: Description
17	RWX	AUTO_OVERRIDE1_PSTATE_LIMIT_EN: automatic override Pstate 1 (reserved for future use) is enabled, if asserted
18:23	RWX	RESERVED_PPMCR: reserved
24:31	RWX	AUTO_OVERRIDE_PSTATE0: automatic override Pstate 0 (for low activity detection)
32:39	RWX	AUTO_OVERRIDE_PSTATE1: automatic override Pstate 1 (reserved for future use)

Register Name	<i>Control Register That Is Written By PMC Sequencer</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_PMC_VF_CTRL_REG
Address	00000000150F015A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PGLOBAL_ACTUAL: global actual Pstate
8:15	RW	MAXREGVCS: maximum regulation point for Vcs, Bit 0 is reserved, bits 1 to 7 are in iVID format
16:23	RW	MAXREGVDD: maximum regulation point for Vdd, Bit 0 is reserved, bits 1 to 7 are in iVID format
24:31	RW	EVIDVCS_EFF: eff. external voltage ID for Vcs in iVID format, Bit 0 is reserved
32:39	RW	EVIDVDD_EFF: eff. external voltage ID for Vdd in iVID format, Bit 0 is reserved

Register Name	<i>Undervolting Register For PCBS</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_UNDERVOLTING_REG
Address	00000000150F015B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PUV_MIN: minimum Pstate for which undervolting is allowed
8:15	RW	PUV_MAX: maximum Pstate for which undervolting is allowed
16:21	RW	KUV: this value indicates how many Pstate ticks a voltage request is undervolted (clipped with Puv_min). Note that the Kuv value is signed

Register Name	<i>PPSIBR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_INDEX_BOUND_REG
Address	00000000150F015C (PCB)
Attributes	
Description	The PPSIBR enables setting the minimum and maximum Pstate that is supported as a pointer into the local Pstate table (which has entries from 0 to 127).

Bits	PCB	Field Mnemonic: Description
0:7	RW	LPSI_MIN: this Pstate index is the index that corresponds to array entry 0. Note that the index domain is obtained by adding 128 to a Pstate, thus, the value is unsigned.
8:14	RW	LPSI_ENTRIES_MINUS_1: this dial contains the value of the number of entries in the Pstate table minus 1

Register Name	<i>PPMBR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_BOUNDS_REG
Address	00000000150F015D (PCB)
Attributes	
Description	The PPMBR enables setting the Pstate bounds that are managed by the OCC. If dial Enable_pmc_pmax_sync_notification is set, firmware must wait after each write to this register until PMC has received the Pmax Sync Interrupt. If a write happens to this register while the previously scheduled Pmax Sync Interrupt has not yet left the PCBS, the error TBD will be set.

Bits	PCB	Field Mnemonic: Description
0:7	RW	PMIN_CLIP: minimum Pstate allowed for this chiplet
8:15	RW	PMAX_CLIP: maximum Pstate allowed for this chiplet (has to be greater or equal to Pmin_clip)

Register Name	<i>PPTCR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_CTRL_REG
Address	00000000150F015E (PCB)
Attributes	
Description	The PPTCR controls the address for writing the local Pstate Table Array (all 96 words are accessible). Note that the protocol requires this register to be set up with the Pstate address first, if a read or a write of the Pstate array is intended, to make sure that the initial address is set correctly. The register PPTR must always be written or read afterward. Note that any access to the PPTR auto-increments this register.

Bits	PCB	Field Mnemonic: Description
0:6	RWX	PSTATE_TABLE_ADDRESS: This is the address of the Pstate table in PCBS, which is auto-incremented after any access to the PTLR.

Register Name	<i>PPTR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_REG
Address	00000000150F015F (PCB)
Attributes	
Description	The PPTR controls the data to be written into the Pstate table and returns the data for a read of the Pstate table. Note that the protocol requires for a write to set this register up after first setting up PPTCR (if the user does not rely on the auto-increment function of the address). For a read of the Pstate table, this register must be read after first setting up PPTCR as well (again if the auto-increment feature of the address is not used). Any access to this register auto-increments the Pstate_table_address by 1. Note also that the read functionality of this register is only functional if PIVRMCSR[ivrm_fsm_enable] = 0. The write functionality works in any case.

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Bits	PCB	Field Mnemonic: Description
0:63	RW	pstate_data This is the field for data bits 0 to 63

Register Name	PPSTR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_STEP_TARGET_REG
Address	00000000150F0160 (PCB)
Attributes	
Description	The PPSTR provides read access to several intermediate values in the Pstate computation pipeline. Writes Are conditioned on the setting of PMGPO[enable_OCC_ctrl_for_local_Pstate_eff_req].

Bits	PCB	Field Mnemonic: Description
0:7	RWX	LOCAL_PSTATE_EFF_REQ: this field represents the effective local Pstate request right before the clipping with Pmin and Pmax if enable_OCC_ctrl_for_local_Pstate_eff_req=0 then the hardware controls this dial, that updates every cycle if enable_OCC_ctrl_for_local_Pstate_eff_req=1 then OCC is in control and can write this field to control the effective local Pstate request that will eventually propagate through the downstream logic and determine the Local PState Actual. Note: if no write to this register is performed, the currently established value is maintained stable forever.
8:15	ROX	LOCAL_PSTATE_TARGET: This field is the target Pstate of a complete Pstate change that is performed in smaller steps
16:23	ROX	LOCAL_CORE_PSTATE_STEP_TARGET: this field represents the intermediate value that is about to be established as the next Local Pstate Actual after completing one step in the process of the transition towards the 'local_Pstate_target' the new voltage, frequency, and clock resonance setting
24:31	ROX	LOCAL_ECO_PSTATE_STEP_TARGET: this field represents the intermediate value that is about to be established as the next Local Pstate Actual after completing one step in the process of the transition towards the 'local_Pstate_target' the new voltage, frequency, and clock resonance setting

Register Name	Read-Only Status Register For DPLL And For Debugging (PDSR)
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_DPLL_STATUS_REG
Address	00000000150F0161 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:14	ROX	DPLL_FF_FREQOUT: frequout output from DPLL (current frequency - bits 2 to 10 correspond to the same scale as the 9 bits of frequin (which need to be multiplied with our frequency step to get the real frequency), the remaining bits just provide a higher accuracy)
15	ROX	DPLL_FREQU_CHANGE: DPLL Frequency change (pin of DPLL without filter)
16	ROX	DPLL_STATUS_SPARE_BIT1: Spare bit.
17	ROX	PMAX_SYNC_PENDING: gets asserted, if the logic has a Pmax sync interrupt outstanding that will be eventually sent to PMC when the Pmax sync criterion is met
18	ROX	GA_ACK_PENDING: gets asserted, if the logic has a global actual Pstate update acknowledgment interrupt outstanding that will be eventually sent to PMC when the GA ack criterion is met
19:26	ROX	CAPPED_GLOBAL_PSTATE_REQ: corresponds to the capped global Pstate request that is presented as Pstate interrupt and send to PMC



Bits	PCB	Field Mnemonic: Description
27	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT2: DPLL runs at Fmax and CPM bit 2 is set. Note that this bit and the following 2 bits indicate, that the CPMs would allow the DPLL to run faster than Fmax.
28	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT3: DPLL runs at Fmax and CPM bit 3 is set
29	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT4: DPLL runs at Fmax and CPM bit 4 is set
30	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT2: DPLL runs at Fmin and CPM bit2 is zero. Note that this bit and the following 2 bits indicate, that the CPMs indicate, that the DPLL should run slower than the currently established Fmin.
31	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT1: DPLL runs at Fmin and CPM bit1 is zero
32	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT0: DPLL runs at Fmin and CPM bit0 is zero
33	ROX_CLRPAR T	DPLL_FASTER_THAN_FMAX_PLUS_DELTA1: The DPLL indicated that it ran once faster than Fmax+dpll_char_delta1
34	ROX_CLRPAR T	DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2: The DPLL indicated that it ran once slower than Fmin-dpll_char_delta2
35:48	ROX	DPLL_MAX_FREQOUT_AFTER_LAST_READ: This dial indicates the maximum DPLL frequout value after the last read of this register (only 14 MSBs)
49:62	ROX	DPLL_MIN_FREQOUT_AFTER_LAST_READ: This dial indicates the minimum DPLL frequout value after the last read of this register (only 14 MSBs)

Register Name	<i>The PIVRMVCR0 Controls The Voltage Stepping Delays</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG0
Address	00000000150F0162 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	IVRM_REQ_PSTATE_STEPDELAY_RISING: Requested Internal Pstate Baby Step Delay - Rising Step. Delay before allowing the next step for a rising Pstate Transition. This dial and ivrm_req_Pstate_stepdelay_lowering allow for differing delays for the two directional transitions if necessary. In 100ns units as established by scan dial ivrm_100ns_value
8:15	RW	IVRM_REQ_PSTATE_STEPDELAY_LOWERING: Requested Internal Pstate Baby Step Delay - Lowering Step. Delay before allowing the next step for a lower Pstate Transition. This dial and ivrm_req_Pstate_stepdelay_rising allow for differing delays for the two directional transitions if necessary. In 100ns units as established by scan dial ivrm_100ns_value

Register Name	<i>The PIVRMVCR1 Controls The Voltage Stepping Delays</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG1
Address	00000000150F0163 (PCB)
Attributes	
Description	

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Bits	PCB	Field Mnemonic: Description
0:7	RW	IVRM_STABILIZE_DELAY_RUN: Stabilization Delay - Run Time Delay to allow a rail to stabilize upon a baby step while the region is operational. In 100ns units as established by scan dial ivrm_100ns_value
8:15	RW	IVRM_STABILIZE_DELAY_IDLE: Stabilization Delay - Idle Transition Delay to allow a rail to stabilize upon a baby step during an idle transition where the activity in the region is quiesced. In 100ns units as established by scan dial ivrm_100ns_value
16:23	RW	IVRM_PFSTR_PROP_DELAY: PFET Strength Propagation Delay Time from PFET Strength values being launched till PFET Strength Valid is asserted. In order to ensure like rails across domains (Core VDD<>ECO VDD, Core VCS<>ECO VCS) are in sync during operational mode, this time value applies to all rails across the domains. This parameter allows for PFET Strength values to settle before PFET Strength Valid is sampled in the Uregs. The value set must the maximum delay for the worst rail timing and must allow for any metastability settling (for example, normally 2-3 cycles for single signals in an asynch handshake interface)
24:31	RW	IVRM_PFSTRVALID_PROP_DELAY: PFETStrength Valid Propagation Delay Time from ivrm_pfstr_prop_delay expiring to where PFET Strength Valid is deasserted. The value is the maximum of a) the minimum pulse width required for PFETStrength Valid and b) the propagation of PFETStrength Valid through (or enough of) the daisy chain. In order to ensure like rails across domains (Core VDD<>ECO VDD, Core VCS<>ECO VCS) are in sync during operational mode, this time value applies to all rails across the domains and thus must be the set to the value of the worst (slowest) rail. The minimum pulse width cannot be violated. The propagation delay can be tuned for more aggressive timing (for example, de-assert before the actual propagation is complete). Measured in prv_nclk cycles. The min delay is 2 cycles. Additional delay can be configured with the following settings 0x00 = No additional delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks
32:39	RW	IVRM_VPUMP_POWERON_TIME: iVRM (VRreg and UReg) - Vpump Power On Time Time necessary for the distributed internal VRM macro circuits to power on. Same delay is required for power on voltage pump circuit. Both delays are in the 8us range. In 100ns units as established by scan dial ivrm_100ns_value
40:47	RW	IVRM_BYPASS_DELAY: iVRM Bypass Propagation Delay Delay time for bypass_b signal propagation. Measured in prv_nclk cycles Target: 50ns 0x00 = No delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks



Bits	PCB	Field Mnemonic: Description
48:55	RW	PFET_VPUMP_ENABLE_DELAY: PFET and Vpump Enable Propagation Delay Delay time for PFET enable and vpump enable signal propagation. Target: 130ns Measured in prv_nclk cycles 0x00 = No delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks
56:62	RW	IVRM_VID_VOUT_THRESHOLD: VID threshold If the output voltage (Vout) is targeting a value below this threshold the slow PFET can backed off from its normal drive strength so as to reduce the ripple at these lower voltage conditions

Register Name	<i>POHR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_OCC_HEARTBEAT_REG
Address	00000000150F0164 (PCB)
Attributes	
Description	Controls the behavior of the OCC heartbeat function.

Bits	PCB	Field Mnemonic: Description
0:7	RW	occ_heartbeat_time ' OCC Heartbeat Time Value' " This field defines the number of ~64us hang timer pulses in which a a PCB read or write of the heartbeat trigger register (of which the offset is specified by dial occ_heartbeat_reg_addr_offset) is not detected that will constitute the loss of the OCC heartbeat. If occ_heartbeat_en is set and upon this loss detection, POHBR[psafe] is forced and, if enabled, the error TBD is activated ' ' '0x00 - unsupported, causes undefined behavior' '0x01 - 64us +0/-1us' '0x02 - 128us +0/-1us' '...' '0xFF - 16320us +0/-1us 16.3ms' " 'Upon the 64us hang pulse, the decremter ticks. if the decremter reaches x00, the heartbeat loss event is triggered.' ' '
8	RW	occ_heartbeat_enable ' OCC Heartbeat Timer Enable' " '0 = Disable the OCC Heartbeat function. Lack of accesses to the register defined by the dial occ_heartbeat_reg_addr_offset does not result in heartbeat loss events to be triggered (no FIRs set nor Safe mode entry).' " '1 = Enable the OCC Heartbeat function. '
9:16	RW	occ_heartbeat_reg_addr_offset This dial allows to configure the address offset within the PCBS power management entity of the register, that will regularly reset the heartbeat timer (which is called heartbeat trigger register). The address offset is 0x100 plus the value of this dial.
17:24	RW	Psafe ' Pstate Safe' " 'This field establishes the Pstate that the core chiplet will take on if:' 'psafe <= PMSR[global_actual_pstate] ' AND any of the following conditions are true:' 'Loss of OCC Heartbeat if occ_heartbeat_en is set' 'PMGPO[force_safe_mode] is set' " 'If psafe > PMSR[global_actual_pstate], the global_actual_pstate is forced.' " 'The value of Psafe needs to be at or below the nominal Pstate to make sure safe operation of all chiplets. '

Register Name	PRCCR0 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG0
Address	00000000150F0165 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function.

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Bits	PCB	Field Mnemonic: Description
0	ROX	RESCLK_DIS: Resonant Clock Enable Master enable of all resonant clocking functions. This dial can be set by setting GP3(22) and can not be set in this PCBS_resonant_Clock_Control_Reg0. 1 = Resonant Clock function is disabled. Default values (0) for resclk_value, resclk_core_sync_value, csb_eco_sync_value 0 = Resonant Clock Control hardware is enabled (the mode is defined by dial resclk_control_mode)
1	RW	RESCLK_CONTROL_MODE: Resonant Clock Control Mode Defines the control means enabled when resclk_dis is not set. 0 = Pstate band hardware mechanism enabled 1 = Manual mode enabled (Firmware mode) If this bit is set to 0, the hardware control mechanism that manages the transition across the Resonant Bands is enabled. If this bit is set to 1, the automatic Pstate band hardware mechanism is disabled and the Firmware is in control of all values of the dial resclk_value, resclk_core_sync_value, csb_eco_sync_value. Firmware must ensure that frequency changes will not cross resonant bands or machine failures may result. resclk_value represents the values for clock sector buffer strength, inductor switch strength and high inductor enable. Firmware must ensure the correct stepping in/out the different bands and propagation of the values (resclk_value) to the core/eco (resclk_core_sync_value / csb_eco_sync_value).
2:4	RW	RESCLK_SYNC_PW: Resonant Clock Sync Pulse Width Number of nest/4 cycles to assert the clock sync signal. This value must be high enough to ensure capture and propagation across the asynchronous chiplet boundary.
5:11	RW	RES_SYNC_DELAY_CNT: Resonant Clock Sync Delay Number of nest/4 cycles wait after the launch of the resclk_value (csb and inductor) before launching the sync to allow these to be captured. This value must be high enough to ensure full propagation to the input of the clock sector buffers and inductor switches.
12:26	RW	RES_CSB_STR_INSTR_LO: Resonant Clock Sector Buffer Strength Instruction - Low Band Mask value that determines whether, during a fixed 15 step sequence, the res_csb_str(0:3) is to be decremented/incremented in entering/exiting the Low Band. During resonant clock Entry, res_csb_str(0:3) decremented by the value pattern from 0 down to 14. During resonant clock Exit, res_csb_str(0:3) incremented by the value pattern from 14 up to 0.
27:41	RW	RES_CSB_STR_INSTR_HI: Resonant Clock Sector Buffer Strength Instruction - High Band Mask value that determines whether, during a fixed 15 step sequence, the res_csb_str(0:3) is to be decremented/incremented in entering/exiting the High Band. During resonant clock Entry, res_csb_str(0:3) decremented by the value pattern from 0 down to 14. During resonant clock Exit, res_csb_str(0:3) incremented by the value pattern from 14 up to 0.

Register Name	PRCCR1 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG 1
Address	00000000150F0166 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function. Writes are conditioned.

Bits	PCB	Field Mnemonic: Description
0:7	RW	FULL_CSB_PS: Full Clock Sector Buffer Pstate Pstate defining the maximum point where the clock sector buffer must be driven to full strength. This allow clocks to be distributed at low Vmin levels. FW needs to make sure that no overlaps occur with bands 2 or 3.
8:15	RW	RES_LOW_LOWER_PS: Low Frequency Resonant Lower (LFRLow) Pstate Pstate defining the lower frequency of the Low Resonant Frequency Band. FW needs to make sure that no overlap occurs with band 0.



Bits	PCB	Field Mnemonic: Description
16:23	RW	RES_LOW_UPPER_PS: Low Frequency Resonant Upper (LFRUpper) Pstate Pstate defining the upper frequency of the Low Resonant Frequency Band. Note that if an overlap occurs with band 3, the hardware behavior is undefined.
24:31	RW	RES_HIGH_LOWER_PS: High Frequency Resonant Lower (HFRLow) Pstate Pstate defining the lower frequency of the High Resonant Frequency Band. Note that if an overlap occurs with band 2, the hardware behavior is undefined.
32:39	RW	RES_HIGH_UPPER_PS: High Frequency Resonant Upper (LFRUpper) Pstate Pstate defining the upper frequency of the High Resonant Frequency Band. This value needs to be greater or equal to high_res_lower_ps.
40:43	RW	NONRES_CSB_VALUE_TI: Clock Sector Buffer Table Index for non-resonant state Table Index into Clock Sector Buffer Table for the nominal, non-resonant state.
44:47	RW	FULL_CSB_VALUE_TI: Clock Sector Buffer Table Index for full CSB value Table Index into Clock Sector Buffer Table for the full CSB strength value.
48:56	RWX	RESCLK_VALUE: Output register driving the 9 bit resclk_value In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current resclk_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. The value in this register represents the following concatenation: csb_str_value(0:3) sw_str(0:3) hi_induct_en.
57	RWX	RESCLK_CORE_SYNC_VALUE: Output register driving the resclk_core_sync signal In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current resclk_core_sync_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. This bit is supposed to be used in order to create a SCOM-controlled pulse to force an update of the resclk propagation registers. A 1 enables the synchronous update, a 0 disables it. Suggested use of this bit is to set it to 1 and then set it back to 0 to create a (long) update pulse.
58	RWX	CSB_ECO_SYNC_VALUE: Output register driving the csb_eco_sync signal In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current csb_eco_sync_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. This bit is supposed to be used in order enable the ECO domain to participate in clock sector buffer strength changes, when switching from nominal strength to full CSB strength. A 1 enables the ECO domain, a 0 disables it from seeing a CSB strength update.

Register Name	PRCCR1 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_STATUS_REG
Address	00000000150F0167 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function.



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Bits	PCB	Field Mnemonic: Description
0	ROX	RESCLK_STATE: Resonant Clock State 0 = Resonant Clocking inactive 1 = Resonant Clocking active Valid if resclk_inprogress = 0. Hardware sets this bit to the right value at the completion of the transition into and out of resonance mode.

Bits	PCB	Field Mnemonic: Description
1	ROX	RES_HI_INDUCT_EN: Resonant High Inductor Enable Valid if resclk_inprogress = 0. This dial provides the current value being propagated. 0 = Resonant Clock mode not active 1 = Resonant Clock mode active
2	ROX	RESCLK_INPROGRESS: Resonant Clock Transition in Progress This bit is set by hardware while a transition is in progress and will be reset by hardware when the operation is complete.
3	ROX	RESCLK_FULL_CSB: Full CSB Clock State 0 = Full CSB Clocking inactive 1 = Full CSB Clocking active Valid if resclk_inprogress = 0. Hardware sets this bit to the right value at the completion of the transition into and out of full CSB mode respectively.

Register Name	<i>PLPFTCR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_CONTROL_REG
Address	00000000150F0168 (PCB)
Attributes	
Description	The PLPFTCR enables firmware to configure the modes that are used for the PCBS Local Pstate Frequency Target Status Register.

Bits	PCB	Field Mnemonic: Description
0:2	RW	DELAY_TIME: This field encodes the delay between the time a Local Actual Pstate change modifies the input to the DPLL and the time frequency acquisition begins to allow the hardware to ignore the frequency transition of the DPLL in order to get better frequency measurements. This field encodes a delay of ~1us to ~128us in power of 2 selects. The delay is defined by $2^{**}delay\_time$ in us. Note that the hardware uses multiples of the slow hang pulse that is running at 1us.
3	RW	RECORD_TRANSITIONS: This bit indicates whether the LPFTSR records events that correspond to Local Actual Pstate changes (and therefore may include DPLL slewing effects.) One usage model would set the periodic sample_time defined by the dial OHA_MODE_REG[tod_pulse_count_match_val] to a time less than the worst-case DPLL slew time but then ignore Pstate transitions because they might include DPLL slew effects.
4:18	RW	MULTIPLIER: This 15-bit unsigned constant is multiplied by the DPLL frequency code (9 bits) implied by the Local Actual Pstate to yield the 24-bit frequency target measured in PCBS-PM clock cycles (core clock / 2). Assuming times in seconds and frequencies in Hz, firmware should set this constant to: $(DPLL\_Frequency\_Code\_Step\_Hz * Sample\_Time\_Seconds) / 2$
19	RW	ENABLE_LPFT_FUNCTION: This is the enable bit to enable the local Pstate frequency target function. A '1' enables the function, a '0' disables it (the value can be changed at any time).

Register Name	<i>PLPFTSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_STATUS_REG
Address	00000000150F0169 (PCB)
Attributes	
Description	

Registers Specification

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Bits	PCB	Field Mnemonic: Description
0	ROX_CLRPART	VALID: If this bit is set then all of the remaining fields of this register are valid. This bit is cleared whenever the register is read or after a local actual Pstate change occurs, and is will be set whenever the hardware completes a valid sample. If firmware reads this register and the valid bit is not set, then it indicates that the Local Pstate target frequency acquisition logic has not been able to complete a frequency acquisition for any Local Actual Pstate change since the last time the LPFTSR was read. This could be due to either of the following factors: 1. Firmware is sampling the LPFTSR faster than the time implied by the sample time defined in OHA by the dial OHA_MODE_REG[tod_pulse_count_match_val] field
1	ROX	CPM_DPLL: If the valid bit is set, then if cpm_dpll is set it indicates that the event recorded by this register was due to a Local Actual Pstate implemented by the DPLL running in CPM-DPLL mode, otherwise the value of this bit is undefined. If the valid bit is not set, this bit is undefined.
2	ROX	IVRM: If the valid bit is set, then if ivrm is set it indicates that the event recorded by this register was due to a Local Actual Pstate whose voltage was set locally by the iVRM operating entirely in regulation mode. If the valid bit is not set, this bit is undefined.
3	ROX	TRANSITION: If the valid bit is set, then if transition is set it indicates that during the observation period a Local Pstate Actual change has occurred, and any performance delta may be due to DPLL frequency slewing. If the valid bit is not set, this bit is undefined
4	ROX	STABLE: If stable is set it indicates that the DPLL input frequency has been stable since the last time the PLPFTSR was read. This bit is set whenever the PLPFTSR is read, and cleared whenever the Fmax input of the DPLL changes. This bit is always valid, regardless of the state of the valid bit. If the PLPFTSR is read on the same cycle a frequency changes then the stable bit is cleared. This bit helps firmware better understand how to interpret the information contained in the PLPFTSR. (Note that this bit should have an attribute ROX_SETPART, but this is not supported by regchk.)
5:28	ROX	DELTA: If the valid bit is set then this is the 24-bit signed difference Measured Cycles - Target Cycles for the event captured by this register. If the valid bit is not set, this dial is undefined.
29:52	ROX	CUMULATIVE: This field records the 24-bit cumulative (signed) delta for all valid samples taken since this field was cleared. Writing any value to this register clears this field. Note that it should have an attribute WOX_CLRPART, but this is not supported by regchk/figtree.
53:60	ROX	PSTATE: If the valid bit is set then this is the Local Actual Pstate of the frequency acquisition that had the minimum (signed) delta of any valid sample taken since the last time the LPFTSR was read. If the valid bit is not set, then this field is undefined.

Register Name	PFSMM1/2 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR1_REG
Address	00000000150F0170 (PCB)
Attributes	
Description	The PFSMM1/2 facilitates debug by providing insight into the internal FSM states of the PCB-slave power-management unit. For expert use only. Coding according to VHDL design.

Bits	PCB	Field Mnemonic: Description
0:6	ROX	BABYSTEP_MAIN_FSM: Main Babystep FSM (mfsm_lt)
7:11	ROX	BABYSTEP_SLAVE_FSM: Babystep Slave FSM (sfsm_lt)
12:16	ROX	CORE_RAILSTEPPER_MAIN_FSM: Main Core Railstepper FSM (mrsfsm_lt)
17:21	ROX	ECO_RAILSTEPPER_MAIN_FSM: Main ECO Railstepper FSM (mrsfsm_lt)



Bits	PCB	Field Mnemonic: Description
22:25	ROX	CORE_RAILSTEPPER_SUB_FSM: Core Railstepper Sub-FSM (srsfsm_lt)
26:29	ROX	ECO_RAILSTEPPER_SUB_FSM: ECO Railstepper Sub-FSM (srsfsm_lt)
30:34	ROX	CORE_RAILSTEPPER_BYP_FSM: Core Railstepper Bypass FSM (byp_fsm_lt)
35:39	ROX	ECO_RAILSTEPPER_BYP_FSM: ECO Railstepper Bypass FSM (byp_fsm_lt)
40:45	ROX	IVRM_CORE_VDD_SEQUENCER_FSM: Core iVRM Sequencer for Vdd (ivrm_fsm_lt)
46:51	ROX	IVRM_CORE_VCS_SEQUENCER_FSM: Core iVRM Sequencer for Vcs (ivrm_fsm_lt)
52:57	ROX	IVRM_ECO_VDD_SEQUENCER_FSM: ECO iVRM Sequencer for Vdd (ivrm_fsm_lt)
58:63	ROX	IVRM_ECO_VCS_SEQUENCER_FSM: ECO iVRM Sequencer for Vcs (ivrm_fsm_lt)

Register Name	<i>Refer To The Description Of PFSMM1.</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR2_REG
Address	00000000150F0171 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:6	ROX	RESCLK_BAND_FSM: Band Sequencer for resonant clocking (band_fsm_lt)
7:10	ROX	RESCLK_LOWRES_FSM: Low Resonant Clocking sequencer (lowres_fsm_lt)
11:14	ROX	RESCLK_HIGHRES_FSM: High Resonant Clocking sequencer (highres_fsm_lt)
15:18	ROX	RESCLK_FULLCSB_FSM: Full-CSB Resonant Clocking sequencer (fullcsb_fsm_lt)
19:22	ROX	RESCLK_UPDATE_FSM: Resonant Clocking Update sequencer (update_fsm_lt)
23:29	ROX	IDLE_TRANSITION_FSM: Idle State Sequence FSM (ifsm_lt)
30:37	ROX	Peco_step_target_uv Current ECO Step Target Pstate (different from Plocal_actual for undervolting)
38:45	ROX	Pcore_step_target_uv Current core Step Target Pstate (different from Plocal_actual for sleep and undervolting)

Register Name	<i>Protect Mode Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.PROTECT_MODE_REG
Address	00000000150F03FE (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	READ_PROTECT_ENABLE: Enable read protection
1	RW	WRITE_PROTECT_ENABLE: Enable write protection

Register Name	<i>Atomic Lock Register</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX05.TP_PCB_SLAVE_INST.ATOMIC_LOCK_REG	
Address	00000000150F03FF (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	RW	ATOMIC_LOCK_ENABLE: Enable atomic lock
1:4	ROX	ATOMIC_ID: Atomic ID

Register Name	<i>Contains The Slave's Primary Address</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.PRIMARY_ADDRESS_REG	
Address	00000000160F0000 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RO	Reserved field (Access type is primary_address)

Register Name	<i>Multicast Group 1</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.MULTICAST_GROUP_1	
Address	00000000160F0001 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST1_GROUP: multicast group1 setting

Register Name	<i>Multicast Group 2</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.MULTICAST_GROUP_2	
Address	00000000160F0002 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST2_GROUP: multicast group2 setting



Register Name	<i>Multicast Group 3</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.MULTICAST_GROUP_3	
Address	00000000160F0003 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST3_GROUP: multicast group3 setting

Register Name	<i>Multicast Group 4</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.MULTICAST_GROUP_4	
Address	00000000160F0004 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST4_GROUP: multicast group4 setting

Register Name	<i>Timeout Select Register</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.TIMEOUT_REG	
Address	00000000160F0010 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:1	RW	Reserved field (Access type is int_timeout)

Register Name	<i>Assist Interrupt Register</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.ASSIST_INTERRUPT_REG	
Address	00000000160F0011 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is attn)
1	ROX	Reserved field (Access type is recov)
2	ROX	Reserved field (Access type is xstop)

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Register Name	GP3 Register (NA In PERV CPLT)
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.GP3_REG
Address	00000000160F0012 (PCB) 00000000160F0013 (PCB1) 00000000160F0014 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset
2	RWX	RWX_WAND	RWX_WOR	GLSMUX_RESET: Glsmux reset for test purpose and stuck active mesh protection. Notice no clocks in the EX if this bit is set.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Put the DPLL in test mode.
4	RWX	RWX_WAND	RWX_WOR	PLL_RST: Put PLL in reset state.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYP: Enable PLL bypass.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pcb_access)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	PM_PI_DECODE: Test override for power management. EX chiplet only.
22	RWX	RWX_WAND	RWX_WOR	RESCLK_DIS: Resonant clocking disable.
23:25	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave will report 'Chiplet Offline'.
27	RWX	RWX_WAND	RWX_WOR	TP_LVLTRANS_FENCE: Electrical winkel fence. Mainly used by power management.
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.
29:31	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)



Register Name	<i>Skew Adjust Data</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.CLK_ADJ_REG	
Address	00000000160F0015 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:15	ROX	

Register Name	<i>Clk Ajust Config</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.CLK_ADJ_SET	
Address	00000000160F0016 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:31	RW	CLK_ADJ_SET_REG: Clk adj config

Register Name	<i>Vital Scan Out</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.VITAL_SCAN_OUT	
Address	00000000160F0017 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	

Register Name	<i>Chiplet Heartbeat Register</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.HEARTBEAT_REG	
Address	00000000160F0018 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	HEARTBEAT_DEAD: Chiplet heartbeat not detected



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Register Name	<i>Lock Indications From PLLs</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.PLL_LOCK_REG
Address	00000000160F0019 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	ROX	Reserved field (Access type is lock)

Register Name	<i>Attn Interrupt</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.ATTN_INTERRUPT_REG
Address	00000000160F001A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is attn)

Register Name	<i>Recov Interrupt</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.RECOV_INTERRUPT_REG
Address	00000000160F001B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is recov)

Register Name	<i>Xstop Interrupt</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.XSTOP_INTERRUPT_REG
Address	00000000160F001C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is xstop)



Register Name	<i>Slave Config Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.SLAVE_CONFIG_REG
Address	00000000160F001E (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	CFG_DISABLE_PERV_THOLD_CHECK: Disable pervasive thold check
1	RW	CFG_DISABLE_MALF_PULSE_GEN: Disable pulse generation for malf alert. Switch back to level
2	RW	CFG_STOP_HANG_CNT_SYS_XSTP: Disable hang counter stop for system xstop
3	RW	CFG_DISABLE_CL_ATOMIC_LOCK: Disable atomic lock for chiplet accesses
4	RW	CFG_DISABLE_HEARTBEAT: Disable check for voltage and gridclock in the chiplet
5	RW	CFG_ZERO_DATA: Sent zero data on any error
6:7	RW	
8:12	RW	ERROR_MASK: mask bits for slave error reporting
13:15	RW	

Register Name	<i>Error Capture Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.ERROR_REG
Address	00000000160F001F (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX_WCLEA R	CE_ERROR: Correctable error on pcb bus
1:3	RWX_WCLEA R	CHIPLET_ERRORS: Errors reported by chiplet 000 = no error 001 = XSCOM command blocked due pending errors 010 chiplet offline 011 partial good 100 invalid address / address error / bad access type 101 clock error 110 parity error / received unexpected packet / wrong packet number 111 timeout This register is for debug purposes only. It only holds meaningful data if it is cleared after each error.
4	RWX_WCLEA R	PARITY_ERROR: Parity error on PCB Interface
5	RWX_WCLEA R	DATA_BUFFER_ERROR: Parity error in data buffer
6	RWX_WCLEA R	ADDR_BUFFER_ERROR: Parity error in address buffer
7	RWX_WCLEA R	PCB_FSM_ERROR: Invalid state error in PCB FSM
8	RWX_WCLEA R	CL_FSM_ERROR: Invalid state error in Chiplet FSM
9	RWX_WCLEA R	INT_RX_FSM_ERROR: Invalid state error in interrupt RX FSM
10	RWX_WCLEA R	INT_TX_FSM_ERROR: Invalid state error in interrupt TX FSM

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Bits	PCB	Field Mnemonic: Description
11	RWX_WCLEAR	INT_TYPE_ERROR: Invalid interrupt type
12	RWX_WCLEAR	CL_DATA_ERROR: Parity error on Chiplet Interface
13	RWX_WCLEAR	INFO_ERROR: Parity error on Chiplet info lines
14	RWX_WCLEAR	UNUSED_0:
15	RWX_WCLEAR	CHIPLET_ATOMIC_LOCK_ERROR: Chiplet atomic lock error
16	RWX_WCLEAR	PCB_INTERFACE_ERROR: Error of pcb interface component for the internal endpoint
17	RWX_WCLEAR	CHIPLET_OFFLINE: Heartbeat check indicated that chiplet is offline
18	RWX_WCLEAR	CHIPLET_GRID_SKITTER: Heartbeat check indicated skitter on the chiplet grid
19	RWX_WCLEAR	GP3_REG_PARITY_ERROR: gp3 register parity bad
20	RWX_WCLEAR	ADDRESS_REG_PARITY_ERROR: address register parity bad
21	RWX_WCLEAR	TIMEOUT_REG_PARITY_ERROR: timeout select register parity bad
22	RWX_WCLEAR	CONFIG_REG_PARITY_ERROR: slave config register parity bad
23	RWX_WCLEAR	CLK_ADJ_REG_PARITY_ERROR: clk adj register parity bad
24	RWX_WCLEAR	DIV_REG_PARITY_ERROR: div register parity bad
25:28	RWX_WCLEAR	PLL_UNLOCK_ERROR: unlock from chiplet pll

Register Name	<i>Hang Pulse Generation Register 0.</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.HANG_PULSE_0_REG
Address	00000000160F0020 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_0: Value of hang pulse 0. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_0: If set to '1', hang pulses are suppressed in case of a xstop



Register Name	<i>Hang Pulse Generation Register 1.</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.HANG_PULSE_1_REG	
Address	00000000160F0021 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_1: Value of hang pulse 1. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_1: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 2.</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.HANG_PULSE_2_REG	
Address	00000000160F0022 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_2: Value of hang pulse 2. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_2: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 3.</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.HANG_PULSE_3_REG	
Address	00000000160F0023 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_3: Value of hang pulse 3. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_3: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 4.</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.HANG_PULSE_4_REG	
Address	00000000160F0024 (PCB)	
Attributes		
Description		

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Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_4: Value of hang pulse 4. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_4: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 5</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.HANG_PULSE_5_REG
Address	00000000160F0025 (PCB)
Attributes	
Description	This hang counter is used exclusively to generate the malfunction alert pulse.

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_5: Value of hang pulse 5. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_5: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 6</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.HANG_PULSE_6_REG
Address	00000000160F0026 (PCB)
Attributes	
Description	This hang counter is exclusively used for heartbeat generation.

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_6: Value of hang pulse 6. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_6: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Divider For Hang Counter Clock</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.PRE_COUNTER_REG
Address	00000000160F0028 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PRE_COUNTER: Divider for hang counter clock. Divides clock by n+1 (default: n=0)



Register Name		PowerManagement GP0		
Mnemonic		EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PMGP0_REG		
Address		00000000160F0100 (PCB) 00000000160F0101 (PCB1) 00000000160F0102 (PCB2)		
Attributes				
Description				
Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PM_DISABLE: Master Switch for the PowerManagement Macro
1	RWX	WOX_AND	WOX_OR	PMGP0_SPARE_BIT1: spare bit
2	RWX	WOX_AND	WOX_OR	TP_TC_RESTART_CORE_DOMAIN: Kicks off small sequencer in OHA to get chiplet clocks back running for fast sleep without involving PORE. From GP-reg and overridden by PowMan State Machine.
3	RWX	WOX_AND	WOX_OR	DPLL_THOLD: Thold for the DPLL clock domain in the chiplet
4	RWX	WOX_AND	WOX_OR	PERV_THOLD: Thold for the Pervasive clock domain in the chiplet
5	RO	RO	RO	Reserved.
6	RO	RO	RO	Reserved.
7	RWX	WOX_AND	WOX_OR	PM_DPLL_TIMER_ENA: Select a timer instead of the DPLL lock bit for criteria to switch to DPLL. The time is defined by thold_timer_sel.
8	RWX	WOX_AND	WOX_OR	DPLL_LOCK_SENSE: DPLL lock sensitivity control (0=faster lock time, 1=slower lock time)
9	RWX	WOX_AND	WOX_OR	PMGP0_SPARE2: spare bit
10	RWX	WOX_AND	WOX_OR	DPLL_RESET: Reset to DPLL
11	RWX	WOX_AND	WOX_OR	PMGP0_SPARE_BIT11: Spare bit
12:19	RWX	WOX_AND	WOX_OR	DPLL_TESTOUT_CTL: DPLL testout control
20	RWX	WOX_AND	WOX_OR	TP_TC_CACHE2CORE_FENCE: Fence from cache to core domain in EX chiplet
21	RWX	WOX_AND	WOX_OR	TP_TC_CORE2CACHE_FENCE: Fence from core to cache domain in EX chiplet
22	RWX	WOX_AND	WOX_OR	TP_TC_PERVASIVE_ECO_FENCE: Pervasive ECO fence
23	RWX	WOX_AND	WOX_OR	CHKSW_HW257424_DISABLE: Chicken switch for interrupt retry exhausted bug (0=fix enabled, 1=fix disabled)
24:26	RWX	WOX_AND	WOX_OR	TP_CLK_ASYNC_RESET_DC: Clk async reset for three glitchless muxes, and the two clock dividers (bit 0 = master GLM, bit 1 = ECO Div2 and ECO GLM, bit 2= core Div1 and core GLM)
27:29	RWX	WOX_AND	WOX_OR	TP_CLKGLM_SEL_DC: Glitchless Mux Select for primary chiplet clock source (feeding both core and eco clock muxes) 000 = refclk, 001 = DPLL. 100 = Use constant selected by bit 34, else refclk
30	RWX	WOX_AND	WOX_OR	TP_CLKGLM_ECO_SEL_DC: Glitchless Mux Select for eco domain (cache_nclk) grid. 0= follow primary source chosen by previous field: 1 = Use constant selected by bit 34
31	ROX	NC	NC	SPECIAL_WKUP_DONE: Indicates that special wakeup is done, if asserted
32:33	RWX	WOX_AND	WOX_OR	TP_CLKGLM_CORE_SEL_DC: Glitchless Mux Select for core domain (nclk grid) mux. 0b00=primary GLS mux output, 0b10=constant input, 0b01=refclk. Valid transitions are 0b01 <-> 0b00 <-> 0b10, 0b11 is illegal

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
34	RWX	WOX_AND	WOX_OR	TP_CLKGLM_CONST_DC: Constant input available to all three ClkGlm
35:36	RWX	WOX_AND	WOX_OR	THOLD_TIMER_SEL: Selection for the thold transition timer in the IDLE state machine. 0b00=1024 cycles delay, 0b01=512 cycles delay, 0b10=256 cycles delay, 0b11= 128 cycles delay
37	RWX	WOX_AND	WOX_OR	BLOCK_ALL_WAKEUP_SOURCES: Setting this bit will make the PM Slave ignore any Wakeup events (ext. interrupt, malfunction alert, any special wakeup bit). This bit is intended to enable firmware concurrent patch capability. Note: This does NOT block the interrupt from being presented to the processor core. The following procedure is required on changes: 1. Firmware may only set this bit after first setting special wakeup and polling for special wakeup complete (OHA and PCB-slave both in running state with AISS and PM FSMs idle). 2. Firmware may only clear this bit if all special wakeup bits are first cleared.
38	RWX	WOX_AND	WOX_OR	TP_TC_DPLL_TESTMODE_DC: ADPLL test mode
39	RWX	WOX_AND	WOX_OR	PM_SLV_WINKLE_FENCE: Fence off the powered off chiplet in winkle. - Logical fence/hold for pcb_slave and pcb_slave_pm. For electrical fence see bit 23.
40	RWX	WOX_AND	WOX_OR	L3_ENABLE_SWITCH: Setting this bit activates l3_edram_enable if allowed by system configuration GP3(28). Resetting this bit deactivates l3_edram_enable.
41	RWX	WOX_AND	WOX_OR	TP_CPLT_IVRM_REFBYPASS_DC: Signal to iVRM (used to be controlled by scan-only block inside EX, but needs to be driven by VIO domain)
42	RWX	WOX_AND	WOX_OR	CHKSW_HW241939_DISABLE: if this bit is set to 1, the fix for HW241939 (pfet enable SCOM-ability) is disabled
43	RWX	WOX_AND	WOX_OR	CHKSW_HW273115_DISABLE: if this bit is set to 1, the fix for HW273115 (Pga ACK noack issue when the babystepper is in the winkle state) is disabled
44	RWX	WOX_AND	WOX_OR	CHKSW_HW245103_DISABLE: if this bit is set to 1, the fix for HW245103 resonant clocking CSB and SW -bit ordering change is disabled
45	RWX	WOX_AND	WOX_OR	CHKSW_HW257534_DISABLE: if this bit is set to 1, the fix for HW257534 (fencing of errors) is disabled
46	RWX	WOX_AND	WOX_OR	CHKSW_HW259509_ENABLE: if this bit is set to 0, the fix for HW259509 (Pstate change hanging, because of DPLL flock timer in a hung state) is disabled
47	RWX	WOX_AND	WOX_OR	CHKSW_HW260345_DISABLE: if set to 1, this bit disables the HW260345 fix (fix was to make sure that we enter bypass mode for iVRM safe mode without a glitch that could cause Vcs in regulation and Vdd in bypass)
48:49	ROX	NC	NC	WAKEUP_INT_TYPE: (Known to be unreliable and not supported, informational usage only) Type of the last wakeup event that caused an exit from sleep or winkle (excluding nap!), regardless of present state. 0b01: External interrupt. 0b10: Malfunction Alert. 0b11: Special Wakeup. 0b00: chiplet has never fully entered and exited a chiplet-level idle state since IPL of the system. (Note this does not necessarily get updated when the processor core enters an idle state, only if the PCB-Slave enters and then exits the idle state for this chiplet).
50	ROX	NC	NC	DPLL_LOCK: DPLL lock indicator
51	ROX	NC	NC	SPECIAL_WKUP_ALL_SOURCES_ORED: logical OR of all special wakeup sources
52	ROX	NC	NC	REGULAR_WKUP_AVAILABLE: logical OR of external interrupt and malfunction alert



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
53	RWX	WOX_AND	WOX_OR	BLOCK_REG_WKUP_SOURCES: blocks ext. int. and malf. Alert from waking up PCBS (no block possible for PC!)

Register Name	PowerManagement GP1
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PMGP1_REG
Address	00000000160F0103 (PCB) 00000000160F0104 (PCB1) 00000000160F0105 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	SLEEP_POWER_DOWN_EN: Sleep Power Down Enable: When set to 1, causes hardware to automatically reduce voltage to the Core domain when entering Sleep mode. The voltage value for power down is chosen by sleep_power_off_sel (bit 2). When set to 0, a request is sent to the PORE engine for assistance entering Sleep.
1	RWX	WOX_AND	WOX_OR	SLEEP_POWER_UP_EN: Sleep Power Up Enable: When set to 1, enables automated hardware restoration of voltage via PFETs and, if enabled, iVRMs when exiting Sleep mode. If this bit is set to 0 the hardware rely on external means (PORE or equivalent) to restore voltage.
2	RWX	WOX_AND	WOX_OR	SLEEP_POWER_OFF_SEL: Sleep Power Off Select: Selects which voltage level to place the Core domain PFETs upon Sleep entry. 0 = Vret (Fast Sleep Mode), 1 = Voff (Deep Sleep Mode). Depending on the setting of pmicr_latency_en, this bit is controlled with a PCB-write (0) or by the PMICR in the core (1).
3	RWX	WOX_AND	WOX_OR	WINKLE_POWER_DOWN_EN: Winkle Power Down Enable: When set to 1, causes hardware to automatically reduce voltage to the entire Chiplet (both Core and ECO Domains) when entering Winkle mode. The voltage value for power down is chosen by winkle_power_off_sel (bit 5). When set to 0, a request is sent to the PORE engine for assistance entering Winkle.
4	RWX	WOX_AND	WOX_OR	WINKLE_POWER_UP_EN: Winkle Power Up Enable: When set to 1, enables automated hardware PFET enablement when exiting Winkle mode. If this bit is set to 0 the hardware rely on external means (PORE or equivalent) to cause the PFETs to be re-enabled.
5	RWX	WOX_AND	WOX_OR	WINKLE_POWER_OFF_SEL: Winkle Power Off Select: Selects which voltage level to place the Core and ECO domain PFETs upon Winkle entry. 0 = Vret (Fast Winkle Mode), 1 = Voff (Deep Winkle Mode). Depending on the setting of pmicr_latency_en, this bit is controlled with a PCB-write (0) or by the PMICR in the core (1).
6	RWX	WOX_AND	WOX_OR	OHA_WKUP_OVERRIDE_EN: Needs to be 0 for normal operation. If set to 1, the two following dials are used to override the regular and special wakeup signal from PCBS to OHA
7	RWX	WOX_AND	WOX_OR	OHA_PM_WKUP_OVERRIDE: Enablement by 'oha_wkup_override_en' forces the regular wakeup signal to OHA to the value of this bit regardless of presence of an interrupt source.
8	RWX	WOX_AND	WOX_OR	OHA_SPC_WKUP_OVERRIDE: Enablement by 'oha_wkup_override_en' forces the special wakeup signal to OHA to the value of this bit, regardless of the firmware settings.

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
9	RWX	WOX_AND	WOX_OR	ENDP_RESET_PM_ONLY: If asserted, an endpoint reset of all power management-related functions (not the regular PCB slave) is performed. Intended usage is for recovery.
10	RWX	WOX_AND	WOX_OR	DPLL_FREQ_OVERRIDE_ENABLE: override Fmax/Fmin only, if '1', using register FREQ_CTRL_REG
11	RWX	WOX_AND	WOX_OR	PM_SPR_OVERRIDE_EN: PM SPR Override Enable The PPMCR (0xNNNN) and PPMICR (0XXXXX) accesses the register resources that make up the PMCR SPR used by hypervisor to management Pstates. Thus, PCB updates to it are disabled in hardware to prevent collisions. This bit allows ownership of the PMCR to be switched from hypervisor to OCC. This switch is immediate in hardware, thus, firmware must ensure the ownership switch is otherwise communicated. 0 = Disables the writing of the PPMCR (0xNNNN) from the PCB and allows SPR 884 writes (mtspr) to update the register resource. 1 = Enables the writing of the PPMCR (0xNNNN) from the PCB.
12	RWX	WOX_AND	WOX_OR	FORCE_SAFE_MODE: Force Safe Mode 0 = Allow other enabled features to determine the operational Pstate. 1 = Forces the minimum of POHBR[psafe] and PPMSR[global_pstate_actual] Pstate for the core chiplet as the operational frequency.
13	RWX	WOX_AND	WOX_OR	IVRM_SAFE_MODE_EN: Internal VRM Safe Mode Enable 0 = Disable the iVRM safe mode, thus, no automatic actions occur, if an iVRM error happens. 1 = if the iVRMs are enabled (PIVRMCSR[ivrm_en] is set) and Pstates are enabled and if the error defined by dial pcbs_ivrm_gross_or_fine_err occurs, then the railstepper is forced into bypass mode to prevent a voltage-frequency hazard
14	RWX	WOX_AND	WOX_OR	IVRM_SAFE_MODE_FORCE_ACTIVE: Internal VRM Safe Mode Force Dial 0 = the hardware decides whether to activate the iVRM safe mode or not 1 = the iVRM safe mode is forced regardless (this makes only sense if ivrm_fsm_enable=1 and Pstates are enabled)
15	RWX	WOX_AND	WOX_OR	PMICR_LATENCY_EN: Selects how the sleep/winkle latency (which is deep/fast) is controlled. If asserted the PMICR controls the winkle/sleep_power_off_sel in PMGP1, otherwise those bits are controlled via SCOM by OCC.
16	RWX	WOX_AND	WOX_OR	ENABLE_OCC_CTRL_FOR_LOCAL_PSTATE_EFF_REQ: controls, if the HW (for value 0) or OCC (value 1) is in control of the Local Pstate Effective register in PPSTR
17	RWX	WOX_AND	WOX_OR	SERIALIZE_PFET_POWERDOWN: if asserted, the pFET sequencer will sequence the core and the ECO domain one after the other when powering down
18	RWX	WOX_AND	WOX_OR	SERIALIZE_PFET_POWERUP: if asserted, the pFET sequencer will sequence the ECO and the core domain one after the other when powering up
19	RWX	WOX_AND	WOX_OR	DISABLE_FORCE_DEEP_TO_FAST_SLEEP: 0: (normal operation) - If PCB Slave reports a recoverable error or a checkstop, a DEEP sleep operation is forced to FAST. The entries in sleep/winkle_power_off_sel remain unchanged. 1: force to FAST is disabled.



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
20	RWX	WOX_AND	WOX_OR	DISABLE_FORCE_DEEP_TO_FAST_WINKLE: 0: (normal operation) - If PCB Slave reports a recoverable error or a checkstop, a DEEP winkle operation is forced to FAST. The entries in sleep/winkle_power_off_sel remain unchanged. 1: force to FAST is disabled.

Register Name	PFET Control/Status Register For Core And ECO Vdd
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PFVDDCNTLSTAT_REG
Address	00000000160F0106 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	CORE_VDD_PFET_FORCE_STATE: Core Domain PFET Force State Provides a means for firmware to force the core domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 4:5 = 00 (both core_vdd_pfet_val_override AND core_vdd_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
2:3	RW	ECO_VDD_PFET_FORCE_STATE: ECO Domain PFET Force State Provides a means for firmware to force the ECO domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 6:7 = 00 (both eco_vdd_pfet_val_override AND eco_vdd_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
4	RW	CORE_VDD_PFET_VAL_OVERRIDE: Core Domain PFET Value Override 0 = Override is disabled
5	RW	CORE_VDD_PFET_SEL_OVERRIDE: Core Domain PFET Stage Select Override 0 = Override is disabled
6	RW	ECO_VDD_PFET_VAL_OVERRIDE: ECO Domain PFET Value Override 0 = Override is disabled
7	RW	ECO_VDD_PFET_SEL_OVERRIDE: ECO Domain PFET Stage Select Override 0 = Override is disabled
8	RW	CORE_VDD_PFET_ENABLE_REGULATION_FINGER: Core Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the core_vdd_pfet_enable_value.
9	RW	ECO_VDD_PFET_ENABLE_REGULATION_FINGER: ECO Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the eco_vdd_pfet_enable_value.

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Bits	PCB	Field Mnemonic: Description
10:21	RW	CORE_VDD_PFET_ENABLE_VALUE: Core PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the Core Domain PFET Enables directly. If core_vdd_pfet_val_override = 1, a write to this field sets the state of the core PFET Enables until core_vdd_pfet_val_override is cleared. If core_vdd_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the core_vdd_pfet_valN_slac registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
22:25	RW	CORE_VDD_PFET_SEL_VALUE: Core PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure core_vdd_pfet_valN_slac(0:11) where N is 0 to 11 if core_vdd_pfet_sel_override = 1. If core_vdd_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
26:37	RW	ECO_VDD_PFET_ENABLE_VALUE: ECO PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the ECO PFET Enables directly. If ECO_vdd_pfet_val_override = 1, a write to this field sets the state of the ECO PFET Enables until ECO_vdd_pfet_val_override is cleared. If eco_vdd_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the eco_vdd_pfet_valN_slac registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
38:41	RW	ECO_VDD_PFET_SEL_VALUE: ECO PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure eco_vdd_pfet_valN_slac(0:11) where N is 0 to 11 if eco_vdd_pfet_sel_override = 1. If eco_vdd_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
42:45	ROX	CORE_VDD_PG_STATE: Core power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
46:49	ROX	CORE_VDD_PG_SEL: For debug, contains the actual index n into Core Domain PFET Value [n] SLAT Register set that contains the Core PFET Enable Value currently enabled.
50:53	ROX	ECO_VDD_PG_STATE: ECO Domain power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
54:57	ROX	ECO_VDD_PG_SEL: For debug, contains the actual index n into ECO Domain PFET Value [n] SLAT Register set that contains the ECO PFET Enable Value currently enabled.

Register Name	PFET Sense Register	
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PFSENSE_REG	
Address	00000000160F0107 (PCB)	
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:11	ROX	TP_CORE_VDD_PFET_ENABLE_SENSE: Not used any more.
12:23	ROX	TP_ECO_VDD_PFET_ENABLE_SENSE: Not used any more.



Bits	PCB	Field Mnemonic: Description
24:35	ROX	TP_CORE_VCS_PFET_ENABLE_SENSE: Not used any more.
36:47	ROX	TP_ECO_VCS_PFET_ENABLE_SENSE: Not used any more.

Register Name	<i>PM Error Summary Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PMERRSUM_REG
Address	00000000160F0108 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	PM_ERROR: PM Error is present. Intended for use by special PCB multicast to see error state of all chiplets with a single read (via 510F0108 to read all chiplets)

Register Name	<i>PM Error Register:</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PMERR_REG
Address	00000000160F0109 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_HANG_ERR: Hang during Unassisted Sleep Entry: SLEEP_ENTRY_NOTIFY_PMC state
1	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ASSIST_HANG_ERR: Hang during Assisted Sleep Entry: SLEEP_ENTRY_NOTIFY_PMC_ASSIST state
2	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ERR: Hang during Unassisted Sleep Exit: SLEEP_EXIT_NOTIFY_PMC state
3	ROX	PCBS_SLEEP_EXIT_INVOKE_PORE_ERR: Hang during Assisted Deep Sleep Exit: SLEEP_EXIT_INVOKE_PORE state
4	ROX	PCBS_WINKLE_ENTRY_NOTIFY_PMC_ERR: Hang during Unassisted Winkle Entry: WINKLE_ENTRY_NOTIFY_PMC state
5	ROX	PCBS_WINKLE_ENTRY_SEND_INT_ASSIST_ERR: Hang during Assisted Winkle Entry: WINKLE_ENTRY_SEND_INT_ASSIST state
6	ROX	PCBS_WINKLE_EXIT_NOTIFY_PMC_ERR: Hang during Unassisted Winkle Exit: WINKLE_EXIT_NOTIFY_PMC state
7	ROX	PCBS_WAIT_DPLL_LOCK_ERR: Hang during Unassisted Exit waiting on DPLL: WAIT_DPLL_LOCK state
8	ROX	PCBS_SPARE8_ERR: spare bit, always 0
9	ROX	PCBS_WINKLE_EXIT_SEND_INT_ASSIST_ERR: Hang during Assisted Winkle Exit: WINKLE_EXIT_SEND_INT_ASSIST state
10	ROX	PCBS_WINKLE_EXIT_SEND_INT_POWUP_ASSIST_ERR: Hang during Assisted Winkle Exit: WINKLE_EXIT_SEND_INT_POWUP_ASSIST state
11	ROX	PCBS_WRITE_FSM_GOTO_REG_IN_INVALID_STATE_ERR: write to FSM goto register in invalid state
12	ROX	PCBS_WRITE_PMGP0_IN_INVALID_STATE_ERR: write to PMGP0 in invalid state

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Bits	PCB	Field Mnemonic: Description
13	ROX	PCBS_FREQ_OVERFLOW_IN_PSTATE_MODE_ERR: frequency of DPLL in Pstate mode overflows (Fnom + desired Pstate > 511)
14	ROX	PCBS_ECO_RS_BYPASS_CONFUSION_ERR: ECO railstepper tried to exit Vcs bypass and enter Vdd bypass in one Pstate step (it is not clear, in which order this strange operation should be performed - most likely it should never happen to avoid that Vcs is greater than Vdd)
15	ROX	PCBS_CORE_RS_BYPASS_CONFUSION_ERR: same as previous error, but for core railstepper (it is not clear, in which order this strange operation should be performed - most likely it should never happen to avoid that Vcs is greater than Vdd)
16	ROX	PCBS_READ_LPST_IN_PSTATE_MODE_ERR: read LPST-array while iVRM FSMs are enabled (dial ivrm_fsm_enable asserted)
17	ROX	PCBS_LPST_READ_CORR_ERR: correctable error occurred when reading the LPST
18	ROX	PCBS_LPST_READ_UNCORR_ERR: uncorrectable error occurred when reading the LPST
19	ROX	PCBS_PFET_STRENGTH_OVERFLOW_ERR: overflow occurred when calculating the pFET strength (in final rounding step!)
20	ROX	PCBS_VDS_LOOKUP_ERR: Vds entry not found in lookup table (when performing the linear search!)
21	ROX	PCBS_IDLE_INTERRUPT_TIMEOUT_ERR: idle interrupt timeout in PCB interrupt controller
22	ROX	PCBS_PSTATE_INTERRUPT_TIMEOUT_ERR: PState interrupt timeout in PCB interrupt controller
23	ROX	PCBS_GLOBAL_ACTUAL_SYNC_INTERRUPT_TIMEOUT_ERR: GlobalActualSync Interrupt timeout in PCB interrupt controller
24	ROX	PCBS_PMAX_SYNC_INTERRUPT_TIMEOUT_ERR: PmaxSync Interrupt timeout in PCB interrupt controller
25	ROX	PCBS_GLOBAL_ACTUAL_PSTATE_PROTOCOL_ERR: a write to global actual Pstate register has occurred before the global actual Pstate interrupt has left PCBS
26	ROX	PCBS_PMAX_PROTOCOL_ERR: a write to the Pmax/Pmin register has occurred before the Pmax sync interrupt has left PCB
27	ROX	PCBS_IVRM_GROSS_OR_FINE_ERR: iVRM gross or fine error (details to be found in PCBS_ivrm_Control_Status_Reg)
28	ROX	PCBS_IVRM_RANGE_ERR: iVRM range error (summary bit, details to be found in PCBS_ivrm_Control_Status_Reg)
29	ROX	PCBS_DPLL_CPM_FMIN_ERR: DPLL CPM Fmin error
30	ROX	PCBS_DPLL_DCO_FULL_ERR: DPLL DCO full
31	ROX	PCBS_DPLL_DCO_EMPTY_ERR: DPLL DCO empty
32	ROX	PCBS_DPLL_INT_ERR: DPLL internal error
33	ROX	PCBS_FMIN_AND_NOT_CPMBIT_ERR: dpll_fmin_and_not_cpmbit (ref. to dial cpm_fmin_clip_error_sel on how to configure this)
34	ROX	PCBS_DPLL_FASTER_THAN_FMAX_PLUS_DELTA1_ERR: dpll_faster_than_fmax_plus_delta1 (for characterization, delta1 is configurable with pll_char_delta1)
35	ROX	PCBS_DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2_ERR: dpll_slower_than_fmin_minus_delta2 (for characterization, delta2 is configurable with pll_char_delta2)
36	ROX	PCBS_RESCLK_CSB_INSTR_VECTOR_CHG_IN_INVALID_STATE_ERR: RESCLK CSB instruction vector change while FSMs none idle
37	ROX	PCBS_RESCLK_BAND_BOUNDARY_CHG_IN_INVALID_STATE_ERR: RESCLK Band boundaries change while FSMs none idle
38	ROX	PCBS_OCC_HEARTBEAT_LOSS_ERR: OCC heartbeat loss
39	ROX	PCBS_SPARE39_ERR: spare bit, always 0
40	ROX	PCBS_SPARE40_ERR: spare bit, always 0



Bits	PCB	Field Mnemonic: Description
41	ROX	PCBS_SPARE41_ERR: spare bit, always 0
42	ROX	PCBS_SPARE42_ERR: spare bit, always 0

Register Name	<i>PM Error Mask Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PMERRMASK_REG
Address	00000000160F010A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_HANG_ERR_MASK: Mask for this error: 1=masked, 0=not masked
1	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ASSIST_HANG_ERR_MASK: Mask for this error: 1=masked, 0=not masked
2	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
3	RW	PCBS_SLEEP_EXIT_INVOKE_PORE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
4	RW	PCBS_WINKLE_ENTRY_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
5	RW	PCBS_WINKLE_ENTRY_SEND_INT_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
6	RW	PCBS_WINKLE_EXIT_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
7	RW	PCBS_WAIT_DPLL_LOCK_ERR_MASK: Mask for this error: 1=masked, 0=not masked
8	RW	PCBS_SPARE8_ERR_MASK: Mask for this error: 1=masked, 0=not masked
9	RW	PCBS_WINKLE_EXIT_SEND_INT_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
10	RW	PCBS_WINKLE_EXIT_SEND_INT_POWUP_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
11	RW	PCBS_WRITE_FSM_GOTO_REG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
12	RW	PCBS_WRITE_PMGPO_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
13	RW	PCBS_FREQ_OVERFLOW_IN_PSTATE_MODE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
14	RW	PCBS_ECO_RS_BYPASS_CONFUSION_ERR_MASK: Mask for this error: 1=masked, 0=not masked
15	RW	PCBS_CORE_RS_BYPASS_CONFUSION_ERR_MASK: Mask for this error: 1=masked, 0=not masked
16	RW	PCBS_READ_LPST_IN_PSTATE_MODE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
17	RW	PCBS_LPST_READ_CORR_ERR_MASK: Mask for this error: 1=masked, 0=not masked
18	RW	PCBS_LPST_READ_UNCORR_ERR_MASK: Mask for this error: 1=masked, 0=not masked
19	RW	PCBS_PFET_STRENGTH_OVERFLOW_ERR_MASK: Mask for this error: 1=masked, 0=not masked
20	RW	PCBS_VDS_LOOKUP_ERR_MASK: Mask for this error: 1=masked, 0=not masked
21	RW	PCBS_IDLE_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
22	RW	PCBS_PSTATE_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
23	RW	PCBS_GLOBAL_ACTUAL_SYNC_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
24	RW	PCBS_PMAX_SYNC_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked

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Bits	PCB	Field Mnemonic: Description
25	RW	PCBS_GLOBAL_ACTUAL_PSTATE_PROTOCOL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
26	RW	PCBS_PMAX_PROTOCOL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
27	RW	PCBS_IVRM_GROSS_OR_FINE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
28	RW	PCBS_IVRM_RANGE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
29	RW	PCBS_DPLL_CPM_FMIN_ERR_MASK: Mask for this error: 1=masked, 0=not masked
30	RW	PCBS_DPLL_DCO_FULL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
31	RW	PCBS_DPLL_DCO_EMPTY_ERR_MASK: Mask for this error: 1=masked, 0=not masked
32	RW	PCBS_DPLL_INT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
33	RW	PCBS_FMIN_AND_NOT_CPMBIT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
34	RW	PCBS_DPLL_FASTER_THAN_FMAX_PLUS_DELTA1_ERR_MASK: Mask for this error: 1=masked, 0=not masked
35	RW	PCBS_DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2_ERR_MASK: Mask for this error: 1=masked, 0=not masked
36	RW	PCBS_RESCLK_CSB_INSTR_VECTOR_CHG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
37	RW	PCBS_RESCLK_BAND_BOUNDARY_CHG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
38	RW	PCBS_OCC_HEARTBEAT_LOSS_ERR_MASK: Mask for this error: 1=masked, 0=not masked
39	RW	PCBS_SPARE39_ERR_MASK: Mask for this error: 1=masked, 0=not masked
40	RW	PCBS_SPARE40_ERR_MASK: Mask for this error: 1=masked, 0=not masked
41	RW	PCBS_SPARE41_ERR_MASK: Mask for this error: 1=masked, 0=not masked
42	RW	PCBS_SPARE42_ERR_MASK: Mask for this error: 1=masked, 0=not masked

Register Name		PM Special Wakeup FSP
Mnemonic		EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PMSPCWKUPFSP_REG
Address		00000000160F010B (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RW	FSP_SPECIAL_WAKEUP: Chiplet Special Wakeup for FSP Firmware use. NOTE: protocol is required when setting this bit

Register Name		PM Special Wakeup OCC
Mnemonic		EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PMSPCWKUPOCC_REG
Address		00000000160F010C (PCB)
Attributes		
Description		



Bits	PCB	Field Mnemonic: Description
0	RW	OCC_SPECIAL_WAKEUP: Chiplet Special Wakeup for OCC Firmware use. NOTE: protocol is required when setting this bit

Register Name	<i>PM Special Wakeup Hypervisor</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PMSPCWKUPPHYP_REG
Address	00000000160F010D (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	PHYP_SPECIAL_WAKEUP: Chiplet Special Wakeup for hypervisor Firmware use. NOTE: protocol is required when setting this bit

Register Name	<i>PFET Control/Status Register For Core And ECO Vcs</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PFVCS_CNTLSTAT_REG
Address	00000000160F010E (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	CORE_VCS_PFET_FORCE_STATE: Core Domain PFET Force State Provides a means for firmware to force the core domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 4:5 = 00 (both core_vcs_pfet_val_override AND core_vcs_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
2:3	RW	ECO_VCS_PFET_FORCE_STATE: ECO Domain PFET Force State Provides a means for firmware to force the ECO domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 6:7 = 00 (both eco_vcs_pfet_val_override AND eco_vcs_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
4	RW	CORE_VCS_PFET_VAL_OVERRIDE: Core Domain PFET Value Override 0 = Override is disabled
5	RW	CORE_VCS_PFET_SEL_OVERRIDE: Core Domain PFET Stage Select Override 0 = Override is disabled
6	RW	ECO_VCS_PFET_VAL_OVERRIDE: ECO Domain PFET Value Override 0 = Override is disabled
7	RW	ECO_VCS_PFET_SEL_OVERRIDE: ECO Domain PFET Stage Select Override 0 = Override is disabled

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Bits	PCB	Field Mnemonic: Description
8	RW	CORE_VCS_PFET_ENABLE_REGULATION_FINGER: Core Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the core_vcs_pfet_enable_value.
9	RW	ECO_VCS_PFET_ENABLE_REGULATION_FINGER: ECO Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the eco_vcs_pfet_enable_value.
10:21	RW	CORE_VCS_PFET_ENABLE_VALUE: Core PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the Core Domain PFET Enables directly. If core_vcs_pfet_val_override = 1, a write to this field sets the state of the core PFET Enables until core_vcs_pfet_val_override is cleared. If core_vcs_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the core_vcs_pfet_valN_slav registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
22:25	RW	CORE_VCS_PFET_SEL_VALUE: Core PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure core_vcs_pfet_valN_slav(0:11) where N is 0 to 11 if core_vcs_pfet_sel_override = 1. If core_vcs_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
26:37	RW	ECO_VCS_PFET_ENABLE_VALUE: ECO PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the ECO PFET Enables directly. If ECO_vcs_pfet_val_override = 1, a write to this field sets the state of the ECO PFET Enables until ECO_vcs_pfet_val_override is cleared. If eco_vcs_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the eco_vcs_pfet_valN_slav registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
38:41	RW	ECO_VCS_PFET_SEL_VALUE: ECO PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure eco_vcs_pfet_valN_slav(0:11) where N is 0 to 11 if eco_vcs_pfet_sel_override = 1. If eco_vcs_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
42:45	ROX	CORE_VCS_PG_STATE: Core power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
46:49	ROX	CORE_VCS_PG_SEL: For debug, contains the actual index n into Core Domain PFET Value [n] SLAT Register set that contains the Core PFET Enable Value currently enabled.
50:53	ROX	ECO_VCS_PG_STATE: ECO Domain power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
54:57	ROX	ECO_VCS_PG_SEL: For debug, contains the actual index n into ECO Domain PFET Value [n] SLAT Register set that contains the ECO PFET Enable Value currently enabled.



Register Name	<i>PM State History Register For Hypervisor</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPHYP_REG
Address	00000000160F0110 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	PHYP_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	PHYP_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	PHYP_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	PHYP_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	PHYP_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	PHYP_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For FSP</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PMSTATEHISTFSP_REG
Address	00000000160F0111 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	FSP_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	FSP_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	FSP_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	FSP_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.

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Bits	PCB	Field Mnemonic: Description
6	ROX_CLRPAR T	FSP_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	FSP_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For OCC</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PMSTATEHISTOCC_REG
Address	00000000160F0112 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	OCC_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	OCC_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	OCC_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	OCC_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	OCC_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	OCC_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For PerfMon</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPERF_REG
Address	00000000160F0113 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	PERF_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	PERF_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	PERF_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	PERF_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	PERF_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	PERF_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM FSM Reset And Babystepper Idle Injects</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.IDLEFSMGOTOCMD_REG
Address	00000000160F0114 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	WO_1P	idle_fsm_goto_cmd ' A write to this reg will proceed the IDLE FSM from WAIT_FOR_PORE_DONE, SLEEP_EXIT_WAIT_FOR_PORE_FAST_EXIT_DONE, or WINKLE_EXIT_WAIT_FOR_PORE_FAST_EXIT_DONE to the following states: ' 0b01: goto IDLE state ' 0b10: goto SLEEP_EXIT_CORE_MESHLET_ON state ' 0b11: goto WINKLE_EXIT_NOTIFY_PMC state ' "
2	RWX	babystp_trigger_sleep_entry ' A write to this reg with a 1 in this field will cause the babystepper to run the sleep entry sequence. This step is needed for an assisted entry into sleep, before the power is actually turned off since the babystepper needs to know about the sleep state. For an unassisted entry, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished entering its sleep mode. ' "
3	RWX	babystp_trigger_winkle_entry ' A write to this reg with a 1 in this field will cause the babystepper to run the winkle entry sequence. This step is needed for an assisted entry into winkle before the power is actually turned off since the babystepper needs to know about the winkle state. For an unassisted entry, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished entering its winkle mode. ' "
4	RWX	babystp_trigger_wakeup ' A write to this reg with a 1 in this field will cause the babystepper to run the wakeup sequence from sleep/winkle depending on the babystepper state of sleep or winkle. This step is needed for an assisted exit from winkle before the power is actually turned off since the babystepper needs to know about the wakeup state. For an unassisted exit, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished waking up from sleep or winkle. ' "

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Register Name	Core PFET Power Up Delay
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.COREPFPUDLY_REG
Address	00000000160F012C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_POWUP_DLY0: Delay used after transitioning to Core Domain power up sequence stage0. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	CORE_POWUP_DLY1: Delay used after transitioning to Core domain power up sequence stage1.
8:19	RW	CORE_POWER_UP_DELAY_SEL: Vector select for which delay to use for the respective power-up stage. Bit mapping: 8 -> core_*_pfet_enable(0) 9 -> core_*_pfet_enable(1) ... 19 -> core_*_pfet_enable(11) Bit meaning: 0 = Use core_powup_dly0 1 = Use core_powup_dly1

Register Name	Core PFET Power Down Delay
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.COREPFPDDLY_REG
Address	00000000160F012D (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_POWDN_DLY0: Delay used after transitioning to Core domain power dn sequence stage1. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	CORE_POWDN_DLY1: Delay used after transitioning to Core domain power dn sequence stage1. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
8:19	RW	CORE_POWER_DN_DELAY_SEL: Vector select for which delay to use for the respective power-dn stage. Bit mapping: 8 -> core_*_pfet_enable(0) 9 -> core_*_pfet_enable(1) ... 19 -> core_*_pfet_enable(11) Bit meaning: 0 = Use core_powdn_dly0 1 = Use core_powdn_dly1



Register Name	Core PFET Vretention	
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.COREPFVRET_REG	
Address	00000000160F0130 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_VRET_SEL: Pointer to the stage representing the Vretention value for the core PFETs. Power down sequences will stop after enabling this stage.
4:7	RW	CORE_VOFF_SEL: Pointer to the stage representing the Voff value for the core PFETs. Power down sequences will stop after enabling this stage.

Register Name	ECO PFET Power Up Delay	
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.ECOPFPUDLY_REG	
Address	00000000160F014C (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_POWUP_DLY0: Delay used after transitioning to ECO domain power up sequence stage0 in terms of refclk period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	ECO_POWUP_DLY1: Delay used after transitioning to ECO domain power up sequence stage1.
8:19	RW	ECO_POWER_UP_DELAY_SEL: Vector select for which delay to use for the respective power-up stage. Bit mapping: 8 -> eco_*_pfet_enable(0) 9 -> eco_*_pfet_enable(1) ... 19 -> eco_*_pfet_enable(11) Bit meaning: 0 = Use eco_powup_dly0 1 = Use eco_powup_dly1

Register Name	ECO PFET Power Down Delay	
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.ECOPFPDDLY_REG	
Address	00000000160F014D (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_POWDN_DLY0: UNUSED/SPARE
4:7	RW	ECO_POWDN_DLY1: Delay used after transitioning to ECO Domain power dn sequence stage1. The delays in this register are in terms of refclk period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.

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Bits	PCB	Field Mnemonic: Description
8:19	RW	ECO_POWER_DN_DELAY_SEL: Vector select for which delay to use for the respective power-down stage. Bit mapping: 8 -> eco_*_pfet_enable(0) 9 -> eco_*_pfet_enable(1) ... 19 -> eco_*_pfet_enable(11) Bit meaning: 0 = Use eco_powdn_dly0 1 = Use eco_powdn_dly1

Register Name		<i>ECO PFET Vretention</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.ECOPFVRET_REG
Address		00000000160F0150 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_VRET_SEL: Pointer to the stage representing the Vretention value for the ECO PFETs. Power down sequences will stop after enabling this stage.
4:7	RW	ECO_VOFF_SEL: Pointer to the stage representing the Voff value for the ECO PFETs. Power down sequences will stop after enabling this stage.

Register Name		<i>Frequency Control Register With Overrides For DPLL</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.FREQ_CTRL_REG
Address		00000000160F0151 (PCB)
Attributes		
Description		Note that overrides to Dpll_fmax are only applied if Dpll_freq_override_enable = 1. A read of all these dials always returns the currently established DPLL frequencies (regardless of any other mode settings).
Bits	PCB	Field Mnemonic: Description
0:8	RWX	DPLL_FMIN: minimum DPLL frequency in CPM-DPLL mode that is set at IPL time A read always returns the currently established value A write is not conditioned on any other dial setting.
9:17	RWX	DPLL_FMAX: DPLL maximum frequency and frequin (these two values are the same in POWER8 processor) without applying bias values: A read always returns the currently established value A write is conditioned on the setting of dpll_freq_override_enable. If dpll_freq_override_enable is asserted, a write causes this field to update. Otherwise the hardware (that is, PStates) are controlling the update of this value.
18:21	RO	Reserved.
22:30	RW	FREQU_AT_PSTATE0: DPLL frequency for Pstate 0



Register Name	<i>DPLL Mode Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.DPLL_CPM_PARM_REG
Address	00000000160F0152 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	LF_SLEWRATEXPI: out of lock slew rate for DPLL
8	RW	LF_USE_CPMXPI: use CPM instead of PFD as loop filter input, if '1' (instead of using both)
9	RW	FF_USE_CPMXPI: use the CPM inputs for the frequency filter, if '1'
10	RW	CPM_FILTER_ENABLE: enables the CPM filter
11	RW	FF_BYPASSXPI: enables frequency filter bypass
12	RW	DCO_OVERRIDE: enables overrides for DCO testing/characterization
13	RW	DCO_INCR: enables increment for DCO testing/characterization, increments only on a rising edge
14	RW	DCO_DECR: enables decrement for DCO testing/characterization, decrements only on a rising edge
15:23	RW	DPLL_LOCK_TIMER_REPLACEMENT_VALUE: if dpll_lock_replacement_timer_mode_en is set, this dial specifies the delay in us, after which it is assumed, that the DPLL has reached a frequency lock condition. Note that values less than 3 will cause in undefined HW behavior (0 will cause HANGs!). if dpll_lock_replacement_timer_mode_en is zero, this dial specifies the delay in pcb_nclk cycles after which the hardware monitors the DPLL frequout output (if dpll_freqout_mode_en is set) or the DPLL flock output (if dpll_flock_mode_en is set). Note that in this case, the value of this dial needs to be greater or equal to 150 (decimal).
24:31	RW	PRE_VRET_PSTATE: Pstate that is stepped to before switching to Vretention defined in PCBS_iVRM_Control_Status_Reg
32	RW	OVERRIDE_PCBS_DPLL_SYNCHRONIZER: Bypasses the 'ping-pong' synchronization logic between the DPLL and the PCBS-PM. NEVER SET TO 1 UNLESS YOU KNOW WHAT YOU ARE DOING!
33:36	RW	DPLL_CHAR_DELTA1: Delta in DPLL ticks for characterization (cf. dial dpll_faster_than_fmax_plus_delta1)
37:40	RW	DPLL_CHAR_DELTA2: Delta in DPLL ticks for characterization (cf. dial dpll_faster_than_fmin_minus_delta2)

Register Name	<i>PPMSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_STATUS_REG
Address	00000000160F0153 (PCB)
Attributes	
Description	The PPMSR provides read access to the power management status that is also shadowed to the PC and visible to the pHyp in the PMSR (with some delay due to the shadowing process).

Bits	PCB	Field Mnemonic: Description
0:7	ROX	global_pstate_actual ' Actual Global Pstate Pstate or Pglobal_actual' " Reads from this field return the presently established global PState value.' " "Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent '

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Bits	PCB	Field Mnemonic: Description
8:15	ROX	LOCAL_PSTATE_ACTUAL: ' Actual Local PState or Plocal_actual' " 'Reads from this field return the presently established local PState value. This value will always be less than or equal to global_pstate_actual.' " 'Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent' "
16:23	ROX	pv_min Minimum Pstate set by the platform.
24:31	ROX	pvf_max Maximum Pstate set by the platform.
32	ROX	spr_em_disabled ' SPR Energy Management Disabled' 'Read from this field indicate whether the platform has disabled the ' 'PMCR and PMICR SPRs to control the chiplet PState. '
33	ROX	Psafe_mode_active Read from this field indicate whether the chiplet has been put into a safe mode with Psafe enabled to a OCC heartbeat loss or other externally forced reasons (0=regular mode, 1=safe mode is active)
34	ROX	iVRM_safe_mode_active Read from this field indicate whether the chiplet has been put the iVRM safe mode (forcing the bypass mode for all iVRMs)
35	ROX	ivrm_enable Read from this field indicate whether the chiplet internal voltage regulation macro is enabled for localized voltage control (0=disabled, 1=enabled) based on ANDing the poweron signals to the iVRMs
36	ROX	all_fsms_in_safe_state For recovery: if this bit is asserted, all Pstate and iVRM control FSMs are in a stable, safe state that allows the recovery routine to proceed with resetting the PCBS PM without the risk of interrupt a critical action
37:40	ROX	pmsr_spares spare bits

Register Name	<i>PIVRMCSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_CONTROL_STATUS_REG
Address	00000000160F0154 (PCB)
Attributes	
Description	The PIVRMCSR provides access to chiplet-level controls of the internal VRM rail set (VDD and VCS) across both the core and ECO domains. The following is valid only for bits 4 to 7: when in automatic iVRM mode (ivrm_fsm_enable=1), these bits provide access to the values established by the automatic hardware mechanism. When In iVRM override mode (ivrm_fsm_enable=0), these bits allow firmware direct control of the values driving the internal VRMs.

Bits	PCB	Field Mnemonic: Description
0	RW	IVRM_FSM_ENABLE: Internal master VRM FSM Enable 0 = Disable Internal VRM FSMs and enable to control the iVRMs with the available override registers (SCOMable) as a backup mode or for setup (override mode) 1 = Enable Internal VRM FSM sequencers (requires that Pstates are enabled with enable_Pstate_mode=1 as well) (automatic mode)
1	RW	USE_IVRM_FOR_VRET: Internal VRM Enabled for Vretention 0 = Disable Internal VRM for Vretention 1 = Enable Internal VRM for Vretention
2	RW	BINSEARCH_CAL_ENA: trigger binary search (level signal)

Bits	PCB	Field Mnemonic: Description
3	RW	PVREF_EN: Internal VRM Power Voltage Reference Forced Enable 0 = Allow hardware to enable/disable pvref circuit 1 = Force enablement of the pvref circuit
4	RWX	IVRM_CORE_VDD_BYPASS_B: Internal VRM Core VDD Bypass (negative active) 0 = VDD Internal Core VRMs in bypass 1 = VDD internal Core VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
5	RWX	IVRM_CORE_VDD_POWERON: Internal VRM Core VDD Poweron 0 = Core VDD Internal VRMs powered off 1 = Core VDD internal VRMs powered on if this bit is not set (=0), the Core VDD internal VRM powered off internally. If this bit is set (=1), the Core VDD internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
6	RWX	IVRM_CORE_VCS_BYPASS_B: Internal VRM Core VCS Bypass (negative active) 0 = VCS Internal Core VRMs in bypass 1 = VCS internal Core VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VCS internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VCS internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
7	RWX	IVRM_CORE_VCS_POWERON: Internal VRM Core VCS Poweron 0 = Core VCS Internal VRMs powered off 1 = Core VCS internal VRMs powered on if this bit is not set (=0), the Core VCS internal VRM powered off internally. If this bit is set (=1), the Core VCS internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
8	RWX	IVRM_ECO_VDD_BYPASS_B: Internal VRM ECO VDD Bypass (negative active) 0 = VDD Internal ECO VRMs in bypass 1 = VDD internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
9	RWX	IVRM_ECO_VDD_POWERON: Internal VRM ECO VDD Bypass (negative active) 0 = VDD Internal ECO VRMs in bypass 1 = VDD internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.

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Bits	PCB	Field Mnemonic: Description
10	RWX	IVRM_ECO_VCS_BYPASS_B: Internal VRM ECO VCS Bypass (negative active) 0 = VCS Internal ECO VRMs in bypass 1 = VCS internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VCS internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VCS internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
11	RWX	IVRM_ECO_VCS_POWERON: Internal VRM ECO VCS Poweron 0 = ECO VCS Internal VRMs powered off 1 = ECO VCS internal VRMs powered on if this bit is not set (=0), the ECO VCS internal VRM powered off internally. If this bit is set (=1), the ECO VCS internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
12:18	RWX	IVRM_VRET_VDD: if use_ivrm_for_Vret is asserted, this dial is used to control the Vdd retention voltage. Note: this field will establish the Core VDD rail for Sleep and both the Core and ECO rail for Winkle. - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
19:25	RWX	IVRM_VRET_VCS: if use_ivrm_for_Vret is asserted, this dial is used to control the Vcs retention voltage. Note: this field will establish the Core VDD rail for Sleep and both the Core and ECO rail for Winkle. - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
26:30	RWX	IVRM_VRET_CORE_VDD_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the Core Vdd iVRM PFET strength for the retention voltage
31:35	RWX	IVRM_VRET_CORE_VCS_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the Core Vcs iVRM PFET strength for the retention voltage
36:40	RWX	IVRM_VRET_ECO_VDD_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the ECO Vdd iVRM PFET strength for the retention voltage
41:45	RWX	IVRM_VRET_ECO_VCS_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the ECO Vcs iVRM PFET strength for the retention voltage
46	RW	PVREF_FAIL: voltage reference fail input to iVRMs
47	ROX	IVRM_PREF_ERROR_GROSS: Voltage Reference Gross Error 0 = Gross Error not detected 1 = Gross Error detected
48	ROX	IVRM_PREF_ERROR_FINE: Voltage Reference Fine Error 0 = Fine Error not detected 1 = Fine Error detected
49	ROX	IVRM_CORE_VDD_RANGE_HI: Core VDD Internal VRM Range Hi Indicator 0 = Core VDD Internal VRM Hi indicator signal not asserted 1 = Core VDD internal VRMs Hi indicator signal asserted
50	ROX	IVRM_CORE_VDD_RANGE_LO: Core VDD Internal VRM Range Low Indicator 0 = Core VDD Internal VRM Low indicator signal not asserted 1 = Core VDD internal VRMs Low indicator signal asserted



Bits	PCB	Field Mnemonic: Description
51	ROX	IVRM_ECO_VDD_RANGE_HI: ECO VDD Internal VRM Range Hi Indicator 0 = ECO VDD Internal VRM Hi indicator signal not asserted 1 = ECO VDD internal VRMs Hi indicator signal asserted
52	ROX	IVRM_ECO_VDD_RANGE_LO: ECO VDD Internal VRM Range Low Indicator 0 = ECO VDD Internal VRM Low indicator signal not asserted 1 = ECO VDD internal VRMs Low indicator signal asserted
53	ROX	IVRM_CORE_VCS_RANGE_HI: Core VCS Internal VRM Range Hi Indicator 0 = Core VCS Internal VRM Hi indicator signal not asserted 1 = Core VCS internal VRMs Hi indicator signal asserted
54	ROX	IVRM_CORE_VCS_RANGE_LO: Core VCS Internal VRM Range Low Indicator 0 = Core VCS Internal VRM Low indicator signal not asserted 1 = Core VCS internal VRMs Low indicator signal asserted
55	ROX	IVRM_ECO_VCS_RANGE_HI: ECO VCS Internal VRM Range Hi Indicator 0 = ECO VCS Internal VRM Hi indicator signal not asserted 1 = ECO VCS internal VRMs Hi indicator signal asserted
56	ROX	IVRM_ECO_VCS_RANGE_LO: ECO VCS Internal VRM Range Low Indicator 0 = ECO VCS Internal VRM Low indicator signal not asserted 1 = ECO VCS internal VRMs Low indicator signal asserted
57	ROX	BINSEARCH_CAL_DONE: binary search done signal
58	RWX	IVRM_CORE_VDD_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
59	RWX	IVRM_CORE_VCS_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
60	RWX	IVRM_ECO_VDD_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
61	RWX	IVRM_ECO_VCS_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
62	RW	IVRM_POWER_DOWN_DISABLE: If this bit is 1, the iVRM poweron signal is left asserted. Power off of the iVRMs is then blocked

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Register Name	PIVRMVSR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VALUE_SETTING_REG
Address	00000000160F0155 (PCB)
Attributes	
Description	The PIVRMVSR allows access to VID values and PFET strength valid signal settings presented to the internal VRM rail set (VDD and VCS) across both the core and ECO domains. When in <code>ivrm_fsm_enable = "auto"</code> mode, this register provides access to the values established by the automatic hardware mechanism. When <code>ivrm_fsm_enable = "override"</code> mode, this register allows firmware direct control of the values driving the internal VRMs which, if the VRMs are not in bypass, will move the voltage settings.

Bits	PCB	Field Mnemonic: Description
0:7	RWX	IVRM_CORE_VDD_IVID: When read, returns the value presently being driving to the Core VDD iVRM. If <code>ivrm_fsm_enable = 0</code> (<code>override_mode</code>), then writes to this field will drive a new VID value to the Core VDD iVRM. If <code>ivrm_fsm_enable = 1</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
8:15	RWX	IVRM_CORE_VCS_IVID: When read, returns the value presently being driving to the Core VCS iVRM. If <code>ivrm_fsm_enable = 0</code> (<code>override_mode</code>), then writes to this field will drive a new VID value to the Core VCS iVRM. If <code>ivrm_fsm_enable = 1</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
16:23	RWX	IVRM_ECO_VDD_IVID: When read, returns the value presently being driving to the Core VDD iVRM. If <code>ivrm_fsm_enable = 0</code> (<code>override_mode</code>), then writes to this field will drive a new VID value to the ECO VDD iVRM. If <code>ivrm_fsm_enable = 1</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
24:31	RWX	IVRM_ECO_VCS_IVID: When read, returns the value presently being driving to the ECO VCS iVRM. If <code>ivrm_fsm_enable = 0</code> (<code>override_mode</code>), then writes to this field will drive a new VID value to the ECO VCS iVRM, If <code>ivrm_fsm_enable = 0</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
32:36	RWX	IVRM_CORE_VDD_PFET_STRENGTH: When read, returns the value presently being driving to the core VCS iVRM. If <code>ivrm_fsm_enable = 0</code> (<code>override_mode</code>), then writes to this field will drive a new strength value to the core VCS iVRM, If <code>ivrm_fsm_enable = 0</code> , writes to this field are not performed.

Bits	PCB	Field Mnemonic: Description
37:41	RWX	IVRM_CORE_VCS_PFET_STRENGTH: This register is assigned to the signals tcex##_tp_ivrm_core_vcs_sense & tcex##_tp_ivrm_core_vdd_sense & tcex##_tp_ivrm_eco_vcs_sense & tcex##_tp_ivrm_eco_vdd_sense & 0b0 Note that all other sense signals are spares now and tied to 0. OUTDATED TEXT: When read, returns the value presently being driving to the core VDD iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the core VDD iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
42:46	RWX	IVRM_ECO_VDD_PFET_STRENGTH: When read, returns the value presently being driving to the ECO VCS iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the ECO VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
47:51	RWX	IVRM_ECO_VCS_PFET_STRENGTH: When read, returns the value presently being driving to the ECO VDD iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the ECO VDD iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
52	RWX	IVRM_VDD_CORE_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the Core VDD iVRM. If ivrm_fsm_enable = 1 AND ivrm_control_mode = 1 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the Core VDD iVRM, If ivrm_fsm_enable = 0 OR ivrm_control_mode = 0, writes to this field are not performed.
53	RWX	IVRM_VCS_CORE_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the Core VCS iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the Core VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
54	RWX	IVRM_VDD_ECO_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the ECO VDD iVRM. If ivrm_fsm_enable = 1 AND ivrm_control_mode = 1 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the ECO VDD iVRM, If ivrm_fsm_enable = 0 OR ivrm_control_mode = 0, writes to this field are not performed.
55	RWX	IVRM_VCS_ECO_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the ECO VCS iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the ECO VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
56	RWX	CORE_VDD_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
57	RWX	CORE_VCS_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
58	RWX	ECO_VDD_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
59	RWX	ECO_VCS_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.

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Register Name		General PCBS Modes And Chicken Switches
Mnemonic		EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBSPM_MODE_REG
Address		00000000160F0156 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RW	ENABLE_PSTATE_MODE: if asserted, Pstate requests (from overrides or PMCR) will be honored, otherwise, the hardware does not do anything. Note to firmware: this is the master switch for Pstates and should be asserted after all sub-modes (that is, lvrn_fsm_en) are setup to avoid enabling unintentional modes during the mode setup.
1	RW	GLOBAL_PSTATE_CHANGE_FOR_IDLE_STATE_ENABLED: if asserted, a global Pstate change to the Nap/Sleep/Winkle-Pstate is requested, when the Nap/Sleep/Winkle state is entered and the individual enable bits in the PIMCR are asserted
2	RW	ENABLE_GLOBAL_PSTATE_REQ: if '1' then enable PMC interrupt with global Pstate change request, otherwise, disable global requests
3	RW	ENABLE_WINKLE_WITH_CPM_MODE: if '1', PCBS automatically changes the DPLL mode to mode 1, when entering winkle, but changes the mode back to CPM mode when exiting. Needed for CPM-DPLL control loop enablement.
4	RW	ENABLE_CLIPPING_OF_GLOBAL_PSTATE_REQ: if '1', PCBS automatically clips global Pstate requests with Pvf_max in PPMBR and sets the 'donate' bit in the interrupt accordingly
5	RW	CHKSW_HW214553: if deasserted, HW214553 (frequin issue in resclk mode) is fixed, if asserted, the fix is not active
6	RW	ENABLE_PMC_PMAX_SYNC_NOTIFICATION: if asserted, the PCBS-PM will send a 'Pmax_sync' interrupt, once the synchronization criterion is met
7	RW	DPLL_LOCK_REPLACEMENT_TIMER_MODE_EN: Select a timer instead of the DPLL lock bit as target frequency reached criterion. This timer has to be setup by the dial dpll_lock_timer_replacement_value. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
8	RW	DPLL_FREQOUT_MODE_EN: Looks at the DPLL frequout to find out, if the target frequency has been reached. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
9	RW	DPLL_FLOCK_MODE_EN: Looks at the real DPLL flock output to find out, if the target frequency has been reached. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
10	RW	ENABLE_SENSE_DELAY_CHARACTERIZATION: If this switch is 0, the sense latches are updated every cycle. If this switch is 1, the sense delay measurement mode is enabled, that starts a sense delay timer, whenever one of the registers that drive the inputs of the iVRMs/pFETs is written via PCB and that triggers a sense register freeze operation, when the sense delay timer reaches the value sense_delay_timer_val. With this mode, the sense delays can be measured in multiples of the PCB-slave clock speed.
11:17	RW	SENSE_DELAY_TIMER_VAL: See the description of enable_sense_delay_characterization for details.
18:19	RW	CPM_FMIN_CLIP_ERROR_SEL: This dial selects, which of the following conditions will cause the FIR bit dpll_fmin_and_not_cpmbit to be set to detect, that the DPLL runs at Fmin, but is still clipped by the CPMs. 0b00 = function is disabled 0b01 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit2 = 0 0b10 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit1 = 0 0b11 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit0 = 0
20:23	RW	DBG_TRACE_SEL: This dial selects the group of signals to be traced for debug in the lab. Details to be found in the Section 'Trace Bus'

Bits	PCB	Field Mnemonic: Description
24:25	RW	TRACE_DATA_SEL: This dial selects the group of signals to be traced for debug in the lab. Details to be found in the Section 'Trace Bus'
26:29	RW	TP_CPLT_IVRM_VPP_TUNE: Tune bits to be set going to the iVRMs

Register Name	<i>PIVRMPS Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_PFETSTR_SENSE_REG
Address	00000000160F0157 (PCB)
Attributes	
Description	This PIVRMPS is used to check that the pFET sense outputs correspond to the driven values (mainly for test).

Bits	PCB	Field Mnemonic: Description
0:4	ROX	IVRM_CORE_VDD_PFETSTR_SNS: Not used any more.
5:9	ROX	IVRM_CORE_VCS_PFETSTR_SNS: This register is assigned to the signals tcex##_tp_ivrm_core_vcs_sense & tcex##_tp_ivrm_core_vdd_sense & tcex##_tp_ivrm_eco_vcs_sense & tcex##_tp_ivrm_eco_vdd_sense & 0b0
10:14	ROX	IVRM_ECO_VDD_PFETSTR_SNS: Not used any more.
15:19	ROX	IVRM_ECO_VCS_PFETSTR_SNS: Not used any more.
20	ROX	IVRM_VDD_CORE_PFETSTR_VALID_SNS: Not used any more.
21	ROX	IVRM_VCS_CORE_PFETSTR_VALID_SNS: Not used any more.
22	ROX	IVRM_VDD_ECO_PFETSTR_VALID_SNS: Not used any more.
23	ROX	IVRM_VCS_ECO_PFETSTR_VALID_SNS: Not used any more.
24	ROX	CORE_VDD_BYPASS_B_SENSE: Not used any more.
25	ROX	CORE_VCS_BYPASS_B_SENSE: Not used any more.
26	ROX	ECO_VDD_BYPASS_B_SENSE: Not used any more.
27	ROX	ECO_VCS_BYPASS_B_SENSE: Not used any more.
28	ROX	CORE_VDD_POWERON_SENSE: Not used any more.
29	ROX	CORE_VCS_POWERON_SENSE: Not used any more.
30	ROX	ECO_VDD_POWERON_SENSE: Not used any more.
31	ROX	ECO_VCS_POWERON_SENSE: Not used any more.
32	ROX	CORE_VDD_VPUMP_EN_SENSE: Not used any more.
33	ROX	CORE_VCS_VPUMP_EN_SENSE: Not used any more.
34	ROX	ECO_VDD_VPUMP_EN_SENSE: Not used any more.
35	ROX	ECO_VCS_VPUMP_EN_SENSE: Not used any more.
36	ROX	CORE_VDD_PFET_LOW_VOUT_SNS: Not used any more.
37	ROX	CORE_VCS_PFET_LOW_VOUT_SNS: Not used any more.
38	ROX	ECO_VDD_PFET_LOW_VOUT_SNS: Not used any more.
39	ROX	ECO_VCS_PFET_LOW_VOUT_SNS: Not used any more.

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Register Name	PPMICR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_IDLE_CONTROL_REG
Address	00000000160F0158 (PCB)
Attributes	
Description	The PPMICR is used to read the PMICR register typically owned (written) by the hypervisor. Writes are conditioned on the setting of the dial Pm_spr_override_en. If Pm_spr_override_en is set, firmware needs to make sure that the special wakeup state of this chiplet is reached before changing any of the latency fields in this register. Otherwise, the hardware behavior is undefined.

Bits	PCB	Field Mnemonic: Description
0:7	ROX	NAP_PSTATE_REQ: Nap Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
8	ROX	NAP_PSTATE_EN: Nap PState Enable 1 = Enable the Nap Pstate (NPS) Request, Nap Global Enable and Nap Latency functions 0 = Disables the Nap Pstate (NPS) Request, Nap Global Enable and Nap Latency functions Reads from the field return the value last written.
9	ROX	NAP_GLOBAL_EN: Nap Global Enable 1 = Upon the execution of a Nap instruction , the Nap Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a Nap instruction , the Nap Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.
10:11	ROX	NAP_LATENCY: Nap Latency not supported for POWER8 processor
12:15	ROX	RESERVED_PPMICR_0: reserved
16:23	ROX	SLEEP_PSTATE_REQ: sleep Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
24	ROX	SLEEP_PSTATE_EN: sleep PState Enable 1 = Enable the sleep Pstate (NPS) Request, sleep Global Enable and sleep Latency functions 0 = Disables the sleep Pstate (NPS) Request, sleep Global Enable and sleep Latency functions Reads from the field return the value last written.
25	ROX	SLEEP_GLOBAL_EN: sleep Global Enable 1 = Upon the execution of a sleep instruction , the sleep Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a sleep instruction , the sleep Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.

Bits	PCB	Field Mnemonic: Description
26:27	ROX	SLEEP_LATENCY: sleep Latency 00 = Cease instructions and honors Pstate change but does not perform additional state changing actions (unsupported in POWER8, maps to 0b10) 01 = Indicates to the platform that a sub-state that would have the lowest latency is enabled (unsupported in POWER8, maps to 0b10) 10 = Indicates to the platform that a sub-state that might have a medium exit latency is enabled (POWER8: Fast Sleep) 11 = Indicates to the platform that a sub-state that might have higher exit latency is enabled (POWER8: Deep Sleep)
28:31	ROX	RESERVED_PPMICR_1: reserved
32:39	ROX	WINKLE_PSTATE_REQ: winkle Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
40	ROX	WINKLE_PSTATE_EN: winkle PState Enable 1 = Enable the winkle Pstate (NPS) Request, winkle Global Enable and winkle Latency functions 0 = Disables the winkle Pstate (NPS) Request, winkle Global Enable and winkle Latency functions Reads from the field return the value last written.
41	ROX	WINKLE_GLOBAL_EN: winkle Global Enable 1 = Upon the execution of a winkle instruction , the winkle Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a winkle instruction , the winkle Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.
42:43	ROX	WINKLE_LATENCY: winkle Latency 00 = Cease instructions and honors Pstate change but does not perform additional state changing actions (unsupported in POWER8, maps to 0b10) 01 = Indicates to the platform that a sub-state that would have the lowest latency is enabled (unsupported in POWER8, maps to 0b10) 10 = Indicates to the platform that a sub-state that might have a medium exit latency is enabled (POWER8: Fast Winkle) 11 = Indicates to the platform that a sub-state that might have higher exit latency is enabled (POWER8: Deep Winkle)
44:47	ROX	RESERVED_PPMICR_2: reserved

Register Name	PPMCR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_CONTROL_REG
Address	00000000160F0159 (PCB)
Attributes	
Description	The PPMCR provides read access to the PMCR register shadow in the PCBS typically owned (written) by the hypervisor. Writes are conditioned on the setting of PMGP1[pm_spr_override_en].

Bits	PCB	Field Mnemonic: Description
0:7	RWX	GLOBAL_PSTATE_REQ: global Pstate request from hypervisor (or OCC)
8:15	RWX	LOCAL_PSTATE_REQ: local Pstate request from hypervisor or OCC
16	RWX	AUTO_OVERRIDE0_PSTATE_LIMIT_EN: automatic override Pstate 0 (for low activity detection) is enabled, if asserted

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Bits	PCB	Field Mnemonic: Description
17	RWX	AUTO_OVERRIDE1_PSTATE_LIMIT_EN: automatic override Pstate 1 (reserved for future use) is enabled, if asserted
18:23	RWX	RESERVED_PPMCR: reserved
24:31	RWX	AUTO_OVERRIDE_PSTATE0: automatic override Pstate 0 (for low activity detection)
32:39	RWX	AUTO_OVERRIDE_PSTATE1: automatic override Pstate 1 (reserved for future use)

Register Name	<i>Control Register That Is Written By PMC Sequencer</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_PMC_VF_CTRL_REG
Address	00000000160F015A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PGLOBAL_ACTUAL: global actual Pstate
8:15	RW	MAXREGVCS: maximum regulation point for Vcs, Bit 0 is reserved, bits 1 to 7 are in iVID format
16:23	RW	MAXREGVDD: maximum regulation point for Vdd, Bit 0 is reserved, bits 1 to 7 are in iVID format
24:31	RW	EVIDVCS_EFF: eff. external voltage ID for Vcs in iVID format, Bit 0 is reserved
32:39	RW	EVIDVDD_EFF: eff. external voltage ID for Vdd in iVID format, Bit 0 is reserved

Register Name	<i>Undervolting Register For PCBS</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_UNDERVOLTING_REG
Address	00000000160F015B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PUV_MIN: minimum Pstate for which undervolting is allowed
8:15	RW	PUV_MAX: maximum Pstate for which undervolting is allowed
16:21	RW	KUV: this value indicates how many Pstate ticks a voltage request is undervolted (clipped with Puv_min). Note that the Kuv value is signed

Register Name	<i>PPSIBR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_INDEX_BOUND_REG
Address	00000000160F015C (PCB)
Attributes	
Description	The PPSIBR enables setting the minimum and maximum Pstate that is supported as a pointer into the local Pstate table (which has entries from 0 to 127).

Bits	PCB	Field Mnemonic: Description
0:7	RW	LPSI_MIN: this Pstate index is the index that corresponds to array entry 0. Note that the index domain is obtained by adding 128 to a Pstate, thus, the value is unsigned.
8:14	RW	LPSI_ENTRIES_MINUS_1: this dial contains the value of the number of entries in the Pstate table minus 1

Register Name	<i>PPMBR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_BOUNDS_REG
Address	00000000160F015D (PCB)
Attributes	
Description	The PPMBR enables setting the Pstate bounds that are managed by the OCC. If dial Enable_pmc_pmax_sync_notification is set, firmware must wait after each write to this register until PMC has received the Pmax Sync Interrupt. If a write happens to this register while the previously scheduled Pmax Sync Interrupt has not yet left the PCBS, the error TBD will be set.

Bits	PCB	Field Mnemonic: Description
0:7	RW	PMIN_CLIP: minimum Pstate allowed for this chiplet
8:15	RW	PMAX_CLIP: maximum Pstate allowed for this chiplet (has to be greater or equal to Pmin_clip)

Register Name	<i>PPTCR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_CTRL_REG
Address	00000000160F015E (PCB)
Attributes	
Description	The PPTCR controls the address for writing the local Pstate Table Array (all 96 words are accessible). Note that the protocol requires this register to be set up with the Pstate address first, if a read or a write of the Pstate array is intended, to make sure that the initial address is set correctly. The register PPTR must always be written or read afterward. Note that any access to the PPTR auto-increments this register.

Bits	PCB	Field Mnemonic: Description
0:6	RWX	PSTATE_TABLE_ADDRESS: This is the address of the Pstate table in PCBS, which is auto-incremented after any access to the PTLR.

Register Name	<i>PPTR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_REG
Address	00000000160F015F (PCB)
Attributes	
Description	The PPTR controls the data to be written into the Pstate table and returns the data for a read of the Pstate table. Note that the protocol requires for a write to set this register up after first setting up PPTCR (if the user does not rely on the auto-increment function of the address). For a read of the Pstate table, this register must be read after first setting up PPTCR as well (again if the auto-increment feature of the address is not used). Any access to this register auto-increments the Pstate_table_address by 1. Note also that the read functionality of this register is only functional if PIVRMCSR[ivrm_fsm_enable] = 0. The write functionality works in any case.

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Bits	PCB	Field Mnemonic: Description
0:63	RW	pstate_data This is the field for data bits 0 to 63

Register Name	<i>PPSTR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_STEP_TARGET_REG
Address	00000000160F0160 (PCB)
Attributes	
Description	The PPSTR provides read access to several intermediate values in the Pstate computation pipeline. Writes Are conditioned on the setting of PMGPO[enable_OCC_ctrl_for_local_Pstate_eff_req].

Bits	PCB	Field Mnemonic: Description
0:7	RWX	LOCAL_PSTATE_EFF_REQ: this field represents the effective local Pstate request right before the clipping with Pmin and Pmax if enable_OCC_ctrl_for_local_Pstate_eff_req=0 then the hardware controls this dial, that updates every cycle if enable_OCC_ctrl_for_local_Pstate_eff_req=1 then OCC is in control and can write this field to control the effective local Pstate request that will eventually propagate through the downstream logic and determine the Local PState Actual. Note: if no write to this register is performed, the currently established value is maintained stable forever.
8:15	ROX	LOCAL_PSTATE_TARGET: This field is the target Pstate of a complete Pstate change that is performed in smaller steps
16:23	ROX	LOCAL_CORE_PSTATE_STEP_TARGET: this field represents the intermediate value that is about to be established as the next Local Pstate Actual after completing one step in the process of the transition towards the 'local_Pstate_target' the new voltage, frequency, and clock resonance setting
24:31	ROX	LOCAL_ECO_PSTATE_STEP_TARGET: this field represents the intermediate value that is about to be established as the next Local Pstate Actual after completing one step in the process of the transition towards the 'local_Pstate_target' the new voltage, frequency, and clock resonance setting

Register Name	<i>Read-Only Status Register For DPLL And For Debugging (PDSR)</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_DPLL_STATUS_REG
Address	00000000160F0161 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:14	ROX	DPLL_FF_FREQOUT: frequout output from DPLL (current frequency - bits 2 to 10 correspond to the same scale as the 9 bits of frequin (which need to be multiplied with our frequency step to get the real frequency), the remaining bits just provide a higher accuracy)
15	ROX	DPLL_FREQU_CHANGE: DPLL Frequency change (pin of DPLL without filter)
16	ROX	DPLL_STATUS_SPARE_BIT1: Spare bit.
17	ROX	PMAX_SYNC_PENDING: gets asserted, if the logic has a Pmax sync interrupt outstanding that will be eventually sent to PMC when the Pmax sync criterion is met
18	ROX	GA_ACK_PENDING: gets asserted, if the logic has a global actual Pstate update acknowledgment interrupt outstanding that will be eventually sent to PMC when the GA ack criterion is met
19:26	ROX	CAPPED_GLOBAL_PSTATE_REQ: corresponds to the capped global Pstate request that is presented as Pstate interrupt and send to PMC

Bits	PCB	Field Mnemonic: Description
27	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT2: DPLL runs at Fmax and CPM bit 2 is set. Note that this bit and the following 2 bits indicate, that the CPMs would allow the DPLL to run faster than Fmax.
28	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT3: DPLL runs at Fmax and CPM bit 3 is set
29	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT4: DPLL runs at Fmax and CPM bit 4 is set
30	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT2: DPLL runs at Fmin and CPM bit2 is zero. Note that this bit and the following 2 bits indicate, that the CPMs indicate, that the DPLL should run slower than the currently established Fmin.
31	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT1: DPLL runs at Fmin and CPM bit1 is zero
32	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT0: DPLL runs at Fmin and CPM bit0 is zero
33	ROX_CLRPAR T	DPLL_FASTER_THAN_FMAX_PLUS_DELTA1: The DPLL indicated that it ran once faster than Fmax+dpll_char_delta1
34	ROX_CLRPAR T	DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2: The DPLL indicated that it ran once slower than Fmin-dpll_char_delta2
35:48	ROX	DPLL_MAX_FREQOUT_AFTER_LAST_READ: This dial indicates the maximum DPLL frequout value after the last read of this register (only 14 MSBs)
49:62	ROX	DPLL_MIN_FREQOUT_AFTER_LAST_READ: This dial indicates the minimum DPLL frequout value after the last read of this register (only 14 MSBs)

Register Name	<i>The PIVRMVCR0 Controls The Voltage Stepping Delays</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG0
Address	00000000160F0162 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	IVRM_REQ_PSTATE_STEPDELAY_RISING: Requested Internal Pstate Baby Step Delay - Rising Step. Delay before allowing the next step for a rising Pstate Transition. This dial and ivrm_req_Pstate_stepdelay_lowering allow for differing delays for the two directional transitions if necessary. In 100ns units as established by scan dial ivrm_100ns_value
8:15	RW	IVRM_REQ_PSTATE_STEPDELAY_LOWERING: Requested Internal Pstate Baby Step Delay - Lowering Step. Delay before allowing the next step for a lower Pstate Transition. This dial and ivrm_req_Pstate_stepdelay_rising allow for differing delays for the two directional transitions if necessary. In 100ns units as established by scan dial ivrm_100ns_value

Register Name	<i>The PIVRMVCR1 Controls The Voltage Stepping Delays</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG1
Address	00000000160F0163 (PCB)
Attributes	
Description	

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Bits	PCB	Field Mnemonic: Description
0:7	RW	IVRM_STABILIZE_DELAY_RUN: Stabilization Delay - Run Time Delay to allow a rail to stabilize upon a baby step while the region is operational. In 100ns units as established by scan dial ivrm_100ns_value
8:15	RW	IVRM_STABILIZE_DELAY_IDLE: Stabilization Delay - Idle Transition Delay to allow a rail to stabilize upon a baby step during an idle transition where the activity in the region is quiesced. In 100ns units as established by scan dial ivrm_100ns_value
16:23	RW	IVRM_PFSTR_PROP_DELAY: PFET Strength Propagation Delay Time from PFET Strength values being launched till PFET Strength Valid is asserted. In order to ensure like rails across domains (Core VDD<>ECO VDD, Core VCS<>ECO VCS) are in sync during operational mode, this time value applies to all rails across the domains. This parameter allows for PFET Strength values to settle before PFET Strength Valid is sampled in the Uregs. The value set must the maximum delay for the worst rail timing and must allow for any metastability settling (for example, normally 2-3 cycles for single signals in an asynch handshake interface)
24:31	RW	IVRM_PFSTRVALID_PROP_DELAY: PFETStrength Valid Propagation Delay Time from ivrm_pfstr_prop_delay expiring to where PFET Strength Valid is deasserted. The value is the maximum of a) the minimum pulse width required for PFETStrength Valid and b) the propagation of PFETStrength Valid through (or enough of) the daisy chain. In order to ensure like rails across domains (Core VDD<>ECO VDD, Core VCS<>ECO VCS) are in sync during operational mode, this time value applies to all rails across the domains and thus must be the set to the value of the worst (slowest) rail. The minimum pulse width cannot be violated. The propagation delay can be tuned for more aggressive timing (for example, de-assert before the actual propagation is complete). Measured in prv_nclk cycles. The min delay is 2 cycles. Additional delay can be configured with the following settings 0x00 = No additional delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks
32:39	RW	IVRM_VPUMP_POWERON_TIME: iVRM (VRreg and UReg) - Vpump Power On Time Time necessary for the distributed internal VRM macro circuits to power on. Same delay is required for power on voltage pump circuit. Both delays are in the 8us range. In 100ns units as established by scan dial ivrm_100ns_value
40:47	RW	IVRM_BYPASS_DELAY: iVRM Bypass Propagation Delay Delay time for bypass_b signal propagation. Measured in prv_nclk cycles Target: 50ns 0x00 = No delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks

Bits	PCB	Field Mnemonic: Description
48:55	RW	PFET_VPUMP_ENABLE_DELAY: PFET and Vpump Enable Propagation Delay Delay time for PFET enable and vpump enable signal propagation. Target: 130ns Measured in prv_nclk cycles 0x00 = No delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks
56:62	RW	IVRM_VID_VOUT_THRESHOLD: VID threshold If the output voltage (Vout) is targeting a value below this threshold the slow PFET can backed off from its normal drive strength so as to reduce the ripple at these lower voltage conditions

Register Name	POHR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_OCC_HEARTBEAT_REG
Address	00000000160F0164 (PCB)
Attributes	
Description	Controls the behavior of the OCC heartbeat function.

Bits	PCB	Field Mnemonic: Description
0:7	RW	occ_heartbeat_time 'OCC Heartbeat Time Value' " 'This field defines the number of ~64us hang timer pulses in which a a PCB read or write of the heartbeat trigger register (of which the offset is specified by dial occ_heartbeat_reg_addr_offset) is not detected that will constitute the loss of the OCC heartbeat. If occ_heartbeat_en is set and upon this loss detection, POHBR[psafe] is forced and, if enabled, the error TBD is activated ' ' 0x00 - unsupported, causes undefined behavior' 0x01 - 64us +0/-1us' 0x02 - 128us +0/-1us' ...' 0xFF - 16320us +0/-1us 16.3ms' " 'Upon the 64us hang pulse, the decremter ticks. if the decremter reaches x00, the heartbeat loss event is triggered.' "
8	RW	occ_heartbeat_enable 'OCC Heartbeat Timer Enable' " '0 = Disable the OCC Heartbeat function. Lack of accesses to the register defined by the dial occ_heartbeat_reg_addr_offset does not result in heartbeat loss events to be triggered (no FIRs set nor Safe mode entry).' " '1 = Enable the OCC Heartbeat function.'
9:16	RW	occ_heartbeat_reg_addr_offset This dial allows to configure the address offset within the PCBS power management entity of the register, that will regularly reset the heartbeat timer (which is called heartbeat trigger register). The address offset is 0x100 plus the value of this dial.
17:24	RW	Psafe 'Pstate Safe' " 'This field establishes the Pstate that the core chiplet will take on if: 'psafe <= PMSR[global_actual_pstate]' 'AND any of the following conditions are true:' 'Loss of OCC Heartbeat if occ_heartbeat_en is set' 'PMGPO[force_safe_mode] is set' " 'If psafe > PMSR[global_actual_pstate], the global_actual_pstate is forced.' " " 'The value of Psafe needs to be at or below the nominal Pstate to make sure safe operation of all chiplets.'

Register Name	PRCCR0 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG 0
Address	00000000160F0165 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function.

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Bits	PCB	Field Mnemonic: Description
0	ROX	RESCLK_DIS: Resonant Clock Enable Master enable of all resonant clocking functions. This dial can be set by setting GP3(22) and can not be set in this PCBS_resonant_Clock_Control_Reg0. 1 = Resonant Clock function is disabled. Default values (0) for resclk_value, resclk_core_sync_value, csb_eco_sync_value 0 = Resonant Clock Control hardware is enabled (the mode is defined by dial resclk_control_mode)
1	RW	RESCLK_CONTROL_MODE: Resonant Clock Control Mode Defines the control means enabled when resclk_dis is not set. 0 = Pstate band hardware mechanism enabled 1 = Manual mode enabled (Firmware mode) If this bit is set to 0, the hardware control mechanism that manages the transition across the Resonant Bands is enabled. If this bit is set to 1, the automatic Pstate band hardware mechanism is disabled and the Firmware is in control of all values of the dial resclk_value, resclk_core_sync_value, csb_eco_sync_value. Firmware must ensure that frequency changes will not cross resonant bands or machine failures may result. resclk_value represents the values for clock sector buffer strength, inductor switch strength and high inductor enable. Firmware must ensure the correct stepping in/out the different bands and propagation of the values (resclk_value) to the core/eco (resclk_core_sync_value / csb_eco_sync_value).
2:4	RW	RESCLK_SYNC_PW: Resonant Clock Sync Pulse Width Number of nest/4 cycles to assert the clock sync signal. This value must be high enough to ensure capture and propagation across the asynchronous chiplet boundary.
5:11	RW	RES_SYNC_DELAY_CNT: Resonant Clock Sync Delay Number of nest/4 cycles wait after the launch of the resclk_value (csb and inductor) before launching the sync to allow these to be captured. This value must be high enough to ensure full propagation to the input of the clock sector buffers and inductor switches.
12:26	RW	RES_CSB_STR_INSTR_LO: Resonant Clock Sector Buffer Strength Instruction - Low Band Mask value that determines whether, during a fixed 15 step sequence, the res_csb_str(0:3) is to be decremented/incremented in entering/exiting the Low Band. During resonant clock Entry, res_csb_str(0:3) decremented by the value pattern from 0 down to 14. During resonant clock Exit, res_csb_str(0:3) incremented by the value pattern from 14 up to 0.
27:41	RW	RES_CSB_STR_INSTR_HI: Resonant Clock Sector Buffer Strength Instruction - High Band Mask value that determines whether, during a fixed 15 step sequence, the res_csb_str(0:3) is to be decremented/incremented in entering/exiting the High Band. During resonant clock Entry, res_csb_str(0:3) decremented by the value pattern from 0 down to 14. During resonant clock Exit, res_csb_str(0:3) incremented by the value pattern from 14 up to 0.

Register Name	PRCCR1 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG 1
Address	00000000160F0166 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function. Writes are conditioned.

Bits	PCB	Field Mnemonic: Description
0:7	RW	FULL_CSB_PS: Full Clock Sector Buffer Pstate Pstate defining the maximum point where the clock sector buffer must be driven to full strength. This allow clocks to be distributed at low Vmin levels. FW needs to make sure that no overlaps occur with bands 2 or 3.
8:15	RW	RES_LOW_LOWER_PS: Low Frequency Resonant Lower (LFRLow) Pstate Pstate defining the lower frequency of the Low Resonant Frequency Band. FW needs to make sure that no overlap occurs with band 0.



Bits	PCB	Field Mnemonic: Description
16:23	RW	RES_LOW_UPPER_PS: Low Frequency Resonant Upper (LFRUpper) Pstate Pstate defining the upper frequency of the Low Resonant Frequency Band. Note that if an overlap occurs with band 3, the hardware behavior is undefined.
24:31	RW	RES_HIGH_LOWER_PS: High Frequency Resonant Lower (HFRLow) Pstate Pstate defining the lower frequency of the High Resonant Frequency Band. Note that if an overlap occurs with band 2, the hardware behavior is undefined.
32:39	RW	RES_HIGH_UPPER_PS: High Frequency Resonant Upper (LFRUpper) Pstate Pstate defining the upper frequency of the High Resonant Frequency Band. This value needs to be greater or equal to high_res_lower_ps.
40:43	RW	NONRES_CSB_VALUE_TI: Clock Sector Buffer Table Index for non-resonant state Table Index into Clock Sector Buffer Table for the nominal, non-resonant state.
44:47	RW	FULL_CSB_VALUE_TI: Clock Sector Buffer Table Index for full CSB value Table Index into Clock Sector Buffer Table for the full CSB strength value.
48:56	RWX	RESCLK_VALUE: Output register driving the 9 bit resclk_value In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current resclk_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. The value in this register represents the following concatenation: csb_str_value(0:3) sw_str(0:3) hi_induct_en.
57	RWX	RESCLK_CORE_SYNC_VALUE: Output register driving the resclk_core_sync signal In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current resclk_core_sync_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. This bit is supposed to be used in order to create a SCOM-controlled pulse to force an update of the resclk propagation registers. A 1 enables the synchronous update, a 0 disables it. Suggested use of this bit is to set it to 1 and then set it back to 0 to create a (long) update pulse.
58	RWX	CSB_ECO_SYNC_VALUE: Output register driving the csb_eco_sync signal In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current csb_eco_sync_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. This bit is supposed to be used in order enable the ECO domain to participate in clock sector buffer strength changes, when switching from nominal strength to full CSB strength. A 1 enables the ECO domain, a 0 disables it from seeing a CSB strength update.

Register Name	PRCCR1 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_STATUS_REG
Address	00000000160F0167 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function.



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Bits	PCB	Field Mnemonic: Description
0	ROX	RESCLK_STATE: Resonant Clock State 0 = Resonant Clocking inactive 1 = Resonant Clocking active Valid if resclk_inprogress = 0. Hardware sets this bit to the right value at the completion of the transition into and out of resonance mode.

Bits	PCB	Field Mnemonic: Description
1	ROX	RES_HI_INDUCT_EN: Resonant High Inductor Enable Valid if resclk_inprogress = 0. This dial provides the current value being propagated. 0 = Resonant Clock mode not active 1 = Resonant Clock mode active
2	ROX	RESCLK_INPROGRESS: Resonant Clock Transition in Progress This bit is set by hardware while a transition is in progress and will be reset by hardware when the operation is complete.
3	ROX	RESCLK_FULL_CSB: Full CSB Clock State 0 = Full CSB Clocking inactive 1 = Full CSB Clocking active Valid if resclk_inprogress = 0. Hardware sets this bit to the right value at the completion of the transition into and out of full CSB mode respectively.

Register Name	<i>PLPFTCR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_CONTROL_REG
Address	00000000160F0168 (PCB)
Attributes	
Description	The PLPFTCR enables firmware to configure the modes that are used for the PCBS Local Pstate Frequency Target Status Register.

Bits	PCB	Field Mnemonic: Description
0:2	RW	DELAY_TIME: This field encodes the delay between the time a Local Actual Pstate change modifies the input to the DPLL and the time frequency acquisition begins to allow the hardware to ignore the frequency transition of the DPLL in order to get better frequency measurements. This field encodes a delay of ~1us to ~128us in power of 2 selects. The delay is defined by $2^{**}delay\_time$ in us. Note that the hardware uses multiples of the slow hang pulse that is running at 1us.
3	RW	RECORD_TRANSITIONS: This bit indicates whether the LPFTSR records events that correspond to Local Actual Pstate changes (and therefore may include DPLL slewing effects.) One usage model would set the periodic sample_time defined by the dial OHA_MODE_REG[tod_pulse_count_match_val] to a time less than the worst-case DPLL slew time but then ignore Pstate transitions because they might include DPLL slew effects.
4:18	RW	MULTIPLIER: This 15-bit unsigned constant is multiplied by the DPLL frequency code (9 bits) implied by the Local Actual Pstate to yield the 24-bit frequency target measured in PCBS-PM clock cycles (core clock / 2). Assuming times in seconds and frequencies in Hz, firmware should set this constant to: $(DPLL\_Frequency\_Code\_Step\_Hz * Sample\_Time\_Seconds) / 2$
19	RW	ENABLE_LPFT_FUNCTION: This is the enable bit to enable the local Pstate frequency target function. A '1' enables the function, a '0' disables it (the value can be changed at any time).

Register Name	<i>PLPFTSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_STATUS_REG
Address	00000000160F0169 (PCB)
Attributes	
Description	Allows firmware to observe local actual Pstate realized frequencies.

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Bits	PCB	Field Mnemonic: Description
0	ROX_CLRPART	VALID: If this bit is set then all of the remaining fields of this register are valid. This bit is cleared whenever the register is read or after a local actual Pstate change occurs, and is will be set whenever the hardware completes a valid sample. If firmware reads this register and the valid bit is not set, then it indicates that the Local Pstate target frequency acquisition logic has not been able to complete a frequency acquisition for any Local Actual Pstate change since the last time the LPFTSR was read. This could be due to either of the following factors: 1. Firmware is sampling the LPFTSR faster than the time implied by the sample time defined in OHA by the dial OHA_MODE_REG[tod_pulse_count_match_val] field
1	ROX	CPM_DPLL: If the valid bit is set, then if cpm_dpll is set it indicates that the event recorded by this register was due to a Local Actual Pstate implemented by the DPLL running in CPM-DPLL mode, otherwise the value of this bit is undefined. If the valid bit is not set, this bit is undefined.
2	ROX	IVRM: If the valid bit is set, then if ivrm is set it indicates that the event recorded by this register was due to a Local Actual Pstate whose voltage was set locally by the iVRM operating entirely in regulation mode. If the valid bit is not set, this bit is undefined.
3	ROX	TRANSITION: If the valid bit is set, then if transition is set it indicates that during the observation period a Local Pstate Actual change has occurred, and any performance delta may be due to DPLL frequency slewing. If the valid bit is not set, this bit is undefined
4	ROX	STABLE: If stable is set it indicates that the DPLL input frequency has been stable since the last time the PLPFTSR was read. This bit is set whenever the PLPFTSR is read, and cleared whenever the Fmax input of the DPLL changes. This bit is always valid, regardless of the state of the valid bit. If the PLPFTSR is read on the same cycle a frequency changes then the stable bit is cleared. This bit helps firmware better understand how to interpret the information contained in the PLPFTSR. (Note that this bit should have an attribute ROX_SETPART, but this is not supported by regchk.)
5:28	ROX	DELTA: If the valid bit is set then this is the 24-bit signed difference Measured Cycles - Target Cycles for the event captured by this register. If the valid bit is not set, this dial is undefined.
29:52	ROX	CUMULATIVE: This field records the 24-bit cumulative (signed) delta for all valid samples taken since this field was cleared. Writing any value to this register clears this field. Note that it should have an attribute WOX_CLRPART, but this is not supported by regchk/figtree.
53:60	ROX	PSTATE: If the valid bit is set then this is the Local Actual Pstate of the frequency acquisition that had the minimum (signed) delta of any valid sample taken since the last time the LPFTSR was read. If the valid bit is not set, then this field is undefined.

Register Name	PFSMM1/2 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR1_REG
Address	00000000160F0170 (PCB)
Attributes	
Description	The PFSMM1/2 facilitates debug by providing insight into the internal FSM states of the PCB-slave power-management unit. For expert use only. Coding according to VHDL design.

Bits	PCB	Field Mnemonic: Description
0:6	ROX	BABYSTEP_MAIN_FSM: Main Babystep FSM (mfsm_lt)
7:11	ROX	BABYSTEP_SLAVE_FSM: Babystep Slave FSM (sfsm_lt)
12:16	ROX	CORE_RAILSTEPPER_MAIN_FSM: Main Core Railstepper FSM (mrsfsm_lt)
17:21	ROX	ECO_RAILSTEPPER_MAIN_FSM: Main ECO Railstepper FSM (mrsfsm_lt)



Bits	PCB	Field Mnemonic: Description
22:25	ROX	CORE_RAILSTEPPER_SUB_FSM: Core Railstepper Sub-FSM (srsfsm_lt)
26:29	ROX	ECO_RAILSTEPPER_SUB_FSM: ECO Railstepper Sub-FSM (srsfsm_lt)
30:34	ROX	CORE_RAILSTEPPER_BYP_FSM: Core Railstepper Bypass FSM (byp_fsm_lt)
35:39	ROX	ECO_RAILSTEPPER_BYP_FSM: ECO Railstepper Bypass FSM (byp_fsm_lt)
40:45	ROX	IVRM_CORE_VDD_SEQUENCER_FSM: Core iVRM Sequencer for Vdd (ivrm_fsm_lt)
46:51	ROX	IVRM_CORE_VCS_SEQUENCER_FSM: Core iVRM Sequencer for Vcs (ivrm_fsm_lt)
52:57	ROX	IVRM_ECO_VDD_SEQUENCER_FSM: ECO iVRM Sequencer for Vdd (ivrm_fsm_lt)
58:63	ROX	IVRM_ECO_VCS_SEQUENCER_FSM: ECO iVRM Sequencer for Vcs (ivrm_fsm_lt)

Register Name	<i>Refer To The Description Of PFSMM1.</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR2_REG
Address	00000000160F0171 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:6	ROX	RESCLK_BAND_FSM: Band Sequencer for resonant clocking (band_fsm_lt)
7:10	ROX	RESCLK_LOWRES_FSM: Low Resonant Clocking sequencer (lowres_fsm_lt)
11:14	ROX	RESCLK_HIGHRES_FSM: High Resonant Clocking sequencer (highres_fsm_lt)
15:18	ROX	RESCLK_FULLCSB_FSM: Full-CSB Resonant Clocking sequencer (fullcsb_fsm_lt)
19:22	ROX	RESCLK_UPDATE_FSM: Resonant Clocking Update sequencer (update_fsm_lt)
23:29	ROX	IDLE_TRANSITION_FSM: Idle State Sequence FSM (ifsm_lt)
30:37	ROX	Peco_step_target_uv Current ECO Step Target Pstate (different from Plocal_actual for undervolting)
38:45	ROX	Pcore_step_target_uv Current core Step Target Pstate (different from Plocal_actual for sleep and undervolting)

Register Name	<i>Protect Mode Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.PROTECT_MODE_REG
Address	00000000160F03FE (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	READ_PROTECT_ENABLE: Enable read protection
1	RW	WRITE_PROTECT_ENABLE: Enable write protection

Register Name	<i>Atomic Lock Register</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX06.TP_PCB_SLAVE_INST.ATOMIC_LOCK_REG	
Address	00000000160F03FF (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	RW	ATOMIC_LOCK_ENABLE: Enable atomic lock
1:4	ROX	ATOMIC_ID: Atomic ID

Register Name	<i>Contains The Slave's Primary Address</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.PRIMARY_ADDRESS_REG	
Address	00000000190F0000 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RO	Reserved field (Access type is primary_address)

Register Name	<i>Multicast Group 1</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.MULTICAST_GROUP_1	
Address	00000000190F0001 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST1_GROUP: multicast group1 setting

Register Name	<i>Multicast Group 2</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.MULTICAST_GROUP_2	
Address	00000000190F0002 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST2_GROUP: multicast group2 setting



Register Name	Multicast Group 3	
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.MULTICAST_GROUP_3	
Address	00000000190F0003 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST3_GROUP: multicast group3 setting

Register Name	Multicast Group 4	
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.MULTICAST_GROUP_4	
Address	00000000190F0004 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST4_GROUP: multicast group4 setting

Register Name	Timeout Select Register	
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.TIMEOUT_REG	
Address	00000000190F0010 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:1	RW	Reserved field (Access type is int_timeout)

Register Name	Assist Interrupt Register	
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.ASSIST_INTERRUPT_REG	
Address	00000000190F0011 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is attn)
1	ROX	Reserved field (Access type is recov)
2	ROX	Reserved field (Access type is xstop)

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Register Name	GP3 Register (NA In PERV CPLT)
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.GP3_REG
Address	00000000190F0012 (PCB) 00000000190F0013 (PCB1) 00000000190F0014 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset
2	RWX	RWX_WAND	RWX_WOR	GLSMUX_RESET: Glsmux reset for test purpose and stuck active mesh protection. Notice no clocks in the EX if this bit is set.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Put the DPLL in test mode.
4	RWX	RWX_WAND	RWX_WOR	PLL_RST: Put PLL in reset state.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYP: Enable PLL bypass.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pcb_access)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	PM_PI_DECODE: Test override for power management. EX chiplet only.
22	RWX	RWX_WAND	RWX_WOR	RESCLK_DIS: Resonant clocking disable.
23:25	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave will report 'Chiplet Offline'.
27	RWX	RWX_WAND	RWX_WOR	TP_LVLTRANS_FENCE: Electrical winkel fence. Mainly used by power management.
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.
29:31	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)



Register Name	<i>Skew Adjust Data</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.CLK_ADJ_REG	
Address	00000000190F0015 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:15	ROX	

Register Name	<i>Clk Ajust Config</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.CLK_ADJ_SET	
Address	00000000190F0016 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:31	RW	CLK_ADJ_SET_REG: Clk adj config

Register Name	<i>Vital Scan Out</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.VITAL_SCAN_OUT	
Address	00000000190F0017 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	

Register Name	<i>Chiplet Heartbeat Register</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.HEARTBEAT_REG	
Address	00000000190F0018 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	HEARTBEAT_DEAD: Chiplet heartbeat not detected

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Register Name	<i>Lock Indications From PLLs</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.PLL_LOCK_REG
Address	00000000190F0019 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	ROX	Reserved field (Access type is lock)

Register Name	<i>Attn Interrupt</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.ATTN_INTERRUPT_REG
Address	00000000190F001A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is attn)

Register Name	<i>Recov Interrupt</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.RECOV_INTERRUPT_REG
Address	00000000190F001B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is recov)

Register Name	<i>Xstop Interrupt</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.XSTOP_INTERRUPT_REG
Address	00000000190F001C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is xstop)



Register Name	<i>Slave Config Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.SLAVE_CONFIG_REG
Address	00000000190F001E (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	CFG_DISABLE_PERV_THOLD_CHECK: Disable pervasive thold check
1	RW	CFG_DISABLE_MALF_PULSE_GEN: Disable pulse generation for malf alert. Switch back to level
2	RW	CFG_STOP_HANG_CNT_SYS_XSTP: Disable hang counter stop for system xstop
3	RW	CFG_DISABLE_CL_ATOMIC_LOCK: Disable atomic lock for chiplet accesses
4	RW	CFG_DISABLE_HEARTBEAT: Disable check for voltage and gridclock in the chiplet
5	RW	CFG_ZERO_DATA: Sent zero data on any error
6:7	RW	
8:12	RW	ERROR_MASK: mask bits for slave error reporting
13:15	RW	

Register Name	<i>Error Capture Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.ERROR_REG
Address	00000000190F001F (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX_WCLEA R	CE_ERROR: Correctable error on pcb bus
1:3	RWX_WCLEA R	CHIPLET_ERRORS: Errors reported by chiplet 000 = no error 001 = XSCOM command blocked due pending errors 010 chiplet offline 011 partial good 100 invalid address / address error / bad access type 101 clock error 110 parity error / received unexpected packet / wrong packet number 111 timeout This register is for debug purposes only. It only holds meaningful data if it is cleared after each error.
4	RWX_WCLEA R	PARITY_ERROR: Parity error on PCB Interface
5	RWX_WCLEA R	DATA_BUFFER_ERROR: Parity error in data buffer
6	RWX_WCLEA R	ADDR_BUFFER_ERROR: Parity error in address buffer
7	RWX_WCLEA R	PCB_FSM_ERROR: Invalid state error in PCB FSM
8	RWX_WCLEA R	CL_FSM_ERROR: Invalid state error in Chiplet FSM
9	RWX_WCLEA R	INT_RX_FSM_ERROR: Invalid state error in interrupt RX FSM
10	RWX_WCLEA R	INT_TX_FSM_ERROR: Invalid state error in interrupt TX FSM

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Bits	PCB	Field Mnemonic: Description
11	RWX_WCLEAR	INT_TYPE_ERROR: Invalid interrupt type
12	RWX_WCLEAR	CL_DATA_ERROR: Parity error on Chiplet Interface
13	RWX_WCLEAR	INFO_ERROR: Parity error on Chiplet info lines
14	RWX_WCLEAR	UNUSED_0:
15	RWX_WCLEAR	CHIPLET_ATOMIC_LOCK_ERROR: Chiplet atomic lock error
16	RWX_WCLEAR	PCB_INTERFACE_ERROR: Error of pcb interface component for the internal endpoint
17	RWX_WCLEAR	CHIPLET_OFFLINE: Heartbeat check indicated that chiplet is offline
18	RWX_WCLEAR	CHIPLET_GRID_SKITTER: Heartbeat check indicated skitter on the chiplet grid
19	RWX_WCLEAR	GP3_REG_PARITY_ERROR: gp3 register parity bad
20	RWX_WCLEAR	ADDRESS_REG_PARITY_ERROR: address register parity bad
21	RWX_WCLEAR	TIMEOUT_REG_PARITY_ERROR: timeout select register parity bad
22	RWX_WCLEAR	CONFIG_REG_PARITY_ERROR: slave config register parity bad
23	RWX_WCLEAR	CLK_ADJ_REG_PARITY_ERROR: clk adj register parity bad
24	RWX_WCLEAR	DIV_REG_PARITY_ERROR: div register parity bad
25:28	RWX_WCLEAR	PLL_UNLOCK_ERROR: unlock from chiplet pll

Register Name		Hang Pulse Generation Register 0.
Mnemonic		EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.HANG_PULSE_0_REG
Address		00000000190F0020 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_0: Value of hang pulse 0. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_0: If set to '1', hang pulses are suppressed in case of a xstop



Register Name	Hang Pulse Generation Register 1.	
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.HANG_PULSE_1_REG	
Address	00000000190F0021 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_1: Value of hang pulse 1. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_1: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	Hang Pulse Generation Register 2.	
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.HANG_PULSE_2_REG	
Address	00000000190F0022 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_2: Value of hang pulse 2. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_2: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	Hang Pulse Generation Register 3.	
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.HANG_PULSE_3_REG	
Address	00000000190F0023 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_3: Value of hang pulse 3. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_3: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	Hang Pulse Generation Register 4.	
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.HANG_PULSE_4_REG	
Address	00000000190F0024 (PCB)	
Attributes		
Description		

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Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_4: Value of hang pulse 4. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_4: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 5</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.HANG_PULSE_5_REG
Address	00000000190F0025 (PCB)
Attributes	
Description	This hang counter is used exclusively to generate the malfunction alert pulse.

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_5: Value of hang pulse 5. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_5: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 6</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.HANG_PULSE_6_REG
Address	00000000190F0026 (PCB)
Attributes	
Description	This hang counter is exclusively used for heartbeat generation.

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_6: Value of hang pulse 6. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_6: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Divider For Hang Counter Clock</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.PRE_COUNTER_REG
Address	00000000190F0028 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PRE_COUNTER: Divider for hang counter clock. Divides clock by n+1 (default: n=0)



Register Name		PowerManagement GP0		
Mnemonic		EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PMGP0_REG		
Address		00000000190F0100 (PCB) 00000000190F0101 (PCB1) 00000000190F0102 (PCB2)		
Attributes				
Description				
Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PM_DISABLE: Master Switch for the PowerManagement Macro
1	RWX	WOX_AND	WOX_OR	PMGP0_SPARE_BIT1: spare bit
2	RWX	WOX_AND	WOX_OR	TP_TC_RESTART_CORE_DOMAIN: Kicks off small sequencer in OHA to get chiplet clocks back running for fast sleep without involving PORE. From GP-reg and overridden by PowMan State Machine.
3	RWX	WOX_AND	WOX_OR	DPLL_THOLD: Thold for the DPLL clock domain in the chiplet
4	RWX	WOX_AND	WOX_OR	PERV_THOLD: Thold for the Pervasive clock domain in the chiplet
5	RO	RO	RO	Reserved.
6	RO	RO	RO	Reserved.
7	RWX	WOX_AND	WOX_OR	PM_DPLL_TIMER_ENA: Select a timer instead of the DPLL lock bit for criteria to switch to DPLL. The time is defined by thold_timer_sel.
8	RWX	WOX_AND	WOX_OR	DPLL_LOCK_SENSE: DPLL lock sensitivity control (0=faster lock time, 1=slower lock time)
9	RWX	WOX_AND	WOX_OR	PMGP0_SPARE2: spare bit
10	RWX	WOX_AND	WOX_OR	DPLL_RESET: Reset to DPLL
11	RWX	WOX_AND	WOX_OR	PMGP0_SPARE_BIT11: Spare bit
12:19	RWX	WOX_AND	WOX_OR	DPLL_TESTOUT_CTL: DPLL testout control
20	RWX	WOX_AND	WOX_OR	TP_TC_CACHE2CORE_FENCE: Fence from cache to core domain in EX chiplet
21	RWX	WOX_AND	WOX_OR	TP_TC_CORE2CACHE_FENCE: Fence from core to cache domain in EX chiplet
22	RWX	WOX_AND	WOX_OR	TP_TC_PERVASIVE_ECO_FENCE: Pervasive ECO fence
23	RWX	WOX_AND	WOX_OR	CHKSW_HW257424_DISABLE: Chicken switch for interrupt retry exhausted bug (0=fix enabled, 1=fix disabled)
24:26	RWX	WOX_AND	WOX_OR	TP_CLK_ASYNC_RESET_DC: Clk async reset for three glitchless muxes, and the two clock dividers (bit 0 = master GLM, bit 1 = ECO Div2 and ECO GLM, bit 2= core Div1 and core GLM)
27:29	RWX	WOX_AND	WOX_OR	TP_CLKGLM_SEL_DC: Glitchless Mux Select for primary chiplet clock source (feeding both core and eco clock muxes) 000 = refclk, 001 = DPLL. 100 = Use constant selected by bit 34, else refclk
30	RWX	WOX_AND	WOX_OR	TP_CLKGLM_ECO_SEL_DC: Glitchless Mux Select for eco domain (cache_nclk) grid. 0= follow primary source chosen by previous field: 1 = Use constant selected by bit 34
31	ROX	NC	NC	SPECIAL_WKUP_DONE: Indicates that special wakeup is done, if asserted
32:33	RWX	WOX_AND	WOX_OR	TP_CLKGLM_CORE_SEL_DC: Glitchless Mux Select for core domain (nclk grid) mux. 0b00=primary GLS mux output, 0b10=constant input, 0b01=refclk. Valid transitions are 0b01 <-> 0b00 <-> 0b10, 0b11 is illegal

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
34	RWX	WOX_AND	WOX_OR	TP_CLKGLM_CONST_DC: Constant input available to all three ClkGlm
35:36	RWX	WOX_AND	WOX_OR	THOLD_TIMER_SEL: Selection for the thold transition timer in the IDLE state machine. 0b00=1024 cycles delay, 0b01=512 cycles delay, 0b10=256 cycles delay, 0b11= 128 cycles delay
37	RWX	WOX_AND	WOX_OR	BLOCK_ALL_WAKEUP_SOURCES: Setting this bit will make the PM Slave ignore any Wakeup events (ext. interrupt, malfunction alert, any special wakeup bit). This bit is intended to enable firmware concurrent patch capability. Note: This does NOT block the interrupt from being presented to the processor core. The following procedure is required on changes: 1. Firmware may only set this bit after first setting special wakeup and polling for special wakeup complete (OHA and PCB-slave both in running state with AISS and PM FSMs idle). 2. Firmware may only clear this bit if all special wakeup bits are first cleared.
38	RWX	WOX_AND	WOX_OR	TP_TC_DPLL_TESTMODE_DC: ADPLL test mode
39	RWX	WOX_AND	WOX_OR	PM_SLV_WINKLE_FENCE: Fence off the powered off chiplet in winkle. - Logical fence/hold for pcb_slave and pcb_slave_pm. For electrical fence see bit 23.
40	RWX	WOX_AND	WOX_OR	L3_ENABLE_SWITCH: Setting this bit activates l3_edram_enable if allowed by system configuration GP3(28). Resetting this bit deactivates l3_edram_enable.
41	RWX	WOX_AND	WOX_OR	TP_CPLT_IVRM_REFBYPASS_DC: Signal to iVRM (used to be controlled by scan-only block inside EX, but needs to be driven by VIO domain)
42	RWX	WOX_AND	WOX_OR	CHKSW_HW241939_DISABLE: if this bit is set to 1, the fix for HW241939 (pfet enable SCOM-ability) is disabled
43	RWX	WOX_AND	WOX_OR	CHKSW_HW273115_DISABLE: if this bit is set to 1, the fix for HW273115 (Pga ACK noack issue when the babystepper is in the winkle state) is disabled
44	RWX	WOX_AND	WOX_OR	CHKSW_HW245103_DISABLE: if this bit is set to 1, the fix for HW245103 resonant clocking CSB and SW -bit ordering change is disabled
45	RWX	WOX_AND	WOX_OR	CHKSW_HW257534_DISABLE: if this bit is set to 1, the fix for HW257534 (fencing of errors) is disabled
46	RWX	WOX_AND	WOX_OR	CHKSW_HW259509_ENABLE: if this bit is set to 0, the fix for HW259509 (Pstate change hanging, because of DPLL flock timer in a hung state) is disabled
47	RWX	WOX_AND	WOX_OR	CHKSW_HW260345_DISABLE: if set to 1, this bit disables the HW260345 fix (fix was to make sure that we enter bypass mode for iVRM safe mode without a glitch that could cause Vcs in regulation and Vdd in bypass)
48:49	ROX	NC	NC	WAKEUP_INT_TYPE: (Known to be unreliable and not supported, informational usage only) Type of the last wakeup event that caused an exit from sleep or winkle (excluding nap!), regardless of present state. 0b01: External interrupt. 0b10: Malfunction Alert. 0b11: Special Wakeup. 0b00: chiplet has never fully entered and exited a chiplet-level idle state since IPL of the system. (Note this does not necessarily get updated when the processor core enters an idle state, only if the PCB-Slave enters and then exits the idle state for this chiplet).
50	ROX	NC	NC	DPLL_LOCK: DPLL lock indicator
51	ROX	NC	NC	SPECIAL_WKUP_ALL_SOURCES_ORED: logical OR of all special wakeup sources
52	ROX	NC	NC	REGULAR_WKUP_AVAILABLE: logical OR of external interrupt and malfunction alert



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
53	RWX	WOX_AND	WOX_OR	BLOCK_REG_WKUP_SOURCES: blocks ext. int. and malf. Alert from waking up PCBS (no block possible for PC!)

Register Name	PowerManagement GP1
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PMGP1_REG
Address	00000000190F0103 (PCB) 00000000190F0104 (PCB1) 00000000190F0105 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	SLEEP_POWER_DOWN_EN: Sleep Power Down Enable: When set to 1, causes hardware to automatically reduce voltage to the Core domain when entering Sleep mode. The voltage value for power down is chosen by sleep_power_off_sel (bit 2). When set to 0, a request is sent to the PORE engine for assistance entering Sleep.
1	RWX	WOX_AND	WOX_OR	SLEEP_POWER_UP_EN: Sleep Power Up Enable: When set to 1, enables automated hardware restoration of voltage via PFETs and, if enabled, iVRMs when exiting Sleep mode. If this bit is set to 0 the hardware rely on external means (PORE or equivalent) to restore voltage.
2	RWX	WOX_AND	WOX_OR	SLEEP_POWER_OFF_SEL: Sleep Power Off Select: Selects which voltage level to place the Core domain PFETs upon Sleep entry. 0 = Vret (Fast Sleep Mode), 1 = Voff (Deep Sleep Mode). Depending on the setting of pmicr_latency_en, this bit is controlled with a PCB-write (0) or by the PMICR in the core (1).
3	RWX	WOX_AND	WOX_OR	WINKLE_POWER_DOWN_EN: Winkle Power Down Enable: When set to 1, causes hardware to automatically reduce voltage to the entire Chiplet (both Core and ECO Domains) when entering Winkle mode. The voltage value for power down is chosen by winkle_power_off_sel (bit 5). When set to 0, a request is sent to the PORE engine for assistance entering Winkle.
4	RWX	WOX_AND	WOX_OR	WINKLE_POWER_UP_EN: Winkle Power Up Enable: When set to 1, enables automated hardware PFET enablement when exiting Winkle mode. If this bit is set to 0 the hardware rely on external means (PORE or equivalent) to cause the PFETs to be re-enabled.
5	RWX	WOX_AND	WOX_OR	WINKLE_POWER_OFF_SEL: Winkle Power Off Select: Selects which voltage level to place the Core and ECO domain PFETs upon Winkle entry. 0 = Vret (Fast Winkle Mode), 1 = Voff (Deep Winkle Mode). Depending on the setting of pmicr_latency_en, this bit is controlled with a PCB-write (0) or by the PMICR in the core (1).
6	RWX	WOX_AND	WOX_OR	OHA_WKUP_OVERRIDE_EN: Needs to be 0 for normal operation. If set to 1, the two following dials are used to override the regular and special wakeup signal from PCBS to OHA
7	RWX	WOX_AND	WOX_OR	OHA_PM_WKUP_OVERRIDE: Enablement by 'oha_wkup_override_en' forces the regular wakeup signal to OHA to the value of this bit regardless of presence of an interrupt source.
8	RWX	WOX_AND	WOX_OR	OHA_SPC_WKUP_OVERRIDE: Enablement by 'oha_wkup_override_en' forces the special wakeup signal to OHA to the value of this bit, regardless of the firmware settings.

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
9	RWX	WOX_AND	WOX_OR	ENDP_RESET_PM_ONLY: If asserted, an endpoint reset of all power management-related functions (not the regular PCB slave) is performed. Intended usage is for recovery.
10	RWX	WOX_AND	WOX_OR	DPLL_FREQ_OVERRIDE_ENABLE: override Fmax/Fmin only, if '1', using register FREQ_CTRL_REG
11	RWX	WOX_AND	WOX_OR	PM_SPR_OVERRIDE_EN: PM SPR Override Enable The PPMCR (0xNNNN) and PPMICR (0XXXXX) accesses the register resources that make up the PMCR SPR used by hypervisor to management Pstates. Thus, PCB updates to it are disabled in hardware to prevent collisions. This bit allows ownership of the PMCR to be switched from hypervisor to OCC. This switch is immediate in hardware, thus, firmware must ensure the ownership switch is otherwise communicated. 0 = Disables the writing of the PPMCR (0xNNNN) from the PCB and allows SPR 884 writes (mtspr) to update the register resource. 1 = Enables the writing of the PPMCR (0xNNNN) from the PCB.
12	RWX	WOX_AND	WOX_OR	FORCE_SAFE_MODE: Force Safe Mode 0 = Allow other enabled features to determine the operational Pstate. 1 = Forces the minimum of POHBR[psafe] and PPMSR[global_pstate_actual] Pstate for the core chiplet as the operational frequency.
13	RWX	WOX_AND	WOX_OR	IVRM_SAFE_MODE_EN: Internal VRM Safe Mode Enable 0 = Disable the iVRM safe mode, thus, no automatic actions occur, if an iVRM error happens. 1 = if the iVRMs are enabled (PIVRMCSR[ivrn_en] is set) and Pstates are enabled and if the error defined by dial pcbs_ivrm_gross_or_fine_err occurs, then the railstepper is forced into bypass mode to prevent a voltage-frequency hazard
14	RWX	WOX_AND	WOX_OR	IVRM_SAFE_MODE_FORCE_ACTIVE: Internal VRM Safe Mode Force Dial 0 = the hardware decides whether to activate the iVRM safe mode or not 1 = the iVRM safe mode is forced regardless (this makes only sense if ivrm_fsm_enable=1 and Pstates are enabled)
15	RWX	WOX_AND	WOX_OR	PMICR_LATENCY_EN: Selects how the sleep/winkle latency (which is deep/fast) is controlled. If asserted the PMICR controls the winkle/sleep_power_off_sel in PMGP1, otherwise those bits are controlled via SCOM by OCC.
16	RWX	WOX_AND	WOX_OR	ENABLE_OCC_CTRL_FOR_LOCAL_PSTATE_EFF_REQ: controls, if the HW (for value 0) or OCC (value 1) is in control of the Local Pstate Effective register in PPSTR
17	RWX	WOX_AND	WOX_OR	SERIALIZE_PFET_POWERDOWN: if asserted, the pFET sequencer will sequence the core and the ECO domain one after the other when powering down
18	RWX	WOX_AND	WOX_OR	SERIALIZE_PFET_POWERUP: if asserted, the pFET sequencer will sequence the ECO and the core domain one after the other when powering up
19	RWX	WOX_AND	WOX_OR	DISABLE_FORCE_DEEP_TO_FAST_SLEEP: 0: (normal operation) - If PCB Slave reports a recoverable error or a checkstop, a DEEP sleep operation is forced to FAST. The entries in sleep/winkle_power_off_sel remain unchanged. 1: force to FAST is disabled.



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
20	RWX	WOX_AND	WOX_OR	DISABLE_FORCE_DEEP_TO_FAST_WINKLE: 0: (normal operation) - If PCB Slave reports a recoverable error or a checkstop, a DEEP winkle operation is forced to FAST. The entries in sleep/winkle_power_off_sel remain unchanged. 1: force to FAST is disabled.

Register Name	PFET Control/Status Register For Core And ECO Vdd
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PFVDDCNTLSTAT_REG
Address	00000000190F0106 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	CORE_VDD_PFET_FORCE_STATE: Core Domain PFET Force State Provides a means for firmware to force the core domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 4:5 = 00 (both core_vdd_pfet_val_override AND core_vdd_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
2:3	RW	ECO_VDD_PFET_FORCE_STATE: ECO Domain PFET Force State Provides a means for firmware to force the ECO domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 6:7 = 00 (both eco_vdd_pfet_val_override AND eco_vdd_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
4	RW	CORE_VDD_PFET_VAL_OVERRIDE: Core Domain PFET Value Override 0 = Override is disabled
5	RW	CORE_VDD_PFET_SEL_OVERRIDE: Core Domain PFET Stage Select Override 0 = Override is disabled
6	RW	ECO_VDD_PFET_VAL_OVERRIDE: ECO Domain PFET Value Override 0 = Override is disabled
7	RW	ECO_VDD_PFET_SEL_OVERRIDE: ECO Domain PFET Stage Select Override 0 = Override is disabled
8	RW	CORE_VDD_PFET_ENABLE_REGULATION_FINGER: Core Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the core_vdd_pfet_enable_value.
9	RW	ECO_VDD_PFET_ENABLE_REGULATION_FINGER: ECO Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the eco_vdd_pfet_enable_value.

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Bits	PCB	Field Mnemonic: Description
10:21	RW	CORE_VDD_PFET_ENABLE_VALUE: Core PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the Core Domain PFET Enables directly. If core_vdd_pfet_val_override = 1, a write to this field sets the state of the core PFET Enables until core_vdd_pfet_val_override is cleared. If core_vdd_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the core_vdd_pfet_valN_slac registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
22:25	RW	CORE_VDD_PFET_SEL_VALUE: Core PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure core_vdd_pfet_valN_slac(0:11) where N is 0 to 11 if core_vdd_pfet_sel_override = 1. If core_vdd_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
26:37	RW	ECO_VDD_PFET_ENABLE_VALUE: ECO PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the ECO PFET Enables directly. If ECO_vdd_pfet_val_override = 1, a write to this field sets the state of the ECO PFET Enables until ECO_vdd_pfet_val_override is cleared. If eco_vdd_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the eco_vdd_pfet_valN_slac registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
38:41	RW	ECO_VDD_PFET_SEL_VALUE: ECO PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure eco_vdd_pfet_valN_slac(0:11) where N is 0 to 11 if eco_vdd_pfet_sel_override = 1. If eco_vdd_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
42:45	ROX	CORE_VDD_PG_STATE: Core power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
46:49	ROX	CORE_VDD_PG_SEL: For debug, contains the actual index n into Core Domain PFET Value [n] SLAT Register set that contains the Core PFET Enable Value currently enabled.
50:53	ROX	ECO_VDD_PG_STATE: ECO Domain power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
54:57	ROX	ECO_VDD_PG_SEL: For debug, contains the actual index n into ECO Domain PFET Value [n] SLAT Register set that contains the ECO PFET Enable Value currently enabled.

Register Name	PFET Sense Register	
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PFSENSE_REG	
Address	00000000190F0107 (PCB)	
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:11	ROX	TP_CORE_VDD_PFET_ENABLE_SENSE: Not used any more.
12:23	ROX	TP_ECO_VDD_PFET_ENABLE_SENSE: Not used any more.



Bits	PCB	Field Mnemonic: Description
24:35	ROX	TP_CORE_VCS_PFET_ENABLE_SENSE: Not used any more.
36:47	ROX	TP_ECO_VCS_PFET_ENABLE_SENSE: Not used any more.

Register Name	<i>PM Error Summary Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PMERRSUM_REG
Address	00000000190F0108 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	PM_ERROR: PM Error is present. Intended for use by special PCB multicast to see error state of all chiplets with a single read (via 510F0108 to read all chiplets)

Register Name	<i>PM Error Register:</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PMERR_REG
Address	00000000190F0109 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_HANG_ERR: Hang during Unassisted Sleep Entry: SLEEP_ENTRY_NOTIFY_PMC state
1	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ASSIST_HANG_ERR: Hang during Assisted Sleep Entry: SLEEP_ENTRY_NOTIFY_PMC_ASSIST state
2	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ERR: Hang during Unassisted Sleep Exit: SLEEP_EXIT_NOTIFY_PMC state
3	ROX	PCBS_SLEEP_EXIT_INVOKE_PORE_ERR: Hang during Assisted Deep Sleep Exit: SLEEP_EXIT_INVOKE_PORE state
4	ROX	PCBS_WINKLE_ENTRY_NOTIFY_PMC_ERR: Hang during Unassisted Winkle Entry: WINKLE_ENTRY_NOTIFY_PMC state
5	ROX	PCBS_WINKLE_ENTRY_SEND_INT_ASSIST_ERR: Hang during Assisted Winkle Entry: WINKLE_ENTRY_SEND_INT_ASSIST state
6	ROX	PCBS_WINKLE_EXIT_NOTIFY_PMC_ERR: Hang during Unassisted Winkle Exit: WINKLE_EXIT_NOTIFY_PMC state
7	ROX	PCBS_WAIT_DPLL_LOCK_ERR: Hang during Unassisted Exit waiting on DPLL: WAIT_DPLL_LOCK state
8	ROX	PCBS_SPARE8_ERR: spare bit, always 0
9	ROX	PCBS_WINKLE_EXIT_SEND_INT_ASSIST_ERR: Hang during Assisted Winkle Exit: WINKLE_EXIT_SEND_INT_ASSIST state
10	ROX	PCBS_WINKLE_EXIT_SEND_INT_POWUP_ASSIST_ERR: Hang during Assisted Winkle Exit: WINKLE_EXIT_SEND_INT_POWUP_ASSIST state
11	ROX	PCBS_WRITE_FSM_GOTO_REG_IN_INVALID_STATE_ERR: write to FSM goto register in invalid state
12	ROX	PCBS_WRITE_PMGP0_IN_INVALID_STATE_ERR: write to PMGP0 in invalid state

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Bits	PCB	Field Mnemonic: Description
13	ROX	PCBS_FREQ_OVERFLOW_IN_PSTATE_MODE_ERR: frequency of DPLL in Pstate mode overflows (Fnom + desired Pstate > 511)
14	ROX	PCBS_ECO_RS_BYPASS_CONFUSION_ERR: ECO railstepper tried to exit Vcs bypass and enter Vdd bypass in one Pstate step (it is not clear, in which order this strange operation should be performed - most likely it should never happen to avoid that Vcs is greater than Vdd)
15	ROX	PCBS_CORE_RS_BYPASS_CONFUSION_ERR: same as previous error, but for core railstepper (it is not clear, in which order this strange operation should be performed - most likely it should never happen to avoid that Vcs is greater than Vdd)
16	ROX	PCBS_READ_LPST_IN_PSTATE_MODE_ERR: read LPST-array while iVRM FSMs are enabled (dial ivrm_fsm_enable asserted)
17	ROX	PCBS_LPST_READ_CORR_ERR: correctable error occurred when reading the LPST
18	ROX	PCBS_LPST_READ_UNCORR_ERR: uncorrectable error occurred when reading the LPST
19	ROX	PCBS_PFET_STRENGTH_OVERFLOW_ERR: overflow occurred when calculating the pFET strength (in final rounding step!)
20	ROX	PCBS_VDS_LOOKUP_ERR: Vds entry not found in lookup table (when performing the linear search!)
21	ROX	PCBS_IDLE_INTERRUPT_TIMEOUT_ERR: idle interrupt timeout in PCB interrupt controller
22	ROX	PCBS_PSTATE_INTERRUPT_TIMEOUT_ERR: PState interrupt timeout in PCB interrupt controller
23	ROX	PCBS_GLOBAL_ACTUAL_SYNC_INTERRUPT_TIMEOUT_ERR: GlobalActualSync Interrupt timeout in PCB interrupt controller
24	ROX	PCBS_PMAX_SYNC_INTERRUPT_TIMEOUT_ERR: PmaxSync Interrupt timeout in PCB interrupt controller
25	ROX	PCBS_GLOBAL_ACTUAL_PSTATE_PROTOCOL_ERR: a write to global actual Pstate register has occurred before the global actual Pstate interrupt has left PCBS
26	ROX	PCBS_PMAX_PROTOCOL_ERR: a write to the Pmax/Pmin register has occurred before the Pmax sync interrupt has left PCB
27	ROX	PCBS_IVRM_GROSS_OR_FINE_ERR: iVRM gross or fine error (details to be found in PCBS_ivrm_Control_Status_Reg)
28	ROX	PCBS_IVRM_RANGE_ERR: iVRM range error (summary bit, details to be found in PCBS_ivrm_Control_Status_Reg)
29	ROX	PCBS_DPLL_CPM_FMIN_ERR: DPLL CPM Fmin error
30	ROX	PCBS_DPLL_DCO_FULL_ERR: DPLL DCO full
31	ROX	PCBS_DPLL_DCO_EMPTY_ERR: DPLL DCO empty
32	ROX	PCBS_DPLL_INT_ERR: DPLL internal error
33	ROX	PCBS_FMIN_AND_NOT_CPMBIT_ERR: dpll_fmin_and_not_cpmbit (ref. to dial cpm_fmin_clip_error_sel on how to configure this)
34	ROX	PCBS_DPLL_FASTER_THAN_FMAX_PLUS_DELTA1_ERR: dpll_faster_than_fmax_plus_delta1 (for characterization, delta1 is configurable with pll_char_delta1)
35	ROX	PCBS_DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2_ERR: dpll_slower_than_fmin_minus_delta2 (for characterization, delta2 is configurable with pll_char_delta2)
36	ROX	PCBS_RESCLK_CSB_INSTR_VECTOR_CHG_IN_INVALID_STATE_ERR: RESCLK CSB instruction vector change while FSMs none idle
37	ROX	PCBS_RESCLK_BAND_BOUNDARY_CHG_IN_INVALID_STATE_ERR: RESCLK Band boundaries change while FSMs none idle
38	ROX	PCBS_OCC_HEARTBEAT_LOSS_ERR: OCC heartbeat loss
39	ROX	PCBS_SPARE39_ERR: spare bit, always 0
40	ROX	PCBS_SPARE40_ERR: spare bit, always 0



Bits	PCB	Field Mnemonic: Description
41	ROX	PCBS_SPARE41_ERR: spare bit, always 0
42	ROX	PCBS_SPARE42_ERR: spare bit, always 0

Register Name	<i>PM Error Mask Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PMERRMASK_REG
Address	00000000190F010A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_HANG_ERR_MASK: Mask for this error: 1=masked, 0=not masked
1	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ASSIST_HANG_ERR_MASK: Mask for this error: 1=masked, 0=not masked
2	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
3	RW	PCBS_SLEEP_EXIT_INVOKE_PORE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
4	RW	PCBS_WINKLE_ENTRY_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
5	RW	PCBS_WINKLE_ENTRY_SEND_INT_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
6	RW	PCBS_WINKLE_EXIT_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
7	RW	PCBS_WAIT_DPLL_LOCK_ERR_MASK: Mask for this error: 1=masked, 0=not masked
8	RW	PCBS_SPARE8_ERR_MASK: Mask for this error: 1=masked, 0=not masked
9	RW	PCBS_WINKLE_EXIT_SEND_INT_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
10	RW	PCBS_WINKLE_EXIT_SEND_INT_POWUP_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
11	RW	PCBS_WRITE_FSM_GOTO_REG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
12	RW	PCBS_WRITE_PMGPO_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
13	RW	PCBS_FREQ_OVERFLOW_IN_PSTATE_MODE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
14	RW	PCBS_ECO_RS_BYPASS_CONFUSION_ERR_MASK: Mask for this error: 1=masked, 0=not masked
15	RW	PCBS_CORE_RS_BYPASS_CONFUSION_ERR_MASK: Mask for this error: 1=masked, 0=not masked
16	RW	PCBS_READ_LPST_IN_PSTATE_MODE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
17	RW	PCBS_LPST_READ_CORR_ERR_MASK: Mask for this error: 1=masked, 0=not masked
18	RW	PCBS_LPST_READ_UNCORR_ERR_MASK: Mask for this error: 1=masked, 0=not masked
19	RW	PCBS_PFET_STRENGTH_OVERFLOW_ERR_MASK: Mask for this error: 1=masked, 0=not masked
20	RW	PCBS_VDS_LOOKUP_ERR_MASK: Mask for this error: 1=masked, 0=not masked
21	RW	PCBS_IDLE_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
22	RW	PCBS_PSTATE_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
23	RW	PCBS_GLOBAL_ACTUAL_SYNC_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
24	RW	PCBS_PMAX_SYNC_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked

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Bits	PCB	Field Mnemonic: Description
25	RW	PCBS_GLOBAL_ACTUAL_PSTATE_PROTOCOL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
26	RW	PCBS_PMAX_PROTOCOL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
27	RW	PCBS_IVRM_GROSS_OR_FINE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
28	RW	PCBS_IVRM_RANGE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
29	RW	PCBS_DPLL_CPM_FMIN_ERR_MASK: Mask for this error: 1=masked, 0=not masked
30	RW	PCBS_DPLL_DCO_FULL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
31	RW	PCBS_DPLL_DCO_EMPTY_ERR_MASK: Mask for this error: 1=masked, 0=not masked
32	RW	PCBS_DPLL_INT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
33	RW	PCBS_FMIN_AND_NOT_CPMBIT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
34	RW	PCBS_DPLL_FASTER_THAN_FMAX_PLUS_DELTA1_ERR_MASK: Mask for this error: 1=masked, 0=not masked
35	RW	PCBS_DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2_ERR_MASK: Mask for this error: 1=masked, 0=not masked
36	RW	PCBS_RESCLK_CSB_INSTR_VECTOR_CHG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
37	RW	PCBS_RESCLK_BAND_BOUNDARY_CHG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
38	RW	PCBS_OCC_HEARTBEAT_LOSS_ERR_MASK: Mask for this error: 1=masked, 0=not masked
39	RW	PCBS_SPARE39_ERR_MASK: Mask for this error: 1=masked, 0=not masked
40	RW	PCBS_SPARE40_ERR_MASK: Mask for this error: 1=masked, 0=not masked
41	RW	PCBS_SPARE41_ERR_MASK: Mask for this error: 1=masked, 0=not masked
42	RW	PCBS_SPARE42_ERR_MASK: Mask for this error: 1=masked, 0=not masked

Register Name		PM Special Wakeup FSP
Mnemonic		EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PMSPCWKUPFSP_REG
Address		00000000190F010B (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RW	FSP_SPECIAL_WAKEUP: Chiplet Special Wakeup for FSP Firmware use. NOTE: protocol is required when setting this bit

Register Name		PM Special Wakeup OCC
Mnemonic		EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PMSPCWKUPOCC_REG
Address		00000000190F010C (PCB)
Attributes		
Description		



Bits	PCB	Field Mnemonic: Description
0	RW	OCC_SPECIAL_WAKEUP: Chiplet Special Wakeup for OCC Firmware use. NOTE: protocol is required when setting this bit

Register Name	<i>PM Special Wakeup Hypervisor</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PMSPCWKUPPHYP_REG
Address	00000000190F010D (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	PHYP_SPECIAL_WAKEUP: Chiplet Special Wakeup for hypervisor Firmware use. NOTE: protocol is required when setting this bit

Register Name	<i>PFET Control/Status Register For Core And ECO Vcs</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PFVCSCTLSTAT_REG
Address	00000000190F010E (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	CORE_VCS_PFET_FORCE_STATE: Core Domain PFET Force State Provides a means for firmware to force the core domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 4:5 = 00 (both core_vcs_pfet_val_override AND core_vcs_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
2:3	RW	ECO_VCS_PFET_FORCE_STATE: ECO Domain PFET Force State Provides a means for firmware to force the ECO domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 6:7 = 00 (both eco_vcs_pfet_val_override AND eco_vcs_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
4	RW	CORE_VCS_PFET_VAL_OVERRIDE: Core Domain PFET Value Override 0 = Override is disabled
5	RW	CORE_VCS_PFET_SEL_OVERRIDE: Core Domain PFET Stage Select Override 0 = Override is disabled
6	RW	ECO_VCS_PFET_VAL_OVERRIDE: ECO Domain PFET Value Override 0 = Override is disabled
7	RW	ECO_VCS_PFET_SEL_OVERRIDE: ECO Domain PFET Stage Select Override 0 = Override is disabled

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Bits	PCB	Field Mnemonic: Description
8	RW	CORE_VCS_PFET_ENABLE_REGULATION_FINGER: Core Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the core_vcs_pfet_enable_value.
9	RW	ECO_VCS_PFET_ENABLE_REGULATION_FINGER: ECO Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the eco_vcs_pfet_enable_value.
10:21	RW	CORE_VCS_PFET_ENABLE_VALUE: Core PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the Core Domain PFET Enables directly. If core_vcs_pfet_val_override = 1, a write to this field sets the state of the core PFET Enables until core_vcs_pfet_val_override is cleared. If core_vcs_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the core_vcs_pfet_valN_slac registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
22:25	RW	CORE_VCS_PFET_SEL_VALUE: Core PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure core_vcs_pfet_valN_slac(0:11) where N is 0 to 11 if core_vcs_pfet_sel_override = 1. If core_vcs_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
26:37	RW	ECO_VCS_PFET_ENABLE_VALUE: ECO PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the ECO PFET Enables directly. If ECO_vcs_pfet_val_override = 1, a write to this field sets the state of the ECO PFET Enables until ECO_vcs_pfet_val_override is cleared. If eco_vcs_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the eco_vcs_pfet_valN_slac registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
38:41	RW	ECO_VCS_PFET_SEL_VALUE: ECO PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure eco_vcs_pfet_valN_slac(0:11) where N is 0 to 11 if eco_vcs_pfet_sel_override = 1. If eco_vcs_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
42:45	ROX	CORE_VCS_PG_STATE: Core power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
46:49	ROX	CORE_VCS_PG_SEL: For debug, contains the actual index n into Core Domain PFET Value [n] SLAT Register set that contains the Core PFET Enable Value currently enabled.
50:53	ROX	ECO_VCS_PG_STATE: ECO Domain power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
54:57	ROX	ECO_VCS_PG_SEL: For debug, contains the actual index n into ECO Domain PFET Value [n] SLAT Register set that contains the ECO PFET Enable Value currently enabled.



Register Name	<i>PM State History Register For Hypervisor</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPHYP_REG
Address	00000000190F0110 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	PHYP_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPART	PHYP_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPART	PHYP_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPART	PHYP_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPART	PHYP_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPART	PHYP_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For FSP</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PMSTATEHISTFSP_REG
Address	00000000190F0111 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	FSP_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPART	FSP_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPART	FSP_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPART	FSP_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.

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Bits	PCB	Field Mnemonic: Description
6	ROX_CLRPAR T	FSP_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	FSP_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For OCC</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PMSTATEHISTOCC_REG
Address	00000000190F0112 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	OCC_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	OCC_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	OCC_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	OCC_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	OCC_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	OCC_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For PerfMon</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPERF_REG
Address	00000000190F0113 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	PERF_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	PERF_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	PERF_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	PERF_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	PERF_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	PERF_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM FSM Reset And Babystepper Idle Injects</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.IDLEFSMGOTOCMD_REG
Address	00000000190F0114 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	WO_1P	idle_fsm_goto_cmd ' A write to this reg will proceed the IDLE FSM from WAIT_FOR_PORE_DONE, SLEEP_EXIT_WAIT_FOR_PORE_FAST_EXIT_DONE, or WINKLE_EXIT_WAIT_FOR_PORE_FAST_EXIT_DONE to the following states: '0b01: goto IDLE state' '0b10: goto SLEEP_EXIT_CORE_MESHLET_ON state' '0b11: goto WINKLE_EXIT_NOTIFY_PMC state '
2	RWX	babystp_trigger_sleep_entry ' A write to this reg with a 1 in this field will cause the babystepper to run the sleep entry sequence. This step is needed for an assisted entry into sleep, before the power is actually turned off since the babystepper needs to know about the sleep state. For an unassisted entry, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished entering its sleep mode. '
3	RWX	babystp_trigger_winkle_entry ' A write to this reg with a 1 in this field will cause the babystepper to run the winkle entry sequence. This step is needed for an assisted entry into winkle before the power is actually turned off since the babystepper needs to know about the winkle state. For an unassisted entry, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished entering its winkle mode. '
4	RWX	babystp_trigger_wakeup ' A write to this reg with a 1 in this field will cause the babystepper to run the wakeup sequence from sleep/winkle depending on the babystepper state of sleep or winkle. This step is needed for an assisted exit from winkle before the power is actually turned off since the babystepper needs to know about the wakeup state. For an unassisted exit, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished waking up from sleep or winkle. '

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Register Name	Core PFET Power Up Delay
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.COREPFPUDLY_REG
Address	00000000190F012C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_POWUP_DLY0: Delay used after transitioning to Core Domain power up sequence stage0. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	CORE_POWUP_DLY1: Delay used after transitioning to Core domain power up sequence stage1.
8:19	RW	CORE_POWER_UP_DELAY_SEL: Vector select for which delay to use for the respective power-up stage. Bit mapping: 8 -> core_*_pfet_enable(0) 9 -> core_*_pfet_enable(1) ... 19 -> core_*_pfet_enable(11) Bit meaning: 0 = Use core_powup_dly0 1 = Use core_powup_dly1

Register Name	Core PFET Power Down Delay
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.COREPFPDDLY_REG
Address	00000000190F012D (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_POWDN_DLY0: Delay used after transitioning to Core domain power dn sequence stage1. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	CORE_POWDN_DLY1: Delay used after transitioning to Core domain power dn sequence stage1. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
8:19	RW	CORE_POWER_DN_DELAY_SEL: Vector select for which delay to use for the respective power-dn stage. Bit mapping: 8 -> core_*_pfet_enable(0) 9 -> core_*_pfet_enable(1) ... 19 -> core_*_pfet_enable(11) Bit meaning: 0 = Use core_powdn_dly0 1 = Use core_powdn_dly1



Register Name	Core PFET Vretention	
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.COREPFVRET_REG	
Address	00000000190F0130 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_VRET_SEL: Pointer to the stage representing the Vretention value for the core PFETs. Power down sequences will stop after enabling this stage.
4:7	RW	CORE_VOFF_SEL: Pointer to the stage representing the Voff value for the core PFETs. Power down sequences will stop after enabling this stage.

Register Name	ECO PFET Power Up Delay	
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.ECOPFPUDLY_REG	
Address	00000000190F014C (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_POWUP_DLY0: Delay used after transitioning to ECO domain power up sequence stage0 in terms of refclk period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	ECO_POWUP_DLY1: Delay used after transitioning to ECO domain power up sequence stage1.
8:19	RW	ECO_POWER_UP_DELAY_SEL: Vector select for which delay to use for the respective power-up stage. Bit mapping: 8 -> eco_*_pfet_enable(0) 9 -> eco_*_pfet_enable(1) ... 19 -> eco_*_pfet_enable(11) Bit meaning: 0 = Use eco_powup_dly0 1 = Use eco_powup_dly1

Register Name	ECO PFET Power Down Delay	
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.ECOPFPDDLY_REG	
Address	00000000190F014D (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_POWDN_DLY0: UNUSED/SPARE
4:7	RW	ECO_POWDN_DLY1: Delay used after transitioning to ECO Domain power dn sequence stage1. The delays in this register are in terms of refclk period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.

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Bits	PCB	Field Mnemonic: Description
8:19	RW	ECO_POWER_DN_DELAY_SEL: Vector select for which delay to use for the respective power-down stage. Bit mapping: 8 -> eco_*_pfet_enable(0) 9 -> eco_*_pfet_enable(1) ... 19 -> eco_*_pfet_enable(11) Bit meaning: 0 = Use eco_powdn_dly0 1 = Use eco_powdn_dly1

Register Name		<i>ECO PFET Vretention</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.ECOPFVRET_REG
Address		00000000190F0150 (PCB)
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_VRET_SEL: Pointer to the stage representing the Vretention value for the ECO PFETs. Power down sequences will stop after enabling this stage.
4:7	RW	ECO_VOFF_SEL: Pointer to the stage representing the Voff value for the ECO PFETs. Power down sequences will stop after enabling this stage.

Register Name		<i>Frequency Control Register With Overrides For DPLL</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.FREQ_CTRL_REG
Address		00000000190F0151 (PCB)
Attributes		
Description		Note that overrides to Dpll_fmax are only applied if Dpll_freq_override_enable = 1. A read of all these dials always returns the currently established DPLL frequencies (regardless of any other mode settings).

Bits	PCB	Field Mnemonic: Description
0:8	RWX	DPLL_FMIN: minimum DPLL frequency in CPM-DPLL mode that is set at IPL time A read always returns the currently established value A write is not conditioned on any other dial setting.
9:17	RWX	DPLL_FMAX: DPLL maximum frequency and frequin (these two values are the same in POWER8 processor) without applying bias values: A read always returns the currently established value A write is conditioned on the setting of dpll_freq_override_enable. If dpll_freq_override_enable is asserted, a write causes this field to update. Otherwise the hardware (that is, PStates) are controlling the update of this value.
18:21	RO	Reserved.
22:30	RW	FREQU_AT_PSTATE0: DPLL frequency for Pstate 0



Register Name	<i>DPLL Mode Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.DPLL_CPM_PARM_REG
Address	00000000190F0152 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	LF_SLEWRATEXPI: out of lock slew rate for DPLL
8	RW	LF_USE_CPMXPI: use CPM instead of PFD as loop filter input, if '1' (instead of using both)
9	RW	FF_USE_CPMXPI: use the CPM inputs for the frequency filter, if '1'
10	RW	CPM_FILTER_ENABLE: enables the CPM filter
11	RW	FF_BYPASSXPI: enables frequency filter bypass
12	RW	DCO_OVERRIDE: enables overrides for DCO testing/characterization
13	RW	DCO_INCR: enables increment for DCO testing/characterization, increments only on a rising edge
14	RW	DCO_DECR: enables decrement for DCO testing/characterization, decrements only on a rising edge
15:23	RW	DPLL_LOCK_TIMER_REPLACEMENT_VALUE: if dpll_lock_replacement_timer_mode_en is set, this dial specifies the delay in us, after which it is assumed, that the DPLL has reached a frequency lock condition. Note that values less than 3 will cause in undefined HW behavior (0 will cause HANGs!). if dpll_lock_replacement_timer_mode_en is zero, this dial specifies the delay in pcb_nclk cycles after which the hardware monitors the DPLL frequout output (if dpll_freqout_mode_en is set) or the DPLL flock output (if dpll_flock_mode_en is set). Note that in this case, the value of this dial needs to be greater or equal to 150 (decimal).
24:31	RW	PRE_VRET_PSTATE: Pstate that is stepped to before switching to Vretention defined in PCBS_iVRM_Control_Status_Reg
32	RW	OVERRIDE_PCBS_DPLL_SYNCHRONIZER: Bypasses the 'ping-pong' synchronization logic between the DPLL and the PCBS-PM. NEVER SET TO 1 UNLESS YOU KNOW WHAT YOU ARE DOING!
33:36	RW	DPLL_CHAR_DELTA1: Delta in DPLL ticks for characterization (cf. dial dpll_faster_than_fmax_plus_delta1)
37:40	RW	DPLL_CHAR_DELTA2: Delta in DPLL ticks for characterization (cf. dial dpll_faster_than_fmin_minus_delta2)

Register Name	<i>PPMSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_STATUS_REG
Address	00000000190F0153 (PCB)
Attributes	
Description	Provides read access to the power management status that is also shadowed to the PC and visible to the hypervisor in the PMSR (with some delay due to the shadowing process).

Bits	PCB	Field Mnemonic: Description
0:7	ROX	global_pstate_actual ' Actual Global Pstate Pstate or Pglobal_actual' " Reads from this field return the presently established global PState value.' " Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent '

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Bits	PCB	Field Mnemonic: Description
8:15	ROX	LOCAL_PSTATE_ACTUAL: ' Actual Local PState or Plocal_actual' " 'Reads from this field return the presently established local PState value. This value will always be less than or equal to global_pstate_actual.' " 'Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent' "
16:23	ROX	pv_min Minimum Pstate set by the platform.
24:31	ROX	pvf_max Maximum Pstate set by the platform.
32	ROX	spr_em_disabled ' SPR Energy Management Disabled' 'Read from this field indicate whether the platform has disabled the ' 'PMCR and PMICR SPRs to control the chiplet PState. '
33	ROX	Psafe_mode_active Read from this field indicate whether the chiplet has been put into a safe mode with Psafe enabled to a OCC heartbeat loss or other externally forced reasons (0=regular mode, 1=safe mode is active)
34	ROX	iVRM_safe_mode_active Read from this field indicate whether the chiplet has been put the iVRM safe mode (forcing the bypass mode for all iVRMs)
35	ROX	ivrm_enable Read from this field indicate whether the chiplet internal voltage regulation macro is enabled for localized voltage control (0=disabled, 1=enabled) based on ANDing the poweron signals to the iVRMs
36	ROX	all_fsms_in_safe_state For recovery: if this bit is asserted, all Pstate and iVRM control FSMs are in a stable, safe state that allows the recovery routine to proceed with resetting the PCBS PM without the risk of interrupt a critical action
37:40	ROX	pmsr_spares spare bits

Register Name	<i>PIVRMCSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_CONTROL_STATUS_REG
Address	00000000190F0154 (PCB)
Attributes	
Description	Provides access to chiplet-level controls of the internal VRM rail set (VDD and VCS) across both the core and ECO domains. The following is valid only for bits 4 to 7. When in automatic iVRM mode (ivrm_fsm_enable = 1), these bits provide access to the values established by the automatic hardware mechanism. When In iVRM override mode (ivrm_fsm_enable = 0), these bits allow firmware direct control of the values driving the internal VRMs.

Bits	PCB	Field Mnemonic: Description
0	RW	IVRM_FSM_ENABLE: Internal master VRM FSM Enable 0 = Disable Internal VRM FSMs and enable to control the iVRMs with the available override registers (SCOMable) as a backup mode or for setup (override mode) 1 = Enable Internal VRM FSM sequencers (requires that Pstates are enabled with enable_Pstate_mode=1 as well) (automatic mode)
1	RW	USE_IVRM_FOR_VRET: Internal VRM Enabled for Vretention 0 = Disable Internal VRM for Vretention 1 = Enable Internal VRM for Vretention
2	RW	BINSEARCH_CAL_ENA: trigger binary search (level signal)

Bits	PCB	Field Mnemonic: Description
3	RW	PVREF_EN: Internal VRM Power Voltage Reference Forced Enable 0 = Allow hardware to enable/disable pvref circuit 1 = Force enablement of the pvref circuit
4	RWX	IVRM_CORE_VDD_BYPASS_B: Internal VRM Core VDD Bypass (negative active) 0 = VDD Internal Core VRMs in bypass 1 = VDD internal Core VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
5	RWX	IVRM_CORE_VDD_POWERON: Internal VRM Core VDD Poweron 0 = Core VDD Internal VRMs powered off 1 = Core VDD internal VRMs powered on if this bit is not set (=0), the Core VDD internal VRM powered off internally. If this bit is set (=1), the Core VDD internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
6	RWX	IVRM_CORE_VCS_BYPASS_B: Internal VRM Core VCS Bypass (negative active) 0 = VCS Internal Core VRMs in bypass 1 = VCS internal Core VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VCS internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VCS internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
7	RWX	IVRM_CORE_VCS_POWERON: Internal VRM Core VCS Poweron 0 = Core VCS Internal VRMs powered off 1 = Core VCS internal VRMs powered on if this bit is not set (=0), the Core VCS internal VRM powered off internally. If this bit is set (=1), the Core VCS internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
8	RWX	IVRM_ECO_VDD_BYPASS_B: Internal VRM ECO VDD Bypass (negative active) 0 = VDD Internal ECO VRMs in bypass 1 = VDD internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
9	RWX	IVRM_ECO_VDD_POWERON: Internal VRM ECO VDD Bypass (negative active) 0 = VDD Internal ECO VRMs in bypass 1 = VDD internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.

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Bits	PCB	Field Mnemonic: Description
10	RWX	IVRM_ECO_VCS_BYPASS_B: Internal VRM ECO VCS Bypass (negative active) 0 = VCS Internal ECO VRMs in bypass 1 = VCS internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VCS internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VCS internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
11	RWX	IVRM_ECO_VCS_POWERON: Internal VRM ECO VCS Poweron 0 = ECO VCS Internal VRMs powered off 1 = ECO VCS internal VRMs powered on if this bit is not set (=0), the ECO VCS internal VRM powered off internally. If this bit is set (=1), the ECO VCS internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
12:18	RWX	IVRM_VRET_VDD: if use_ivrm_for_Vret is asserted, this dial is used to control the Vdd retention voltage. Note: this field will establish the Core VDD rail for Sleep and both the Core and ECO rail for Winkle. - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
19:25	RWX	IVRM_VRET_VCS: if use_ivrm_for_Vret is asserted, this dial is used to control the Vcs retention voltage. Note: this field will establish the Core VDD rail for Sleep and both the Core and ECO rail for Winkle. - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
26:30	RWX	IVRM_VRET_CORE_VDD_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the Core Vdd iVRM PFET strength for the retention voltage
31:35	RWX	IVRM_VRET_CORE_VCS_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the Core Vcs iVRM PFET strength for the retention voltage
36:40	RWX	IVRM_VRET_ECO_VDD_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the ECO Vdd iVRM PFET strength for the retention voltage
41:45	RWX	IVRM_VRET_ECO_VCS_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the ECO Vcs iVRM PFET strength for the retention voltage
46	RW	PVREF_FAIL: voltage reference fail input to iVRMs
47	ROX	IVRM_PREF_ERROR_GROSS: Voltage Reference Gross Error 0 = Gross Error not detected 1 = Gross Error detected
48	ROX	IVRM_PREF_ERROR_FINE: Voltage Reference Fine Error 0 = Fine Error not detected 1 = Fine Error detected
49	ROX	IVRM_CORE_VDD_RANGE_HI: Core VDD Internal VRM Range Hi Indicator 0 = Core VDD Internal VRM Hi indicator signal not asserted 1 = Core VDD internal VRMs Hi indicator signal asserted
50	ROX	IVRM_CORE_VDD_RANGE_LO: Core VDD Internal VRM Range Low Indicator 0 = Core VDD Internal VRM Low indicator signal not asserted 1 = Core VDD internal VRMs Low indicator signal asserted

Bits	PCB	Field Mnemonic: Description
51	ROX	IVRM_ECO_VDD_RANGE_HI: ECO VDD Internal VRM Range Hi Indicator 0 = ECO VDD Internal VRM Hi indicator signal not asserted 1 = ECO VDD internal VRMs Hi indicator signal asserted
52	ROX	IVRM_ECO_VDD_RANGE_LO: ECO VDD Internal VRM Range Low Indicator 0 = ECO VDD Internal VRM Low indicator signal not asserted 1 = ECO VDD internal VRMs Low indicator signal asserted
53	ROX	IVRM_CORE_VCS_RANGE_HI: Core VCS Internal VRM Range Hi Indicator 0 = Core VCS Internal VRM Hi indicator signal not asserted 1 = Core VCS internal VRMs Hi indicator signal asserted
54	ROX	IVRM_CORE_VCS_RANGE_LO: Core VCS Internal VRM Range Low Indicator 0 = Core VCS Internal VRM Low indicator signal not asserted 1 = Core VCS internal VRMs Low indicator signal asserted
55	ROX	IVRM_ECO_VCS_RANGE_HI: ECO VCS Internal VRM Range Hi Indicator 0 = ECO VCS Internal VRM Hi indicator signal not asserted 1 = ECO VCS internal VRMs Hi indicator signal asserted
56	ROX	IVRM_ECO_VCS_RANGE_LO: ECO VCS Internal VRM Range Low Indicator 0 = ECO VCS Internal VRM Low indicator signal not asserted 1 = ECO VCS internal VRMs Low indicator signal asserted
57	ROX	BINSEARCH_CAL_DONE: binary search done signal
58	RWX	IVRM_CORE_VDD_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
59	RWX	IVRM_CORE_VCS_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
60	RWX	IVRM_ECO_VDD_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
61	RWX	IVRM_ECO_VCS_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
62	RW	IVRM_POWER_DOWN_DISABLE: If this bit is 1, the iVRM poweron signal is left asserted. Power off of the iVRMs is then blocked

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Register Name	<i>PIVRMVSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VALUE_SETTING_REG
Address	00000000190F0155 (PCB)
Attributes	
Description	Allows access to VID values and PFET strength valid signal settings presented to the internal VRM rail set (VDD and VCS) across both the core and ECO domains. When in <code>ivrm_fsm_enable = "auto"</code> mode, this register provides access to the values established by the automatic hardware mechanism. When <code>ivrm_fsm_enable = "override"</code> mode, this register allows firmware direct control of the values driving the internal VRMs which, if the VRMs are not in bypass, will move the voltage settings.

Bits	PCB	Field Mnemonic: Description
0:7	RWX	IVRM_CORE_VDD_IVID: When read, returns the value presently being driving to the Core VDD iVRM. If <code>ivrm_fsm_enable = 0</code> (<code>override_mode</code>), then writes to this field will drive a new VID value to the Core VDD iVRM. If <code>ivrm_fsm_enable = 1</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
8:15	RWX	IVRM_CORE_VCS_IVID: When read, returns the value presently being driving to the Core VCS iVRM. If <code>ivrm_fsm_enable = 0</code> (<code>override_mode</code>), then writes to this field will drive a new VID value to the Core VCS iVRM. If <code>ivrm_fsm_enable = 1</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
16:23	RWX	IVRM_ECO_VDD_IVID: When read, returns the value presently being driving to the Core VDD iVRM. If <code>ivrm_fsm_enable = 0</code> (<code>override_mode</code>), then writes to this field will drive a new VID value to the ECO VDD iVRM. If <code>ivrm_fsm_enable = 1</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
24:31	RWX	IVRM_ECO_VCS_IVID: When read, returns the value presently being driving to the ECO VCS iVRM. If <code>ivrm_fsm_enable = 0</code> (<code>override_mode</code>), then writes to this field will drive a new VID value to the ECO VCS iVRM. If <code>ivrm_fsm_enable = 0</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
32:36	RWX	IVRM_CORE_VDD_PFET_STRENGTH: When read, returns the value presently being driving to the core VCS iVRM. If <code>ivrm_fsm_enable = 0</code> (<code>override_mode</code>), then writes to this field will drive a new strength value to the core VCS iVRM. If <code>ivrm_fsm_enable = 0</code> , writes to this field are not performed.

Bits	PCB	Field Mnemonic: Description
37:41	RWX	IVRM_CORE_VCS_PFET_STRENGTH: This register is assigned to the signals tcex##_tp_ivrm_core_vcs_sense & tcex##_tp_ivrm_core_vdd_sense & tcex##_tp_ivrm_eco_vcs_sense & tcex##_tp_ivrm_eco_vdd_sense & 0b0 Note that all other sense signals are spares now and tied to 0. OUTDATED TEXT: When read, returns the value presently being driving to the core VDD iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the core VDD iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
42:46	RWX	IVRM_ECO_VDD_PFET_STRENGTH: When read, returns the value presently being driving to the ECO VCS iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the ECO VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
47:51	RWX	IVRM_ECO_VCS_PFET_STRENGTH: When read, returns the value presently being driving to the ECO VDD iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the ECO VDD iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
52	RWX	IVRM_VDD_CORE_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the Core VDD iVRM. If ivrm_fsm_enable = 1 AND ivrm_control_mode = 1 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the Core VDD iVRM, If ivrm_fsm_enable = 0 OR ivrm_control_mode = 0, writes to this field are not performed.
53	RWX	IVRM_VCS_CORE_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the Core VCS iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the Core VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
54	RWX	IVRM_VDD_ECO_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the ECO VDD iVRM. If ivrm_fsm_enable = 1 AND ivrm_control_mode = 1 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the ECO VDD iVRM, If ivrm_fsm_enable = 0 OR ivrm_control_mode = 0, writes to this field are not performed.
55	RWX	IVRM_VCS_ECO_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the ECO VCS iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the ECO VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
56	RWX	CORE_VDD_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
57	RWX	CORE_VCS_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
58	RWX	ECO_VDD_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
59	RWX	ECO_VCS_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.

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Register Name		General PCBS Modes And Chicken Switches
Mnemonic		EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBSPM_MODE_REG
Address		00000000190F0156 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RW	ENABLE_PSTATE_MODE: if asserted, Pstate requests (from overrides or PMCR) will be honored, otherwise, the hardware does not do anything. Note to firmware: this is the master switch for Pstates and should be asserted after all sub-modes (that is, lvrn_fsm_en) are setup to avoid enabling unintentional modes during the mode setup.
1	RW	GLOBAL_PSTATE_CHANGE_FOR_IDLE_STATE_ENABLED: if asserted, a global Pstate change to the Nap/Sleep/Winkle-Pstate is requested, when the Nap/Sleep/Winkle state is entered and the individual enable bits in the PIMCR are asserted
2	RW	ENABLE_GLOBAL_PSTATE_REQ: if '1' then enable PMC interrupt with global Pstate change request, otherwise, disable global requests
3	RW	ENABLE_WINKLE_WITH_CPM_MODE: if '1', PCBS automatically changes the DPLL mode to mode 1, when entering winkle, but changes the mode back to CPM mode when exiting. Needed for CPM-DPLL control loop enablement.
4	RW	ENABLE_CLIPPING_OF_GLOBAL_PSTATE_REQ: if '1', PCBS automatically clips global Pstate requests with Pvf_max in PPMBR and sets the 'donate' bit in the interrupt accordingly
5	RW	CHKSW_HW214553: if deasserted, HW214553 (frequin issue in resclk mode) is fixed, if asserted, the fix is not active
6	RW	ENABLE_PMC_PMAX_SYNC_NOTIFICATION: if asserted, the PCBS-PM will send a 'Pmax_sync' interrupt, once the synchronization criterion is met
7	RW	DPLL_LOCK_REPLACEMENT_TIMER_MODE_EN: Select a timer instead of the DPLL lock bit as target frequency reached criterion. This timer has to be setup by the dial dpll_lock_timer_replacement_value. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
8	RW	DPLL_FREQOUT_MODE_EN: Looks at the DPLL frequout to find out, if the target frequency has been reached. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
9	RW	DPLL_FLOCK_MODE_EN: Looks at the real DPLL flock output to find out, if the target frequency has been reached. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
10	RW	ENABLE_SENSE_DELAY_CHARACTERIZATION: If this switch is 0, the sense latches are updated every cycle. If this switch is 1, the sense delay measurement mode is enabled, that starts a sense delay timer, whenever one of the registers that drive the inputs of the iVRMs/pFETs is written via PCB and that triggers a sense register freeze operation, when the sense delay timer reaches the value sense_delay_timer_val. With this mode, the sense delays can be measured in multiples of the PCB-slave clock speed.
11:17	RW	SENSE_DELAY_TIMER_VAL: See the description of enable_sense_delay_characterization for details.
18:19	RW	CPM_FMIN_CLIP_ERROR_SEL: This dial selects, which of the following conditions will cause the FIR bit dpll_fmin_and_not_cpmbit to be set to detect, that the DPLL runs at Fmin, but is still clipped by the CPMs. 0b00 = function is disabled 0b01 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit2 = 0 0b10 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit1 = 0 0b11 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit0 = 0
20:23	RW	DBG_TRACE_SEL: This dial selects the group of signals to be traced for debug in the lab. Details to be found in the Section 'Trace Bus'

Bits	PCB	Field Mnemonic: Description
24:25	RW	TRACE_DATA_SEL: This dial selects the group of signals to be traced for debug in the lab. Details to be found in the Section 'Trace Bus'
26:29	RW	TP_CPLT_IVRM_VPP_TUNE: Tune bits to be set going to the iVRMs

Register Name	<i>PIVRMPS Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_PFETSTR_SENSE_REG
Address	00000000190F0157 (PCB)
Attributes	
Description	Used to check that the pFET sense outputs correspond to the driven values (mainly for test).

Bits	PCB	Field Mnemonic: Description
0:4	ROX	IVRM_CORE_VDD_PFETSTR_SNS: Not used any more.
5:9	ROX	IVRM_CORE_VCS_PFETSTR_SNS: This register is assigned to the signals tcex##_tp_ivrm_core_vcs_sense & tcex##_tp_ivrm_core_vdd_sense & tcex##_tp_ivrm_eco_vcs_sense & tcex##_tp_ivrm_eco_vdd_sense & 0b0
10:14	ROX	IVRM_ECO_VDD_PFETSTR_SNS: Not used any more.
15:19	ROX	IVRM_ECO_VCS_PFETSTR_SNS: Not used any more.
20	ROX	IVRM_VDD_CORE_PFETSTR_VALID_SNS: Not used any more.
21	ROX	IVRM_VCS_CORE_PFETSTR_VALID_SNS: Not used any more.
22	ROX	IVRM_VDD_ECO_PFETSTR_VALID_SNS: Not used any more.
23	ROX	IVRM_VCS_ECO_PFETSTR_VALID_SNS: Not used any more.
24	ROX	CORE_VDD_BYPASS_B_SENSE: Not used any more.
25	ROX	CORE_VCS_BYPASS_B_SENSE: Not used any more.
26	ROX	ECO_VDD_BYPASS_B_SENSE: Not used any more.
27	ROX	ECO_VCS_BYPASS_B_SENSE: Not used any more.
28	ROX	CORE_VDD_POWERON_SENSE: Not used any more.
29	ROX	CORE_VCS_POWERON_SENSE: Not used any more.
30	ROX	ECO_VDD_POWERON_SENSE: Not used any more.
31	ROX	ECO_VCS_POWERON_SENSE: Not used any more.
32	ROX	CORE_VDD_VPUMP_EN_SENSE: Not used any more.
33	ROX	CORE_VCS_VPUMP_EN_SENSE: Not used any more.
34	ROX	ECO_VDD_VPUMP_EN_SENSE: Not used any more.
35	ROX	ECO_VCS_VPUMP_EN_SENSE: Not used any more.
36	ROX	CORE_VDD_PFET_LOW_VOUT_SNS: Not used any more.
37	ROX	CORE_VCS_PFET_LOW_VOUT_SNS: Not used any more.
38	ROX	ECO_VDD_PFET_LOW_VOUT_SNS: Not used any more.
39	ROX	ECO_VCS_PFET_LOW_VOUT_SNS: Not used any more.

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Register Name	PPMICR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_IDLE_CONTROL_REG
Address	00000000190F0158 (PCB)
Attributes	
Description	Used to read the PMICR register typically owned (written) by the hypervisor. Writes are conditioned on the setting of the dial Pm_spr_override_en. If Pm_spr_override_en is set, firmware must make sure that the special wakeup state of this chiplet is reached before changing any of the latency fields in this register. Otherwise, the hardware behavior is undefined.

Bits	PCB	Field Mnemonic: Description
0:7	ROX	NAP_PSTATE_REQ: Nap Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
8	ROX	NAP_PSTATE_EN: Nap PState Enable 1 = Enable the Nap Pstate (NPS) Request, Nap Global Enable and Nap Latency functions 0 = Disables the Nap Pstate (NPS) Request, Nap Global Enable and Nap Latency functions Reads from the field return the value last written.
9	ROX	NAP_GLOBAL_EN: Nap Global Enable 1 = Upon the execution of a Nap instruction , the Nap Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a Nap instruction , the Nap Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.
10:11	ROX	NAP_LATENCY: Nap Latency not supported for POWER8 processor
12:15	ROX	RESERVED_PPMICR_0: reserved
16:23	ROX	SLEEP_PSTATE_REQ: sleep Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
24	ROX	SLEEP_PSTATE_EN: sleep PState Enable 1 = Enable the sleep Pstate (NPS) Request, sleep Global Enable and sleep Latency functions 0 = Disables the sleep Pstate (NPS) Request, sleep Global Enable and sleep Latency functions Reads from the field return the value last written.
25	ROX	SLEEP_GLOBAL_EN: sleep Global Enable 1 = Upon the execution of a sleep instruction , the sleep Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a sleep instruction , the sleep Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.

Bits	PCB	Field Mnemonic: Description
26:27	ROX	SLEEP_LATENCY: sleep Latency 00 = Cease instructions and honors Pstate change but does not perform additional state changing actions (unsupported in POWER8, maps to 0b10) 01 = Indicates to the platform that a sub-state that would have the lowest latency is enabled (unsupported in POWER8, maps to 0b10) 10 = Indicates to the platform that a sub-state that might have a medium exit latency is enabled (POWER8: Fast Sleep) 11 = Indicates to the platform that a sub-state that might have higher exit latency is enabled (POWER8: Deep Sleep)
28:31	ROX	RESERVED_PPMICR_1: reserved
32:39	ROX	WINKLE_PSTATE_REQ: winkle Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
40	ROX	WINKLE_PSTATE_EN: winkle PState Enable 1 = Enable the winkle Pstate (NPS) Request, winkle Global Enable and winkle Latency functions 0 = Disables the winkle Pstate (NPS) Request, winkle Global Enable and winkle Latency functions Reads from the field return the value last written.
41	ROX	WINKLE_GLOBAL_EN: winkle Global Enable 1 = Upon the execution of a winkle instruction , the winkle Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a winkle instruction , the winkle Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.
42:43	ROX	WINKLE_LATENCY: winkle Latency 00 = Cease instructions and honors Pstate change but does not perform additional state changing actions (unsupported in POWER8, maps to 0b10) 01 = Indicates to the platform that a sub-state that would have the lowest latency is enabled (unsupported in POWER8, maps to 0b10) 10 = Indicates to the platform that a sub-state that might have a medium exit latency is enabled (POWER8: Fast Winkle) 11 = Indicates to the platform that a sub-state that might have higher exit latency is enabled (POWER8: Deep Winkle)
44:47	ROX	RESERVED_PPMICR_2: reserved

Register Name	PPMCR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_CONTROL_REG
Address	00000000190F0159 (PCB)
Attributes	
Description	Provides read access to the PMCR register shadow in the PCBS, typically owned (written) by the hypervisor. Writes are conditioned on the setting of PMGP1[pm_spr_override_en].

Bits	PCB	Field Mnemonic: Description
0:7	RWX	GLOBAL_PSTATE_REQ: global Pstate request from pHyp (or OCC)
8:15	RWX	LOCAL_PSTATE_REQ: local Pstate request from hypervisor or OCC
16	RWX	AUTO_OVERRIDE0_PSTATE_LIMIT_EN: automatic override Pstate 0 (for low activity detection) is enabled, if asserted



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Bits	PCB	Field Mnemonic: Description
17	RWX	AUTO_OVERRIDE1_PSTATE_LIMIT_EN: automatic override Pstate 1 (reserved for future use) is enabled, if asserted
18:23	RWX	RESERVED_PPMCR: reserved
24:31	RWX	AUTO_OVERRIDE_PSTATE0: automatic override Pstate 0 (for low activity detection)
32:39	RWX	AUTO_OVERRIDE_PSTATE1: automatic override Pstate 1 (reserved for future use)

Register Name	<i>Control Register That Is Written By PMC Sequencer</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_PMC_VF_CTRL_REG
Address	00000000190F015A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PGLOBAL_ACTUAL: global actual Pstate
8:15	RW	MAXREGVCS: maximum regulation point for Vcs, Bit 0 is reserved, bits 1 to 7 are in iVID format
16:23	RW	MAXREGVDD: maximum regulation point for Vdd, Bit 0 is reserved, bits 1 to 7 are in iVID format
24:31	RW	EVIDVCS_EFF: eff. external voltage ID for Vcs in iVID format, Bit 0 is reserved
32:39	RW	EVIDVDD_EFF: eff. external voltage ID for Vdd in iVID format, Bit 0 is reserved

Register Name	<i>Undervolting Register For PCBS</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_UNDERVOLTING_REG
Address	00000000190F015B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PUV_MIN: minimum Pstate for which undervolting is allowed
8:15	RW	PUV_MAX: maximum Pstate for which undervolting is allowed
16:21	RW	KUV: this value indicates how many Pstate ticks a voltage request is undervolted (clipped with Puv_min). Note that the Kuv value is signed

Register Name	<i>PPSIBR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_INDEX_BOUND_REG
Address	00000000190F015C (PCB)
Attributes	
Description	Enables setting the minimum and maximum Pstate that is supported as a pointer into the local Pstate table (which has entries from 0 to 127).



Bits	PCB	Field Mnemonic: Description
0:7	RW	LPSI_MIN: this Pstate index is the index that corresponds to array entry 0. Note that the index domain is obtained by adding 128 to a Pstate, thus, the value is unsigned.
8:14	RW	LPSI_ENTRIES_MINUS_1: this dial contains the value of the number of entries in the Pstate table minus 1

Register Name	<i>PPMBR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_BOUNDS_REG
Address	00000000190F015D (PCB)
Attributes	
Description	Enables setting the Pstate bounds that are managed by the OCC. If dial Enable_pmc_pmax_sync_notification is set, firmware must wait after each write to this register until the PMC has received the Pmax Sync Interrupt. If a write happens to this register while the previously scheduled Pmax Sync Interrupt has not yet left PCBS, the error TBD will be set.

Bits	PCB	Field Mnemonic: Description
0:7	RW	PMIN_CLIP: minimum Pstate allowed for this chiplet
8:15	RW	PMAX_CLIP: maximum Pstate allowed for this chiplet (has to be greater or equal to Pmin_clip)

Register Name	<i>PPTCR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_CTRL_REG
Address	00000000190F015E (PCB)
Attributes	
Description	Controls the address for writing the local Pstate table array (all 96 words are accessible). Note that the protocol requires this register to be set up with the Pstate address first, if a read or a write of the Pstate array is intended, to make sure that the initial address is set correctly. The register PPTR must always be written or read afterward. Note that any access to the PPTR auto-increments this register.

Bits	PCB	Field Mnemonic: Description
0:6	RWX	PSTATE_TABLE_ADDRESS: This is the address of the Pstate table in PCBS, which is auto-incremented after any access to the PTLR.

Register Name	<i>PPTR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_REG
Address	00000000190F015F (PCB)
Attributes	
Description	Controls the data to be written into the Pstate table and returns the data for a read of the Pstate table. Note that the protocol requires for a write to set this register up after first setting up PPTCR (if the user does not rely on the auto-increment function of the address). For a read of the Pstate table, this register must be read after first setting up PPTCR as well (again if the auto-increment feature of the address is not used). Any access to this register auto-increments the Pstate_table_address by 1. Note also that the read functionality of this register is only functional if PIVRMCSR[ivrm_fsm_enable] = 0. The write functionality works in any case.

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Bits	PCB	Field Mnemonic: Description
0:63	RW	pstate_data This is the field for data bits 0 to 63

Register Name	PPSTR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_STEP_TARGET_REG
Address	00000000190F0160 (PCB)
Attributes	
Description	Provides read access to several intermediate values in the Pstate computation pipeline. Writes are conditioned on the setting of PMGP0[enable_OCC_ctrl_for_local_Pstate_eff_req].

Bits	PCB	Field Mnemonic: Description
0:7	RWX	LOCAL_PSTATE_EFF_REQ: this field represents the effective local Pstate request right before the clipping with Pmin and Pmax if enable_OCC_ctrl_for_local_Pstate_eff_req=0 then the hardware controls this dial, that updates every cycle if enable_OCC_ctrl_for_local_Pstate_eff_req=1 then OCC is in control and can write this field to control the effective local Pstate request that will eventually propagate through the downstream logic and determine the Local PState Actual. Note: if no write to this register is performed, the currently established value is maintained stable forever.
8:15	ROX	LOCAL_PSTATE_TARGET: This field is the target Pstate of a complete Pstate change that is performed in smaller steps
16:23	ROX	LOCAL_CORE_PSTATE_STEP_TARGET: this field represents the intermediate value that is about to be established as the next Local Pstate Actual after completing one step in the process of the transition towards the 'local_Pstate_target' the new voltage, frequency, and clock resonance setting
24:31	ROX	LOCAL_ECO_PSTATE_STEP_TARGET: this field represents the intermediate value that is about to be established as the next Local Pstate Actual after completing one step in the process of the transition towards the 'local_Pstate_target' the new voltage, frequency, and clock resonance setting

Register Name	Read-Only Status Register For DPLL And For Debugging (PDSR)
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_DPLL_STATUS_REG
Address	00000000190F0161 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:14	ROX	DPLL_FF_FREQOUT: frequout output from DPLL (current frequency - bits 2 to 10 correspond to the same scale as the 9 bits of frequin (which need to be multiplied with our frequency step to get the real frequency), the remaining bits just provide a higher accuracy)
15	ROX	DPLL_FREQU_CHANGE: DPLL Frequency change (pin of DPLL without filter)
16	ROX	DPLL_STATUS_SPARE_BIT1: Spare bit.
17	ROX	PMAX_SYNC_PENDING: gets asserted, if the logic has a Pmax sync interrupt outstanding that will be eventually sent to PMC when the Pmax sync criterion is met
18	ROX	GA_ACK_PENDING: gets asserted, if the logic has a global actual Pstate update acknowledgment interrupt outstanding that will be eventually sent to PMC when the GA ack criterion is met
19:26	ROX	CAPPED_GLOBAL_PSTATE_REQ: corresponds to the capped global Pstate request that is presented as Pstate interrupt and send to PMC



Bits	PCB	Field Mnemonic: Description
27	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT2: DPLL runs at Fmax and CPM bit 2 is set. Note that this bit and the following 2 bits indicate, that the CPMs would allow the DPLL to run faster than Fmax.
28	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT3: DPLL runs at Fmax and CPM bit 3 is set
29	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT4: DPLL runs at Fmax and CPM bit 4 is set
30	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT2: DPLL runs at Fmin and CPM bit2 is zero. Note that this bit and the following 2 bits indicate, that the CPMs indicate, that the DPLL should run slower than the currently established Fmin.
31	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT1: DPLL runs at Fmin and CPM bit1 is zero
32	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT0: DPLL runs at Fmin and CPM bit0 is zero
33	ROX_CLRPAR T	DPLL_FASTER_THAN_FMAX_PLUS_DELTA1: The DPLL indicated that it ran once faster than Fmax+dppl_char_delta1
34	ROX_CLRPAR T	DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2: The DPLL indicated that it ran once slower than Fmin-dpll_char_delta2
35:48	ROX	DPLL_MAX_FREQOUT_AFTER_LAST_READ: This dial indicates the maximum DPLL frequout value after the last read of this register (only 14 MSBs)
49:62	ROX	DPLL_MIN_FREQOUT_AFTER_LAST_READ: This dial indicates the minimum DPLL frequout value after the last read of this register (only 14 MSBs)

Register Name	<i>The PIVRMVCR0 Controls The Voltage Stepping Delays</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG0
Address	00000000190F0162 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	IVRM_REQ_PSTATE_STEPDELAY_RISING: Requested Internal Pstate Baby Step Delay - Rising Step. Delay before allowing the next step for a rising Pstate Transition. This dial and ivrm_req_Pstate_stepdelay_lowering allow for differing delays for the two directional transitions if necessary. In 100ns units as established by scan dial ivrm_100ns_value
8:15	RW	IVRM_REQ_PSTATE_STEPDELAY_LOWERING: Requested Internal Pstate Baby Step Delay - Lowering Step. Delay before allowing the next step for a lower Pstate Transition. This dial and ivrm_req_Pstate_stepdelay_rising allow for differing delays for the two directional transitions if necessary. In 100ns units as established by scan dial ivrm_100ns_value

Register Name	<i>The PIVRMVCR1 Controls The Voltage Stepping Delays</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG1
Address	00000000190F0163 (PCB)
Attributes	
Description	

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Bits	PCB	Field Mnemonic: Description
0:7	RW	IVRM_STABILIZE_DELAY_RUN: Stabilization Delay - Run Time Delay to allow a rail to stabilize upon a baby step while the region is operational. In 100ns units as established by scan dial ivrm_100ns_value
8:15	RW	IVRM_STABILIZE_DELAY_IDLE: Stabilization Delay - Idle Transition Delay to allow a rail to stabilize upon a baby step during an idle transition where the activity in the region is quiesced. In 100ns units as established by scan dial ivrm_100ns_value
16:23	RW	IVRM_PFSTR_PROP_DELAY: PFET Strength Propagation Delay Time from PFET Strength values being launched till PFET Strength Valid is asserted. In order to ensure like rails across domains (Core VDD<>ECO VDD, Core VCS<>ECO VCS) are in sync during operational mode, this time value applies to all rails across the domains. This parameter allows for PFET Strength values to settle before PFET Strength Valid is sampled in the Uregs. The value set must the maximum delay for the worst rail timing and must allow for any metastability settling (for example, normally 2-3 cycles for single signals in an asynch handshake interface)
24:31	RW	IVRM_PFSTRVALID_PROP_DELAY: PFETStrength Valid Propagation Delay Time from ivrm_pfstr_prop_delay expiring to where PFET Strength Valid is deasserted. The value is the maximum of a) the minimum pulse width required for PFETStrength Valid and b) the propagation of PFETStrength Valid through (or enough of) the daisy chain. In order to ensure like rails across domains (Core VDD<>ECO VDD, Core VCS<>ECO VCS) are in sync during operational mode, this time value applies to all rails across the domains and thus must be the set to the value of the worst (slowest) rail. The minimum pulse width cannot be violated. The propagation delay can be tuned for more aggressive timing (for example, de-assert before the actual propagation is complete). Measured in prv_nclk cycles. The min delay is 2 cycles. Additional delay can be configured with the following settings 0x00 = No additional delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks
32:39	RW	IVRM_VPUMP_POWERON_TIME: iVRM (VRreg and UReg) - Vpump Power On Time Time necessary for the distributed internal VRM macro circuits to power on. Same delay is required for power on voltage pump circuit. Both delays are in the 8us range. In 100ns units as established by scan dial ivrm_100ns_value
40:47	RW	IVRM_BYPASS_DELAY: iVRM Bypass Propagation Delay Delay time for bypass_b signal propagation. Measured in prv_nclk cycles Target: 50ns 0x00 = No delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks
48:55	RW	PFET_VPUMP_ENABLE_DELAY: PFET and Vpump Enable Propagation Delay Delay time for PFET enable and vpump enable signal propagation. Target: 130ns Measured in prv_nclk cycles 0x00 = No delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks
56:62	RW	IVRM_VID_VOUT_THRESHOLD: VID threshold If the output voltage (Vout) is targeting a value below this threshold the slow PFET can backed off from its normal drive strength so as to reduce the ripple at these lower voltage conditions

Register Name	POHR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_OCC_HEARTBEAT_REG
Address	00000000190F0164 (PCB)
Attributes	
Description	Controls the behavior of the OCC heartbeat function.

Bits	PCB	Field Mnemonic: Description
0:7	RW	occ_heartbeat_time 'OCC Heartbeat Time Value' " 'This field defines the number of ~64us hang timer pulses in which a a PCB read or write of the heartbeat trigger register (of which the offset is specified by dial occ_heartbeat_reg_addr_offset) is not detected that will constitute the loss of the OCC heartbeat. If occ_heartbeat_en is set and upon this loss detection, POHBR[psafe] is forced and, if enabled, the error TBD is activated ' " '0x00 - unsupported, causes undefined behavior' '0x01 - 64us +0/-1us' '0x02 - 128us +0/-1us' '...' '0xFF - 16320us +0/-1us 16.3ms' " 'Upon the 64us hang pulse, the decremter ticks. if the decremter reaches x00, the heartbeat loss event is triggered.' " '
8	RW	occ_heartbeat_enable 'OCC Heartbeat Timer Enable' " '0 = Disable the OCC Heartbeat function. Lack of accesses to the register defined by the dial occ_heartbeat_reg_addr_offset does not result in heartbeat loss events to be triggered (no FIRs set nor Safe mode entry).' " '1 = Enable the OCC Heartbeat function. '
9:16	RW	occ_heartbeat_reg_addr_offset This dial allows to configure the address offset within the PCBS power management entity of the register, that will regularly reset the heartbeat timer (which is called heartbeat trigger register). The address offset is 0x100 plus the value of this dial.
17:24	RW	Psafe 'Pstate Safe' " 'This field establishes the Pstate that the core chiplet will take on if: 'psafe <= PMSR[global_actual_pstate] 'AND any of the following conditions are true:' 'Loss of OCC Heartbeat if occ_heartbeat_en is set' 'PMGP0[force_safe_mode] is set' " 'If psafe > PMSR[global_actual_pstate], the global_actual_pstate is forced.' " 'The value of Psafe needs to be at or below the nominal Pstate to make sure safe operation of all chiplets. '

Register Name	PRCCR0 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG 0
Address	00000000190F0165 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function.

Bits	PCB	Field Mnemonic: Description
0	ROX	RESCLK_DIS: Resonant Clock Enable Master enable of all resonant clocking functions. This dial can be set by setting GP3(22) and can not be set in this PCBS_resonant_Clock_Control_Reg0. 1 = Resonant Clock function is disabled. Default values (0) for resclk_value, resclk_core_sync_value, csb_eco_sync_value 0 = Resonant Clock Control hardware is enabled (the mode is defined by dial resclk_control_mode)

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Bits	PCB	Field Mnemonic: Description
1	RW	RESCLK_CONTROL_MODE: Resonant Clock Control Mode Defines the control means enabled when resclk_dis is not set. 0 = Pstate band hardware mechanism enabled 1 = Manual mode enabled (Firmware mode) If this bit is set to 0, the hardware control mechanism that manages the transition across the Resonant Bands is enabled. If this bit is set to 1, the automatic Pstate band hardware mechanism is disabled and the Firmware is in control of all values of the dial resclk_value, resclk_core_sync_value, csb_eco_sync_value. Firmware must ensure that frequency changes will not cross resonant bands or machine failures may result. resclk_value represents the values for clock sector buffer strength, inductor switch strength and high inductor enable. Firmware must ensure the correct stepping in/out the different bands and propagation of the values (resclk_value) to the core/eco (resclk_core_sync_value / csb_eco_sync_value).
2:4	RW	RESCLK_SYNC_PW: Resonant Clock Sync Pulse Width Number of nest/4 cycles to assert the clock sync signal. This value must be high enough to ensure capture and propagation across the asynchronous chiplet boundary.
5:11	RW	RES_SYNC_DELAY_CNT: Resonant Clock Sync Delay Number of nest/4 cycles wait after the launch of the resclk_value (csb and inductor) before launching the sync to allow these to be captured. This value must be high enough to ensure full propagation to the input of the clock sector buffers and inductor switches.
12:26	RW	RES_CSB_STR_INSTR_LO: Resonant Clock Sector Buffer Strength Instruction - Low Band Mask value that determines whether, during a fixed 15 step sequence, the res_csb_str(0:3) is to be decremented/incremented in entering/exiting the Low Band. During resonant clock Entry, res_csb_str(0:3) decremented by the value pattern from 0 down to 14. During resonant clock Exit, res_csb_str(0:3) incremented by the value pattern from 14 up to 0.
27:41	RW	RES_CSB_STR_INSTR_HI: Resonant Clock Sector Buffer Strength Instruction - High Band Mask value that determines whether, during a fixed 15 step sequence, the res_csb_str(0:3) is to be decremented/incremented in entering/exiting the High Band. During resonant clock Entry, res_csb_str(0:3) decremented by the value pattern from 0 down to 14. During resonant clock Exit, res_csb_str(0:3) incremented by the value pattern from 14 up to 0.

Register Name	PRCCR1 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG 1
Address	00000000190F0166 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function. Writes are conditioned.

Bits	PCB	Field Mnemonic: Description
0:7	RW	FULL_CSB_PS: Full Clock Sector Buffer Pstate Pstate defining the maximum point where the clock sector buffer must be driven to full strength. This allow clocks to be distributed at low Vmin levels. FW needs to make sure that no overlaps occur with bands 2 or 3.
8:15	RW	RES_LOW_LOWER_PS: Low Frequency Resonant Lower (LFRLow) Pstate Pstate defining the lower frequency of the Low Resonant Frequency Band. FW needs to make sure that no overlap occurs with band 0.
16:23	RW	RES_LOW_UPPER_PS: Low Frequency Resonant Upper (LFRUpper) Pstate Pstate defining the upper frequency of the Low Resonant Frequency Band. Note that if an overlap occurs with band 3, the hardware behavior is undefined.
24:31	RW	RES_HIGH_LOWER_PS: High Frequency Resonant Lower (HFRLow) Pstate Pstate defining the lower frequency of the High Resonant Frequency Band. Note that if an overlap occurs with band 2, the hardware behavior is undefined.

Bits	PCB	Field Mnemonic: Description
32:39	RW	RES_HIGH_UPPER_PS: High Frequency Resonant Upper (LFRUpper) Pstate Pstate defining the upper frequency of the High Resonant Frequency Band. This value needs to be greater or equal to high_res_lower_ps.
40:43	RW	NONRES_CSB_VALUE_TI: Clock Sector Buffer Table Index for non-resonant state Table Index into Clock Sector Buffer Table for the nominal, non-resonant state.
44:47	RW	FULL_CSB_VALUE_TI: Clock Sector Buffer Table Index for full CSB value Table Index into Clock Sector Buffer Table for the full CSB strength value.
48:56	RWX	RESCLK_VALUE: Output register driving the 9 bit resclk_value In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current resclk_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. The value in this register represents the following concatenation: csb_str_value(0:3) sw_str(0:3) hi_induct_en.
57	RWX	RESCLK_CORE_SYNC_VALUE: Output register driving the resclk_core_sync signal In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current resclk_core_sync_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. This bit is supposed to be used in order to create a SCOM-controlled pulse to force an update of the resclk propagation registers. A 1 enables the synchronous update, a 0 disables it. Suggested use of this bit is to set it to 1 and then set it back to 0 to create a (long) update pulse.
58	RWX	CSB_ECO_SYNC_VALUE: Output register driving the csb_eco_sync signal In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current csb_eco_sync_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. This bit is supposed to be used in order enable the ECO domain to participate in clock sector buffer strength changes, when switching from nominal strength to full CSB strength. A 1 enables the ECO domain, a 0 disables it from seeing a CSB strength update.

Register Name	PRCCR1 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_STATUS_REG
Address	00000000190F0167 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function.

Bits	PCB	Field Mnemonic: Description
0	ROX	RESCLK_STATE: Resonant Clock State 0 = Resonant Clocking inactive 1 = Resonant Clocking active Valid if resclk_inprogress = 0. Hardware sets this bit to the right value at the completion of the transition into and out of resonance mode.

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Bits	PCB	Field Mnemonic: Description
1	ROX	RES_HI_INDUCT_EN: Resonant High Inductor Enable Valid if resclk_inprogress = 0. This dial provides the current value being propagated. 0 = Resonant Clock mode not active 1 = Resonant Clock mode active
2	ROX	RESCLK_INPROGRESS: Resonant Clock Transition in Progress This bit is set by hardware while a transition is in progress and will be reset by hardware when the operation is complete.
3	ROX	RESCLK_FULL_CSB: Full CSB Clock State 0 = Full CSB Clocking inactive 1 = Full CSB Clocking active Valid if resclk_inprogress = 0. Hardware sets this bit to the right value at the completion of the transition into and out of full CSB mode respectively.

Register Name	<i>PLPFTCR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_CONTROL_REG
Address	00000000190F0168 (PCB)
Attributes	
Description	Allows firmware to configure the modes that are used for the PCBS Local Pstate Frequency Target Status Register.

Bits	PCB	Field Mnemonic: Description
0:2	RW	DELAY_TIME: This field encodes the delay between the time a Local Actual Pstate change modifies the input to the DPLL and the time frequency acquisition begins to allow the hardware to ignore the frequency transition of the DPLL in order to get better frequency measurements. This field encodes a delay of ~1us to ~128us in power of 2 selects. The delay is defined by $2^{\text{delay\_time}}$ in us. Note that the hardware uses multiples of the slow hang pulse that is running at 1us.
3	RW	RECORD_TRANSITIONS: This bit indicates whether the LPFTSR records events that correspond to Local Actual Pstate changes (and therefore may include DPLL slewing effects.) One usage model would set the periodic sample_time defined by the dial OHA_MODE_REG[tod_pulse_count_match_val] to a time less than the worst-case DPLL slew time but then ignore Pstate transitions because they might include DPLL slew effects.
4:18	RW	MULTIPLIER: This 15-bit unsigned constant is multiplied by the DPLL frequency code (9 bits) implied by the Local Actual Pstate to yield the 24-bit frequency target measured in PCBS-PM clock cycles (core clock / 2). Assuming times in seconds and frequencies in Hz, firmware should set this constant to: $(\text{DPLL\_Frequency\_Code\_Step\_Hz} * \text{Sample\_Time\_Seconds}) / 2$
19	RW	ENABLE_LPFT_FUNCTION: This is the enable bit to enable the local Pstate frequency target function. A '1' enables the function, a '0' disables it (the value can be changed at any time).

Register Name	<i>PLPFTSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_STATUS_REG
Address	00000000190F0169 (PCB)
Attributes	
Description	Allows firmware to observe local actual Pstate realized frequencies.

Bits	PCB	Field Mnemonic: Description
0	ROX_CLRPART	VALID: If this bit is set then all of the remaining fields of this register are valid. This bit is cleared whenever the register is read or after a local actual Pstate change occurs, and is will be set whenever the hardware completes a valid sample. If firmware reads this register and the valid bit is not set, then it indicates that the Local Pstate target frequency acquisition logic has not been able to complete a frequency acquisition for any Local Actual Pstate change since the last time the LPFTSR was read. This could be due to either of the following factors: 1. Firmware is sampling the LPFTSR faster than the time implied by the sample time defined in OHA by the dial OHA_MODE_REG[tod_pulse_count_match_val] field
1	ROX	CPM_DPLL: If the valid bit is set, then if cpm_dpll is set it indicates that the event recorded by this register was due to a Local Actual Pstate implemented by the DPLL running in CPM-DPLL mode, otherwise the value of this bit is undefined. If the valid bit is not set, this bit is undefined.
2	ROX	IVRM: If the valid bit is set, then if ivrm is set it indicates that the event recorded by this register was due to a Local Actual Pstate whose voltage was set locally by the iVRM operating entirely in regulation mode. If the valid bit is not set, this bit is undefined.
3	ROX	TRANSITION: If the valid bit is set, then if transition is set it indicates that during the observation period a Local Pstate Actual change has occurred, and any performance delta may be due to DPLL frequency slewing. If the valid bit is not set, this bit is undefined
4	ROX	STABLE: If stable is set it indicates that the DPLL input frequency has been stable since the last time the PLPFTSR was read. This bit is set whenever the PLPFTSR is read, and cleared whenever the Fmax input of the DPLL changes. This bit is always valid, regardless of the state of the valid bit. If the PLPFTSR is read on the same cycle a frequency changes then the stable bit is cleared. This bit helps firmware better understand how to interpret the information contained in the PLPFTSR. (Note that this bit should have an attribute ROX_SETPART, but this is not supported by regchk.)
5:28	ROX	DELTA: If the valid bit is set then this is the 24-bit signed difference Measured Cycles - Target Cycles for the event captured by this register. If the valid bit is not set, this dial is undefined.
29:52	ROX	CUMULATIVE: This field records the 24-bit cumulative (signed) delta for all valid samples taken since this field was cleared. Writing any value to this register clears this field. Note that it should have an attribute WOX_CLRPART, but this is not supported by regchk/figtree.
53:60	ROX	PSTATE: If the valid bit is set then this is the Local Actual Pstate of the frequency acquisition that had the minimum (signed) delta of any valid sample taken since the last time the LPFTSR was read. If the valid bit is not set, then this field is undefined.

Register Name	PFSMM1/2 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR1_REG
Address	00000000190F0170 (PCB)
Attributes	
Description	Facilitates debug by providing insight into the internal FSM states of the PCB-slave power-management unit. For expert use only. Coding according to VHDL design.

Bits	PCB	Field Mnemonic: Description
0:6	ROX	BABYSTEP_MAIN_FSM: Main Babystep FSM (mfsm_lt)
7:11	ROX	BABYSTEP_SLAVE_FSM: Babystep Slave FSM (sfsm_lt)
12:16	ROX	CORE_RAILSTEPPER_MAIN_FSM: Main Core Railstepper FSM (mrsfsm_lt)
17:21	ROX	ECO_RAILSTEPPER_MAIN_FSM: Main ECO Railstepper FSM (mrsfsm_lt)

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Bits	PCB	Field Mnemonic: Description
22:25	ROX	CORE_RAILSTEPPER_SUB_FSM: Core Railstepper Sub-FSM (srsfsm_lt)
26:29	ROX	ECO_RAILSTEPPER_SUB_FSM: ECO Railstepper Sub-FSM (srsfsm_lt)
30:34	ROX	CORE_RAILSTEPPER_BYP_FSM: Core Railstepper Bypass FSM (byp_fsm_lt)
35:39	ROX	ECO_RAILSTEPPER_BYP_FSM: ECO Railstepper Bypass FSM (byp_fsm_lt)
40:45	ROX	IVRM_CORE_VDD_SEQUENCER_FSM: Core iVRM Sequencer for Vdd (ivrm_fsm_lt)
46:51	ROX	IVRM_CORE_VCS_SEQUENCER_FSM: Core iVRM Sequencer for Vcs (ivrm_fsm_lt)
52:57	ROX	IVRM_ECO_VDD_SEQUENCER_FSM: ECO iVRM Sequencer for Vdd (ivrm_fsm_lt)
58:63	ROX	IVRM_ECO_VCS_SEQUENCER_FSM: ECO iVRM Sequencer for Vcs (ivrm_fsm_lt)

Register Name	<i>Refer To The Description Of PFSMM1.</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR2_REG
Address	00000000190F0171 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:6	ROX	RESCLK_BAND_FSM: Band Sequencer for resonant clocking (band_fsm_lt)
7:10	ROX	RESCLK_LOWRES_FSM: Low Resonant Clocking sequencer (lowres_fsm_lt)
11:14	ROX	RESCLK_HIGHRES_FSM: High Resonant Clocking sequencer (highres_fsm_lt)
15:18	ROX	RESCLK_FULLCSB_FSM: Full-CSB Resonant Clocking sequencer (fullcsb_fsm_lt)
19:22	ROX	RESCLK_UPDATE_FSM: Resonant Clocking Update sequencer (update_fsm_lt)
23:29	ROX	IDLE_TRANSITION_FSM: Idle State Sequence FSM (ifsm_lt)
30:37	ROX	Peco_step_target_uv Current ECO Step Target Pstate (different from Plocal_actual for undervolting)
38:45	ROX	Pcore_step_target_uv Current core Step Target Pstate (different from Plocal_actual for sleep and undervolting)

Register Name	<i>Protect Mode Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.PROTECT_MODE_REG
Address	00000000190F03FE (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	READ_PROTECT_ENABLE: Enable read protection
1	RW	WRITE_PROTECT_ENABLE: Enable write protection

Register Name	<i>Atomic Lock Register</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX09.TP_PCB_SLAVE_INST.ATOMIC_LOCK_REG	
Address	00000000190F03FF (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	RW	ATOMIC_LOCK_ENABLE: Enable atomic lock
1:4	ROX	ATOMIC_ID: Atomic ID

Register Name	<i>Contains The Slave's Primary Address</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.PRIMARY_ADDRESS_REG	
Address	000000001A0F0000 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RO	Reserved field (Access type is primary_address)

Register Name	<i>Multicast Group 1</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.MULTICAST_GROUP_1	
Address	000000001A0F0001 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST1_GROUP: multicast group1 setting

Register Name	<i>Multicast Group 2</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.MULTICAST_GROUP_2	
Address	000000001A0F0002 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST2_GROUP: multicast group2 setting

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Register Name	<i>Multicast Group 3</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.MULTICAST_GROUP_3
Address	000000001A0F0003 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST3_GROUP: multicast group3 setting

Register Name	<i>Multicast Group 4</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.MULTICAST_GROUP_4
Address	000000001A0F0004 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST4_GROUP: multicast group4 setting

Register Name	<i>Timeout Select Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.TIMEOUT_REG
Address	000000001A0F0010 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	Reserved field (Access type is int_timeout)

Register Name	<i>Assist Interrupt Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.ASSIST_INTERRUPT_REG
Address	000000001A0F0011 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is attn)
1	ROX	Reserved field (Access type is recov)
2	ROX	Reserved field (Access type is xstop)



Register Name	GP3 Register (NA In PERV CPLT)
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.GP3_REG
Address	000000001A0F0012 (PCB) 000000001A0F0013 (PCB1) 000000001A0F0014 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset
2	RWX	RWX_WAND	RWX_WOR	GLSMUX_RESET: Glsmux reset for test purpose and stuck active mesh protection. Notice no clocks in the EX if this bit is set.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Put the DPLL in test mode.
4	RWX	RWX_WAND	RWX_WOR	PLL_RST: Put PLL in reset state.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYP: Enable PLL bypass.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pcb_access)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	PM_PI_DECODE: Test override for power management. EX chiplet only.
22	RWX	RWX_WAND	RWX_WOR	RESCLK_DIS: Resonant clocking disable.
23:25	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave will report 'Chiplet Offline'.
27	RWX	RWX_WAND	RWX_WOR	TP_LVLTRANS_FENCE: Electrical winkel fence. Mainly used by power management.
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.
29:31	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)

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Register Name	<i>Skew Adjust Data</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.CLK_ADJ_REG
Address	000000001A0F0015 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:15	ROX	

Register Name	<i>Clk Ajust Config</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.CLK_ADJ_SET
Address	000000001A0F0016 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:31	RW	CLK_ADJ_SET_REG: Clk adj config

Register Name	<i>Vital Scan Out</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.VITAL_SCAN_OUT
Address	000000001A0F0017 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	

Register Name	<i>Chiplet Heartbeat Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.HEARTBEAT_REG
Address	000000001A0F0018 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	HEARTBEAT_DEAD: Chiplet heartbeat not detected



Register Name	<i>Lock Indications From PLLs</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.PLL_LOCK_REG	
Address	000000001A0F0019 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:3	ROX	Reserved field (Access type is lock)

Register Name	<i>Attn Interrupt</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.ATTN_INTERRUPT_REG	
Address	000000001A0F001A (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is attn)

Register Name	<i>Recov Interrupt</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.RECOV_INTERRUPT_REG	
Address	000000001A0F001B (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is recov)

Register Name	<i>Xstop Interrupt</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.XSTOP_INTERRUPT_REG	
Address	000000001A0F001C (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is xstop)

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Register Name	<i>Slave Config Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.SLAVE_CONFIG_REG
Address	000000001A0F001E (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	CFG_DISABLE_PERV_THOLD_CHECK: Disable pervasive thold check
1	RW	CFG_DISABLE_MALF_PULSE_GEN: Disable pulse generation for malf alert. Switch back to level
2	RW	CFG_STOP_HANG_CNT_SYS_XSTP: Disable hang counter stop for system xstop
3	RW	CFG_DISABLE_CL_ATOMIC_LOCK: Disable atomic lock for chiplet accesses
4	RW	CFG_DISABLE_HEARTBEAT: Disable check for voltage and gridclock in the chiplet
5	RW	CFG_ZERO_DATA: Sent zero data on any error
6:7	RW	
8:12	RW	ERROR_MASK: mask bits for slave error reporting
13:15	RW	

Register Name	<i>Error Capture Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.ERROR_REG
Address	000000001A0F001F (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX_WCLEA R	CE_ERROR: Correctable error on pcb bus
1:3	RWX_WCLEA R	CHIPLET_ERRORS: Errors reported by chiplet 000 = no error 001 = XSCOM command blocked due pending errors 010 chiplet offline 011 partial good 100 invalid address / address error / bad access type 101 clock error 110 parity error / received unexpected packet / wrong packet number 111 timeout This register is for debug purposes only. It only holds meaningful data if it is cleared after each error.
4	RWX_WCLEA R	PARITY_ERROR: Parity error on PCB Interface
5	RWX_WCLEA R	DATA_BUFFER_ERROR: Parity error in data buffer
6	RWX_WCLEA R	ADDR_BUFFER_ERROR: Parity error in address buffer
7	RWX_WCLEA R	PCB_FSM_ERROR: Invalid state error in PCB FSM
8	RWX_WCLEA R	CL_FSM_ERROR: Invalid state error in Chiplet FSM
9	RWX_WCLEA R	INT_RX_FSM_ERROR: Invalid state error in interrupt RX FSM
10	RWX_WCLEA R	INT_TX_FSM_ERROR: Invalid state error in interrupt TX FSM



Bits	PCB	Field Mnemonic: Description
11	RWX_WCLEAR	INT_TYPE_ERROR: Invalid interrupt type
12	RWX_WCLEAR	CL_DATA_ERROR: Parity error on Chiplet Interface
13	RWX_WCLEAR	INFO_ERROR: Parity error on Chiplet info lines
14	RWX_WCLEAR	UNUSED_0:
15	RWX_WCLEAR	CHIPLET_ATOMIC_LOCK_ERROR: Chiplet atomic lock error
16	RWX_WCLEAR	PCB_INTERFACE_ERROR: Error of pcb interface component for the internal endpoint
17	RWX_WCLEAR	CHIPLET_OFFLINE: Heartbeat check indicated that chiplet is offline
18	RWX_WCLEAR	CHIPLET_GRID_SKITTER: Heartbeat check indicated skitter on the chiplet grid
19	RWX_WCLEAR	GP3_REG_PARITY_ERROR: gp3 register parity bad
20	RWX_WCLEAR	ADDRESS_REG_PARITY_ERROR: address register parity bad
21	RWX_WCLEAR	TIMEOUT_REG_PARITY_ERROR: timeout select register parity bad
22	RWX_WCLEAR	CONFIG_REG_PARITY_ERROR: slave config register parity bad
23	RWX_WCLEAR	CLK_ADJ_REG_PARITY_ERROR: clk adj register parity bad
24	RWX_WCLEAR	DIV_REG_PARITY_ERROR: div register parity bad
25:28	RWX_WCLEAR	PLL_UNLOCK_ERROR: unlock from chiplet pll

Register Name	<i>Hang Pulse Generation Register 0.</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.HANG_PULSE_0_REG
Address	000000001A0F0020 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_0: Value of hang pulse 0. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_0: If set to '1', hang pulses are suppressed in case of a xstop

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Register Name	<i>Hang Pulse Generation Register 1.</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.HANG_PULSE_1_REG
Address	000000001A0F0021 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_1: Value of hang pulse 1. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_1: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 2.</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.HANG_PULSE_2_REG
Address	000000001A0F0022 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_2: Value of hang pulse 2. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_2: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 3.</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.HANG_PULSE_3_REG
Address	000000001A0F0023 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_3: Value of hang pulse 3. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_3: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 4</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.HANG_PULSE_4_REG
Address	000000001A0F0024 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_4: Value of hang pulse 4. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_4: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 5</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.HANG_PULSE_5_REG
Address	000000001A0F0025 (PCB)
Attributes	
Description	This hang counter is used exclusively to generate the malfunction alert pulse.

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_5: Value of hang pulse 5. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_5: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 6</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.HANG_PULSE_6_REG
Address	000000001A0F0026 (PCB)
Attributes	
Description	This hang counter is exclusively used for heartbeat generation.

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_6: Value of hang pulse 6. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_6: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Divider For Hang Counter Clock</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.PRE_COUNTER_REG
Address	000000001A0F0028 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PRE_COUNTER: Divider for hang counter clock. Divides clock by n+1 (default: n=0)

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Register Name		PowerManagement GP0		
Mnemonic		EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PMGP0_REG		
Address		000000001A0F0100 (PCB) 000000001A0F0101 (PCB1) 000000001A0F0102 (PCB2)		
Attributes				
Description				
Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PM_DISABLE: Master Switch for the PowerManagement Macro
1	RWX	WOX_AND	WOX_OR	PMGP0_SPARE_BIT1: spare bit
2	RWX	WOX_AND	WOX_OR	TP_TC_RESTART_CORE_DOMAIN: Kicks off small sequencer in OHA to get chiplet clocks back running for fast sleep without involving PORE. From GP-reg and overridden by PowMan State Machine.
3	RWX	WOX_AND	WOX_OR	DPLL_THOLD: Thold for the DPLL clock domain in the chiplet
4	RWX	WOX_AND	WOX_OR	PERV_THOLD: Thold for the Pervasive clock domain in the chiplet
5	RO	RO	RO	Reserved.
6	RO	RO	RO	Reserved.
7	RWX	WOX_AND	WOX_OR	PM_DPLL_TIMER_ENA: Select a timer instead of the DPLL lock bit for criteria to switch to DPLL. The time is defined by thold_timer_sel.
8	RWX	WOX_AND	WOX_OR	DPLL_LOCK_SENSE: DPLL lock sensitivity control (0=faster lock time, 1=slower lock time)
9	RWX	WOX_AND	WOX_OR	PMGP0_SPARE2: spare bit
10	RWX	WOX_AND	WOX_OR	DPLL_RESET: Reset to DPLL
11	RWX	WOX_AND	WOX_OR	PMGP0_SPARE_BIT11: Spare bit
12:19	RWX	WOX_AND	WOX_OR	DPLL_TESTOUT_CTL: DPLL testout control
20	RWX	WOX_AND	WOX_OR	TP_TC_CACHE2CORE_FENCE: Fence from cache to core domain in EX chiplet
21	RWX	WOX_AND	WOX_OR	TP_TC_CORE2CACHE_FENCE: Fence from core to cache domain in EX chiplet
22	RWX	WOX_AND	WOX_OR	TP_TC_PERVASIVE_ECO_FENCE: Pervasive ECO fence
23	RWX	WOX_AND	WOX_OR	CHKSW_HW257424_DISABLE: Chicken switch for interrupt retry exhausted bug (0=fix enabled, 1=fix disabled)
24:26	RWX	WOX_AND	WOX_OR	TP_CLK_ASYNC_RESET_DC: Clk async reset for three glitchless muxes, and the two clock dividers (bit 0 = master GLM, bit 1 = ECO Div2 and ECO GLM, bit 2= core Div1 and core GLM)
27:29	RWX	WOX_AND	WOX_OR	TP_CLKGLM_SEL_DC: Glitchless Mux Select for primary chiplet clock source (feeding both core and eco clock muxes) 000 = refclk, 001 = DPLL. 100 = Use constant selected by bit 34, else refclk
30	RWX	WOX_AND	WOX_OR	TP_CLKGLM_ECO_SEL_DC: Glitchless Mux Select for eco domain (cache_nclk) grid. 0= follow primary source chosen by previous field: 1 = Use constant selected by bit 34
31	ROX	NC	NC	SPECIAL_WKUP_DONE: Indicates that special wakeup is done, if asserted
32:33	RWX	WOX_AND	WOX_OR	TP_CLKGLM_CORE_SEL_DC: Glitchless Mux Select for core domain (nclk grid) mux. 0b00=primary GLS mux output, 0b10=constant input, 0b01=refclk. Valid transitions are 0b01 <-> 0b00 <-> 0b10, 0b11 is illegal



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
34	RWX	WOX_AND	WOX_OR	TP_CLKGLM_CONST_DC: Constant input available to all three ClkGlm
35:36	RWX	WOX_AND	WOX_OR	THOLD_TIMER_SEL: Selection for the thold transition timer in the IDLE state machine. 0b00=1024 cycles delay, 0b01=512 cycles delay, 0b10=256 cycles delay, 0b11= 128 cycles delay
37	RWX	WOX_AND	WOX_OR	BLOCK_ALL_WAKEUP_SOURCES: Setting this bit will make the PM Slave ignore any Wakeup events (ext. interrupt, malfunction alert, any special wakeup bit). This bit is intended to enable firmware concurrent patch capability. Note: This does NOT block the interrupt from being presented to the processor core. The following procedure is required on changes: 1. Firmware may only set this bit after first setting special wakeup and polling for special wakeup complete (OHA and PCB-slave both in running state with AISS and PM FSMs idle). 2. Firmware may only clear this bit if all special wakeup bits are first cleared.
38	RWX	WOX_AND	WOX_OR	TP_TC_DPLL_TESTMODE_DC: ADPLL test mode
39	RWX	WOX_AND	WOX_OR	PM_SLV_WINKLE_FENCE: Fence off the powered off chiplet in winkle. - Logical fence/hold for pcb_slave and pcb_slave_pm. For electrical fence see bit 23.
40	RWX	WOX_AND	WOX_OR	L3_ENABLE_SWITCH: Setting this bit activates l3_edram_enable if allowed by system configuration GP3(28). Resetting this bit deactivates l3_edram_enable.
41	RWX	WOX_AND	WOX_OR	TP_CPLT_IVRM_REFBYPASS_DC: Signal to iVRM (used to be controlled by scan-only block inside EX, but needs to be driven by VIO domain)
42	RWX	WOX_AND	WOX_OR	CHKSW_HW241939_DISABLE: if this bit is set to 1, the fix for HW241939 (pfet enable SCOM-ability) is disabled
43	RWX	WOX_AND	WOX_OR	CHKSW_HW273115_DISABLE: if this bit is set to 1, the fix for HW273115 (Pga ACK noack issue when the babystepper is in the winkle state) is disabled
44	RWX	WOX_AND	WOX_OR	CHKSW_HW245103_DISABLE: if this bit is set to 1, the fix for HW245103 resonant clocking CSB and SW -bit ordering change is disabled
45	RWX	WOX_AND	WOX_OR	CHKSW_HW257534_DISABLE: if this bit is set to 1, the fix for HW257534 (fencing of errors) is disabled
46	RWX	WOX_AND	WOX_OR	CHKSW_HW259509_ENABLE: if this bit is set to 0, the fix for HW259509 (Pstate change hanging, because of DPLL flock timer in a hung state) is disabled
47	RWX	WOX_AND	WOX_OR	CHKSW_HW260345_DISABLE: if set to 1, this bit disables the HW260345 fix (fix was to make sure that we enter bypass mode for iVRM safe mode without a glitch that could cause Vcs in regulation and Vdd in bypass)
48:49	ROX	NC	NC	WAKEUP_INT_TYPE: (Known to be unreliable and not supported, informational usage only) Type of the last wakeup event that caused an exit from sleep or winkle (excluding nap!), regardless of present state. 0b01: External interrupt. 0b10: Malfunction Alert. 0b11: Special Wakeup. 0b00: chiplet has never fully entered and exited a chiplet-level idle state since IPL of the system. (Note this does not necessarily get updated when the processor core enters an idle state, only if the PCB-Slave enters and then exits the idle state for this chiplet).
50	ROX	NC	NC	DPLL_LOCK: DPLL lock indicator
51	ROX	NC	NC	SPECIAL_WKUP_ALL_SOURCES_ORED: logical OR of all special wakeup sources
52	ROX	NC	NC	REGULAR_WKUP_AVAILABLE: logical OR of external interrupt and malfunction alert

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
53	RWX	WOX_AND	WOX_OR	BLOCK_REG_WKUP_SOURCES: blocks ext. int. and malf. Alert from waking up PCBS (no block possible for PC!)

Register Name	<i>PowerManagement GP1</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PMGP1_REG
Address	000000001A0F0103 (PCB) 000000001A0F0104 (PCB1) 000000001A0F0105 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	SLEEP_POWER_DOWN_EN: Sleep Power Down Enable: When set to 1, causes hardware to automatically reduce voltage to the Core domain when entering Sleep mode. The voltage value for power down is chosen by sleep_power_off_sel (bit 2). When set to 0, a request is sent to the PORE engine for assistance entering Sleep.
1	RWX	WOX_AND	WOX_OR	SLEEP_POWER_UP_EN: Sleep Power Up Enable: When set to 1, enables automated hardware restoration of voltage via PFETs and, if enabled, iVRMs when exiting Sleep mode. If this bit is set to 0 the hardware rely on external means (PORE or equivalent) to restore voltage.
2	RWX	WOX_AND	WOX_OR	SLEEP_POWER_OFF_SEL: Sleep Power Off Select: Selects which voltage level to place the Core domain PFETs upon Sleep entry. 0 = Vret (Fast Sleep Mode), 1 = Voff (Deep Sleep Mode). Depending on the setting of pmicr_latency_en, this bit is controlled with a PCB-write (0) or by the PMICR in the core (1).
3	RWX	WOX_AND	WOX_OR	WINKLE_POWER_DOWN_EN: Winkle Power Down Enable: When set to 1, causes hardware to automatically reduce voltage to the entire Chiplet (both Core and ECO Domains) when entering Winkle mode. The voltage value for power down is chosen by winkle_power_off_sel (bit 5). When set to 0, a request is sent to the PORE engine for assistance entering Winkle.
4	RWX	WOX_AND	WOX_OR	WINKLE_POWER_UP_EN: Winkle Power Up Enable: When set to 1, enables automated hardware PFET enablement when exiting Winkle mode. If this bit is set to 0 the hardware rely on external means (PORE or equivalent) to cause the PFETs to be re-enabled.
5	RWX	WOX_AND	WOX_OR	WINKLE_POWER_OFF_SEL: Winkle Power Off Select: Selects which voltage level to place the Core and ECO domain PFETs upon Winkle entry. 0 = Vret (Fast Winkle Mode), 1 = Voff (Deep Winkle Mode). Depending on the setting of pmicr_latency_en, this bit is controlled with a PCB-write (0) or by the PMICR in the core (1).
6	RWX	WOX_AND	WOX_OR	OHA_WKUP_OVERRIDE_EN: Needs to be 0 for normal operation. If set to 1, the two following dials are used to override the regular and special wakeup signal from PCBS to OHA
7	RWX	WOX_AND	WOX_OR	OHA_PM_WKUP_OVERRIDE: Enablement by 'oha_wkup_override_en' forces the regular wakeup signal to OHA to the value of this bit regardless of presence of an interrupt source.
8	RWX	WOX_AND	WOX_OR	OHA_SPC_WKUP_OVERRIDE: Enablement by 'oha_wkup_override_en' forces the special wakeup signal to OHA to the value of this bit, regardless of the firmware settings.

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
9	RWX	WOX_AND	WOX_OR	ENDP_RESET_PM_ONLY: If asserted, an endpoint reset of all power management-related functions (not the regular PCB slave) is performed. Intended usage is for recovery.
10	RWX	WOX_AND	WOX_OR	DPLL_FREQ_OVERRIDE_ENABLE: override Fmax/Fmin only, if '1', using register FREQ_CTRL_REG
11	RWX	WOX_AND	WOX_OR	PM_SPR_OVERRIDE_EN: PM SPR Override Enable The PPMCR (0xNNNN) and PPMICR (0XXXXX) accesses the register resources that make up the PMCR SPR used by hypervisor to management Pstates. Thus, PCB updates to it are disabled in hardware to prevent collisions. This bit allows ownership of the PMCR to be switched from hypervisor to OCC. This switch is immediate in hardware, thus, firmware must ensure the ownership switch is otherwise communicated. 0 = Disables the writing of the PPMCR (0xNNNN) from the PCB and allows SPR 884 writes (mtspr) to update the register resource. 1 = Enables the writing of the PPMCR (0xNNNN) from the PCB.
12	RWX	WOX_AND	WOX_OR	FORCE_SAFE_MODE: Force Safe Mode 0 = Allow other enabled features to determine the operational Pstate. 1 = Forces the minimum of POHBR[psafe] and PPMSR[global_pstate_actual] Pstate for the core chiplet as the operational frequency.
13	RWX	WOX_AND	WOX_OR	IVRM_SAFE_MODE_EN: Internal VRM Safe Mode Enable 0 = Disable the iVRM safe mode, thus, no automatic actions occur, if an iVRM error happens. 1 = if the iVRMs are enabled (PIVRMCSR[ivm_en] is set) and Pstates are enabled and if the error defined by dial pcbs_ivrm_gross_or_fine_err occurs, then the railstepper is forced into bypass mode to prevent a voltage-frequency hazard
14	RWX	WOX_AND	WOX_OR	IVRM_SAFE_MODE_FORCE_ACTIVE: Internal VRM Safe Mode Force Dial 0 = the hardware decides whether to activate the iVRM safe mode or not 1 = the iVRM safe mode is forced regardless (this makes only sense if ivrm_fsm_enable=1 and Pstates are enabled)
15	RWX	WOX_AND	WOX_OR	PMICR_LATENCY_EN: Selects how the sleep/winkle latency (which is deep/fast) is controlled. If asserted the PMICR controls the winkle/sleep_power_off_sel in PMGP1, otherwise those bits are controlled via SCOM by OCC.
16	RWX	WOX_AND	WOX_OR	ENABLE_OCC_CTRL_FOR_LOCAL_PSTATE_EFF_REQ: controls, if the HW (for value 0) or OCC (value 1) is in control of the Local Pstate Effective register in PPSTR
17	RWX	WOX_AND	WOX_OR	SERIALIZE_PFET_POWERDOWN: if asserted, the pFET sequencer will sequence the core and the ECO domain one after the other when powering down
18	RWX	WOX_AND	WOX_OR	SERIALIZE_PFET_POWERUP: if asserted, the pFET sequencer will sequence the ECO and the core domain one after the other when powering up
19	RWX	WOX_AND	WOX_OR	DISABLE_FORCE_DEEP_TO_FAST_SLEEP: 0: (normal operation) - If PCB Slave reports a recoverable error or a checkstop, a DEEP sleep operation is forced to FAST. The entries in sleep/winkle_power_off_sel remain unchanged. 1: force to FAST is disabled.

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
20	RWX	WOX_AND	WOX_OR	DISABLE_FORCE_DEEP_TO_FAST_WINKLE: 0: (normal operation) - If PCB Slave reports a recoverable error or a checkstop, a DEEP winkle operation is forced to FAST. The entries in sleep/winkle_power_off_sel remain unchanged. 1: force to FAST is disabled.

Register Name	<i>PFET Control/Status Register For Core And ECO Vdd</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PFVDDCNTLSTAT_REG
Address	000000001A0F0106 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	CORE_VDD_PFET_FORCE_STATE: Core Domain PFET Force State Provides a means for firmware to force the core domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 4:5 = 00 (both core_vdd_pfet_val_override AND core_vdd_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
2:3	RW	ECO_VDD_PFET_FORCE_STATE: ECO Domain PFET Force State Provides a means for firmware to force the ECO domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 6:7 = 00 (both eco_vdd_pfet_val_override AND eco_vdd_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
4	RW	CORE_VDD_PFET_VAL_OVERRIDE: Core Domain PFET Value Override 0 = Override is disabled
5	RW	CORE_VDD_PFET_SEL_OVERRIDE: Core Domain PFET Stage Select Override 0 = Override is disabled
6	RW	ECO_VDD_PFET_VAL_OVERRIDE: ECO Domain PFET Value Override 0 = Override is disabled
7	RW	ECO_VDD_PFET_SEL_OVERRIDE: ECO Domain PFET Stage Select Override 0 = Override is disabled
8	RW	CORE_VDD_PFET_ENABLE_REGULATION_FINGER: Core Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the core_vdd_pfet_enable_value.
9	RW	ECO_VDD_PFET_ENABLE_REGULATION_FINGER: ECO Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the eco_vdd_pfet_enable_value.



Bits	PCB	Field Mnemonic: Description
10:21	RW	CORE_VDD_PFET_ENABLE_VALUE: Core PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the Core Domain PFET Enables directly. If core_vdd_pfet_val_override = 1, a write to this field sets the state of the core PFET Enables until core_vdd_pfet_val_override is cleared. If core_vdd_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the core_vdd_pfet_valN_slav registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
22:25	RW	CORE_VDD_PFET_SEL_VALUE: Core PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure core_vdd_pfet_valN_slav(0:11) where N is 0 to 11 if core_vdd_pfet_sel_override = 1. If core_vdd_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
26:37	RW	ECO_VDD_PFET_ENABLE_VALUE: ECO PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the ECO PFET Enables directly. If ECO_vdd_pfet_val_override = 1, a write to this field sets the state of the ECO PFET Enables until ECO_vdd_pfet_val_override is cleared. If eco_vdd_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the eco_vdd_pfet_valN_slav registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
38:41	RW	ECO_VDD_PFET_SEL_VALUE: ECO PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure eco_vdd_pfet_valN_slav(0:11) where N is 0 to 11 if eco_vdd_pfet_sel_override = 1. If eco_vdd_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
42:45	ROX	CORE_VDD_PG_STATE: Core power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
46:49	ROX	CORE_VDD_PG_SEL: For debug, contains the actual index n into Core Domain PFET Value [n] SLAT Register set that contains the Core PFET Enable Value currently enabled.
50:53	ROX	ECO_VDD_PG_STATE: ECO Domain power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
54:57	ROX	ECO_VDD_PG_SEL: For debug, contains the actual index n into ECO Domain PFET Value [n] SLAT Register set that contains the ECO PFET Enable Value currently enabled.

Register Name	PFET Sense Register	
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PFSENSE_REG	
Address	000000001A0F0107 (PCB)	
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:11	ROX	TP_CORE_VDD_PFET_ENABLE_SENSE: Not used any more.
12:23	ROX	TP_ECO_VDD_PFET_ENABLE_SENSE: Not used any more.



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Bits	PCB	Field Mnemonic: Description
24:35	ROX	TP_CORE_VCS_PFET_ENABLE_SENSE: Not used any more.
36:47	ROX	TP_ECO_VCS_PFET_ENABLE_SENSE: Not used any more.

Register Name	<i>PM Error Summary Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PMERRSUM_REG
Address	000000001A0F0108 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	PM_ERROR: PM Error is present. Intended for use by special PCB multicast to see error state of all chiplets with a single read (via 510F0108 to read all chiplets)

Register Name	<i>PM Error Register:</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PMERR_REG
Address	000000001A0F0109 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_HANG_ERR: Hang during Unassisted Sleep Entry: SLEEP_ENTRY_NOTIFY_PMC state
1	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ASSIST_HANG_ERR: Hang during Assisted Sleep Entry: SLEEP_ENTRY_NOTIFY_PMC_ASSIST state
2	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ERR: Hang during Unassisted Sleep Exit: SLEEP_EXIT_NOTIFY_PMC state
3	ROX	PCBS_SLEEP_EXIT_INVOKE_PORE_ERR: Hang during Assisted Deep Sleep Exit: SLEEP_EXIT_INVOKE_PORE state
4	ROX	PCBS_WINKLE_ENTRY_NOTIFY_PMC_ERR: Hang during Unassisted Winkle Entry: WINKLE_ENTRY_NOTIFY_PMC state
5	ROX	PCBS_WINKLE_ENTRY_SEND_INT_ASSIST_ERR: Hang during Assisted Winkle Entry: WINKLE_ENTRY_SEND_INT_ASSIST state
6	ROX	PCBS_WINKLE_EXIT_NOTIFY_PMC_ERR: Hang during Unassisted Winkle Exit: WINKLE_EXIT_NOTIFY_PMC state
7	ROX	PCBS_WAIT_DPLL_LOCK_ERR: Hang during Unassisted Exit waiting on DPLL: WAIT_DPLL_LOCK state
8	ROX	PCBS_SPARE8_ERR: spare bit, always 0
9	ROX	PCBS_WINKLE_EXIT_SEND_INT_ASSIST_ERR: Hang during Assisted Winkle Exit: WINKLE_EXIT_SEND_INT_ASSIST state
10	ROX	PCBS_WINKLE_EXIT_SEND_INT_POWUP_ASSIST_ERR: Hang during Assisted Winkle Exit: WINKLE_EXIT_SEND_INT_POWUP_ASSIST state
11	ROX	PCBS_WRITE_FSM_GOTO_REG_IN_INVALID_STATE_ERR: write to FSM goto register in invalid state
12	ROX	PCBS_WRITE_PMGP0_IN_INVALID_STATE_ERR: write to PMGP0 in invalid state

Bits	PCB	Field Mnemonic: Description
13	ROX	PCBS_FREQ_OVERFLOW_IN_PSTATE_MODE_ERR: frequency of DPLL in Pstate mode overflows (Fnom + desired Pstate > 511)
14	ROX	PCBS_ECO_RS_BYPASS_CONFUSION_ERR: ECO railstepper tried to exit Vcs bypass and enter Vdd bypass in one Pstate step (it is not clear, in which order this strange operation should be performed - most likely it should never happen to avoid that Vcs is greater than Vdd)
15	ROX	PCBS_CORE_RS_BYPASS_CONFUSION_ERR: same as previous error, but for core railstepper (it is not clear, in which order this strange operation should be performed - most likely it should never happen to avoid that Vcs is greater than Vdd)
16	ROX	PCBS_READ_LPST_IN_PSTATE_MODE_ERR: read LPST-array while iVRM FSMs are enabled (dial ivrm_fsm_enable asserted)
17	ROX	PCBS_LPST_READ_CORR_ERR: correctable error occurred when reading the LPST
18	ROX	PCBS_LPST_READ_UNCORR_ERR: uncorrectable error occurred when reading the LPST
19	ROX	PCBS_PFET_STRENGTH_OVERFLOW_ERR: overflow occurred when calculating the pFET strength (in final rounding step!)
20	ROX	PCBS_VDS_LOOKUP_ERR: Vds entry not found in lookup table (when performing the linear search!)
21	ROX	PCBS_IDLE_INTERRUPT_TIMEOUT_ERR: idle interrupt timeout in PCB interrupt controller
22	ROX	PCBS_PSTATE_INTERRUPT_TIMEOUT_ERR: PState interrupt timeout in PCB interrupt controller
23	ROX	PCBS_GLOBAL_ACTUAL_SYNC_INTERRUPT_TIMEOUT_ERR: GlobalActualSync Interrupt timeout in PCB interrupt controller
24	ROX	PCBS_PMAX_SYNC_INTERRUPT_TIMEOUT_ERR: PmaxSync Interrupt timeout in PCB interrupt controller
25	ROX	PCBS_GLOBAL_ACTUAL_PSTATE_PROTOCOL_ERR: a write to global actual Pstate register has occurred before the global actual Pstate interrupt has left PCBS
26	ROX	PCBS_PMAX_PROTOCOL_ERR: a write to the Pmax/Pmin register has occurred before the Pmax sync interrupt has left PCB
27	ROX	PCBS_IVRM_GROSS_OR_FINE_ERR: iVRM gross or fine error (details to be found in PCBS_ivrm_Control_Status_Reg)
28	ROX	PCBS_IVRM_RANGE_ERR: iVRM range error (summary bit, details to be found in PCBS_ivrm_Control_Status_Reg)
29	ROX	PCBS_DPLL_CPM_FMIN_ERR: DPLL CPM Fmin error
30	ROX	PCBS_DPLL_DCO_FULL_ERR: DPLL DCO full
31	ROX	PCBS_DPLL_DCO_EMPTY_ERR: DPLL DCO empty
32	ROX	PCBS_DPLL_INT_ERR: DPLL internal error
33	ROX	PCBS_FMIN_AND_NOT_CPMBIT_ERR: dpll_fmin_and_not_cpmbit (ref. to dial cpm_fmin_clip_error_sel on how to configure this)
34	ROX	PCBS_DPLL_FASTER_THAN_FMAX_PLUS_DELTA1_ERR: dpll_faster_than_fmax_plus_delta1 (for characterization, delta1 is configurable with pll_char_delta1)
35	ROX	PCBS_DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2_ERR: dpll_slower_than_fmin_minus_delta2 (for characterization, delta2 is configurable with pll_char_delta2)
36	ROX	PCBS_RESCLK_CSB_INSTR_VECTOR_CHG_IN_INVALID_STATE_ERR: RESCLK CSB instruction vector change while FSMs none idle
37	ROX	PCBS_RESCLK_BAND_BOUNDARY_CHG_IN_INVALID_STATE_ERR: RESCLK Band boundaries change while FSMs none idle
38	ROX	PCBS_OCC_HEARTBEAT_LOSS_ERR: OCC heartbeat loss
39	ROX	PCBS_SPARE39_ERR: spare bit, always 0
40	ROX	PCBS_SPARE40_ERR: spare bit, always 0



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Bits	PCB	Field Mnemonic: Description
41	ROX	PCBS_SPARE41_ERR: spare bit, always 0
42	ROX	PCBS_SPARE42_ERR: spare bit, always 0

Register Name	<i>PM Error Mask Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PMERRMASK_REG
Address	000000001A0F010A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_HANG_ERR_MASK: Mask for this error: 1=masked, 0=not masked
1	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ASSIST_HANG_ERR_MASK: Mask for this error: 1=masked, 0=not masked
2	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
3	RW	PCBS_SLEEP_EXIT_INVOKE_PORE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
4	RW	PCBS_WINKLE_ENTRY_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
5	RW	PCBS_WINKLE_ENTRY_SEND_INT_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
6	RW	PCBS_WINKLE_EXIT_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
7	RW	PCBS_WAIT_DPLL_LOCK_ERR_MASK: Mask for this error: 1=masked, 0=not masked
8	RW	PCBS_SPARE8_ERR_MASK: Mask for this error: 1=masked, 0=not masked
9	RW	PCBS_WINKLE_EXIT_SEND_INT_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
10	RW	PCBS_WINKLE_EXIT_SEND_INT_POWUP_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
11	RW	PCBS_WRITE_FSM_GOTO_REG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
12	RW	PCBS_WRITE_PMGPO_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
13	RW	PCBS_FREQ_OVERFLOW_IN_PSTATE_MODE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
14	RW	PCBS_ECO_RS_BYPASS_CONFUSION_ERR_MASK: Mask for this error: 1=masked, 0=not masked
15	RW	PCBS_CORE_RS_BYPASS_CONFUSION_ERR_MASK: Mask for this error: 1=masked, 0=not masked
16	RW	PCBS_READ_LPST_IN_PSTATE_MODE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
17	RW	PCBS_LPST_READ_CORR_ERR_MASK: Mask for this error: 1=masked, 0=not masked
18	RW	PCBS_LPST_READ_UNCORR_ERR_MASK: Mask for this error: 1=masked, 0=not masked
19	RW	PCBS_PFET_STRENGTH_OVERFLOW_ERR_MASK: Mask for this error: 1=masked, 0=not masked
20	RW	PCBS_VDS_LOOKUP_ERR_MASK: Mask for this error: 1=masked, 0=not masked
21	RW	PCBS_IDLE_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
22	RW	PCBS_PSTATE_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
23	RW	PCBS_GLOBAL_ACTUAL_SYNC_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
24	RW	PCBS_PMAX_SYNC_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked



Bits	PCB	Field Mnemonic: Description
25	RW	PCBS_GLOBAL_ACTUAL_PSTATE_PROTOCOL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
26	RW	PCBS_PMAX_PROTOCOL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
27	RW	PCBS_IVRM_GROSS_OR_FINE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
28	RW	PCBS_IVRM_RANGE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
29	RW	PCBS_DPLL_CPM_FMIN_ERR_MASK: Mask for this error: 1=masked, 0=not masked
30	RW	PCBS_DPLL_DCO_FULL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
31	RW	PCBS_DPLL_DCO_EMPTY_ERR_MASK: Mask for this error: 1=masked, 0=not masked
32	RW	PCBS_DPLL_INT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
33	RW	PCBS_FMIN_AND_NOT_CPMBIT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
34	RW	PCBS_DPLL_FASTER_THAN_FMAX_PLUS_DELTA1_ERR_MASK: Mask for this error: 1=masked, 0=not masked
35	RW	PCBS_DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2_ERR_MASK: Mask for this error: 1=masked, 0=not masked
36	RW	PCBS_RESCLK_CSB_INSTR_VECTOR_CHG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
37	RW	PCBS_RESCLK_BAND_BOUNDARY_CHG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
38	RW	PCBS_OCC_HEARTBEAT_LOSS_ERR_MASK: Mask for this error: 1=masked, 0=not masked
39	RW	PCBS_SPARE39_ERR_MASK: Mask for this error: 1=masked, 0=not masked
40	RW	PCBS_SPARE40_ERR_MASK: Mask for this error: 1=masked, 0=not masked
41	RW	PCBS_SPARE41_ERR_MASK: Mask for this error: 1=masked, 0=not masked
42	RW	PCBS_SPARE42_ERR_MASK: Mask for this error: 1=masked, 0=not masked

Register Name		<i>PM Special Wakeup FSP</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PMSPCWKUPFSP_REG
Address		000000001A0F010B (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RW	FSP_SPECIAL_WAKEUP: Chiplet Special Wakeup for FSP Firmware use. NOTE: protocol is required when setting this bit

Register Name		<i>PM Special Wakeup OCC</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PMSPCWKUPOCC_REG
Address		000000001A0F010C (PCB)
Attributes		
Description		

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Bits	PCB	Field Mnemonic: Description
0	RW	OCC_SPECIAL_WAKEUP: Chiplet Special Wakeup for OCC Firmware use. NOTE: protocol is required when setting this bit

Register Name	<i>PM Special Wakeup Hypervisor</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PMSPCWKUPPHYP_REG
Address	000000001A0F010D (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	PHYP_SPECIAL_WAKEUP: Chiplet Special Wakeup for hypervisor Firmware use. NOTE: protocol is required when setting this bit

Register Name	<i>PFET Control/Status Register For Core And ECO Vcs</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PFVCS_CNTLSTAT_REG
Address	000000001A0F010E (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	CORE_VCS_PFET_FORCE_STATE: Core Domain PFET Force State Provides a means for firmware to force the core domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 4:5 = 00 (both core_vcs_pfet_val_override AND core_vcs_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
2:3	RW	ECO_VCS_PFET_FORCE_STATE: ECO Domain PFET Force State Provides a means for firmware to force the ECO domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 6:7 = 00 (both eco_vcs_pfet_val_override AND eco_vcs_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
4	RW	CORE_VCS_PFET_VAL_OVERRIDE: Core Domain PFET Value Override 0 = Override is disabled
5	RW	CORE_VCS_PFET_SEL_OVERRIDE: Core Domain PFET Stage Select Override 0 = Override is disabled
6	RW	ECO_VCS_PFET_VAL_OVERRIDE: ECO Domain PFET Value Override 0 = Override is disabled
7	RW	ECO_VCS_PFET_SEL_OVERRIDE: ECO Domain PFET Stage Select Override 0 = Override is disabled

Bits	PCB	Field Mnemonic: Description
8	RW	CORE_VCS_PFET_ENABLE_REGULATION_FINGER: Core Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the core_vcs_pfet_enable_value.
9	RW	ECO_VCS_PFET_ENABLE_REGULATION_FINGER: ECO Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the eco_vcs_pfet_enable_value.
10:21	RW	CORE_VCS_PFET_ENABLE_VALUE: Core PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the Core Domain PFET Enables directly. If core_vcs_pfet_val_override = 1, a write to this field sets the state of the core PFET Enables until core_vcs_pfet_val_override is cleared. If core_vcs_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the core_vcs_pfet_valN_slav registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
22:25	RW	CORE_VCS_PFET_SEL_VALUE: Core PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure core_vcs_pfet_valN_slav(0:11) where N is 0 to 11 if core_vcs_pfet_sel_override = 1. If core_vcs_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
26:37	RW	ECO_VCS_PFET_ENABLE_VALUE: ECO PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the ECO PFET Enables directly. If ECO_vcs_pfet_val_override = 1, a write to this field sets the state of the ECO PFET Enables until ECO_vcs_pfet_val_override is cleared. If eco_vcs_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the eco_vcs_pfet_valN_slav registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
38:41	RW	ECO_VCS_PFET_SEL_VALUE: ECO PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure eco_vcs_pfet_valN_slav(0:11) where N is 0 to 11 if eco_vcs_pfet_sel_override = 1. If eco_vcs_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
42:45	ROX	CORE_VCS_PG_STATE: Core power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
46:49	ROX	CORE_VCS_PG_SEL: For debug, contains the actual index n into Core Domain PFET Value [n] SLAT Register set that contains the Core PFET Enable Value currently enabled.
50:53	ROX	ECO_VCS_PG_STATE: ECO Domain power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
54:57	ROX	ECO_VCS_PG_SEL: For debug, contains the actual index n into ECO Domain PFET Value [n] SLAT Register set that contains the ECO PFET Enable Value currently enabled.

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Register Name	<i>PM State History Register For Hypervisor</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPHYP_REG
Address	000000001A0F0110 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	PHYP_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	PHYP_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	PHYP_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	PHYP_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	PHYP_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	PHYP_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For FSP</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PMSTATEHISTFSP_REG
Address	000000001A0F0111 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	FSP_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	FSP_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	FSP_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	FSP_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.



Bits	PCB	Field Mnemonic: Description
6	ROX_CLRPAR T	FSP_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	FSP_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For OCC</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PMSTATEHISTOCC_REG
Address	000000001A0F0112 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	OCC_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	OCC_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	OCC_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	OCC_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	OCC_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	OCC_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For PerfMon</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPERF_REG
Address	000000001A0F0113 (PCB)
Attributes	
Description	

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Bits	PCB	Field Mnemonic: Description
0:2	ROX	PERF_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	PERF_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	PERF_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	PERF_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	PERF_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	PERF_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM FSM Reset And Babystepper Idle Injects</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.IDLEFSMGOTOCMD_REG
Address	000000001A0F0114 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	WO_1P	idle_fsm_goto_cmd ' A write to this reg will proceed the IDLE FSM from WAIT_FOR_PORE_DONE, SLEEP_EXIT_WAIT_FOR_PORE_FAST_EXIT_DONE, or WINKLE_EXIT_WAIT_FOR_PORE_FAST_EXIT_DONE to the following states: ' 0b01: goto IDLE state ' 0b10: goto SLEEP_EXIT_CORE_MESHLET_ON state ' 0b11: goto WINKLE_EXIT_NOTIFY_PMC state ' '
2	RWX	babystp_trigger_sleep_entry ' A write to this reg with a 1 in this field will cause the babystepper to run the sleep entry sequence. This step is needed for an assisted entry into sleep, before the power is actually turned off since the babystepper needs to know about the sleep state. For an unassisted entry, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished entering its sleep mode. '
3	RWX	babystp_trigger_winkle_entry ' A write to this reg with a 1 in this field will cause the babystepper to run the winkle entry sequence. This step is needed for an assisted entry into winkle before the power is actually turned off since the babystepper needs to know about the winkle state. For an unassisted entry, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished entering its winkle mode. '
4	RWX	babystp_trigger_wakeup ' A write to this reg with a 1 in this field will cause the babystepper to run the wakeup sequence from sleep/winkle depending on the babystepper state of sleep or winkle. This step is needed for an assisted exit from winkle before the power is actually turned off since the babystepper needs to know about the wakeup state. For an unassisted exit, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished waking up from sleep or winkle. '



Register Name	<i>Core PFET Power Up Delay</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.COREPFPUDLY_REG
Address	000000001A0F012C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_POWUP_DLY0: Delay used after transitioning to Core Domain power up sequence stage0. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	CORE_POWUP_DLY1: Delay used after transitioning to Core domain power up sequence stage1.
8:19	RW	CORE_POWER_UP_DELAY_SEL: Vector select for which delay to use for the respective power-up stage. Bit mapping: 8 -> core_*_pfet_enable(0) 9 -> core_*_pfet_enable(1) ... 19 -> core_*_pfet_enable(11) Bit meaning: 0 = Use core_powup_dly0 1 = Use core_powup_dly1

Register Name	<i>Core PFET Power Down Delay</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.COREPFPDDLY_REG
Address	000000001A0F012D (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_POWDN_DLY0: Delay used after transitioning to Core domain power dn sequence stage1. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	CORE_POWDN_DLY1: Delay used after transitioning to Core domain power dn sequence stage1. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
8:19	RW	CORE_POWER_DN_DELAY_SEL: Vector select for which delay to use for the respective power-dn stage. Bit mapping: 8 -> core_*_pfet_enable(0) 9 -> core_*_pfet_enable(1) ... 19 -> core_*_pfet_enable(11) Bit meaning: 0 = Use core_powdn_dly0 1 = Use core_powdn_dly1

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Register Name	Core PFET Vretention
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.COREPFVRET_REG
Address	000000001A0F0130 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_VRET_SEL: Pointer to the stage representing the Vretention value for the core PFETs. Power down sequences will stop after enabling this stage.
4:7	RW	CORE_VOFF_SEL: Pointer to the stage representing the Voff value for the core PFETs. Power down sequences will stop after enabling this stage.

Register Name	ECO PFET Power Up Delay
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.ECOPFPUDLY_REG
Address	000000001A0F014C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_POWUP_DLY0: Delay used after transitioning to ECO domain power up sequence stage0 in terms of refclk period (4.46ns) times 2^(15 minus this value). Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	ECO_POWUP_DLY1: Delay used after transitioning to ECO domain power up sequence stage1.
8:19	RW	ECO_POWER_UP_DELAY_SEL: Vector select for which delay to use for the respective power-up stage. Bit mapping: 8 -> eco_*_pfet_enable(0) 9 -> eco_*_pfet_enable(1) ... 19 -> eco_*_pfet_enable(11) Bit meaning: 0 = Use eco_powup_dly0 1 = Use eco_powup_dly1

Register Name	ECO PFET Power Down Delay
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.ECOPFPDDLY_REG
Address	000000001A0F014D (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_POWDN_DLY0: UNUSED/SPARE
4:7	RW	ECO_POWDN_DLY1: Delay used after transitioning to ECO Domain power dn sequence stage1. The delays in this register are in terms of refclk period (4.46ns) times 2^(15 minus this value). Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.

Bits	PCB	Field Mnemonic: Description
8:19	RW	ECO_POWER_DN_DELAY_SEL: Vector select for which delay to use for the respective power-down stage. Bit mapping: 8 -> eco_*_pfet_enable(0) 9 -> eco_*_pfet_enable(1) ... 19 -> eco_*_pfet_enable(11) Bit meaning: 0 = Use eco_powdn_dly0 1 = Use eco_powdn_dly1

Register Name		<i>ECO PFET Vretention</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.ECOPFVRET_REG
Address		000000001A0F0150 (PCB)
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_VRET_SEL: Pointer to the stage representing the Vretention value for the ECO PFETs. Power down sequences will stop after enabling this stage.
4:7	RW	ECO_VOFF_SEL: Pointer to the stage representing the Voff value for the ECO PFETs. Power down sequences will stop after enabling this stage.

Register Name		<i>Frequency Control Register With Overrides For DPLL</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.FREQ_CTRL_REG
Address		000000001A0F0151 (PCB)
Attributes		
Description		Note that overrides to Dpll_fmax are only applied if Dpll_freq_override_enable = 1. A read of all these dials always returns the currently established DPLL frequencies (regardless of any other mode settings).

Bits	PCB	Field Mnemonic: Description
0:8	RO	Reserved.
9:17	RWX	DPLL_FMAX: DPLL maximum frequency and frequin (these two values are the same in POWER8 processor) without applying bias values: A read always returns the currently established value A write is conditioned on the setting of dpll_freq_override_enable. If dpll_freq_override_enable is asserted, a write causes this field to update. Otherwise the hardware (that is, PStates) are controlling the update of this value.
18:21	RO	Reserved.
22:30	RW	FREQU_AT_PSTATE0: DPLL frequency for Pstate 0

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Register Name	<i>DPLL Mode Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.DPLL_CPM_PARM_REG
Address	000000001A0F0152 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	LF_SLEWRATEXPI: out of lock slew rate for DPLL
8	RW	LF_USE_CPMXPI: use CPM instead of PFD as loop filter input, if '1' (instead of using both)
9	RW	FF_USE_CPMXPI: use the CPM inputs for the frequency filter, if '1'
10	RW	CPM_FILTER_ENABLE: enables the CPM filter
11	RW	FF_BYPASSXPI: enables frequency filter bypass
12	RW	DCO_OVERRIDE: enables overrides for DCO testing/characterization
13	RW	DCO_INCR: enables increment for DCO testing/characterization, increments only on a rising edge
14	RW	DCO_DECR: enables decrement for DCO testing/characterization, decrements only on a rising edge
15:23	RW	DPLL_LOCK_TIMER_REPLACEMENT_VALUE: if dpll_lock_replacement_timer_mode_en is set, this dial specifies the delay in us, after which it is assumed, that the DPLL has reached a frequency lock condition. Note that values less than 3 will cause in undefined HW behavior (0 will cause HANGs!). if dpll_lock_replacement_timer_mode_en is zero, this dial specifies the delay in pcb_nclk cycles after which the hardware monitors the DPLL frequout output (if dpll_freqout_mode_en is set) or the DPLL flock output (if dpll_flock_mode_en is set). Note that in this case, the value of this dial needs to be greater or equal to 150 (decimal).
24:31	RW	PRE_VRET_PSTATE: Pstate that is stepped to before switching to Vretention defined in PCBS_iVRM_Control_Status_Reg
32	RW	OVERRIDE_PCBS_DPLL_SYNCHRONIZER: Bypasses the 'ping-pong' synchronization logic between the DPLL and the PCBS-PM. NEVER SET TO 1 UNLESS YOU KNOW WHAT YOU ARE DOING!
33:36	RW	DPLL_CHAR_DELTA1: Delta in DPLL ticks for characterization (cf. dial dpll_faster_than_fmax_plus_delta1)
37:40	RW	DPLL_CHAR_DELTA2: Delta in DPLL ticks for characterization (cf. dial dpll_faster_than_fmin_minus_delta2)

Register Name	<i>PPMSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_STATUS_REG
Address	000000001A0F0153 (PCB)
Attributes	
Description	Provides read access to the power management status that is also shadowed to the PC and visible to the hypervisor in the PMSR (with some delay due to the shadowing process).

Bits	PCB	Field Mnemonic: Description
0:7	ROX	global_pstate_actual ' Actual Global Pstate Pstate or Pglobal_actual ' " Reads from this field return the presently established global PState value.' " "Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent '

Bits	PCB	Field Mnemonic: Description
8:15	ROX	LOCAL_PSTATE_ACTUAL: ' Actual Local PState or Plocal_actual' " 'Reads from this field return the presently established local PState value. This value will always be less than or equal to global_pstate_actual.' " 'Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent' "
16:23	ROX	pv_min Minimum Pstate set by the platform.
24:31	ROX	pvf_max Maximum Pstate set by the platform.
32	ROX	spr_em_disabled ' SPR Energy Management Disabled' 'Read from this field indicate whether the platform has disabled the 'PMCR and PMICR SPRs to control the chiplet PState. '
33	ROX	Psafe_mode_active Read from this field indicate whether the chiplet has been put into a safe mode with Psafe enabled to a OCC heartbeat loss or other externally forced reasons (0=regular mode, 1=safe mode is active)
34	ROX	iVRM_safe_mode_active Read from this field indicate whether the chiplet has been put the iVRM safe mode (forcing the bypass mode for all iVRMs)
35	ROX	ivrm_enable Read from this field indicate whether the chiplet internal voltage regulation macro is enabled for localized voltage control (0=disabled, 1=enabled) based on ANDing the poweron signals to the iVRMs
36	ROX	all_fsms_in_safe_state For recovery: if this bit is asserted, all Pstate and iVRM control FSMs are in a stable, safe state that allows the recovery routine to proceed with resetting the PCBS PM without the risk of interrupt a critical action
37:40	ROX	pmsr_spares spare bits

Register Name	<i>PIVRMCSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_CONTROL_STATUS_REG
Address	000000001A0F0154 (PCB)
Attributes	
Description	Provides access to chiplet-level controls of the internal VRM rail set (VDD and VCS) across both the core and ECO domains. The following is valid only for bits 4 to 7. When in automatic iVRM mode (ivrm_fsm_enable = 1), these bits provide access to the values established by the automatic hardware mechanism. When In iVRM override mode (ivrm_fsm_enable = 0), these bits allow firmware direct control of the values driving the internal VRMs.

Bits	PCB	Field Mnemonic: Description
0	RW	IVRM_FSM_ENABLE: Internal master VRM FSM Enable 0 = Disable Internal VRM FSMs and enable to control the iVRMs with the available override registers (SCOMable) as a backup mode or for setup (override mode) 1 = Enable Internal VRM FSM sequencers (requires that Pstates are enabled with enable_Pstate_mode=1 as well) (automatic mode)
1	RW	USE_IVRM_FOR_VRET: Internal VRM Enabled for Vretention 0 = Disable Internal VRM for Vretention 1 = Enable Internal VRM for Vretention
2	RW	BINSEARCH_CAL_ENA: trigger binary search (level signal)

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Bits	PCB	Field Mnemonic: Description
3	RW	PVREF_EN: Internal VRM Power Voltage Reference Forced Enable 0 = Allow hardware to enable/disable pvref circuit 1 = Force enablement of the pvref circuit
4	RWX	IVRM_CORE_VDD_BYPASS_B: Internal VRM Core VDD Bypass (negative active) 0 = VDD Internal Core VRMs in bypass 1 = VDD internal Core VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
5	RWX	IVRM_CORE_VDD_POWERON: Internal VRM Core VDD Poweron 0 = Core VDD Internal VRMs powered off 1 = Core VDD internal VRMs powered on if this bit is not set (=0), the Core VDD internal VRM powered off internally. If this bit is set (=1), the Core VDD internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
6	RWX	IVRM_CORE_VCS_BYPASS_B: Internal VRM Core VCS Bypass (negative active) 0 = VCS Internal Core VRMs in bypass 1 = VCS internal Core VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VCS internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VCS internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
7	RWX	IVRM_CORE_VCS_POWERON: Internal VRM Core VCS Poweron 0 = Core VCS Internal VRMs powered off 1 = Core VCS internal VRMs powered on if this bit is not set (=0), the Core VCS internal VRM powered off internally. If this bit is set (=1), the Core VCS internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
8	RWX	IVRM_ECO_VDD_BYPASS_B: Internal VRM ECO VDD Bypass (negative active) 0 = VDD Internal ECO VRMs in bypass 1 = VDD internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
9	RWX	IVRM_ECO_VDD_POWERON: Internal VRM ECO VDD Bypass (negative active) 0 = VDD Internal ECO VRMs in bypass 1 = VDD internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.

Bits	PCB	Field Mnemonic: Description
10	RWX	IVRM_ECO_VCS_BYPASS_B: Internal VRM ECO VCS Bypass (negative active) 0 = VCS Internal ECO VRMs in bypass 1 = VCS internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VCS internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VCS internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
11	RWX	IVRM_ECO_VCS_POWERON: Internal VRM ECO VCS Poweron 0 = ECO VCS Internal VRMs powered off 1 = ECO VCS internal VRMs powered on if this bit is not set (=0), the ECO VCS internal VRM powered off internally. If this bit is set (=1), the ECO VCS internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
12:18	RWX	IVRM_VRET_VDD: if use_ivrm_for_Vret is asserted, this dial is used to control the Vdd retention voltage. Note: this field will establish the Core VDD rail for Sleep and both the Core and ECO rail for Winkle. - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
19:25	RWX	IVRM_VRET_VCS: if use_ivrm_for_Vret is asserted, this dial is used to control the Vcs retention voltage. Note: this field will establish the Core VDD rail for Sleep and both the Core and ECO rail for Winkle. - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
26:30	RWX	IVRM_VRET_CORE_VDD_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the Core Vdd iVRM PFET strength for the retention voltage
31:35	RWX	IVRM_VRET_CORE_VCS_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the Core Vcs iVRM PFET strength for the retention voltage
36:40	RWX	IVRM_VRET_ECO_VDD_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the ECO Vdd iVRM PFET strength for the retention voltage
41:45	RWX	IVRM_VRET_ECO_VCS_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the ECO Vcs iVRM PFET strength for the retention voltage
46	RW	PVREF_FAIL: voltage reference fail input to iVRMs
47	ROX	IVRM_PREF_ERROR_GROSS: Voltage Reference Gross Error 0 = Gross Error not detected 1 = Gross Error detected
48	ROX	IVRM_PREF_ERROR_FINE: Voltage Reference Fine Error 0 = Fine Error not detected 1 = Fine Error detected
49	ROX	IVRM_CORE_VDD_RANGE_HI: Core VDD Internal VRM Range Hi Indicator 0 = Core VDD Internal VRM Hi indicator signal not asserted 1 = Core VDD internal VRMs Hi indicator signal asserted
50	ROX	IVRM_CORE_VDD_RANGE_LO: Core VDD Internal VRM Range Low Indicator 0 = Core VDD Internal VRM Low indicator signal not asserted 1 = Core VDD internal VRMs Low indicator signal asserted

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Bits	PCB	Field Mnemonic: Description
51	ROX	IVRM_ECO_VDD_RANGE_HI: ECO VDD Internal VRM Range Hi Indicator 0 = ECO VDD Internal VRM Hi indicator signal not asserted 1 = ECO VDD internal VRMs Hi indicator signal asserted
52	ROX	IVRM_ECO_VDD_RANGE_LO: ECO VDD Internal VRM Range Low Indicator 0 = ECO VDD Internal VRM Low indicator signal not asserted 1 = ECO VDD internal VRMs Low indicator signal asserted
53	ROX	IVRM_CORE_VCS_RANGE_HI: Core VCS Internal VRM Range Hi Indicator 0 = Core VCS Internal VRM Hi indicator signal not asserted 1 = Core VCS internal VRMs Hi indicator signal asserted
54	ROX	IVRM_CORE_VCS_RANGE_LO: Core VCS Internal VRM Range Low Indicator 0 = Core VCS Internal VRM Low indicator signal not asserted 1 = Core VCS internal VRMs Low indicator signal asserted
55	ROX	IVRM_ECO_VCS_RANGE_HI: ECO VCS Internal VRM Range Hi Indicator 0 = ECO VCS Internal VRM Hi indicator signal not asserted 1 = ECO VCS internal VRMs Hi indicator signal asserted
56	ROX	IVRM_ECO_VCS_RANGE_LO: ECO VCS Internal VRM Range Low Indicator 0 = ECO VCS Internal VRM Low indicator signal not asserted 1 = ECO VCS internal VRMs Low indicator signal asserted
57	ROX	BINSEARCH_CAL_DONE: binary search done signal
58	RWX	IVRM_CORE_VDD_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
59	RWX	IVRM_CORE_VCS_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
60	RWX	IVRM_ECO_VDD_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
61	RWX	IVRM_ECO_VCS_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
62	RW	IVRM_POWER_DOWN_DISABLE: If this bit is 1, the iVRM poweron signal is left asserted. Power off of the iVRMs is then blocked

Register Name	<i>PIVRMVSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VALUE_SETTING_REG
Address	000000001A0F0155 (PCB)
Attributes	
Description	Allows access to VID values and PFET strength valid signal settings presented to the internal VRM rail set (VDD and VCS) across both the core and ECO domains. When in <code>ivrm_fsm_enable = "auto"</code> mode, this register provides access to the values established by the automatic hardware mechanism. When <code>ivrm_fsm_enable = "override"</code> mode, this register allows firmware direct control of the values driving the internal VRMs which, if the VRMs are not in bypass, will move the voltage settings.

Bits	PCB	Field Mnemonic: Description
0:7	RWX	IVRM_CORE_VDD_IVID: When read, returns the value presently being driving to the Core VDD iVRM. If <code>ivrm_fsm_enable = 0</code> (<code>override_mode</code>), then writes to this field will drive a new VID value to the Core VDD iVRM. If <code>ivrm_fsm_enable = 1</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
8:15	RWX	IVRM_CORE_VCS_IVID: When read, returns the value presently being driving to the Core VCS iVRM. If <code>ivrm_fsm_enable = 0</code> (<code>override_mode</code>), then writes to this field will drive a new VID value to the Core VCS iVRM. If <code>ivrm_fsm_enable = 1</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
16:23	RWX	IVRM_ECO_VDD_IVID: When read, returns the value presently being driving to the Core VDD iVRM. If <code>ivrm_fsm_enable = 0</code> (<code>override_mode</code>), then writes to this field will drive a new VID value to the ECO VDD iVRM. If <code>ivrm_fsm_enable = 1</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
24:31	RWX	IVRM_ECO_VCS_IVID: When read, returns the value presently being driving to the ECO VCS iVRM. If <code>ivrm_fsm_enable = 0</code> (<code>override_mode</code>), then writes to this field will drive a new VID value to the ECO VCS iVRM, If <code>ivrm_fsm_enable = 0</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
32:36	RWX	IVRM_CORE_VDD_PFET_STRENGTH: When read, returns the value presently being driving to the core VCS iVRM. If <code>ivrm_fsm_enable = 0</code> (<code>override_mode</code>), then writes to this field will drive a new strength value to the core VCS iVRM, If <code>ivrm_fsm_enable = 0</code> , writes to this field are not performed.

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Bits	PCB	Field Mnemonic: Description
37:41	RWX	IVRM_CORE_VCS_PFET_STRENGTH: This register is assigned to the signals tcex##_tp_ivrm_core_vcs_sense & tcex##_tp_ivrm_core_vdd_sense & tcex##_tp_ivrm_eco_vcs_sense & tcex##_tp_ivrm_eco_vdd_sense & 0b0 Note that all other sense signals are spares now and tied to 0. OUTDATED TEXT: When read, returns the value presently being driving to the core VDD iVRM. If ivrm_fsm_enable =0 (override_mode), then writes to this field will drive a new strength value to the core VDD iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
42:46	RWX	IVRM_ECO_VDD_PFET_STRENGTH: When read, returns the value presently being driving to the ECO VCS iVRM. If ivrm_fsm_enable =0 (override_mode), then writes to this field will drive a new strength value to the ECO VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
47:51	RWX	IVRM_ECO_VCS_PFET_STRENGTH: When read, returns the value presently being driving to the ECO VDD iVRM. If ivrm_fsm_enable =0 (override_mode), then writes to this field will drive a new strength value to the ECO VDD iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
52	RWX	IVRM_VDD_CORE_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the Core VDD iVRM. If ivrm_fsm_enable =1 AND ivrm_control_mode = 1 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the Core VDD iVRM, If ivrm_fsm_enable = 0 OR ivrm_control_mode = 0, writes to this field are not performed.
53	RWX	IVRM_VCS_CORE_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the Core VCS iVRM. If ivrm_fsm_enable =0 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the Core VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
54	RWX	IVRM_VDD_ECO_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the ECO VDD iVRM. If ivrm_fsm_enable =1 AND ivrm_control_mode = 1 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the ECO VDD iVRM, If ivrm_fsm_enable = 0 OR ivrm_control_mode = 0, writes to this field are not performed.
55	RWX	IVRM_VCS_ECO_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the ECO VCS iVRM. If ivrm_fsm_enable =0 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the ECO VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
56	RWX	CORE_VDD_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable =0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
57	RWX	CORE_VCS_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable =0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
58	RWX	ECO_VDD_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable =0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
59	RWX	ECO_VCS_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable =0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.

Register Name		<i>General PCBS Modes And Chicken Switches</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBSPM_MODE_REG
Address		000000001A0F0156 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RW	ENABLE_PSTATE_MODE: if asserted, Pstate requests (from overrides or PMCR) will be honored, otherwise, the hardware does not do anything. Note to firmware: this is the master switch for Pstates and should be asserted after all sub-modes (that is, lvrn_fsm_en) are setup to avoid enabling unintentional modes during the mode setup.
1	RW	GLOBAL_PSTATE_CHANGE_FOR_IDLE_STATE_ENABLED: if asserted, a global Pstate change to the Nap/Sleep/Winkle-Pstate is requested, when the Nap/Sleep/Winkle state is entered and the individual enable bits in the PIMCR are asserted
2	RW	ENABLE_GLOBAL_PSTATE_REQ: if '1' then enable PMC interrupt with global Pstate change request, otherwise, disable global requests
3	RW	ENABLE_WINKLE_WITH_CPM_MODE: if '1', PCBS automatically changes the DPLL mode to mode 1, when entering winkle, but changes the mode back to CPM mode when exiting. Needed for CPM-DPLL control loop enablement.
4	RW	ENABLE_CLIPPING_OF_GLOBAL_PSTATE_REQ: if '1', PCBS automatically clips global Pstate requests with Pvf_max in PPMBR and sets the 'donate' bit in the interrupt accordingly
5	RW	CHKSW_HW214553: if deasserted, HW214553 (frequin issue in resclk mode) is fixed, if asserted, the fix is not active
6	RW	ENABLE_PMC_PMAX_SYNC_NOTIFICATION: if asserted, the PCBS-PM will send a 'Pmax_sync' interrupt, once the synchronization criterion is met
7	RW	DPLL_LOCK_REPLACEMENT_TIMER_MODE_EN: Select a timer instead of the DPLL lock bit as target frequency reached criterion. This timer has to be setup by the dial dpll_lock_timer_replacement_value. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
8	RW	DPLL_FREQOUT_MODE_EN: Looks at the DPLL frequout to find out, if the target frequency has been reached. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
9	RW	DPLL_FLOCK_MODE_EN: Looks at the real DPLL flock output to find out, if the target frequency has been reached. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
10	RW	ENABLE_SENSE_DELAY_CHARACTERIZATION: If this switch is 0, the sense latches are updated every cycle. If this switch is 1, the sense delay measurement mode is enabled, that starts a sense delay timer, whenever one of the registers that drive the inputs of the iVRMs/pFETs is written via PCB and that triggers a sense register freeze operation, when the sense delay timer reaches the value sense_delay_timer_val. With this mode, the sense delays can be measured in multiples of the PCB-slave clock speed.
11:17	RW	SENSE_DELAY_TIMER_VAL: See the description of enable_sense_delay_characterization for details.
18:19	RW	CPM_FMIN_CLIP_ERROR_SEL: This dial selects, which of the following conditions will cause the FIR bit dpll_fmin_and_not_cpmbit to be set to detect, that the DPLL runs at Fmin, but is still clipped by the CPMs. 0b00 = function is disabled 0b01 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit2 = 0 0b10 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit1 = 0 0b11 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit0 = 0
20:23	RW	DBG_TRACE_SEL: This dial selects the group of signals to be traced for debug in the lab. Details to be found in the Section 'Trace Bus'

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Bits	PCB	Field Mnemonic: Description
24:25	RW	TRACE_DATA_SEL: This dial selects the group of signals to be traced for debug in the lab. Details to be found in the Section 'Trace Bus'
26:29	RW	TP_CPLT_IVRM_VPP_TUNE: Tune bits to be set going to the iVRMs

Register Name	<i>PIVRMPS Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_PFETSTR_SENSE_REG
Address	000000001A0F0157 (PCB)
Attributes	
Description	Used to check that the pFET sense outputs correspond to the driven values (mainly for test).

Bits	PCB	Field Mnemonic: Description
0:4	ROX	IVRM_CORE_VDD_PFETSTR_SNS: Not used any more.
5:9	ROX	IVRM_CORE_VCS_PFETSTR_SNS: This register is assigned to the signals tcex##_tp_ivrm_core_vcs_sense & tcex##_tp_ivrm_core_vdd_sense & tcex##_tp_ivrm_eco_vcs_sense & tcex##_tp_ivrm_eco_vdd_sense & 0b0
10:14	ROX	IVRM_ECO_VDD_PFETSTR_SNS: Not used any more.
15:19	ROX	IVRM_ECO_VCS_PFETSTR_SNS: Not used any more.
20	ROX	IVRM_VDD_CORE_PFETSTR_VALID_SNS: Not used any more.
21	ROX	IVRM_VCS_CORE_PFETSTR_VALID_SNS: Not used any more.
22	ROX	IVRM_VDD_ECO_PFETSTR_VALID_SNS: Not used any more.
23	ROX	IVRM_VCS_ECO_PFETSTR_VALID_SNS: Not used any more.
24	ROX	CORE_VDD_BYPASS_B_SENSE: Not used any more.
25	ROX	CORE_VCS_BYPASS_B_SENSE: Not used any more.
26	ROX	ECO_VDD_BYPASS_B_SENSE: Not used any more.
27	ROX	ECO_VCS_BYPASS_B_SENSE: Not used any more.
28	ROX	CORE_VDD_POWERON_SENSE: Not used any more.
29	ROX	CORE_VCS_POWERON_SENSE: Not used any more.
30	ROX	ECO_VDD_POWERON_SENSE: Not used any more.
31	ROX	ECO_VCS_POWERON_SENSE: Not used any more.
32	ROX	CORE_VDD_VPUMP_EN_SENSE: Not used any more.
33	ROX	CORE_VCS_VPUMP_EN_SENSE: Not used any more.
34	ROX	ECO_VDD_VPUMP_EN_SENSE: Not used any more.
35	ROX	ECO_VCS_VPUMP_EN_SENSE: Not used any more.
36	ROX	CORE_VDD_PFET_LOW_VOUT_SNS: Not used any more.
37	ROX	CORE_VCS_PFET_LOW_VOUT_SNS: Not used any more.
38	ROX	ECO_VDD_PFET_LOW_VOUT_SNS: Not used any more.
39	ROX	ECO_VCS_PFET_LOW_VOUT_SNS: Not used any more.



Register Name	PPMICR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_IDLE_CONTROL_REG
Address	000000001A0F0158 (PCB)
Attributes	
Description	Used to read the PMICR register typically owned (written) by the hypervisor. Writes are conditioned on the setting of the dial Pm_spr_override_en. If Pm_spr_override_en is set, firmware must make sure that the special wakeup state of this chiplet is reached before changing any of the latency fields in this register. Otherwise, the hardware behavior is undefined.

Bits	PCB	Field Mnemonic: Description
0:7	ROX	NAP_PSTATE_REQ: Nap Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
8	ROX	NAP_PSTATE_EN: Nap PState Enable 1 = Enable the Nap Pstate (NPS) Request, Nap Global Enable and Nap Latency functions 0 = Disables the Nap Pstate (NPS) Request, Nap Global Enable and Nap Latency functions Reads from the field return the value last written.
9	ROX	NAP_GLOBAL_EN: Nap Global Enable 1 = Upon the execution of a Nap instruction , the Nap Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a Nap instruction , the Nap Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.
10:11	ROX	NAP_LATENCY: Nap Latency not supported for POWER8 processor
12:15	ROX	RESERVED_PPMICR_0: reserved
16:23	ROX	SLEEP_PSTATE_REQ: sleep Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
24	ROX	SLEEP_PSTATE_EN: sleep PState Enable 1 = Enable the sleep Pstate (NPS) Request, sleep Global Enable and sleep Latency functions 0 = Disables the sleep Pstate (NPS) Request, sleep Global Enable and sleep Latency functions Reads from the field return the value last written.
25	ROX	SLEEP_GLOBAL_EN: sleep Global Enable 1 = Upon the execution of a sleep instruction , the sleep Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a sleep instruction , the sleep Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.

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Bits	PCB	Field Mnemonic: Description
26:27	ROX	SLEEP_LATENCY: sleep Latency 00 = Cease instructions and honors Pstate change but does not perform additional state changing actions (unsupported in POWER8, maps to 0b10) 01 = Indicates to the platform that a sub-state that would have the lowest latency is enabled (unsupported in POWER8, maps to 0b10) 10 = Indicates to the platform that a sub-state that might have a medium exit latency is enabled (POWER8: Fast Sleep) 11 = Indicates to the platform that a sub-state that might have higher exit latency is enabled (POWER8: Deep Sleep)
28:31	ROX	RESERVED_PPMICR_1: reserved
32:39	ROX	WINKLE_PSTATE_REQ: winkle Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
40	ROX	WINKLE_PSTATE_EN: winkle PState Enable 1 = Enable the winkle Pstate (NPS) Request, winkle Global Enable and winkle Latency functions 0 = Disables the winkle Pstate (NPS) Request, winkle Global Enable and winkle Latency functions Reads from the field return the value last written.
41	ROX	WINKLE_GLOBAL_EN: winkle Global Enable 1 = Upon the execution of a winkle instruction , the winkle Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a winkle instruction , the winkle Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.
42:43	ROX	WINKLE_LATENCY: winkle Latency 00 = Cease instructions and honors Pstate change but does not perform additional state changing actions (unsupported in POWER8, maps to 0b10) 01 = Indicates to the platform that a sub-state that would have the lowest latency is enabled (unsupported in POWER8, maps to 0b10) 10 = Indicates to the platform that a sub-state that might have a medium exit latency is enabled (POWER8: Fast Winkle) 11 = Indicates to the platform that a sub-state that might have higher exit latency is enabled (POWER8: Deep Winkle)
44:47	ROX	RESERVED_PPMICR_2: reserved

Register Name	PPMCR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_CONTROL_REG
Address	000000001A0F0159 (PCB)
Attributes	
Description	Provides read access to the PMCR register shadow in the PCBS, typically owned (written) by the hypervisor. Writes are conditioned on the setting of PMGP1[pm_spr_override_en].

Bits	PCB	Field Mnemonic: Description
0:7	RWX	GLOBAL_PSTATE_REQ: global Pstate request from hypervisor (or OCC)
8:15	RWX	LOCAL_PSTATE_REQ: local Pstate request from hypervisor or OCC
16	RWX	AUTO_OVERRIDE0_PSTATE_LIMIT_EN: automatic override Pstate 0 (for low activity detection) is enabled, if asserted



Bits	PCB	Field Mnemonic: Description
17	RWX	AUTO_OVERRIDE1_PSTATE_LIMIT_EN: automatic override Pstate 1 (reserved for future use) is enabled, if asserted
18:23	RWX	RESERVED_PPMCR: reserved
24:31	RWX	AUTO_OVERRIDE_PSTATE0: automatic override Pstate 0 (for low activity detection)
32:39	RWX	AUTO_OVERRIDE_PSTATE1: automatic override Pstate 1 (reserved for future use)

Register Name	<i>Control Register That Is Written By PMC Sequencer</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_PMC_VF_CTRL_REG
Address	000000001A0F015A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PGLOBAL_ACTUAL: global actual Pstate
8:15	RW	MAXREGVCS: maximum regulation point for Vcs, Bit 0 is reserved, bits 1 to 7 are in iVID format
16:23	RW	MAXREGVDD: maximum regulation point for Vdd, Bit 0 is reserved, bits 1 to 7 are in iVID format
24:31	RW	EVIDVCS_EFF: eff. external voltage ID for Vcs in iVID format, Bit 0 is reserved
32:39	RW	EVIDVDD_EFF: eff. external voltage ID for Vdd in iVID format, Bit 0 is reserved

Register Name	<i>Undervolting Register For PCBS</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_UNDERVOLTING_REG
Address	000000001A0F015B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PUV_MIN: minimum Pstate for which undervolting is allowed
8:15	RW	PUV_MAX: maximum Pstate for which undervolting is allowed
16:21	RW	KUV: this value indicates how many Pstate ticks a voltage request is undervolted (clipped with Puv_min). Note that the Kuv value is signed

Register Name	<i>PPSIBR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_INDEX_BOUND_REG
Address	000000001A0F015C (PCB)
Attributes	
Description	Enables setting the minimum and maximum Pstate that is supported as a pointer into the local Pstate table (which has entries from 0 to 127).

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Bits	PCB	Field Mnemonic: Description
0:7	RW	LPSI_MIN: this Pstate index is the index that corresponds to array entry 0. Note that the index domain is obtained by adding 128 to a Pstate, thus, the value is unsigned.
8:14	RW	LPSI_ENTRIES_MINUS_1: this dial contains the value of the number of entries in the Pstate table minus 1

Register Name	<i>PPMBR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_BOUNDS_REG
Address	000000001A0F015D (PCB)
Attributes	
Description	Enables setting the Pstate bounds that are managed by the OCC. If dial Enable_pmc_pmax_sync_notification is set, firmware must wait after each write to this register until the PMC has received the Pmax Sync Interrupt. If a write happens to this register while the previously scheduled Pmax Sync Interrupt has not yet left PCBS, the error TBD will be set.

Bits	PCB	Field Mnemonic: Description
0:7	RW	PMIN_CLIP: minimum Pstate allowed for this chiplet
8:15	RW	PMAX_CLIP: maximum Pstate allowed for this chiplet (has to be greater or equal to Pmin_clip)

Register Name	<i>PPTCR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_CTRL_REG
Address	000000001A0F015E (PCB)
Attributes	
Description	Controls the address for writing the local Pstate table array (all 96 words are accessible). Note that the protocol requires this register to be set up with the Pstate address first, if a read or a write of the Pstate array is intended, to make sure that the initial address is set correctly. The register PPTR must always be written or read afterward. Note that any access to the PPTR auto-increments this register.

Bits	PCB	Field Mnemonic: Description
0:6	RWX	PSTATE_TABLE_ADDRESS: This is the address of the Pstate table in PCBS, which is auto-incremented after any access to the PTLR.

Register Name	<i>PPTR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_REG
Address	000000001A0F015F (PCB)
Attributes	
Description	Controls the data to be written into the Pstate table and returns the data for a read of the Pstate table. Note that the protocol requires for a write to set this register up after first setting up PPTCR (if the user does not rely on the auto-increment function of the address). For a read of the Pstate table, this register must be read after first setting up PPTCR as well (again if the auto-increment feature of the address is not used). Any access to this register auto-increments the Pstate_table_address by 1. Note also that the read functionality of this register is only functional if PIVRMCSR[ivrm_fsm_enable] = 0. The write functionality works in any case.

Bits	PCB	Field Mnemonic: Description
0:63	RW	pstate_data This is the field for data bits 0 to 63

Register Name	<i>PPSTR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_STEP_TARGET_REG
Address	000000001A0F0160 (PCB)
Attributes	
Description	Provides read access to several intermediate values in the Pstate computation pipeline. Writes are conditioned on the setting of PMGP0[enable_OCC_ctrl_for_local_Pstate_eff_req].

Bits	PCB	Field Mnemonic: Description
0:7	RWX	LOCAL_PSTATE_EFF_REQ: this field represents the effective local Pstate request right before the clipping with Pmin and Pmax if enable_OCC_ctrl_for_local_Pstate_eff_req=0 then the hardware controls this dial, that updates every cycle if enable_OCC_ctrl_for_local_Pstate_eff_req=1 then OCC is in control and can write this field to control the effective local Pstate request that will eventually propagate through the downstream logic and determine the Local PState Actual. Note: if no write to this register is performed, the currently established value is maintained stable forever.
8:15	ROX	LOCAL_PSTATE_TARGET: This field is the target Pstate of a complete Pstate change that is performed in smaller steps
16:23	ROX	LOCAL_CORE_PSTATE_STEP_TARGET: this field represents the intermediate value that is about to be established as the next Local Pstate Actual after completing one step in the process of the transition towards the 'local_Pstate_target' the new voltage, frequency, and clock resonance setting
24:31	ROX	LOCAL_ECO_PSTATE_STEP_TARGET: this field represents the intermediate value that is about to be established as the next Local Pstate Actual after completing one step in the process of the transition towards the 'local_Pstate_target' the new voltage, frequency, and clock resonance setting

Register Name	<i>Read-Only Status Register For DPLL And For Debugging (PDSR)</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_DPLL_STATUS_REG
Address	000000001A0F0161 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:14	ROX	DPLL_FF_FREQOUT: frequout output from DPLL (current frequency - bits 2 to 10 correspond to the same scale as the 9 bits of frequin (which need to be multiplied with our frequency step to get the real frequency), the remaining bits just provide a higher accuracy)
15	ROX	DPLL_FREQU_CHANGE: DPLL Frequency change (pin of DPLL without filter)
16	ROX	DPLL_STATUS_SPARE_BIT1: Spare bit.
17	ROX	PMAX_SYNC_PENDING: gets asserted, if the logic has a Pmax sync interrupt outstanding that will be eventually sent to PMC when the Pmax sync criterion is met
18	ROX	GA_ACK_PENDING: gets asserted, if the logic has a global actual Pstate update acknowledgment interrupt outstanding that will be eventually sent to PMC when the GA ack criterion is met
19:26	ROX	CAPPED_GLOBAL_PSTATE_REQ: corresponds to the capped global Pstate request that is presented as Pstate interrupt and send to PMC

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Bits	PCB	Field Mnemonic: Description
27	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT2: DPLL runs at Fmax and CPM bit 2 is set. Note that this bit and the following 2 bits indicate, that the CPMs would allow the DPLL to run faster than Fmax.
28	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT3: DPLL runs at Fmax and CPM bit 3 is set
29	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT4: DPLL runs at Fmax and CPM bit 4 is set
30	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT2: DPLL runs at Fmin and CPM bit2 is zero. Note that this bit and the following 2 bits indicate, that the CPMs indicate, that the DPLL should run slower than the currently established Fmin.
31	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT1: DPLL runs at Fmin and CPM bit1 is zero
32	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT0: DPLL runs at Fmin and CPM bit0 is zero
33	ROX_CLRPAR T	DPLL_FASTER_THAN_FMAX_PLUS_DELTA1: The DPLL indicated that it ran once faster than Fmax+dppl_char_delta1
34	ROX_CLRPAR T	DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2: The DPLL indicated that it ran once slower than Fmin-dppl_char_delta2
35:48	ROX	DPLL_MAX_FREQOUT_AFTER_LAST_READ: This dial indicates the maximum DPLL frequout value after the last read of this register (only 14 MSBs)
49:62	ROX	DPLL_MIN_FREQOUT_AFTER_LAST_READ: This dial indicates the minimum DPLL frequout value after the last read of this register (only 14 MSBs)

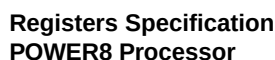
Register Name	<i>The PIVRMVCR0 Controls The Voltage Stepping Delays</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG0
Address	000000001A0F0162 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	IVRM_REQ_PSTATE_STEPDELAY_RISING: Requested Internal Pstate Baby Step Delay - Rising Step. Delay before allowing the next step for a rising Pstate Transition. This dial and ivrm_req_Pstate_stepdelay_lowering allow for differing delays for the two directional transitions if necessary. In 100ns units as established by scan dial ivrm_100ns_value
8:15	RW	IVRM_REQ_PSTATE_STEPDELAY_LOWERING: Requested Internal Pstate Baby Step Delay - Lowering Step. Delay before allowing the next step for a lower Pstate Transition. This dial and ivrm_req_Pstate_stepdelay_rising allow for differing delays for the two directional transitions if necessary. In 100ns units as established by scan dial ivrm_100ns_value

Register Name	<i>PIVRMVCR1 Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG1
Address	000000001A0F0163 (PCB)
Attributes	
Description	The PIVRMVCR1 controls the voltage stepping delays.



Bits	PCB	Field Mnemonic: Description
0:7	RW	IVRM_STABILIZE_DELAY_RUN: Stabilization Delay - Run Time Delay to allow a rail to stabilize upon a baby step while the region is operational. In 100ns units as established by scan dial ivrm_100ns_value
8:15	RW	IVRM_STABILIZE_DELAY_IDLE: Stabilization Delay - Idle Transition Delay to allow a rail to stabilize upon a baby step during an idle transition where the activity in the region is quiesced. In 100ns units as established by scan dial ivrm_100ns_value
16:23	RW	IVRM_PFSTR_PROP_DELAY: PFET Strength Propagation Delay Time from PFET Strength values being launched till PFET Strength Valid is asserted. In order to ensure like rails across domains (Core VDD<>ECO VDD, Core VCS<>ECO VCS) are in sync during operational mode, this time value applies to all rails across the domains. This parameter allows for PFET Strength values to settle before PFET Strength Valid is sampled in the Uregs. The value set must the maximum delay for the worst rail timing and must allow for any metastability settling (for example, normally 2-3 cycles for single signals in an asynch handshake interface)
24:31	RW	IVRM_PFSTRVALID_PROP_DELAY: PFETStrength Valid Propagation Delay Time from ivrm_pfstr_prop_delay expiring to where PFET Strength Valid is deasserted. The value is the maximum of a) the minimum pulse width required for PFETStrength Valid and b) the propagation of PFETStrength Vald through (or enough of) the daisy chain. In order to ensure like rails across domains (Core VDD<>ECO VDD, Core VCS<>ECO VCS) are in sync during operational mode, this time value applies to all rails across the domains and thus must be the set to the value of the worst (slowest) rail. The minimum pulse width cannot be violated. The propagation delay can be tuned for more aggressive timing (for example, de-assert before the actual propagation is complete). Measured in prv_nclk cycles. The min delay is 2 cycles. Additional delay can be configured with the following settings 0x00 = No additional delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks
32:39	RW	IVRM_VPUMP_POWERON_TIME: iVRM (VRreg and UReg) - Vpump Power On Time Time necessary for the distributed internal VRM macro circuits to power on. Same delay is required for power on voltage pump circuit. Both delays are in the 8us range. In 100ns units as established by scan dial ivrm_100ns_value



Register Name	<i>POHR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_OCC_HEARTBEAT_REG
Address	000000001A0F0164 (PCB)
Attributes	
Description	Controls the behavior of the OCC heartbeat function.

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Register Name	PRCCR0 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG 0
Address	000000001A0F0165 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function.

Bits	PCB	Field Mnemonic: Description
0	ROX	RESCLK_DIS: Resonant Clock Enable Master enable of all resonant clocking functions. This dial can be set by setting GP3(22) and can not be set in this PCBS_resonant_Clock_Control_Reg0. 1 = Resonant Clock function is disabled. Default values (0) for resclk_value, resclk_core_sync_value, csb_eco_sync_value 0 = Resonant Clock Control hardware is enabled (the mode is defined by dial resclk_control_mode)
1	RW	RESCLK_CONTROL_MODE: Resonant Clock Control Mode Defines the control means enabled when resclk_dis is not set. 0 = Pstate band hardware mechanism enabled 1 = Manual mode enabled (Firmware mode) If this bit is set to 0, the hardware control mechanism that manages the transition across the Resonant Bands is enabled. If this bit is set to 1, the automatic Pstate band hardware mechanism is disabled and the Firmware is in control of all values of the dial resclk_value, resclk_core_sync_value, csb_eco_sync_value. Firmware must ensure that frequency changes will not cross resonant bands or machine failures may result. resclk_value represents the values for clock sector buffer strength, inductor switch strength and high inductor enable. Firmware must ensure the correct stepping in/out the different bands and propagation of the values (resclk_value) to the core/eco (resclk_core_sync_value / csb_eco_sync_value).
2:4	RW	RESCLK_SYNC_PW: Resonant Clock Sync Pulse Width Number of nest/4 cycles to assert the clock sync signal. This value must be high enough to ensure capture and propagation across the asynchronous chiplet boundary.
5:11	RW	RES_SYNC_DELAY_CNT: Resonant Clock Sync Delay Number of nest/4 cycles wait after the launch of the resclk_value (csb and inductor) before launching the sync to allow these to be captured. This value must be high enough to ensure full propagation to the input of the clock sector buffers and inductor switches.
12:26	RW	RES_CSB_STR_INSTR_LO: Resonant Clock Sector Buffer Strength Instruction - Low Band Mask value that determines whether, during a fixed 15 step sequence, the res_csb_str(0:3) is to be decremented/incremented in entering/exiting the Low Band. During resonant clock Entry, res_csb_str(0:3) decremented by the value pattern from 0 down to 14. During resonant clock Exit, res_csb_str(0:3) incremented by the value pattern from 14 up to 0.
27:41	RW	RES_CSB_STR_INSTR_HI: Resonant Clock Sector Buffer Strength Instruction - High Band Mask value that determines whether, during a fixed 15 step sequence, the res_csb_str(0:3) is to be decremented/incremented in entering/exiting the High Band. During resonant clock Entry, res_csb_str(0:3) decremented by the value pattern from 0 down to 14. During resonant clock Exit, res_csb_str(0:3) incremented by the value pattern from 14 up to 0.

Register Name	PRCCR1 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG 1
Address	000000001A0F0166 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function. Writes are conditioned.

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Bits	PCB	Field Mnemonic: Description
0:7	RW	FULL_CSB_PS: Full Clock Sector Buffer Pstate Pstate defining the maximum point where the clock sector buffer must be driven to full strength. This allow clocks to be distributed at low Vmin levels. FW needs to make sure that no overlaps occur with bands 2 or 3.
8:15	RW	RES_LOW_LOWER_PS: Low Frequency Resonant Lower (LFRLow) Pstate Pstate defining the lower frequency of the Low Resonant Frequency Band. FW needs to make sure that no overlap occurs with band 0.
16:23	RW	RES_LOW_UPPER_PS: Low Frequency Resonant Upper (LFRUpper) Pstate Pstate defining the upper frequency of the Low Resonant Frequency Band. Note that if an overlap occurs with band 3, the hardware behavior is undefined.
24:31	RW	RES_HIGH_LOWER_PS: High Frequency Resonant Lower (HFRLow) Pstate Pstate defining the lower frequency of the High Resonant Frequency Band. Note that if an overlap occurs with band 2, the hardware behavior is undefined.
32:39	RW	RES_HIGH_UPPER_PS: High Frequency Resonant Upper (LFRUpper) Pstate Pstate defining the upper frequency of the High Resonant Frequency Band. This value needs to be greater or equal to high_res_lower_ps.
40:43	RW	NONRES_CSB_VALUE_TI: Clock Sector Buffer Table Index for non-resonant state Table Index into Clock Sector Buffer Table for the nominal, non-resonant state.
44:47	RW	FULL_CSB_VALUE_TI: Clock Sector Buffer Table Index for full CSB value Table Index into Clock Sector Buffer Table for the full CSB strength value.
48:56	RWX	RESCLK_VALUE: Output register driving the 9 bit resclk_value In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current resclk_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. The value in this register represents the following concatenation: csb_str_value(0:3) sw_str(0:3) hi_induct_en.
57	RWX	RESCLK_CORE_SYNC_VALUE: Output register driving the resclk_core_sync signal In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current resclk_core_sync_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. This bit is supposed to be used in order to create a SCOM-controlled pulse to force an update of the resclk propagation registers. A 1 enables the synchronous update, a 0 disables it. Suggested use of this bit is to set it to 1 and then set it back to 0 to create a (long) update pulse.
58	RWX	CSB_ECO_SYNC_VALUE: Output register driving the csb_eco_sync signal In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current csb_eco_sync_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. This bit is supposed to be used in order enable the ECO domain to participate in clock sector buffer strength changes, when switching from nominal strength to full CSB strength. A 1 enables the ECO domain, a 0 disables it from seeing a CSB strength update.

Register Name	<i>PRCCR1 Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_STATUS_REG
Address	000000001A0F0167 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function.

Bits	PCB	Field Mnemonic: Description
0	ROX	RESCLK_STATE: Resonant Clock State 0 = Resonant Clocking inactive 1 = Resonant Clocking active Valid if resclk_inprogress = 0. Hardware sets this bit to the right value at the completion of the transition into and out of resonance mode.
1	ROX	RES_HI_INDUCT_EN: Resonant High Inductor Enable Valid if resclk_inprogress = 0. This dial provides the current value being propagated. 0 = Resonant Clock mode not active 1 = Resonant Clock mode active
2	ROX	RESCLK_INPROGRESS: Resonant Clock Transition in Progress This bit is set by hardware while a transition is in progress and will be reset by hardware when the operation is complete.
3	ROX	RESCLK_FULL_CSB: Full CSB Clock State 0 = Full CSB Clocking inactive 1 = Full CSB Clocking active Valid if resclk_inprogress = 0. Hardware sets this bit to the right value at the completion of the transition into and out of full CSB mode respectively.

Register Name	<i>PLPFTCR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_CONTROL_REG
Address	000000001A0F0168 (PCB)
Attributes	
Description	Allows firmware to configure the modes that are used for the PCBS Local Pstate Frequency Target Status Register.

Bits	PCB	Field Mnemonic: Description
0:2	RW	DELAY_TIME: This field encodes the delay between the time a Local Actual Pstate change modifies the input to the DPLL and the time frequency acquisition begins to allow the hardware to ignore the frequency transition of the DPLL in order to get better frequency measurements. This field encodes a delay of ~1us to ~128us in power of 2 selects. The delay is defined by 2**delay_time in us. Note that the hardware uses multiples of the slow hang pulse that is running at 1us.
3	RW	RECORD_TRANSITIONS: This bit indicates whether the LPFTSR records events that correspond to Local Actual Pstate changes (and therefore may include DPLL slewing effects.) One usage model would set the periodic sample_time defined by the dial OHA_MODE_REG[tod_pulse_count_match_val] to a time less than the worst-case DPLL slew time but then ignore Pstate transitions because they might include DPLL slew effects.

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Bits	PCB	Field Mnemonic: Description
4:18	RW	MULTIPLIER: This 15-bit unsigned constant is multiplied by the DPLL frequency code (9 bits) implied by the Local Actual Pstate to yield the 24-bit frequency target measured in PCBS-PM clock cycles (core clock / 2). Assuming times in seconds and frequencies in Hz, firmware should set this constant to: (DPLL_Frequency_Code_Step_Hz * Sample_Time_Seconds) / 2
19	RW	ENABLE_LPFT_FUNCTION: This is the enable bit to enable the local Pstate frequency target function. A '1' enables the function, a '0' disables it (the value can be changed at any time).

Register Name	PLPFTSR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_STATUS_REG
Address	000000001A0F0169 (PCB)
Attributes	
Description	Allows firmware to observe local actual Pstate realized frequencies.

Bits	PCB	Field Mnemonic: Description
0	ROX_CLRPART	VALID: If this bit is set then all of the remaining fields of this register are valid. This bit is cleared whenever the register is read or after a local actual Pstate change occurs, and is will be set whenever the hardware completes a valid sample. If firmware reads this register and the valid bit is not set, then it indicates that the Local Pstate target frequency acquisition logic has not been able to complete a frequency acquisition for any Local Actual Pstate change since the last time the LPFTSR was read. This could be due to either of the following factors: 1. Firmware is sampling the LPFTSR faster than the time implied by the sample time defined in OHA by the dial OHA_MODE_REG[tod_pulse_count_match_val] field
1	ROX	CPM_DPLL: If the valid bit is set, then if cpm_dpll is set it indicates that the event recorded by this register was due to a Local Actual Pstate implemented by the DPLL running in CPM-DPLL mode, otherwise the value of this bit is undefined. If the valid bit is not set, this bit is undefined.
2	ROX	IVRM: If the valid bit is set, then if ivrm is set it indicates that the event recorded by this register was due to a Local Actual Pstate whose voltage was set locally by the iVRM operating entirely in regulation mode. If the valid bit is not set, this bit is undefined.
3	ROX	TRANSITION: If the valid bit is set, then if transition is set it indicates that during the observation period a Local Pstate Actual change has occurred, and any performance delta may be due to DPLL frequency slewing. If the valid bit is not set, this bit is undefined
4	ROX	STABLE: If stable is set it indicates that the DPLL input frequency has been stable since the last time the PLPFTSR was read. This bit is set whenever the PLPFTSR is read, and cleared whenever the Fmax input of the DPLL changes. This bit is always valid, regardless of the state of the valid bit. If the PLPFTSR is read on the same cycle a frequency changes then the stable bit is cleared. This bit helps firmware better understand how to interpret the information contained in the PLPFTSR. (Note that this bit should have an attribute ROX_SETPART, but this is not supported by regchk.)
5:28	ROX	DELTA: If the valid bit is set then this is the 24-bit signed difference Measured Cycles - Target Cycles for the event captured by this register. If the valid bit is not set, this dial is undefined.
29:52	ROX	CUMULATIVE: This field records the 24-bit cumulative (signed) delta for all valid samples taken since this field was cleared. Writing any value to this register clears this field. Note that it should have an attribute WOX_CLRPART, but this is not supported by regchk/figtree.

Bits	PCB	Field Mnemonic: Description
53:60	ROX	PSTATE: If the valid bit is set then this is the Local Actual Pstate of the frequency acquisition that had the minimum (signed) delta of any valid sample taken since the last time the LPFTSR was read. If the valid bit is not set, then this field is undefined.

Register Name	<i>PFSMM1/2 Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR1_REG
Address	000000001A0F0170 (PCB)
Attributes	
Description	Facilitates debug by providing insight into the internal FSM states of the PCB-slave power-management unit. For expert use only. Coding according to VHDL design.

Bits	PCB	Field Mnemonic: Description
0:6	ROX	BABYSTEP_MAIN_FSM: Main Babystep FSM (mfsm_lt)
7:11	ROX	BABYSTEP_SLAVE_FSM: Babystep Slave FSM (sfsm_lt)
12:16	ROX	CORE_RAILSTEPPER_MAIN_FSM: Main Core Railstepper FSM (mrsfsm_lt)
17:21	ROX	ECO_RAILSTEPPER_MAIN_FSM: Main ECO Railstepper FSM (mrsfsm_lt)
22:25	ROX	CORE_RAILSTEPPER_SUB_FSM: Core Railstepper Sub-FSM (srsfsm_lt)
26:29	ROX	ECO_RAILSTEPPER_SUB_FSM: ECO Railstepper Sub-FSM (srsfsm_lt)
30:34	ROX	CORE_RAILSTEPPER_BYP_FSM: Core Railstepper Bypass FSM (byp_fsm_lt)
35:39	ROX	ECO_RAILSTEPPER_BYP_FSM: ECO Railstepper Bypass FSM (byp_fsm_lt)
40:45	ROX	IVRM_CORE_VDD_SEQUENCER_FSM: Core iVRM Sequencer for Vdd (ivrm_fsm_lt)
46:51	ROX	IVRM_CORE_VCS_SEQUENCER_FSM: Core iVRM Sequencer for Vcs (ivrm_fsm_lt)
52:57	ROX	IVRM_ECO_VDD_SEQUENCER_FSM: ECO iVRM Sequencer for Vdd (ivrm_fsm_lt)
58:63	ROX	IVRM_ECO_VCS_SEQUENCER_FSM: ECO iVRM Sequencer for Vcs (ivrm_fsm_lt)

Register Name	<i>Refer To The Description Of PFSMM1.</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR2_REG
Address	000000001A0F0171 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:6	ROX	RESCLK_BAND_FSM: Band Sequencer for resonant clocking (band_fsm_lt)
7:10	ROX	RESCLK_LOWRES_FSM: Low Resonant Clocking sequencer (lowres_fsm_lt)
11:14	ROX	RESCLK_HIGHRES_FSM: High Resonant Clocking sequencer (highres_fsm_lt)
15:18	ROX	RESCLK_FULLCSB_FSM: Full-CSB Resonant Clocking sequencer (fullcsb_fsm_lt)
19:22	ROX	RESCLK_UPDATE_FSM: Resonant Clocking Update sequencer (update_fsm_lt)

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Bits	PCB	Field Mnemonic: Description
23:29	ROX	IDLE_TRANSITION_FSM: Idle State Sequence FSM (ifsm_lt)
30:37	ROX	Peco_step_target_uv Current ECO Step Target Pstate (different from Plocal_actual for undervolting)
38:45	ROX	Pcore_step_target_uv Current core Step Target Pstate (different from Plocal_actual for sleep and undervolting)

Register Name	<i>Protect Mode Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.PROTECT_MODE_REG
Address	000000001A0F03FE (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	READ_PROTECT_ENABLE: Enable read protection
1	RW	WRITE_PROTECT_ENABLE: Enable write protection

Register Name	<i>Atomic Lock Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX10.TP_PCB_SLAVE_INST.ATOMIC_LOCK_REG
Address	000000001A0F03FF (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	ATOMIC_LOCK_ENABLE: Enable atomic lock
1:4	ROX	ATOMIC_ID: Atomic ID

Register Name	<i>Contains The Slave's Primary Address</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.PRIMARY_ADDRESS_REG
Address	000000001B0F0000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RO	Reserved field (Access type is primary_address)



Register Name	<i>Multicast Group 1</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.MULTICAST_GROUP_1	
Address	000000001B0F0001 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST1_GROUP: multicast group1 setting

Register Name	<i>Multicast Group 2</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.MULTICAST_GROUP_2	
Address	000000001B0F0002 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST2_GROUP: multicast group2 setting

Register Name	<i>Multicast Group 3</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.MULTICAST_GROUP_3	
Address	000000001B0F0003 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST3_GROUP: multicast group3 setting

Register Name	<i>Multicast Group 4</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.MULTICAST_GROUP_4	
Address	000000001B0F0004 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST4_GROUP: multicast group4 setting

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Register Name	<i>Timeout Select Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.TIMEOUT_REG
Address	000000001B0F0010 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	Reserved field (Access type is int_timeout)

Register Name	<i>Assist Interrupt Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.ASSIST_INTERRUPT_REG
Address	000000001B0F0011 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is attn)
1	ROX	Reserved field (Access type is recov)
2	ROX	Reserved field (Access type is xstop)

Register Name	<i>GP3 Register (NA In PERV CPLT)</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.GP3_REG
Address	000000001B0F0012 (PCB) 000000001B0F0013 (PCB1) 000000001B0F0014 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset
2	RWX	RWX_WAND	RWX_WOR	GLSMUX_RESET: Glsmux reset for test purpose and stuck active mesh protection. Notice no clocks in the EX if this bit is set.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Put the DPLL in test mode.
4	RWX	RWX_WAND	RWX_WOR	PLL_RST: Put PLL in reset state.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYP: Enable PLL bypass.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pcb_access)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	PM_PI_DECODE: Test override for power management. EX chiplet only.
22	RWX	RWX_WAND	RWX_WOR	RESCLK_DIS: Resonant clocking disable.
23:25	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave will report 'Chiplet Offline'.
27	RWX	RWX_WAND	RWX_WOR	TP_LVLTRANS_FENCE: Electrical winkel fence. Mainly used by power management.
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.
29:31	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)

Register Name		<i>Skew Adjust Data</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.CLK_ADJ_REG
Address		000000001B0F0015 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:15	ROX	

Register Name		<i>Clk Ajust Config</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.CLK_ADJ_SET
Address		000000001B0F0016 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:31	RW	CLK_ADJ_SET_REG: Clk adj config

Register Name		<i>Vital Scan Out</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.VITAL_SCAN_OUT
Address		000000001B0F0017 (PCB)
Attributes		
Description		

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Bits	PCB	Field Mnemonic: Description
0	ROX	

Register Name	<i>Chiplet Heartbeat Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.HEARTBEAT_REG
Address	000000001B0F0018 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	HEARTBEAT_DEAD: Chiplet heartbeat not detected

Register Name	<i>Lock Indications From PLLs</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.PLL_LOCK_REG
Address	000000001B0F0019 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	ROX	Reserved field (Access type is lock)

Register Name	<i>Attn Interrupt</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.ATTN_INTERRUPT_REG
Address	000000001B0F001A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is attn)

Register Name	<i>Recov Interrupt</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.RECOV_INTERRUPT_REG
Address	000000001B0F001B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is recov)



Register Name	<i>Xstop Interrupt</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.XSTOP_INTERRUPT_REG
Address	000000001B0F001C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is xstop)

Register Name	<i>Slave Config Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.SLAVE_CONFIG_REG
Address	000000001B0F001E (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	CFG_DISABLE_PERV_THOLD_CHECK: Disable pervasive thold check
1	RW	CFG_DISABLE_MALF_PULSE_GEN: Disable pulse generation for malf alert. Switch back to level
2	RW	CFG_STOP_HANG_CNT_SYS_XSTP: Disable hang counter stop for system xstop
3	RW	CFG_DISABLE_CL_ATOMIC_LOCK: Disable atomic lock for chiplet accesses
4	RW	CFG_DISABLE_HEARTBEAT: Disable check for voltage and gridclock in the chiplet
5	RW	CFG_ZERO_DATA: Sent zero data on any error
6:7	RW	
8:12	RW	ERROR_MASK: mask bits for slave error reporting
13:15	RW	

Register Name	<i>Error Capture Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.ERROR_REG
Address	000000001B0F001F (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX_WCLEAR	CE_ERROR: Correctable error on pcb bus
1:3	RWX_WCLEAR	CHIPLET_ERRORS: Errors reported by chiplet 000 = no error 001 = XSCOM command blocked due pending errors 010 chiplet offline 011 partial good 100 invalid address / address error / bad access type 101 clock error 110 parity error / received unexpected packet / wrong packet number 111 timeout This register is for debug purposes only. It only holds meaningful data if it is cleared after each error.
4	RWX_WCLEAR	PARITY_ERROR: Parity error on PCB Interface

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Bits	PCB	Field Mnemonic: Description
5	RWX_WCLEAR	DATA_BUFFER_ERROR: Parity error in data buffer
6	RWX_WCLEAR	ADDR_BUFFER_ERROR: Parity error in address buffer
7	RWX_WCLEAR	PCB_FSM_ERROR: Invalid state error in PCB FSM
8	RWX_WCLEAR	CL_FSM_ERROR: Invalid state error in Chiplet FSM
9	RWX_WCLEAR	INT_RX_FSM_ERROR: Invalid state error in interrupt RX FSM
10	RWX_WCLEAR	INT_TX_FSM_ERROR: Invalid state error in interrupt TX FSM
11	RWX_WCLEAR	INT_TYPE_ERROR: Invalid interrupt type
12	RWX_WCLEAR	CL_DATA_ERROR: Parity error on Chiplet Interface
13	RWX_WCLEAR	INFO_ERROR: Parity error on Chiplet info lines
14	RWX_WCLEAR	UNUSED_0:
15	RWX_WCLEAR	CHIPLET_ATOMIC_LOCK_ERROR: Chiplet atomic lock error
16	RWX_WCLEAR	PCB_INTERFACE_ERROR: Error of pcb interface component for the internal endpoint
17	RWX_WCLEAR	CHIPLET_OFFLINE: Heartbeat check indicated that chiplet is offline
18	RWX_WCLEAR	CHIPLET_GRID_SKITTER: Heartbeat check indicated skitter on the chiplet grid
19	RWX_WCLEAR	GP3_REG_PARITY_ERROR: gp3 register parity bad
20	RWX_WCLEAR	ADDRESS_REG_PARITY_ERROR: address register parity bad
21	RWX_WCLEAR	TIMEOUT_REG_PARITY_ERROR: timeout select register parity bad
22	RWX_WCLEAR	CONFIG_REG_PARITY_ERROR: slave config register parity bad
23	RWX_WCLEAR	CLK_ADJ_REG_PARITY_ERROR: clk adj register parity bad
24	RWX_WCLEAR	DIV_REG_PARITY_ERROR: div register parity bad
25:28	RWX_WCLEAR	PLL_UNLOCK_ERROR: unlock from chiplet pll



Register Name	<i>Hang Pulse Generation Register 0</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.HANG_PULSE_0_REG
Address	000000001B0F0020 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_0: Value of hang pulse 0. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_0: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 1</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.HANG_PULSE_1_REG
Address	000000001B0F0021 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_1: Value of hang pulse 1. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_1: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 2</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.HANG_PULSE_2_REG
Address	000000001B0F0022 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_2: Value of hang pulse 2. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_2: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 3</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.HANG_PULSE_3_REG
Address	000000001B0F0023 (PCB)
Attributes	
Description	

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Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_3: Value of hang pulse 3. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_3: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 4</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.HANG_PULSE_4_REG
Address	000000001B0F0024 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_4: Value of hang pulse 4. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_4: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 5</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.HANG_PULSE_5_REG
Address	000000001B0F0025 (PCB)
Attributes	
Description	This hang counter is used exclusively to generate the malfunction alert pulse.

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_5: Value of hang pulse 5. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_5: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 6</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.HANG_PULSE_6_REG
Address	000000001B0F0026 (PCB)
Attributes	
Description	This hang counter is exclusively used for heartbeat generation.

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_6: Value of hang pulse 6. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_6: If set to '1', hang pulses are suppressed in case of a xstop



Register Name	<i>Divider For Hang Counter Clock</i>		
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.PRE_COUNTER_REG		
Address	000000001B0F0028 (PCB)		
Attributes			
Description			

Bits	PCB	Field Mnemonic: Description
0:7	RW	PRE_COUNTER: Divider for hang counter clock. Divides clock by n+1 (default: n=0)

Register Name	<i>PowerManagement GP0</i>		
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PMGPO_REG		
Address	000000001B0F0100 (PCB) 000000001B0F0101 (PCB1) 000000001B0F0102 (PCB2)		
Attributes			
Description			

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PM_DISABLE: Master Switch for the PowerManagement Macro
1	RWX	WOX_AND	WOX_OR	PMGP0_SPARE_BIT1: spare bit
2	RWX	WOX_AND	WOX_OR	TP_TC_RESTART_CORE_DOMAIN: Kicks off small sequencer in OHA to get chiplet clocks back running for fast sleep without involving PORE. From GP-reg and overridden by PowMan State Machine.
3	RWX	WOX_AND	WOX_OR	DPLL_THOLD: Thold for the DPLL clock domain in the chiplet
4	RWX	WOX_AND	WOX_OR	PERV_THOLD: Thold for the Pervasive clock domain in the chiplet
5	RO	RO	RO	Reserved.
6	RO	RO	RO	Reserved.
7	RWX	WOX_AND	WOX_OR	PM_DPLL_TIMER_ENA: Select a timer instead of the DPLL lock bit for criteria to switch to DPLL. The time is defined by thold_timer_sel.
8	RWX	WOX_AND	WOX_OR	DPLL_LOCK_SENSE: DPLL lock sensitivity control (0=faster lock time, 1=slower lock time)
9	RWX	WOX_AND	WOX_OR	PMGP0_SPARE2: spare bit
10	RWX	WOX_AND	WOX_OR	DPLL_RESET: Reset to DPLL
11	RWX	WOX_AND	WOX_OR	PMGP0_SPARE_BIT11: Spare bit
12:19	RWX	WOX_AND	WOX_OR	DPLL_TESTOUT_CTL: DPLL testout control
20	RWX	WOX_AND	WOX_OR	TP_TC_CACHE2CORE_FENCE: Fence from cache to core domain in EX chiplet
21	RWX	WOX_AND	WOX_OR	TP_TC_CORE2CACHE_FENCE: Fence from core to cache domain in EX chiplet
22	RWX	WOX_AND	WOX_OR	TP_TC_PERVASIVE_ECO_FENCE: Pervasive ECO fence
23	RWX	WOX_AND	WOX_OR	CHKSW_HW257424_DISABLE: Chicken switch for interrupt retry exhausted bug (0=fix enabled, 1=fix disabled)

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
24:26	RWX	WOX_AND	WOX_OR	TP_CLK_ASYNC_RESET_DC: Clk async reset for three glitchless muxes, and the two clock dividers (bit 0 = master GLM, bit 1 = ECO Div2 and ECO GLM, bit 2= core Div1 and core GLM)
27:29	RWX	WOX_AND	WOX_OR	TP_CLKGLM_SEL_DC: Glitchless Mux Select for primary chiplet clock source (feeding both core and eco clock muxes) 000 = refclk, 001 = DPLL. 100 = Use constant selected by bit 34, else refclk
30	RWX	WOX_AND	WOX_OR	TP_CLKGLM_ECO_SEL_DC: Glitchless Mux Select for eco domain (cache_nclk) grid. 0= follow primary source chosen by previous field: 1 = Use constant selected by bit 34
31	ROX	NC	NC	SPECIAL_WKUP_DONE: Indicates that special wakeup is done, if asserted
32:33	RWX	WOX_AND	WOX_OR	TP_CLKGLM_CORE_SEL_DC: Glitchless Mux Select for core domain (nclk grid) mux. 0b00=primary GLS mux output, 0b10=constant input, 0b01=refclk. Valid transitions are 0b01 <-> 0b00 <-> 0b10, 0b11 is illegal
34	RWX	WOX_AND	WOX_OR	TP_CLKGLM_CONST_DC: Constant input available to all three ClkGlm
35:36	RWX	WOX_AND	WOX_OR	THOLD_TIMER_SEL: Selection for the thold transition timer in the IDLE state machine. 0b00=1024 cycles delay, 0b01=512 cycles delay, 0b10=256 cycles delay, 0b11= 128 cycles delay
37	RWX	WOX_AND	WOX_OR	BLOCK_ALL_WAKEUP_SOURCES: Setting this bit will make the PM Slave ignore any Wakeup events (ext. interrupt, malfunction alert, any special wakeup bit). This bit is intended to enable firmware concurrent patch capability. Note: This does NOT block the interrupt from being presented to the processor core. The following procedure is required on changes: 1. Firmware may only set this bit after first setting special wakeup and polling for special wakeup complete (OHA and PCB-slave both in running state with AISS and PM FSMs idle). 2. Firmware may only clear this bit if all special wakeup bits are first cleared.
38	RWX	WOX_AND	WOX_OR	TP_TC_DPLL_TESTMODE_DC: ADPLL test mode
39	RWX	WOX_AND	WOX_OR	PM_SLV_WINKLE_FENCE: Fence off the powered off chiplet in winkle. - Logical fence/hold for pcb_slave and pcb_slave_pm. For electrical fence see bit 23.
40	RWX	WOX_AND	WOX_OR	L3_ENABLE_SWITCH: Setting this bit activates l3_edram_enable if allowed by system configuration GP3(28). Resetting this bit deactivates l3_edram_enable.
41	RWX	WOX_AND	WOX_OR	TP_CPLT_IVRM_REFBYPASS_DC: Signal to iVRM (used to be controlled by scan-only block inside EX, but needs to be driven by VIO domain)
42	RWX	WOX_AND	WOX_OR	CHKSW_HW241939_DISABLE: if this bit is set to 1, the fix for HW241939 (pfet enable SCOM-ability) is disabled
43	RWX	WOX_AND	WOX_OR	CHKSW_HW273115_DISABLE: if this bit is set to 1, the fix for HW273115 (Pga ACK noack issue when the babystepper is in the winkle state) is disabled
44	RWX	WOX_AND	WOX_OR	CHKSW_HW245103_DISABLE: if this bit is set to 1, the fix for HW245103 resonant clocking CSB and SW -bit ordering change is disabled
45	RWX	WOX_AND	WOX_OR	CHKSW_HW257534_DISABLE: if this bit is set to 1, the fix for HW257534 (fencing of errors) is disabled
46	RWX	WOX_AND	WOX_OR	CHKSW_HW259509_ENABLE: if this bit is set to 0, the fix for HW259509 (Pstate change hanging, because of DPLL flock timer in a hung state) is disabled
47	RWX	WOX_AND	WOX_OR	CHKSW_HW260345_DISABLE: if set to 1, this bit disables the HW260345 fix (fix was to make sure that we enter bypass mode for iVRM safe mode without a glitch that could cause Vcs in regulation and Vdd in bypass)

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
48:49	ROX	NC	NC	WAKEUP_INT_TYPE: (Known to be unreliable and not supported, informational usage only) Type of the last wakeup event that caused an exit from sleep or winkle (excluding nap!), regardless of present state. 0b01: External interrupt. 0b10: Malfuction Alert. 0b11: Special Wakeup. 0b00: chiplet has never fully entered and exited a chiplet-level idle state since IPL of the system. (Note this does not necessarily get updated when the processor core enters an idle state, only if the PCB-Slave enters and then exits the idle state for this chiplet).
50	ROX	NC	NC	DPLL_LOCK: DPLL lock indicator
51	ROX	NC	NC	SPECIAL_WKUP_ALL_SOURCES_ORED: logical OR of all special wakeup sources
52	ROX	NC	NC	REGULAR_WKUP_AVAILABLE: logical OR of external interrupt and malfuction alert
53	RWX	WOX_AND	WOX_OR	BLOCK_REG_WKUP_SOURCES: blocks ext. int. and malf. Alert from waking up PCBS (no block possible for PC!)

Register Name	<i>PowerManagement GP1</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PMGP1_REG
Address	000000001B0F0103 (PCB) 000000001B0F0104 (PCB1) 000000001B0F0105 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	SLEEP_POWER_DOWN_EN: Sleep Power Down Enable: When set to 1, causes hardware to automatically reduce voltage to the Core domain when entering Sleep mode. The voltage value for power down is chosen by sleep_power_off_sel (bit 2). When set to 0, a request is sent to the PORE engine for assistance entering Sleep.
1	RWX	WOX_AND	WOX_OR	SLEEP_POWER_UP_EN: Sleep Power Up Enable: When set to 1, enables automated hardware restoration of voltage via PFETs and, if enabled, iVRMs when exiting Sleep mode. If this bit is set to 0 the hardware rely on external means (PORE or equivalent) to restore voltage.
2	RWX	WOX_AND	WOX_OR	SLEEP_POWER_OFF_SEL: Sleep Power Off Select: Selects which voltage level to place the Core domain PFETs upon Sleep entry. 0 = Vret (Fast Sleep Mode), 1 = Voff (Deep Sleep Mode). Depending on the setting of pmicr_latency_en, this bit is controlled with a PCB-write (0) or by the PMICR in the core (1).
3	RWX	WOX_AND	WOX_OR	WINKLE_POWER_DOWN_EN: Winkle Power Down Enable: When set to 1, causes hardware to automatically reduce voltage to the entire Chiplet (both Core and ECO Domains) when entering Winkle mode. The voltage value for power down is chosen by winkle_power_off_sel (bit 5). When set to 0, a request is sent to the PORE engine for assistance entering Winkle.
4	RWX	WOX_AND	WOX_OR	WINKLE_POWER_UP_EN: Winkle Power Up Enable: When set to 1, enables automated hardware PFET enablement when exiting Winkle mode. If this bit is set to 0 the hardware rely on external means (PORE or equivalent) to cause the PFETs to be re-enabled.

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
5	RWX	WOX_AND	WOX_OR	WINKLE_POWER_OFF_SEL: Winkle Power Off Select: Selects which voltage level to place the Core and ECO domain PFETs upon Winkle entry. 0 = Vret (Fast Winkle Mode), 1 = Voff (Deep Winkle Mode). Depending on the setting of pmicr_latency_en, this bit is controlled with a PCB-write (0) or by the PMICR in the core (1).
6	RWX	WOX_AND	WOX_OR	OHA_WKUP_OVERRIDE_EN: Needs to be 0 for normal operation. If set to 1, the two following dials are used to override the regular and special wakeup signal from PCBS to OHA
7	RWX	WOX_AND	WOX_OR	OHA_PM_WKUP_OVERRIDE: Enablement by 'oha_wkup_override_en' forces the regular wakeup signal to OHA to the value of this bit regardless of presence of an interrupt source.
8	RWX	WOX_AND	WOX_OR	OHA_SPC_WKUP_OVERRIDE: Enablement by 'oha_wkup_override_en' forces the special wakeup signal to OHA to the value of this bit, regardless of the firmware settings.
9	RWX	WOX_AND	WOX_OR	ENDP_RESET_PM_ONLY: If asserted, an endpoint reset of all power management-related functions (not the regular PCB slave) is performed. Intended usage is for recovery.
10	RWX	WOX_AND	WOX_OR	DPLL_FREQ_OVERRIDE_ENABLE: override Fmax/Fmin only, if '1', using register FREQ_CTRL_REG
11	RWX	WOX_AND	WOX_OR	PM_SPR_OVERRIDE_EN: PM SPR Override Enable The PPMCR (0xNNNN) and PPMICR (0XXXXX) accesses the register resources that make up the PMCR SPR used by hypervisor to management Pstates. Thus, PCB updates to it are disabled in hardware to prevent collisions. This bit allows ownership of the PMCR to be switched from hypervisor to OCC. This switch is immediate in hardware, thus, firmware must ensure the ownership switch is otherwise communicated. 0 = Disables the writing of the PPMCR (0xNNNN) from the PCB and allows SPR 884 writes (mtspr) to update the register resource. 1 = Enables the writing of the PPMCR (0xNNNN) from the PCB.
12	RWX	WOX_AND	WOX_OR	FORCE_SAFE_MODE: Force Safe Mode 0 = Allow other enabled features to determine the operational Pstate. 1 = Forces the minimum of POHBR[psafe] and PPMCR[global_pstate_actual] Pstate for the core chiplet as the operational frequency.
13	RWX	WOX_AND	WOX_OR	IVRM_SAFE_MODE_EN: Internal VRM Safe Mode Enable 0 = Disable the iVRM safe mode, thus, no automatic actions occur, if an iVRM error happens. 1 = if the iVRMs are enabled (PIVRMCSR[ivrn_en] is set) and Pstates are enabled and if the error defined by dial pcbs_ivrm_gross_or_fine_err occurs, then the railstepper is forced into bypass mode to prevent a voltage-frequency hazard
14	RWX	WOX_AND	WOX_OR	IVRM_SAFE_MODE_FORCE_ACTIVE: Internal VRM Safe Mode Force Dial 0 = the hardware decides whether to activate the iVRM safe mode or not 1 = the iVRM safe mode is forced regardless (this makes only sense if ivrm_fsm_enable=1 and Pstates are enabled)
15	RWX	WOX_AND	WOX_OR	PMICR_LATENCY_EN: Selects how the sleep/winkle latency (which is deep/fast) is controlled. If asserted the PMICR controls the winkle/sleep_power_off_sel in PMGP1, otherwise those bits are controlled via SCOM by OCC.
16	RWX	WOX_AND	WOX_OR	ENABLE_OCC_CTRL_FOR_LOCAL_PSTATE_EFF_REQ: controls, if the HW (for value 0) or OCC (value 1) is in control of the Local Pstate Effective register in PPSTR

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
17	RWX	WOX_AND	WOX_OR	SERIALIZE_PFET_POWERDOWN: if asserted, the pFET sequencer will sequence the core and the ECO domain one after the other when powering down
18	RWX	WOX_AND	WOX_OR	SERIALIZE_PFET_POWERUP: if asserted, the pFET sequencer will sequence the ECO and the core domain one after the other when powering up
19	RWX	WOX_AND	WOX_OR	DISABLE_FORCE_DEEP_TO_FAST_SLEEP: 0: (normal operation) - If PCB Slave reports a recoverable error or a checkstop, a DEEP sleep operation is forced to FAST. The entries in sleep/winkle_power_off_sel remain unchanged. 1: force to FAST is disabled.
20	RWX	WOX_AND	WOX_OR	DISABLE_FORCE_DEEP_TO_FAST_WINKLE: 0: (normal operation) - If PCB Slave reports a recoverable error or a checkstop, a DEEP winkle operation is forced to FAST. The entries in sleep/winkle_power_off_sel remain unchanged. 1: force to FAST is disabled.

Register Name	<i>PFET Control/Status Register For Core And ECO Vdd</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PFVDDCNTLSTAT_REG
Address	000000001B0F0106 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	CORE_VDD_PFET_FORCE_STATE: Core Domain PFET Force State Provides a means for firmware to force the core domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 4:5 = 00 (both core_vdd_pfet_val_override AND core_vdd_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
2:3	RW	ECO_VDD_PFET_FORCE_STATE: ECO Domain PFET Force State Provides a means for firmware to force the ECO domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 6:7 = 00 (both eco_vdd_pfet_val_override AND eco_vdd_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
4	RW	CORE_VDD_PFET_VAL_OVERRIDE: Core Domain PFET Value Override 0 = Override is disabled
5	RW	CORE_VDD_PFET_SEL_OVERRIDE: Core Domain PFET Stage Select Override 0 = Override is disabled
6	RW	ECO_VDD_PFET_VAL_OVERRIDE: ECO Domain PFET Value Override 0 = Override is disabled
7	RW	ECO_VDD_PFET_SEL_OVERRIDE: ECO Domain PFET Stage Select Override 0 = Override is disabled

Registers Specification

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Bits	PCB	Field Mnemonic: Description
8	RW	CORE_VDD_PFET_ENABLE_REGULATION_FINGER: Core Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the core_vdd_pfet_enable_value.
9	RW	ECO_VDD_PFET_ENABLE_REGULATION_FINGER: ECO Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the eco_vdd_pfet_enable_value.
10:21	RW	CORE_VDD_PFET_ENABLE_VALUE: Core PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the Core Domain PFET Enables directly. If core_vdd_pfet_val_override = 1, a write to this field sets the state of the core PFET Enables until core_vdd_pfet_val_override is cleared. If core_vdd_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the core_vdd_pfet_valN_slac registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
22:25	RW	CORE_VDD_PFET_SEL_VALUE: Core PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure core_vdd_pfet_valN_slac(0:11) where N is 0 to 11 if core_vdd_pfet_sel_override = 1. If core_vdd_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
26:37	RW	ECO_VDD_PFET_ENABLE_VALUE: ECO PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the ECO PFET Enables directly. If ECO_vdd_pfet_val_override = 1, a write to this field sets the state of the ECO PFET Enables until ECO_vdd_pfet_val_override is cleared. If eco_vdd_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the eco_vdd_pfet_valN_slac registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
38:41	RW	ECO_VDD_PFET_SEL_VALUE: ECO PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure eco_vdd_pfet_valN_slac(0:11) where N is 0 to 11 if eco_vdd_pfet_sel_override = 1. If eco_vdd_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
42:45	ROX	CORE_VDD_PG_STATE: Core power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
46:49	ROX	CORE_VDD_PG_SEL: For debug, contains the actual index n into Core Domain PFET Value [n] SLAT Register set that contains the Core PFET Enable Value currently enabled.
50:53	ROX	ECO_VDD_PG_STATE: ECO Domain power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
54:57	ROX	ECO_VDD_PG_SEL: For debug, contains the actual index n into ECO Domain PFET Value [n] SLAT Register set that contains the ECO PFET Enable Value currently enabled.



Register Name	<i>PFET Sense Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PFSENSE_REG
Address	000000001B0F0107 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:11	ROX	TP_CORE_VDD_PFET_ENABLE_SENSE: Not used any more.
12:23	ROX	TP_ECO_VDD_PFET_ENABLE_SENSE: Not used any more.
24:35	ROX	TP_CORE_VCS_PFET_ENABLE_SENSE: Not used any more.
36:47	ROX	TP_ECO_VCS_PFET_ENABLE_SENSE: Not used any more.

Register Name	<i>PM Error Summary Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PMERRSUM_REG
Address	000000001B0F0108 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	PM_ERROR: PM Error is present. Intended for use by special PCB multicast to see error state of all chiplets with a single read (via 510F0108 to read all chiplets)

Register Name	<i>PM Error Register:</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PMERR_REG
Address	000000001B0F0109 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_HANG_ERR: Hang during Unassisted Sleep Entry: SLEEP_ENTRY_NOTIFY_PMC state
1	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ASSIST_HANG_ERR: Hang during Assisted Sleep Entry: SLEEP_ENTRY_NOTIFY_PMC_ASSIST state
2	ROX	PCBS_SLEEP_EXIT_INVOKE_PORE_ERR: Hang during Unassisted Sleep Exit: SLEEP_EXIT_NOTIFY_PMC state
3	ROX	PCBS_SLEEP_EXIT_INVOKE_PORE_ERR: Hang during Assisted Deep Sleep Exit: SLEEP_EXIT_INVOKE_PORE state
4	ROX	PCBS_WINKLE_ENTRY_NOTIFY_PMC_ERR: Hang during Unassisted Winkle Entry: WINKLE_ENTRY_NOTIFY_PMC state
5	ROX	PCBS_WINKLE_ENTRY_SEND_INT_ASSIST_ERR: Hang during Assisted Winkle Entry: WINKLE_ENTRY_SEND_INT_ASSIST state
6	ROX	PCBS_WINKLE_EXIT_NOTIFY_PMC_ERR: Hang during Unassisted Winkle Exit: WINKLE_EXIT_NOTIFY_PMC state

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Bits	PCB	Field Mnemonic: Description
7	ROX	PCBS_WAIT_DPLL_LOCK_ERR: Hang during Unassisted Exit waiting on DPLL: WAIT_DPLL_LOCK state
8	ROX	PCBS_SPARE8_ERR: spare bit, always 0
9	ROX	PCBS_WINKLE_EXIT_SEND_INT_ASSIST_ERR: Hang during Assisted Winkle Exit: WINKLE_EXIT_SEND_INT_ASSIST state
10	ROX	PCBS_WINKLE_EXIT_SEND_INT_POWUP_ASSIST_ERR: Hang during Assisted Winkle Exit: WINKLE_EXIT_SEND_INT_POWUP_ASSIST state
11	ROX	PCBS_WRITE_FSM_GOTO_REG_IN_INVALID_STATE_ERR: write to FSM goto register in invalid state
12	ROX	PCBS_WRITE_PMGP0_IN_INVALID_STATE_ERR: write to PMGP0 in invalid state
13	ROX	PCBS_FREQ_OVERFLOW_IN_PSTATE_MODE_ERR: frequency of DPLL in Pstate mode overflows (Fnom + desired Pstate > 511)
14	ROX	PCBS_ECO_RS_BYPASS_CONFUSION_ERR: ECO railstepper tried to exit Vcs bypass and enter Vdd bypass in one Pstate step (it is not clear, in which order this strange operation should be performed - most likely it should never happen to avoid that Vcs is greater than Vdd)
15	ROX	PCBS_CORE_RS_BYPASS_CONFUSION_ERR: same as previous error, but for core railstepper (it is not clear, in which order this strange operation should be performed - most likely it should never happen to avoid that Vcs is greater than Vdd)
16	ROX	PCBS_READ_LPST_IN_PSTATE_MODE_ERR: read LPST-array while iVRM FSMs are enabled (dial ivrm_fsm_enable asserted)
17	ROX	PCBS_LPST_READ_CORR_ERR: correctable error occurred when reading the LPST
18	ROX	PCBS_LPST_READ_UNCORR_ERR: uncorrectable error occurred when reading the LPST
19	ROX	PCBS_PFET_STRENGTH_OVERFLOW_ERR: overflow occurred when calculating the pFET strength (in final rounding step!)
20	ROX	PCBS_VDS_LOOKUP_ERR: Vds entry not found in lookup table (when performing the linear search!)
21	ROX	PCBS_IDLE_INTERRUPT_TIMEOUT_ERR: idle interrupt timeout in PCB interrupt controller
22	ROX	PCBS_PSTATE_INTERRUPT_TIMEOUT_ERR: PState interrupt timeout in PCB interrupt controller
23	ROX	PCBS_GLOBAL_ACTUAL_SYNC_INTERRUPT_TIMEOUT_ERR: GlobalActualSync Interrupt timeout in PCB interrupt controller
24	ROX	PCBS_PMAX_SYNC_INTERRUPT_TIMEOUT_ERR: PmaxSync Interrupt timeout in PCB interrupt controller
25	ROX	PCBS_GLOBAL_ACTUAL_PSTATE_PROTOCOL_ERR: a write to global actual Pstate register has occurred before the global actual Pstate interrupt has left PCBS
26	ROX	PCBS_PMAX_PROTOCOL_ERR: a write to the Pmax/Pmin register has occurred before the Pmax sync interrupt has left PCB
27	ROX	PCBS_IVRM_GROSS_OR_FINE_ERR: iVRM gross or fine error (details to be found in PCBS_ivrm_Control_Status_Reg)
28	ROX	PCBS_IVRM_RANGE_ERR: iVRM range error (summary bit, details to be found in PCBS_ivrm_Control_Status_Reg)
29	ROX	PCBS_DPLL_CPM_FMIN_ERR: DPLL CPM Fmin error
30	ROX	PCBS_DPLL_DCO_FULL_ERR: DPLL DCO full
31	ROX	PCBS_DPLL_DCO_EMPTY_ERR: DPLL DCO empty
32	ROX	PCBS_DPLL_INT_ERR: DPLL internal error
33	ROX	PCBS_FMIN_AND_NOT_CPMBIT_ERR: dpll_fmin_and_not_cpmbit (ref. to dial cpm_fmin_clip_error_sel on how to configure this)
34	ROX	PCBS_DPLL_FASTER_THAN_FMAX_PLUS_DELTA1_ERR: dpll_faster_than_fmax_plus_delta1 (for characterization, delta1 is configurable with pll_char_delta1)



Bits	PCB	Field Mnemonic: Description
35	ROX	PCBS_DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2_ERR: dpll_slower_than_fmin_minus_delta2 (for characterization, delta2 is configurable with pll_char_delta2)
36	ROX	PCBS_RESCLK_CSB_INSTR_VECTOR_CHG_IN_INVALID_STATE_ERR: RESCLK CSB instruction vector change while FSMs none idle
37	ROX	PCBS_RESCLK_BAND_BOUNDARY_CHG_IN_INVALID_STATE_ERR: RESCLK Band boundaries change while FSMs none idle
38	ROX	PCBS_OCC_HEARTBEAT_LOSS_ERR: OCC heartbeat loss
39	ROX	PCBS_SPARE39_ERR: spare bit, always 0
40	ROX	PCBS_SPARE40_ERR: spare bit, always 0
41	ROX	PCBS_SPARE41_ERR: spare bit, always 0
42	ROX	PCBS_SPARE42_ERR: spare bit, always 0

Register Name	<i>PM Error Mask Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PMERRMASK_REG
Address	000000001B0F010A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_HANG_ERR_MASK: Mask for this error: 1=masked, 0=not masked
1	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ASSIST_HANG_ERR_MASK: Mask for this error: 1=masked, 0=not masked
2	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
3	RW	PCBS_SLEEP_EXIT_INVOKE_PORE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
4	RW	PCBS_WINKLE_ENTRY_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
5	RW	PCBS_WINKLE_ENTRY_SEND_INT_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
6	RW	PCBS_WINKLE_EXIT_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
7	RW	PCBS_WAIT_DPLL_LOCK_ERR_MASK: Mask for this error: 1=masked, 0=not masked
8	RW	PCBS_SPARE8_ERR_MASK: Mask for this error: 1=masked, 0=not masked
9	RW	PCBS_WINKLE_EXIT_SEND_INT_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
10	RW	PCBS_WINKLE_EXIT_SEND_INT_POWUP_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
11	RW	PCBS_WRITE_FSM_GOTO_REG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
12	RW	PCBS_WRITE_PMGP0_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
13	RW	PCBS_FREQ_OVERFLOW_IN_PSTATE_MODE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
14	RW	PCBS_ECO_RS_BYPASS_CONFUSION_ERR_MASK: Mask for this error: 1=masked, 0=not masked
15	RW	PCBS_CORE_RS_BYPASS_CONFUSION_ERR_MASK: Mask for this error: 1=masked, 0=not masked
16	RW	PCBS_READ_LPST_IN_PSTATE_MODE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
17	RW	PCBS_LPST_READ_CORR_ERR_MASK: Mask for this error: 1=masked, 0=not masked
18	RW	PCBS_LPST_READ_UNCORR_ERR_MASK: Mask for this error: 1=masked, 0=not masked

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Bits	PCB	Field Mnemonic: Description
19	RW	PCBS_PFET_STRENGTH_OVERFLOW_ERR_MASK: Mask for this error: 1=masked, 0=not masked
20	RW	PCBS_VDS_LOOKUP_ERR_MASK: Mask for this error: 1=masked, 0=not masked
21	RW	PCBS_IDLE_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
22	RW	PCBS_PSTATE_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
23	RW	PCBS_GLOBAL_ACTUAL_SYNC_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
24	RW	PCBS_PMAX_SYNC_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
25	RW	PCBS_GLOBAL_ACTUAL_PSTATE_PROTOCOL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
26	RW	PCBS_PMAX_PROTOCOL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
27	RW	PCBS_IVRM_GROSS_OR_FINE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
28	RW	PCBS_IVRM_RANGE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
29	RW	PCBS_DPLL_CPM_FMIN_ERR_MASK: Mask for this error: 1=masked, 0=not masked
30	RW	PCBS_DPLL_DCO_FULL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
31	RW	PCBS_DPLL_DCO_EMPTY_ERR_MASK: Mask for this error: 1=masked, 0=not masked
32	RW	PCBS_DPLL_INT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
33	RW	PCBS_FMIN_AND_NOT_CPMBIT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
34	RW	PCBS_DPLL_FASTER_THAN_FMAX_PLUS_DELTA1_ERR_MASK: Mask for this error: 1=masked, 0=not masked
35	RW	PCBS_DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2_ERR_MASK: Mask for this error: 1=masked, 0=not masked
36	RW	PCBS_RESCLK_CSB_INSTR_VECTOR_CHG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
37	RW	PCBS_RESCLK_BAND_BOUNDARY_CHG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
38	RW	PCBS_OCC_HEARTBEAT_LOSS_ERR_MASK: Mask for this error: 1=masked, 0=not masked
39	RW	PCBS_SPARE39_ERR_MASK: Mask for this error: 1=masked, 0=not masked
40	RW	PCBS_SPARE40_ERR_MASK: Mask for this error: 1=masked, 0=not masked
41	RW	PCBS_SPARE41_ERR_MASK: Mask for this error: 1=masked, 0=not masked
42	RW	PCBS_SPARE42_ERR_MASK: Mask for this error: 1=masked, 0=not masked

Register Name		<i>PM Special Wakeup FSP</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PMSPCWKUPFSP_REG
Address		000000001B0F010B (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RW	FSP_SPECIAL_WAKEUP: Chiplet Special Wakeup for FSP Firmware use. NOTE: protocol is required when setting this bit

Register Name	<i>PM Special Wakeup OCC</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PMSPCWKUPOCC_REG	
Address	000000001B0F010C (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	RW	OCC_SPECIAL_WAKEUP: Chiplet Special Wakeup for OCC Firmware use. NOTE: protocol is required when setting this bit

Register Name	<i>PM Special Wakeup Hypervisor</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PMSPCWKUPPHYP_REG	
Address	000000001B0F010D (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	RW	PHYP_SPECIAL_WAKEUP: Chiplet Special Wakeup for hypervisor Firmware use. NOTE: protocol is required when setting this bit

Register Name	<i>PFET Control/Status Register For Core And ECO Vcs</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PFVCS_CNTLSTAT_REG	
Address	000000001B0F010E (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:1	RW	CORE_VCS_PFET_FORCE_STATE: Core Domain PFET Force State Provides a means for firmware to force the core domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 4:5 = 00 (both core_vcs_pfet_val_override AND core_vcs_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
2:3	RW	ECO_VCS_PFET_FORCE_STATE: ECO Domain PFET Force State Provides a means for firmware to force the ECO domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 6:7 = 00 (both eco_vcs_pfet_val_override AND eco_vcs_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
4	RW	CORE_VCS_PFET_VAL_OVERRIDE: Core Domain PFET Value Override 0 = Override is disabled

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Bits	PCB	Field Mnemonic: Description
5	RW	CORE_VCS_PFET_SEL_OVERRIDE: Core Domain PFET Stage Select Override 0 = Override is disabled
6	RW	ECO_VCS_PFET_VAL_OVERRIDE: ECO Domain PFET Value Override 0 = Override is disabled
7	RW	ECO_VCS_PFET_SEL_OVERRIDE: ECO Domain PFET Stage Select Override 0 = Override is disabled
8	RW	CORE_VCS_PFET_ENABLE_REGULATION_FINGER: Core Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the core_vcs_pfet_enable_value.
9	RW	ECO_VCS_PFET_ENABLE_REGULATION_FINGER: ECO Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the eco_vcs_pfet_enable_value.
10:21	RW	CORE_VCS_PFET_ENABLE_VALUE: Core PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the Core Domain PFET Enables directly. If core_vcs_pfet_val_override = 1, a write to this field sets the state of the core PFET Enables until core_vcs_pfet_val_override is cleared. If core_vcs_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the core_vcs_pfet_valN_slat registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
22:25	RW	CORE_VCS_PFET_SEL_VALUE: Core PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure core_vcs_pfet_valN_slate(0:11) where N is 0 to 11 if core_vcs_pfet_sel_override = 1. If core_vcs_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
26:37	RW	ECO_VCS_PFET_ENABLE_VALUE: ECO PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the ECO PFET Enables directly. If ECO_vcs_pfet_val_override = 1, a write to this field sets the state of the ECO PFET Enables until ECO_vcs_pfet_val_override is cleared. If eco_vcs_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the eco_vcs_pfet_valN_slat registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
38:41	RW	ECO_VCS_PFET_SEL_VALUE: ECO PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure eco_vcs_pfet_valN_slate(0:11) where N is 0 to 11 if eco_vcs_pfet_sel_override = 1. If eco_vcs_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
42:45	ROX	CORE_VCS_PG_STATE: Core power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
46:49	ROX	CORE_VCS_PG_SEL: For debug, contains the actual index n into Core Domain PFET Value [n] SLAT Register set that contains the Core PFET Enable Value currently enabled.



Bits	PCB	Field Mnemonic: Description
50:53	ROX	ECO_VCS_PG_STATE: ECO Domain power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
54:57	ROX	ECO_VCS_PG_SEL: For debug, contains the actual index n into ECO Domain PFET Value [n] SLAT Register set that contains the ECO PFET Enable Value currently enabled.

Register Name	<i>PM State History Register For Hypervisor</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPHYP_REG
Address	000000001B0F0110 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	PHYP_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	PHYP_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	PHYP_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	PHYP_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	PHYP_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	PHYP_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For FSP</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PMSTATEHISTFSP_REG
Address	000000001B0F0111 (PCB)
Attributes	
Description	

Registers Specification

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Bits	PCB	Field Mnemonic: Description
0:2	ROX	FSP_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	FSP_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	FSP_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	FSP_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	FSP_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	FSP_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For OCC</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PMSTATEHISTOCC_REG
Address	000000001B0F0112 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	OCC_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	OCC_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	OCC_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	OCC_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	OCC_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	OCC_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For PerfMon</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPERF_REG
Address	000000001B0F0113 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	PERF_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	PERF_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	PERF_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	PERF_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	PERF_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	PERF_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM FSM Reset And Babystepper Idle Injects</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.IDLEFSMGOTOCMD_REG
Address	000000001B0F0114 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	WO_1P	idle_fsm_goto_cmd ' A write to this reg will proceed the IDLE FSM from WAIT_FOR_PORE_DONE, SLEEP_EXIT_WAIT_FOR_PORE_FAST_EXIT_DONE, or WINKLE_EXIT_WAIT_FOR_PORE_FAST_EXIT_DONE to the following states: ' 0b01: goto IDLE state ' 0b10: goto SLEEP_EXIT_CORE_MESHLET_ON state ' 0b11: goto WINKLE_EXIT_NOTIFY_PMC state '
2	RWX	babystp_trigger_sleep_entry ' A write to this reg with a 1 in this field will cause the babystepper to run the sleep entry sequence. This step is needed for an assisted entry into sleep, before the power is actually turned off since the babystepper needs to know about the sleep state. For an unassisted entry, writing this register must not be performed.' '' 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished entering its sleep mode.'

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Bits	PCB	Field Mnemonic: Description
3	RWX	babystp_trigger_winkle_entry ' A write to this reg with a 1 in this field will cause the babystepper to run the winkle entry sequence. This step is needed for an assisted entry into winkle before the power is actually turned off since the babystepper needs to know about the winkle state. For an unassisted entry, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished entering its winkle mode. '
4	RWX	babystp_trigger_wakeup ' A write to this reg with a 1 in this field will cause the babystepper to run the wakeup sequence from sleep/winkle depending on the babystepper state of sleep or winkle. This step is needed for an assisted exit from winkle before the power is actually turned off since the babystepper needs to know about the wakeup state. For an unassisted exit, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished waking up from sleep or winkle. '

Register Name	Core PFET Power Up Delay
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.COREPFPUDLY_REG
Address	000000001B0F012C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_POWUP_DLY0: Delay used after transitioning to Core Domain power up sequence stage0. The delays in this register are in terms of PCBS clock period (4.46ns) times 2^(15 minus this value). Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	CORE_POWUP_DLY1: Delay used after transitioning to Core domain power up sequence stage1.
8:19	RW	CORE_POWER_UP_DELAY_SEL: Vector select for which delay to use for the respective power-up stage. Bit mapping: 8 -> core_*_pfet_enable(0) 9 -> core_*_pfet_enable(1) ... 19 -> core_*_pfet_enable(11) Bit meaning: 0 = Use core_powup_dly0 1 = Use core_powup_dly1

Register Name	Core PFET Power Down Delay
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.COREPFPDDLY_REG
Address	000000001B0F012D (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_POWDN_DLY0: Delay used after transitioning to Core domain power dn sequence stage1. The delays in this register are in terms of PCBS clock period (4.46ns) times 2^(15 minus this value). Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	CORE_POWDN_DLY1: Delay used after transitioning to Core domain power dn sequence stage1. The delays in this register are in terms of PCBS clock period (4.46ns) times 2^(15 minus this value). Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.

Bits	PCB	Field Mnemonic: Description
8:19	RW	CORE_POWER_DN_DELAY_SEL: Vector select for which delay to use for the respective power-dn stage. Bit mapping: 8 -> core_*_pfet_enable(0) 9 -> core_*_pfet_enable(1) ... 19 -> core_*_pfet_enable(11) Bit meaning: 0 = Use core_powdn_dly0 1 = Use core_powdn_dly1

Register Name		Core PFET Vretention
Mnemonic		EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.COREPFVRET_REG
Address		000000001B0F0130 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_VRET_SEL: Pointer to the stage representing the Vretention value for the core PFETs. Power down sequences will stop after enabling this stage.
4:7	RW	CORE_VOFF_SEL: Pointer to the stage representing the Voff value for the core PFETs. Power down sequences will stop after enabling this stage.

Register Name		ECO PFET Power Up Delay
Mnemonic		EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.ECOPFPUDLY_REG
Address		000000001B0F014C (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_POWUP_DLY0: Delay used after transitioning to ECO domain power up sequence stage0 in terms of refclk period (4.46ns) times 2^(15 minus this value). Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	ECO_POWUP_DLY1: Delay used after transitioning to ECO domain power up sequence stage1.
8:19	RW	ECO_POWER_UP_DELAY_SEL: Vector select for which delay to use for the respective power-up stage. Bit mapping: 8 -> eco_*_pfet_enable(0) 9 -> eco_*_pfet_enable(1) ... 19 -> eco_*_pfet_enable(11) Bit meaning: 0 = Use eco_powup_dly0 1 = Use eco_powup_dly1

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Register Name	<i>ECO PFET Power Down Delay</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.ECOPFPDDLY_REG
Address	000000001B0F014D (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_POWDN_DLY0: UNUSED/SPARE
4:7	RW	ECO_POWDN_DLY1: Delay used after transitioning to ECO Domain power dn sequence stage1. The delays in this register are in terms of refclk period (4.46ns) times 2^(15 minus this value). Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
8:19	RW	ECO_POWER_DN_DELAY_SEL: Vector select for which delay to use for the respective power-down stage. Bit mapping: 8 -> eco_*_pfet_enable(0) 9 -> eco_*_pfet_enable(1) ... 19 -> eco_*_pfet_enable(11) Bit meaning: 0 = Use eco_powdn_dly0 1 = Use eco_powdn_dly1

Register Name	<i>ECO PFET Vretention</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.ECOPFVRET_REG
Address	000000001B0F0150 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_VRET_SEL: Pointer to the stage representing the Vretention value for the ECO PFETs. Power down sequences will stop after enabling this stage.
4:7	RW	ECO_VOFF_SEL: Pointer to the stage representing the Voff value for the ECO PFETs. Power down sequences will stop after enabling this stage.

Register Name	<i>Frequency Control Register With Overrides For DPLL</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.FREQ_CTRL_REG
Address	000000001B0F0151 (PCB)
Attributes	
Description	Note that overrides to Dpll_fmax are only applied if Dpll_freq_override_enable = 1. A read of all these dials always returns the currently established DPLL frequencies (regardless of any other mode settings).

Bits	PCB	Field Mnemonic: Description
0:8	RWX	DPLL_FMIN: minimum DPLL frequency in CPM-DPLL mode that is set at IPL time A read always returns the currently established value A write is not conditioned on any other dial setting.

Bits	PCB	Field Mnemonic: Description
9:17	RWX	DPLL_FMAX: DPLL maximum frequency and frequin (these two values are the same in POWER8 processor) without applying bias values: A read always returns the currently established value A write is conditioned on the setting of dpll_freq_override_enable. If dpll_freq_override_enable is asserted, a write causes this field to update. Otherwise the hardware (that is, PStates) are controlling the update of this value.
18:21	RO	Reserved.
22:30	RW	FREQU_AT_PSTATE0: DPLL frequency for Pstate 0

Register Name	<i>DPLL Mode Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.DPLL_CPM_PARM_REG
Address	000000001B0F0152 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	LF_SLEWRATEXPI: out of lock slew rate for DPLL
8	RW	LF_USE_CPMXPI: use CPM instead of PFD as loop filter input, if '1' (instead of using both)
9	RW	FF_USE_CPMXPI: use the CPM inputs for the frequency filter, if '1'
10	RW	CPM_FILTER_ENABLE: enables the CPM filter
11	RW	FF_BYPASSXPI: enables frequency filter bypass
12	RW	DCO_OVERRIDE: enables overrides for DCO testing/characterization
13	RW	DCO_INCR: enables increment for DCO testing/characterization, increments only on a rising edge
14	RW	DCO_DECR: enables decrement for DCO testing/characterization, decrements only on a rising edge
15:23	RW	DPLL_LOCK_TIMER_REPLACEMENT_VALUE: if dpll_lock_replacement_timer_mode_en is set, this dial specifies the delay in us, after which it is assumed, that the DPLL has reached a frequency lock condition. Note that values less than 3 will cause in undefined HW behavior (0 will cause HANGs!). if dpll_lock_replacement_timer_mode_en is zero, this dial specifies the delay in pcb_nclk cycles after which the hardware monitors the DPLL frequout output (if dpll_freqout_mode_en is set) or the DPLL flock output (if dpll_flock_mode_en is set). Note that in this case, the value of this dial needs to be greater or equal to 150 (decimal).
24:31	RW	PRE_VRET_PSTATE: Pstate that is stepped to before switching to Vretention defined in PCBS_iVRM_Control_Status_Reg
32	RW	OVERRIDE_PCBS_DPLL_SYNCHRONIZER: Bypasses the 'ping-pong' synchronization logic between the DPLL and the PCBS-PM. NEVER SET TO 1 UNLESS YOU KNOW WHAT YOU ARE DOING!
33:36	RW	DPLL_CHAR_DELTA1: Delta in DPLL ticks for characterization (cf. dial dpll_faster_than_fmax_plus_delta1)
37:40	RW	DPLL_CHAR_DELTA2: Delta in DPLL ticks for characterization (cf. dial dpll_faster_than_fmin_minus_delta2)

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Register Name	PPMSR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_STATUS_REG
Address	000000001B0F0153 (PCB)
Attributes	
Description	Provides read access to the power management status that is also shadowed to the PC and visible to the hypervisor in the PMSR (with some delay due to the shadowing process).

Bits	PCB	Field Mnemonic: Description
0:7	ROX	global_pstate_actual ' Actual Global Pstate or Pglobal_actual' '' Reads from this field return the presently established global PState value.' '' Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent '
8:15	ROX	LOCAL_PSTATE_ACTUAL: ' Actual Local PState or Plocal_actual' '' Reads from this field return the presently established local PState value. This value will always be less than or equal to global_pstate_actual.' '' Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent ''
16:23	ROX	pv_min Minimum Pstate set by the platform.
24:31	ROX	pvf_max Maximum Pstate set by the platform.
32	ROX	spr_em_disabled ' SPR Energy Management Disabled' 'Read from this field indicate whether the platform has disabled the 'PMCR and PMICR SPRs to control the chiplet Pstate. '
33	ROX	Psafe_mode_active Read from this field indicate whether the chiplet has been put into a safe mode with Psafe enabled to a OCC heartbeat loss or other externally forced reasons (0=regular mode, 1=safe mode is active)
34	ROX	iVRM_safe_mode_active Read from this field indicate whether the chiplet has been put the iVRM safe mode (forcing the bypass mode for all iVRMs)
35	ROX	ivrm_enable Read from this field indicate whether the chiplet internal voltage regulation macro is enabled for localized voltage control (0=disabled, 1=enabled) based on ANDing the poweron signals to the iVRMs
36	ROX	all_fsms_in_safe_state For recovery: if this bit is asserted, all Pstate and iVRM control FSMs are in a stable, safe state that allows the recovery routine to proceed with resetting the PCBS PM without the risk of interrupt a critical action
37:40	ROX	pmsr_spares spare bits

Register Name	PIVRMCSR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_CONTROL_STATUS_REG
Address	000000001B0F0154 (PCB)
Attributes	
Description	Provides access to chiplet-level controls of the internal VRM rail set (VDD and VCS) across both the core and ECO domains. The following is valid only for bits 4 to 7. When in automatic iVRM mode (ivrm_fsm_enable = 1), these bits provide access to the values established by the automatic hardware mechanism. When In iVRM override mode (ivrm_fsm_enable = 0), these bits allow firmware direct control of the values driving the internal VRMs.

Bits	PCB	Field Mnemonic: Description
0	RW	IVRM_FSM_ENABLE: Internal master VRM FSM Enable 0 = Disable Internal VRM FSMs and enable to control the iVRMs with the available override registers (SCOMable) as a backup mode or for setup (override mode) 1 = Enable Internal VRM FSM sequencers (requires that Pstates are enabled with enable_Pstate_mode=1 as well) (automatic mode)
1	RW	USE_IVRM_FOR_VRET: Internal VRM Enabled for Vretention 0 = Disable Internal VRM for Vretention 1 = Enable Internal VRM for Vretention
2	RW	BINSEARCH_CAL_ENA: trigger binary search (level signal)
3	RW	PVREF_EN: Internal VRM Power Voltage Reference Forced Enable 0 = Allow hardware to enable/disable pvref circuit 1 = Force enablement of the pvref circuit
4	RWX	IVRM_CORE_VDD_BYPASS_B: Internal VRM Core VDD Bypass (negative active) 0 = VDD Internal Core VRMs in bypass 1 = VDD internal Core VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
5	RWX	IVRM_CORE_VDD_POWERON: Internal VRM Core VDD Poweron 0 = Core VDD Internal VRMs powered off 1 = Core VDD internal VRMs powered on if this bit is not set (=0), the Core VDD internal VRM powered off internally. If this bit is set (=1), the Core VDD internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
6	RWX	IVRM_CORE_VCS_BYPASS_B: Internal VRM Core VCS Bypass (negative active) 0 = VCS Internal Core VRMs in bypass 1 = VCS internal Core VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VCS internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VCS internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
7	RWX	IVRM_CORE_VCS_POWERON: Internal VRM Core VCS Poweron 0 = Core VCS Internal VRMs powered off 1 = Core VCS internal VRMs powered on if this bit is not set (=0), the Core VCS internal VRM powered off internally. If this bit is set (=1), the Core VCS internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
8	RWX	IVRM_ECO_VDD_BYPASS_B: Internal VRM ECO VDD Bypass (negative active) 0 = VDD Internal ECO VRMs in bypass 1 = VDD internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.

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Bits	PCB	Field Mnemonic: Description
9	RWX	IVRM_ECO_VDD_POWERON: Internal VRM ECO VDD Bypass (negative active) 0 = VDD Internal ECO VRMs in bypass 1 = VDD internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
10	RWX	IVRM_ECO_VCS_BYPASS_B: Internal VRM ECO VCS Bypass (negative active) 0 = VCS Internal ECO VRMs in bypass 1 = VCS internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VCS internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VCS internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
11	RWX	IVRM_ECO_VCS_POWERON: Internal VRM ECO VCS Poweron 0 = ECO VCS Internal VRMs powered off 1 = ECO VCS internal VRMs powered on if this bit is not set (=0), the ECO VCS internal VRM powered off internally. If this bit is set (=1), the ECO VCS internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
12:18	RWX	IVRM_VRET_VDD: if use_ivrm_for_Vret is asserted, this dial is used to control the Vdd retention voltage. Note: this field will establish the Core VDD rail for Sleep and both the Core and ECO rail for Winkle. - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
19:25	RWX	IVRM_VRET_VCS: if use_ivrm_for_Vret is asserted, this dial is used to control the Vcs retention voltage. Note: this field will establish the Core VDD rail for Sleep and both the Core and ECO rail for Winkle. - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
26:30	RWX	IVRM_VRET_CORE_VDD_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the Core Vdd iVRM PFET strength for the retention voltage
31:35	RWX	IVRM_VRET_CORE_VCS_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the Core Vcs iVRM PFET strength for the retention voltage
36:40	RWX	IVRM_VRET_ECO_VDD_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the ECO Vdd iVRM PFET strength for the retention voltage
41:45	RWX	IVRM_VRET_ECO_VCS_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the ECO Vcs iVRM PFET strength for the retention voltage
46	RW	PVREF_FAIL: voltage reference fail input to iVRMs
47	ROX	IVRM_PREF_ERROR_GROSS: Voltage Reference Gross Error 0 = Gross Error not detected 1 = Gross Error detected
48	ROX	IVRM_PREF_ERROR_FINE: Voltage Reference Fine Error 0 = Fine Error not detected 1 = Fine Error detected

Bits	PCB	Field Mnemonic: Description
49	ROX	IVRM_CORE_VDD_RANGE_HI: Core VDD Internal VRM Range Hi Indicator 0 = Core VDD Internal VRM Hi indicator signal not asserted 1 = Core VDD internal VRMs Hi indicator signal asserted
50	ROX	IVRM_CORE_VDD_RANGE_LO: Core VDD Internal VRM Range Low Indicator 0 = Core VDD Internal VRM Low indicator signal not asserted 1 = Core VDD internal VRMs Low indicator signal asserted
51	ROX	IVRM_ECO_VDD_RANGE_HI: ECO VDD Internal VRM Range Hi Indicator 0 = ECO VDD Internal VRM Hi indicator signal not asserted 1 = ECO VDD internal VRMs Hi indicator signal asserted
52	ROX	IVRM_ECO_VDD_RANGE_LO: ECO VDD Internal VRM Range Low Indicator 0 = ECO VDD Internal VRM Low indicator signal not asserted 1 = ECO VDD internal VRMs Low indicator signal asserted
53	ROX	IVRM_CORE_VCS_RANGE_HI: Core VCS Internal VRM Range Hi Indicator 0 = Core VCS Internal VRM Hi indicator signal not asserted 1 = Core VCS internal VRMs Hi indicator signal asserted
54	ROX	IVRM_CORE_VCS_RANGE_LO: Core VCS Internal VRM Range Low Indicator 0 = Core VCS Internal VRM Low indicator signal not asserted 1 = Core VCS internal VRMs Low indicator signal asserted
55	ROX	IVRM_ECO_VCS_RANGE_HI: ECO VCS Internal VRM Range Hi Indicator 0 = ECO VCS Internal VRM Hi indicator signal not asserted 1 = ECO VCS internal VRMs Hi indicator signal asserted
56	ROX	IVRM_ECO_VCS_RANGE_LO: ECO VCS Internal VRM Range Low Indicator 0 = ECO VCS Internal VRM Low indicator signal not asserted 1 = ECO VCS internal VRMs Low indicator signal asserted
57	ROX	BINSEARCH_CAL_DONE: binary search done signal
58	RWX	IVRM_CORE_VDD_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
59	RWX	IVRM_CORE_VCS_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
60	RWX	IVRM_ECO_VDD_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
61	RWX	IVRM_ECO_VCS_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
62	RW	IVRM_POWER_DOWN_DISABLE: If this bit is 1, the iVRM poweron signal is left asserted. Power off of the iVRMs is then blocked

Registers Specification

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Register Name	<i>PIVRMVSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VALUE_SETTING_REG
Address	000000001B0F0155 (PCB)
Attributes	
Description	Allows access to VID values and PFET strength valid signal settings presented to the internal VRM rail set (VDD and VCS) across both the core and ECO domains. When in <code>ivrm_fsm_enable = "auto"</code> mode, this register provides access to the values established by the automatic hardware mechanism. When <code>ivrm_fsm_enable = "override"</code> mode, this register allows firmware direct control of the values driving the internal VRMs which, if the VRMs are not in bypass, will move the voltage settings.

Bits	PCB	Field Mnemonic: Description
0:7	RWX	IVRM_CORE_VDD_IVID: When read, returns the value presently being driving to the Core VDD iVRM. If <code>ivrm_fsm_enable = 0</code> (override_mode), then writes to this field will drive a new VID value to the Core VDD iVRM. If <code>ivrm_fsm_enable = 1</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
8:15	RWX	IVRM_CORE_VCS_IVID: When read, returns the value presently being driving to the Core VCS iVRM. If <code>ivrm_fsm_enable = 0</code> (override_mode), then writes to this field will drive a new VID value to the Core VCS iVRM. If <code>ivrm_fsm_enable = 1</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
16:23	RWX	IVRM_ECO_VDD_IVID: When read, returns the value presently being driving to the Core VDD iVRM. If <code>ivrm_fsm_enable = 0</code> (override_mode), then writes to this field will drive a new VID value to the ECO VDD iVRM. If <code>ivrm_fsm_enable = 1</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
24:31	RWX	IVRM_ECO_VCS_IVID: When read, returns the value presently being driving to the ECO VCS iVRM. If <code>ivrm_fsm_enable = 0</code> (override_mode), then writes to this field will drive a new VID value to the ECO VCS iVRM, If <code>ivrm_fsm_enable = 0</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
32:36	RWX	IVRM_CORE_VDD_PFET_STRENGTH: When read, returns the value presently being driving to the core VCS iVRM. If <code>ivrm_fsm_enable = 0</code> (override_mode), then writes to this field will drive a new strength value to the core VCS iVRM, If <code>ivrm_fsm_enable = 0</code> , writes to this field are not performed.

Bits	PCB	Field Mnemonic: Description
37:41	RWX	IVRM_CORE_VCS_PFET_STRENGTH: This register is assigned to the signals tcex##_tp_ivrm_core_vcs_sense & tcex##_tp_ivrm_core_vdd_sense & tcex##_tp_ivrm_eco_vcs_sense & tcex##_tp_ivrm_eco_vdd_sense & 0b0 Note that all other sense signals are spares now and tied to 0. OUTDATED TEXT: When read, returns the value presently being driving to the core VDD iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the core VDD iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
42:46	RWX	IVRM_ECO_VDD_PFET_STRENGTH: When read, returns the value presently being driving to the ECO VCS iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the ECO VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
47:51	RWX	IVRM_ECO_VCS_PFET_STRENGTH: When read, returns the value presently being driving to the ECO VDD iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the ECO VDD iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
52	RWX	IVRM_VDD_CORE_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the Core VDD iVRM. If ivrm_fsm_enable = 1 AND ivrm_control_mode = 1 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the Core VDD iVRM, If ivrm_fsm_enable = 0 OR ivrm_control_mode = 0, writes to this field are not performed.
53	RWX	IVRM_VCS_CORE_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the Core VCS iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the Core VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
54	RWX	IVRM_VDD_ECO_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the ECO VDD iVRM. If ivrm_fsm_enable = 1 AND ivrm_control_mode = 1 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the ECO VDD iVRM, If ivrm_fsm_enable = 0 OR ivrm_control_mode = 0, writes to this field are not performed.
55	RWX	IVRM_VCS_ECO_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the ECO VCS iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the ECO VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
56	RWX	CORE_VDD_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
57	RWX	CORE_VCS_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
58	RWX	ECO_VDD_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
59	RWX	ECO_VCS_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.

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Register Name		General PCBS Modes And Debug Switches
Mnemonic		EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBSPM_MODE_REG
Address		000000001B0F0156 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RW	ENABLE_PSTATE_MODE: if asserted, Pstate requests (from overrides or PMCR) will be honored, otherwise, the hardware does not do anything. Note to firmware: this is the master switch for Pstates and should be asserted after all sub-modes (that is, lvrn_fsm_en) are setup to avoid enabling unintentional modes during the mode setup.
1	RW	GLOBAL_PSTATE_CHANGE_FOR_IDLE_STATE_ENABLED: if asserted, a global Pstate change to the Nap/Sleep/Winkle-Pstate is requested, when the Nap/Sleep/Winkle state is entered and the individual enable bits in the PIMCR are asserted
2	RW	ENABLE_GLOBAL_PSTATE_REQ: if '1' then enable PMC interrupt with global Pstate change request, otherwise, disable global requests
3	RW	ENABLE_WINKLE_WITH_CPM_MODE: if '1', PCBS automatically changes the DPLL mode to mode 1, when entering winkle, but changes the mode back to CPM mode when exiting. Needed for CPM-DPLL control loop enablement.
4	RW	ENABLE_CLIPPING_OF_GLOBAL_PSTATE_REQ: if '1', PCBS automatically clips global Pstate requests with Pvf_max in PPMBR and sets the 'donate' bit in the interrupt accordingly
5	RW	CHKSW_HW214553: if deasserted, HW214553 (frequin issue in resclk mode) is fixed, if asserted, the fix is not active
6	RW	ENABLE_PMC_PMAX_SYNC_NOTIFICATION: if asserted, the PCBS-PM will send a 'Pmax_sync' interrupt, once the synchronization criterion is met
7	RW	DPLL_LOCK_REPLACEMENT_TIMER_MODE_EN: Select a timer instead of the DPLL lock bit as target frequency reached criterion. This timer has to be setup by the dial dpll_lock_timer_replacement_value. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
8	RW	DPLL_FREQOUT_MODE_EN: Looks at the DPLL frequout to find out, if the target frequency has been reached. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
9	RW	DPLL_FLOCK_MODE_EN: Looks at the real DPLL flock output to find out, if the target frequency has been reached. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
10	RW	ENABLE_SENSE_DELAY_CHARACTERIZATION: If this switch is 0, the sense latches are updated every cycle. If this switch is 1, the sense delay measurement mode is enabled, that starts a sense delay timer, whenever one of the registers that drive the inputs of the iVRMs/pFETs is written via PCB and that triggers a sense register freeze operation, when the sense delay timer reaches the value sense_delay_timer_val. With this mode, the sense delays can be measured in multiples of the PCB-slave clock speed.
11:17	RW	SENSE_DELAY_TIMER_VAL: See the description of enable_sense_delay_characterization for details.
18:19	RW	CPM_FMIN_CLIP_ERROR_SEL: This dial selects, which of the following conditions will cause the FIR bit dpll_fmin_and_not_cpmbit to be set to detect, that the DPLL runs at Fmin, but is still clipped by the CPMs. 0b00 = function is disabled 0b01 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit2 = 0 0b10 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit1 = 0 0b11 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit0 = 0
20:23	RW	DBG_TRACE_SEL: This dial selects the group of signals to be traced for debug in the lab. Details to be found in the Section 'Trace Bus'

Bits	PCB	Field Mnemonic: Description
24:25	RW	TRACE_DATA_SEL: This dial selects the group of signals to be traced for debug in the lab. Details to be found in the Section 'Trace Bus'
26:29	RW	TP_CPLT_IVRM_VPP_TUNE: Tune bits to be set going to the iVRMs

Register Name	<i>PIVRMPS Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_PFETSTR_SENSE_REG
Address	000000001B0F0157 (PCB)
Attributes	
Description	Used to check that the pFET sense outputs correspond to the driven values (mainly for test).

Bits	PCB	Field Mnemonic: Description
0:4	ROX	IVRM_CORE_VDD_PFETSTR_SNS: Not used any more.
5:9	ROX	IVRM_CORE_VCS_PFETSTR_SNS: This register is assigned to the signals tcex##_tp_ivrm_core_vcs_sense & tcex##_tp_ivrm_core_vdd_sense & tcex##_tp_ivrm_eco_vcs_sense & tcex##_tp_ivrm_eco_vdd_sense & 0b0
10:14	ROX	IVRM_ECO_VDD_PFETSTR_SNS: Not used any more.
15:19	ROX	IVRM_ECO_VCS_PFETSTR_SNS: Not used any more.
20	ROX	IVRM_VDD_CORE_PFETSTR_VALID_SNS: Not used any more.
21	ROX	IVRM_VCS_CORE_PFETSTR_VALID_SNS: Not used any more.
22	ROX	IVRM_VDD_ECO_PFETSTR_VALID_SNS: Not used any more.
23	ROX	IVRM_VCS_ECO_PFETSTR_VALID_SNS: Not used any more.
24	ROX	CORE_VDD_BYPASS_B_SENSE: Not used any more.
25	ROX	CORE_VCS_BYPASS_B_SENSE: Not used any more.
26	ROX	ECO_VDD_BYPASS_B_SENSE: Not used any more.
27	ROX	ECO_VCS_BYPASS_B_SENSE: Not used any more.
28	ROX	CORE_VDD_POWERON_SENSE: Not used any more.
29	ROX	CORE_VCS_POWERON_SENSE: Not used any more.
30	ROX	ECO_VDD_POWERON_SENSE: Not used any more.
31	ROX	ECO_VCS_POWERON_SENSE: Not used any more.
32	ROX	CORE_VDD_VPUMP_EN_SENSE: Not used any more.
33	ROX	CORE_VCS_VPUMP_EN_SENSE: Not used any more.
34	ROX	ECO_VDD_VPUMP_EN_SENSE: Not used any more.
35	ROX	ECO_VCS_VPUMP_EN_SENSE: Not used any more.
36	ROX	CORE_VDD_PFET_LOW_VOUT_SNS: Not used any more.
37	ROX	CORE_VCS_PFET_LOW_VOUT_SNS: Not used any more.
38	ROX	ECO_VDD_PFET_LOW_VOUT_SNS: Not used any more.
39	ROX	ECO_VCS_PFET_LOW_VOUT_SNS: Not used any more.

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Register Name	PPMICR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_IDLE_CONTROL_REG
Address	000000001B0F0158 (PCB)
Attributes	
Description	Used to read the PMICR register typically owned (written) by the hypervisor. Writes are conditioned on the setting of the dial Pm_spr_override_en. If Pm_spr_override_en is set, firmware must make sure that the special wakeup state of this chiplet is reached before changing any of the latency fields in this register. Otherwise, the hardware behavior is undefined.

Bits	PCB	Field Mnemonic: Description
0:7	ROX	NAP_PSTATE_REQ: Nap Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
8	ROX	NAP_PSTATE_EN: Nap PState Enable 1 = Enable the Nap Pstate (NPS) Request, Nap Global Enable and Nap Latency functions 0 = Disables the Nap Pstate (NPS) Request, Nap Global Enable and Nap Latency functions Reads from the field return the value last written.
9	ROX	NAP_GLOBAL_EN: Nap Global Enable 1 = Upon the execution of a Nap instruction , the Nap Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a Nap instruction , the Nap Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.
10:11	ROX	NAP_LATENCY: Nap Latency not supported for POWER8 processor
12:15	ROX	RESERVED_PPMICR_0: reserved
16:23	ROX	SLEEP_PSTATE_REQ: sleep Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
24	ROX	SLEEP_PSTATE_EN: sleep PState Enable 1 = Enable the sleep Pstate (NPS) Request, sleep Global Enable and sleep Latency functions 0 = Disables the sleep Pstate (NPS) Request, sleep Global Enable and sleep Latency functions Reads from the field return the value last written.
25	ROX	SLEEP_GLOBAL_EN: sleep Global Enable 1 = Upon the execution of a sleep instruction , the sleep Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a sleep instruction , the sleep Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.



Bits	PCB	Field Mnemonic: Description
26:27	ROX	SLEEP_LATENCY: sleep Latency 00 = Cease instructions and honors Pstate change but does not perform additional state changing actions (unsupported in POWER8, maps to 0b10) 01 = Indicates to the platform that a sub-state that would have the lowest latency is enabled (unsupported in POWER8, maps to 0b10) 10 = Indicates to the platform that a sub-state that might have a medium exit latency is enabled (POWER8: Fast Sleep) 11 = Indicates to the platform that a sub-state that might have higher exit latency is enabled (POWER8: Deep Sleep)
28:31	ROX	RESERVED_PPMICR_1: reserved
32:39	ROX	WINKLE_PSTATE_REQ: winkle Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
40	ROX	WINKLE_PSTATE_EN: winkle PState Enable 1 = Enable the winkle Pstate (NPS) Request, winkle Global Enable and winkle Latency functions 0 = Disables the winkle Pstate (NPS) Request, winkle Global Enable and winkle Latency functions Reads from the field return the value last written.
41	ROX	WINKLE_GLOBAL_EN: winkle Global Enable 1 = Upon the execution of a winkle instruction , the winkle Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a winkle instruction , the winkle Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.
42:43	ROX	WINKLE_LATENCY: winkle Latency 00 = Cease instructions and honors Pstate change but does not perform additional state changing actions (unsupported in POWER8, maps to 0b10) 01 = Indicates to the platform that a sub-state that would have the lowest latency is enabled (unsupported in POWER8, maps to 0b10) 10 = Indicates to the platform that a sub-state that might have a medium exit latency is enabled (POWER8: Fast Winkle) 11 = Indicates to the platform that a sub-state that might have higher exit latency is enabled (POWER8: Deep Winkle)
44:47	ROX	RESERVED_PPMICR_2: reserved

Register Name	<i>PPMCR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_CONTROL_REG
Address	000000001B0F0159 (PCB)
Attributes	
Description	Provides read access to the PMCR register shadow in the PCBS, typically owned (written) by the hypervisor. Writes are conditioned on the setting of PMGP1[pm_spr_override_en].

Bits	PCB	Field Mnemonic: Description
0:7	RWX	GLOBAL_PSTATE_REQ: global Pstate request from hypervisor (or OCC)
8:15	RWX	LOCAL_PSTATE_REQ: local Pstate request from hypervisor or OCC
16	RWX	AUTO_OVERRIDE0_PSTATE_LIMIT_EN: automatic override Pstate 0 (for low activity detection) is enabled, if asserted

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Bits	PCB	Field Mnemonic: Description
17	RWX	AUTO_OVERRIDE1_PSTATE_LIMIT_EN: automatic override Pstate 1 (reserved for future use) is enabled, if asserted
18:23	RWX	RESERVED_PPMCR: reserved
24:31	RWX	AUTO_OVERRIDE_PSTATE0: automatic override Pstate 0 (for low activity detection)
32:39	RWX	AUTO_OVERRIDE_PSTATE1: automatic override Pstate 1 (reserved for future use)

Register Name	<i>Control Register That Is Written By PMC Sequencer</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_PMC_VF_CTRL_REG
Address	000000001B0F015A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PGLOBAL_ACTUAL: global actual Pstate
8:15	RW	MAXREGVCS: maximum regulation point for Vcs, Bit 0 is reserved, bits 1 to 7 are in iVID format
16:23	RW	MAXREGVDD: maximum regulation point for Vdd, Bit 0 is reserved, bits 1 to 7 are in iVID format
24:31	RW	EVIDVCS_EFF: eff. external voltage ID for Vcs in iVID format, Bit 0 is reserved
32:39	RW	EVIDVDD_EFF: eff. external voltage ID for Vdd in iVID format, Bit 0 is reserved

Register Name	<i>Undervolting Register For PCBS</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_UNDERVOLTING_REG
Address	000000001B0F015B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PUV_MIN: minimum Pstate for which undervolting is allowed
8:15	RW	PUV_MAX: maximum Pstate for which undervolting is allowed
16:21	RW	KUV: this value indicates how many Pstate ticks a voltage request is undervolted (clipped with Puv_min). Note that the Kuv value is signed

Register Name	<i>PPSIBR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_INDEX_BOUND_REG
Address	000000001B0F015C (PCB)
Attributes	
Description	Enables setting the minimum and maximum Pstate that is supported as a pointer into the local Pstate table (which has entries from 0 to 127).

Bits	PCB	Field Mnemonic: Description
0:7	RW	LPSI_MIN: this Pstate index is the index that corresponds to array entry 0. Note that the index domain is obtained by adding 128 to a Pstate, thus, the value is unsigned.
8:14	RW	LPSI_ENTRIES_MINUS_1: this dial contains the value of the number of entries in the Pstate table minus 1

Register Name	<i>PPMBR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_BOUNDS_REG
Address	000000001B0F015D (PCB)
Attributes	
Description	The PPMBR enables setting the Pstate bounds that are managed by the OCC. If dial Enable_pmc_pmax_sync_notification is set, firmware must wait after each write to this register until PMC has received the Pmax Sync Interrupt. If a write happens to this register while the previously scheduled Pmax Sync Interrupt has not yet left the PCBS, the error TBD will be set.

Bits	PCB	Field Mnemonic: Description
0:7	RW	PMIN_CLIP: minimum Pstate allowed for this chiplet
8:15	RW	PMAX_CLIP: maximum Pstate allowed for this chiplet (has to be greater or equal to Pmin_clip)

Register Name	<i>PPTCR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_CTRL_REG
Address	000000001B0F015E (PCB)
Attributes	
Description	The PPTCR controls the address for writing the local Pstate Table Array (all 96 words are accessible). Note that the protocol requires this register to be set up with the Pstate address first, if a read or a write of the Pstate array is intended, to make sure that the initial address is set correctly. The register PPTR must always be written or read afterward. Note that any access to the PPTR auto-increments this register.

Bits	PCB	Field Mnemonic: Description
0:6	RWX	PSTATE_TABLE_ADDRESS: This is the address of the Pstate table in PCBS, which is auto-incremented after any access to the PTLR.

Register Name	<i>PPTR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_REG
Address	000000001B0F015F (PCB)
Attributes	
Description	The PPTR controls the data to be written into the Pstate table and returns the data for a read of the Pstate table. Note that the protocol requires for a write to set this register up after first setting up PPTCR (if the user does not rely on the auto-increment function of the address). For a read of the Pstate table, this register must be read after first setting up PPTCR as well (again if the auto-increment feature of the address is not used). Any access to this register auto-increments the Pstate_table_address by 1. Note also that the read functionality of this register is only functional if PIVRMCSR[ivrm_fsm_enable] = 0. The write functionality works in any case.

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Bits	PCB	Field Mnemonic: Description
0:63	RW	pstate_data This is the field for data bits 0 to 63

Register Name	PPSTR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_STEP_TARGET_REG
Address	000000001B0F0160 (PCB)
Attributes	
Description	The PPSTR provides read access to several intermediate values in the Pstate computation pipeline. Writes Are conditioned on the setting of PMGPO[enable_OCC_ctrl_for_local_Pstate_eff_req].

Bits	PCB	Field Mnemonic: Description
0:7	RWX	LOCAL_PSTATE_EFF_REQ: this field represents the effective local Pstate request right before the clipping with Pmin and Pmax if enable_OCC_ctrl_for_local_Pstate_eff_req=0 then the hardware controls this dial, that updates every cycle if enable_OCC_ctrl_for_local_Pstate_eff_req=1 then OCC is in control and can write this field to control the effective local Pstate request that will eventually propagate through the downstream logic and determine the Local PState Actual. Note: if no write to this register is performed, the currently established value is maintained stable forever.
8:15	ROX	LOCAL_PSTATE_TARGET: This field is the target Pstate of a complete Pstate change that is performed in smaller steps
16:23	ROX	LOCAL_CORE_PSTATE_STEP_TARGET: this field represents the intermediate value that is about to be established as the next Local Pstate Actual after completing one step in the process of the transition towards the 'local_Pstate_target' the new voltage, frequency, and clock resonance setting
24:31	ROX	LOCAL_ECO_PSTATE_STEP_TARGET: this field represents the intermediate value that is about to be established as the next Local Pstate Actual after completing one step in the process of the transition towards the 'local_Pstate_target' the new voltage, frequency, and clock resonance setting

Register Name	Read-Only Status Register For DPLL And For Debugging (PDSR)
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_DPLL_STATUS_REG
Address	000000001B0F0161 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:14	ROX	DPLL_FF_FREQOUT: frequout output from DPLL (current frequency - bits 2 to 10 correspond to the same scale as the 9 bits of frequin (which need to be multiplied with our frequency step to get the real frequency), the remaining bits just provide a higher accuracy)
15	ROX	DPLL_FREQU_CHANGE: DPLL Frequency change (pin of DPLL without filter)
16	ROX	DPLL_STATUS_SPARE_BIT1: Spare bit.
17	ROX	PMAX_SYNC_PENDING: gets asserted, if the logic has a Pmax sync interrupt outstanding that will be eventually sent to PMC when the Pmax sync criterion is met
18	ROX	GA_ACK_PENDING: gets asserted, if the logic has a global actual Pstate update acknowledgment interrupt outstanding that will be eventually sent to PMC when the GA ack criterion is met
19:26	ROX	CAPPED_GLOBAL_PSTATE_REQ: corresponds to the capped global Pstate request that is presented as Pstate interrupt and send to PMC

Bits	PCB	Field Mnemonic: Description
27	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT2: DPLL runs at Fmax and CPM bit 2 is set. Note that this bit and the following 2 bits indicate, that the CPMs would allow the DPLL to run faster than Fmax.
28	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT3: DPLL runs at Fmax and CPM bit 3 is set
29	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT4: DPLL runs at Fmax and CPM bit 4 is set
30	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT2: DPLL runs at Fmin and CPM bit2 is zero. Note that this bit and the following 2 bits indicate, that the CPMs indicate, that the DPLL should run slower than the currently established Fmin.
31	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT1: DPLL runs at Fmin and CPM bit1 is zero
32	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT0: DPLL runs at Fmin and CPM bit0 is zero
33	ROX_CLRPAR T	DPLL_FASTER_THAN_FMAX_PLUS_DELTA1: The DPLL indicated that it ran once faster than Fmax+dpll_char_delta1
34	ROX_CLRPAR T	DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2: The DPLL indicated that it ran once slower than Fmin-dpll_char_delta2
35:48	ROX	DPLL_MAX_FREQOUT_AFTER_LAST_READ: This dial indicates the maximum DPLL frequout value after the last read of this register (only 14 MSBs)
49:62	ROX	DPLL_MIN_FREQOUT_AFTER_LAST_READ: This dial indicates the minimum DPLL frequout value after the last read of this register (only 14 MSBs)

Register Name	<i>The PIVRMVCR0 Controls The Voltage Stepping Delays</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG0
Address	000000001B0F0162 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	IVRM_REQ_PSTATE_STEPDELAY_RISING: Requested Internal Pstate Baby Step Delay - Rising Step. Delay before allowing the next step for a rising Pstate Transition. This dial and ivrm_req_Pstate_stepdelay_lowering allow for differing delays for the two directional transitions if necessary. In 100ns units as established by scan dial ivrm_100ns_value
8:15	RW	IVRM_REQ_PSTATE_STEPDELAY_LOWERING: Requested Internal Pstate Baby Step Delay - Lowering Step. Delay before allowing the next step for a lower Pstate Transition. This dial and ivrm_req_Pstate_stepdelay_rising allow for differing delays for the two directional transitions if necessary. In 100ns units as established by scan dial ivrm_100ns_value

Register Name	<i>The PIVRMVCR1 Controls The Voltage Stepping Delays</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG1
Address	000000001B0F0163 (PCB)
Attributes	
Description	

Registers Specification

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Bits	PCB	Field Mnemonic: Description
0:7	RW	IVRM_STABILIZE_DELAY_RUN: Stabilization Delay - Run Time Delay to allow a rail to stabilize upon a baby step while the region is operational. In 100ns units as established by scan dial ivrm_100ns_value
8:15	RW	IVRM_STABILIZE_DELAY_IDLE: Stabilization Delay - Idle Transition Delay to allow a rail to stabilize upon a baby step during an idle transition where the activity in the region is quiesced. In 100ns units as established by scan dial ivrm_100ns_value
16:23	RW	IVRM_PFSTR_PROP_DELAY: PFET Strength Propagation Delay Time from PFET Strength values being launched till PFET Strength Valid is asserted. In order to ensure like rails across domains (Core VDD<>ECO VDD, Core VCS<>ECO VCS) are in sync during operational mode, this time value applies to all rails across the domains. This parameter allows for PFET Strength values to settle before PFET Strength Valid is sampled in the Uregs. The value set must the maximum delay for the worst rail timing and must allow for any metastability settling (for example, normally 2-3 cycles for single signals in an asynch handshake interface)
24:31	RW	IVRM_PFSTRVALID_PROP_DELAY: PFETStrength Valid Propagation Delay Time from ivrm_pfstr_prop_delay expiring to where PFET Strength Valid is deasserted. The value is the maximum of a) the minimum pulse width required for PFETStrength Valid and b) the propagation of PFETStrength Valid through (or enough of) the daisy chain. In order to ensure like rails across domains (Core VDD<>ECO VDD, Core VCS<>ECO VCS) are in sync during operational mode, this time value applies to all rails across the domains and thus must be the set to the value of the worst (slowest) rail. The minimum pulse width cannot be violated. The propagation delay can be tuned for more aggressive timing (for example, de-assert before the actual propagation is complete). Measured in prv_nclk cycles. The min delay is 2 cycles. Additional delay can be configured with the following settings 0x00 = No additional delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks
32:39	RW	IVRM_VPUMP_POWERON_TIME: iVRM (VRreg and UReg) - Vpump Power On Time Time necessary for the distributed internal VRM macro circuits to power on. Same delay is required for power on voltage pump circuit. Both delays are in the 8us range. In 100ns units as established by scan dial ivrm_100ns_value
40:47	RW	IVRM_BYPASS_DELAY: iVRM Bypass Propagation Delay Delay time for bypass_b signal propagation. Measured in prv_nclk cycles Target: 50ns 0x00 = No delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks

Bits	PCB	Field Mnemonic: Description
48:55	RW	PFET_VPUMP_ENABLE_DELAY: PFET and Vpump Enable Propagation Delay Delay time for PFET enable and vpump enable signal propagation. Target: 130ns Measured in prv_nclk cycles 0x00 = No delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks
56:62	RW	IVRM_VID_VOUT_THRESHOLD: VID threshold If the output voltage (Vout) is targeting a value below this threshold the slow PFET can backed off from its normal drive strength so as to reduce the ripple at these lower voltage conditions

Register Name	POHR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_OCC_HEARTBEAT_REG
Address	000000001B0F0164 (PCB)
Attributes	
Description	Controls the behavior of the OCC heartbeat function.

Bits	PCB	Field Mnemonic: Description
0:7	RW	occ_heartbeat_time 'OCC Heartbeat Time Value' " 'This field defines the number of ~64us hang timer pulses in which a a PCB read or write of the heartbeat trigger register (of which the offset is specified by dial occ_heartbeat_reg_addr_offset) is not detected that will constitute the loss of the OCC heartbeat. If occ_heartbeat_en is set and upon this loss detection, POHBR[psafe] is forced and, if enabled, the error TBD is activated ' ' 0x00 - unsupported, causes undefined behavior' 0x01 - 64us +0/-1us' 0x02 - 128us +0/-1us' ...' 0xFF - 16320us +0/-1us 16.3ms' " 'Upon the 64us hang pulse, the decremter ticks. if the decremter reaches x00, the heartbeat loss event is triggered.' "
8	RW	occ_heartbeat_enable 'OCC Heartbeat Timer Enable' " '0 = Disable the OCC Heartbeat function. Lack of accesses to the register defined by the dial occ_heartbeat_reg_addr_offset does not result in heartbeat loss events to be triggered (no FIRs set nor Safe mode entry).' " '1 = Enable the OCC Heartbeat function. '
9:16	RW	occ_heartbeat_reg_addr_offset This dial allows to configure the address offset within the PCBS power management entity of the register, that will regularly reset the heartbeat timer (which is called heartbeat trigger register). The address offset is 0x100 plus the value of this dial.
17:24	RW	Psafe 'Pstate Safe' " 'This field establishes the Pstate that the core chiplet will take on if: 'psafe <= PMSR[global_actual_pstate] 'AND any of the following conditions are true:' 'Loss of OCC Heartbeat if occ_heartbeat_en is set' 'PMGP0[force_safe_mode] is set' " 'If psafe > PMSR[global_actual_pstate], the global_actual_pstate is forced.' " 'The value of Psafe needs to be at or below the nominal Pstate to make sure safe operation of all chiplets. '

Register Name	PRCCR0 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG 0
Address	000000001B0F0165 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function.

Registers Specification

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Bits	PCB	Field Mnemonic: Description
0	ROX	RESCLK_DIS: Resonant Clock Enable Master enable of all resonant clocking functions. This dial can be set by setting GP3(22) and can not be set in this PCBS_resonant_Clock_Control_Reg0. 1 = Resonant Clock function is disabled. Default values (0) for resclk_value, resclk_core_sync_value, csb_eco_sync_value 0 = Resonant Clock Control hardware is enabled (the mode is defined by dial resclk_control_mode)
1	RW	RESCLK_CONTROL_MODE: Resonant Clock Control Mode Defines the control means enabled when resclk_dis is not set. 0 = Pstate band hardware mechanism enabled 1 = Manual mode enabled (Firmware mode) If this bit is set to 0, the hardware control mechanism that manages the transition across the Resonant Bands is enabled. If this bit is set to 1, the automatic Pstate band hardware mechanism is disabled and the Firmware is in control of all values of the dial resclk_value, resclk_core_sync_value, csb_eco_sync_value. Firmware must ensure that frequency changes will not cross resonant bands or machine failures may result. resclk_value represents the values for clock sector buffer strength, inductor switch strength and high inductor enable. Firmware must ensure the correct stepping in/out the different bands and propagation of the values (resclk_value) to the core/eco (resclk_core_sync_value / csb_eco_sync_value).
2:4	RW	RESCLK_SYNC_PW: Resonant Clock Sync Pulse Width Number of nest/4 cycles to assert the clock sync signal. This value must be high enough to ensure capture and propagation across the asynchronous chiplet boundary.
5:11	RW	RES_SYNC_DELAY_CNT: Resonant Clock Sync Delay Number of nest/4 cycles wait after the launch of the resclk_value (csb and inductor) before launching the sync to allow these to be captured. This value must be high enough to ensure full propagation to the input of the clock sector buffers and inductor switches.
12:26	RW	RES_CSB_STR_INSTR_LO: Resonant Clock Sector Buffer Strength Instruction - Low Band Mask value that determines whether, during a fixed 15 step sequence, the res_csb_str(0:3) is to be decremented/incremented in entering/exiting the Low Band. During resonant clock Entry, res_csb_str(0:3) decremented by the value pattern from 0 down to 14. During resonant clock Exit, res_csb_str(0:3) incremented by the value pattern from 14 up to 0.
27:41	RW	RES_CSB_STR_INSTR_HI: Resonant Clock Sector Buffer Strength Instruction - High Band Mask value that determines whether, during a fixed 15 step sequence, the res_csb_str(0:3) is to be decremented/incremented in entering/exiting the High Band. During resonant clock Entry, res_csb_str(0:3) decremented by the value pattern from 0 down to 14. During resonant clock Exit, res_csb_str(0:3) incremented by the value pattern from 14 up to 0.

Register Name	PRCCR1 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG 1
Address	000000001B0F0166 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function. Writes are conditioned.

Bits	PCB	Field Mnemonic: Description
0:7	RW	FULL_CSB_PS: Full Clock Sector Buffer Pstate Pstate defining the maximum point where the clock sector buffer must be driven to full strength. This allow clocks to be distributed at low Vmin levels. FW needs to make sure that no overlaps occur with bands 2 or 3.
8:15	RW	RES_LOW_LOWER_PS: Low Frequency Resonant Lower (LFRLow) Pstate Pstate defining the lower frequency of the Low Resonant Frequency Band. FW needs to make sure that no overlap occurs with band 0.



Bits	PCB	Field Mnemonic: Description
16:23	RW	RES_LOW_UPPER_PS: Low Frequency Resonant Upper (LFRUpper) Pstate Pstate defining the upper frequency of the Low Resonant Frequency Band. Note that if an overlap occurs with band 3, the hardware behavior is undefined.
24:31	RW	RES_HIGH_LOWER_PS: High Frequency Resonant Lower (HFRLow) Pstate Pstate defining the lower frequency of the High Resonant Frequency Band. Note that if an overlap occurs with band 2, the hardware behavior is undefined.
32:39	RW	RES_HIGH_UPPER_PS: High Frequency Resonant Upper (LFRUpper) Pstate Pstate defining the upper frequency of the High Resonant Frequency Band. This value needs to be greater or equal to high_res_lower_ps.
40:43	RW	NONRES_CSB_VALUE_TI: Clock Sector Buffer Table Index for non-resonant state Table Index into Clock Sector Buffer Table for the nominal, non-resonant state.
44:47	RW	FULL_CSB_VALUE_TI: Clock Sector Buffer Table Index for full CSB value Table Index into Clock Sector Buffer Table for the full CSB strength value.
48:56	RWX	RESCLK_VALUE: Output register driving the 9 bit resclk_value In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current resclk_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. The value in this register represents the following concatenation: csb_str_value(0:3) sw_str(0:3) hi_induct_en.
57	RWX	RESCLK_CORE_SYNC_VALUE: Output register driving the resclk_core_sync signal In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current resclk_core_sync_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. This bit is supposed to be used in order to create a SCOM-controlled pulse to force an update of the resclk propagation registers. A 1 enables the synchronous update, a 0 disables it. Suggested use of this bit is to set it to 1 and then set it back to 0 to create a (long) update pulse.
58	RWX	CSB_ECO_SYNC_VALUE: Output register driving the csb_eco_sync signal In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current csb_eco_sync_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. This bit is supposed to be used in order enable the ECO domain to participate in clock sector buffer strength changes, when switching from nominal strength to full CSB strength. A 1 enables the ECO domain, a 0 disables it from seeing a CSB strength update.

Register Name	<i>PRCCR1 Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_STATUS_REG
Address	000000001B0F0167 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function.



Registers Specification

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Bits	PCB	Field Mnemonic: Description
0	ROX	RESCLK_STATE: Resonant Clock State 0 = Resonant Clocking inactive 1 = Resonant Clocking active Valid if resclk_inprogress = 0. Hardware sets this bit to the right value at the completion of the transition into and out of resonance mode.



Bits	PCB	Field Mnemonic: Description
1	ROX	RES_HI_INDUCT_EN: Resonant High Inductor Enable Valid if resclk_inprogress = 0. This dial provides the current value being propagated. 0 = Resonant Clock mode not active 1 = Resonant Clock mode active
2	ROX	RESCLK_INPROGRESS: Resonant Clock Transition in Progress This bit is set by hardware while a transition is in progress and will be reset by hardware when the operation is complete.
3	ROX	RESCLK_FULL_CSB: Full CSB Clock State 0 = Full CSB Clocking inactive 1 = Full CSB Clocking active Valid if resclk_inprogress = 0. Hardware sets this bit to the right value at the completion of the transition into and out of full CSB mode respectively.

Register Name	<i>PLPFTCR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_CONTROL_REG
Address	000000001B0F0168 (PCB)
Attributes	
Description	Allows firmware to configure the modes that are used for the PCBS Local Pstate Frequency Target Status Register.

Bits	PCB	Field Mnemonic: Description
0:2	RW	DELAY_TIME: This field encodes the delay between the time a Local Actual Pstate change modifies the input to the DPLL and the time frequency acquisition begins to allow the hardware to ignore the frequency transition of the DPLL in order to get better frequency measurements. This field encodes a delay of ~1us to ~128us in power of 2 selects. The delay is defined by $2^{**}delay\_time$ in us. Note that the hardware uses multiples of the slow hang pulse that is running at 1us.
3	RW	RECORD_TRANSITIONS: This bit indicates whether the LPFTSR records events that correspond to Local Actual Pstate changes (and therefore may include DPLL slewing effects.) One usage model would set the periodic sample_time defined by the dial OHA_MODE_REG[tod_pulse_count_match_val] to a time less than the worst-case DPLL slew time but then ignore Pstate transitions because they might include DPLL slew effects.
4:18	RW	MULTIPLIER: This 15-bit unsigned constant is multiplied by the DPLL frequency code (9 bits) implied by the Local Actual Pstate to yield the 24-bit frequency target measured in PCBS-PM clock cycles (core clock / 2). Assuming times in seconds and frequencies in Hz, firmware should set this constant to: $(DPLL\_Frequency\_Code\_Step\_Hz * Sample\_Time\_Seconds) / 2$
19	RW	ENABLE_LPFT_FUNCTION: This is the enable bit to enable the local Pstate frequency target function. A '1' enables the function, a '0' disables it (the value can be changed at any time).

Register Name	<i>PLPFTSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_STATUS_REG
Address	000000001B0F0169 (PCB)
Attributes	
Description	Allows firmware to observe local actual Pstate realized frequencies.

Registers Specification

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Bits	PCB	Field Mnemonic: Description
0	ROX_CLRPART	VALID: If this bit is set then all of the remaining fields of this register are valid. This bit is cleared whenever the register is read or after a local actual Pstate change occurs, and is will be set whenever the hardware completes a valid sample. If firmware reads this register and the valid bit is not set, then it indicates that the Local Pstate target frequency acquisition logic has not been able to complete a frequency acquisition for any Local Actual Pstate change since the last time the LPFTSR was read. This could be due to either of the following factors: 1. Firmware is sampling the LPFTSR faster than the time implied by the sample time defined in OHA by the dial OHA_MODE_REG[tod_pulse_count_match_val] field
1	ROX	CPM_DPLL: If the valid bit is set, then if cpm_dpll is set it indicates that the event recorded by this register was due to a Local Actual Pstate implemented by the DPLL running in CPM-DPLL mode, otherwise the value of this bit is undefined. If the valid bit is not set, this bit is undefined.
2	ROX	IVRM: If the valid bit is set, then if ivrm is set it indicates that the event recorded by this register was due to a Local Actual Pstate whose voltage was set locally by the iVRM operating entirely in regulation mode. If the valid bit is not set, this bit is undefined.
3	ROX	TRANSITION: If the valid bit is set, then if transition is set it indicates that during the observation period a Local Pstate Actual change has occurred, and any performance delta may be due to DPLL frequency slewing. If the valid bit is not set, this bit is undefined
4	ROX	STABLE: If stable is set it indicates that the DPLL input frequency has been stable since the last time the PLPFTSR was read. This bit is set whenever the PLPFTSR is read, and cleared whenever the Fmax input of the DPLL changes. This bit is always valid, regardless of the state of the valid bit. If the PLPFTSR is read on the same cycle a frequency changes then the stable bit is cleared. This bit helps firmware better understand how to interpret the information contained in the PLPFTSR. (Note that this bit should have an attribute ROX_SETPART, but this is not supported by regchk.)
5:28	ROX	DELTA: If the valid bit is set then this is the 24-bit signed difference Measured Cycles - Target Cycles for the event captured by this register. If the valid bit is not set, this dial is undefined.
29:52	ROX	CUMULATIVE: This field records the 24-bit cumulative (signed) delta for all valid samples taken since this field was cleared. Writing any value to this register clears this field. Note that it should have an attribute WOX_CLRPART, but this is not supported by regchk/figtree.
53:60	ROX	PSTATE: If the valid bit is set then this is the Local Actual Pstate of the frequency acquisition that had the minimum (signed) delta of any valid sample taken since the last time the LPFTSR was read. If the valid bit is not set, then this field is undefined.

Register Name	PFSMM1/2 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR1_REG
Address	000000001B0F0170 (PCB)
Attributes	
Description	Facilitates debug by providing insight into the internal FSM states of the PCB-slave power-management unit. For expert use only. Coding according to VHDL design.

Bits	PCB	Field Mnemonic: Description
0:6	ROX	BABYSTEP_MAIN_FSM: Main Babystep FSM (mfsm_lt)
7:11	ROX	BABYSTEP_SLAVE_FSM: Babystep Slave FSM (sfsm_lt)
12:16	ROX	CORE_RAILSTEPPER_MAIN_FSM: Main Core Railstepper FSM (mrsfsm_lt)
17:21	ROX	ECO_RAILSTEPPER_MAIN_FSM: Main ECO Railstepper FSM (mrsfsm_lt)



Bits	PCB	Field Mnemonic: Description
22:25	ROX	CORE_RAILSTEPPER_SUB_FSM: Core Railstepper Sub-FSM (srsfsm_lt)
26:29	ROX	ECO_RAILSTEPPER_SUB_FSM: ECO Railstepper Sub-FSM (srsfsm_lt)
30:34	ROX	CORE_RAILSTEPPER_BYP_FSM: Core Railstepper Bypass FSM (byp_fsm_lt)
35:39	ROX	ECO_RAILSTEPPER_BYP_FSM: ECO Railstepper Bypass FSM (byp_fsm_lt)
40:45	ROX	IVRM_CORE_VDD_SEQUENCER_FSM: Core iVRM Sequencer for Vdd (ivrm_fsm_lt)
46:51	ROX	IVRM_CORE_VCS_SEQUENCER_FSM: Core iVRM Sequencer for Vcs (ivrm_fsm_lt)
52:57	ROX	IVRM_ECO_VDD_SEQUENCER_FSM: ECO iVRM Sequencer for Vdd (ivrm_fsm_lt)
58:63	ROX	IVRM_ECO_VCS_SEQUENCER_FSM: ECO iVRM Sequencer for Vcs (ivrm_fsm_lt)

Register Name	<i>Refer To The Description Of PFSMM1</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR2_REG
Address	000000001B0F0171 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:6	ROX	RESCLK_BAND_FSM: Band Sequencer for resonant clocking (band_fsm_lt)
7:10	ROX	RESCLK_LOWRES_FSM: Low Resonant Clocking sequencer (lowres_fsm_lt)
11:14	ROX	RESCLK_HIGHRES_FSM: High Resonant Clocking sequencer (highres_fsm_lt)
15:18	ROX	RESCLK_FULLCSB_FSM: Full-CSB Resonant Clocking sequencer (fullcsb_fsm_lt)
19:22	ROX	RESCLK_UPDATE_FSM: Resonant Clocking Update sequencer (update_fsm_lt)
23:29	ROX	IDLE_TRANSITION_FSM: Idle State Sequence FSM (ifsm_lt)
30:37	ROX	Peco_step_target_uv Current ECO Step Target Pstate (different from Plocal_actual for undervolting)
38:45	ROX	Pcore_step_target_uv Current core Step Target Pstate (different from Plocal_actual for sleep and undervolting)

Register Name	<i>Protect Mode Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.PROTECT_MODE_REG
Address	000000001B0F03FE (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	READ_PROTECT_ENABLE: Enable read protection
1	RW	WRITE_PROTECT_ENABLE: Enable write protection

Register Name	<i>Atomic Lock Register</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX11.TP_PCB_SLAVE_INST.ATOMIC_LOCK_REG	
Address	000000001B0F03FF (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	RW	ATOMIC_LOCK_ENABLE: Enable atomic lock
1:4	ROX	ATOMIC_ID: Atomic ID

Register Name	<i>Contains The Slave's Primary Address</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.PRIMARY_ADDRESS_REG	
Address	000000001C0F0000 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RO	Reserved field (Access type is primary_address)

Register Name	<i>Multicast Group 1</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.MULTICAST_GROUP_1	
Address	000000001C0F0001 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST1_GROUP: multicast group1 setting

Register Name	<i>Multicast Group 2</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.MULTICAST_GROUP_2	
Address	000000001C0F0002 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST2_GROUP: multicast group2 setting



Register Name	Multicast Group 3	
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.MULTICAST_GROUP_3	
Address	000000001C0F0003 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST3_GROUP: multicast group3 setting

Register Name	Multicast Group 4	
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.MULTICAST_GROUP_4	
Address	000000001C0F0004 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST4_GROUP: multicast group4 setting

Register Name	Timeout Select Register	
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.TIMEOUT_REG	
Address	000000001C0F0010 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:1	RW	Reserved field (Access type is int_timeout)

Register Name	Assist Interrupt Register	
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.ASSIST_INTERRUPT_REG	
Address	000000001C0F0011 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is attn)
1	ROX	Reserved field (Access type is recov)
2	ROX	Reserved field (Access type is xstop)

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Register Name	GP3 Register (NA In PERV CPLT)
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.GP3_REG
Address	000000001C0F0012 (PCB) 000000001C0F0013 (PCB1) 000000001C0F0014 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset
2	RWX	RWX_WAND	RWX_WOR	GLSMUX_RESET: Glsmux reset for test purpose and stuck active mesh protection. Notice no clocks in the EX if this bit is set.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Put the DPLL in test mode.
4	RWX	RWX_WAND	RWX_WOR	PLL_RST: Put PLL in reset state.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYP: Enable PLL bypass.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pcb_access)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	PM_PI_DECODE: Test override for power management. EX chiplet only.
22	RWX	RWX_WAND	RWX_WOR	RESCLK_DIS: Resonant clocking disable.
23:25	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave will report 'Chiplet Offline'.
27	RWX	RWX_WAND	RWX_WOR	TP_LVLTRANS_FENCE: Electrical winkel fence. Mainly used by power management.
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.
29:31	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)



Register Name	<i>Skew Adjust Data</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.CLK_ADJ_REG	
Address	000000001C0F0015 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:15	ROX	

Register Name	<i>Clk Ajust Config</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.CLK_ADJ_SET	
Address	000000001C0F0016 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:31	RW	CLK_ADJ_SET_REG: Clk adj config

Register Name	<i>Vital Scan Out</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.VITAL_SCAN_OUT	
Address	000000001C0F0017 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	

Register Name	<i>Chiplet Heartbeat Register</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.HEARTBEAT_REG	
Address	000000001C0F0018 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	HEARTBEAT_DEAD: Chiplet heartbeat not detected

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Register Name	<i>Lock Indications From PLLs</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.PLL_LOCK_REG
Address	000000001C0F0019 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	ROX	Reserved field (Access type is lock)

Register Name	<i>Attn Interrupt</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.ATTN_INTERRUPT_REG
Address	000000001C0F001A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is attn)

Register Name	<i>Recov Interrupt</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.RECOV_INTERRUPT_REG
Address	000000001C0F001B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is recov)

Register Name	<i>Xstop Interrupt</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.XSTOP_INTERRUPT_REG
Address	000000001C0F001C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is xstop)



Register Name	<i>Slave Config Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.SLAVE_CONFIG_REG
Address	000000001C0F001E (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	CFG_DISABLE_PERV_THOLD_CHECK: Disable pervasive thold check
1	RW	CFG_DISABLE_MALF_PULSE_GEN: Disable pulse generation for malf alert. Switch back to level
2	RW	CFG_STOP_HANG_CNT_SYS_XSTP: Disable hang counter stop for system xstop
3	RW	CFG_DISABLE_CL_ATOMIC_LOCK: Disable atomic lock for chiplet accesses
4	RW	CFG_DISABLE_HEARTBEAT: Disable check for voltage and gridclock in the chiplet
5	RW	CFG_ZERO_DATA: Sent zero data on any error
6:7	RW	
8:12	RW	ERROR_MASK: mask bits for slave error reporting
13:15	RW	

Register Name	<i>Error Capture Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.ERROR_REG
Address	000000001C0F001F (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX_WCLEA R	CE_ERROR: Correctable error on pcb bus
1:3	RWX_WCLEA R	CHIPLET_ERRORS: Errors reported by chiplet 000 = no error 001 = XSCOM command blocked due pending errors 010 chiplet offline 011 partial good 100 invalid address / address error / bad access type 101 clock error 110 parity error / received unexpected packet / wrong packet number 111 timeout This register is for debug purposes only. It only holds meaningful data if it is cleared after each error.
4	RWX_WCLEA R	PARITY_ERROR: Parity error on PCB Interface
5	RWX_WCLEA R	DATA_BUFFER_ERROR: Parity error in data buffer
6	RWX_WCLEA R	ADDR_BUFFER_ERROR: Parity error in address buffer
7	RWX_WCLEA R	PCB_FSM_ERROR: Invalid state error in PCB FSM
8	RWX_WCLEA R	CL_FSM_ERROR: Invalid state error in Chiplet FSM
9	RWX_WCLEA R	INT_RX_FSM_ERROR: Invalid state error in interrupt RX FSM
10	RWX_WCLEA R	INT_TX_FSM_ERROR: Invalid state error in interrupt TX FSM

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Bits	PCB	Field Mnemonic: Description
11	RWX_WCLEAR	INT_TYPE_ERROR: Invalid interrupt type
12	RWX_WCLEAR	CL_DATA_ERROR: Parity error on Chiplet Interface
13	RWX_WCLEAR	INFO_ERROR: Parity error on Chiplet info lines
14	RWX_WCLEAR	UNUSED_0:
15	RWX_WCLEAR	CHIPLET_ATOMIC_LOCK_ERROR: Chiplet atomic lock error
16	RWX_WCLEAR	PCB_INTERFACE_ERROR: Error of pcb interface component for the internal endpoint
17	RWX_WCLEAR	CHIPLET_OFFLINE: Heartbeat check indicated that chiplet is offline
18	RWX_WCLEAR	CHIPLET_GRID_SKITTER: Heartbeat check indicated skitter on the chiplet grid
19	RWX_WCLEAR	GP3_REG_PARITY_ERROR: gp3 register parity bad
20	RWX_WCLEAR	ADDRESS_REG_PARITY_ERROR: address register parity bad
21	RWX_WCLEAR	TIMEOUT_REG_PARITY_ERROR: timeout select register parity bad
22	RWX_WCLEAR	CONFIG_REG_PARITY_ERROR: slave config register parity bad
23	RWX_WCLEAR	CLK_ADJ_REG_PARITY_ERROR: clk adj register parity bad
24	RWX_WCLEAR	DIV_REG_PARITY_ERROR: div register parity bad
25:28	RWX_WCLEAR	PLL_UNLOCK_ERROR: unlock from chiplet pll

Register Name	<i>Hang Pulse Generation Register 0.</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.HANG_PULSE_0_REG
Address	000000001C0F0020 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_0: Value of hang pulse 0. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_0: If set to '1', hang pulses are suppressed in case of a xstop



Register Name	<i>Hang Pulse Generation Register 1.</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.HANG_PULSE_1_REG	
Address	000000001C0F0021 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_1: Value of hang pulse 1. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_1: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 2.</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.HANG_PULSE_2_REG	
Address	000000001C0F0022 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_2: Value of hang pulse 2. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_2: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 3.</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.HANG_PULSE_3_REG	
Address	000000001C0F0023 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_3: Value of hang pulse 3. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_3: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 4.</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.HANG_PULSE_4_REG	
Address	000000001C0F0024 (PCB)	
Attributes		
Description		

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Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_4: Value of hang pulse 4. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_4: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 5</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.HANG_PULSE_5_REG
Address	000000001C0F0025 (PCB)
Attributes	
Description	This hang counter is exclusively used to generate the malfunction alert pulse.

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_5: Value of hang pulse 5. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_5: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 6</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.HANG_PULSE_6_REG
Address	000000001C0F0026 (PCB)
Attributes	
Description	This hang counter is exclusively used for heartbeat generation.

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_6: Value of hang pulse 6. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_6: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Divider For Hang Counter Clock</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.PRE_COUNTER_REG
Address	000000001C0F0028 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PRE_COUNTER: Divider for hang counter clock. Divides clock by n+1 (default: n=0)



Register Name		<i>PowerManagement GP0</i>		
Mnemonic		EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PMGPO_REG		
Address		000000001C0F0100 (PCB) 000000001C0F0101 (PCB1) 000000001C0F0102 (PCB2)		
Attributes				
Description				
Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PM_DISABLE: Master Switch for the PowerManagement Macro
1	RWX	WOX_AND	WOX_OR	PMGP0_SPARE_BIT1: spare bit
2	RWX	WOX_AND	WOX_OR	TP_TC_RESTART_CORE_DOMAIN: Kicks off small sequencer in OHA to get chiplet clocks back running for fast sleep without involving PORE. From GP-reg and overridden by PowMan State Machine.
3	RWX	WOX_AND	WOX_OR	DPLL_THOLD: Thold for the DPLL clock domain in the chiplet
4	RWX	WOX_AND	WOX_OR	PERV_THOLD: Thold for the Pervasive clock domain in the chiplet
5	RO	RO	RO	Reserved.
6	RO	RO	RO	Reserved.
7	RWX	WOX_AND	WOX_OR	PM_DPLL_TIMER_ENA: Select a timer instead of the DPLL lock bit for criteria to switch to DPLL. The time is defined by thold_timer_sel.
8	RWX	WOX_AND	WOX_OR	DPLL_LOCK_SENSE: DPLL lock sensitivity control (0=faster lock time, 1=slower lock time)
9	RWX	WOX_AND	WOX_OR	PMGP0_SPARE2: spare bit
10	RWX	WOX_AND	WOX_OR	DPLL_RESET: Reset to DPLL
11	RWX	WOX_AND	WOX_OR	PMGP0_SPARE_BIT11: Spare bit
12:19	RWX	WOX_AND	WOX_OR	DPLL_TESTOUT_CTL: DPLL testout control
20	RWX	WOX_AND	WOX_OR	TP_TC_CACHE2CORE_FENCE: Fence from cache to core domain in EX chiplet
21	RWX	WOX_AND	WOX_OR	TP_TC_CORE2CACHE_FENCE: Fence from core to cache domain in EX chiplet
22	RWX	WOX_AND	WOX_OR	TP_TC_PERVASIVE_ECO_FENCE: Pervasive ECO fence
23	RWX	WOX_AND	WOX_OR	CHKSW_HW257424_DISABLE: Chicken switch for interrupt retry exhausted bug (0=fix enabled, 1=fix disabled)
24:26	RWX	WOX_AND	WOX_OR	TP_CLK_ASYNC_RESET_DC: Clk async reset for three glitchless muxes, and the two clock dividers (bit 0 = master GLM, bit 1 = ECO Div2 and ECO GLM, bit 2= core Div1 and core GLM)
27:29	RWX	WOX_AND	WOX_OR	TP_CLKGLM_SEL_DC: Glitchless Mux Select for primary chiplet clock source (feeding both core and eco clock muxes) 000 = refclk, 001 = DPLL. 100 = Use constant selected by bit 34, else refclk
30	RWX	WOX_AND	WOX_OR	TP_CLKGLM_ECO_SEL_DC: Glitchless Mux Select for eco domain (cache_nclk) grid. 0= follow primary source chosen by previous field: 1 = Use constant selected by bit 34
31	ROX	NC	NC	SPECIAL_WKUP_DONE: Indicates that special wakeup is done, if asserted
32:33	RWX	WOX_AND	WOX_OR	TP_CLKGLM_CORE_SEL_DC: Glitchless Mux Select for core domain (nclk grid) mux. 0b00=primary GLS mux output, 0b10=constant input, 0b01=refclk. Valid transitions are 0b01 <-> 0b00 <-> 0b10, 0b11 is illegal

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
34	RWX	WOX_AND	WOX_OR	TP_CLKGLM_CONST_DC: Constant input available to all three ClkGlm
35:36	RWX	WOX_AND	WOX_OR	THOLD_TIMER_SEL: Selection for the thold transition timer in the IDLE state machine. 0b00=1024 cycles delay, 0b01=512 cycles delay, 0b10=256 cycles delay, 0b11= 128 cycles delay
37	RWX	WOX_AND	WOX_OR	BLOCK_ALL_WAKEUP_SOURCES: Setting this bit will make the PM Slave ignore any Wakeup events (ext. interrupt, malfunction alert, any special wakeup bit). This bit is intended to enable firmware concurrent patch capability. Note: This does NOT block the interrupt from being presented to the processor core. The following procedure is required on changes: 1. Firmware may only set this bit after first setting special wakeup and polling for special wakeup complete (OHA and PCB-slave both in running state with AISS and PM FSMs idle). 2. Firmware may only clear this bit if all special wakeup bits are first cleared.
38	RWX	WOX_AND	WOX_OR	TP_TC_DPLL_TESTMODE_DC: ADPLL test mode
39	RWX	WOX_AND	WOX_OR	PM_SLV_WINKLE_FENCE: Fence off the powered off chiplet in winkle. - Logical fence/hold for pcb_slave and pcb_slave_pm. For electrical fence see bit 23.
40	RWX	WOX_AND	WOX_OR	L3_ENABLE_SWITCH: Setting this bit activates l3_edram_enable if allowed by system configuration GP3(28). Resetting this bit deactivates l3_edram_enable.
41	RWX	WOX_AND	WOX_OR	TP_CPLT_IVRM_REFBYPASS_DC: Signal to iVRM (used to be controlled by scan-only block inside EX, but needs to be driven by VIO domain)
42	RWX	WOX_AND	WOX_OR	CHKSW_HW241939_DISABLE: if this bit is set to 1, the fix for HW241939 (pfet enable SCOM-ability) is disabled
43	RWX	WOX_AND	WOX_OR	CHKSW_HW273115_DISABLE: if this bit is set to 1, the fix for HW273115 (Pga ACK noack issue when the babystepper is in the winkle state) is disabled
44	RWX	WOX_AND	WOX_OR	CHKSW_HW245103_DISABLE: if this bit is set to 1, the fix for HW245103 resonant clocking CSB and SW -bit ordering change is disabled
45	RWX	WOX_AND	WOX_OR	CHKSW_HW257534_DISABLE: if this bit is set to 1, the fix for HW257534 (fencing of errors) is disabled
46	RWX	WOX_AND	WOX_OR	CHKSW_HW259509_ENABLE: if this bit is set to 0, the fix for HW259509 (Pstate change hanging, because of DPLL flock timer in a hung state) is disabled
47	RWX	WOX_AND	WOX_OR	CHKSW_HW260345_DISABLE: if set to 1, this bit disables the HW260345 fix (fix was to make sure that we enter bypass mode for iVRM safe mode without a glitch that could cause Vcs in regulation and Vdd in bypass)
48:49	ROX	NC	NC	WAKEUP_INT_TYPE: (Known to be unreliable and not supported, informational usage only) Type of the last wakeup event that caused an exit from sleep or winkle (excluding nap!), regardless of present state. 0b01: External interrupt. 0b10: Malfunction Alert. 0b11: Special Wakeup. 0b00: chiplet has never fully entered and exited a chiplet-level idle state since IPL of the system. (Note this does not necessarily get updated when the processor core enters an idle state, only if the PCB-Slave enters and then exits the idle state for this chiplet).
50	ROX	NC	NC	DPLL_LOCK: DPLL lock indicator
51	ROX	NC	NC	SPECIAL_WKUP_ALL_SOURCES_ORED: logical OR of all special wakeup sources
52	ROX	NC	NC	REGULAR_WKUP_AVAILABLE: logical OR of external interrupt and malfunction alert

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
53	RWX	WOX_AND	WOX_OR	BLOCK_REG_WKUP_SOURCES: blocks ext. int. and malf. Alert from waking up PCBS (no block possible for PC!)

Register Name	<i>PowerManagement GP1</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PMGP1_REG
Address	000000001C0F0103 (PCB) 000000001C0F0104 (PCB1) 000000001C0F0105 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	SLEEP_POWER_DOWN_EN: Sleep Power Down Enable: When set to 1, causes hardware to automatically reduce voltage to the Core domain when entering Sleep mode. The voltage value for power down is chosen by sleep_power_off_sel (bit 2). When set to 0, a request is sent to the PORE engine for assistance entering Sleep.
1	RWX	WOX_AND	WOX_OR	SLEEP_POWER_UP_EN: Sleep Power Up Enable: When set to 1, enables automated hardware restoration of voltage via PFETs and, if enabled, iVRMs when exiting Sleep mode. If this bit is set to 0 the hardware rely on external means (PORE or equivalent) to restore voltage.
2	RWX	WOX_AND	WOX_OR	SLEEP_POWER_OFF_SEL: Sleep Power Off Select: Selects which voltage level to place the Core domain PFETs upon Sleep entry. 0 = Vret (Fast Sleep Mode), 1 = Voff (Deep Sleep Mode). Depending on the setting of pmicr_latency_en, this bit is controlled with a PCB-write (0) or by the PMICR in the core (1).
3	RWX	WOX_AND	WOX_OR	WINKLE_POWER_DOWN_EN: Winkle Power Down Enable: When set to 1, causes hardware to automatically reduce voltage to the entire Chiplet (both Core and ECO Domains) when entering Winkle mode. The voltage value for power down is chosen by winkle_power_off_sel (bit 5). When set to 0, a request is sent to the PORE engine for assistance entering Winkle.
4	RWX	WOX_AND	WOX_OR	WINKLE_POWER_UP_EN: Winkle Power Up Enable: When set to 1, enables automated hardware PFET enablement when exiting Winkle mode. If this bit is set to 0 the hardware rely on external means (PORE or equivalent) to cause the PFETs to be re-enabled.
5	RWX	WOX_AND	WOX_OR	WINKLE_POWER_OFF_SEL: Winkle Power Off Select: Selects which voltage level to place the Core and ECO domain PFETs upon Winkle entry. 0 = Vret (Fast Winkle Mode), 1 = Voff (Deep Winkle Mode). Depending on the setting of pmicr_latency_en, this bit is controlled with a PCB-write (0) or by the PMICR in the core (1).
6	RWX	WOX_AND	WOX_OR	OHA_WKUP_OVERRIDE_EN: Needs to be 0 for normal operation. If set to 1, the two following dials are used to override the regular and special wakeup signal from PCBS to OHA
7	RWX	WOX_AND	WOX_OR	OHA_PM_WKUP_OVERRIDE: Enablement by 'oha_wkup_override_en' forces the regular wakeup signal to OHA to the value of this bit regardless of presence of an interrupt source.
8	RWX	WOX_AND	WOX_OR	OHA_SPC_WKUP_OVERRIDE: Enablement by 'oha_wkup_override_en' forces the special wakeup signal to OHA to the value of this bit, regardless of the firmware settings.

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
9	RWX	WOX_AND	WOX_OR	ENDP_RESET_PM_ONLY: If asserted, an endpoint reset of all power management-related functions (not the regular PCB slave) is performed. Intended usage is for recovery.
10	RWX	WOX_AND	WOX_OR	DPLL_FREQ_OVERRIDE_ENABLE: override Fmax/Fmin only, if '1', using register FREQ_CTRL_REG
11	RWX	WOX_AND	WOX_OR	PM_SPR_OVERRIDE_EN: PM SPR Override Enable The PPMCR (0xNNNN) and PPMICR (0XXXXX) accesses the register resources that make up the PMCR SPR used by hypervisor to management Pstates. Thus, PCB updates to it are disabled in hardware to prevent collisions. This bit allows ownership of the PMCR to be switched from hypervisor to OCC. This switch is immediate in hardware, thus, firmware must ensure the ownership switch is otherwise communicated. 0 = Disables the writing of the PPMCR (0xNNNN) from the PCB and allows SPR 884 writes (mtspr) to update the register resource. 1 = Enables the writing of the PPMCR (0xNNNN) from the PCB.
12	RWX	WOX_AND	WOX_OR	FORCE_SAFE_MODE: Force Safe Mode 0 = Allow other enabled features to determine the operational Pstate. 1 = Forces the minimum of POHBR[psafe] and PPMSR[global_pstate_actual] Pstate for the core chiplet as the operational frequency.
13	RWX	WOX_AND	WOX_OR	IVRM_SAFE_MODE_EN: Internal VRM Safe Mode Enable 0 = Disable the iVRM safe mode, thus, no automatic actions occur, if an iVRM error happens. 1 = if the iVRMs are enabled (PIVRMCSR[ivrn_en] is set) and Pstates are enabled and if the error defined by dial pcbs_ivrm_gross_or_fine_err occurs, then the railstepper is forced into bypass mode to prevent a voltage-frequency hazard
14	RWX	WOX_AND	WOX_OR	IVRM_SAFE_MODE_FORCE_ACTIVE: Internal VRM Safe Mode Force Dial 0 = the hardware decides whether to activate the iVRM safe mode or not 1 = the iVRM safe mode is forced regardless (this makes only sense if ivrm_fsm_enable=1 and Pstates are enabled)
15	RWX	WOX_AND	WOX_OR	PMICR_LATENCY_EN: Selects how the sleep/winkle latency (which is deep/fast) is controlled. If asserted the PMICR controls the winkle/sleep_power_off_sel in PMGP1, otherwise those bits are controlled via SCOM by OCC.
16	RWX	WOX_AND	WOX_OR	ENABLE_OCC_CTRL_FOR_LOCAL_PSTATE_EFF_REQ: controls, if the HW (for value 0) or OCC (value 1) is in control of the Local Pstate Effective register in PPSTR
17	RWX	WOX_AND	WOX_OR	SERIALIZE_PFET_POWERDOWN: if asserted, the pFET sequencer will sequence the core and the ECO domain one after the other when powering down
18	RWX	WOX_AND	WOX_OR	SERIALIZE_PFET_POWERUP: if asserted, the pFET sequencer will sequence the ECO and the core domain one after the other when powering up
19	RWX	WOX_AND	WOX_OR	DISABLE_FORCE_DEEP_TO_FAST_SLEEP: 0: (normal operation) - If PCB Slave reports a recoverable error or a checkstop, a DEEP sleep operation is forced to FAST. The entries in sleep/winkle_power_off_sel remain unchanged. 1: force to FAST is disabled.



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
20	RWX	WOX_AND	WOX_OR	DISABLE_FORCE_DEEP_TO_FAST_WINKLE: 0: (normal operation) - If PCB Slave reports a recoverable error or a checkstop, a DEEP winkle operation is forced to FAST. The entries in sleep/winkle_power_off_sel remain unchanged. 1: force to FAST is disabled.

Register Name	PFET Control/Status Register For Core And ECO Vdd
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PFVDDCNTLSTAT_REG
Address	000000001C0F0106 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	CORE_VDD_PFET_FORCE_STATE: Core Domain PFET Force State Provides a means for firmware to force the core domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 4:5 = 00 (both core_vdd_pfet_val_override AND core_vdd_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
2:3	RW	ECO_VDD_PFET_FORCE_STATE: ECO Domain PFET Force State Provides a means for firmware to force the ECO domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 6:7 = 00 (both eco_vdd_pfet_val_override AND eco_vdd_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
4	RW	CORE_VDD_PFET_VAL_OVERRIDE: Core Domain PFET Value Override 0 = Override is disabled
5	RW	CORE_VDD_PFET_SEL_OVERRIDE: Core Domain PFET Stage Select Override 0 = Override is disabled
6	RW	ECO_VDD_PFET_VAL_OVERRIDE: ECO Domain PFET Value Override 0 = Override is disabled
7	RW	ECO_VDD_PFET_SEL_OVERRIDE: ECO Domain PFET Stage Select Override 0 = Override is disabled
8	RW	CORE_VDD_PFET_ENABLE_REGULATION_FINGER: Core Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the core_vdd_pfet_enable_value.
9	RW	ECO_VDD_PFET_ENABLE_REGULATION_FINGER: ECO Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the eco_vdd_pfet_enable_value.

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Bits	PCB	Field Mnemonic: Description
10:21	RW	CORE_VDD_PFET_ENABLE_VALUE: Core PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the Core Domain PFET Enables directly. If core_vdd_pfet_val_override = 1, a write to this field sets the state of the core PFET Enables until core_vdd_pfet_val_override is cleared. If core_vdd_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the core_vdd_pfet_valN_slav registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
22:25	RW	CORE_VDD_PFET_SEL_VALUE: Core PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure core_vdd_pfet_valN_slav(0:11) where N is 0 to 11 if core_vdd_pfet_sel_override = 1. If core_vdd_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
26:37	RW	ECO_VDD_PFET_ENABLE_VALUE: ECO PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the ECO PFET Enables directly. If ECO_vdd_pfet_val_override = 1, a write to this field sets the state of the ECO PFET Enables until ECO_vdd_pfet_val_override is cleared. If eco_vdd_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the eco_vdd_pfet_valN_slav registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
38:41	RW	ECO_VDD_PFET_SEL_VALUE: ECO PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure eco_vdd_pfet_valN_slav(0:11) where N is 0 to 11 if eco_vdd_pfet_sel_override = 1. If eco_vdd_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
42:45	ROX	CORE_VDD_PG_STATE: Core power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
46:49	ROX	CORE_VDD_PG_SEL: For debug, contains the actual index n into Core Domain PFET Value [n] SLAT Register set that contains the Core PFET Enable Value currently enabled.
50:53	ROX	ECO_VDD_PG_STATE: ECO Domain power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
54:57	ROX	ECO_VDD_PG_SEL: For debug, contains the actual index n into ECO Domain PFET Value [n] SLAT Register set that contains the ECO PFET Enable Value currently enabled.

Register Name	PFET Sense Register	
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PFSENSE_REG	
Address	000000001C0F0107 (PCB)	
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:11	ROX	TP_CORE_VDD_PFET_ENABLE_SENSE: Not used any more.
12:23	ROX	TP_ECO_VDD_PFET_ENABLE_SENSE: Not used any more.



Bits	PCB	Field Mnemonic: Description
24:35	ROX	TP_CORE_VCS_PFET_ENABLE_SENSE: Not used any more.
36:47	ROX	TP_ECO_VCS_PFET_ENABLE_SENSE: Not used any more.

Register Name	<i>PM Error Summary Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PMERRSUM_REG
Address	000000001C0F0108 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	PM_ERROR: PM Error is present. Intended for use by special PCB multicast to see error state of all chiplets with a single read (via 510F0108 to read all chiplets)

Register Name	<i>PM Error Register:</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PMERR_REG
Address	000000001C0F0109 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_HANG_ERR: Hang during Unassisted Sleep Entry: SLEEP_ENTRY_NOTIFY_PMC state
1	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ASSIST_HANG_ERR: Hang during Assisted Sleep Entry: SLEEP_ENTRY_NOTIFY_PMC_ASSIST state
2	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ERR: Hang during Unassisted Sleep Exit: SLEEP_EXIT_NOTIFY_PMC state
3	ROX	PCBS_SLEEP_EXIT_INVOKE_PORE_ERR: Hang during Assisted Deep Sleep Exit: SLEEP_EXIT_INVOKE_PORE state
4	ROX	PCBS_WINKLE_ENTRY_NOTIFY_PMC_ERR: Hang during Unassisted Winkle Entry: WINKLE_ENTRY_NOTIFY_PMC state
5	ROX	PCBS_WINKLE_ENTRY_SEND_INT_ASSIST_ERR: Hang during Assisted Winkle Entry: WINKLE_ENTRY_SEND_INT_ASSIST state
6	ROX	PCBS_WINKLE_EXIT_NOTIFY_PMC_ERR: Hang during Unassisted Winkle Exit: WINKLE_EXIT_NOTIFY_PMC state
7	ROX	PCBS_WAIT_DPLL_LOCK_ERR: Hang during Unassisted Exit waiting on DPLL: WAIT_DPLL_LOCK state
8	ROX	PCBS_SPARE8_ERR: spare bit, always 0
9	ROX	PCBS_WINKLE_EXIT_SEND_INT_ASSIST_ERR: Hang during Assisted Winkle Exit: WINKLE_EXIT_SEND_INT_ASSIST state
10	ROX	PCBS_WINKLE_EXIT_SEND_INT_POWUP_ASSIST_ERR: Hang during Assisted Winkle Exit: WINKLE_EXIT_SEND_INT_POWUP_ASSIST state
11	ROX	PCBS_WRITE_FSM_GOTO_REG_IN_INVALID_STATE_ERR: write to FSM goto register in invalid state
12	ROX	PCBS_WRITE_PMGP0_IN_INVALID_STATE_ERR: write to PMGP0 in invalid state

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Bits	PCB	Field Mnemonic: Description
13	ROX	PCBS_FREQ_OVERFLOW_IN_PSTATE_MODE_ERR: frequency of DPLL in Pstate mode overflows (Fnom + desired Pstate > 511)
14	ROX	PCBS_ECO_RS_BYPASS_CONFUSION_ERR: ECO railstepper tried to exit Vcs bypass and enter Vdd bypass in one Pstate step (it is not clear, in which order this strange operation should be performed - most likely it should never happen to avoid that Vcs is greater than Vdd)
15	ROX	PCBS_CORE_RS_BYPASS_CONFUSION_ERR: same as previous error, but for core railstepper (it is not clear, in which order this strange operation should be performed - most likely it should never happen to avoid that Vcs is greater than Vdd)
16	ROX	PCBS_READ_LPST_IN_PSTATE_MODE_ERR: read LPST-array while iVRM FSMs are enabled (dial ivrm_fsm_enable asserted)
17	ROX	PCBS_LPST_READ_CORR_ERR: correctable error occurred when reading the LPST
18	ROX	PCBS_LPST_READ_UNCORR_ERR: uncorrectable error occurred when reading the LPST
19	ROX	PCBS_PFET_STRENGTH_OVERFLOW_ERR: overflow occurred when calculating the pFET strength (in final rounding step!)
20	ROX	PCBS_VDS_LOOKUP_ERR: Vds entry not found in lookup table (when performing the linear search!)
21	ROX	PCBS_IDLE_INTERRUPT_TIMEOUT_ERR: idle interrupt timeout in PCB interrupt controller
22	ROX	PCBS_PSTATE_INTERRUPT_TIMEOUT_ERR: PState interrupt timeout in PCB interrupt controller
23	ROX	PCBS_GLOBAL_ACTUAL_SYNC_INTERRUPT_TIMEOUT_ERR: GlobalActualSync Interrupt timeout in PCB interrupt controller
24	ROX	PCBS_PMAX_SYNC_INTERRUPT_TIMEOUT_ERR: PmaxSync Interrupt timeout in PCB interrupt controller
25	ROX	PCBS_GLOBAL_ACTUAL_PSTATE_PROTOCOL_ERR: a write to global actual Pstate register has occurred before the global actual Pstate interrupt has left PCBS
26	ROX	PCBS_PMAX_PROTOCOL_ERR: a write to the Pmax/Pmin register has occurred before the Pmax sync interrupt has left PCB
27	ROX	PCBS_IVRM_GROSS_OR_FINE_ERR: iVRM gross or fine error (details to be found in PCBS_ivrm_Control_Status_Reg)
28	ROX	PCBS_IVRM_RANGE_ERR: iVRM range error (summary bit, details to be found in PCBS_ivrm_Control_Status_Reg)
29	ROX	PCBS_DPLL_CPM_FMIN_ERR: DPLL CPM Fmin error
30	ROX	PCBS_DPLL_DCO_FULL_ERR: DPLL DCO full
31	ROX	PCBS_DPLL_DCO_EMPTY_ERR: DPLL DCO empty
32	ROX	PCBS_DPLL_INT_ERR: DPLL internal error
33	ROX	PCBS_FMIN_AND_NOT_CPMBIT_ERR: dpll_fmin_and_not_cpmbit (ref. to dial cpm_fmin_clip_error_sel on how to configure this)
34	ROX	PCBS_DPLL_FASTER_THAN_FMAX_PLUS_DELTA1_ERR: dpll_faster_than_fmax_plus_delta1 (for characterization, delta1 is configurable with pll_char_delta1)
35	ROX	PCBS_DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2_ERR: dpll_slower_than_fmin_minus_delta2 (for characterization, delta2 is configurable with pll_char_delta2)
36	ROX	PCBS_RESCLK_CSB_INSTR_VECTOR_CHG_IN_INVALID_STATE_ERR: RESCLK CSB instruction vector change while FSMs none idle
37	ROX	PCBS_RESCLK_BAND_BOUNDARY_CHG_IN_INVALID_STATE_ERR: RESCLK Band boundaries change while FSMs none idle
38	ROX	PCBS_OCC_HEARTBEAT_LOSS_ERR: OCC heartbeat loss
39	ROX	PCBS_SPARE39_ERR: spare bit, always 0
40	ROX	PCBS_SPARE40_ERR: spare bit, always 0



Bits	PCB	Field Mnemonic: Description
41	ROX	PCBS_SPARE41_ERR: spare bit, always 0
42	ROX	PCBS_SPARE42_ERR: spare bit, always 0

Register Name	<i>PM Error Mask Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PMERRMASK_REG
Address	000000001C0F010A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_HANG_ERR_MASK: Mask for this error: 1=masked, 0=not masked
1	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ASSIST_HANG_ERR_MASK: Mask for this error: 1=masked, 0=not masked
2	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
3	RW	PCBS_SLEEP_EXIT_INVOKE_PORE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
4	RW	PCBS_WINKLE_ENTRY_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
5	RW	PCBS_WINKLE_ENTRY_SEND_INT_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
6	RW	PCBS_WINKLE_EXIT_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
7	RW	PCBS_WAIT_DPLL_LOCK_ERR_MASK: Mask for this error: 1=masked, 0=not masked
8	RW	PCBS_SPARE8_ERR_MASK: Mask for this error: 1=masked, 0=not masked
9	RW	PCBS_WINKLE_EXIT_SEND_INT_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
10	RW	PCBS_WINKLE_EXIT_SEND_INT_POWUP_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
11	RW	PCBS_WRITE_FSM_GOTO_REG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
12	RW	PCBS_WRITE_PMGPO_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
13	RW	PCBS_FREQ_OVERFLOW_IN_PSTATE_MODE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
14	RW	PCBS_ECO_RS_BYPASS_CONFUSION_ERR_MASK: Mask for this error: 1=masked, 0=not masked
15	RW	PCBS_CORE_RS_BYPASS_CONFUSION_ERR_MASK: Mask for this error: 1=masked, 0=not masked
16	RW	PCBS_READ_LPST_IN_PSTATE_MODE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
17	RW	PCBS_LPST_READ_CORR_ERR_MASK: Mask for this error: 1=masked, 0=not masked
18	RW	PCBS_LPST_READ_UNCORR_ERR_MASK: Mask for this error: 1=masked, 0=not masked
19	RW	PCBS_PFET_STRENGTH_OVERFLOW_ERR_MASK: Mask for this error: 1=masked, 0=not masked
20	RW	PCBS_VDS_LOOKUP_ERR_MASK: Mask for this error: 1=masked, 0=not masked
21	RW	PCBS_IDLE_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
22	RW	PCBS_PSTATE_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
23	RW	PCBS_GLOBAL_ACTUAL_SYNC_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
24	RW	PCBS_PMAX_SYNC_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked

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Bits	PCB	Field Mnemonic: Description
25	RW	PCBS_GLOBAL_ACTUAL_PSTATE_PROTOCOL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
26	RW	PCBS_PMAX_PROTOCOL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
27	RW	PCBS_IVRM_GROSS_OR_FINE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
28	RW	PCBS_IVRM_RANGE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
29	RW	PCBS_DPLL_CPM_FMIN_ERR_MASK: Mask for this error: 1=masked, 0=not masked
30	RW	PCBS_DPLL_DCO_FULL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
31	RW	PCBS_DPLL_DCO_EMPTY_ERR_MASK: Mask for this error: 1=masked, 0=not masked
32	RW	PCBS_DPLL_INT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
33	RW	PCBS_FMIN_AND_NOT_CPMBIT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
34	RW	PCBS_DPLL_FASTER_THAN_FMAX_PLUS_DELTA1_ERR_MASK: Mask for this error: 1=masked, 0=not masked
35	RW	PCBS_DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2_ERR_MASK: Mask for this error: 1=masked, 0=not masked
36	RW	PCBS_RESCLK_CSB_INSTR_VECTOR_CHG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
37	RW	PCBS_RESCLK_BAND_BOUNDARY_CHG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
38	RW	PCBS_OCC_HEARTBEAT_LOSS_ERR_MASK: Mask for this error: 1=masked, 0=not masked
39	RW	PCBS_SPARE39_ERR_MASK: Mask for this error: 1=masked, 0=not masked
40	RW	PCBS_SPARE40_ERR_MASK: Mask for this error: 1=masked, 0=not masked
41	RW	PCBS_SPARE41_ERR_MASK: Mask for this error: 1=masked, 0=not masked
42	RW	PCBS_SPARE42_ERR_MASK: Mask for this error: 1=masked, 0=not masked

Register Name		<i>PM Special Wakeup FSP</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PMSPCWKUPFSP_REG
Address		000000001C0F010B (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RW	FSP_SPECIAL_WAKEUP: Chiplet Special Wakeup for FSP Firmware use. NOTE: protocol is required when setting this bit

Register Name		<i>PM Special Wakeup OCC</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PMSPCWKUPOCC_REG
Address		000000001C0F010C (PCB)
Attributes		
Description		



Bits	PCB	Field Mnemonic: Description
0	RW	OCC_SPECIAL_WAKEUP: Chiplet Special Wakeup for OCC Firmware use. NOTE: protocol is required when setting this bit

Register Name	<i>PM Special Wakeup Hypervisor</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PMSPCWKUPPHYP_REG
Address	000000001C0F010D (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	PHYP_SPECIAL_WAKEUP: Chiplet Special Wakeup for hypervisor Firmware use. NOTE: protocol is required when setting this bit

Register Name	<i>PFET Control/Status Register For Core And ECO Vcs</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PFVCS_CNTLSTAT_REG
Address	000000001C0F010E (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	CORE_VCS_PFET_FORCE_STATE: Core Domain PFET Force State Provides a means for firmware to force the core domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 4:5 = 00 (both core_vcs_pfet_val_override AND core_vcs_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
2:3	RW	ECO_VCS_PFET_FORCE_STATE: ECO Domain PFET Force State Provides a means for firmware to force the ECO domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 6:7 = 00 (both eco_vcs_pfet_val_override AND eco_vcs_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
4	RW	CORE_VCS_PFET_VAL_OVERRIDE: Core Domain PFET Value Override 0 = Override is disabled
5	RW	CORE_VCS_PFET_SEL_OVERRIDE: Core Domain PFET Stage Select Override 0 = Override is disabled
6	RW	ECO_VCS_PFET_VAL_OVERRIDE: ECO Domain PFET Value Override 0 = Override is disabled
7	RW	ECO_VCS_PFET_SEL_OVERRIDE: ECO Domain PFET Stage Select Override 0 = Override is disabled

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Bits	PCB	Field Mnemonic: Description
8	RW	CORE_VCS_PFET_ENABLE_REGULATION_FINGER: Core Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the core_vcs_pfet_enable_value.
9	RW	ECO_VCS_PFET_ENABLE_REGULATION_FINGER: ECO Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the eco_vcs_pfet_enable_value.
10:21	RW	CORE_VCS_PFET_ENABLE_VALUE: Core PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the Core Domain PFET Enables directly. If core_vcs_pfet_val_override = 1, a write to this field sets the state of the core PFET Enables until core_vcs_pfet_val_override is cleared. If core_vcs_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the core_vcs_pfet_valN_slav registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
22:25	RW	CORE_VCS_PFET_SEL_VALUE: Core PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure core_vcs_pfet_valN_slav(0:11) where N is 0 to 11 if core_vcs_pfet_sel_override = 1. If core_vcs_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
26:37	RW	ECO_VCS_PFET_ENABLE_VALUE: ECO PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the ECO PFET Enables directly. If ECO_vcs_pfet_val_override = 1, a write to this field sets the state of the ECO PFET Enables until ECO_vcs_pfet_val_override is cleared. If eco_vcs_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the eco_vcs_pfet_valN_slav registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
38:41	RW	ECO_VCS_PFET_SEL_VALUE: ECO PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure eco_vcs_pfet_valN_slav(0:11) where N is 0 to 11 if eco_vcs_pfet_sel_override = 1. If eco_vcs_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
42:45	ROX	CORE_VCS_PG_STATE: Core power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
46:49	ROX	CORE_VCS_PG_SEL: For debug, contains the actual index n into Core Domain PFET Value [n] SLAT Register set that contains the Core PFET Enable Value currently enabled.
50:53	ROX	ECO_VCS_PG_STATE: ECO Domain power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
54:57	ROX	ECO_VCS_PG_SEL: For debug, contains the actual index n into ECO Domain PFET Value [n] SLAT Register set that contains the ECO PFET Enable Value currently enabled.



Register Name	<i>PM State History Register For Hypervisor</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPHYP_REG
Address	000000001C0F0110 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	PHYP_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPART	PHYP_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPART	PHYP_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPART	PHYP_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPART	PHYP_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPART	PHYP_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For FSP</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PMSTATEHISTFSP_REG
Address	000000001C0F0111 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	FSP_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPART	FSP_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPART	FSP_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPART	FSP_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.

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Bits	PCB	Field Mnemonic: Description
6	ROX_CLRPAR T	FSP_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	FSP_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For OCC</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PMSTATEHISTOCC_REG
Address	000000001C0F0112 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	OCC_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	OCC_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	OCC_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	OCC_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	OCC_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	OCC_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For PerfMon</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPERF_REG
Address	000000001C0F0113 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	PERF_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	PERF_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	PERF_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	PERF_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	PERF_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	PERF_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM FSM Reset And Babystepper Idle Injects</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.IDLEFSMGOTOCMD_REG
Address	000000001C0F0114 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	WO_1P	idle_fsm_goto_cmd ' A write to this reg will proceed the IDLE FSM from WAIT_FOR_PORE_DONE, SLEEP_EXIT_WAIT_FOR_PORE_FAST_EXIT_DONE, or WINKLE_EXIT_WAIT_FOR_PORE_FAST_EXIT_DONE to the following states: ' 0b01: goto IDLE state ' 0b10: goto SLEEP_EXIT_CORE_MESHLET_ON state ' 0b11: goto WINKLE_EXIT_NOTIFY_PMC state ' "
2	RWX	babystp_trigger_sleep_entry ' A write to this reg with a 1 in this field will cause the babystepper to run the sleep entry sequence. This step is needed for an assisted entry into sleep, before the power is actually turned off since the babystepper needs to know about the sleep state. For an unassisted entry, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished entering its sleep mode. ' "
3	RWX	babystp_trigger_winkle_entry ' A write to this reg with a 1 in this field will cause the babystepper to run the winkle entry sequence. This step is needed for an assisted entry into winkle before the power is actually turned off since the babystepper needs to know about the winkle state. For an unassisted entry, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished entering its winkle mode. ' "
4	RWX	babystp_trigger_wakeup ' A write to this reg with a 1 in this field will cause the babystepper to run the wakeup sequence from sleep/winkle depending on the babystepper state of sleep or winkle. This step is needed for an assisted exit from winkle before the power is actually turned off since the babystepper needs to know about the wakeup state. For an unassisted exit, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished waking up from sleep or winkle. ' "

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Register Name	Core PFET Power Up Delay
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.COREPFPUDLY_REG
Address	000000001C0F012C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_POWUP_DLY0: Delay used after transitioning to Core Domain power up sequence stage0. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	CORE_POWUP_DLY1: Delay used after transitioning to Core domain power up sequence stage1.
8:19	RW	CORE_POWER_UP_DELAY_SEL: Vector select for which delay to use for the respective power-up stage. Bit mapping: 8 -> core_*_pfet_enable(0) 9 -> core_*_pfet_enable(1) ... 19 -> core_*_pfet_enable(11) Bit meaning: 0 = Use core_powup_dly0 1 = Use core_powup_dly1

Register Name	Core PFET Power Down Delay
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.COREPFPDDLY_REG
Address	000000001C0F012D (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_POWDN_DLY0: Delay used after transitioning to Core domain power dn sequence stage1. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	CORE_POWDN_DLY1: Delay used after transitioning to Core domain power dn sequence stage1. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
8:19	RW	CORE_POWER_DN_DELAY_SEL: Vector select for which delay to use for the respective power-dn stage. Bit mapping: 8 -> core_*_pfet_enable(0) 9 -> core_*_pfet_enable(1) ... 19 -> core_*_pfet_enable(11) Bit meaning: 0 = Use core_powdn_dly0 1 = Use core_powdn_dly1



Register Name	Core PFET Vretention	
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.COREPFVRET_REG	
Address	000000001C0F0130 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_VRET_SEL: Pointer to the stage representing the Vretention value for the core PFETs. Power down sequences will stop after enabling this stage.
4:7	RW	CORE_VOFF_SEL: Pointer to the stage representing the Voff value for the core PFETs. Power down sequences will stop after enabling this stage.

Register Name	ECO PFET Power Up Delay	
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.ECOPFPUDLY_REG	
Address	000000001C0F014C (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_POWUP_DLY0: Delay used after transitioning to ECO domain power up sequence stage0 in terms of refclk period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	ECO_POWUP_DLY1: Delay used after transitioning to ECO domain power up sequence stage1.
8:19	RW	ECO_POWER_UP_DELAY_SEL: Vector select for which delay to use for the respective power-up stage. Bit mapping: 8 -> eco_*_pfet_enable(0) 9 -> eco_*_pfet_enable(1) ... 19 -> eco_*_pfet_enable(11) Bit meaning: 0 = Use eco_powup_dly0 1 = Use eco_powup_dly1

Register Name	ECO PFET Power Down Delay	
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.ECOPFPDDLY_REG	
Address	000000001C0F014D (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_POWDN_DLY0: UNUSED/SPARE
4:7	RW	ECO_POWDN_DLY1: Delay used after transitioning to ECO Domain power dn sequence stage1. The delays in this register are in terms of refclk period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.

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Bits	PCB	Field Mnemonic: Description
8:19	RW	ECO_POWER_DN_DELAY_SEL: Vector select for which delay to use for the respective power-down stage. Bit mapping: 8 -> eco_*_pfet_enable(0) 9 -> eco_*_pfet_enable(1) ... 19 -> eco_*_pfet_enable(11) Bit meaning: 0 = Use eco_powdn_dly0 1 = Use eco_powdn_dly1

Register Name		ECO PFET Vretention
Mnemonic		EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.ECOPFVRET_REG
Address		000000001C0F0150 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_VRET_SEL: Pointer to the stage representing the Vretention value for the ECO PFETs. Power down sequences will stop after enabling this stage.
4:7	RW	ECO_VOFF_SEL: Pointer to the stage representing the Voff value for the ECO PFETs. Power down sequences will stop after enabling this stage.

Register Name		Frequency Control Register With Overrides For DPLL
Mnemonic		EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.FREQ_CTRL_REG
Address		000000001C0F0151 (PCB)
Attributes		
Description		Note that overrides to Dpll_fmax are only applied if Dpll_freq_override_enable = 1. A read of all these dials always returns the currently established DPLL frequencies (regardless of any other mode settings).
Bits	PCB	Field Mnemonic: Description
0:8	RWX	DPLL_FMIN: minimum DPLL frequency in CPM-DPLL mode that is set at IPL time A read always returns the currently established value A write is not conditioned on any other dial setting.
9:17	RWX	DPLL_FMAX: DPLL maximum frequency and frequin (these two values are the same in POWER8 processor) without applying bias values: A read always returns the currently established value A write is conditioned on the setting of dpll_freq_override_enable. If dpll_freq_override_enable is asserted, a write causes this field to update. Otherwise the hardware (that is, PStates) are controlling the update of this value.
18:21	RO	Reserved.
22:30	RW	FREQU_AT_PSTATE0: DPLL frequency for Pstate 0



Register Name	<i>DPLL Mode Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.DPLL_CPM_PARM_REG
Address	000000001C0F0152 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	LF_SLEWRATEXPI: out of lock slew rate for DPLL
8	RW	LF_USE_CPMXPI: use CPM instead of PFD as loop filter input, if '1' (instead of using both)
9	RW	FF_USE_CPMXPI: use the CPM inputs for the frequency filter, if '1'
10	RW	CPM_FILTER_ENABLE: enables the CPM filter
11	RW	FF_BYPASSXPI: enables frequency filter bypass
12	RW	DCO_OVERRIDE: enables overrides for DCO testing/characterization
13	RW	DCO_INCR: enables increment for DCO testing/characterization, increments only on a rising edge
14	RW	DCO_DECR: enables decrement for DCO testing/characterization, decrements only on a rising edge
15:23	RW	DPLL_LOCK_TIMER_REPLACEMENT_VALUE: if dpll_lock_replacement_timer_mode_en is set, this dial specifies the delay in us, after which it is assumed, that the DPLL has reached a frequency lock condition. Note that values less than 3 will cause in undefined HW behavior (0 will cause HANGs!). if dpll_lock_replacement_timer_mode_en is zero, this dial specifies the delay in pcb_nclk cycles after which the hardware monitors the DPLL frequout output (if dpll_freqout_mode_en is set) or the DPLL flock output (if dpll_flock_mode_en is set). Note that in this case, the value of this dial needs to be greater or equal to 150 (decimal).
24:31	RW	PRE_VRET_PSTATE: Pstate that is stepped to before switching to Vretention defined in PCBS_iVRM_Control_Status_Reg
32	RW	OVERRIDE_PCBS_DPLL_SYNCHRONIZER: Bypasses the 'ping-pong' synchronization logic between the DPLL and the PCBS-PM. NEVER SET TO 1 UNLESS YOU KNOW WHAT YOU ARE DOING!
33:36	RW	DPLL_CHAR_DELTA1: Delta in DPLL ticks for characterization (cf. dial dpll_faster_than_fmax_plus_delta1)
37:40	RW	DPLL_CHAR_DELTA2: Delta in DPLL ticks for characterization (cf. dial dpll_faster_than_fmin_minus_delta2)

Register Name	<i>PPMSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_STATUS_REG
Address	000000001C0F0153 (PCB)
Attributes	
Description	The PPMSR provides read access to the power management status that is also shadowed to the PC and visible to the hypervisor in the PMSR (with some delay due to the shadowing process).

Bits	PCB	Field Mnemonic: Description
0:7	ROX	global_pstate_actual ' Actual Global Pstate Pstate or Pglobal_actual' " Reads from this field return the presently established global PState value." " Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent '

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Bits	PCB	Field Mnemonic: Description
8:15	ROX	LOCAL_PSTATE_ACTUAL: ' Actual Local PState or Plocal_actual' " 'Reads from this field return the presently established local PState value. This value will always be less than or equal to global_pstate_actual.' " 'Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent' "
16:23	ROX	pv_min Minimum Pstate set by the platform.
24:31	ROX	pvf_max Maximum Pstate set by the platform.
32	ROX	spr_em_disabled ' SPR Energy Management Disabled' 'Read from this field indicate whether the platform has disabled the 'PMICR and PMICR SPRs to control the chiplet PState.'
33	ROX	Psafe_mode_active Read from this field indicate whether the chiplet has been put into a safe mode with Psafe enabled to a OCC heartbeat loss or other externally forced reasons (0=regular mode, 1=safe mode is active)
34	ROX	iVRM_safe_mode_active Read from this field indicate whether the chiplet has been put the iVRM safe mode (forcing the bypass mode for all iVRMs)
35	ROX	ivrm_enable Read from this field indicate whether the chiplet internal voltage regulation macro is enabled for localized voltage control (0=disabled, 1=enabled) based on ANDing the poweron signals to the iVRMs
36	ROX	all_fsms_in_safe_state For recovery: if this bit is asserted, all Pstate and iVRM control FSMs are in a stable, safe state that allows the recovery routine to proceed with resetting the PCBS PM without the risk of interrupt a critical action
37:40	ROX	pmsr_spares spare bits

Register Name	<i>PIVRMCSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_CONTROL_STATUS_REG
Address	000000001C0F0154 (PCB)
Attributes	
Description	Provides access to chiplet-level controls of the internal VRM rail set (VDD and VCS) across both the core and ECO domains. The following is valid only for bits 4 to 7. When in automatic iVRM mode (ivrm_fsm_enable = 1), these bits provide access to the values established by the automatic hardware mechanism. When In iVRM override mode (ivrm_fsm_enable = 0), these bits allow firmware direct control of the values driving the internal VRMs.

Bits	PCB	Field Mnemonic: Description
0	RW	IVRM_FSM_ENABLE: Internal master VRM FSM Enable 0 = Disable Internal VRM FSMs and enable to control the iVRMs with the available override registers (SCOMable) as a backup mode or for setup (override mode) 1 = Enable Internal VRM FSM sequencers (requires that Pstates are enabled with enable_Pstate_mode=1 as well) (automatic mode)
1	RW	USE_IVRM_FOR_VRET: Internal VRM Enabled for Vretention 0 = Disable Internal VRM for Vretention 1 = Enable Internal VRM for Vretention
2	RW	BINSEARCH_CAL_ENA: trigger binary search (level signal)

Bits	PCB	Field Mnemonic: Description
3	RW	PVREF_EN: Internal VRM Power Voltage Reference Forced Enable 0 = Allow hardware to enable/disable pvref circuit 1 = Force enablement of the pvref circuit
4	RWX	IVRM_CORE_VDD_BYPASS_B: Internal VRM Core VDD Bypass (negative active) 0 = VDD Internal Core VRMs in bypass 1 = VDD internal Core VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
5	RWX	IVRM_CORE_VDD_POWERON: Internal VRM Core VDD Poweron 0 = Core VDD Internal VRMs powered off 1 = Core VDD internal VRMs powered on if this bit is not set (=0), the Core VDD internal VRM powered off internally. If this bit is set (=1), the Core VDD internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
6	RWX	IVRM_CORE_VCS_BYPASS_B: Internal VRM Core VCS Bypass (negative active) 0 = VCS Internal Core VRMs in bypass 1 = VCS internal Core VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VCS internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VCS internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
7	RWX	IVRM_CORE_VCS_POWERON: Internal VRM Core VCS Poweron 0 = Core VCS Internal VRMs powered off 1 = Core VCS internal VRMs powered on if this bit is not set (=0), the Core VCS internal VRM powered off internally. If this bit is set (=1), the Core VCS internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
8	RWX	IVRM_ECO_VDD_BYPASS_B: Internal VRM ECO VDD Bypass (negative active) 0 = VDD Internal ECO VRMs in bypass 1 = VDD internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
9	RWX	IVRM_ECO_VDD_POWERON: Internal VRM ECO VDD Bypass (negative active) 0 = VDD Internal ECO VRMs in bypass 1 = VDD internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.

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Bits	PCB	Field Mnemonic: Description
10	RWX	IVRM_ECO_VCS_BYPASS_B: Internal VRM ECO VCS Bypass (negative active) 0 = VCS Internal ECO VRMs in bypass 1 = VCS internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VCS internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VCS internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
11	RWX	IVRM_ECO_VCS_POWERON: Internal VRM ECO VCS Poweron 0 = ECO VCS Internal VRMs powered off 1 = ECO VCS internal VRMs powered on if this bit is not set (=0), the ECO VCS internal VRM powered off internally. If this bit is set (=1), the ECO VCS internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
12:18	RWX	IVRM_VRET_VDD: if use_ivrm_for_Vret is asserted, this dial is used to control the Vdd retention voltage. Note: this field will establish the Core VDD rail for Sleep and both the Core and ECO rail for Winkle. - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
19:25	RWX	IVRM_VRET_VCS: if use_ivrm_for_Vret is asserted, this dial is used to control the Vcs retention voltage. Note: this field will establish the Core VDD rail for Sleep and both the Core and ECO rail for Winkle. - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
26:30	RWX	IVRM_VRET_CORE_VDD_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the Core Vdd iVRM PFET strength for the retention voltage
31:35	RWX	IVRM_VRET_CORE_VCS_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the Core Vcs iVRM PFET strength for the retention voltage
36:40	RWX	IVRM_VRET_ECO_VDD_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the ECO Vdd iVRM PFET strength for the retention voltage
41:45	RWX	IVRM_VRET_ECO_VCS_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the ECO Vcs iVRM PFET strength for the retention voltage
46	RW	PVREF_FAIL: voltage reference fail input to iVRMs
47	ROX	IVRM_PREF_ERROR_GROSS: Voltage Reference Gross Error 0 = Gross Error not detected 1 = Gross Error detected
48	ROX	IVRM_PREF_ERROR_FINE: Voltage Reference Fine Error 0 = Fine Error not detected 1 = Fine Error detected
49	ROX	IVRM_CORE_VDD_RANGE_HI: Core VDD Internal VRM Range Hi Indicator 0 = Core VDD Internal VRM Hi indicator signal not asserted 1 = Core VDD internal VRMs Hi indicator signal asserted
50	ROX	IVRM_CORE_VDD_RANGE_LO: Core VDD Internal VRM Range Low Indicator 0 = Core VDD Internal VRM Low indicator signal not asserted 1 = Core VDD internal VRMs Low indicator signal asserted



Bits	PCB	Field Mnemonic: Description
51	ROX	IVRM_ECO_VDD_RANGE_HI: ECO VDD Internal VRM Range Hi Indicator 0 = ECO VDD Internal VRM Hi indicator signal not asserted 1 = ECO VDD internal VRMs Hi indicator signal asserted
52	ROX	IVRM_ECO_VDD_RANGE_LO: ECO VDD Internal VRM Range Low Indicator 0 = ECO VDD Internal VRM Low indicator signal not asserted 1 = ECO VDD internal VRMs Low indicator signal asserted
53	ROX	IVRM_CORE_VCS_RANGE_HI: Core VCS Internal VRM Range Hi Indicator 0 = Core VCS Internal VRM Hi indicator signal not asserted 1 = Core VCS internal VRMs Hi indicator signal asserted
54	ROX	IVRM_CORE_VCS_RANGE_LO: Core VCS Internal VRM Range Low Indicator 0 = Core VCS Internal VRM Low indicator signal not asserted 1 = Core VCS internal VRMs Low indicator signal asserted
55	ROX	IVRM_ECO_VCS_RANGE_HI: ECO VCS Internal VRM Range Hi Indicator 0 = ECO VCS Internal VRM Hi indicator signal not asserted 1 = ECO VCS internal VRMs Hi indicator signal asserted
56	ROX	IVRM_ECO_VCS_RANGE_LO: ECO VCS Internal VRM Range Low Indicator 0 = ECO VCS Internal VRM Low indicator signal not asserted 1 = ECO VCS internal VRMs Low indicator signal asserted
57	ROX	BINSEARCH_CAL_DONE: binary search done signal
58	RWX	IVRM_CORE_VDD_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
59	RWX	IVRM_CORE_VCS_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
60	RWX	IVRM_ECO_VDD_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
61	RWX	IVRM_ECO_VCS_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
62	RW	IVRM_POWER_DOWN_DISABLE: If this bit is 1, the iVRM poweron signal is left asserted. Power off of the iVRMs is then blocked

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Register Name	<i>The PIVRMVSR</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VALUE_SETTING_REG
Address	000000001C0F0155 (PCB)
Attributes	
Description	The PIVRMVSR allows access to VID values and PFET strength valid signal settings presented to the internal VRM rail set (VDD and VCS) across both the core and ECO domains. When in <code>ivrm_fsm_enable = "auto"</code> mode, this register provides access to the values established by the automatic hardware mechanism. When <code>ivrm_fsm_enable = "override"</code> mode, this register allows firmware direct control of the values driving the internal VRMs which, if the VRMs are not in bypass, will move the voltage settings.

Bits	PCB	Field Mnemonic: Description
0:7	RWX	IVRM_CORE_VDD_IVID: When read, returns the value presently being driving to the Core VDD iVRM. If <code>ivrm_fsm_enable = 0</code> (override_mode), then writes to this field will drive a new VID value to the Core VDD iVRM. If <code>ivrm_fsm_enable = 1</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
8:15	RWX	IVRM_CORE_VCS_IVID: When read, returns the value presently being driving to the Core VCS iVRM. If <code>ivrm_fsm_enable = 0</code> (override_mode), then writes to this field will drive a new VID value to the Core VCS iVRM. If <code>ivrm_fsm_enable = 1</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
16:23	RWX	IVRM_ECO_VDD_IVID: When read, returns the value presently being driving to the Core VDD iVRM. If <code>ivrm_fsm_enable = 0</code> (override_mode), then writes to this field will drive a new VID value to the ECO VDD iVRM. If <code>ivrm_fsm_enable = 1</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
24:31	RWX	IVRM_ECO_VCS_IVID: When read, returns the value presently being driving to the ECO VCS iVRM. If <code>ivrm_fsm_enable = 0</code> (override_mode), then writes to this field will drive a new VID value to the ECO VCS iVRM, If <code>ivrm_fsm_enable = 0</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
32:36	RWX	IVRM_CORE_VDD_PFET_STRENGTH: When read, returns the value presently being driving to the core VCS iVRM. If <code>ivrm_fsm_enable = 0</code> (override_mode), then writes to this field will drive a new strength value to the core VCS iVRM, If <code>ivrm_fsm_enable = 0</code> , writes to this field are not performed.

Bits	PCB	Field Mnemonic: Description
37:41	RWX	IVRM_CORE_VCS_PFET_STRENGTH: This register is assigned to the signals tcex##_tp_ivrm_core_vcs_sense & tcex##_tp_ivrm_core_vdd_sense & tcex##_tp_ivrm_eco_vcs_sense & tcex##_tp_ivrm_eco_vdd_sense & 0b0 Note that all other sense signals are spares now and tied to 0. OUTDATED TEXT: When read, returns the value presently being driving to the core VDD iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the core VDD iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
42:46	RWX	IVRM_ECO_VDD_PFET_STRENGTH: When read, returns the value presently being driving to the ECO VCS iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the ECO VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
47:51	RWX	IVRM_ECO_VCS_PFET_STRENGTH: When read, returns the value presently being driving to the ECO VDD iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the ECO VDD iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
52	RWX	IVRM_VDD_CORE_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the Core VDD iVRM. If ivrm_fsm_enable = 1 AND ivrm_control_mode = 1 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the Core VDD iVRM, If ivrm_fsm_enable = 0 OR ivrm_control_mode = 0, writes to this field are not performed.
53	RWX	IVRM_VCS_CORE_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the Core VCS iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the Core VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
54	RWX	IVRM_VDD_ECO_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the ECO VDD iVRM. If ivrm_fsm_enable = 1 AND ivrm_control_mode = 1 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the ECO VDD iVRM, If ivrm_fsm_enable = 0 OR ivrm_control_mode = 0, writes to this field are not performed.
55	RWX	IVRM_VCS_ECO_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the ECO VCS iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the ECO VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
56	RWX	CORE_VDD_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
57	RWX	CORE_VCS_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
58	RWX	ECO_VDD_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
59	RWX	ECO_VCS_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.

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Register Name		General PCBS Modes And Chicken Switches
Mnemonic		EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBSPM_MODE_REG
Address		000000001C0F0156 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RW	ENABLE_PSTATE_MODE: if asserted, Pstate requests (from overrides or PMCR) will be honored, otherwise, the hardware does not do anything. Note to firmware: this is the master switch for Pstates and should be asserted after all sub-modes (that is, lvrn_fsm_en) are setup to avoid enabling unintentional modes during the mode setup.
1	RW	GLOBAL_PSTATE_CHANGE_FOR_IDLE_STATE_ENABLED: if asserted, a global Pstate change to the Nap/Sleep/Winkle-Pstate is requested, when the Nap/Sleep/Winkle state is entered and the individual enable bits in the PIMCR are asserted
2	RW	ENABLE_GLOBAL_PSTATE_REQ: if '1' then enable PMC interrupt with global Pstate change request, otherwise, disable global requests
3	RW	ENABLE_WINKLE_WITH_CPM_MODE: if '1', PCBS automatically changes the DPLL mode to mode 1, when entering winkle, but changes the mode back to CPM mode when exiting. Needed for CPM-DPLL control loop enablement.
4	RW	ENABLE_CLIPPING_OF_GLOBAL_PSTATE_REQ: if '1', PCBS automatically clips global Pstate requests with Pvf_max in PPMBR and sets the 'donate' bit in the interrupt accordingly
5	RW	CHKSW_HW214553: if deasserted, HW214553 (frequin issue in resclk mode) is fixed, if asserted, the fix is not active
6	RW	ENABLE_PMC_PMAX_SYNC_NOTIFICATION: if asserted, the PCBS-PM will send a 'Pmax_sync' interrupt, once the synchronization criterion is met
7	RW	DPLL_LOCK_REPLACEMENT_TIMER_MODE_EN: Select a timer instead of the DPLL lock bit as target frequency reached criterion. This timer has to be setup by the dial dpll_lock_timer_replacement_value. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
8	RW	DPLL_FREQOUT_MODE_EN: Looks at the DPLL frequout to find out, if the target frequency has been reached. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
9	RW	DPLL_FLOCK_MODE_EN: Looks at the real DPLL flock output to find out, if the target frequency has been reached. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
10	RW	ENABLE_SENSE_DELAY_CHARACTERIZATION: If this switch is 0, the sense latches are updated every cycle. If this switch is 1, the sense delay measurement mode is enabled, that starts a sense delay timer, whenever one of the registers that drive the inputs of the iVRMs/pFETs is written via PCB and that triggers a sense register freeze operation, when the sense delay timer reaches the value sense_delay_timer_val. With this mode, the sense delays can be measured in multiples of the PCB-slave clock speed.
11:17	RW	SENSE_DELAY_TIMER_VAL: See the description of enable_sense_delay_characterization for details.
18:19	RW	CPM_FMIN_CLIP_ERROR_SEL: This dial selects, which of the following conditions will cause the FIR bit dpll_fmin_and_not_cpmbit to be set to detect, that the DPLL runs at Fmin, but is still clipped by the CPMs. 0b00 = function is disabled 0b01 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit2 = 0 0b10 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit1 = 0 0b11 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit0 = 0
20:23	RW	DBG_TRACE_SEL: This dial selects the group of signals to be traced for debug in the lab. Details to be found in the Section 'Trace Bus'

Bits	PCB	Field Mnemonic: Description
24:25	RW	TRACE_DATA_SEL: This dial selects the group of signals to be traced for debug in the lab. Details to be found in the Section 'Trace Bus'
26:29	RW	TP_CPLT_IVRM_VPP_TUNE: Tune bits to be set going to the iVRMs

Register Name	<i>PIVRMPS Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_PFETSTR_SENSE_REG
Address	000000001C0F0157 (PCB)
Attributes	
Description	Used to check that the pFET sense outputs correspond to the driven values (mainly for test).

Bits	PCB	Field Mnemonic: Description
0:4	ROX	IVRM_CORE_VDD_PFETSTR_SNS: Not used any more.
5:9	ROX	IVRM_CORE_VCS_PFETSTR_SNS: This register is assigned to the signals tcex##_tp_ivrm_core_vcs_sense & tcex##_tp_ivrm_core_vdd_sense & tcex##_tp_ivrm_eco_vcs_sense & tcex##_tp_ivrm_eco_vdd_sense & 0b0
10:14	ROX	IVRM_ECO_VDD_PFETSTR_SNS: Not used any more.
15:19	ROX	IVRM_ECO_VCS_PFETSTR_SNS: Not used any more.
20	ROX	IVRM_VDD_CORE_PFETSTR_VALID_SNS: Not used any more.
21	ROX	IVRM_VCS_CORE_PFETSTR_VALID_SNS: Not used any more.
22	ROX	IVRM_VDD_ECO_PFETSTR_VALID_SNS: Not used any more.
23	ROX	IVRM_VCS_ECO_PFETSTR_VALID_SNS: Not used any more.
24	ROX	CORE_VDD_BYPASS_B_SENSE: Not used any more.
25	ROX	CORE_VCS_BYPASS_B_SENSE: Not used any more.
26	ROX	ECO_VDD_BYPASS_B_SENSE: Not used any more.
27	ROX	ECO_VCS_BYPASS_B_SENSE: Not used any more.
28	ROX	CORE_VDD_POWERON_SENSE: Not used any more.
29	ROX	CORE_VCS_POWERON_SENSE: Not used any more.
30	ROX	ECO_VDD_POWERON_SENSE: Not used any more.
31	ROX	ECO_VCS_POWERON_SENSE: Not used any more.
32	ROX	CORE_VDD_VPUMP_EN_SENSE: Not used any more.
33	ROX	CORE_VCS_VPUMP_EN_SENSE: Not used any more.
34	ROX	ECO_VDD_VPUMP_EN_SENSE: Not used any more.
35	ROX	ECO_VCS_VPUMP_EN_SENSE: Not used any more.
36	ROX	CORE_VDD_PFET_LOW_VOUT_SNS: Not used any more.
37	ROX	CORE_VCS_PFET_LOW_VOUT_SNS: Not used any more.
38	ROX	ECO_VDD_PFET_LOW_VOUT_SNS: Not used any more.
39	ROX	ECO_VCS_PFET_LOW_VOUT_SNS: Not used any more.



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Register Name	PPMICR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_IDLE_CONTROL_REG
Address	000000001C0F0158 (PCB)
Attributes	
Description	Used to read the PMICR register typically owned (written) by the hypervisor. Writes are conditioned on the setting of the dial Pm_spr_override_en. If Pm_spr_override_en is set, firmware must make sure that the special wakeup state of this chiplet is reached before changing any of the latency fields in this register. Otherwise, the hardware behavior is undefined.

Bits	PCB	Field Mnemonic: Description
0:7	ROX	NAP_PSTATE_REQ: Nap Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
8	ROX	NAP_PSTATE_EN: Nap PState Enable 1 = Enable the Nap Pstate (NPS) Request, Nap Global Enable and Nap Latency functions 0 = Disables the Nap Pstate (NPS) Request, Nap Global Enable and Nap Latency functions Reads from the field return the value last written.
9	ROX	NAP_GLOBAL_EN: Nap Global Enable 1 = Upon the execution of a Nap instruction , the Nap Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a Nap instruction , the Nap Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.
10:11	ROX	NAP_LATENCY: Nap Latency not supported for POWER8 processor
12:15	ROX	RESERVED_PPMICR_0: reserved
16:23	ROX	SLEEP_PSTATE_REQ: sleep Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
24	ROX	SLEEP_PSTATE_EN: sleep PState Enable 1 = Enable the sleep Pstate (NPS) Request, sleep Global Enable and sleep Latency functions 0 = Disables the sleep Pstate (NPS) Request, sleep Global Enable and sleep Latency functions Reads from the field return the value last written.
25	ROX	SLEEP_GLOBAL_EN: sleep Global Enable 1 = Upon the execution of a sleep instruction , the sleep Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a sleep instruction , the sleep Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.



Bits	PCB	Field Mnemonic: Description
26:27	ROX	SLEEP_LATENCY: sleep Latency 00 = Cease instructions and honors Pstate change but does not perform additional state changing actions (unsupported in POWER8, maps to 0b10) 01 = Indicates to the platform that a sub-state that would have the lowest latency is enabled (unsupported in POWER8, maps to 0b10) 10 = Indicates to the platform that a sub-state that might have a medium exit latency is enabled (POWER8: Fast Sleep) 11 = Indicates to the platform that a sub-state that might have higher exit latency is enabled (POWER8: Deep Sleep)
28:31	ROX	RESERVED_PPMICR_1: reserved
32:39	ROX	WINKLE_PSTATE_REQ: winkle Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
40	ROX	WINKLE_PSTATE_EN: winkle PState Enable 1 = Enable the winkle Pstate (NPS) Request, winkle Global Enable and winkle Latency functions 0 = Disables the winkle Pstate (NPS) Request, winkle Global Enable and winkle Latency functions Reads from the field return the value last written.
41	ROX	WINKLE_GLOBAL_EN: winkle Global Enable 1 = Upon the execution of a winkle instruction , the winkle Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a winkle instruction , the winkle Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.
42:43	ROX	WINKLE_LATENCY: winkle Latency 00 = Cease instructions and honors Pstate change but does not perform additional state changing actions (unsupported in POWER8, maps to 0b10) 01 = Indicates to the platform that a sub-state that would have the lowest latency is enabled (unsupported in POWER8, maps to 0b10) 10 = Indicates to the platform that a sub-state that might have a medium exit latency is enabled (POWER8: Fast Winkle) 11 = Indicates to the platform that a sub-state that might have higher exit latency is enabled (POWER8: Deep Winkle)
44:47	ROX	RESERVED_PPMICR_2: reserved

Register Name	<i>PPMCR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_CONTROL_REG
Address	000000001C0F0159 (PCB)
Attributes	
Description	Provides read access to the PMCR register shadow in the PCBS, typically owned (written) by the hypervisor. Writes are conditioned on the setting of PMGP1[pm_spr_override_en].

Bits	PCB	Field Mnemonic: Description
0:7	RWX	GLOBAL_PSTATE_REQ: global Pstate request from hypervisor (or OCC)
8:15	RWX	LOCAL_PSTATE_REQ: local Pstate request from hypervisor or OCC
16	RWX	AUTO_OVERRIDE0_PSTATE_LIMIT_EN: automatic override Pstate 0 (for low activity detection) is enabled, if asserted

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Bits	PCB	Field Mnemonic: Description
17	RWX	AUTO_OVERRIDE1_PSTATE_LIMIT_EN: automatic override Pstate 1 (reserved for future use) is enabled, if asserted
18:23	RWX	RESERVED_PPMCR: reserved
24:31	RWX	AUTO_OVERRIDE_PSTATE0: automatic override Pstate 0 (for low activity detection)
32:39	RWX	AUTO_OVERRIDE_PSTATE1: automatic override Pstate 1 (reserved for future use)

Register Name	<i>Control Register That Is Written By PMC Sequencer</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_PMC_VF_CTRL_REG
Address	000000001C0F015A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PGLOBAL_ACTUAL: global actual Pstate
8:15	RW	MAXREGVCS: maximum regulation point for Vcs, Bit 0 is reserved, bits 1 to 7 are in iVID format
16:23	RW	MAXREGVDD: maximum regulation point for Vdd, Bit 0 is reserved, bits 1 to 7 are in iVID format
24:31	RW	EVIDVCS_EFF: eff. external voltage ID for Vcs in iVID format, Bit 0 is reserved
32:39	RW	EVIDVDD_EFF: eff. external voltage ID for Vdd in iVID format, Bit 0 is reserved

Register Name	<i>Undervolting Register For PCBS</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_UNDERVOLTING_REG
Address	000000001C0F015B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PUV_MIN: minimum Pstate for which undervolting is allowed
8:15	RW	PUV_MAX: maximum Pstate for which undervolting is allowed
16:21	RW	KUV: this value indicates how many Pstate ticks a voltage request is undervolted (clipped with Puv_min). Note that the Kuv value is signed

Register Name	<i>The PPSIBR</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_INDEX_BOUND_REG
Address	000000001C0F015C (PCB)
Attributes	
Description	Enables setting the minimum and maximum Pstate that is supported as a pointer into the local Pstate table (which has entries from 0 to 127).



Bits	PCB	Field Mnemonic: Description
0:7	RW	LPSI_MIN: this Pstate index is the index that corresponds to array entry 0. Note that the index domain is obtained by adding 128 to a Pstate, thus, the value is unsigned.
8:14	RW	LPSI_ENTRIES_MINUS_1: this dial contains the value of the number of entries in the Pstate table minus 1

Register Name	PPMBR Register	
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_BOUNDS_REG	
Address	000000001C0F015D (PCB)	
Attributes		
Description	Enables setting the Pstate bounds that are managed by the OCC. If dial Enable_pmc_pmax_sync_notification is set, firmware must wait after each write to this register until the PMC has received the Pmax Sync Interrupt. If a write happens to this register while the previously scheduled Pmax Sync Interrupt has not yet left PCBS, the error TBD will be set.	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PMIN_CLIP: minimum Pstate allowed for this chiplet
8:15	RW	PMAX_CLIP: maximum Pstate allowed for this chiplet (has to be greater or equal to Pmin_clip)

Register Name	PPTCR Register	
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_CTRL_REG	
Address	000000001C0F015E (PCB)	
Attributes		
Description	Controls the address for writing the local Pstate table array (all 96 words are accessible). Note that the protocol requires this register to be set up with the Pstate address first, if a read or a write of the Pstate array is intended, to make sure that the initial address is set correctly. The register PPTR must always be written or read afterward. Note that any access to the PPTR auto-increments this register.	

Bits	PCB	Field Mnemonic: Description
0:6	RWX	PSTATE_TABLE_ADDRESS: This is the address of the Pstate table in PCBS, which is auto-incremented after any access to the PTLR.

Register Name	PPTR Register	
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_REG	
Address	000000001C0F015F (PCB)	
Attributes		
Description	The PPTR controls the data to be written into the Pstate table and returns the data for a read of the Pstate table. Note that the protocol requires for a write to set this register up after first setting up PPTCR (if the user does not rely on the auto-increment function of the address). For a read of the Pstate table, this register must be read after first setting up PPTCR as well (again if the auto-increment feature of the address is not used). Any access to this register auto-increments the Pstate_table_address by 1. Note also that the read functionality of this register is only functional if PIVRMCSR[jvrm_fsm_enable] = 0. The write functionality works in any case.	

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Bits	PCB	Field Mnemonic: Description
0:63	RW	pstate_data This is the field for data bits 0 to 63

Register Name	PPSTR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_STEP_TARGET_REG
Address	000000001C0F0160 (PCB)
Attributes	
Description	The PPSTR provides read access to several intermediate values in the Pstate computation pipeline. Writes Are conditioned on the setting of PMGPO[enable_OCC_ctrl_for_local_Pstate_eff_req].

Bits	PCB	Field Mnemonic: Description
0:7	RWX	LOCAL_PSTATE_EFF_REQ: this field represents the effective local Pstate request right before the clipping with Pmin and Pmax if enable_OCC_ctrl_for_local_Pstate_eff_req=0 then the hardware controls this dial, that updates every cycle if enable_OCC_ctrl_for_local_Pstate_eff_req=1 then OCC is in control and can write this field to control the effective local Pstate request that will eventually propagate through the downstream logic and determine the Local PState Actual. Note: if no write to this register is performed, the currently established value is maintained stable forever.
8:15	ROX	LOCAL_PSTATE_TARGET: This field is the target Pstate of a complete Pstate change that is performed in smaller steps
16:23	ROX	LOCAL_CORE_PSTATE_STEP_TARGET: this field represents the intermediate value that is about to be established as the next Local Pstate Actual after completing one step in the process of the transition towards the 'local_Pstate_target' the new voltage, frequency, and clock resonance setting
24:31	ROX	LOCAL_ECO_PSTATE_STEP_TARGET: this field represents the intermediate value that is about to be established as the next Local Pstate Actual after completing one step in the process of the transition towards the 'local_Pstate_target' the new voltage, frequency, and clock resonance setting

Register Name	Read-Only Status Register For DPLL And For Debugging (PDSR)
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_DPLL_STATUS_REG
Address	000000001C0F0161 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:14	ROX	DPLL_FF_FREQOUT: frequout output from DPLL (current frequency - bits 2 to 10 correspond to the same scale as the 9 bits of frequin (which need to be multiplied with our frequency step to get the real frequency), the remaining bits just provide a higher accuracy)
15	ROX	DPLL_FREQU_CHANGE: DPLL Frequency change (pin of DPLL without filter)
16	ROX	DPLL_STATUS_SPARE_BIT1: Spare bit.
17	ROX	PMAX_SYNC_PENDING: gets asserted, if the logic has a Pmax sync interrupt outstanding that will be eventually sent to PMC when the Pmax sync criterion is met
18	ROX	GA_ACK_PENDING: gets asserted, if the logic has a global actual Pstate update acknowledgment interrupt outstanding that will be eventually sent to PMC when the GA ack criterion is met
19:26	ROX	CAPPED_GLOBAL_PSTATE_REQ: corresponds to the capped global Pstate request that is presented as Pstate interrupt and send to PMC

Bits	PCB	Field Mnemonic: Description
27	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT2: DPLL runs at Fmax and CPM bit 2 is set. Note that this bit and the following 2 bits indicate, that the CPMs would allow the DPLL to run faster than Fmax.
28	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT3: DPLL runs at Fmax and CPM bit 3 is set
29	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT4: DPLL runs at Fmax and CPM bit 4 is set
30	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT2: DPLL runs at Fmin and CPM bit2 is zero. Note that this bit and the following 2 bits indicate, that the CPMs indicate, that the DPLL should run slower than the currently established Fmin.
31	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT1: DPLL runs at Fmin and CPM bit1 is zero
32	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT0: DPLL runs at Fmin and CPM bit0 is zero
33	ROX_CLRPAR T	DPLL_FASTER_THAN_FMAX_PLUS_DELTA1: The DPLL indicated that it ran once faster than Fmax+dpll_char_delta1
34	ROX_CLRPAR T	DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2: The DPLL indicated that it ran once slower than Fmin-dpll_char_delta2
35:48	ROX	DPLL_MAX_FREQOUT_AFTER_LAST_READ: This dial indicates the maximum DPLL frequout value after the last read of this register (only 14 MSBs)
49:62	ROX	DPLL_MIN_FREQOUT_AFTER_LAST_READ: This dial indicates the minimum DPLL frequout value after the last read of this register (only 14 MSBs)

Register Name	<i>The PIVRMVCR0 Controls The Voltage Stepping Delays</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG0
Address	000000001C0F0162 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	IVRM_REQ_PSTATE_STEPDELAY_RISING: Requested Internal Pstate Baby Step Delay - Rising Step. Delay before allowing the next step for a rising Pstate Transition. This dial and ivrm_req_Pstate_stepdelay_lowering allow for differing delays for the two directional transitions if necessary. In 100ns units as established by scan dial ivrm_100ns_value
8:15	RW	IVRM_REQ_PSTATE_STEPDELAY_LOWERING: Requested Internal Pstate Baby Step Delay - Lowering Step. Delay before allowing the next step for a lower Pstate Transition. This dial and ivrm_req_Pstate_stepdelay_rising allow for differing delays for the two directional transitions if necessary. In 100ns units as established by scan dial ivrm_100ns_value

Register Name	<i>The PIVRMVCR1 Controls The Voltage Stepping Delays</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG1
Address	000000001C0F0163 (PCB)
Attributes	
Description	

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Bits	PCB	Field Mnemonic: Description
0:7	RW	IVRM_STABILIZE_DELAY_RUN: Stabilization Delay - Run Time Delay to allow a rail to stabilize upon a baby step while the region is operational. In 100ns units as established by scan dial ivrm_100ns_value
8:15	RW	IVRM_STABILIZE_DELAY_IDLE: Stabilization Delay - Idle Transition Delay to allow a rail to stabilize upon a baby step during an idle transition where the activity in the region is quiesced. In 100ns units as established by scan dial ivrm_100ns_value
16:23	RW	IVRM_PFSTR_PROP_DELAY: PFET Strength Propagation Delay Time from PFET Strength values being launched till PFET Strength Valid is asserted. In order to ensure like rails across domains (Core VDD<>ECO VDD, Core VCS<>ECO VCS) are in sync during operational mode, this time value applies to all rails across the domains. This parameter allows for PFET Strength values to settle before PFET Strength Valid is sampled in the Uregs. The value set must the maximum delay for the worst rail timing and must allow for any metastability settling (for example, normally 2-3 cycles for single signals in an asynch handshake interface)
24:31	RW	IVRM_PFSTRVALID_PROP_DELAY: PFETStrength Valid Propagation Delay Time from ivrm_pfstr_prop_delay expiring to where PFET Strength Valid is deasserted. The value is the maximum of a) the minimum pulse width required for PFETStrength Valid and b) the propagation of PFETStrength Valid through (or enough of) the daisy chain. In order to ensure like rails across domains (Core VDD<>ECO VDD, Core VCS<>ECO VCS) are in sync during operational mode, this time value applies to all rails across the domains and thus must be the set to the value of the worst (slowest) rail. The minimum pulse width cannot be violated. The propagation delay can be tuned for more aggressive timing (for example, de-assert before the actual propagation is complete). Measured in prv_nclk cycles. The min delay is 2 cycles. Additional delay can be configured with the following settings 0x00 = No additional delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks
32:39	RW	IVRM_VPUMP_POWERON_TIME: iVRM (VRreg and UReg) - Vpump Power On Time Time necessary for the distributed internal VRM macro circuits to power on. Same delay is required for power on voltage pump circuit. Both delays are in the 8us range. In 100ns units as established by scan dial ivrm_100ns_value
40:47	RW	IVRM_BYPASS_DELAY: iVRM Bypass Propagation Delay Delay time for bypass_b signal propagation. Measured in prv_nclk cycles Target: 50ns 0x00 = No delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks

Bits	PCB	Field Mnemonic: Description
48:55	RW	PFET_VPUMP_ENABLE_DELAY: PFET and Vpump Enable Propagation Delay Delay time for PFET enable and vpump enable signal propagation. Target: 130ns Measured in prv_nclk cycles 0x00 = No delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks
56:62	RW	IVRM_VID_VOUT_THRESHOLD: VID threshold If the output voltage (Vout) is targeting a value below this threshold the slow PFET can backed off from its normal drive strength so as to reduce the ripple at these lower voltage conditions

Register Name	POHR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_OCC_HEARTBEAT_REG
Address	000000001C0F0164 (PCB)
Attributes	
Description	Controls the behavior of the OCC heartbeat function.

Bits	PCB	Field Mnemonic: Description
0:7	RW	occ_heartbeat_time 'OCC Heartbeat Time Value' " 'This field defines the number of ~64us hang timer pulses in which a a PCB read or write of the heartbeat trigger register (of which the offset is specified by dial occ_heartbeat_reg_addr_offset) is not detected that will constitute the loss of the OCC heartbeat. If occ_heartbeat_en is set and upon this loss detection, POHBR[psafe] is forced and, if enabled, the error TBD is activated ' " '0x00 - unsupported, causes undefined behavior' '0x01 - 64us +0/-1us' '0x02 - 128us +0/-1us' '...' '0xFF - 16320us +0/-1us 16.3ms' " 'Upon the 64us hang pulse, the decremter ticks. if the decremter reaches x00, the heartbeat loss event is triggered.' "
8	RW	occ_heartbeat_enable 'OCC Heartbeat Timer Enable' " '0 = Disable the OCC Heartbeat function. Lack of accesses to the register defined by the dial occ_heartbeat_reg_addr_offset does not result in heartbeat loss events to be triggered (no FIRs set nor Safe mode entry).' " '1 = Enable the OCC Heartbeat function. '
9:16	RW	occ_heartbeat_reg_addr_offset This dial allows to configure the address offset within the PCBS power management entity of the register, that will regularly reset the heartbeat timer (which is called heartbeat trigger register). The address offset is 0x100 plus the value of this dial.
17:24	RW	Psafe 'Pstate Safe' " 'This field establishes the Pstate that the core chiplet will take on if: 'psafe <= PMSR[global_actual_pstate] 'AND any of the following conditions are true:' 'Loss of OCC Heartbeat if occ_heartbeat_en is set' 'PMGP0[force_safe_mode] is set' " 'If psafe > PMSR[global_actual_pstate], the global_actual_pstate is forced.' " " 'The value of Psafe needs to be at or below the nominal Pstate to make sure safe operation of all chiplets. '

Register Name	PRCCR0 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG 0
Address	000000001C0F0165 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function.

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Bits	PCB	Field Mnemonic: Description
0	ROX	RESCLK_DIS: Resonant Clock Enable Master enable of all resonant clocking functions. This dial can be set by setting GP3(22) and can not be set in this PCBS_resonant_Clock_Control_Reg0. 1 = Resonant Clock function is disabled. Default values (0) for resclk_value, resclk_core_sync_value, csb_eco_sync_value 0 = Resonant Clock Control hardware is enabled (the mode is defined by dial resclk_control_mode)
1	RW	RESCLK_CONTROL_MODE: Resonant Clock Control Mode Defines the control means enabled when resclk_dis is not set. 0 = Pstate band hardware mechanism enabled 1 = Manual mode enabled (Firmware mode) If this bit is set to 0, the hardware control mechanism that manages the transition across the Resonant Bands is enabled. If this bit is set to 1, the automatic Pstate band hardware mechanism is disabled and the Firmware is in control of all values of the dial resclk_value, resclk_core_sync_value, csb_eco_sync_value. Firmware must ensure that frequency changes will not cross resonant bands or machine failures may result. resclk_value represents the values for clock sector buffer strength, inductor switch strength and high inductor enable. Firmware must ensure the correct stepping in/out the different bands and propagation of the values (resclk_value) to the core/eco (resclk_core_sync_value / csb_eco_sync_value).
2:4	RW	RESCLK_SYNC_PW: Resonant Clock Sync Pulse Width Number of nest/4 cycles to assert the clock sync signal. This value must be high enough to ensure capture and propagation across the asynchronous chiplet boundary.
5:11	RW	RES_SYNC_DELAY_CNT: Resonant Clock Sync Delay Number of nest/4 cycles wait after the launch of the resclk_value (csb and inductor) before launching the sync to allow these to be captured. This value must be high enough to ensure full propagation to the input of the clock sector buffers and inductor switches.
12:26	RW	RES_CSB_STR_INSTR_LO: Resonant Clock Sector Buffer Strength Instruction - Low Band Mask value that determines whether, during a fixed 15 step sequence, the res_csb_str(0:3) is to be decremented/incremented in entering/exiting the Low Band. During resonant clock Entry, res_csb_str(0:3) decremented by the value pattern from 0 down to 14. During resonant clock Exit, res_csb_str(0:3) incremented by the value pattern from 14 up to 0.
27:41	RW	RES_CSB_STR_INSTR_HI: Resonant Clock Sector Buffer Strength Instruction - High Band Mask value that determines whether, during a fixed 15 step sequence, the res_csb_str(0:3) is to be decremented/incremented in entering/exiting the High Band. During resonant clock Entry, res_csb_str(0:3) decremented by the value pattern from 0 down to 14. During resonant clock Exit, res_csb_str(0:3) incremented by the value pattern from 14 up to 0.

Register Name	PRCCR1 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG 1
Address	000000001C0F0166 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function. Writes are conditioned.

Bits	PCB	Field Mnemonic: Description
0:7	RW	FULL_CSB_PS: Full Clock Sector Buffer Pstate Pstate defining the maximum point where the clock sector buffer must be driven to full strength. This allow clocks to be distributed at low Vmin levels. FW needs to make sure that no overlaps occur with bands 2 or 3.
8:15	RW	RES_LOW_LOWER_PS: Low Frequency Resonant Lower (LFRLow) Pstate Pstate defining the lower frequency of the Low Resonant Frequency Band. FW needs to make sure that no overlap occurs with band 0.



Bits	PCB	Field Mnemonic: Description
16:23	RW	RES_LOW_UPPER_PS: Low Frequency Resonant Upper (LFRUpper) Pstate Pstate defining the upper frequency of the Low Resonant Frequency Band. Note that if an overlap occurs with band 3, the hardware behavior is undefined.
24:31	RW	RES_HIGH_LOWER_PS: High Frequency Resonant Lower (HFRLow) Pstate Pstate defining the lower frequency of the High Resonant Frequency Band. Note that if an overlap occurs with band 2, the hardware behavior is undefined.
32:39	RW	RES_HIGH_UPPER_PS: High Frequency Resonant Upper (LFRUpper) Pstate Pstate defining the upper frequency of the High Resonant Frequency Band. This value needs to be greater or equal to high_res_lower_ps.
40:43	RW	NONRES_CSB_VALUE_TI: Clock Sector Buffer Table Index for non-resonant state Table Index into Clock Sector Buffer Table for the nominal, non-resonant state.
44:47	RW	FULL_CSB_VALUE_TI: Clock Sector Buffer Table Index for full CSB value Table Index into Clock Sector Buffer Table for the full CSB strength value.
48:56	RWX	RESCLK_VALUE: Output register driving the 9 bit resclk_value In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current resclk_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. The value in this register represents the following concatenation: csb_str_value(0:3) sw_str(0:3) hi_induct_en.
57	RWX	RESCLK_CORE_SYNC_VALUE: Output register driving the resclk_core_sync signal In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current resclk_core_sync_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. This bit is supposed to be used in order to create a SCOM-controlled pulse to force an update of the resclk propagation registers. A 1 enables the synchronous update, a 0 disables it. Suggested use of this bit is to set it to 1 and then set it back to 0 to create a (long) update pulse.
58	RWX	CSB_ECO_SYNC_VALUE: Output register driving the csb_eco_sync signal In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current csb_eco_sync_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. This bit is supposed to be used in order enable the ECO domain to participate in clock sector buffer strength changes, when switching from nominal strength to full CSB strength. A 1 enables the ECO domain, a 0 disables it from seeing a CSB strength update.

Register Name	PRCCR1 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_STATUS_REG
Address	000000001C0F0167 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function.



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Bits	PCB	Field Mnemonic: Description
0	ROX	RESCLK_STATE: Resonant Clock State 0 = Resonant Clocking inactive 1 = Resonant Clocking active Valid if resclk_inprogress = 0. Hardware sets this bit to the right value at the completion of the transition into and out of resonance mode.

Bits	PCB	Field Mnemonic: Description
1	ROX	RES_HI_INDUCT_EN: Resonant High Inductor Enable Valid if resclk_inprogress = 0. This dial provides the current value being propagated. 0 = Resonant Clock mode not active 1 = Resonant Clock mode active
2	ROX	RESCLK_INPROGRESS: Resonant Clock Transition in Progress This bit is set by hardware while a transition is in progress and will be reset by hardware when the operation is complete.
3	ROX	RESCLK_FULL_CSB: Full CSB Clock State 0 = Full CSB Clocking inactive 1 = Full CSB Clocking active Valid if resclk_inprogress = 0. Hardware sets this bit to the right value at the completion of the transition into and out of full CSB mode respectively.

Register Name	<i>PLPFTCR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_CONTROL_REG
Address	000000001C0F0168 (PCB)
Attributes	
Description	Allows firmware to configure the modes that are used for the PCBS Local Pstate Frequency Target Status Register.

Bits	PCB	Field Mnemonic: Description
0:2	RW	DELAY_TIME: This field encodes the delay between the time a Local Actual Pstate change modifies the input to the DPLL and the time frequency acquisition begins to allow the hardware to ignore the frequency transition of the DPLL in order to get better frequency measurements. This field encodes a delay of ~1us to ~128us in power of 2 selects. The delay is defined by $2^{**}delay\_time$ in us. Note that the hardware uses multiples of the slow hang pulse that is running at 1us.
3	RW	RECORD_TRANSITIONS: This bit indicates whether the LPFTSR records events that correspond to Local Actual Pstate changes (and therefore may include DPLL slewing effects.) One usage model would set the periodic sample_time defined by the dial OHA_MODE_REG[tod_pulse_count_match_val] to a time less than the worst-case DPLL slew time but then ignore Pstate transitions because they might include DPLL slew effects.
4:18	RW	MULTIPLIER: This 15-bit unsigned constant is multiplied by the DPLL frequency code (9 bits) implied by the Local Actual Pstate to yield the 24-bit frequency target measured in PCBS-PM clock cycles (core clock / 2). Assuming times in seconds and frequencies in Hz, firmware should set this constant to: $(DPLL\_Frequency\_Code\_Step\_Hz * Sample\_Time\_Seconds) / 2$
19	RW	ENABLE_LPFT_FUNCTION: This is the enable bit to enable the local Pstate frequency target function. A '1' enables the function, a '0' disables it (the value can be changed at any time).

Register Name	<i>PLPFTSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_STATUS_REG
Address	000000001C0F0169 (PCB)
Attributes	
Description	Allows firmware to observe local actual Pstate realized frequencies.

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Bits	PCB	Field Mnemonic: Description
0	ROX_CLRPART	VALID: If this bit is set then all of the remaining fields of this register are valid. This bit is cleared whenever the register is read or after a local actual Pstate change occurs, and is will be set whenever the hardware completes a valid sample. If firmware reads this register and the valid bit is not set, then it indicates that the Local Pstate target frequency acquisition logic has not been able to complete a frequency acquisition for any Local Actual Pstate change since the last time the LPFTSR was read. This could be due to either of the following factors: 1. Firmware is sampling the LPFTSR faster than the time implied by the sample time defined in OHA by the dial OHA_MODE_REG[tod_pulse_count_match_val] field
1	ROX	CPM_DPLL: If the valid bit is set, then if cpm_dpll is set it indicates that the event recorded by this register was due to a Local Actual Pstate implemented by the DPLL running in CPM-DPLL mode, otherwise the value of this bit is undefined. If the valid bit is not set, this bit is undefined.
2	ROX	IVRM: If the valid bit is set, then if ivrm is set it indicates that the event recorded by this register was due to a Local Actual Pstate whose voltage was set locally by the iVRM operating entirely in regulation mode. If the valid bit is not set, this bit is undefined.
3	ROX	TRANSITION: If the valid bit is set, then if transition is set it indicates that during the observation period a Local Pstate Actual change has occurred, and any performance delta may be due to DPLL frequency slewing. If the valid bit is not set, this bit is undefined
4	ROX	STABLE: If stable is set it indicates that the DPLL input frequency has been stable since the last time the PLPFTSR was read. This bit is set whenever the PLPFTSR is read, and cleared whenever the Fmax input of the DPLL changes. This bit is always valid, regardless of the state of the valid bit. If the PLPFTSR is read on the same cycle a frequency changes then the stable bit is cleared. This bit helps firmware better understand how to interpret the information contained in the PLPFTSR. (Note that this bit should have an attribute ROX_SETPART, but this is not supported by regchk.)
5:28	ROX	DELTA: If the valid bit is set then this is the 24-bit signed difference Measured Cycles - Target Cycles for the event captured by this register. If the valid bit is not set, this dial is undefined.
29:52	ROX	CUMULATIVE: This field records the 24-bit cumulative (signed) delta for all valid samples taken since this field was cleared. Writing any value to this register clears this field. Note that it should have an attribute WOX_CLRPART, but this is not supported by regchk/figtree.
53:60	ROX	PSTATE: If the valid bit is set then this is the Local Actual Pstate of the frequency acquisition that had the minimum (signed) delta of any valid sample taken since the last time the LPFTSR was read. If the valid bit is not set, then this field is undefined.

Register Name	PFSMM1/2 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR1_REG
Address	000000001C0F0170 (PCB)
Attributes	
Description	Facilitates debug by providing insight into the internal FSM states of the PCB-slave power-management unit. For expert use only. Coding according to VHDL design.

Bits	PCB	Field Mnemonic: Description
0:6	ROX	BABYSTEP_MAIN_FSM: Main Babystep FSM (mfsm_lt)
7:11	ROX	BABYSTEP_SLAVE_FSM: Babystep Slave FSM (sfsm_lt)
12:16	ROX	CORE_RAILSTEPPER_MAIN_FSM: Main Core Railstepper FSM (mrsfsm_lt)
17:21	ROX	ECO_RAILSTEPPER_MAIN_FSM: Main ECO Railstepper FSM (mrsfsm_lt)



Bits	PCB	Field Mnemonic: Description
22:25	ROX	CORE_RAILSTEPPER_SUB_FSM: Core Railstepper Sub-FSM (srsfsm_lt)
26:29	ROX	ECO_RAILSTEPPER_SUB_FSM: ECO Railstepper Sub-FSM (srsfsm_lt)
30:34	ROX	CORE_RAILSTEPPER_BYP_FSM: Core Railstepper Bypass FSM (byp_fsm_lt)
35:39	ROX	ECO_RAILSTEPPER_BYP_FSM: ECO Railstepper Bypass FSM (byp_fsm_lt)
40:45	ROX	IVRM_CORE_VDD_SEQUENCER_FSM: Core iVRM Sequencer for Vdd (ivrm_fsm_lt)
46:51	ROX	IVRM_CORE_VCS_SEQUENCER_FSM: Core iVRM Sequencer for Vcs (ivrm_fsm_lt)
52:57	ROX	IVRM_ECO_VDD_SEQUENCER_FSM: ECO iVRM Sequencer for Vdd (ivrm_fsm_lt)
58:63	ROX	IVRM_ECO_VCS_SEQUENCER_FSM: ECO iVRM Sequencer for Vcs (ivrm_fsm_lt)

Register Name	<i>Refer To The Description Of PFSMM1</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR2_REG
Address	000000001C0F0171 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:6	ROX	RESCLK_BAND_FSM: Band Sequencer for resonant clocking (band_fsm_lt)
7:10	ROX	RESCLK_LOWRES_FSM: Low Resonant Clocking sequencer (lowres_fsm_lt)
11:14	ROX	RESCLK_HIGHRES_FSM: High Resonant Clocking sequencer (highres_fsm_lt)
15:18	ROX	RESCLK_FULLCSB_FSM: Full-CSB Resonant Clocking sequencer (fullcsb_fsm_lt)
19:22	ROX	RESCLK_UPDATE_FSM: Resonant Clocking Update sequencer (update_fsm_lt)
23:29	ROX	IDLE_TRANSITION_FSM: Idle State Sequence FSM (ifsm_lt)
30:37	ROX	Peco_step_target_uv Current ECO Step Target Pstate (different from Plocal_actual for undervolting)
38:45	ROX	Pcore_step_target_uv Current core Step Target Pstate (different from Plocal_actual for sleep and undervolting)

Register Name	<i>Protect Mode Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.PROTECT_MODE_REG
Address	000000001C0F03FE (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	READ_PROTECT_ENABLE: Enable read protection
1	RW	WRITE_PROTECT_ENABLE: Enable write protection

Register Name	<i>Atomic Lock Register</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX12.TP_PCB_SLAVE_INST.ATOMIC_LOCK_REG	
Address	000000001C0F03FF (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	RW	ATOMIC_LOCK_ENABLE: Enable atomic lock
1:4	ROX	ATOMIC_ID: Atomic ID

Register Name	<i>Contains The Slave's Primary Address</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.PRIMARY_ADDRESS_REG	
Address	000000001D0F0000 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RO	Reserved field (Access type is primary_address)

Register Name	<i>Multicast Group 1</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.MULTICAST_GROUP_1	
Address	000000001D0F0001 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST1_GROUP: multicast group1 setting

Register Name	<i>Multicast Group 2</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.MULTICAST_GROUP_2	
Address	000000001D0F0002 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST2_GROUP: multicast group2 setting



Register Name	<i>Multicast Group 3</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.MULTICAST_GROUP_3	
Address	000000001D0F0003 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST3_GROUP: multicast group3 setting

Register Name	<i>Multicast Group 4</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.MULTICAST_GROUP_4	
Address	000000001D0F0004 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST4_GROUP: multicast group4 setting

Register Name	<i>Timeout Select Register</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.TIMEOUT_REG	
Address	000000001D0F0010 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:1	RW	Reserved field (Access type is int_timeout)

Register Name	<i>Assist Interrupt Register</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.ASSIST_INTERRUPT_REG	
Address	000000001D0F0011 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is attn)
1	ROX	Reserved field (Access type is recov)
2	ROX	Reserved field (Access type is xstop)

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Register Name	GP3 Register (NA In PERV CPLT)
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.GP3_REG
Address	000000001D0F0012 (PCB) 000000001D0F0013 (PCB1) 000000001D0F0014 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset
2	RWX	RWX_WAND	RWX_WOR	GLSMUX_RESET: Glsmux reset for test purpose and stuck active mesh protection. Notice no clocks in the EX if this bit is set.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Put the DPLL in test mode.
4	RWX	RWX_WAND	RWX_WOR	PLL_RST: Put PLL in reset state.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYP: Enable PLL bypass.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pcb_access)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	PM_PI_DECODE: Test override for power management. EX chiplet only.
22	RWX	RWX_WAND	RWX_WOR	RESCLK_DIS: Resonant clocking disable.
23:25	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave will report 'Chiplet Offline'.
27	RWX	RWX_WAND	RWX_WOR	TP_LVLTRANS_FENCE: Electrical winkel fence. Mainly used by power management.
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.
29:31	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)



Register Name	<i>Skew Adjust Data</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.CLK_ADJ_REG	
Address	000000001D0F0015 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:15	ROX	

Register Name	<i>Clk Ajust Config</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.CLK_ADJ_SET	
Address	000000001D0F0016 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:31	RW	CLK_ADJ_SET_REG: Clk adj config

Register Name	<i>Vital Scan Out</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.VITAL_SCAN_OUT	
Address	000000001D0F0017 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	

Register Name	<i>Chiplet Heartbeat Register</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.HEARTBEAT_REG	
Address	000000001D0F0018 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	HEARTBEAT_DEAD: Chiplet heartbeat not detected

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Register Name	<i>Lock Indications From PLLs</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.PLL_LOCK_REG
Address	000000001D0F0019 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	ROX	Reserved field (Access type is lock)

Register Name	<i>Attn Interrupt</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.ATTN_INTERRUPT_REG
Address	000000001D0F001A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is attn)

Register Name	<i>Recov Interrupt</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.RECOV_INTERRUPT_REG
Address	000000001D0F001B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is recov)

Register Name	<i>Xstop Interrupt</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.XSTOP_INTERRUPT_REG
Address	000000001D0F001C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is xstop)



Register Name	<i>Slave Config Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.SLAVE_CONFIG_REG
Address	000000001D0F001E (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	CFG_DISABLE_PERV_THOLD_CHECK: Disable pervasive thold check
1	RW	CFG_DISABLE_MALF_PULSE_GEN: Disable pulse generation for malf alert. Switch back to level
2	RW	CFG_STOP_HANG_CNT_SYS_XSTP: Disable hang counter stop for system xstop
3	RW	CFG_DISABLE_CL_ATOMIC_LOCK: Disable atomic lock for chiplet accesses
4	RW	CFG_DISABLE_HEARTBEAT: Disable check for voltage and gridclock in the chiplet
5	RW	CFG_ZERO_DATA: Sent zero data on any error
6:7	RW	
8:12	RW	ERROR_MASK: mask bits for slave error reporting
13:15	RW	

Register Name	<i>Error Capture Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.ERROR_REG
Address	000000001D0F001F (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX_WCLEA R	CE_ERROR: Correctable error on pcb bus
1:3	RWX_WCLEA R	CHIPLET_ERRORS: Errors reported by chiplet 000 = no error 001 = XSCOM command blocked due pending errors 010 chiplet offline 011 partial good 100 invalid address / address error / bad access type 101 clock error 110 parity error / received unexpected packet / wrong packet number 111 timeout This register is for debug purposes only. It only holds meaningful data if it is cleared after each error.
4	RWX_WCLEA R	PARITY_ERROR: Parity error on PCB Interface
5	RWX_WCLEA R	DATA_BUFFER_ERROR: Parity error in data buffer
6	RWX_WCLEA R	ADDR_BUFFER_ERROR: Parity error in address buffer
7	RWX_WCLEA R	PCB_FSM_ERROR: Invalid state error in PCB FSM
8	RWX_WCLEA R	CL_FSM_ERROR: Invalid state error in Chiplet FSM
9	RWX_WCLEA R	INT_RX_FSM_ERROR: Invalid state error in interrupt RX FSM
10	RWX_WCLEA R	INT_TX_FSM_ERROR: Invalid state error in interrupt TX FSM

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Bits	PCB	Field Mnemonic: Description
11	RWX_WCLEAR	INT_TYPE_ERROR: Invalid interrupt type
12	RWX_WCLEAR	CL_DATA_ERROR: Parity error on Chiplet Interface
13	RWX_WCLEAR	INFO_ERROR: Parity error on Chiplet info lines
14	RWX_WCLEAR	UNUSED_0:
15	RWX_WCLEAR	CHIPLET_ATOMIC_LOCK_ERROR: Chiplet atomic lock error
16	RWX_WCLEAR	PCB_INTERFACE_ERROR: Error of pcb interface component for the internal endpoint
17	RWX_WCLEAR	CHIPLET_OFFLINE: Heartbeat check indicated that chiplet is offline
18	RWX_WCLEAR	CHIPLET_GRID_SKITTER: Heartbeat check indicated skitter on the chiplet grid
19	RWX_WCLEAR	GP3_REG_PARITY_ERROR: gp3 register parity bad
20	RWX_WCLEAR	ADDRESS_REG_PARITY_ERROR: address register parity bad
21	RWX_WCLEAR	TIMEOUT_REG_PARITY_ERROR: timeout select register parity bad
22	RWX_WCLEAR	CONFIG_REG_PARITY_ERROR: slave config register parity bad
23	RWX_WCLEAR	CLK_ADJ_REG_PARITY_ERROR: clk adj register parity bad
24	RWX_WCLEAR	DIV_REG_PARITY_ERROR: div register parity bad
25:28	RWX_WCLEAR	PLL_UNLOCK_ERROR: unlock from chiplet pll

Register Name		Hang Pulse Generation Register 0.
Mnemonic		EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.HANG_PULSE_0_REG
Address		000000001D0F0020 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_0: Value of hang pulse 0. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_0: If set to '1', hang pulses are suppressed in case of a xstop



Register Name	<i>Hang Pulse Generation Register 1.</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.HANG_PULSE_1_REG	
Address	000000001D0F0021 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_1: Value of hang pulse 1. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_1: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 2.</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.HANG_PULSE_2_REG	
Address	000000001D0F0022 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_2: Value of hang pulse 2. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_2: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 3.</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.HANG_PULSE_3_REG	
Address	000000001D0F0023 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_3: Value of hang pulse 3. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_3: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 4.</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.HANG_PULSE_4_REG	
Address	000000001D0F0024 (PCB)	
Attributes		
Description		

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Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_4: Value of hang pulse 4. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_4: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 5</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.HANG_PULSE_5_REG
Address	000000001D0F0025 (PCB)
Attributes	
Description	This hang counter is used exclusively to generate the malfunction alert pulse.

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_5: Value of hang pulse 5. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_5: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 6</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.HANG_PULSE_6_REG
Address	000000001D0F0026 (PCB)
Attributes	
Description	This hang counter is exclusively used for heartbeat generation.

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_6: Value of hang pulse 6. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_6: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Divider For Hang Counter Clock</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.PRE_COUNTER_REG
Address	000000001D0F0028 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PRE_COUNTER: Divider for hang counter clock. Divides clock by n+1 (default: n=0)



Register Name		<i>PowerManagement GP0</i>		
Mnemonic		EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PMGP0_REG		
Address		000000001D0F0100 (PCB) 000000001D0F0101 (PCB1) 000000001D0F0102 (PCB2)		
Attributes				
Description				
Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PM_DISABLE: Master Switch for the PowerManagement Macro
1	RWX	WOX_AND	WOX_OR	PMGP0_SPARE_BIT1: spare bit
2	RWX	WOX_AND	WOX_OR	TP_TC_RESTART_CORE_DOMAIN: Kicks off small sequencer in OHA to get chiplet clocks back running for fast sleep without involving PORE. From GP-reg and overridden by PowMan State Machine.
3	RWX	WOX_AND	WOX_OR	DPLL_THOLD: Thold for the DPLL clock domain in the chiplet
4	RWX	WOX_AND	WOX_OR	PERV_THOLD: Thold for the Pervasive clock domain in the chiplet
5	RO	RO	RO	Reserved.
6	RO	RO	RO	Reserved.
7	RWX	WOX_AND	WOX_OR	PM_DPLL_TIMER_ENA: Select a timer instead of the DPLL lock bit for criteria to switch to DPLL. The time is defined by thold_timer_sel.
8	RWX	WOX_AND	WOX_OR	DPLL_LOCK_SENSE: DPLL lock sensitivity control (0=faster lock time, 1=slower lock time)
9	RWX	WOX_AND	WOX_OR	PMGP0_SPARE2: spare bit
10	RWX	WOX_AND	WOX_OR	DPLL_RESET: Reset to DPLL
11	RWX	WOX_AND	WOX_OR	PMGP0_SPARE_BIT11: Spare bit
12:19	RWX	WOX_AND	WOX_OR	DPLL_TESTOUT_CTL: DPLL testout control
20	RWX	WOX_AND	WOX_OR	TP_TC_CACHE2CORE_FENCE: Fence from cache to core domain in EX chiplet
21	RWX	WOX_AND	WOX_OR	TP_TC_CORE2CACHE_FENCE: Fence from core to cache domain in EX chiplet
22	RWX	WOX_AND	WOX_OR	TP_TC_PERVASIVE_ECO_FENCE: Pervasive ECO fence
23	RWX	WOX_AND	WOX_OR	CHKSW_HW257424_DISABLE: Chicken switch for interrupt retry exhausted bug (0=fix enabled, 1=fix disabled)
24:26	RWX	WOX_AND	WOX_OR	TP_CLK_ASYNC_RESET_DC: Clk async reset for three glitchless muxes, and the two clock dividers (bit 0 = master GLM, bit 1 = ECO Div2 and ECO GLM, bit 2= core Div1 and core GLM)
27:29	RWX	WOX_AND	WOX_OR	TP_CLKGLM_SEL_DC: Glitchless Mux Select for primary chiplet clock source (feeding both core and eco clock muxes) 000 = refclk, 001 = DPLL. 100 = Use constant selected by bit 34, else refclk
30	RWX	WOX_AND	WOX_OR	TP_CLKGLM_ECO_SEL_DC: Glitchless Mux Select for eco domain (cache_nclk) grid. 0= follow primary source chosen by previous field: 1 = Use constant selected by bit 34
31	ROX	NC	NC	SPECIAL_WKUP_DONE: Indicates that special wakeup is done, if asserted
32:33	RWX	WOX_AND	WOX_OR	TP_CLKGLM_CORE_SEL_DC: Glitchless Mux Select for core domain (nclk grid) mux. 0b00=primary GLS mux output, 0b10=constant input, 0b01=refclk. Valid transitions are 0b01 <-> 0b00 <-> 0b10, 0b11 is illegal

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
34	RWX	WOX_AND	WOX_OR	TP_CLKGLM_CONST_DC: Constant input available to all three ClkGlm
35:36	RWX	WOX_AND	WOX_OR	THOLD_TIMER_SEL: Selection for the thold transition timer in the IDLE state machine. 0b00=1024 cycles delay, 0b01=512 cycles delay, 0b10=256 cycles delay, 0b11= 128 cycles delay
37	RWX	WOX_AND	WOX_OR	BLOCK_ALL_WAKEUP_SOURCES: Setting this bit will make the PM Slave ignore any Wakeup events (ext. interrupt, malfunction alert, any special wakeup bit). This bit is intended to enable firmware concurrent patch capability. Note: This does NOT block the interrupt from being presented to the processor core. The following procedure is required on changes: 1. Firmware may only set this bit after first setting special wakeup and polling for special wakeup complete (OHA and PCB-slave both in running state with AISS and PM FSMs idle). 2. Firmware may only clear this bit if all special wakeup bits are first cleared.
38	RWX	WOX_AND	WOX_OR	TP_TC_DPLL_TESTMODE_DC: ADPLL test mode
39	RWX	WOX_AND	WOX_OR	PM_SLV_WINKLE_FENCE: Fence off the powered off chiplet in winkle. - Logical fence/hold for pcb_slave and pcb_slave_pm. For electrical fence see bit 23.
40	RWX	WOX_AND	WOX_OR	L3_ENABLE_SWITCH: Setting this bit activates l3_edram_enable if allowed by system configuration GP3(28). Resetting this bit deactivates l3_edram_enable.
41	RWX	WOX_AND	WOX_OR	TP_CPLT_IVRM_REFBYPASS_DC: Signal to iVRM (used to be controlled by scan-only block inside EX, but needs to be driven by VIO domain)
42	RWX	WOX_AND	WOX_OR	CHKSW_HW241939_DISABLE: if this bit is set to 1, the fix for HW241939 (pfet enable SCOM-ability) is disabled
43	RWX	WOX_AND	WOX_OR	CHKSW_HW273115_DISABLE: if this bit is set to 1, the fix for HW273115 (Pga ACK noack issue when the babystepper is in the winkle state) is disabled
44	RWX	WOX_AND	WOX_OR	CHKSW_HW245103_DISABLE: if this bit is set to 1, the fix for HW245103 resonant clocking CSB and SW -bit ordering change is disabled
45	RWX	WOX_AND	WOX_OR	CHKSW_HW257534_DISABLE: if this bit is set to 1, the fix for HW257534 (fencing of errors) is disabled
46	RWX	WOX_AND	WOX_OR	CHKSW_HW259509_ENABLE: if this bit is set to 0, the fix for HW259509 (Pstate change hanging, because of DPLL flock timer in a hung state) is disabled
47	RWX	WOX_AND	WOX_OR	CHKSW_HW260345_DISABLE: if set to 1, this bit disables the HW260345 fix (fix was to make sure that we enter bypass mode for iVRM safe mode without a glitch that could cause Vcs in regulation and Vdd in bypass)
48:49	ROX	NC	NC	WAKEUP_INT_TYPE: (Known to be unreliable and not supported, informational usage only) Type of the last wakeup event that caused an exit from sleep or winkle (excluding nap!), regardless of present state. 0b01: External interrupt. 0b10: Malfunction Alert. 0b11: Special Wakeup. 0b00: chiplet has never fully entered and exited a chiplet-level idle state since IPL of the system. (Note this does not necessarily get updated when the processor core enters an idle state, only if the PCB-Slave enters and then exits the idle state for this chiplet).
50	ROX	NC	NC	DPLL_LOCK: DPLL lock indicator
51	ROX	NC	NC	SPECIAL_WKUP_ALL_SOURCES_ORED: logical OR of all special wakeup sources
52	ROX	NC	NC	REGULAR_WKUP_AVAILABLE: logical OR of external interrupt and malfunction alert



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
53	RWX	WOX_AND	WOX_OR	BLOCK_REG_WKUP_SOURCES: blocks ext. int. and malf. Alert from waking up PCBS (no block possible for PC!)

Register Name	PowerManagement GP1
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PMGP1_REG
Address	000000001D0F0103 (PCB) 000000001D0F0104 (PCB1) 000000001D0F0105 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	SLEEP_POWER_DOWN_EN: Sleep Power Down Enable: When set to 1, causes hardware to automatically reduce voltage to the Core domain when entering Sleep mode. The voltage value for power down is chosen by sleep_power_off_sel (bit 2). When set to 0, a request is sent to the PORE engine for assistance entering Sleep.
1	RWX	WOX_AND	WOX_OR	SLEEP_POWER_UP_EN: Sleep Power Up Enable: When set to 1, enables automated hardware restoration of voltage via PFETs and, if enabled, iVRMs when exiting Sleep mode. If this bit is set to 0 the hardware rely on external means (PORE or equivalent) to restore voltage.
2	RWX	WOX_AND	WOX_OR	SLEEP_POWER_OFF_SEL: Sleep Power Off Select: Selects which voltage level to place the Core domain PFETs upon Sleep entry. 0 = Vret (Fast Sleep Mode), 1 = Voff (Deep Sleep Mode). Depending on the setting of pmicr_latency_en, this bit is controlled with a PCB-write (0) or by the PMICR in the core (1).
3	RWX	WOX_AND	WOX_OR	WINKLE_POWER_DOWN_EN: Winkle Power Down Enable: When set to 1, causes hardware to automatically reduce voltage to the entire Chiplet (both Core and ECO Domains) when entering Winkle mode. The voltage value for power down is chosen by winkle_power_off_sel (bit 5). When set to 0, a request is sent to the PORE engine for assistance entering Winkle.
4	RWX	WOX_AND	WOX_OR	WINKLE_POWER_UP_EN: Winkle Power Up Enable: When set to 1, enables automated hardware PFET enablement when exiting Winkle mode. If this bit is set to 0 the hardware rely on external means (PORE or equivalent) to cause the PFETs to be re-enabled.
5	RWX	WOX_AND	WOX_OR	WINKLE_POWER_OFF_SEL: Winkle Power Off Select: Selects which voltage level to place the Core and ECO domain PFETs upon Winkle entry. 0 = Vret (Fast Winkle Mode), 1 = Voff (Deep Winkle Mode). Depending on the setting of pmicr_latency_en, this bit is controlled with a PCB-write (0) or by the PMICR in the core (1).
6	RWX	WOX_AND	WOX_OR	OHA_WKUP_OVERRIDE_EN: Needs to be 0 for normal operation. If set to 1, the two following dials are used to override the regular and special wakeup signal from PCBS to OHA
7	RWX	WOX_AND	WOX_OR	OHA_PM_WKUP_OVERRIDE: Enablement by 'oha_wkup_override_en' forces the regular wakeup signal to OHA to the value of this bit regardless of presence of an interrupt source.
8	RWX	WOX_AND	WOX_OR	OHA_SPC_WKUP_OVERRIDE: Enablement by 'oha_wkup_override_en' forces the special wakeup signal to OHA to the value of this bit, regardless of the firmware settings.

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
9	RWX	WOX_AND	WOX_OR	ENDP_RESET_PM_ONLY: If asserted, an endpoint reset of all power management-related functions (not the regular PCB slave) is performed. Intended usage is for recovery.
10	RWX	WOX_AND	WOX_OR	DPLL_FREQ_OVERRIDE_ENABLE: override Fmax/Fmin only, if '1', using register FREQ_CTRL_REG
11	RWX	WOX_AND	WOX_OR	PM_SPR_OVERRIDE_EN: PM SPR Override Enable The PPMCR (0xNNNN) and PPMICR (0XXXXX) accesses the register resources that make up the PMCR SPR used by hypervisor to management Pstates. Thus, PCB updates to it are disabled in hardware to prevent collisions. This bit allows ownership of the PMCR to be switched from hypervisor to OCC. This switch is immediate in hardware, thus, firmware must ensure the ownership switch is otherwise communicated. 0 = Disables the writing of the PPMCR (0xNNNN) from the PCB and allows SPR 884 writes (mtspr) to update the register resource. 1 = Enables the writing of the PPMCR (0xNNNN) from the PCB.
12	RWX	WOX_AND	WOX_OR	FORCE_SAFE_MODE: Force Safe Mode 0 = Allow other enabled features to determine the operational Pstate. 1 = Forces the minimum of POHBR[psafe] and PPMSR[global_pstate_actual] Pstate for the core chiplet as the operational frequency.
13	RWX	WOX_AND	WOX_OR	IVRM_SAFE_MODE_EN: Internal VRM Safe Mode Enable 0 = Disable the iVRM safe mode, thus, no automatic actions occur, if an iVRM error happens. 1 = if the iVRMs are enabled (PIVRMCSR[ivrn_en] is set) and Pstates are enabled and if the error defined by dial pcbs_ivrm_gross_or_fine_err occurs, then the railstepper is forced into bypass mode to prevent a voltage-frequency hazard
14	RWX	WOX_AND	WOX_OR	IVRM_SAFE_MODE_FORCE_ACTIVE: Internal VRM Safe Mode Force Dial 0 = the hardware decides whether to activate the iVRM safe mode or not 1 = the iVRM safe mode is forced regardless (this makes only sense if ivrm_fsm_enable=1 and Pstates are enabled)
15	RWX	WOX_AND	WOX_OR	PMICR_LATENCY_EN: Selects how the sleep/winkle latency (which is deep/fast) is controlled. If asserted the PMICR controls the winkle/sleep_power_off_sel in PMGP1, otherwise those bits are controlled via SCOM by OCC.
16	RWX	WOX_AND	WOX_OR	ENABLE_OCC_CTRL_FOR_LOCAL_PSTATE_EFF_REQ: controls, if the HW (for value 0) or OCC (value 1) is in control of the Local Pstate Effective register in PPSTR
17	RWX	WOX_AND	WOX_OR	SERIALIZE_PFET_POWERDOWN: if asserted, the pFET sequencer will sequence the core and the ECO domain one after the other when powering down
18	RWX	WOX_AND	WOX_OR	SERIALIZE_PFET_POWERUP: if asserted, the pFET sequencer will sequence the ECO and the core domain one after the other when powering up
19	RWX	WOX_AND	WOX_OR	DISABLE_FORCE_DEEP_TO_FAST_SLEEP: 0: (normal operation) - If PCB Slave reports a recoverable error or a checkstop, a DEEP sleep operation is forced to FAST. The entries in sleep/winkle_power_off_sel remain unchanged. 1: force to FAST is disabled.



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
20	RWX	WOX_AND	WOX_OR	DISABLE_FORCE_DEEP_TO_FAST_WINKLE: 0: (normal operation) - If PCB Slave reports a recoverable error or a checkstop, a DEEP winkle operation is forced to FAST. The entries in sleep/winkle_power_off_sel remain unchanged. 1: force to FAST is disabled.

Register Name	<i>PFET Control/Status Register For Core And ECO Vdd</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PFVDDCNTLSTAT_REG
Address	000000001D0F0106 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	CORE_VDD_PFET_FORCE_STATE: Core Domain PFET Force State Provides a means for firmware to force the core domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 4:5 = 00 (both core_vdd_pfet_val_override AND core_vdd_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
2:3	RW	ECO_VDD_PFET_FORCE_STATE: ECO Domain PFET Force State Provides a means for firmware to force the ECO domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 6:7 = 00 (both eco_vdd_pfet_val_override AND eco_vdd_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
4	RW	CORE_VDD_PFET_VAL_OVERRIDE: Core Domain PFET Value Override 0 = Override is disabled
5	RW	CORE_VDD_PFET_SEL_OVERRIDE: Core Domain PFET Stage Select Override 0 = Override is disabled
6	RW	ECO_VDD_PFET_VAL_OVERRIDE: ECO Domain PFET Value Override 0 = Override is disabled
7	RW	ECO_VDD_PFET_SEL_OVERRIDE: ECO Domain PFET Stage Select Override 0 = Override is disabled
8	RW	CORE_VDD_PFET_ENABLE_REGULATION_FINGER: Core Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the core_vdd_pfet_enable_value.
9	RW	ECO_VDD_PFET_ENABLE_REGULATION_FINGER: ECO Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the eco_vdd_pfet_enable_value.

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Bits	PCB	Field Mnemonic: Description
10:21	RW	CORE_VDD_PFET_ENABLE_VALUE: Core PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the Core Domain PFET Enables directly. If core_vdd_pfet_val_override = 1, a write to this field sets the state of the core PFET Enables until core_vdd_pfet_val_override is cleared. If core_vdd_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the core_vdd_pfet_valN_slav registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
22:25	RW	CORE_VDD_PFET_SEL_VALUE: Core PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure core_vdd_pfet_valN_slav(0:11) where N is 0 to 11 if core_vdd_pfet_sel_override = 1. If core_vdd_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
26:37	RW	ECO_VDD_PFET_ENABLE_VALUE: ECO PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the ECO PFET Enables directly. If ECO_vdd_pfet_val_override = 1, a write to this field sets the state of the ECO PFET Enables until ECO_vdd_pfet_val_override is cleared. If eco_vdd_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the eco_vdd_pfet_valN_slav registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
38:41	RW	ECO_VDD_PFET_SEL_VALUE: ECO PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure eco_vdd_pfet_valN_slav(0:11) where N is 0 to 11 if eco_vdd_pfet_sel_override = 1. If eco_vdd_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
42:45	ROX	CORE_VDD_PG_STATE: Core power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
46:49	ROX	CORE_VDD_PG_SEL: For debug, contains the actual index n into Core Domain PFET Value [n] SLAT Register set that contains the Core PFET Enable Value currently enabled.
50:53	ROX	ECO_VDD_PG_STATE: ECO Domain power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
54:57	ROX	ECO_VDD_PG_SEL: For debug, contains the actual index n into ECO Domain PFET Value [n] SLAT Register set that contains the ECO PFET Enable Value currently enabled.

Register Name	PFET Sense Register	
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PFSENSE_REG	
Address	000000001D0F0107 (PCB)	
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:11	ROX	TP_CORE_VDD_PFET_ENABLE_SENSE: Not used any more.
12:23	ROX	TP_ECO_VDD_PFET_ENABLE_SENSE: Not used any more.



Bits	PCB	Field Mnemonic: Description
24:35	ROX	TP_CORE_VCS_PFET_ENABLE_SENSE: Not used any more.
36:47	ROX	TP_ECO_VCS_PFET_ENABLE_SENSE: Not used any more.

Register Name	<i>PM Error Summary Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PMERRSUM_REG
Address	000000001D0F0108 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	PM_ERROR: PM Error is present. Intended for use by special PCB multicast to see error state of all chiplets with a single read (via 510F0108 to read all chiplets)

Register Name	<i>PM Error Register:</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PMERR_REG
Address	000000001D0F0109 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_HANG_ERR: Hang during Unassisted Sleep Entry: SLEEP_ENTRY_NOTIFY_PMC state
1	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ASSIST_HANG_ERR: Hang during Assisted Sleep Entry: SLEEP_ENTRY_NOTIFY_PMC_ASSIST state
2	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ERR: Hang during Unassisted Sleep Exit: SLEEP_EXIT_NOTIFY_PMC state
3	ROX	PCBS_SLEEP_EXIT_INVOKE_PORE_ERR: Hang during Assisted Deep Sleep Exit: SLEEP_EXIT_INVOKE_PORE state
4	ROX	PCBS_WINKLE_ENTRY_NOTIFY_PMC_ERR: Hang during Unassisted Winkle Entry: WINKLE_ENTRY_NOTIFY_PMC state
5	ROX	PCBS_WINKLE_ENTRY_SEND_INT_ASSIST_ERR: Hang during Assisted Winkle Entry: WINKLE_ENTRY_SEND_INT_ASSIST state
6	ROX	PCBS_WINKLE_EXIT_NOTIFY_PMC_ERR: Hang during Unassisted Winkle Exit: WINKLE_EXIT_NOTIFY_PMC state
7	ROX	PCBS_WAIT_DPLL_LOCK_ERR: Hang during Unassisted Exit waiting on DPLL: WAIT_DPLL_LOCK state
8	ROX	PCBS_SPARE8_ERR: spare bit, always 0
9	ROX	PCBS_WINKLE_EXIT_SEND_INT_ASSIST_ERR: Hang during Assisted Winkle Exit: WINKLE_EXIT_SEND_INT_ASSIST state
10	ROX	PCBS_WINKLE_EXIT_SEND_INT_POWUP_ASSIST_ERR: Hang during Assisted Winkle Exit: WINKLE_EXIT_SEND_INT_POWUP_ASSIST state
11	ROX	PCBS_WRITE_FSM_GOTO_REG_IN_INVALID_STATE_ERR: write to FSM goto register in invalid state
12	ROX	PCBS_WRITE_PMGP0_IN_INVALID_STATE_ERR: write to PMGP0 in invalid state

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Bits	PCB	Field Mnemonic: Description
13	ROX	PCBS_FREQ_OVERFLOW_IN_PSTATE_MODE_ERR: frequency of DPLL in Pstate mode overflows (Fnom + desired Pstate > 511)
14	ROX	PCBS_ECO_RS_BYPASS_CONFUSION_ERR: ECO railstepper tried to exit Vcs bypass and enter Vdd bypass in one Pstate step (it is not clear, in which order this strange operation should be performed - most likely it should never happen to avoid that Vcs is greater than Vdd)
15	ROX	PCBS_CORE_RS_BYPASS_CONFUSION_ERR: same as previous error, but for core railstepper (it is not clear, in which order this strange operation should be performed - most likely it should never happen to avoid that Vcs is greater than Vdd)
16	ROX	PCBS_READ_LPST_IN_PSTATE_MODE_ERR: read LPST-array while iVRM FSMs are enabled (dial ivrm_fsm_enable asserted)
17	ROX	PCBS_LPST_READ_CORR_ERR: correctable error occurred when reading the LPST
18	ROX	PCBS_LPST_READ_UNCORR_ERR: uncorrectable error occurred when reading the LPST
19	ROX	PCBS_PFET_STRENGTH_OVERFLOW_ERR: overflow occurred when calculating the pFET strength (in final rounding step!)
20	ROX	PCBS_VDS_LOOKUP_ERR: Vds entry not found in lookup table (when performing the linear search!)
21	ROX	PCBS_IDLE_INTERRUPT_TIMEOUT_ERR: idle interrupt timeout in PCB interrupt controller
22	ROX	PCBS_PSTATE_INTERRUPT_TIMEOUT_ERR: PState interrupt timeout in PCB interrupt controller
23	ROX	PCBS_GLOBAL_ACTUAL_SYNC_INTERRUPT_TIMEOUT_ERR: GlobalActualSync Interrupt timeout in PCB interrupt controller
24	ROX	PCBS_PMAX_SYNC_INTERRUPT_TIMEOUT_ERR: PmaxSync Interrupt timeout in PCB interrupt controller
25	ROX	PCBS_GLOBAL_ACTUAL_PSTATE_PROTOCOL_ERR: a write to global actual Pstate register has occurred before the global actual Pstate interrupt has left PCBS
26	ROX	PCBS_PMAX_PROTOCOL_ERR: a write to the Pmax/Pmin register has occurred before the Pmax sync interrupt has left PCB
27	ROX	PCBS_IVRM_GROSS_OR_FINE_ERR: iVRM gross or fine error (details to be found in PCBS_ivrm_Control_Status_Reg)
28	ROX	PCBS_IVRM_RANGE_ERR: iVRM range error (summary bit, details to be found in PCBS_ivrm_Control_Status_Reg)
29	ROX	PCBS_DPLL_CPM_FMIN_ERR: DPLL CPM Fmin error
30	ROX	PCBS_DPLL_DCO_FULL_ERR: DPLL DCO full
31	ROX	PCBS_DPLL_DCO_EMPTY_ERR: DPLL DCO empty
32	ROX	PCBS_DPLL_INT_ERR: DPLL internal error
33	ROX	PCBS_FMIN_AND_NOT_CPMBIT_ERR: dpll_fmin_and_not_cpmbit (ref. to dial cpm_fmin_clip_error_sel on how to configure this)
34	ROX	PCBS_DPLL_FASTER_THAN_FMAX_PLUS_DELTA1_ERR: dpll_faster_than_fmax_plus_delta1 (for characterization, delta1 is configurable with pll_char_delta1)
35	ROX	PCBS_DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2_ERR: dpll_slower_than_fmin_minus_delta2 (for characterization, delta2 is configurable with pll_char_delta2)
36	ROX	PCBS_RESCLK_CSB_INSTR_VECTOR_CHG_IN_INVALID_STATE_ERR: RESCLK CSB instruction vector change while FSMs none idle
37	ROX	PCBS_RESCLK_BAND_BOUNDARY_CHG_IN_INVALID_STATE_ERR: RESCLK Band boundaries change while FSMs none idle
38	ROX	PCBS_OCC_HEARTBEAT_LOSS_ERR: OCC heartbeat loss
39	ROX	PCBS_SPARE39_ERR: spare bit, always 0
40	ROX	PCBS_SPARE40_ERR: spare bit, always 0



Bits	PCB	Field Mnemonic: Description
41	ROX	PCBS_SPARE41_ERR: spare bit, always 0
42	ROX	PCBS_SPARE42_ERR: spare bit, always 0

Register Name	<i>PM Error Mask Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PMERRMASK_REG
Address	000000001D0F010A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_HANG_ERR_MASK: Mask for this error: 1=masked, 0=not masked
1	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ASSIST_HANG_ERR_MASK: Mask for this error: 1=masked, 0=not masked
2	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
3	RW	PCBS_SLEEP_EXIT_INVOKE_PORE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
4	RW	PCBS_WINKLE_ENTRY_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
5	RW	PCBS_WINKLE_ENTRY_SEND_INT_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
6	RW	PCBS_WINKLE_EXIT_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
7	RW	PCBS_WAIT_DPLL_LOCK_ERR_MASK: Mask for this error: 1=masked, 0=not masked
8	RW	PCBS_SPARE8_ERR_MASK: Mask for this error: 1=masked, 0=not masked
9	RW	PCBS_WINKLE_EXIT_SEND_INT_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
10	RW	PCBS_WINKLE_EXIT_SEND_INT_POWUP_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
11	RW	PCBS_WRITE_FSM_GOTO_REG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
12	RW	PCBS_WRITE_PMGPO_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
13	RW	PCBS_FREQ_OVERFLOW_IN_PSTATE_MODE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
14	RW	PCBS_ECO_RS_BYPASS_CONFUSION_ERR_MASK: Mask for this error: 1=masked, 0=not masked
15	RW	PCBS_CORE_RS_BYPASS_CONFUSION_ERR_MASK: Mask for this error: 1=masked, 0=not masked
16	RW	PCBS_READ_LPST_IN_PSTATE_MODE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
17	RW	PCBS_LPST_READ_CORR_ERR_MASK: Mask for this error: 1=masked, 0=not masked
18	RW	PCBS_LPST_READ_UNCORR_ERR_MASK: Mask for this error: 1=masked, 0=not masked
19	RW	PCBS_PFET_STRENGTH_OVERFLOW_ERR_MASK: Mask for this error: 1=masked, 0=not masked
20	RW	PCBS_VDS_LOOKUP_ERR_MASK: Mask for this error: 1=masked, 0=not masked
21	RW	PCBS_IDLE_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
22	RW	PCBS_PSTATE_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
23	RW	PCBS_GLOBAL_ACTUAL_SYNC_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
24	RW	PCBS_PMAX_SYNC_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked

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Bits	PCB	Field Mnemonic: Description
25	RW	PCBS_GLOBAL_ACTUAL_PSTATE_PROTOCOL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
26	RW	PCBS_PMAX_PROTOCOL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
27	RW	PCBS_IVRM_GROSS_OR_FINE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
28	RW	PCBS_IVRM_RANGE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
29	RW	PCBS_DPLL_CPM_FMIN_ERR_MASK: Mask for this error: 1=masked, 0=not masked
30	RW	PCBS_DPLL_DCO_FULL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
31	RW	PCBS_DPLL_DCO_EMPTY_ERR_MASK: Mask for this error: 1=masked, 0=not masked
32	RW	PCBS_DPLL_INT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
33	RW	PCBS_FMIN_AND_NOT_CPMBIT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
34	RW	PCBS_DPLL_FASTER_THAN_FMAX_PLUS_DELTA1_ERR_MASK: Mask for this error: 1=masked, 0=not masked
35	RW	PCBS_DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2_ERR_MASK: Mask for this error: 1=masked, 0=not masked
36	RW	PCBS_RESCLK_CSB_INSTR_VECTOR_CHG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
37	RW	PCBS_RESCLK_BAND_BOUNDARY_CHG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
38	RW	PCBS_OCC_HEARTBEAT_LOSS_ERR_MASK: Mask for this error: 1=masked, 0=not masked
39	RW	PCBS_SPARE39_ERR_MASK: Mask for this error: 1=masked, 0=not masked
40	RW	PCBS_SPARE40_ERR_MASK: Mask for this error: 1=masked, 0=not masked
41	RW	PCBS_SPARE41_ERR_MASK: Mask for this error: 1=masked, 0=not masked
42	RW	PCBS_SPARE42_ERR_MASK: Mask for this error: 1=masked, 0=not masked

Register Name		PM Special Wakeup FSP
Mnemonic		EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PMSPCWKUPFSP_REG
Address		000000001D0F010B (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RW	FSP_SPECIAL_WAKEUP: Chiplet Special Wakeup for FSP Firmware use. NOTE: protocol is required when setting this bit

Register Name		PM Special Wakeup OCC
Mnemonic		EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PMSPCWKUPOCC_REG
Address		000000001D0F010C (PCB)
Attributes		
Description		



Bits	PCB	Field Mnemonic: Description
0	RW	OCC_SPECIAL_WAKEUP: Chiplet Special Wakeup for OCC Firmware use. NOTE: protocol is required when setting this bit

Register Name	<i>PM Special Wakeup Hypervisor</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PMSPCWKUPPHYP_REG
Address	000000001D0F010D (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	PHYP_SPECIAL_WAKEUP: Chiplet Special Wakeup for hypervisor Firmware use. NOTE: protocol is required when setting this bit

Register Name	<i>PFET Control/Status Register For Core And ECO Vcs</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PFVCS_CNTLSTAT_REG
Address	000000001D0F010E (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	CORE_VCS_PFET_FORCE_STATE: Core Domain PFET Force State Provides a means for firmware to force the core domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 4:5 = 00 (both core_vcs_pfet_val_override AND core_vcs_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
2:3	RW	ECO_VCS_PFET_FORCE_STATE: ECO Domain PFET Force State Provides a means for firmware to force the ECO domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 6:7 = 00 (both eco_vcs_pfet_val_override AND eco_vcs_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
4	RW	CORE_VCS_PFET_VAL_OVERRIDE: Core Domain PFET Value Override 0 = Override is disabled
5	RW	CORE_VCS_PFET_SEL_OVERRIDE: Core Domain PFET Stage Select Override 0 = Override is disabled
6	RW	ECO_VCS_PFET_VAL_OVERRIDE: ECO Domain PFET Value Override 0 = Override is disabled
7	RW	ECO_VCS_PFET_SEL_OVERRIDE: ECO Domain PFET Stage Select Override 0 = Override is disabled

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Bits	PCB	Field Mnemonic: Description
8	RW	CORE_VCS_PFET_ENABLE_REGULATION_FINGER: Core Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the core_vcs_pfet_enable_value.
9	RW	ECO_VCS_PFET_ENABLE_REGULATION_FINGER: ECO Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the eco_vcs_pfet_enable_value.
10:21	RW	CORE_VCS_PFET_ENABLE_VALUE: Core PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the Core Domain PFET Enables directly. If core_vcs_pfet_val_override = 1, a write to this field sets the state of the core PFET Enables until core_vcs_pfet_val_override is cleared. If core_vcs_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the core_vcs_pfet_valN_slav registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
22:25	RW	CORE_VCS_PFET_SEL_VALUE: Core PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure core_vcs_pfet_valN_slav(0:11) where N is 0 to 11 if core_vcs_pfet_sel_override = 1. If core_vcs_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
26:37	RW	ECO_VCS_PFET_ENABLE_VALUE: ECO PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the ECO PFET Enables directly. If ECO_vcs_pfet_val_override = 1, a write to this field sets the state of the ECO PFET Enables until ECO_vcs_pfet_val_override is cleared. If eco_vcs_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the eco_vcs_pfet_valN_slav registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
38:41	RW	ECO_VCS_PFET_SEL_VALUE: ECO PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure eco_vcs_pfet_valN_slav(0:11) where N is 0 to 11 if eco_vcs_pfet_sel_override = 1. If eco_vcs_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
42:45	ROX	CORE_VCS_PG_STATE: Core power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
46:49	ROX	CORE_VCS_PG_SEL: For debug, contains the actual index n into Core Domain PFET Value [n] SLAT Register set that contains the Core PFET Enable Value currently enabled.
50:53	ROX	ECO_VCS_PG_STATE: ECO Domain power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
54:57	ROX	ECO_VCS_PG_SEL: For debug, contains the actual index n into ECO Domain PFET Value [n] SLAT Register set that contains the ECO PFET Enable Value currently enabled.



Register Name	<i>PM State History Register For Hypervisor</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPHYP_REG
Address	000000001D0F0110 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	PHYP_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	PHYP_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	PHYP_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	PHYP_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	PHYP_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	PHYP_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For FSP</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PMSTATEHISTFSP_REG
Address	000000001D0F0111 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	FSP_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	FSP_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	FSP_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	FSP_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.



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Bits	PCB	Field Mnemonic: Description
6	ROX_CLRPAR T	FSP_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	FSP_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For OCC</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PMSTATEHISTOCC_REG
Address	000000001D0F0112 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	OCC_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	OCC_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	OCC_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	OCC_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	OCC_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	OCC_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For PerfMon</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPERF_REG
Address	000000001D0F0113 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	PERF_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	PERF_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	PERF_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	PERF_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	PERF_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	PERF_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM FSM Reset And Babystepper Idle Injects</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.IDLEFSMGOTOCMD_REG
Address	000000001D0F0114 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	WO_1P	idle_fsm_goto_cmd ' A write to this reg will proceed the IDLE FSM from WAIT_FOR_PORE_DONE, SLEEP_EXIT_WAIT_FOR_PORE_FAST_EXIT_DONE, or WINKLE_EXIT_WAIT_FOR_PORE_FAST_EXIT_DONE to the following states: ' 0b01: goto IDLE state ' 0b10: goto SLEEP_EXIT_CORE_MESHLET_ON state ' 0b11: goto WINKLE_EXIT_NOTIFY_PMC state ' "
2	RWX	babystp_trigger_sleep_entry ' A write to this reg with a 1 in this field will cause the babystepper to run the sleep entry sequence. This step is needed for an assisted entry into sleep, before the power is actually turned off since the babystepper needs to know about the sleep state. For an unassisted entry, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished entering its sleep mode. ' "
3	RWX	babystp_trigger_winkle_entry ' A write to this reg with a 1 in this field will cause the babystepper to run the winkle entry sequence. This step is needed for an assisted entry into winkle before the power is actually turned off since the babystepper needs to know about the winkle state. For an unassisted entry, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished entering its winkle mode. ' "
4	RWX	babystp_trigger_wakeup ' A write to this reg with a 1 in this field will cause the babystepper to run the wakeup sequence from sleep/winkle depending on the babystepper state of sleep or winkle. This step is needed for an assisted exit from winkle before the power is actually turned off since the babystepper needs to know about the wakeup state. For an unassisted exit, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished waking up from sleep or winkle. ' "

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Register Name	Core PFET Power Up Delay
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.COREPFPUDLY_REG
Address	000000001D0F012C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_POWUP_DLY0: Delay used after transitioning to Core Domain power up sequence stage0. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	CORE_POWUP_DLY1: Delay used after transitioning to Core domain power up sequence stage1.
8:19	RW	CORE_POWER_UP_DELAY_SEL: Vector select for which delay to use for the respective power-up stage. Bit mapping: 8 -> core_*_pfet_enable(0) 9 -> core_*_pfet_enable(1) ... 19 -> core_*_pfet_enable(11) Bit meaning: 0 = Use core_powup_dly0 1 = Use core_powup_dly1

Register Name	Core PFET Power Down Delay
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.COREPFPDDLY_REG
Address	000000001D0F012D (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_POWDN_DLY0: Delay used after transitioning to Core domain power dn sequence stage1. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	CORE_POWDN_DLY1: Delay used after transitioning to Core domain power dn sequence stage1. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
8:19	RW	CORE_POWER_DN_DELAY_SEL: Vector select for which delay to use for the respective power-dn stage. Bit mapping: 8 -> core_*_pfet_enable(0) 9 -> core_*_pfet_enable(1) ... 19 -> core_*_pfet_enable(11) Bit meaning: 0 = Use core_powdn_dly0 1 = Use core_powdn_dly1



Register Name	Core PFET Vretention	
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.COREPFVRET_REG	
Address	000000001D0F0130 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_VRET_SEL: Pointer to the stage representing the Vretention value for the core PFETs. Power down sequences will stop after enabling this stage.
4:7	RW	CORE_VOFF_SEL: Pointer to the stage representing the Voff value for the core PFETs. Power down sequences will stop after enabling this stage.

Register Name	ECO PFET Power Up Delay	
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.ECOPFPUDLY_REG	
Address	000000001D0F014C (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_POWUP_DLY0: Delay used after transitioning to ECO domain power up sequence stage0 in terms of refclk period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	ECO_POWUP_DLY1: Delay used after transitioning to ECO domain power up sequence stage1.
8:19	RW	ECO_POWER_UP_DELAY_SEL: Vector select for which delay to use for the respective power-up stage. Bit mapping: 8 -> eco_*_pfet_enable(0) 9 -> eco_*_pfet_enable(1) ... 19 -> eco_*_pfet_enable(11) Bit meaning: 0 = Use eco_powup_dly0 1 = Use eco_powup_dly1

Register Name	ECO PFET Power Down Delay	
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.ECOPFPDDLY_REG	
Address	000000001D0F014D (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_POWDN_DLY0: UNUSED/SPARE
4:7	RW	ECO_POWDN_DLY1: Delay used after transitioning to ECO Domain power dn sequence stage1. The delays in this register are in terms of refclk period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.

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Bits	PCB	Field Mnemonic: Description
8:19	RW	ECO_POWER_DN_DELAY_SEL: Vector select for which delay to use for the respective power-down stage. Bit mapping: 8 -> eco_*_pfet_enable(0) 9 -> eco_*_pfet_enable(1) ... 19 -> eco_*_pfet_enable(11) Bit meaning: 0 = Use eco_powdn_dly0 1 = Use eco_powdn_dly1

Register Name		<i>ECO PFET Vretention</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.ECOPFVRET_REG
Address		000000001D0F0150 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_VRET_SEL: Pointer to the stage representing the Vretention value for the ECO PFETs. Power down sequences will stop after enabling this stage.
4:7	RW	ECO_VOFF_SEL: Pointer to the stage representing the Voff value for the ECO PFETs. Power down sequences will stop after enabling this stage.

Register Name		<i>Frequency Control Register With Overrides For DPLL</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.FREQ_CTRL_REG
Address		000000001D0F0151 (PCB)
Attributes		
Description		Note that overrides to Dpll_fmax are only applied if Dpll_freq_override_enable = 1. A read of all these dials always returns the currently established DPLL frequencies (regardless of any other mode settings).
Bits	PCB	Field Mnemonic: Description
0:8	RWX	DPLL_FMIN: minimum DPLL frequency in CPM-DPLL mode that is set at IPL time A read always returns the currently established value A write is not conditioned on any other dial setting.
9:17	RWX	DPLL_FMAX: DPLL maximum frequency and frequin (these two values are the same in POWER8 processor) without applying bias values: A read always returns the currently established value A write is conditioned on the setting of dpll_freq_override_enable. If dpll_freq_override_enable is asserted, a write causes this field to update. Otherwise the hardware (that is, PStates) are controlling the update of this value.
18:21	RO	Reserved.
22:30	RW	FREQU_AT_PSTATE0: DPLL frequency for Pstate 0



Register Name	<i>DPLL Mode Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.DPLL_CPM_PARM_REG
Address	000000001D0F0152 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	LF_SLEWRATEXPI: out of lock slew rate for DPLL
8	RW	LF_USE_CPMXPI: use CPM instead of PFD as loop filter input, if '1' (instead of using both)
9	RW	FF_USE_CPMXPI: use the CPM inputs for the frequency filter, if '1'
10	RW	CPM_FILTER_ENABLE: enables the CPM filter
11	RW	FF_BYPASSXPI: enables frequency filter bypass
12	RW	DCO_OVERRIDE: enables overrides for DCO testing/characterization
13	RW	DCO_INCR: enables increment for DCO testing/characterization, increments only on a rising edge
14	RW	DCO_DECR: enables decrement for DCO testing/characterization, decrements only on a rising edge
15:23	RW	DPLL_LOCK_TIMER_REPLACEMENT_VALUE: if dpll_lock_replacement_timer_mode_en is set, this dial specifies the delay in us, after which it is assumed, that the DPLL has reached a frequency lock condition. Note that values less than 3 will cause in undefined HW behavior (0 will cause HANGs!). if dpll_lock_replacement_timer_mode_en is zero, this dial specifies the delay in pcb_nclk cycles after which the hardware monitors the DPLL frequout output (if dpll_freqout_mode_en is set) or the DPLL flock output (if dpll_flock_mode_en is set). Note that in this case, the value of this dial needs to be greater or equal to 150 (decimal).
24:31	RW	PRE_VRET_PSTATE: Pstate that is stepped to before switching to Vretention defined in PCBS_iVRM_Control_Status_Reg
32	RW	OVERRIDE_PCBS_DPLL_SYNCHRONIZER: Bypasses the 'ping-pong' synchronization logic between the DPLL and the PCBS-PM. NEVER SET TO 1 UNLESS YOU KNOW WHAT YOU ARE DOING!
33:36	RW	DPLL_CHAR_DELTA1: Delta in DPLL ticks for characterization (cf. dial dpll_faster_than_fmax_plus_delta1)
37:40	RW	DPLL_CHAR_DELTA2: Delta in DPLL ticks for characterization (cf. dial dpll_faster_than_fmin_minus_delta2)

Register Name	<i>PPMSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_STATUS_REG
Address	000000001D0F0153 (PCB)
Attributes	
Description	Provides read access to the power management status that is also shadowed to the PC and visible to the hypervisor in the PMSR (with some delay due to the shadowing process).

Bits	PCB	Field Mnemonic: Description
0:7	ROX	global_pstate_actual ' Actual Global Pstate Pstate or Pglobal_actual' " Reads from this field return the presently established global PState value." " Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent '

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Bits	PCB	Field Mnemonic: Description
8:15	ROX	LOCAL_PSTATE_ACTUAL: ' Actual Local PState or Plocal_actual' " 'Reads from this field return the presently established local PState value. This value will always be less than or equal to global_pstate_actual.' " 'Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent' "
16:23	ROX	pv_min Minimum Pstate set by the platform.
24:31	ROX	pvf_max Maximum Pstate set by the platform.
32	ROX	spr_em_disabled ' SPR Energy Management Disabled' 'Read from this field indicate whether the platform has disabled the ' 'PMCR and PMICR SPRs to control the chiplet PState. '
33	ROX	Psafe_mode_active Read from this field indicate whether the chiplet has been put into a safe mode with Psafe enabled to a OCC heartbeat loss or other externally forced reasons (0=regular mode, 1=safe mode is active)
34	ROX	iVRM_safe_mode_active Read from this field indicate whether the chiplet has been put the iVRM safe mode (forcing the bypass mode for all iVRMs)
35	ROX	ivrm_enable Read from this field indicate whether the chiplet internal voltage regulation macro is enabled for localized voltage control (0=disabled, 1=enabled) based on ANDing the poweron signals to the iVRMs
36	ROX	all_fsms_in_safe_state For recovery: if this bit is asserted, all Pstate and iVRM control FSMs are in a stable, safe state that allows the recovery routine to proceed with resetting the PCBS PM without the risk of interrupt a critical action
37:40	ROX	pmsr_spares spare bits

Register Name	<i>PIVRMCSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_CONTROL_STATUS_REG
Address	000000001D0F0154 (PCB)
Attributes	
Description	Provides access to chiplet-level controls of the internal VRM rail set (VDD and VCS) across both the core and ECO domains. The following is valid only for bits 4 to 7. When in automatic iVRM mode (ivrm_fsm_enable = 1), these bits provide access to the values established by the automatic hardware mechanism. When In iVRM override mode (ivrm_fsm_enable = 0), these bits allow firmware direct control of the values driving the internal VRMs.

Bits	PCB	Field Mnemonic: Description
0	RW	IVRM_FSM_ENABLE: Internal master VRM FSM Enable 0 = Disable Internal VRM FSMs and enable to control the iVRMs with the available override registers (SCOMable) as a backup mode or for setup (override mode) 1 = Enable Internal VRM FSM sequencers (requires that Pstates are enabled with enable_Pstate_mode=1 as well) (automatic mode)
1	RW	USE_IVRM_FOR_VRET: Internal VRM Enabled for Vretention 0 = Disable Internal VRM for Vretention 1 = Enable Internal VRM for Vretention
2	RW	BINSEARCH_CAL_ENA: trigger binary search (level signal)

Bits	PCB	Field Mnemonic: Description
3	RW	PVREF_EN: Internal VRM Power Voltage Reference Forced Enable 0 = Allow hardware to enable/disable pvref circuit 1 = Force enablement of the pvref circuit
4	RWX	IVRM_CORE_VDD_BYPASS_B: Internal VRM Core VDD Bypass (negative active) 0 = VDD Internal Core VRMs in bypass 1 = VDD internal Core VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
5	RWX	IVRM_CORE_VDD_POWERON: Internal VRM Core VDD Poweron 0 = Core VDD Internal VRMs powered off 1 = Core VDD internal VRMs powered on if this bit is not set (=0), the Core VDD internal VRM powered off internally. If this bit is set (=1), the Core VDD internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
6	RWX	IVRM_CORE_VCS_BYPASS_B: Internal VRM Core VCS Bypass (negative active) 0 = VCS Internal Core VRMs in bypass 1 = VCS internal Core VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VCS internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VCS internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
7	RWX	IVRM_CORE_VCS_POWERON: Internal VRM Core VCS Poweron 0 = Core VCS Internal VRMs powered off 1 = Core VCS internal VRMs powered on if this bit is not set (=0), the Core VCS internal VRM powered off internally. If this bit is set (=1), the Core VCS internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
8	RWX	IVRM_ECO_VDD_BYPASS_B: Internal VRM ECO VDD Bypass (negative active) 0 = VDD Internal ECO VRMs in bypass 1 = VDD internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
9	RWX	IVRM_ECO_VDD_POWERON: Internal VRM ECO VDD Bypass (negative active) 0 = VDD Internal ECO VRMs in bypass 1 = VDD internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.

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Bits	PCB	Field Mnemonic: Description
10	RWX	IVRM_ECO_VCS_BYPASS_B: Internal VRM ECO VCS Bypass (negative active) 0 = VCS Internal ECO VRMs in bypass 1 = VCS internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VCS internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VCS internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
11	RWX	IVRM_ECO_VCS_POWERON: Internal VRM ECO VCS Poweron 0 = ECO VCS Internal VRMs powered off 1 = ECO VCS internal VRMs powered on if this bit is not set (=0), the ECO VCS internal VRM powered off internally. If this bit is set (=1), the ECO VCS internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
12:18	RWX	IVRM_VRET_VDD: if use_ivrm_for_Vret is asserted, this dial is used to control the Vdd retention voltage. Note: this field will establish the Core VDD rail for Sleep and both the Core and ECO rail for Winkle. - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
19:25	RWX	IVRM_VRET_VCS: if use_ivrm_for_Vret is asserted, this dial is used to control the Vcs retention voltage. Note: this field will establish the Core VDD rail for Sleep and both the Core and ECO rail for Winkle. - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
26:30	RWX	IVRM_VRET_CORE_VDD_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the Core Vdd iVRM PFET strength for the retention voltage
31:35	RWX	IVRM_VRET_CORE_VCS_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the Core Vcs iVRM PFET strength for the retention voltage
36:40	RWX	IVRM_VRET_ECO_VDD_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the ECO Vdd iVRM PFET strength for the retention voltage
41:45	RWX	IVRM_VRET_ECO_VCS_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the ECO Vcs iVRM PFET strength for the retention voltage
46	RW	PVREF_FAIL: voltage reference fail input to iVRMs
47	ROX	IVRM_PREF_ERROR_GROSS: Voltage Reference Gross Error 0 = Gross Error not detected 1 = Gross Error detected
48	ROX	IVRM_PREF_ERROR_FINE: Voltage Reference Fine Error 0 = Fine Error not detected 1 = Fine Error detected
49	ROX	IVRM_CORE_VDD_RANGE_HI: Core VDD Internal VRM Range Hi Indicator 0 = Core VDD Internal VRM Hi indicator signal not asserted 1 = Core VDD internal VRMs Hi indicator signal asserted
50	ROX	IVRM_CORE_VDD_RANGE_LO: Core VDD Internal VRM Range Low Indicator 0 = Core VDD Internal VRM Low indicator signal not asserted 1 = Core VDD internal VRMs Low indicator signal asserted

Bits	PCB	Field Mnemonic: Description
51	ROX	IVRM_ECO_VDD_RANGE_HI: ECO VDD Internal VRM Range Hi Indicator 0 = ECO VDD Internal VRM Hi indicator signal not asserted 1 = ECO VDD internal VRMs Hi indicator signal asserted
52	ROX	IVRM_ECO_VDD_RANGE_LO: ECO VDD Internal VRM Range Low Indicator 0 = ECO VDD Internal VRM Low indicator signal not asserted 1 = ECO VDD internal VRMs Low indicator signal asserted
53	ROX	IVRM_CORE_VCS_RANGE_HI: Core VCS Internal VRM Range Hi Indicator 0 = Core VCS Internal VRM Hi indicator signal not asserted 1 = Core VCS internal VRMs Hi indicator signal asserted
54	ROX	IVRM_CORE_VCS_RANGE_LO: Core VCS Internal VRM Range Low Indicator 0 = Core VCS Internal VRM Low indicator signal not asserted 1 = Core VCS internal VRMs Low indicator signal asserted
55	ROX	IVRM_ECO_VCS_RANGE_HI: ECO VCS Internal VRM Range Hi Indicator 0 = ECO VCS Internal VRM Hi indicator signal not asserted 1 = ECO VCS internal VRMs Hi indicator signal asserted
56	ROX	IVRM_ECO_VCS_RANGE_LO: ECO VCS Internal VRM Range Low Indicator 0 = ECO VCS Internal VRM Low indicator signal not asserted 1 = ECO VCS internal VRMs Low indicator signal asserted
57	ROX	BINSEARCH_CAL_DONE: binary search done signal
58	RWX	IVRM_CORE_VDD_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
59	RWX	IVRM_CORE_VCS_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
60	RWX	IVRM_ECO_VDD_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
61	RWX	IVRM_ECO_VCS_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
62	RW	IVRM_POWER_DOWN_DISABLE: If this bit is 1, the iVRM poweron signal is left asserted. Power off of the iVRMs is then blocked

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Register Name	PIVRMVSR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VALUE_SETTING_REG
Address	000000001D0F0155 (PCB)
Attributes	
Description	Allows access to VID values and PFET strength valid signal settings presented to the internal VRM rail set (VDD and VCS) across both the core and ECO domains. When in <code>ivrm_fsm_enable = "auto"</code> mode, this register provides access to the values established by the automatic hardware mechanism. When <code>ivrm_fsm_enable = "override"</code> mode, this register allows firmware direct control of the values driving the internal VRMs which, if the VRMs are not in bypass, will move the voltage settings.

Bits	PCB	Field Mnemonic: Description
0:7	RWX	IVRM_CORE_VDD_IVID: When read, returns the value presently being driving to the Core VDD iVRM. If <code>ivrm_fsm_enable = 0</code> (override_mode), then writes to this field will drive a new VID value to the Core VDD iVRM. If <code>ivrm_fsm_enable = 1</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
8:15	RWX	IVRM_CORE_VCS_IVID: When read, returns the value presently being driving to the Core VCS iVRM. If <code>ivrm_fsm_enable = 0</code> (override_mode), then writes to this field will drive a new VID value to the Core VCS iVRM. If <code>ivrm_fsm_enable = 1</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
16:23	RWX	IVRM_ECO_VDD_IVID: When read, returns the value presently being driving to the Core VDD iVRM. If <code>ivrm_fsm_enable = 0</code> (override_mode), then writes to this field will drive a new VID value to the ECO VDD iVRM. If <code>ivrm_fsm_enable = 1</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
24:31	RWX	IVRM_ECO_VCS_IVID: When read, returns the value presently being driving to the ECO VCS iVRM. If <code>ivrm_fsm_enable = 0</code> (override_mode), then writes to this field will drive a new VID value to the ECO VCS iVRM, If <code>ivrm_fsm_enable = 0</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
32:36	RWX	IVRM_CORE_VDD_PFET_STRENGTH: When read, returns the value presently being driving to the core VCS iVRM. If <code>ivrm_fsm_enable = 0</code> (override_mode), then writes to this field will drive a new strength value to the core VCS iVRM, If <code>ivrm_fsm_enable = 0</code> , writes to this field are not performed.

Bits	PCB	Field Mnemonic: Description
37:41	RWX	IVRM_CORE_VCS_PFET_STRENGTH: This register is assigned to the signals tcex##_tp_ivrm_core_vcs_sense & tcex##_tp_ivrm_core_vdd_sense & tcex##_tp_ivrm_eco_vcs_sense & tcex##_tp_ivrm_eco_vdd_sense & 0b0 Note that all other sense signals are spares now and tied to 0. OUTDATED TEXT: When read, returns the value presently being driving to the core VDD iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the core VDD iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
42:46	RWX	IVRM_ECO_VDD_PFET_STRENGTH: When read, returns the value presently being driving to the ECO VCS iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the ECO VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
47:51	RWX	IVRM_ECO_VCS_PFET_STRENGTH: When read, returns the value presently being driving to the ECO VDD iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the ECO VDD iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
52	RWX	IVRM_VDD_CORE_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the Core VDD iVRM. If ivrm_fsm_enable = 1 AND ivrm_control_mode = 1 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the Core VDD iVRM, If ivrm_fsm_enable = 0 OR ivrm_control_mode = 0, writes to this field are not performed.
53	RWX	IVRM_VCS_CORE_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the Core VCS iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the Core VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
54	RWX	IVRM_VDD_ECO_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the ECO VDD iVRM. If ivrm_fsm_enable = 1 AND ivrm_control_mode = 1 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the ECO VDD iVRM, If ivrm_fsm_enable = 0 OR ivrm_control_mode = 0, writes to this field are not performed.
55	RWX	IVRM_VCS_ECO_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the ECO VCS iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the ECO VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
56	RWX	CORE_VDD_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
57	RWX	CORE_VCS_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
58	RWX	ECO_VDD_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
59	RWX	ECO_VCS_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.

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Register Name		General PCBS Modes And Chicken Switches
Mnemonic		EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBSPM_MODE_REG
Address		000000001D0F0156 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RW	ENABLE_PSTATE_MODE: if asserted, Pstate requests (from overrides or PMCR) will be honored, otherwise, the hardware does not do anything. Note to firmware: this is the master switch for Pstates and should be asserted after all sub-modes (that is, lvrn_fsm_en) are setup to avoid enabling unintentional modes during the mode setup.
1	RW	GLOBAL_PSTATE_CHANGE_FOR_IDLE_STATE_ENABLED: if asserted, a global Pstate change to the Nap/Sleep/Winkle-Pstate is requested, when the Nap/Sleep/Winkle state is entered and the individual enable bits in the PIMCR are asserted
2	RW	ENABLE_GLOBAL_PSTATE_REQ: if '1' then enable PMC interrupt with global Pstate change request, otherwise, disable global requests
3	RW	ENABLE_WINKLE_WITH_CPM_MODE: if '1', PCBS automatically changes the DPLL mode to mode 1, when entering winkle, but changes the mode back to CPM mode when exiting. Needed for CPM-DPLL control loop enablement.
4	RW	ENABLE_CLIPPING_OF_GLOBAL_PSTATE_REQ: if '1', PCBS automatically clips global Pstate requests with Pvf_max in PPMBR and sets the 'donate' bit in the interrupt accordingly
5	RW	CHKSW_HW214553: if deasserted, HW214553 (frequin issue in resclk mode) is fixed, if asserted, the fix is not active
6	RW	ENABLE_PMC_PMAX_SYNC_NOTIFICATION: if asserted, the PCBS-PM will send a 'Pmax_sync' interrupt, once the synchronization criterion is met
7	RW	DPLL_LOCK_REPLACEMENT_TIMER_MODE_EN: Select a timer instead of the DPLL lock bit as target frequency reached criterion. This timer has to be setup by the dial dpll_lock_timer_replacement_value. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
8	RW	DPLL_FREQOUT_MODE_EN: Looks at the DPLL frequout to find out, if the target frequency has been reached. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
9	RW	DPLL_FLOCK_MODE_EN: Looks at the real DPLL flock output to find out, if the target frequency has been reached. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
10	RW	ENABLE_SENSE_DELAY_CHARACTERIZATION: If this switch is 0, the sense latches are updated every cycle. If this switch is 1, the sense delay measurement mode is enabled, that starts a sense delay timer, whenever one of the registers that drive the inputs of the iVRMs/pFETs is written via PCB and that triggers a sense register freeze operation, when the sense delay timer reaches the value sense_delay_timer_val. With this mode, the sense delays can be measured in multiples of the PCB-slave clock speed.
11:17	RW	SENSE_DELAY_TIMER_VAL: See the description of enable_sense_delay_characterization for details.
18:19	RW	CPM_FMIN_CLIP_ERROR_SEL: This dial selects, which of the following conditions will cause the FIR bit dpll_fmin_and_not_cpmbit to be set to detect, that the DPLL runs at Fmin, but is still clipped by the CPMs. 0b00 = function is disabled 0b01 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit2 = 0 0b10 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit1 = 0 0b11 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit0 = 0
20:23	RW	DBG_TRACE_SEL: This dial selects the group of signals to be traced for debug in the lab. Details to be found in the Section 'Trace Bus'

Bits	PCB	Field Mnemonic: Description
24:25	RW	TRACE_DATA_SEL: This dial selects the group of signals to be traced for debug in the lab. Details to be found in the Section 'Trace Bus'
26:29	RW	TP_CPLT_IVRM_VPP_TUNE: Tune bits to be set going to the iVRMs

Register Name	<i>PIVRMPS Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_PFETSTR_SENSE_REG
Address	000000001D0F0157 (PCB)
Attributes	
Description	Used to check that the pFET sense outputs correspond to the driven values (mainly for test).

Bits	PCB	Field Mnemonic: Description
0:4	ROX	IVRM_CORE_VDD_PFETSTR_SNS: Not used any more.
5:9	ROX	IVRM_CORE_VCS_PFETSTR_SNS: This register is assigned to the signals tcex##_tp_ivrm_core_vcs_sense & tcex##_tp_ivrm_core_vdd_sense & tcex##_tp_ivrm_eco_vcs_sense & tcex##_tp_ivrm_eco_vdd_sense & 0b0
10:14	ROX	IVRM_ECO_VDD_PFETSTR_SNS: Not used any more.
15:19	ROX	IVRM_ECO_VCS_PFETSTR_SNS: Not used any more.
20	ROX	IVRM_VDD_CORE_PFETSTR_VALID_SNS: Not used any more.
21	ROX	IVRM_VCS_CORE_PFETSTR_VALID_SNS: Not used any more.
22	ROX	IVRM_VDD_ECO_PFETSTR_VALID_SNS: Not used any more.
23	ROX	IVRM_VCS_ECO_PFETSTR_VALID_SNS: Not used any more.
24	ROX	CORE_VDD_BYPASS_B_SENSE: Not used any more.
25	ROX	CORE_VCS_BYPASS_B_SENSE: Not used any more.
26	ROX	ECO_VDD_BYPASS_B_SENSE: Not used any more.
27	ROX	ECO_VCS_BYPASS_B_SENSE: Not used any more.
28	ROX	CORE_VDD_POWERON_SENSE: Not used any more.
29	ROX	CORE_VCS_POWERON_SENSE: Not used any more.
30	ROX	ECO_VDD_POWERON_SENSE: Not used any more.
31	ROX	ECO_VCS_POWERON_SENSE: Not used any more.
32	ROX	CORE_VDD_VPUMP_EN_SENSE: Not used any more.
33	ROX	CORE_VCS_VPUMP_EN_SENSE: Not used any more.
34	ROX	ECO_VDD_VPUMP_EN_SENSE: Not used any more.
35	ROX	ECO_VCS_VPUMP_EN_SENSE: Not used any more.
36	ROX	CORE_VDD_PFET_LOW_VOUT_SNS: Not used any more.
37	ROX	CORE_VCS_PFET_LOW_VOUT_SNS: Not used any more.
38	ROX	ECO_VDD_PFET_LOW_VOUT_SNS: Not used any more.
39	ROX	ECO_VCS_PFET_LOW_VOUT_SNS: Not used any more.

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Register Name	PPMICR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_IDLE_CONTROL_REG
Address	000000001D0F0158 (PCB)
Attributes	
Description	Used to read the PMICR register typically owned (written) by the hypervisor. Writes are conditioned on the setting of the dial Pm_spr_override_en. If Pm_spr_override_en is set, firmware must make sure that the special wakeup state of this chiplet is reached before changing any of the latency fields in this register. Otherwise, the hardware behavior is undefined.

Bits	PCB	Field Mnemonic: Description
0:7	ROX	NAP_PSTATE_REQ: Nap Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
8	ROX	NAP_PSTATE_EN: Nap PState Enable 1 = Enable the Nap Pstate (NPS) Request, Nap Global Enable and Nap Latency functions 0 = Disables the Nap Pstate (NPS) Request, Nap Global Enable and Nap Latency functions Reads from the field return the value last written.
9	ROX	NAP_GLOBAL_EN: Nap Global Enable 1 = Upon the execution of a Nap instruction , the Nap Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a Nap instruction , the Nap Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.
10:11	ROX	NAP_LATENCY: Nap Latency not supported for POWER8 processor
12:15	ROX	RESERVED_PPMICR_0: reserved
16:23	ROX	SLEEP_PSTATE_REQ: sleep Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
24	ROX	SLEEP_PSTATE_EN: sleep PState Enable 1 = Enable the sleep Pstate (NPS) Request, sleep Global Enable and sleep Latency functions 0 = Disables the sleep Pstate (NPS) Request, sleep Global Enable and sleep Latency functions Reads from the field return the value last written.
25	ROX	SLEEP_GLOBAL_EN: sleep Global Enable 1 = Upon the execution of a sleep instruction , the sleep Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a sleep instruction , the sleep Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.

Bits	PCB	Field Mnemonic: Description
26:27	ROX	SLEEP_LATENCY: sleep Latency 00 = Cease instructions and honors Pstate change but does not perform additional state changing actions (unsupported in POWER8, maps to 0b10) 01 = Indicates to the platform that a sub-state that would have the lowest latency is enabled (unsupported in POWER8, maps to 0b10) 10 = Indicates to the platform that a sub-state that might have a medium exit latency is enabled (POWER8: Fast Sleep) 11 = Indicates to the platform that a sub-state that might have higher exit latency is enabled (POWER8: Deep Sleep)
28:31	ROX	RESERVED_PPMICR_1: reserved
32:39	ROX	WINKLE_PSTATE_REQ: winkle Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
40	ROX	WINKLE_PSTATE_EN: winkle PState Enable 1 = Enable the winkle Pstate (NPS) Request, winkle Global Enable and winkle Latency functions 0 = Disables the winkle Pstate (NPS) Request, winkle Global Enable and winkle Latency functions Reads from the field return the value last written.
41	ROX	WINKLE_GLOBAL_EN: winkle Global Enable 1 = Upon the execution of a winkle instruction , the winkle Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a winkle instruction , the winkle Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.
42:43	ROX	WINKLE_LATENCY: winkle Latency 00 = Cease instructions and honors Pstate change but does not perform additional state changing actions (unsupported in POWER8, maps to 0b10) 01 = Indicates to the platform that a sub-state that would have the lowest latency is enabled (unsupported in POWER8, maps to 0b10) 10 = Indicates to the platform that a sub-state that might have a medium exit latency is enabled (POWER8: Fast Winkle) 11 = Indicates to the platform that a sub-state that might have higher exit latency is enabled (POWER8: Deep Winkle)
44:47	ROX	RESERVED_PPMICR_2: reserved

Register Name	PPMCR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_CONTROL_REG
Address	000000001D0F0159 (PCB)
Attributes	
Description	Provides read access to the PMCR register shadow in the PCBS, typically owned (written) by the hypervisor. Writes are conditioned on the setting of PMGP1[pm_spr_override_en].

Bits	PCB	Field Mnemonic: Description
0:7	RWX	GLOBAL_PSTATE_REQ: global Pstate request from hypervisor (or OCC)
8:15	RWX	LOCAL_PSTATE_REQ: local Pstate request from hypervisor or OCC
16	RWX	AUTO_OVERRIDE0_PSTATE_LIMIT_EN: automatic override Pstate 0 (for low activity detection) is enabled, if asserted



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Bits	PCB	Field Mnemonic: Description
17	RWX	AUTO_OVERRIDE1_PSTATE_LIMIT_EN: automatic override Pstate 1 (reserved for future use) is enabled, if asserted
18:23	RWX	RESERVED_PPMCR: reserved
24:31	RWX	AUTO_OVERRIDE_PSTATE0: automatic override Pstate 0 (for low activity detection)
32:39	RWX	AUTO_OVERRIDE_PSTATE1: automatic override Pstate 1 (reserved for future use)

Register Name	<i>Control Register That Is Written By PMC Sequencer</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_PMC_VF_CTRL_REG
Address	000000001D0F015A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PGLOBAL_ACTUAL: global actual Pstate
8:15	RW	MAXREGVCS: maximum regulation point for Vcs, Bit 0 is reserved, bits 1 to 7 are in iVID format
16:23	RW	MAXREGVDD: maximum regulation point for Vdd, Bit 0 is reserved, bits 1 to 7 are in iVID format
24:31	RW	EVIDVCS_EFF: eff. external voltage ID for Vcs in iVID format, Bit 0 is reserved
32:39	RW	EVIDVDD_EFF: eff. external voltage ID for Vdd in iVID format, Bit 0 is reserved

Register Name	<i>Undervolting Register For PCBS</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_UNDERVOLTING_REG
Address	000000001D0F015B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PUV_MIN: minimum Pstate for which undervolting is allowed
8:15	RW	PUV_MAX: maximum Pstate for which undervolting is allowed
16:21	RW	KUV: this value indicates how many Pstate ticks a voltage request is undervolted (clipped with Puv_min). Note that the Kuv value is signed

Register Name	<i>PPSIBR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_INDEX_BOUND_REG
Address	000000001D0F015C (PCB)
Attributes	
Description	Enables setting the minimum and maximum Pstate that is supported as a pointer into the local Pstate table (which has entries from 0 to 127).

Bits	PCB	Field Mnemonic: Description
0:7	RW	LPSI_MIN: this Pstate index is the index that corresponds to array entry 0. Note that the index domain is obtained by adding 128 to a Pstate, thus, the value is unsigned.
8:14	RW	LPSI_ENTRIES_MINUS_1: this dial contains the value of the number of entries in the Pstate table minus 1

Register Name	<i>PPMBR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_BOUNDS_REG
Address	000000001D0F015D (PCB)
Attributes	
Description	Enables setting the Pstate bounds that are managed by the OCC. If dial Enable_pmc_pmax_sync_notification is set, firmware must wait after each write to this register until the PMC has received the Pmax Sync Interrupt. If a write happens to this register while the previously scheduled Pmax Sync Interrupt has not yet left PCBs, the error TBD will be set.

Bits	PCB	Field Mnemonic: Description
0:7	RW	PMIN_CLIP: minimum Pstate allowed for this chiplet
8:15	RW	PMAX_CLIP: maximum Pstate allowed for this chiplet (has to be greater or equal to Pmin_clip)

Register Name	<i>The PPTCR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_CTRL_REG
Address	000000001D0F015E (PCB)
Attributes	
Description	Controls the address for writing the local Pstate table array (all 96 words are accessible). Note that the protocol requires this register to be set up with the Pstate address first, if a read or a write of the Pstate array is intended, to make sure that the initial address is set correctly. The register PPTR must always be written or read afterward. Note that any access to the PPTR auto-increments this register.

Bits	PCB	Field Mnemonic: Description
0:6	RWX	PSTATE_TABLE_ADDRESS: This is the address of the Pstate table in PCBs, which is auto-incremented after any access to the PTLR.

Register Name	<i>PPTR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_REG
Address	000000001D0F015F (PCB)
Attributes	
Description	Controls the data to be written into the Pstate table and returns the data for a read of the Pstate table. Note that the protocol requires for a write to set this register up after first setting up PPTCR (if the user does not rely on the auto-increment function of the address). For a read of the Pstate table, this register must be read after first setting up PPTCR as well (again if the auto-increment feature of the address is not used). Any access to this register auto-increments the Pstate_table_address by 1. Note also that the read functionality of this register is only functional if PIVRMCSR[ivrm_fsm_enable] = 0. The write functionality works in any case.

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Bits	PCB	Field Mnemonic: Description
0:63	RW	pstate_data This is the field for data bits 0 to 63

Register Name	PPSTR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_STEP_TARGET_REG
Address	000000001D0F0160 (PCB)
Attributes	
Description	Provides read access to several intermediate values in the Pstate computation pipeline. Writes are conditioned on the setting of PMGP0[enable_OCC_ctrl_for_local_Pstate_eff_req].

Bits	PCB	Field Mnemonic: Description
0:7	RWX	LOCAL_PSTATE_EFF_REQ: this field represents the effective local Pstate request right before the clipping with Pmin and Pmax if enable_OCC_ctrl_for_local_Pstate_eff_req=0 then the hardware controls this dial, that updates every cycle if enable_OCC_ctrl_for_local_Pstate_eff_req=1 then OCC is in control and can write this field to control the effective local Pstate request that will eventually propagate through the downstream logic and determine the Local PState Actual. Note: if no write to this register is performed, the currently established value is maintained stable forever.
8:15	ROX	LOCAL_PSTATE_TARGET: This field is the target Pstate of a complete Pstate change that is performed in smaller steps
16:23	ROX	LOCAL_CORE_PSTATE_STEP_TARGET: this field represents the intermediate value that is about to be established as the next Local Pstate Actual after completing one step in the process of the transition towards the 'local_Pstate_target' the new voltage, frequency, and clock resonance setting
24:31	ROX	LOCAL_ECO_PSTATE_STEP_TARGET: this field represents the intermediate value that is about to be established as the next Local Pstate Actual after completing one step in the process of the transition towards the 'local_Pstate_target' the new voltage, frequency, and clock resonance setting

Register Name	Read-Only Status Register For DPLL And For Debugging (PDSR)
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_DPLL_STATUS_REG
Address	000000001D0F0161 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:14	ROX	DPLL_FF_FREQOUT: frequout output from DPLL (current frequency - bits 2 to 10 correspond to the same scale as the 9 bits of frequin (which need to be multiplied with our frequency step to get the real frequency), the remaining bits just provide a higher accuracy)
15	ROX	DPLL_FREQU_CHANGE: DPLL Frequency change (pin of DPLL without filter)
16	ROX	DPLL_STATUS_SPARE_BIT1: Spare bit.
17	ROX	PMAX_SYNC_PENDING: gets asserted, if the logic has a Pmax sync interrupt outstanding that will be eventually sent to PMC when the Pmax sync criterion is met
18	ROX	GA_ACK_PENDING: gets asserted, if the logic has a global actual Pstate update acknowledgment interrupt outstanding that will be eventually sent to PMC when the GA ack criterion is met
19:26	ROX	CAPPED_GLOBAL_PSTATE_REQ: corresponds to the capped global Pstate request that is presented as Pstate interrupt and send to PMC



Bits	PCB	Field Mnemonic: Description
27	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT2: DPLL runs at Fmax and CPM bit 2 is set. Note that this bit and the following 2 bits indicate, that the CPMs would allow the DPLL to run faster than Fmax.
28	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT3: DPLL runs at Fmax and CPM bit 3 is set
29	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT4: DPLL runs at Fmax and CPM bit 4 is set
30	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT2: DPLL runs at Fmin and CPM bit2 is zero. Note that this bit and the following 2 bits indicate, that the CPMs indicate, that the DPLL should run slower than the currently established Fmin.
31	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT1: DPLL runs at Fmin and CPM bit1 is zero
32	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT0: DPLL runs at Fmin and CPM bit0 is zero
33	ROX_CLRPAR T	DPLL_FASTER_THAN_FMAX_PLUS_DELTA1: The DPLL indicated that it ran once faster than Fmax+dpll_char_delta1
34	ROX_CLRPAR T	DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2: The DPLL indicated that it ran once slower than Fmin-dpll_char_delta2
35:48	ROX	DPLL_MAX_FREQOUT_AFTER_LAST_READ: This dial indicates the maximum DPLL frequout value after the last read of this register (only 14 MSBs)
49:62	ROX	DPLL_MIN_FREQOUT_AFTER_LAST_READ: This dial indicates the minimum DPLL frequout value after the last read of this register (only 14 MSBs)

Register Name	<i>The PIVRMVCR0 Controls The Voltage Stepping Delays</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG0
Address	000000001D0F0162 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	IVRM_REQ_PSTATE_STEPDELAY_RISING: Requested Internal Pstate Baby Step Delay - Rising Step. Delay before allowing the next step for a rising Pstate Transition. This dial and ivrm_req_Pstate_stepdelay_lowering allow for differing delays for the two directional transitions if necessary. In 100ns units as established by scan dial ivrm_100ns_value
8:15	RW	IVRM_REQ_PSTATE_STEPDELAY_LOWERING: Requested Internal Pstate Baby Step Delay - Lowering Step. Delay before allowing the next step for a lower Pstate Transition. This dial and ivrm_req_Pstate_stepdelay_rising allow for differing delays for the two directional transitions if necessary. In 100ns units as established by scan dial ivrm_100ns_value

Register Name	<i>The PIVRMVCR1 Controls The Voltage Stepping Delays</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG1
Address	000000001D0F0163 (PCB)
Attributes	
Description	

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Bits	PCB	Field Mnemonic: Description
0:7	RW	IVRM_STABILIZE_DELAY_RUN: Stabilization Delay - Run Time Delay to allow a rail to stabilize upon a baby step while the region is operational. In 100ns units as established by scan dial ivrm_100ns_value
8:15	RW	IVRM_STABILIZE_DELAY_IDLE: Stabilization Delay - Idle Transition Delay to allow a rail to stabilize upon a baby step during an idle transition where the activity in the region is quiesced. In 100ns units as established by scan dial ivrm_100ns_value
16:23	RW	IVRM_PFSTR_PROP_DELAY: PFET Strength Propagation Delay Time from PFET Strength values being launched till PFET Strength Valid is asserted. In order to ensure like rails across domains (Core VDD<>ECO VDD, Core VCS<>ECO VCS) are in sync during operational mode, this time value applies to all rails across the domains. This parameter allows for PFET Strength values to settle before PFET Strength Valid is sampled in the Uregs. The value set must the maximum delay for the worst rail timing and must allow for any metastability settling (for example, normally 2-3 cycles for single signals in an asynch handshake interface)
24:31	RW	IVRM_PFSTRVALID_PROP_DELAY: PFETStrength Valid Propagation Delay Time from ivrm_pfstr_prop_delay expiring to where PFET Strength Valid is deasserted. The value is the maximum of a) the minimum pulse width required for PFETStrength Valid and b) the propagation of PFETStrength Valid through (or enough of) the daisy chain. In order to ensure like rails across domains (Core VDD<>ECO VDD, Core VCS<>ECO VCS) are in sync during operational mode, this time value applies to all rails across the domains and thus must be the set to the value of the worst (slowest) rail. The minimum pulse width cannot be violated. The propagation delay can be tuned for more aggressive timing (for example, de-assert before the actual propagation is complete). Measured in prv_nclk cycles. The min delay is 2 cycles. Additional delay can be configured with the following settings 0x00 = No additional delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks
32:39	RW	IVRM_VPUMP_POWERON_TIME: iVRM (VRreg and UReg) - Vpump Power On Time Time necessary for the distributed internal VRM macro circuits to power on. Same delay is required for power on voltage pump circuit. Both delays are in the 8us range. In 100ns units as established by scan dial ivrm_100ns_value
40:47	RW	IVRM_BYPASS_DELAY: iVRM Bypass Propagation Delay Delay time for bypass_b signal propagation. Measured in prv_nclk cycles Target: 50ns 0x00 = No delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks

Bits	PCB	Field Mnemonic: Description
48:55	RW	PFET_VPUMP_ENABLE_DELAY: PFET and Vpump Enable Propagation Delay Delay time for PFET enable and vpump enable signal propagation. Target: 130ns Measured in prv_nclk cycles 0x00 = No delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks
56:62	RW	IVRM_VID_VOUT_THRESHOLD: VID threshold If the output voltage (Vout) is targeting a value below this threshold the slow PFET can backed off from its normal drive strength so as to reduce the ripple at these lower voltage conditions

Register Name	POHR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_OCC_HEARTBEAT_REG
Address	000000001D0F0164 (PCB)
Attributes	
Description	Controls the behavior of the OCC heartbeat function.

Bits	PCB	Field Mnemonic: Description
0:7	RW	occ_heartbeat_time 'OCC Heartbeat Time Value' " 'This field defines the number of ~64us hang timer pulses in which a a PCB read or write of the heartbeat trigger register (of which the offset is specified by dial occ_heartbeat_reg_addr_offset) is not detected that will constitute the loss of the OCC heartbeat. If occ_heartbeat_en is set and upon this loss detection, POHBR[psafe] is forced and, if enabled, the error TBD is activated ' " '0x00 - unsupported, causes undefined behavior' '0x01 - 64us +0/-1us' '0x02 - 128us +0/-1us' '...' '0xFF - 16320us +0/-1us 16.3ms' " 'Upon the 64us hang pulse, the decremter ticks. if the decremter reaches x00, the heartbeat loss event is triggered.' "
8	RW	occ_heartbeat_enable 'OCC Heartbeat Timer Enable' " '0 = Disable the OCC Heartbeat function. Lack of accesses to the register defined by the dial occ_heartbeat_reg_addr_offset does not result in heartbeat loss events to be triggered (no FIRs set nor Safe mode entry).' " '1 = Enable the OCC Heartbeat function. '
9:16	RW	occ_heartbeat_reg_addr_offset This dial allows to configure the address offset within the PCBS power management entity of the register, that will regularly reset the heartbeat timer (which is called heartbeat trigger register). The address offset is 0x100 plus the value of this dial.
17:24	RW	Psafe 'Pstate Safe' " 'This field establishes the Pstate that the core chiplet will take on if: 'psafe <= PMSR[global_actual_pstate] 'AND any of the following conditions are true:' 'Loss of OCC Heartbeat if occ_heartbeat_en is set' 'PMGPO[force_safe_mode] is set' " 'If psafe > PMSR[global_actual_pstate], the global_actual_pstate is forced.' " 'The value of Psafe needs to be at or below the nominal Pstate to make sure safe operation of all chiplets. '

Register Name	PRCCR0 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG 0
Address	000000001D0F0165 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function.

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Bits	PCB	Field Mnemonic: Description
0	ROX	RESCLK_DIS: Resonant Clock Enable Master enable of all resonant clocking functions. This dial can be set by setting GP3(22) and can not be set in this PCBS_resonant_Clock_Control_Reg0. 1 = Resonant Clock function is disabled. Default values (0) for resclk_value, resclk_core_sync_value, csb_eco_sync_value 0 = Resonant Clock Control hardware is enabled (the mode is defined by dial resclk_control_mode)
1	RW	RESCLK_CONTROL_MODE: Resonant Clock Control Mode Defines the control means enabled when resclk_dis is not set. 0 = Pstate band hardware mechanism enabled 1 = Manual mode enabled (Firmware mode) If this bit is set to 0, the hardware control mechanism that manages the transition across the Resonant Bands is enabled. If this bit is set to 1, the automatic Pstate band hardware mechanism is disabled and the Firmware is in control of all values of the dial resclk_value, resclk_core_sync_value, csb_eco_sync_value. Firmware must ensure that frequency changes will not cross resonant bands or machine failures may result. resclk_value represents the values for clock sector buffer strength, inductor switch strength and high inductor enable. Firmware must ensure the correct stepping in/out the different bands and propagation of the values (resclk_value) to the core/eco (resclk_core_sync_value / csb_eco_sync_value).
2:4	RW	RESCLK_SYNC_PW: Resonant Clock Sync Pulse Width Number of nest/4 cycles to assert the clock sync signal. This value must be high enough to ensure capture and propagation across the asynchronous chiplet boundary.
5:11	RW	RES_SYNC_DELAY_CNT: Resonant Clock Sync Delay Number of nest/4 cycles wait after the launch of the resclk_value (csb and inductor) before launching the sync to allow these to be captured. This value must be high enough to ensure full propagation to the input of the clock sector buffers and inductor switches.
12:26	RW	RES_CSB_STR_INSTR_LO: Resonant Clock Sector Buffer Strength Instruction - Low Band Mask value that determines whether, during a fixed 15 step sequence, the res_csb_str(0:3) is to be decremented/incremented in entering/exiting the Low Band. During resonant clock Entry, res_csb_str(0:3) decremented by the value pattern from 0 down to 14. During resonant clock Exit, res_csb_str(0:3) incremented by the value pattern from 14 up to 0.
27:41	RW	RES_CSB_STR_INSTR_HI: Resonant Clock Sector Buffer Strength Instruction - High Band Mask value that determines whether, during a fixed 15 step sequence, the res_csb_str(0:3) is to be decremented/incremented in entering/exiting the High Band. During resonant clock Entry, res_csb_str(0:3) decremented by the value pattern from 0 down to 14. During resonant clock Exit, res_csb_str(0:3) incremented by the value pattern from 14 up to 0.

Register Name	<i>The PRCCR1</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG 1
Address	000000001D0F0166 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	FULL_CSB_PS: Full Clock Sector Buffer Pstate Pstate defining the maximum point where the clock sector buffer must be driven to full strength. This allow clocks to be distributed at low Vmin levels. FW needs to make sure that no overlaps occur with bands 2 or 3.
8:15	RW	RES_LOW_LOWER_PS: Low Frequency Resonant Lower (LFRLow) Pstate Pstate defining the lower frequency of the Low Resonant Frequency Band. FW needs to make sure that no overlap occurs with band 0.



Bits	PCB	Field Mnemonic: Description
16:23	RW	RES_LOW_UPPER_PS: Low Frequency Resonant Upper (LFRUpper) Pstate Pstate defining the upper frequency of the Low Resonant Frequency Band. Note that if an overlap occurs with band 3, the hardware behavior is undefined.
24:31	RW	RES_HIGH_LOWER_PS: High Frequency Resonant Lower (HFRLow) Pstate Pstate defining the lower frequency of the High Resonant Frequency Band. Note that if an overlap occurs with band 2, the hardware behavior is undefined.
32:39	RW	RES_HIGH_UPPER_PS: High Frequency Resonant Upper (LFRUpper) Pstate Pstate defining the upper frequency of the High Resonant Frequency Band. This value needs to be greater or equal to high_res_lower_ps.
40:43	RW	NONRES_CSB_VALUE_TI: Clock Sector Buffer Table Index for non-resonant state Table Index into Clock Sector Buffer Table for the nominal, non-resonant state.
44:47	RW	FULL_CSB_VALUE_TI: Clock Sector Buffer Table Index for full CSB value Table Index into Clock Sector Buffer Table for the full CSB strength value.
48:56	RWX	RESCLK_VALUE: Output register driving the 9 bit resclk_value In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current resclk_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. The value in this register represents the following concatenation: csb_str_value(0:3) sw_str(0:3) hi_induct_en.
57	RWX	RESCLK_CORE_SYNC_VALUE: Output register driving the resclk_core_sync signal In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current resclk_core_sync_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. This bit is supposed to be used in order to create a SCOM-controlled pulse to force an update of the resclk propagation registers. A 1 enables the synchronous update, a 0 disables it. Suggested use of this bit is to set it to 1 and then set it back to 0 to create a (long) update pulse.
58	RWX	CSB_ECO_SYNC_VALUE: Output register driving the csb_eco_sync signal In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current csb_eco_sync_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. This bit is supposed to be used in order enable the ECO domain to participate in clock sector buffer strength changes, when switching from nominal strength to full CSB strength. A 1 enables the ECO domain, a 0 disables it from seeing a CSB strength update.

Register Name	PRCCR1 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_STATUS_REG
Address	000000001D0F0167 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function.



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Bits	PCB	Field Mnemonic: Description
0	ROX	RESCLK_STATE: Resonant Clock State 0 = Resonant Clocking inactive 1 = Resonant Clocking active Valid if resclk_inprogress = 0. Hardware sets this bit to the right value at the completion of the transition into and out of resonance mode.

Bits	PCB	Field Mnemonic: Description
1	ROX	RES_HI_INDUCT_EN: Resonant High Inductor Enable Valid if resclk_inprogress = 0. This dial provides the current value being propagated. 0 = Resonant Clock mode not active 1 = Resonant Clock mode active
2	ROX	RESCLK_INPROGRESS: Resonant Clock Transition in Progress This bit is set by hardware while a transition is in progress and will be reset by hardware when the operation is complete.
3	ROX	RESCLK_FULL_CSB: Full CSB Clock State 0 = Full CSB Clocking inactive 1 = Full CSB Clocking active Valid if resclk_inprogress = 0. Hardware sets this bit to the right value at the completion of the transition into and out of full CSB mode respectively.

Register Name	<i>PLPFTCR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_CONTROL_REG
Address	000000001D0F0168 (PCB)
Attributes	
Description	Allows firmware to configure the modes that are used for the PCBS Local Pstate Frequency Target Status Register.

Bits	PCB	Field Mnemonic: Description
0:2	RW	DELAY_TIME: This field encodes the delay between the time a Local Actual Pstate change modifies the input to the DPLL and the time frequency acquisition begins to allow the hardware to ignore the frequency transition of the DPLL in order to get better frequency measurements. This field encodes a delay of ~1us to ~128us in power of 2 selects. The delay is defined by $2^{**}delay\_time$ in us. Note that the hardware uses multiples of the slow hang pulse that is running at 1us.
3	RW	RECORD_TRANSITIONS: This bit indicates whether the LPFTSR records events that correspond to Local Actual Pstate changes (and therefore may include DPLL slewing effects.) One usage model would set the periodic sample_time defined by the dial OHA_MODE_REG[tod_pulse_count_match_val] to a time less than the worst-case DPLL slew time but then ignore Pstate transitions because they might include DPLL slew effects.
4:18	RW	MULTIPLIER: This 15-bit unsigned constant is multiplied by the DPLL frequency code (9 bits) implied by the Local Actual Pstate to yield the 24-bit frequency target measured in PCBS-PM clock cycles (core clock / 2). Assuming times in seconds and frequencies in Hz, firmware should set this constant to: $(DPLL\_Frequency\_Code\_Step\_Hz * Sample\_Time\_Seconds) / 2$
19	RW	ENABLE_LPFT_FUNCTION: This is the enable bit to enable the local Pstate frequency target function. A '1' enables the function, a '0' disables it (the value can be changed at any time).

Register Name	<i>PLPFTSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_STATUS_REG
Address	000000001D0F0169 (PCB)
Attributes	
Description	Allows firmware to observe local actual Pstate realized frequencies.

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Bits	PCB	Field Mnemonic: Description
0	ROX_CLRPAR T	VALID: If this bit is set then all of the remaining fields of this register are valid. This bit is cleared whenever the register is read or after a local actual Pstate change occurs, and is will be set whenever the hardware completes a valid sample. If firmware reads this register and the valid bit is not set, then it indicates that the Local Pstate target frequency acquisition logic has not been able to complete a frequency acquisition for any Local Actual Pstate change since the last time the LPFTSR was read. This could be due to either of the following factors: 1. Firmware is sampling the LPFTSR faster than the time implied by the sample time defined in OHA by the dial OHA_MODE_REG[tod_pulse_count_match_val] field
1	ROX	CPM_DPLL: If the valid bit is set, then if cpm_dpll is set it indicates that the event recorded by this register was due to a Local Actual Pstate implemented by the DPLL running in CPM-DPLL mode, otherwise the value of this bit is undefined. If the valid bit is not set, this bit is undefined.
2	ROX	IVRM: If the valid bit is set, then if ivrm is set it indicates that the event recorded by this register was due to a Local Actual Pstate whose voltage was set locally by the iVRM operating entirely in regulation mode. If the valid bit is not set, this bit is undefined.
3	ROX	TRANSITION: If the valid bit is set, then if transition is set it indicates that during the observation period a Local Pstate Actual change has occurred, and any performance delta may be due to DPLL frequency slewing. If the valid bit is not set, this bit is undefined
4	ROX	STABLE: If stable is set it indicates that the DPLL input frequency has been stable since the last time the PLPFTSR was read. This bit is set whenever the PLPFTSR is read, and cleared whenever the Fmax input of the DPLL changes. This bit is always valid, regardless of the state of the valid bit. If the PLPFTSR is read on the same cycle a frequency changes then the stable bit is cleared. This bit helps firmware better understand how to interpret the information contained in the PLPFTSR. (Note that this bit should have an attribute ROX_SETPART, but this is not supported by regchk.)
5:28	ROX	DELTA: If the valid bit is set then this is the 24-bit signed difference Measured Cycles - Target Cycles for the event captured by this register. If the valid bit is not set, this dial is undefined.
29:52	ROX	CUMULATIVE: This field records the 24-bit cumulative (signed) delta for all valid samples taken since this field was cleared. Writing any value to this register clears this field. Note that it should have an attribute WOX_CLRPART, but this is not supported by regchk/figtree.
53:60	ROX	PSTATE: If the valid bit is set then this is the Local Actual Pstate of the frequency acquisition that had the minimum (signed) delta of any valid sample taken since the last time the LPFTSR was read. If the valid bit is not set, then this field is undefined.

Register Name	<i>PFSMM1/2 Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR1_REG
Address	000000001D0F0170 (PCB)
Attributes	
Description	Facilitates debug by providing insight into the internal FSM states of the PCB-slave power-management unit. For expert use only. Coding according to VHDL design.

Bits	PCB	Field Mnemonic: Description
0:6	ROX	BABYSTEP_MAIN_FSM: Main Babystep FSM (mfsm_lt)
7:11	ROX	BABYSTEP_SLAVE_FSM: Babystep Slave FSM (sfsm_lt)
12:16	ROX	CORE_RAILSTEPPER_MAIN_FSM: Main Core Railstepper FSM (mrsfsm_lt)
17:21	ROX	ECO_RAILSTEPPER_MAIN_FSM: Main ECO Railstepper FSM (mrsfsm_lt)



Bits	PCB	Field Mnemonic: Description
22:25	ROX	CORE_RAILSTEPPER_SUB_FSM: Core Railstepper Sub-FSM (srsfsm_lt)
26:29	ROX	ECO_RAILSTEPPER_SUB_FSM: ECO Railstepper Sub-FSM (srsfsm_lt)
30:34	ROX	CORE_RAILSTEPPER_BYP_FSM: Core Railstepper Bypass FSM (byp_fsm_lt)
35:39	ROX	ECO_RAILSTEPPER_BYP_FSM: ECO Railstepper Bypass FSM (byp_fsm_lt)
40:45	ROX	IVRM_CORE_VDD_SEQUENCER_FSM: Core iVRM Sequencer for Vdd (ivrm_fsm_lt)
46:51	ROX	IVRM_CORE_VCS_SEQUENCER_FSM: Core iVRM Sequencer for Vcs (ivrm_fsm_lt)
52:57	ROX	IVRM_ECO_VDD_SEQUENCER_FSM: ECO iVRM Sequencer for Vdd (ivrm_fsm_lt)
58:63	ROX	IVRM_ECO_VCS_SEQUENCER_FSM: ECO iVRM Sequencer for Vcs (ivrm_fsm_lt)

Register Name	<i>Refer To The Description Of PFSMM1</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR2_REG
Address	000000001D0F0171 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:6	ROX	RESCLK_BAND_FSM: Band Sequencer for resonant clocking (band_fsm_lt)
7:10	ROX	RESCLK_LOWRES_FSM: Low Resonant Clocking sequencer (lowres_fsm_lt)
11:14	ROX	RESCLK_HIGHRES_FSM: High Resonant Clocking sequencer (highres_fsm_lt)
15:18	ROX	RESCLK_FULLCSB_FSM: Full-CSB Resonant Clocking sequencer (fullcsb_fsm_lt)
19:22	ROX	RESCLK_UPDATE_FSM: Resonant Clocking Update sequencer (update_fsm_lt)
23:29	ROX	IDLE_TRANSITION_FSM: Idle State Sequence FSM (ifsm_lt)
30:37	ROX	Peco_step_target_uv Current ECO Step Target Pstate (different from Plocal_actual for undervolting)
38:45	ROX	Pcore_step_target_uv Current core Step Target Pstate (different from Plocal_actual for sleep and undervolting)

Register Name	<i>Protect Mode Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.PROTECT_MODE_REG
Address	000000001D0F03FE (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	READ_PROTECT_ENABLE: Enable read protection
1	RW	WRITE_PROTECT_ENABLE: Enable write protection

Register Name	<i>Atomic Lock Register</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX13.TP_PCB_SLAVE_INST.ATOMIC_LOCK_REG	
Address	000000001D0F03FF (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	RW	ATOMIC_LOCK_ENABLE: Enable atomic lock
1:4	ROX	ATOMIC_ID: Atomic ID

Register Name	<i>Contains The Slave's Primary Address</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.PRIMARY_ADDRESS_REG	
Address	000000001E0F0000 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RO	Reserved field (Access type is primary_address)

Register Name	<i>Multicast Group 1</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.MULTICAST_GROUP_1	
Address	000000001E0F0001 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST1_GROUP: multicast group1 setting

Register Name	<i>Multicast Group 2</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.MULTICAST_GROUP_2	
Address	000000001E0F0002 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST2_GROUP: multicast group2 setting



Register Name	<i>Multicast Group 3</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.MULTICAST_GROUP_3	
Address	000000001E0F0003 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST3_GROUP: multicast group3 setting

Register Name	<i>Multicast Group 4</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.MULTICAST_GROUP_4	
Address	000000001E0F0004 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:2	RO	constant=0b111
3:5	RW	MULTICAST4_GROUP: multicast group4 setting

Register Name	<i>Timeout Select Register</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.TIMEOUT_REG	
Address	000000001E0F0010 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:1	RW	Reserved field (Access type is int_timeout)

Register Name	<i>Assist Interrupt Register</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.ASSIST_INTERRUPT_REG	
Address	000000001E0F0011 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is attn)
1	ROX	Reserved field (Access type is recov)
2	ROX	Reserved field (Access type is xstop)

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Register Name	GP3 Register (NA In PERV CPLT)
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.GP3_REG
Address	000000001E0F0012 (PCB) 000000001E0F0013 (PCB1) 000000001E0F0014 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if chiplet is good
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset
2	RWX	RWX_WAND	RWX_WOR	GLSMUX_RESET: Glsmux reset for test purpose and stuck active mesh protection. Notice no clocks in the EX if this bit is set.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Put the DPLL in test mode.
4	RWX	RWX_WAND	RWX_WOR	PLL_RST: Put PLL in reset state.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYP: Enable PLL bypass.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pcb_access)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	PM_PI_DECODE: Test override for power management. EX chiplet only.
22	RWX	RWX_WAND	RWX_WOR	RESCLK_DIS: Resonant clocking disable.
23:25	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the Chiplet from the PCB Bus. If set, PCB Slave will report 'Chiplet Offline'.
27	RWX	RWX_WAND	RWX_WOR	TP_LVLTRANS_FENCE: Electrical winkel fence. Mainly used by power management.
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.
29:31	RWX	RWX_WAND	RWX_WOR	Reserved field (Access type is pm_access)



Register Name	<i>Skew Adjust Data</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.CLK_ADJ_REG	
Address	000000001E0F0015 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:15	ROX	

Register Name	<i>Clk Ajust Config</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.CLK_ADJ_SET	
Address	000000001E0F0016 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:31	RW	CLK_ADJ_SET_REG: Clk adj config

Register Name	<i>Vital Scan Out</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.VITAL_SCAN_OUT	
Address	000000001E0F0017 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	

Register Name	<i>Chiplet Heartbeat Register</i>	
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.HEARTBEAT_REG	
Address	000000001E0F0018 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	ROX	HEARTBEAT_DEAD: Chiplet heartbeat not detected

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Register Name	<i>Lock Indications From PLLs</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.PLL_LOCK_REG
Address	000000001E0F0019 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	ROX	Reserved field (Access type is lock)

Register Name	<i>Attn Interrupt</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.ATTN_INTERRUPT_REG
Address	000000001E0F001A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is attn)

Register Name	<i>Recov Interrupt</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.RECOV_INTERRUPT_REG
Address	000000001E0F001B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is recov)

Register Name	<i>Xstop Interrupt</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.XSTOP_INTERRUPT_REG
Address	000000001E0F001C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	Reserved field (Access type is xstop)

Register Name	<i>Slave Config Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.SLAVE_CONFIG_REG
Address	000000001E0F001E (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	CFG_DISABLE_PERV_THOLD_CHECK: Disable pervasive thold check
1	RW	CFG_DISABLE_MALF_PULSE_GEN: Disable pulse generation for malf alert. Switch back to level
2	RW	CFG_STOP_HANG_CNT_SYS_XSTP: Disable hang counter stop for system xstop
3	RW	CFG_DISABLE_CL_ATOMIC_LOCK: Disable atomic lock for chiplet accesses
4	RW	CFG_DISABLE_HEARTBEAT: Disable check for voltage and gridclock in the chiplet
5	RW	CFG_ZERO_DATA: Sent zero data on any error
6:7	RW	
8:12	RW	ERROR_MASK: mask bits for slave error reporting
13:15	RW	

Register Name	<i>Error Capture Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.ERROR_REG
Address	000000001E0F001F (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX_WCLEAR	CE_ERROR: Correctable error on pcb bus
1:3	RWX_WCLEAR	CHIPLET_ERRORS: Errors reported by chiplet 000 = no error 001 = XSCOM command blocked due pending errors 010 chiplet offline 011 partial good 100 invalid address / address error / bad access type 101 clock error 110 parity error / received unexpected packet / wrong packet number 111 timeout This register is for debug purposes only. It only holds meaningful data if it is cleared after each error.
4	RWX_WCLEAR	PARITY_ERROR: Parity error on PCB Interface
5	RWX_WCLEAR	DATA_BUFFER_ERROR: Parity error in data buffer
6	RWX_WCLEAR	ADDR_BUFFER_ERROR: Parity error in address buffer
7	RWX_WCLEAR	PCB_FSM_ERROR: Invalid state error in PCB FSM
8	RWX_WCLEAR	CL_FSM_ERROR: Invalid state error in Chiplet FSM
9	RWX_WCLEAR	INT_RX_FSM_ERROR: Invalid state error in interrupt RX FSM
10	RWX_WCLEAR	INT_TX_FSM_ERROR: Invalid state error in interrupt TX FSM

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Bits	PCB	Field Mnemonic: Description
11	RWX_WCLEAR	INT_TYPE_ERROR: Invalid interrupt type
12	RWX_WCLEAR	CL_DATA_ERROR: Parity error on Chiplet Interface
13	RWX_WCLEAR	INFO_ERROR: Parity error on Chiplet info lines
14	RWX_WCLEAR	UNUSED_0:
15	RWX_WCLEAR	CHIPLET_ATOMIC_LOCK_ERROR: Chiplet atomic lock error
16	RWX_WCLEAR	PCB_INTERFACE_ERROR: Error of pcb interface component for the internal endpoint
17	RWX_WCLEAR	CHIPLET_OFFLINE: Heartbeat check indicated that chiplet is offline
18	RWX_WCLEAR	CHIPLET_GRID_SKITTER: Heartbeat check indicated skitter on the chiplet grid
19	RWX_WCLEAR	GP3_REG_PARITY_ERROR: gp3 register parity bad
20	RWX_WCLEAR	ADDRESS_REG_PARITY_ERROR: address register parity bad
21	RWX_WCLEAR	TIMEOUT_REG_PARITY_ERROR: timeout select register parity bad
22	RWX_WCLEAR	CONFIG_REG_PARITY_ERROR: slave config register parity bad
23	RWX_WCLEAR	CLK_ADJ_REG_PARITY_ERROR: clk adj register parity bad
24	RWX_WCLEAR	DIV_REG_PARITY_ERROR: div register parity bad
25:28	RWX_WCLEAR	PLL_UNLOCK_ERROR: unlock from chiplet pll

Register Name		Hang Pulse Generation Register 0.
Mnemonic		EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.HANG_PULSE_0_REG
Address		000000001E0F0020 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_0: Value of hang pulse 0. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_0: If set to '1', hang pulses are suppressed in case of a xstop



Register Name	Hang Pulse Generation Register 1	
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.HANG_PULSE_1_REG	
Address	000000001E0F0021 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_1: Value of hang pulse 1. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_1: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	Hang Pulse Generation Register 2	
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.HANG_PULSE_2_REG	
Address	000000001E0F0022 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_2: Value of hang pulse 2. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_2: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	Hang Pulse Generation Register 3	
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.HANG_PULSE_3_REG	
Address	000000001E0F0023 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_3: Value of hang pulse 3. Time period = $2^{\text{value}} * (\text{precounter\_reg}+1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_3: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	Hang Pulse Generation Register 4	
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.HANG_PULSE_4_REG	
Address	000000001E0F0024 (PCB)	
Attributes		
Description		

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Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_4: Value of hang pulse 4. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_4: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 5</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.HANG_PULSE_5_REG
Address	000000001E0F0025 (PCB)
Attributes	
Description	This hang counter is used exclusively to generate the malfunction alert pulse.

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_5: Value of hang pulse 5. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_5: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Hang Pulse Generation Register 6</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.HANG_PULSE_6_REG
Address	000000001E0F0026 (PCB)
Attributes	
Description	This hang counter is exclusively used for heartbeat generation.

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_6: Value of hang pulse 6. Time period = $2^{\text{value}} * (\text{precounter\_reg} + 1) / \text{pcb\_freq}$, $34 \geq \text{value} > 0$
6	RW	SUPPRESS_HANG_6: If set to '1', hang pulses are suppressed in case of a xstop

Register Name	<i>Divider For Hang Counter Clock</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.PRE_COUNTER_REG
Address	000000001E0F0028 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PRE_COUNTER: Divider for hang counter clock. Divides clock by n+1 (default: n=0)



Register Name		<i>PowerManagement GP0</i>		
Mnemonic		EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PMGPO_REG		
Address		000000001E0F0100 (PCB) 000000001E0F0101 (PCB1) 000000001E0F0102 (PCB2)		
Attributes				
Description				
Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	PM_DISABLE: Master Switch for the PowerManagement Macro
1	RWX	WOX_AND	WOX_OR	PMGP0_SPARE_BIT1: spare bit
2	RWX	WOX_AND	WOX_OR	TP_TC_RESTART_CORE_DOMAIN: Kicks off small sequencer in OHA to get chiplet clocks back running for fast sleep without involving PORE. From GP-reg and overridden by PowMan State Machine.
3	RWX	WOX_AND	WOX_OR	DPLL_THOLD: Thold for the DPLL clock domain in the chiplet
4	RWX	WOX_AND	WOX_OR	PERV_THOLD: Thold for the Pervasive clock domain in the chiplet
5	RO	RO	RO	Reserved.
6	RO	RO	RO	Reserved.
7	RWX	WOX_AND	WOX_OR	PM_DPLL_TIMER_ENA: Select a timer instead of the DPLL lock bit for criteria to switch to DPLL. The time is defined by thold_timer_sel.
8	RWX	WOX_AND	WOX_OR	DPLL_LOCK_SENSE: DPLL lock sensitivity control (0=faster lock time, 1=slower lock time)
9	RWX	WOX_AND	WOX_OR	PMGP0_SPARE2: spare bit
10	RWX	WOX_AND	WOX_OR	DPLL_RESET: Reset to DPLL
11	RWX	WOX_AND	WOX_OR	PMGP0_SPARE_BIT11: Spare bit
12:19	RWX	WOX_AND	WOX_OR	DPLL_TESTOUT_CTL: DPLL testout control
20	RWX	WOX_AND	WOX_OR	TP_TC_CACHE2CORE_FENCE: Fence from cache to core domain in EX chiplet
21	RWX	WOX_AND	WOX_OR	TP_TC_CORE2CACHE_FENCE: Fence from core to cache domain in EX chiplet
22	RWX	WOX_AND	WOX_OR	TP_TC_PERVASIVE_ECO_FENCE: Pervasive ECO fence
23	RWX	WOX_AND	WOX_OR	CHKSW_HW257424_DISABLE: Chicken switch for interrupt retry exhausted bug (0=fix enabled, 1=fix disabled)
24:26	RWX	WOX_AND	WOX_OR	TP_CLK_ASYNC_RESET_DC: Clk async reset for three glitchless muxes, and the two clock dividers (bit 0 = master GLM, bit 1 = ECO Div2 and ECO GLM, bit 2= core Div1 and core GLM)
27:29	RWX	WOX_AND	WOX_OR	TP_CLKGLM_SEL_DC: Glitchless Mux Select for primary chiplet clock source (feeding both core and eco clock muxes) 000 = refclk, 001 = DPLL. 100 = Use constant selected by bit 34, else refclk
30	RWX	WOX_AND	WOX_OR	TP_CLKGLM_ECO_SEL_DC: Glitchless Mux Select for eco domain (cache_nclk) grid. 0= follow primary source chosen by previous field: 1 = Use constant selected by bit 34
31	ROX	NC	NC	SPECIAL_WKUP_DONE: Indicates that special wakeup is done, if asserted
32:33	RWX	WOX_AND	WOX_OR	TP_CLKGLM_CORE_SEL_DC: Glitchless Mux Select for core domain (nclk grid) mux. 0b00=primary GLS mux output, 0b10=constant input, 0b01=refclk. Valid transitions are 0b01 <-> 0b00 <-> 0b10, 0b11 is illegal

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
34	RWX	WOX_AND	WOX_OR	TP_CLKGLM_CONST_DC: Constant input available to all three ClkGlm
35:36	RWX	WOX_AND	WOX_OR	THOLD_TIMER_SEL: Selection for the thold transition timer in the IDLE state machine. 0b00=1024 cycles delay, 0b01=512 cycles delay, 0b10=256 cycles delay, 0b11= 128 cycles delay
37	RWX	WOX_AND	WOX_OR	BLOCK_ALL_WAKEUP_SOURCES: Setting this bit will make the PM Slave ignore any Wakeup events (ext. interrupt, malfunction alert, any special wakeup bit). This bit is intended to enable firmware concurrent patch capability. Note: This does NOT block the interrupt from being presented to the processor core. The following procedure is required on changes: 1. Firmware may only set this bit after first setting special wakeup and polling for special wakeup complete (OHA and PCB-slave both in running state with AISS and PM FSMs idle). 2. Firmware may only clear this bit if all special wakeup bits are first cleared.
38	RWX	WOX_AND	WOX_OR	TP_TC_DPLL_TESTMODE_DC: ADPLL test mode
39	RWX	WOX_AND	WOX_OR	PM_SLV_WINKLE_FENCE: Fence off the powered off chiplet in winkle. - Logical fence/hold for pcb_slave and pcb_slave_pm. For electrical fence see bit 23.
40	RWX	WOX_AND	WOX_OR	L3_ENABLE_SWITCH: Setting this bit activates l3_edram_enable if allowed by system configuration GP3(28). Resetting this bit deactivates l3_edram_enable.
41	RWX	WOX_AND	WOX_OR	TP_CPLT_IVRM_REFBYPASS_DC: Signal to iVRM (used to be controlled by scan-only block inside EX, but needs to be driven by VIO domain)
42	RWX	WOX_AND	WOX_OR	CHKSW_HW241939_DISABLE: if this bit is set to 1, the fix for HW241939 (pfet enable SCOM-ability) is disabled
43	RWX	WOX_AND	WOX_OR	CHKSW_HW273115_DISABLE: if this bit is set to 1, the fix for HW273115 (Pga ACK noack issue when the babystepper is in the winkle state) is disabled
44	RWX	WOX_AND	WOX_OR	CHKSW_HW245103_DISABLE: if this bit is set to 1, the fix for HW245103 resonant clocking CSB and SW -bit ordering change is disabled
45	RWX	WOX_AND	WOX_OR	CHKSW_HW257534_DISABLE: if this bit is set to 1, the fix for HW257534 (fencing of errors) is disabled
46	RWX	WOX_AND	WOX_OR	CHKSW_HW259509_ENABLE: if this bit is set to 0, the fix for HW259509 (Pstate change hanging, because of DPLL flock timer in a hung state) is disabled
47	RWX	WOX_AND	WOX_OR	CHKSW_HW260345_DISABLE: if set to 1, this bit disables the HW260345 fix (fix was to make sure that we enter bypass mode for iVRM safe mode without a glitch that could cause Vcs in regulation and Vdd in bypass)
48:49	ROX	NC	NC	WAKEUP_INT_TYPE: (Known to be unreliable and not supported, informational usage only) Type of the last wakeup event that caused an exit from sleep or winkle (excluding nap!), regardless of present state. 0b01: External interrupt. 0b10: Malfunction Alert. 0b11: Special Wakeup. 0b00: chiplet has never fully entered and exited a chiplet-level idle state since IPL of the system. (Note this does not necessarily get updated when the processor core enters an idle state, only if the PCB-Slave enters and then exits the idle state for this chiplet).
50	ROX	NC	NC	DPLL_LOCK: DPLL lock indicator
51	ROX	NC	NC	SPECIAL_WKUP_ALL_SOURCES_ORED: logical OR of all special wakeup sources
52	ROX	NC	NC	REGULAR_WKUP_AVAILABLE: logical OR of external interrupt and malfunction alert



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
53	RWX	WOX_AND	WOX_OR	BLOCK_REG_WKUP_SOURCES: blocks ext. int. and malf. Alert from waking up PCBS (no block possible for PC!)

Register Name	PowerManagement GP1
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PMGP1_REG
Address	000000001E0F0103 (PCB) 000000001E0F0104 (PCB1) 000000001E0F0105 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	SLEEP_POWER_DOWN_EN: Sleep Power Down Enable: When set to 1, causes hardware to automatically reduce voltage to the Core domain when entering Sleep mode. The voltage value for power down is chosen by sleep_power_off_sel (bit 2). When set to 0, a request is sent to the PORE engine for assistance entering Sleep.
1	RWX	WOX_AND	WOX_OR	SLEEP_POWER_UP_EN: Sleep Power Up Enable: When set to 1, enables automated hardware restoration of voltage via PFETs and, if enabled, iVRMs when exiting Sleep mode. If this bit is set to 0 the hardware rely on external means (PORE or equivalent) to restore voltage.
2	RWX	WOX_AND	WOX_OR	SLEEP_POWER_OFF_SEL: Sleep Power Off Select: Selects which voltage level to place the Core domain PFETs upon Sleep entry. 0 = Vret (Fast Sleep Mode), 1 = Voff (Deep Sleep Mode). Depending on the setting of pmicr_latency_en, this bit is controlled with a PCB-write (0) or by the PMICR in the core (1).
3	RWX	WOX_AND	WOX_OR	WINKLE_POWER_DOWN_EN: Winkle Power Down Enable: When set to 1, causes hardware to automatically reduce voltage to the entire Chiplet (both Core and ECO Domains) when entering Winkle mode. The voltage value for power down is chosen by winkle_power_off_sel (bit 5). When set to 0, a request is sent to the PORE engine for assistance entering Winkle.
4	RWX	WOX_AND	WOX_OR	WINKLE_POWER_UP_EN: Winkle Power Up Enable: When set to 1, enables automated hardware PFET enablement when exiting Winkle mode. If this bit is set to 0 the hardware rely on external means (PORE or equivalent) to cause the PFETs to be re-enabled.
5	RWX	WOX_AND	WOX_OR	WINKLE_POWER_OFF_SEL: Winkle Power Off Select: Selects which voltage level to place the Core and ECO domain PFETs upon Winkle entry. 0 = Vret (Fast Winkle Mode), 1 = Voff (Deep Winkle Mode). Depending on the setting of pmicr_latency_en, this bit is controlled with a PCB-write (0) or by the PMICR in the core (1).
6	RWX	WOX_AND	WOX_OR	OHA_WKUP_OVERRIDE_EN: Needs to be 0 for normal operation. If set to 1, the two following dials are used to override the regular and special wakeup signal from PCBS to OHA
7	RWX	WOX_AND	WOX_OR	OHA_PM_WKUP_OVERRIDE: Enablement by 'oha_wkup_override_en' forces the regular wakeup signal to OHA to the value of this bit regardless of presence of an interrupt source.
8	RWX	WOX_AND	WOX_OR	OHA_SPC_WKUP_OVERRIDE: Enablement by 'oha_wkup_override_en' forces the special wakeup signal to OHA to the value of this bit, regardless of the firmware settings.

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Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
9	RWX	WOX_AND	WOX_OR	ENDP_RESET_PM_ONLY: If asserted, an endpoint reset of all power management-related functions (not the regular PCB slave) is performed. Intended usage is for recovery.
10	RWX	WOX_AND	WOX_OR	DPLL_FREQ_OVERRIDE_ENABLE: override Fmax/Fmin only, if '1', using register FREQ_CTRL_REG
11	RWX	WOX_AND	WOX_OR	PM_SPR_OVERRIDE_EN: PM SPR Override Enable The PPMCR (0xNNNN) and PPMICR (0XXXXX) accesses the register resources that make up the PMCR SPR used by hypervisor to management Pstates. Thus, PCB updates to it are disabled in hardware to prevent collisions. This bit allows ownership of the PMCR to be switched from hypervisor to OCC. This switch is immediate in hardware, thus, firmware must ensure the ownership switch is otherwise communicated. 0 = Disables the writing of the PPMCR (0xNNNN) from the PCB and allows SPR 884 writes (mtspr) to update the register resource. 1 = Enables the writing of the PPMCR (0xNNNN) from the PCB.
12	RWX	WOX_AND	WOX_OR	FORCE_SAFE_MODE: Force Safe Mode 0 = Allow other enabled features to determine the operational Pstate. 1 = Forces the minimum of POHBR[psafe] and PPMSR[global_pstate_actual] Pstate for the core chiplet as the operational frequency.
13	RWX	WOX_AND	WOX_OR	IVRM_SAFE_MODE_EN: Internal VRM Safe Mode Enable 0 = Disable the iVRM safe mode, thus, no automatic actions occur, if an iVRM error happens. 1 = if the iVRMs are enabled (PIVRMCSR[ivrm_en] is set) and Pstates are enabled and if the error defined by dial pcbs_ivrm_gross_or_fine_err occurs, then the railstepper is forced into bypass mode to prevent a voltage-frequency hazard
14	RWX	WOX_AND	WOX_OR	IVRM_SAFE_MODE_FORCE_ACTIVE: Internal VRM Safe Mode Force Dial 0 = the hardware decides whether to activate the iVRM safe mode or not 1 = the iVRM safe mode is forced regardless (this makes only sense if ivrm_fsm_enable=1 and Pstates are enabled)
15	RWX	WOX_AND	WOX_OR	PMICR_LATENCY_EN: Selects how the sleep/winkle latency (which is deep/fast) is controlled. If asserted the PMICR controls the winkle/sleep_power_off_sel in PMGP1, otherwise those bits are controlled via SCOM by OCC.
16	RWX	WOX_AND	WOX_OR	ENABLE_OCC_CTRL_FOR_LOCAL_PSTATE_EFF_REQ: controls, if the HW (for value 0) or OCC (value 1) is in control of the Local Pstate Effective register in PPSTR
17	RWX	WOX_AND	WOX_OR	SERIALIZE_PFET_POWERDOWN: if asserted, the pFET sequencer will sequence the core and the ECO domain one after the other when powering down
18	RWX	WOX_AND	WOX_OR	SERIALIZE_PFET_POWERUP: if asserted, the pFET sequencer will sequence the ECO and the core domain one after the other when powering up
19	RWX	WOX_AND	WOX_OR	DISABLE_FORCE_DEEP_TO_FAST_SLEEP: 0: (normal operation) - If PCB Slave reports a recoverable error or a checkstop, a DEEP sleep operation is forced to FAST. The entries in sleep/winkle_power_off_sel remain unchanged. 1: force to FAST is disabled.



Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
20	RWX	WOX_AND	WOX_OR	DISABLE_FORCE_DEEP_TO_FAST_WINKLE: 0: (normal operation) - If PCB Slave reports a recoverable error or a checkstop, a DEEP winkle operation is forced to FAST. The entries in sleep/winkle_power_off_sel remain unchanged. 1: force to FAST is disabled.

Register Name	<i>PFET Control/Status Register For Core And ECO Vdd</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PFVDDCNTLSTAT_REG
Address	000000001E0F0106 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	CORE_VDD_PFET_FORCE_STATE: Core Domain PFET Force State Provides a means for firmware to force the core domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 4:5 = 00 (both core_vdd_pfet_val_override AND core_vdd_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
2:3	RW	ECO_VDD_PFET_FORCE_STATE: ECO Domain PFET Force State Provides a means for firmware to force the ECO domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 6:7 = 00 (both eco_vdd_pfet_val_override AND eco_vdd_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
4	RW	CORE_VDD_PFET_VAL_OVERRIDE: Core Domain PFET Value Override 0 = Override is disabled
5	RW	CORE_VDD_PFET_SEL_OVERRIDE: Core Domain PFET Stage Select Override 0 = Override is disabled
6	RW	ECO_VDD_PFET_VAL_OVERRIDE: ECO Domain PFET Value Override 0 = Override is disabled
7	RW	ECO_VDD_PFET_SEL_OVERRIDE: ECO Domain PFET Stage Select Override 0 = Override is disabled
8	RW	CORE_VDD_PFET_ENABLE_REGULATION_FINGER: Core Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the core_vdd_pfet_enable_value.
9	RW	ECO_VDD_PFET_ENABLE_REGULATION_FINGER: ECO Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the eco_vdd_pfet_enable_value.

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Bits	PCB	Field Mnemonic: Description
10:21	RW	CORE_VDD_PFET_ENABLE_VALUE: Core PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the Core Domain PFET Enables directly. If core_vdd_pfet_val_override = 1, a write to this field sets the state of the core PFET Enables until core_vdd_pfet_val_override is cleared. If core_vdd_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the core_vdd_pfet_valN_slac registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
22:25	RW	CORE_VDD_PFET_SEL_VALUE: Core PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure core_vdd_pfet_valN_slac(0:11) where N is 0 to 11 if core_vdd_pfet_sel_override = 1. If core_vdd_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
26:37	RW	ECO_VDD_PFET_ENABLE_VALUE: ECO PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the ECO PFET Enables directly. If ECO_vdd_pfet_val_override = 1, a write to this field sets the state of the ECO PFET Enables until ECO_vdd_pfet_val_override is cleared. If eco_vdd_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the eco_vdd_pfet_valN_slac registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
38:41	RW	ECO_VDD_PFET_SEL_VALUE: ECO PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure eco_vdd_pfet_valN_slac(0:11) where N is 0 to 11 if eco_vdd_pfet_sel_override = 1. If eco_vdd_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
42:45	ROX	CORE_VDD_PG_STATE: Core power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
46:49	ROX	CORE_VDD_PG_SEL: For debug, contains the actual index n into Core Domain PFET Value [n] SLAT Register set that contains the Core PFET Enable Value currently enabled.
50:53	ROX	ECO_VDD_PG_STATE: ECO Domain power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
54:57	ROX	ECO_VDD_PG_SEL: For debug, contains the actual index n into ECO Domain PFET Value [n] SLAT Register set that contains the ECO PFET Enable Value currently enabled.

Register Name	PFET Sense Register	
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PFSENSE_REG	
Address	000000001E0F0107 (PCB)	
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:11	ROX	TP_CORE_VDD_PFET_ENABLE_SENSE: Not used any more.
12:23	ROX	TP_ECO_VDD_PFET_ENABLE_SENSE: Not used any more.



Bits	PCB	Field Mnemonic: Description
24:35	ROX	TP_CORE_VCS_PFET_ENABLE_SENSE: Not used any more.
36:47	ROX	TP_ECO_VCS_PFET_ENABLE_SENSE: Not used any more.

Register Name	<i>PM Error Summary Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PMERRSUM_REG
Address	000000001E0F0108 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	PM_ERROR: PM Error is present. Intended for use by special PCB multicast to see error state of all chiplets with a single read (via 510F0108 to read all chiplets)

Register Name	<i>PM Error Register:</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PMERR_REG
Address	000000001E0F0109 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_HANG_ERR: Hang during Unassisted Sleep Entry: SLEEP_ENTRY_NOTIFY_PMC state
1	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ASSIST_HANG_ERR: Hang during Assisted Sleep Entry: SLEEP_ENTRY_NOTIFY_PMC_ASSIST state
2	ROX	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ERR: Hang during Unassisted Sleep Exit: SLEEP_EXIT_NOTIFY_PMC state
3	ROX	PCBS_SLEEP_EXIT_INVOKE_PORE_ERR: Hang during Assisted Deep Sleep Exit: SLEEP_EXIT_INVOKE_PORE state
4	ROX	PCBS_WINKLE_ENTRY_NOTIFY_PMC_ERR: Hang during Unassisted Winkle Entry: WINKLE_ENTRY_NOTIFY_PMC state
5	ROX	PCBS_WINKLE_ENTRY_SEND_INT_ASSIST_ERR: Hang during Assisted Winkle Entry: WINKLE_ENTRY_SEND_INT_ASSIST state
6	ROX	PCBS_WINKLE_EXIT_NOTIFY_PMC_ERR: Hang during Unassisted Winkle Exit: WINKLE_EXIT_NOTIFY_PMC state
7	ROX	PCBS_WAIT_DPLL_LOCK_ERR: Hang during Unassisted Exit waiting on DPLL: WAIT_DPLL_LOCK state
8	ROX	PCBS_SPARE8_ERR: spare bit, always 0
9	ROX	PCBS_WINKLE_EXIT_SEND_INT_ASSIST_ERR: Hang during Assisted Winkle Exit: WINKLE_EXIT_SEND_INT_ASSIST state
10	ROX	PCBS_WINKLE_EXIT_SEND_INT_POWUP_ASSIST_ERR: Hang during Assisted Winkle Exit: WINKLE_EXIT_SEND_INT_POWUP_ASSIST state
11	ROX	PCBS_WRITE_FSM_GOTO_REG_IN_INVALID_STATE_ERR: write to FSM goto register in invalid state
12	ROX	PCBS_WRITE_PMGP0_IN_INVALID_STATE_ERR: write to PMGP0 in invalid state

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Bits	PCB	Field Mnemonic: Description
13	ROX	PCBS_FREQ_OVERFLOW_IN_PSTATE_MODE_ERR: frequency of DPLL in Pstate mode overflows (Fnom + desired Pstate > 511)
14	ROX	PCBS_ECO_RS_BYPASS_CONFUSION_ERR: ECO railstepper tried to exit Vcs bypass and enter Vdd bypass in one Pstate step (it is not clear, in which order this strange operation should be performed - most likely it should never happen to avoid that Vcs is greater than Vdd)
15	ROX	PCBS_CORE_RS_BYPASS_CONFUSION_ERR: same as previous error, but for core railstepper (it is not clear, in which order this strange operation should be performed - most likely it should never happen to avoid that Vcs is greater than Vdd)
16	ROX	PCBS_READ_LPST_IN_PSTATE_MODE_ERR: read LPST-array while iVRM FSMs are enabled (dial ivrm_fsm_enable asserted)
17	ROX	PCBS_LPST_READ_CORR_ERR: correctable error occurred when reading the LPST
18	ROX	PCBS_LPST_READ_UNCORR_ERR: uncorrectable error occurred when reading the LPST
19	ROX	PCBS_PFET_STRENGTH_OVERFLOW_ERR: overflow occurred when calculating the pFET strength (in final rounding step!)
20	ROX	PCBS_VDS_LOOKUP_ERR: Vds entry not found in lookup table (when performing the linear search!)
21	ROX	PCBS_IDLE_INTERRUPT_TIMEOUT_ERR: idle interrupt timeout in PCB interrupt controller
22	ROX	PCBS_PSTATE_INTERRUPT_TIMEOUT_ERR: PState interrupt timeout in PCB interrupt controller
23	ROX	PCBS_GLOBAL_ACTUAL_SYNC_INTERRUPT_TIMEOUT_ERR: GlobalActualSync Interrupt timeout in PCB interrupt controller
24	ROX	PCBS_PMAX_SYNC_INTERRUPT_TIMEOUT_ERR: PmaxSync Interrupt timeout in PCB interrupt controller
25	ROX	PCBS_GLOBAL_ACTUAL_PSTATE_PROTOCOL_ERR: a write to global actual Pstate register has occurred before the global actual Pstate interrupt has left PCBS
26	ROX	PCBS_PMAX_PROTOCOL_ERR: a write to the Pmax/Pmin register has occurred before the Pmax sync interrupt has left PCB
27	ROX	PCBS_IVRM_GROSS_OR_FINE_ERR: iVRM gross or fine error (details to be found in PCBS_ivrm_Control_Status_Reg)
28	ROX	PCBS_IVRM_RANGE_ERR: iVRM range error (summary bit, details to be found in PCBS_ivrm_Control_Status_Reg)
29	ROX	PCBS_DPLL_CPM_FMIN_ERR: DPLL CPM Fmin error
30	ROX	PCBS_DPLL_DCO_FULL_ERR: DPLL DCO full
31	ROX	PCBS_DPLL_DCO_EMPTY_ERR: DPLL DCO empty
32	ROX	PCBS_DPLL_INT_ERR: DPLL internal error
33	ROX	PCBS_FMIN_AND_NOT_CPMBIT_ERR: dpll_fmin_and_not_cpmbit (ref. to dial cpm_fmin_clip_error_sel on how to configure this)
34	ROX	PCBS_DPLL_FASTER_THAN_FMAX_PLUS_DELTA1_ERR: dpll_faster_than_fmax_plus_delta1 (for characterization, delta1 is configurable with pll_char_delta1)
35	ROX	PCBS_DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2_ERR: dpll_slower_than_fmin_minus_delta2 (for characterization, delta2 is configurable with pll_char_delta2)
36	ROX	PCBS_RESCLK_CSB_INSTR_VECTOR_CHG_IN_INVALID_STATE_ERR: RESCLK CSB instruction vector change while FSMs none idle
37	ROX	PCBS_RESCLK_BAND_BOUNDARY_CHG_IN_INVALID_STATE_ERR: RESCLK Band boundaries change while FSMs none idle
38	ROX	PCBS_OCC_HEARTBEAT_LOSS_ERR: OCC heartbeat loss
39	ROX	PCBS_SPARE39_ERR: spare bit, always 0
40	ROX	PCBS_SPARE40_ERR: spare bit, always 0



Bits	PCB	Field Mnemonic: Description
41	ROX	PCBS_SPARE41_ERR: spare bit, always 0
42	ROX	PCBS_SPARE42_ERR: spare bit, always 0

Register Name	<i>PM Error Mask Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PMERRMASK_REG
Address	000000001E0F010A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_HANG_ERR_MASK: Mask for this error: 1=masked, 0=not masked
1	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ASSIST_HANG_ERR_MASK: Mask for this error: 1=masked, 0=not masked
2	RW	PCBS_SLEEP_ENTRY_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
3	RW	PCBS_SLEEP_EXIT_INVOKE_PORE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
4	RW	PCBS_WINKLE_ENTRY_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
5	RW	PCBS_WINKLE_ENTRY_SEND_INT_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
6	RW	PCBS_WINKLE_EXIT_NOTIFY_PMC_ERR_MASK: Mask for this error: 1=masked, 0=not masked
7	RW	PCBS_WAIT_DPLL_LOCK_ERR_MASK: Mask for this error: 1=masked, 0=not masked
8	RW	PCBS_SPARE8_ERR_MASK: Mask for this error: 1=masked, 0=not masked
9	RW	PCBS_WINKLE_EXIT_SEND_INT_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
10	RW	PCBS_WINKLE_EXIT_SEND_INT_POWUP_ASSIST_ERR_MASK: Mask for this error: 1=masked, 0=not masked
11	RW	PCBS_WRITE_FSM_GOTO_REG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
12	RW	PCBS_WRITE_PMGPO_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
13	RW	PCBS_FREQ_OVERFLOW_IN_PSTATE_MODE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
14	RW	PCBS_ECO_RS_BYPASS_CONFUSION_ERR_MASK: Mask for this error: 1=masked, 0=not masked
15	RW	PCBS_CORE_RS_BYPASS_CONFUSION_ERR_MASK: Mask for this error: 1=masked, 0=not masked
16	RW	PCBS_READ_LPST_IN_PSTATE_MODE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
17	RW	PCBS_LPST_READ_CORR_ERR_MASK: Mask for this error: 1=masked, 0=not masked
18	RW	PCBS_LPST_READ_UNCORR_ERR_MASK: Mask for this error: 1=masked, 0=not masked
19	RW	PCBS_PFET_STRENGTH_OVERFLOW_ERR_MASK: Mask for this error: 1=masked, 0=not masked
20	RW	PCBS_VDS_LOOKUP_ERR_MASK: Mask for this error: 1=masked, 0=not masked
21	RW	PCBS_IDLE_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
22	RW	PCBS_PSTATE_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
23	RW	PCBS_GLOBAL_ACTUAL_SYNC_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
24	RW	PCBS_PMAX_SYNC_INTERRUPT_TIMEOUT_ERR_MASK: Mask for this error: 1=masked, 0=not masked

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Bits	PCB	Field Mnemonic: Description
25	RW	PCBS_GLOBAL_ACTUAL_PSTATE_PROTOCOL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
26	RW	PCBS_PMAX_PROTOCOL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
27	RW	PCBS_IVRM_GROSS_OR_FINE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
28	RW	PCBS_IVRM_RANGE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
29	RW	PCBS_DPLL_CPM_FMIN_ERR_MASK: Mask for this error: 1=masked, 0=not masked
30	RW	PCBS_DPLL_DCO_FULL_ERR_MASK: Mask for this error: 1=masked, 0=not masked
31	RW	PCBS_DPLL_DCO_EMPTY_ERR_MASK: Mask for this error: 1=masked, 0=not masked
32	RW	PCBS_DPLL_INT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
33	RW	PCBS_FMIN_AND_NOT_CPMBIT_ERR_MASK: Mask for this error: 1=masked, 0=not masked
34	RW	PCBS_DPLL_FASTER_THAN_FMAX_PLUS_DELTA1_ERR_MASK: Mask for this error: 1=masked, 0=not masked
35	RW	PCBS_DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2_ERR_MASK: Mask for this error: 1=masked, 0=not masked
36	RW	PCBS_RESCLK_CSB_INSTR_VECTOR_CHG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
37	RW	PCBS_RESCLK_BAND_BOUNDARY_CHG_IN_INVALID_STATE_ERR_MASK: Mask for this error: 1=masked, 0=not masked
38	RW	PCBS_OCC_HEARTBEAT_LOSS_ERR_MASK: Mask for this error: 1=masked, 0=not masked
39	RW	PCBS_SPARE39_ERR_MASK: Mask for this error: 1=masked, 0=not masked
40	RW	PCBS_SPARE40_ERR_MASK: Mask for this error: 1=masked, 0=not masked
41	RW	PCBS_SPARE41_ERR_MASK: Mask for this error: 1=masked, 0=not masked
42	RW	PCBS_SPARE42_ERR_MASK: Mask for this error: 1=masked, 0=not masked

Register Name		<i>PM Special Wakeup FSP</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PMSPCWKUPFSP_REG
Address		000000001E0F010B (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RW	FSP_SPECIAL_WAKEUP: Chiplet Special Wakeup for FSP Firmware use. NOTE: protocol is required when setting this bit

Register Name		<i>PM Special Wakeup OCC</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PMSPCWKUPOCC_REG
Address		000000001E0F010C (PCB)
Attributes		
Description		



Bits	PCB	Field Mnemonic: Description
0	RW	OCC_SPECIAL_WAKEUP: Chiplet Special Wakeup for OCC Firmware use. NOTE: protocol is required when setting this bit

Register Name	<i>PM Special Wakeup Hypervisor</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PMSPCWKUPPHYP_REG
Address	000000001E0F010D (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	PHYP_SPECIAL_WAKEUP: Chiplet Special Wakeup for hypervisor Firmware use. NOTE: protocol is required when setting this bit

Register Name	<i>PFET Control/Status Register For Core And ECO Vcs</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PFVCS_CNTLSTAT_REG
Address	000000001E0F010E (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RW	CORE_VCS_PFET_FORCE_STATE: Core Domain PFET Force State Provides a means for firmware to force the core domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 4:5 = 00 (both core_vcs_pfet_val_override AND core_vcs_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
2:3	RW	ECO_VCS_PFET_FORCE_STATE: ECO Domain PFET Force State Provides a means for firmware to force the ECO domain PFETs to well known end states using the hardware sequencing mechanisms b00 = No operation b01 = Force Voff b10 = Force Vret b11 = Force Von This field is only valid if bits 6:7 = 00 (both eco_vcs_pfet_val_override AND eco_vcs_pfet_sel_override are disabled). Set these bits to 00, if master_p7plus_mode_enable is on.
4	RW	CORE_VCS_PFET_VAL_OVERRIDE: Core Domain PFET Value Override 0 = Override is disabled
5	RW	CORE_VCS_PFET_SEL_OVERRIDE: Core Domain PFET Stage Select Override 0 = Override is disabled
6	RW	ECO_VCS_PFET_VAL_OVERRIDE: ECO Domain PFET Value Override 0 = Override is disabled
7	RW	ECO_VCS_PFET_SEL_OVERRIDE: ECO Domain PFET Stage Select Override 0 = Override is disabled

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Bits	PCB	Field Mnemonic: Description
8	RW	CORE_VCS_PFET_ENABLE_REGULATION_FINGER: Core Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the core_vcs_pfet_enable_value.
9	RW	ECO_VCS_PFET_ENABLE_REGULATION_FINGER: ECO Domain PFET Regulation Finger Enable Bit 0 = Regulation Finger controlled by pFET enable FSM 1 = Regulation Finger is powered on If this bit is asserted, the pFET finger that is used for the iVRM is forced to be enabled regardless of the setting of the regular pfet_enable FSM. If it is deasserted, the pFET sequencer controls this finger with the eco_vcs_pfet_enable_value.
10:21	RW	CORE_VCS_PFET_ENABLE_VALUE: Core PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the Core Domain PFET Enables directly. If core_vcs_pfet_val_override = 1, a write to this field sets the state of the core PFET Enables until core_vcs_pfet_val_override is cleared. If core_vcs_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the core_vcs_pfet_valN_slav registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
22:25	RW	CORE_VCS_PFET_SEL_VALUE: Core PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure core_vcs_pfet_valN_slav(0:11) where N is 0 to 11 if core_vcs_pfet_sel_override = 1. If core_vcs_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
26:37	RW	ECO_VCS_PFET_ENABLE_VALUE: ECO PFET Enable Value Intended for manual control override usage, a write to this field sets the state of the ECO PFET Enables directly. If ECO_vcs_pfet_val_override = 1, a write to this field sets the state of the ECO PFET Enables until ECO_vcs_pfet_val_override is cleared. If eco_vcs_pfet_val_override = 0, a write to this field takes on the value for 1 cycle and then returns to the value produced by the eco_vcs_pfet_valN_slav registers. A write of this type is not recommended and may produce undefined results. Reads will return the present state.
38:41	RW	ECO_VCS_PFET_SEL_VALUE: ECO PFET Select Value Intended for manual control override usage, a write to this field will index value N into the registers structure eco_vcs_pfet_valN_slav(0:11) where N is 0 to 11 if eco_vcs_pfet_sel_override = 1. If eco_vcs_pfet_sel_override = 0, the field is written but no further action is taken. x0: xB - Index xC:xF - Reserved Reads will return the present state of the field.
42:45	ROX	CORE_VCS_PG_STATE: Core power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
46:49	ROX	CORE_VCS_PG_SEL: For debug, contains the actual index n into Core Domain PFET Value [n] SLAT Register set that contains the Core PFET Enable Value currently enabled.
50:53	ROX	ECO_VCS_PG_STATE: ECO Domain power gate sequencer FSM (1 hot) bit 0 = Idle, bit 1 = Increment, bit 2 = Decrement, bit 3 = Wait
54:57	ROX	ECO_VCS_PG_SEL: For debug, contains the actual index n into ECO Domain PFET Value [n] SLAT Register set that contains the ECO PFET Enable Value currently enabled.



Register Name	<i>PM State History Register For Hypervisor</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPHYP_REG
Address	000000001E0F0110 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	PHYP_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPART	PHYP_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPART	PHYP_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPART	PHYP_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPART	PHYP_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPART	PHYP_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For FSP</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PMSTATEHISTFSP_REG
Address	000000001E0F0111 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	FSP_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPART	FSP_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPART	FSP_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPART	FSP_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.

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Bits	PCB	Field Mnemonic: Description
6	ROX_CLRPAR T	FSP_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	FSP_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For OCC</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PMSTATEHISTOCC_REG
Address	000000001E0F0112 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	OCC_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	OCC_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	OCC_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	OCC_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	OCC_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	OCC_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM State History Register For PerfMon</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PMSTATEHISTPERF_REG
Address	000000001E0F0113 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	ROX	PERF_PM_STATE: Current IDLE state of the chiplet. 0b000: Run 0b001: Special Wakeup 0b010: Nap 0b011: Legacy Sleep 0b100: Fast Sleep 0b101: Deep Sleep 0b110: Fast Winkle 0b111: Deep Winkle
3	ROX_CLRPAR T	PERF_PAST_CORE_INSTRUCT_STOP: Sticky bit for having seen an Idle state with core instructions stopped (pm_state gt 0b001). This bit clears on register read.
4	ROX_CLRPAR T	PERF_PAST_CORE_CLK_STOP: Sticky bit for having seen an Idle state with core clocks stopped (pm_state gt 0b010). This bit clears on register read.
5	ROX_CLRPAR T	PERF_PAST_CORE_PWR_OFF: Sticky bit for having seen an Idle state with core powered off (pm_state = 0b101 0b111). This bit clears on register read.
6	ROX_CLRPAR T	PERF_PAST_ECO_CLK_STOP: Sticky bit for having seen an Idle state with eco clocks stopped (pm_state = 0b011 0b110 0b111). This bit clears on register read.
7	ROX_CLRPAR T	PERF_PAST_ECO_PWR_OFF: Sticky bit for having seen an Idle state with eco powered off (pm_state = 0b111). This bit clears on register read.

Register Name	<i>PM FSM Reset And Babystepper Idle Injects</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.IDLEFSMGOTOCMD_REG
Address	000000001E0F0114 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	WO_1P	idle_fsm_goto_cmd ' A write to this reg will proceed the IDLE FSM from WAIT_FOR_PORE_DONE, SLEEP_EXIT_WAIT_FOR_PORE_FAST_EXIT_DONE, or WINKLE_EXIT_WAIT_FOR_PORE_FAST_EXIT_DONE to the following states: ' 0b01: goto IDLE state ' 0b10: goto SLEEP_EXIT_CORE_MESHLET_ON state ' 0b11: goto WINKLE_EXIT_NOTIFY_PMC state ' "
2	RWX	babystp_trigger_sleep_entry ' A write to this reg with a 1 in this field will cause the babystepper to run the sleep entry sequence. This step is needed for an assisted entry into sleep, before the power is actually turned off since the babystepper needs to know about the sleep state. For an unassisted entry, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished entering its sleep mode. ' "
3	RWX	babystp_trigger_winkle_entry ' A write to this reg with a 1 in this field will cause the babystepper to run the winkle entry sequence. This step is needed for an assisted entry into winkle before the power is actually turned off since the babystepper needs to know about the winkle state. For an unassisted entry, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished entering its winkle mode. ' "
4	RWX	babystp_trigger_wakeup ' A write to this reg with a 1 in this field will cause the babystepper to run the wakeup sequence from sleep/winkle depending on the babystepper state of sleep or winkle. This step is needed for an assisted exit from winkle before the power is actually turned off since the babystepper needs to know about the wakeup state. For an unassisted exit, writing this register must not be performed. ' " 'Firmware needs to poll this bit until it is cleared to make sure that the babystepper has finished waking up from sleep or winkle. ' "

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Register Name	Core PFET Power Up Delay
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.COREPFPUDLY_REG
Address	000000001E0F012C (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_POWUP_DLY0: Delay used after transitioning to Core Domain power up sequence stage0. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	CORE_POWUP_DLY1: Delay used after transitioning to Core domain power up sequence stage1.
8:19	RW	CORE_POWER_UP_DELAY_SEL: Vector select for which delay to use for the respective power-up stage. Bit mapping: 8 -> core_*_pfet_enable(0) 9 -> core_*_pfet_enable(1) ... 19 -> core_*_pfet_enable(11) Bit meaning: 0 = Use core_powup_dly0 1 = Use core_powup_dly1

Register Name	Core PFET Power Down Delay
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.COREPFPDDLY_REG
Address	000000001E0F012D (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_POWDN_DLY0: Delay used after transitioning to Core domain power dn sequence stage1. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	CORE_POWDN_DLY1: Delay used after transitioning to Core domain power dn sequence stage1. The delays in this register are in terms of PCBS clock period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
8:19	RW	CORE_POWER_DN_DELAY_SEL: Vector select for which delay to use for the respective power-dn stage. Bit mapping: 8 -> core_*_pfet_enable(0) 9 -> core_*_pfet_enable(1) ... 19 -> core_*_pfet_enable(11) Bit meaning: 0 = Use core_powdn_dly0 1 = Use core_powdn_dly1



Register Name	Core PFET Vretention	
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.COREPFVRET_REG	
Address	000000001E0F0130 (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:3	RW	CORE_VRET_SEL: Pointer to the stage representing the Vretention value for the core PFETs. Power down sequences will stop after enabling this stage.
4:7	RW	CORE_VOFF_SEL: Pointer to the stage representing the Voff value for the core PFETs. Power down sequences will stop after enabling this stage.

Register Name	ECO PFET Power Up Delay	
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.ECOPFPUDLY_REG	
Address	000000001E0F014C (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_POWUP_DLY0: Delay used after transitioning to ECO domain power up sequence stage0 in terms of refclk period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.
4:7	RW	ECO_POWUP_DLY1: Delay used after transitioning to ECO domain power up sequence stage1.
8:19	RW	ECO_POWER_UP_DELAY_SEL: Vector select for which delay to use for the respective power-up stage. Bit mapping: 8 -> eco_*_pfet_enable(0) 9 -> eco_*_pfet_enable(1) ... 19 -> eco_*_pfet_enable(11) Bit meaning: 0 = Use eco_powup_dly0 1 = Use eco_powup_dly1

Register Name	ECO PFET Power Down Delay	
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.ECOPFPDDLY_REG	
Address	000000001E0F014D (PCB)	
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_POWDN_DLY0: UNUSED/SPARE
4:7	RW	ECO_POWDN_DLY1: Delay used after transitioning to ECO Domain power dn sequence stage1. The delays in this register are in terms of refclk period (4.46ns) times 2 ^(15 minus this value) . Note: chooses the Power of 2 bit position of core_pg_timer(0:15) which is running off pcb_nclk.

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Bits	PCB	Field Mnemonic: Description
8:19	RW	ECO_POWER_DN_DELAY_SEL: Vector select for which delay to use for the respective power-down stage. Bit mapping: 8 -> eco_*_pfet_enable(0) 9 -> eco_*_pfet_enable(1) ... 19 -> eco_*_pfet_enable(11) Bit meaning: 0 = Use eco_powdn_dly0 1 = Use eco_powdn_dly1

Register Name		<i>ECO PFET Vretention</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.ECOPFVRET_REG
Address		000000001E0F0150 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0:3	RW	ECO_VRET_SEL: Pointer to the stage representing the Vretention value for the ECO PFETs. Power down sequences will stop after enabling this stage.
4:7	RW	ECO_VOFF_SEL: Pointer to the stage representing the Voff value for the ECO PFETs. Power down sequences will stop after enabling this stage.

Register Name		<i>Frequency Control Register With Overrides For DPLL</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.FREQ_CTRL_REG
Address		000000001E0F0151 (PCB)
Attributes		
Description		Note that overrides to Dpll_fmax are only applied if Dpll_freq_override_enable = 1. A read of all these dials always returns the currently established DPLL frequencies (regardless of any other mode settings).
Bits	PCB	Field Mnemonic: Description
0:8	RO	Reserved.
9:17	RWX	DPLL_FMAX: DPLL maximum frequency and frequin (these two values are the same in POWER8 processor) without applying bias values: A read always returns the currently established value A write is conditioned on the setting of dpll_freq_override_enable. If dpll_freq_override_enable is asserted, a write causes this field to update. Otherwise the hardware (that is, PStates) are controlling the update of this value.
18:21	RO	Reserved.
22:30	RW	FREQU_AT_PSTATE0: DPLL frequency for Pstate 0



Register Name	<i>DPLL Mode Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.DPLL_CPM_PARM_REG
Address	000000001E0F0152 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	LF_SLEWRATEXPI: out of lock slew rate for DPLL
8	RW	LF_USE_CPMXPI: use CPM instead of PFD as loop filter input, if '1' (instead of using both)
9	RW	FF_USE_CPMXPI: use the CPM inputs for the frequency filter, if '1'
10	RW	CPM_FILTER_ENABLE: enables the CPM filter
11	RW	FF_BYPASSXPI: enables frequency filter bypass
12	RW	DCO_OVERRIDE: enables overrides for DCO testing/characterization
13	RW	DCO_INCR: enables increment for DCO testing/characterization, increments only on a rising edge
14	RW	DCO_DECR: enables decrement for DCO testing/characterization, decrements only on a rising edge
15:23	RW	DPLL_LOCK_TIMER_REPLACEMENT_VALUE: if dpll_lock_replacement_timer_mode_en is set, this dial specifies the delay in us, after which it is assumed, that the DPLL has reached a frequency lock condition. Note that values less than 3 will cause in undefined HW behavior (0 will cause HANGs!). if dpll_lock_replacement_timer_mode_en is zero, this dial specifies the delay in pcb_nclk cycles after which the hardware monitors the DPLL frequout output (if dpll_freqout_mode_en is set) or the DPLL flock output (if dpll_flock_mode_en is set). Note that in this case, the value of this dial needs to be greater or equal to 150 (decimal).
24:31	RW	PRE_VRET_PSTATE: Pstate that is stepped to before switching to Vretention defined in PCBS_iVRM_Control_Status_Reg
32	RW	OVERRIDE_PCBS_DPLL_SYNCHRONIZER: Bypasses the 'ping-pong' synchronization logic between the DPLL and the PCBS-PM. NEVER SET TO 1 UNLESS YOU KNOW WHAT YOU ARE DOING!
33:36	RW	DPLL_CHAR_DELTA1: Delta in DPLL ticks for characterization (cf. dial dpll_faster_than_fmax_plus_delta1)
37:40	RW	DPLL_CHAR_DELTA2: Delta in DPLL ticks for characterization (cf. dial dpll_faster_than_fmin_minus_delta2)

Register Name	<i>PPMSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_STATUS_REG
Address	000000001E0F0153 (PCB)
Attributes	
Description	Provides read access to the power management status that is also shadowed to the PC and visible to the hypervisor in the PMSR (with some delay due to the shadowing process).

Bits	PCB	Field Mnemonic: Description
0:7	ROX	global_pstate_actual ' Actual Global Pstate Pstate or Pglobal_actual' " Reads from this field return the presently established global PState value." " Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent '

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Bits	PCB	Field Mnemonic: Description
8:15	ROX	LOCAL_PSTATE_ACTUAL: ' Actual Local PState or Plocal_actual' " 'Reads from this field return the presently established local PState value. This value will always be less than or equal to global_pstate_actual.' " 'Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent' "
16:23	ROX	pv_min Minimum Pstate set by the platform.
24:31	ROX	pvf_max Maximum Pstate set by the platform.
32	ROX	spr_em_disabled ' SPR Energy Management Disabled' 'Read from this field indicate whether the platform has disabled the ' 'PMCR and PMICR SPRs to control the chiplet PState. '
33	ROX	Psafe_mode_active Read from this field indicate whether the chiplet has been put into a safe mode with Psafe enabled to a OCC heartbeat loss or other externally forced reasons (0=regular mode, 1=safe mode is active)
34	ROX	iVRM_safe_mode_active Read from this field indicate whether the chiplet has been put the iVRM safe mode (forcing the bypass mode for all iVRMs)
35	ROX	ivrm_enable Read from this field indicate whether the chiplet internal voltage regulation macro is enabled for localized voltage control (0=disabled, 1=enabled) based on ANDing the poweron signals to the iVRMs
36	ROX	all_fsms_in_safe_state For recovery: if this bit is asserted, all Pstate and iVRM control FSMs are in a stable, safe state that allows the recovery routine to proceed with resetting the PCBS PM without the risk of interrupt a critical action
37:40	ROX	pmsr_spares spare bits

Register Name	<i>PIVRMCSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_CONTROL_STATUS_REG
Address	000000001E0F0154 (PCB)
Attributes	
Description	Provides access to chiplet-level controls of the internal VRM rail set (VDD and VCS) across both the core and ECO domains. The following is valid only for bits 4 to 7. When in automatic iVRM mode (ivrm_fsm_enable = 1), these bits provide access to the values established by the automatic hardware mechanism. When In iVRM override mode (ivrm_fsm_enable = 0), these bits allow firmware direct control of the values driving the internal VRMs.

Bits	PCB	Field Mnemonic: Description
0	RW	IVRM_FSM_ENABLE: Internal master VRM FSM Enable 0 = Disable Internal VRM FSMs and enable to control the iVRMs with the available override registers (SCOMable) as a backup mode or for setup (override mode) 1 = Enable Internal VRM FSM sequencers (requires that Pstates are enabled with enable_Pstate_mode=1 as well) (automatic mode)
1	RW	USE_IVRM_FOR_VRET: Internal VRM Enabled for Vretention 0 = Disable Internal VRM for Vretention 1 = Enable Internal VRM for Vretention
2	RW	BINSEARCH_CAL_ENA: trigger binary search (level signal)

Bits	PCB	Field Mnemonic: Description
3	RW	PVREF_EN: Internal VRM Power Voltage Reference Forced Enable 0 = Allow hardware to enable/disable pvref circuit 1 = Force enablement of the pvref circuit
4	RWX	IVRM_CORE_VDD_BYPASS_B: Internal VRM Core VDD Bypass (negative active) 0 = VDD Internal Core VRMs in bypass 1 = VDD internal Core VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
5	RWX	IVRM_CORE_VDD_POWERON: Internal VRM Core VDD Poweron 0 = Core VDD Internal VRMs powered off 1 = Core VDD internal VRMs powered on if this bit is not set (=0), the Core VDD internal VRM powered off internally. If this bit is set (=1), the Core VDD internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
6	RWX	IVRM_CORE_VCS_BYPASS_B: Internal VRM Core VCS Bypass (negative active) 0 = VCS Internal Core VRMs in bypass 1 = VCS internal Core VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VCS internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VCS internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
7	RWX	IVRM_CORE_VCS_POWERON: Internal VRM Core VCS Poweron 0 = Core VCS Internal VRMs powered off 1 = Core VCS internal VRMs powered on if this bit is not set (=0), the Core VCS internal VRM powered off internally. If this bit is set (=1), the Core VCS internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
8	RWX	IVRM_ECO_VDD_BYPASS_B: Internal VRM ECO VDD Bypass (negative active) 0 = VDD Internal ECO VRMs in bypass 1 = VDD internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
9	RWX	IVRM_ECO_VDD_POWERON: Internal VRM ECO VDD Bypass (negative active) 0 = VDD Internal ECO VRMs in bypass 1 = VDD internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VDD internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VDD internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.

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Bits	PCB	Field Mnemonic: Description
10	RWX	IVRM_ECO_VCS_BYPASS_B: Internal VRM ECO VCS Bypass (negative active) 0 = VCS Internal ECO VRMs in bypass 1 = VCS internal ECO VRMs not in bypass Reading returns the current state with the following meaning: if this bit is not set (=0), the VCS internal VRMs are held in bypass. If this bit is set (=1) and ivrm_fsm_enable is set (=1), the VCS internal VRMs are enabled to regulate based on the ivrm_vdd_vid(0:7) voltage ID. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
11	RWX	IVRM_ECO_VCS_POWERON: Internal VRM ECO VCS Poweron 0 = ECO VCS Internal VRMs powered off 1 = ECO VCS internal VRMs powered on if this bit is not set (=0), the ECO VCS internal VRM powered off internally. If this bit is set (=1), the ECO VCS internal VRM is powered on and must be so in order to regulate. Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
12:18	RWX	IVRM_VRET_VDD: if use_ivrm_for_Vret is asserted, this dial is used to control the Vdd retention voltage. Note: this field will establish the Core VDD rail for Sleep and both the Core and ECO rail for Winkle. - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
19:25	RWX	IVRM_VRET_VCS: if use_ivrm_for_Vret is asserted, this dial is used to control the Vcs retention voltage. Note: this field will establish the Core VDD rail for Sleep and both the Core and ECO rail for Winkle. - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
26:30	RWX	IVRM_VRET_CORE_VDD_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the Core Vdd iVRM PFET strength for the retention voltage
31:35	RWX	IVRM_VRET_CORE_VCS_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the Core Vcs iVRM PFET strength for the retention voltage
36:40	RWX	IVRM_VRET_ECO_VDD_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the ECO Vdd iVRM PFET strength for the retention voltage
41:45	RWX	IVRM_VRET_ECO_VCS_PFET_STRENGTH: if use_ivrm_for_Vret is asserted, this dial is used to control the ECO Vcs iVRM PFET strength for the retention voltage
46	RW	PVREF_FAIL: voltage reference fail input to iVRMs
47	ROX	IVRM_PREF_ERROR_GROSS: Voltage Reference Gross Error 0 = Gross Error not detected 1 = Gross Error detected
48	ROX	IVRM_PREF_ERROR_FINE: Voltage Reference Fine Error 0 = Fine Error not detected 1 = Fine Error detected
49	ROX	IVRM_CORE_VDD_RANGE_HI: Core VDD Internal VRM Range Hi Indicator 0 = Core VDD Internal VRM Hi indicator signal not asserted 1 = Core VDD internal VRMs Hi indicator signal asserted
50	ROX	IVRM_CORE_VDD_RANGE_LO: Core VDD Internal VRM Range Low Indicator 0 = Core VDD Internal VRM Low indicator signal not asserted 1 = Core VDD internal VRMs Low indicator signal asserted

Bits	PCB	Field Mnemonic: Description
51	ROX	IVRM_ECO_VDD_RANGE_HI: ECO VDD Internal VRM Range Hi Indicator 0 = ECO VDD Internal VRM Hi indicator signal not asserted 1 = ECO VDD internal VRMs Hi indicator signal asserted
52	ROX	IVRM_ECO_VDD_RANGE_LO: ECO VDD Internal VRM Range Low Indicator 0 = ECO VDD Internal VRM Low indicator signal not asserted 1 = ECO VDD internal VRMs Low indicator signal asserted
53	ROX	IVRM_CORE_VCS_RANGE_HI: Core VCS Internal VRM Range Hi Indicator 0 = Core VCS Internal VRM Hi indicator signal not asserted 1 = Core VCS internal VRMs Hi indicator signal asserted
54	ROX	IVRM_CORE_VCS_RANGE_LO: Core VCS Internal VRM Range Low Indicator 0 = Core VCS Internal VRM Low indicator signal not asserted 1 = Core VCS internal VRMs Low indicator signal asserted
55	ROX	IVRM_ECO_VCS_RANGE_HI: ECO VCS Internal VRM Range Hi Indicator 0 = ECO VCS Internal VRM Hi indicator signal not asserted 1 = ECO VCS internal VRMs Hi indicator signal asserted
56	ROX	IVRM_ECO_VCS_RANGE_LO: ECO VCS Internal VRM Range Low Indicator 0 = ECO VCS Internal VRM Low indicator signal not asserted 1 = ECO VCS internal VRMs Low indicator signal asserted
57	ROX	BINSEARCH_CAL_DONE: binary search done signal
58	RWX	IVRM_CORE_VDD_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
59	RWX	IVRM_CORE_VCS_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
60	RWX	IVRM_ECO_VDD_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
61	RWX	IVRM_ECO_VCS_PFET_LOW_VOUT: Indicator that the output voltage (Vout) is targeting a value below a threshold 0 = VID to IVRM > VID threshold (ivrm_vid_vout_threshold) 1 = VID to IVRM <= VID threshold (ivrm_vid_vout_threshold) Writes are only enabled if ivrm_fsm_enable is set to zero (override mode). Otherwise, writes to this field are discarded.
62	RW	IVRM_POWER_DOWN_DISABLE: If this bit is 1, the iVRM poweron signal is left asserted. Power off of the iVRMs is then blocked

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Register Name	<i>PIVRMVSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VALUE_SETTING_REG
Address	000000001E0F0155 (PCB)
Attributes	
Description	Allows access to VID values and PFET strength valid signal settings presented to the internal VRM rail set (VDD and VCS) across both the core and ECO domains. When in <code>ivrm_fsm_enable = "auto"</code> mode, this register provides access to the values established by the automatic hardware mechanism. When <code>ivrm_fsm_enable = "override"</code> mode, this register allows firmware direct control of the values driving the internal VRMs which, if the VRMs are not in bypass, will move the voltage settings.

Bits	PCB	Field Mnemonic: Description
0:7	RWX	IVRM_CORE_VDD_IVID: When read, returns the value presently being driving to the Core VDD iVRM. If <code>ivrm_fsm_enable = 0</code> (override_mode), then writes to this field will drive a new VID value to the Core VDD iVRM. If <code>ivrm_fsm_enable = 1</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
8:15	RWX	IVRM_CORE_VCS_IVID: When read, returns the value presently being driving to the Core VCS iVRM. If <code>ivrm_fsm_enable = 0</code> (override_mode), then writes to this field will drive a new VID value to the Core VCS iVRM. If <code>ivrm_fsm_enable = 1</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
16:23	RWX	IVRM_ECO_VDD_IVID: When read, returns the value presently being driving to the Core VDD iVRM. If <code>ivrm_fsm_enable = 0</code> (override_mode), then writes to this field will drive a new VID value to the ECO VDD iVRM. If <code>ivrm_fsm_enable = 1</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
24:31	RWX	IVRM_ECO_VCS_IVID: When read, returns the value presently being driving to the ECO VCS iVRM. If <code>ivrm_fsm_enable = 0</code> (override_mode), then writes to this field will drive a new VID value to the ECO VCS iVRM, If <code>ivrm_fsm_enable = 0</code> , writes to this field are not performed. 0 = Reserved 1:7 = <code>ivid_vdd</code> - Encoded based on zero origin at 600mV with 6.25mV granularity - 0x00: 600mV - 0x01: 606.25mV - - 0x7F: 1.39375mV
32:36	RWX	IVRM_CORE_VDD_PFET_STRENGTH: When read, returns the value presently being driving to the core VCS iVRM. If <code>ivrm_fsm_enable = 0</code> (override_mode), then writes to this field will drive a new strength value to the core VCS iVRM, If <code>ivrm_fsm_enable = 0</code> , writes to this field are not performed.

Bits	PCB	Field Mnemonic: Description
37:41	RWX	IVRM_CORE_VCS_PFET_STRENGTH: This register is assigned to the signals tcex##_tp_ivrm_core_vcs_sense & tcex##_tp_ivrm_core_vdd_sense & tcex##_tp_ivrm_eco_vcs_sense & tcex##_tp_ivrm_eco_vdd_sense & 0b0 Note that all other sense signals are spares now and tied to 0. OUTDATED TEXT: When read, returns the value presently being driving to the core VDD iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the core VDD iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
42:46	RWX	IVRM_ECO_VDD_PFET_STRENGTH: When read, returns the value presently being driving to the ECO VCS iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the ECO VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
47:51	RWX	IVRM_ECO_VCS_PFET_STRENGTH: When read, returns the value presently being driving to the ECO VDD iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new strength value to the ECO VDD iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
52	RWX	IVRM_VDD_CORE_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the Core VDD iVRM. If ivrm_fsm_enable = 1 AND ivrm_control_mode = 1 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the Core VDD iVRM, If ivrm_fsm_enable = 0 OR ivrm_control_mode = 0, writes to this field are not performed.
53	RWX	IVRM_VCS_CORE_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the Core VCS iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the Core VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
54	RWX	IVRM_VDD_ECO_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the ECO VDD iVRM. If ivrm_fsm_enable = 1 AND ivrm_control_mode = 1 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the ECO VDD iVRM, If ivrm_fsm_enable = 0 OR ivrm_control_mode = 0, writes to this field are not performed.
55	RWX	IVRM_VCS_ECO_PFETSTR_VALID: When read, returns the PFET Strength Valid signal presently being driven to the ECO VCS iVRM. If ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive a new PFET Strength Valid value to the ECO VCS iVRM, If ivrm_fsm_enable = 1, writes to this field are not performed.
56	RWX	CORE_VDD_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
57	RWX	CORE_VCS_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
58	RWX	ECO_VDD_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.
59	RWX	ECO_VCS_VPUMP_EN: voltage pump enable: when read returns the current value, when written and if ivrm_fsm_enable = 0 (override_mode), then writes to this field will drive the value to the voltage pump, otherwise writes are discarded.

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Register Name		General PCBS Modes And Chicken Switches
Mnemonic		EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBSPM_MODE_REG
Address		000000001E0F0156 (PCB)
Attributes		
Description		
Bits	PCB	Field Mnemonic: Description
0	RW	ENABLE_PSTATE_MODE: if asserted, Pstate requests (from overrides or PMCR) will be honored, otherwise, the hardware does not do anything. Note to firmware: this is the master switch for Pstates and should be asserted after all sub-modes (that is, lvrn_fsm_en) are setup to avoid enabling unintentional modes during the mode setup.
1	RW	GLOBAL_PSTATE_CHANGE_FOR_IDLE_STATE_ENABLED: if asserted, a global Pstate change to the Nap/Sleep/Winkle-Pstate is requested, when the Nap/Sleep/Winkle state is entered and the individual enable bits in the PIMCR are asserted
2	RW	ENABLE_GLOBAL_PSTATE_REQ: if '1' then enable PMC interrupt with global Pstate change request, otherwise, disable global requests
3	RW	ENABLE_WINKLE_WITH_CPM_MODE: if '1', PCBS automatically changes the DPLL mode to mode 1, when entering winkle, but changes the mode back to CPM mode when exiting. Needed for CPM-DPLL control loop enablement.
4	RW	ENABLE_CLIPPING_OF_GLOBAL_PSTATE_REQ: if '1', PCBS automatically clips global Pstate requests with Pvf_max in PPMBR and sets the 'donate' bit in the interrupt accordingly
5	RW	CHKSW_HW214553: if deasserted, HW214553 (frequin issue in resclk mode) is fixed, if asserted, the fix is not active
6	RW	ENABLE_PMC_PMAX_SYNC_NOTIFICATION: if asserted, the PCBS-PM will send a 'Pmax_sync' interrupt, once the synchronization criterion is met
7	RW	DPLL_LOCK_REPLACEMENT_TIMER_MODE_EN: Select a timer instead of the DPLL lock bit as target frequency reached criterion. This timer has to be setup by the dial dpll_lock_timer_replacement_value. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
8	RW	DPLL_FREQOUT_MODE_EN: Looks at the DPLL frequout to find out, if the target frequency has been reached. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
9	RW	DPLL_FLOCK_MODE_EN: Looks at the real DPLL flock output to find out, if the target frequency has been reached. Note that exactly one of the 3 mode bits dpll_lock_replacement_timer_mode_en or dpll_freqout_mode_en or dpll_flock_mode_en needs to be asserted.
10	RW	ENABLE_SENSE_DELAY_CHARACTERIZATION: If this switch is 0, the sense latches are updated every cycle. If this switch is 1, the sense delay measurement mode is enabled, that starts a sense delay timer, whenever one of the registers that drive the inputs of the iVRMs/pFETs is written via PCB and that triggers a sense register freeze operation, when the sense delay timer reaches the value sense_delay_timer_val. With this mode, the sense delays can be measured in multiples of the PCB-slave clock speed.
11:17	RW	SENSE_DELAY_TIMER_VAL: See the description of enable_sense_delay_characterization for details.
18:19	RW	CPM_FMIN_CLIP_ERROR_SEL: This dial selects, which of the following conditions will cause the FIR bit dpll_fmin_and_not_cpmbit to be set to detect, that the DPLL runs at Fmin, but is still clipped by the CPMs. 0b00 = function is disabled 0b01 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit2 = 0 0b10 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit1 = 0 0b11 = Bit where DPLL indicates it is clipped AND dpll_cpm_data bit0 = 0
20:23	RW	DBG_TRACE_SEL: This dial selects the group of signals to be traced for debug in the lab. Details to be found in the Section 'Trace Bus'

Bits	PCB	Field Mnemonic: Description
24:25	RW	TRACE_DATA_SEL: This dial selects the group of signals to be traced for debug in the lab. Details to be found in the Section 'Trace Bus'
26:29	RW	TP_CPLT_IVRM_VPP_TUNE: Tune bits to be set going to the iVRMs

Register Name	<i>PIVRMPS Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_PFETSTR_SENSE_REG
Address	000000001E0F0157 (PCB)
Attributes	
Description	Used to check that the pFET sense outputs correspond to the driven values (mainly for test).

Bits	PCB	Field Mnemonic: Description
0:4	ROX	IVRM_CORE_VDD_PFETSTR_SNS: Not used any more.
5:9	ROX	IVRM_CORE_VCS_PFETSTR_SNS: This register is assigned to the signals tcex##_tp_ivrm_core_vcs_sense & tcex##_tp_ivrm_core_vdd_sense & tcex##_tp_ivrm_eco_vcs_sense & tcex##_tp_ivrm_eco_vdd_sense & 0b0
10:14	ROX	IVRM_ECO_VDD_PFETSTR_SNS: Not used any more.
15:19	ROX	IVRM_ECO_VCS_PFETSTR_SNS: Not used any more.
20	ROX	IVRM_VDD_CORE_PFETSTR_VALID_SNS: Not used any more.
21	ROX	IVRM_VCS_CORE_PFETSTR_VALID_SNS: Not used any more.
22	ROX	IVRM_VDD_ECO_PFETSTR_VALID_SNS: Not used any more.
23	ROX	IVRM_VCS_ECO_PFETSTR_VALID_SNS: Not used any more.
24	ROX	CORE_VDD_BYPASS_B_SENSE: Not used any more.
25	ROX	CORE_VCS_BYPASS_B_SENSE: Not used any more.
26	ROX	ECO_VDD_BYPASS_B_SENSE: Not used any more.
27	ROX	ECO_VCS_BYPASS_B_SENSE: Not used any more.
28	ROX	CORE_VDD_POWERON_SENSE: Not used any more.
29	ROX	CORE_VCS_POWERON_SENSE: Not used any more.
30	ROX	ECO_VDD_POWERON_SENSE: Not used any more.
31	ROX	ECO_VCS_POWERON_SENSE: Not used any more.
32	ROX	CORE_VDD_VPUMP_EN_SENSE: Not used any more.
33	ROX	CORE_VCS_VPUMP_EN_SENSE: Not used any more.
34	ROX	ECO_VDD_VPUMP_EN_SENSE: Not used any more.
35	ROX	ECO_VCS_VPUMP_EN_SENSE: Not used any more.
36	ROX	CORE_VDD_PFET_LOW_VOUT_SNS: Not used any more.
37	ROX	CORE_VCS_PFET_LOW_VOUT_SNS: Not used any more.
38	ROX	ECO_VDD_PFET_LOW_VOUT_SNS: Not used any more.
39	ROX	ECO_VCS_PFET_LOW_VOUT_SNS: Not used any more.

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Register Name	<i>PPMICR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_IDLE_CONTROL_REG
Address	000000001E0F0158 (PCB)
Attributes	
Description	Used to read the PMICR register typically owned (written) by the hypervisor. Writes are conditioned on the setting of the dial Pm_spr_override_en. If Pm_spr_override_en is set, firmware must make sure that the special wakeup state of this chiplet is reached before changing any of the latency fields in this register. Otherwise, the hardware behavior is undefined.

Bits	PCB	Field Mnemonic: Description
0:7	ROX	NAP_PSTATE_REQ: Nap Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
8	ROX	NAP_PSTATE_EN: Nap PState Enable 1 = Enable the Nap Pstate (NPS) Request, Nap Global Enable and Nap Latency functions 0 = Disables the Nap Pstate (NPS) Request, Nap Global Enable and Nap Latency functions Reads from the field return the value last written.
9	ROX	NAP_GLOBAL_EN: Nap Global Enable 1 = Upon the execution of a Nap instruction , the Nap Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a Nap instruction , the Nap Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.
10:11	ROX	NAP_LATENCY: Nap Latency not supported for POWER8 processor
12:15	ROX	RESERVED_PPMICR_0: reserved
16:23	ROX	SLEEP_PSTATE_REQ: sleep Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
24	ROX	SLEEP_PSTATE_EN: sleep PState Enable 1 = Enable the sleep Pstate (NPS) Request, sleep Global Enable and sleep Latency functions 0 = Disables the sleep Pstate (NPS) Request, sleep Global Enable and sleep Latency functions Reads from the field return the value last written.
25	ROX	SLEEP_GLOBAL_EN: sleep Global Enable 1 = Upon the execution of a sleep instruction , the sleep Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a sleep instruction , the sleep Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.



Bits	PCB	Field Mnemonic: Description
26:27	ROX	SLEEP_LATENCY: sleep Latency 00 = Cease instructions and honors Pstate change but does not perform additional state changing actions (unsupported in POWER8, maps to 0b10) 01 = Indicates to the platform that a sub-state that would have the lowest latency is enabled (unsupported in POWER8, maps to 0b10) 10 = Indicates to the platform that a sub-state that might have a medium exit latency is enabled (POWER8: Fast Sleep) 11 = Indicates to the platform that a sub-state that might have higher exit latency is enabled (POWER8: Deep Sleep)
28:31	ROX	RESERVED_PPMICR_1: reserved
32:39	ROX	WINKLE_PSTATE_REQ: winkle Pstate (NPS) Request Writes to this field will initiate a coordination action with any available central element that will arbitrate between other cores that may share a power rail with this core. Reads from the field return the value last written. Value is an 8 bit signed integer representing an offset from Fnominal. Legal values are +127 to -128 with the value increment being platform dependent.
40	ROX	WINKLE_PSTATE_EN: winkle PState Enable 1 = Enable the winkle Pstate (NPS) Request, winkle Global Enable and winkle Latency functions 0 = Disables the winkle Pstate (NPS) Request, winkle Global Enable and winkle Latency functions Reads from the field return the value last written.
41	ROX	WINKLE_GLOBAL_EN: winkle Global Enable 1 = Upon the execution of a winkle instruction , the winkle Pstate (NPS) Request is be sent to the central element as a Global Pstate Request 0 = Upon the execution of a winkle instruction , the winkle Pstate (NPS) Request is be sent to the local element as a Local Pstate Request Reads from the field return the value last written.
42:43	ROX	WINKLE_LATENCY: winkle Latency 00 = Cease instructions and honors Pstate change but does not perform additional state changing actions (unsupported in POWER8, maps to 0b10) 01 = Indicates to the platform that a sub-state that would have the lowest latency is enabled (unsupported in POWER8, maps to 0b10) 10 = Indicates to the platform that a sub-state that might have a medium exit latency is enabled (POWER8: Fast Winkle) 11 = Indicates to the platform that a sub-state that might have higher exit latency is enabled (POWER8: Deep Winkle)
44:47	ROX	RESERVED_PPMICR_2: reserved

Register Name	<i>PPMCR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_CONTROL_REG
Address	000000001E0F0159 (PCB)
Attributes	
Description	Provides read access to the PMCR register shadow in the PCBS, typically owned (written) by the hypervisor. Writes are conditioned on the setting of PMGP1[pm_spr_override_en].

Bits	PCB	Field Mnemonic: Description
0:7	RWX	GLOBAL_PSTATE_REQ: global Pstate request from hypervisor (or OCC)
8:15	RWX	LOCAL_PSTATE_REQ: local Pstate request from hypervisor or OCC
16	RWX	AUTO_OVERRIDE0_PSTATE_LIMIT_EN: automatic override Pstate 0 (for low activity detection) is enabled, if asserted

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Bits	PCB	Field Mnemonic: Description
17	RWX	AUTO_OVERRIDE1_PSTATE_LIMIT_EN: automatic override Pstate 1 (reserved for future use) is enabled, if asserted
18:23	RWX	RESERVED_PPMCR: reserved
24:31	RWX	AUTO_OVERRIDE_PSTATE0: automatic override Pstate 0 (for low activity detection)
32:39	RWX	AUTO_OVERRIDE_PSTATE1: automatic override Pstate 1 (reserved for future use)

Register Name	<i>Control Register That Is Written By PMC Sequencer</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_PMC_VF_CTRL_REG
Address	000000001E0F015A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PGLOBAL_ACTUAL: global actual Pstate
8:15	RW	MAXREGVCS: maximum regulation point for Vcs, Bit 0 is reserved, bits 1 to 7 are in iVID format
16:23	RW	MAXREGVDD: maximum regulation point for Vdd, Bit 0 is reserved, bits 1 to 7 are in iVID format
24:31	RW	EVIDVCS_EFF: eff. external voltage ID for Vcs in iVID format, Bit 0 is reserved
32:39	RW	EVIDVDD_EFF: eff. external voltage ID for Vdd in iVID format, Bit 0 is reserved

Register Name	<i>Undervolting Register For PCBS</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_UNDERVOLTING_REG
Address	000000001E0F015B (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PUV_MIN: minimum Pstate for which undervolting is allowed
8:15	RW	PUV_MAX: maximum Pstate for which undervolting is allowed
16:21	RW	KUV: this value indicates how many Pstate ticks a voltage request is undervolted (clipped with Puv_min). Note that the Kuv value is signed

Register Name	<i>The PPSIBR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_INDEX_BOUND_REG
Address	000000001E0F015C (PCB)
Attributes	
Description	Enables setting the minimum and maximum Pstate that is supported as a pointer into the local Pstate table (which has entries from 0 to 127).



Bits	PCB	Field Mnemonic: Description
0:7	RW	LPSI_MIN: this Pstate index is the index that corresponds to array entry 0. Note that the index domain is obtained by adding 128 to a Pstate, thus, the value is unsigned.
8:14	RW	LPSI_ENTRIES_MINUS_1: this dial contains the value of the number of entries in the Pstate table minus 1

Register Name	PPMBR Register	
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_POWER_MANAGEMENT_BOUNDS_REG	
Address	000000001E0F015D (PCB)	
Attributes		
Description	Enables setting the Pstate bounds that are managed by the OCC. If dial Enable_pmc_pmax_sync_notification is set, firmware must wait after each write to this register until the PMC has received the Pmax Sync Interrupt. If a write happens to this register while the previously scheduled Pmax Sync Interrupt has not yet left PCBs, the error TBD will be set.	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PMIN_CLIP: minimum Pstate allowed for this chiplet
8:15	RW	PMAX_CLIP: maximum Pstate allowed for this chiplet (has to be greater or equal to Pmin_clip)

Register Name	PPTCR Register	
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_CTRL_REG	
Address	000000001E0F015E (PCB)	
Attributes		
Description	Controls the address for writing the local Pstate table array (all 96 words are accessible). Note that the protocol requires this register to be set up with the Pstate address first, if a read or a write of the Pstate array is intended, to make sure that the initial address is set correctly. The register PPTR must always be written or read afterward. Note that any access to the PPTR auto-increments this register.	

Bits	PCB	Field Mnemonic: Description
0:6	RWX	PSTATE_TABLE_ADDRESS: This is the address of the Pstate table in PCBs, which is auto-incremented after any access to the PTLR.

Register Name	The PPTR Register	
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_TABLE_REG	
Address	000000001E0F015F (PCB)	
Attributes		
Description	Controls the data to be written into the Pstate table and returns the data for a read of the Pstate table. Note that the protocol requires for a write to set this register up after first setting up PPTCR (if the user does not rely on the auto-increment function of the address). For a read of the Pstate table, this register must be read after first setting up PPTCR as well (again if the auto-increment feature of the address is not used). Any access to this register auto-increments the Pstate_table_address by 1. Note also that the read functionality of this register is only functional if PIVRMCSR[ivrm_fsm_enable] = 0. The write functionality works in any case.	

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Bits	PCB	Field Mnemonic: Description
0:63	RW	pstate_data This is the field for data bits 0 to 63

Register Name	<i>The PPSTR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_PSTATE_STEP_TARGET_REG
Address	000000001E0F0160 (PCB)
Attributes	
Description	Provides read access to several intermediate values in the Pstate computation pipeline. Writes are conditioned on the setting of PMGP0[enable_OCC_ctrl_for_local_Pstate_eff_req].

Bits	PCB	Field Mnemonic: Description
0:7	RWX	LOCAL_PSTATE_EFF_REQ: this field represents the effective local Pstate request right before the clipping with Pmin and Pmax if enable_OCC_ctrl_for_local_Pstate_eff_req=0 then the hardware controls this dial, that updates every cycle if enable_OCC_ctrl_for_local_Pstate_eff_req=1 then OCC is in control and can write this field to control the effective local Pstate request that will eventually propagate through the downstream logic and determine the Local PState Actual. Note: if no write to this register is performed, the currently established value is maintained stable forever.
8:15	ROX	LOCAL_PSTATE_TARGET: This field is the target Pstate of a complete Pstate change that is performed in smaller steps
16:23	ROX	LOCAL_CORE_PSTATE_STEP_TARGET: this field represents the intermediate value that is about to be established as the next Local Pstate Actual after completing one step in the process of the transition towards the 'local_Pstate_target' the new voltage, frequency, and clock resonance setting
24:31	ROX	LOCAL_ECO_PSTATE_STEP_TARGET: this field represents the intermediate value that is about to be established as the next Local Pstate Actual after completing one step in the process of the transition towards the 'local_Pstate_target' the new voltage, frequency, and clock resonance setting

Register Name	<i>Read-Only Status Register For DPLL And For Debugging (PDSR)</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_DPLL_STATUS_REG
Address	000000001E0F0161 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:14	ROX	DPLL_FF_FREQOUT: frequout output from DPLL (current frequency - bits 2 to 10 correspond to the same scale as the 9 bits of frequin (which need to be multiplied with our frequency step to get the real frequency), the remaining bits just provide a higher accuracy)
15	ROX	DPLL_FREQU_CHANGE: DPLL Frequency change (pin of DPLL without filter)
16	ROX	DPLL_STATUS_SPARE_BIT1: Spare bit.
17	ROX	PMAX_SYNC_PENDING: gets asserted, if the logic has a Pmax sync interrupt outstanding that will be eventually sent to PMC when the Pmax sync criterion is met
18	ROX	GA_ACK_PENDING: gets asserted, if the logic has a global actual Pstate update acknowledgment interrupt outstanding that will be eventually sent to PMC when the GA ack criterion is met
19:26	ROX	CAPPED_GLOBAL_PSTATE_REQ: corresponds to the capped global Pstate request that is presented as Pstate interrupt and send to PMC



Bits	PCB	Field Mnemonic: Description
27	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT2: DPLL runs at Fmax and CPM bit 2 is set. Note that this bit and the following 2 bits indicate, that the CPMs would allow the DPLL to run faster than Fmax.
28	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT3: DPLL runs at Fmax and CPM bit 3 is set
29	ROX_CLRPAR T	DPLL_FMAX_AND_CPMBIT4: DPLL runs at Fmax and CPM bit 4 is set
30	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT2: DPLL runs at Fmin and CPM bit2 is zero. Note that this bit and the following 2 bits indicate, that the CPMs indicate, that the DPLL should run slower than the currently established Fmin.
31	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT1: DPLL runs at Fmin and CPM bit1 is zero
32	ROX_CLRPAR T	DPLL_FMIN_AND_NOT_CPMBIT0: DPLL runs at Fmin and CPM bit0 is zero
33	ROX_CLRPAR T	DPLL_FASTER_THAN_FMAX_PLUS_DELTA1: The DPLL indicated that it ran once faster than Fmax+dppl_char_delta1
34	ROX_CLRPAR T	DPLL_SLOWER_THAN_FMIN_MINUS_DELTA2: The DPLL indicated that it ran once slower than Fmin-dpll_char_delta2
35:48	ROX	DPLL_MAX_FREQOUT_AFTER_LAST_READ: This dial indicates the maximum DPLL frequout value after the last read of this register (only 14 MSBs)
49:62	ROX	DPLL_MIN_FREQOUT_AFTER_LAST_READ: This dial indicates the minimum DPLL frequout value after the last read of this register (only 14 MSBs)

Register Name	<i>The PIVRMVCR0 Controls The Voltage Stepping Delays</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG0
Address	000000001E0F0162 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	IVRM_REQ_PSTATE_STEPDELAY_RISING: Requested Internal Pstate Baby Step Delay - Rising Step. Delay before allowing the next step for a rising Pstate Transition. This dial and ivrm_req_Pstate_stepdelay_lowering allow for differing delays for the two directional transitions if necessary. In 100ns units as established by scan dial ivrm_100ns_value
8:15	RW	IVRM_REQ_PSTATE_STEPDELAY_LOWERING: Requested Internal Pstate Baby Step Delay - Lowering Step. Delay before allowing the next step for a lower Pstate Transition. This dial and ivrm_req_Pstate_stepdelay_rising allow for differing delays for the two directional transitions if necessary. In 100ns units as established by scan dial ivrm_100ns_value

Register Name	<i>The PIVRMVCR1 Controls The Voltage Stepping Delays</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_IVRM_VID_CONTROL_REG1
Address	000000001E0F0163 (PCB)
Attributes	
Description	

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Bits	PCB	Field Mnemonic: Description
0:7	RW	IVRM_STABILIZE_DELAY_RUN: Stabilization Delay - Run Time Delay to allow a rail to stabilize upon a baby step while the region is operational. In 100ns units as established by scan dial ivrm_100ns_value
8:15	RW	IVRM_STABILIZE_DELAY_IDLE: Stabilization Delay - Idle Transition Delay to allow a rail to stabilize upon a baby step during an idle transition where the activity in the region is quiesced. In 100ns units as established by scan dial ivrm_100ns_value
16:23	RW	IVRM_PFSTR_PROP_DELAY: PFET Strength Propagation Delay Time from PFET Strength values being launched till PFET Strength Valid is asserted. In order to ensure like rails across domains (Core VDD<>ECO VDD, Core VCS<>ECO VCS) are in sync during operational mode, this time value applies to all rails across the domains. This parameter allows for PFET Strength values to settle before PFET Strength Valid is sampled in the Uregs. The value set must the maximum delay for the worst rail timing and must allow for any metastability settling (for example, normally 2-3 cycles for single signals in an asynch handshake interface)
24:31	RW	IVRM_PFSTRVALID_PROP_DELAY: PFETStrength Valid Propagation Delay Time from ivrm_pfstr_prop_delay expiring to where PFET Strength Valid is deasserted. The value is the maximum of a) the minimum pulse width required for PFETStrength Valid and b) the propagation of PFETStrength Valid through (or enough of) the daisy chain. In order to ensure like rails across domains (Core VDD<>ECO VDD, Core VCS<>ECO VCS) are in sync during operational mode, this time value applies to all rails across the domains and thus must be the set to the value of the worst (slowest) rail. The minimum pulse width cannot be violated. The propagation delay can be tuned for more aggressive timing (for example, de-assert before the actual propagation is complete). Measured in prv_nclk cycles. The min delay is 2 cycles. Additional delay can be configured with the following settings 0x00 = No additional delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks
32:39	RW	IVRM_VPUMP_POWERON_TIME: iVRM (VRreg and UReg) - Vpump Power On Time Time necessary for the distributed internal VRM macro circuits to power on. Same delay is required for power on voltage pump circuit. Both delays are in the 8us range. In 100ns units as established by scan dial ivrm_100ns_value
40:47	RW	IVRM_BYPASS_DELAY: iVRM Bypass Propagation Delay Delay time for bypass_b signal propagation. Measured in prv_nclk cycles Target: 50ns 0x00 = No delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks

Bits	PCB	Field Mnemonic: Description
48:55	RW	PFET_VPUMP_ENABLE_DELAY: PFET and Vpump Enable Propagation Delay Delay time for PFET enable and vpump enable signal propagation. Target: 130ns Measured in prv_nclk cycles 0x00 = No delay 0x01 = 1 prv_nclk ... 0xFF = 255 prv_nclks
56:62	RW	IVRM_VID_VOUT_THRESHOLD: VID threshold If the output voltage (Vout) is targeting a value below this threshold the slow PFET can backed off from its normal drive strength so as to reduce the ripple at these lower voltage conditions

Register Name	POHR Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_OCC_HEARTBEAT_REG
Address	000000001E0F0164 (PCB)
Attributes	
Description	Controls the behavior of the OCC heartbeat function.

Bits	PCB	Field Mnemonic: Description
0:7	RW	occ_heartbeat_time 'OCC Heartbeat Time Value' " 'This field defines the number of ~64us hang timer pulses in which a a PCB read or write of the heartbeat trigger register (of which the offset is specified by dial occ_heartbeat_reg_addr_offset) is not detected that will constitute the loss of the OCC heartbeat. If occ_heartbeat_en is set and upon this loss detection, POHBR[psafe] is forced and, if enabled, the error TBD is activated ' " '0x00 - unsupported, causes undefined behavior' '0x01 - 64us +0/-1us' '0x02 - 128us +0/-1us' '...' '0xFF - 16320us +0/-1us 16.3ms' " 'Upon the 64us hang pulse, the decremter ticks. if the decremter reaches x00, the heartbeat loss event is triggered.' "
8	RW	occ_heartbeat_enable 'OCC Heartbeat Timer Enable' " '0 = Disable the OCC Heartbeat function. Lack of accesses to the register defined by the dial occ_heartbeat_reg_addr_offset does not result in heartbeat loss events to be triggered (no FIRs set nor Safe mode entry).' " '1 = Enable the OCC Heartbeat function. '
9:16	RW	occ_heartbeat_reg_addr_offset This dial allows to configure the address offset within the PCBS power management entity of the register, that will regularly reset the heartbeat timer (which is called heartbeat trigger register). The address offset is 0x100 plus the value of this dial.
17:24	RW	Psafe 'Pstate Safe' " 'This field establishes the Pstate that the core chiplet will take on if: 'psafe <= PMSR[global_actual_pstate] 'AND any of the following conditions are true: 'Loss of OCC Heartbeat if occ_heartbeat_en is set' 'PMGP0[force_safe_mode] is set' " 'If psafe > PMSR[global_actual_pstate], the global_actual_pstate is forced.' " "The value of Psafe needs to be at or below the nominal Pstate to make sure safe operation of all chiplets. '

Register Name	PRCCR0 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG 0
Address	000000001E0F0165 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function.

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Bits	PCB	Field Mnemonic: Description
0	ROX	RESCLK_DIS: Resonant Clock Enable Master enable of all resonant clocking functions. This dial can be set by setting GP3(22) and can not be set in this PCBS_resonant_Clock_Control_Reg0. 1 = Resonant Clock function is disabled. Default values (0) for resclk_value, resclk_core_sync_value, csb_eco_sync_value 0 = Resonant Clock Control hardware is enabled (the mode is defined by dial resclk_control_mode)
1	RW	RESCLK_CONTROL_MODE: Resonant Clock Control Mode Defines the control means enabled when resclk_dis is not set. 0 = Pstate band hardware mechanism enabled 1 = Manual mode enabled (Firmware mode) If this bit is set to 0, the hardware control mechanism that manages the transition across the Resonant Bands is enabled. If this bit is set to 1, the automatic Pstate band hardware mechanism is disabled and the Firmware is in control of all values of the dial resclk_value, resclk_core_sync_value, csb_eco_sync_value. Firmware must ensure that frequency changes will not cross resonant bands or machine failures may result. resclk_value represents the values for clock sector buffer strength, inductor switch strength and high inductor enable. Firmware must ensure the correct stepping in/out the different bands and propagation of the values (resclk_value) to the core/eco (resclk_core_sync_value / csb_eco_sync_value).
2:4	RW	RESCLK_SYNC_PW: Resonant Clock Sync Pulse Width Number of nest/4 cycles to assert the clock sync signal. This value must be high enough to ensure capture and propagation across the asynchronous chiplet boundary.
5:11	RW	RES_SYNC_DELAY_CNT: Resonant Clock Sync Delay Number of nest/4 cycles wait after the launch of the resclk_value (csb and inductor) before launching the sync to allow these to be captured. This value must be high enough to ensure full propagation to the input of the clock sector buffers and inductor switches.
12:26	RW	RES_CSB_STR_INSTR_LO: Resonant Clock Sector Buffer Strength Instruction - Low Band Mask value that determines whether, during a fixed 15 step sequence, the res_csb_str(0:3) is to be decremented/incremented in entering/exiting the Low Band. During resonant clock Entry, res_csb_str(0:3) decremented by the value pattern from 0 down to 14. During resonant clock Exit, res_csb_str(0:3) incremented by the value pattern from 14 up to 0.
27:41	RW	RES_CSB_STR_INSTR_HI: Resonant Clock Sector Buffer Strength Instruction - High Band Mask value that determines whether, during a fixed 15 step sequence, the res_csb_str(0:3) is to be decremented/incremented in entering/exiting the High Band. During resonant clock Entry, res_csb_str(0:3) decremented by the value pattern from 0 down to 14. During resonant clock Exit, res_csb_str(0:3) incremented by the value pattern from 14 up to 0.

Register Name	PRCCR1 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_CONTROL_REG 1
Address	000000001E0F0166 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function. Writes are conditioned.

Bits	PCB	Field Mnemonic: Description
0:7	RW	FULL_CSB_PS: Full Clock Sector Buffer Pstate Pstate defining the maximum point where the clock sector buffer must be driven to full strength. This allow clocks to be distributed at low Vmin levels. FW needs to make sure that no overlaps occur with bands 2 or 3.
8:15	RW	RES_LOW_LOWER_PS: Low Frequency Resonant Lower (LFRLow) Pstate Pstate defining the lower frequency of the Low Resonant Frequency Band. FW needs to make sure that no overlap occurs with band 0.

Bits	PCB	Field Mnemonic: Description
16:23	RW	RES_LOW_UPPER_PS: Low Frequency Resonant Upper (LFRUpper) Pstate Pstate defining the upper frequency of the Low Resonant Frequency Band. Note that if an overlap occurs with band 3, the hardware behavior is undefined.
24:31	RW	RES_HIGH_LOWER_PS: High Frequency Resonant Lower (HFRLow) Pstate Pstate defining the lower frequency of the High Resonant Frequency Band. Note that if an overlap occurs with band 2, the hardware behavior is undefined.
32:39	RW	RES_HIGH_UPPER_PS: High Frequency Resonant Upper (LFRUpper) Pstate Pstate defining the upper frequency of the High Resonant Frequency Band. This value needs to be greater or equal to high_res_lower_ps.
40:43	RW	NONRES_CSB_VALUE_TI: Clock Sector Buffer Table Index for non-resonant state Table Index into Clock Sector Buffer Table for the nominal, non-resonant state.
44:47	RW	FULL_CSB_VALUE_TI: Clock Sector Buffer Table Index for full CSB value Table Index into Clock Sector Buffer Table for the full CSB strength value.
48:56	RWX	RESCLK_VALUE: Output register driving the 9 bit resclk_value In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current resclk_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. The value in this register represents the following concatenation: csb_str_value(0:3) sw_str(0:3) hi_induct_en.
57	RWX	RESCLK_CORE_SYNC_VALUE: Output register driving the resclk_core_sync signal In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current resclk_core_sync_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. This bit is supposed to be used in order to create a SCOM-controlled pulse to force an update of the resclk propagation registers. A 1 enables the synchronous update, a 0 disables it. Suggested use of this bit is to set it to 1 and then set it back to 0 to create a (long) update pulse.
58	RWX	CSB_ECO_SYNC_VALUE: Output register driving the csb_eco_sync signal In Pstate-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 0) then this is a read-only register to report the current csb_eco_sync_value chosen by the HW. In Manual-mode (PCBS_Resonant_Clock_Control_Reg0[resclk_dis] = 0 and PCBS_Resonant_Clock_Control_Reg0[resclk_control_mode] = 1) then this is a read-write register and the user can control the resonance settings via SCOM. This bit is supposed to be used in order enable the ECO domain to participate in clock sector buffer strength changes, when switching from nominal strength to full CSB strength. A 1 enables the ECO domain, a 0 disables it from seeing a CSB strength update.

Register Name	PRCCR1 Register
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_RESONANT_CLOCK_STATUS_REG
Address	000000001E0F0167 (PCB)
Attributes	
Description	Controls the behavior of the resonant clocking function.



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Bits	PCB	Field Mnemonic: Description
0	ROX	RESCLK_STATE: Resonant Clock State 0 = Resonant Clocking inactive 1 = Resonant Clocking active Valid if resclk_inprogress = 0. Hardware sets this bit to the right value at the completion of the transition into and out of resonance mode.

Bits	PCB	Field Mnemonic: Description
1	ROX	RES_HI_INDUCT_EN: Resonant High Inductor Enable Valid if resclk_inprogress = 0. This dial provides the current value being propagated. 0 = Resonant Clock mode not active 1 = Resonant Clock mode active
2	ROX	RESCLK_INPROGRESS: Resonant Clock Transition in Progress This bit is set by hardware while a transition is in progress and will be reset by hardware when the operation is complete.
3	ROX	RESCLK_FULL_CSB: Full CSB Clock State 0 = Full CSB Clocking inactive 1 = Full CSB Clocking active Valid if resclk_inprogress = 0. Hardware sets this bit to the right value at the completion of the transition into and out of full CSB mode respectively.

Register Name	<i>PLPFTCR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_CONTROL_REG
Address	000000001E0F0168 (PCB)
Attributes	
Description	Allows firmware to configure the modes that are used for the PCBS Local Pstate Frequency Target Status Register.

Bits	PCB	Field Mnemonic: Description
0:2	RW	DELAY_TIME: This field encodes the delay between the time a Local Actual Pstate change modifies the input to the DPLL and the time frequency acquisition begins to allow the hardware to ignore the frequency transition of the DPLL in order to get better frequency measurements. This field encodes a delay of ~1us to ~128us in power of 2 selects. The delay is defined by $2^{**}delay\_time$ in us. Note that the hardware uses multiples of the slow hang pulse that is running at 1us.
3	RW	RECORD_TRANSITIONS: This bit indicates whether the LPFTSR records events that correspond to Local Actual Pstate changes (and therefore may include DPLL slewing effects.) One usage model would set the periodic sample_time defined by the dial OHA_MODE_REG[tod_pulse_count_match_val] to a time less than the worst-case DPLL slew time but then ignore Pstate transitions because they might include DPLL slew effects.
4:18	RW	MULTIPLIER: This 15-bit unsigned constant is multiplied by the DPLL frequency code (9 bits) implied by the Local Actual Pstate to yield the 24-bit frequency target measured in PCBS-PM clock cycles (core clock / 2). Assuming times in seconds and frequencies in Hz, firmware should set this constant to: $(DPLL\_Frequency\_Code\_Step\_Hz * Sample\_Time\_Seconds) / 2$
19	RW	ENABLE_LPFT_FUNCTION: This is the enable bit to enable the local Pstate frequency target function. A '1' enables the function, a '0' disables it (the value can be changed at any time).

Register Name	<i>PLPFTSR Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_LOCAL_PSTATE_FREQUENCY_TARGET_STATUS_REG
Address	000000001E0F0169 (PCB)
Attributes	
Description	Allows firmware to observe local actual Pstate realized frequencies.

Registers Specification

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Bits	PCB	Field Mnemonic: Description
0	ROX_CLRPART	VALID: If this bit is set then all of the remaining fields of this register are valid. This bit is cleared whenever the register is read or after a local actual Pstate change occurs, and is will be set whenever the hardware completes a valid sample. If firmware reads this register and the valid bit is not set, then it indicates that the Local Pstate target frequency acquisition logic has not been able to complete a frequency acquisition for any Local Actual Pstate change since the last time the LPFTSR was read. This could be due to either of the following factors: 1. Firmware is sampling the LPFTSR faster than the time implied by the sample time defined in OHA by the dial OHA_MODE_REG[tod_pulse_count_match_val] field
1	ROX	CPM_DPLL: If the valid bit is set, then if cpm_dpll is set it indicates that the event recorded by this register was due to a Local Actual Pstate implemented by the DPLL running in CPM-DPLL mode, otherwise the value of this bit is undefined. If the valid bit is not set, this bit is undefined.
2	ROX	IVRM: If the valid bit is set, then if ivrm is set it indicates that the event recorded by this register was due to a Local Actual Pstate whose voltage was set locally by the iVRM operating entirely in regulation mode. If the valid bit is not set, this bit is undefined.
3	ROX	TRANSITION: If the valid bit is set, then if transition is set it indicates that during the observation period a Local Pstate Actual change has occurred, and any performance delta may be due to DPLL frequency slewing. If the valid bit is not set, this bit is undefined
4	ROX	STABLE: If stable is set it indicates that the DPLL input frequency has been stable since the last time the PLPFTSR was read. This bit is set whenever the PLPFTSR is read, and cleared whenever the Fmax input of the DPLL changes. This bit is always valid, regardless of the state of the valid bit. If the PLPFTSR is read on the same cycle a frequency changes then the stable bit is cleared. This bit helps firmware better understand how to interpret the information contained in the PLPFTSR. (Note that this bit should have an attribute ROX_SETPART, but this is not supported by regchk.)
5:28	ROX	DELTA: If the valid bit is set then this is the 24-bit signed difference Measured Cycles - Target Cycles for the event captured by this register. If the valid bit is not set, this dial is undefined.
29:52	ROX	CUMULATIVE: This field records the 24-bit cumulative (signed) delta for all valid samples taken since this field was cleared. Writing any value to this register clears this field. Note that it should have an attribute WOX_CLRPART, but this is not supported by regchk/figtree.
53:60	ROX	PSTATE: If the valid bit is set then this is the Local Actual Pstate of the frequency acquisition that had the minimum (signed) delta of any valid sample taken since the last time the LPFTSR was read. If the valid bit is not set, then this field is undefined.

Register Name	<i>The PFSMM1/2 Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR1_REG
Address	000000001E0F0170 (PCB)
Attributes	
Description	Facilitates debug by providing insight into the internal FSM states of the PCB-slave power-management unit. For expert use only. Coding according to VHDL design.

Bits	PCB	Field Mnemonic: Description
0:6	ROX	BABYSTEP_MAIN_FSM: Main Babystep FSM (mfsm_lt)
7:11	ROX	BABYSTEP_SLAVE_FSM: Babystep Slave FSM (sfsm_lt)
12:16	ROX	CORE_RAILSTEPPER_MAIN_FSM: Main Core Railstepper FSM (mrsfsm_lt)
17:21	ROX	ECO_RAILSTEPPER_MAIN_FSM: Main ECO Railstepper FSM (mrsfsm_lt)



Bits	PCB	Field Mnemonic: Description
22:25	ROX	CORE_RAILSTEPPER_SUB_FSM: Core Railstepper Sub-FSM (srsfsm_lt)
26:29	ROX	ECO_RAILSTEPPER_SUB_FSM: ECO Railstepper Sub-FSM (srsfsm_lt)
30:34	ROX	CORE_RAILSTEPPER_BYP_FSM: Core Railstepper Bypass FSM (byp_fsm_lt)
35:39	ROX	ECO_RAILSTEPPER_BYP_FSM: ECO Railstepper Bypass FSM (byp_fsm_lt)
40:45	ROX	IVRM_CORE_VDD_SEQUENCER_FSM: Core iVRM Sequencer for Vdd (ivrm_fsm_lt)
46:51	ROX	IVRM_CORE_VCS_SEQUENCER_FSM: Core iVRM Sequencer for Vcs (ivrm_fsm_lt)
52:57	ROX	IVRM_ECO_VDD_SEQUENCER_FSM: ECO iVRM Sequencer for Vdd (ivrm_fsm_lt)
58:63	ROX	IVRM_ECO_VCS_SEQUENCER_FSM: ECO iVRM Sequencer for Vcs (ivrm_fsm_lt)

Register Name	<i>Refer To The Description Of PFSMM1.</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_PM_INST.PCBS_FSM_MONITOR2_REG
Address	000000001E0F0171 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:6	ROX	RESCLK_BAND_FSM: Band Sequencer for resonant clocking (band_fsm_lt)
7:10	ROX	RESCLK_LOWRES_FSM: Low Resonant Clocking sequencer (lowres_fsm_lt)
11:14	ROX	RESCLK_HIGHRES_FSM: High Resonant Clocking sequencer (highres_fsm_lt)
15:18	ROX	RESCLK_FULLCSB_FSM: Full-CSB Resonant Clocking sequencer (fullcsb_fsm_lt)
19:22	ROX	RESCLK_UPDATE_FSM: Resonant Clocking Update sequencer (update_fsm_lt)
23:29	ROX	IDLE_TRANSITION_FSM: Idle State Sequence FSM (ifsm_lt)
30:37	ROX	Peco_step_target_uv Current ECO Step Target Pstate (different from Plocal_actual for undervolting)
38:45	ROX	Pcore_step_target_uv Current core Step Target Pstate (different from Plocal_actual for sleep and undervolting)

Register Name	<i>Protect Mode Register</i>
Mnemonic	EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.PROTECT_MODE_REG
Address	000000001E0F03FE (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	READ_PROTECT_ENABLE: Enable read protection
1	RW	WRITE_PROTECT_ENABLE: Enable write protection



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Register Name		<i>Atomic Lock Register</i>
Mnemonic		EH.TPCHIP.NET.PCBSLEX14.TP_PCB_SLAVE_INST.ATOMIC_LOCK_REG
Address		000000001E0F03FF (PCB)
Attributes		
Description		

Bits	PCB	Field Mnemonic: Description
0	RW	ATOMIC_LOCK_ENABLE: Enable atomic lock
1:4	ROX	ATOMIC_ID: Atomic ID