POWER8 Common Registers Specification

Advance

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Revision Log

Each release of this document supersedes all previously released versions. The revision log lists all significant changes made to the document since its initial release.

Version	Revision Date	Description
1.0	30 July 2014	Initial release.

About this Document

This document describes the IBM® POWER8™ registers used by both the POWER8 Processor and the POWER8 Memory Buffer. These registers are referred to as "common" registers. Throughout this document, the term “processor” refers to the POWER8 Processor and “memory buffer” refers to the POWER8 Memory Buffer.

To ensure you have the most current version of this document, visit the OpenPOWER Connect website.

Who Should Read this Document

This manual is intended for system software and hardware developers and application programmers who want to develop products for the POWER8 processor or the POWER8 memory buffer. It is assumed that the reader understands operating systems, microprocessor system design, basic principles of reduced instruction set computer (RISC) processing, and details of the Power Instruction Set Architecture (ISA).

Representation of Numbers

Numbers are generally shown in decimal format, unless designated as follows:

- Hexadecimal values are usually preceded by “0x.”
  For example: 0x000000000204000D
- Binary values in sentences are usually preceded by “0b.”
  For example: 0b1

Note: A bit value that is immaterial, which is called a “don't care” bit, is represented by an “X” or "x."

Bit Significance

In the POWER8 documentation, the smallest bit number represents the most significant bit of a field, and the largest bit number represents the least significant bit of a field.

Organization

The table of contents provides a list register names. An address map lists the registers in alphabetical order by mnemonic (see Chapter 2 on page 14). The registers themselves are arranged by their addresses.

Terminolgy

For definitions of the acronyms and abbreviations used in this document, see the Glossary on page 130.

Related Documents

The following documents can be helpful when reading this specification. They are available through OpenPOWER Connect or Power.org.

POWER8 Processor User's Manual for the Single-Chip Module
POWER8 Processor Datasheet for the Single-Chip Module
POWER8 Processor Registers Specification
POWER8 Memory Buffer Datasheet
POWER8 Memory Buffer User's Manual
POWER8 Memory Buffer Registers Specification

Power ISA User Instruction Set Architecture - Book I (Version 2.07)
Power ISA Virtual Environment Architecture - Book II (Version 2.07)
Power ISA Operating Environment Architecture (Server Environment) - Book III-S (Version 2.07)

1. Introduction

The POWER8 processor is a superscalar symmetric multiprocessor designed for use in servers and large-cluster systems. It uses IBM complementary metal-oxide semiconductor (CMOS) 22 nm silicon-on-insulator (SOI) technology with 15 metal layers. The POWER8 processor can have up to 12 cores enabled on a single chip in the single-chip module (SCM) configuration. Each core has eight threads using simultaneous multithreading (SMT). The SMT is dynamically tunable, so that each core can have one, two, four, or eight threads.

The IBM POWER8 memory buffer supports multiple system configurations. It uses a high-speed differential interface to communicate with a processor chip using a memory-agnostic protocol. The memory controller and associated memory-interface maintenance and calibration functions are initiated and contained within the memory buffer chip. The buffer also contains a 16 MB on-board cache to support prefetching and improve system performance.

This document describes the POWER8 registers used by both the POWER8 processor and the POWER8 memory buffer. These registers are referred to as "common" registers. Throughout this document, the term “processor” refers to the POWER8 processor and “memory buffer” refers to the POWER8 memory buffer.

1.1 Accessing Registers

A register can have multiple addresses with a different addresses for different chiplets. The types of access permitted can vary by chiplets. The following table summarizes the valid register access types.

Access Type	Description
RW	Readable and writable
RW_WOR	Readable and writable. A write ORs written data with existing data and stores the result.
RW_WAND	Readable and writable. A write ANDs written data with existing data and stores result.
RW_WCLEAR	Readable and writable. A write of a ‘1’ clears the bit. A write of a ‘0’ does nothing.
RW_WCLRPART	Readable and writable. Any write to the address clears the bits regardless of value.
RW_WSETPART	Readable and writable. Any write to the address sets the bits regardless of value.
WO	Same as RW, but bits are write-only.
WO_OR	Same as RW_WOR, but bits are write-only.
WO_AND	Same as RW_WAND, but bits are write-only.
WO_CLEAR	Same as RW_WCLEAR, but bits are write-only.
WO_CLRPART	Same as RW_WCLRPART, but bits are write-only.
WO_SETPART	Same as RW_WSETPART, but bits are write-only.
WO_nP Write	Only pulsed. A write of ‘1’ creates a pulse for n register clocks. A read returns ‘0’.
WO_n_mP	Write-only pulsed. A write of ‘1’ creates a pulse for a minimum of n register clocks and a maximum of m register clocks. A read returns ‘0’.
RO	Read only. Only to be used if a bit is tied. Status bits should be ROX.
NC	Not connected; that is, the data cannot be written or read by that access.
RWX	Same as RW, but unstable. Can be changed functionally.
RWX_WOR	Same as RW_WOR, but unstable. Can be changed functionally.
RWX_WAND	Same as RW_WAND, but unstable. Can be changed functionally.
RWX_WCLEAR	Same as RW_WCLEAR, but unstable. Can be changed functionally.
RWX_WCLRPART	Same as RW_WCLRPART, but unstable. Can be changed functionally.
RWX_WSETPART	Same as RW_WSETPART, but unstable. Can be changed functionally.
WOX	Same as WO, but unstable. Can be changed functionally.
WOX_OR	Same as WO_OR, but unstable. Can be changed functionally.

Access Type	Description
WOX_AND	Same as WO_AND, but unstable. Can be changed functionally.
WOX_CLEAR	Same as WO_CLEAR, but unstable. Can be changed functionally.
WOX_CLRPART	Same as WO_CLRPART, but unstable. Can be changed functionally.
WOX_SETPART	Same as WO_SETPART, but unstable. Can be changed functionally.
WOX_nP	Same as WO_nP, but unstable. Can be changed functionally.
WOX_n_mP	Same as WO_n_mP, but unstable. Can be changed functionally.
ROX	Same as RO, but unstable. Can be changed functionally.
ROX_CLRPART	Same as ROX, but a read access will clear the bits after they have been accessed.
NCX	Same as NC, but unstable. Can be changed functionally.

2. Address Table

The POWER8 Common registers are listed alphabetically by mnemonic in the following address table.

Mnemonic	Address	Page
ABUS.TX_WRAP.PLL_A.CWRAP.PLL_CNTRL0	0x0000000000000000	20
ABUS.TX_WRAP.PLL_A.CWRAP.PLL_CNTRL1	0x0000000000000001	31
ABUS.TX_WRAP.PLL_A.CWRAP.PLL_CNTRL2	0x0000000000000002	33
ABUS.TX_WRAP.PLL_A.CWRAP.PLL_CNTRL_SETUP0	0x0000000000000003	36
ABUS.TX_WRAP.PLL_A.CWRAP.PLL_CNTRL_SETUP1	0x0000000000000004	39
ABUS.TX_WRAP.PLL_A.CWRAP.PLL_CNTRL_SETUP2	0x0000000000000005	42
EH.TPC.CC_PROTECT_MODE_REG	0x00000000020303FE	117
EH.TPC.CLK_REGION	0x0000000002030006	113
EH.TPC.CLOCK_STAT	0x0000000002030008	114
EH.TPC.EPS.FIR.LOCAL_FIR_ACTION0	0x0000000002040010	121
EH.TPC.EPS.FIR.LOCAL_FIR_ACTION1	0x0000000002040011	121
EH.TPC.EPS.FIR.LOCAL_FIR_MASK	0x000000000204000D	121
EH.TPC.EPS.FIR.MODE_REG	0x0000000002040008	119
EH.TPC.EPS.PSC.DEBUG_STATUS_REG	0x0000000002010004	109
EH.TPC.EPS.PSC.PSCOM_MODE_REG	0x0000000002010000	109
EH.TPC.ERROR_STATUS	0x0000000002030009	116
EH.TPC.FIR_MASK	0x0000000002040002	118
EH.TPC.GP0	0x0000000002000000	28
EH.TPC.GP1	0x0000000002000001	107
EH.TPC.GP2	0x0000000002000002	107
EH.TPC.GP4	0x0000000002000003	108
EH.TPC.LOCAL_FIR	0x000000000204000A	120
EH.TPC.OPCG_REG0	0x0000000002030002	110
EH.TPC.OPCG_REG1	0x0000000002030003	111
EH.TPC.OPCG_REG2	0x0000000002030004	111
EH.TPC.OPCG_REG3	0x0000000002030005	112
EH.TPC.RFIR	0x0000000002040001	118
EH.TPC.SCANSELQ	0x0000000002030007	113
EH.TPC.SPATTN	0x0000000002040004	119
EH.TPC.SPA_MASK	0x0000000002040007	119
EH.TPC.XFIR	0x0000000002040000	117
EH.TPCHIP.NET.PCBSLNEST.GP3_REG	0x00000000020F0012	123
EH.TPCHIP.NET.PCBSLNEST.HANG_PULSE_0_REG	0x00000000020F0020	124
EH.TPCHIP.NET.PCBSLNEST.HANG_PULSE_1_REG	0x00000000020F0021	124
EH.TPCHIP.NET.PCBSLNEST.HANG_PULSE_2_REG	0x00000000020F0022	125
EH.TPCHIP.NET.PCBSLNEST.HANG_PULSE_3_REG	0x00000000020F0023	125
EH.TPCHIP.NET.PCBSLNEST.HANG_PULSE_4_REG	0x00000000020F0024	125
EH.TPCHIP.NET.PCBSLNEST.HANG_PULSE_5_REG	0x00000000020F0025	125
EH.TPCHIP.NET.PCBSLNEST.HANG_PULSE_6_REG	0x00000000020F0026	126
EH.TPCHIP.NET.PCBSLNEST.MULTICAST_GROUP_1	0x00000000020F0001	121
EH.TPCHIP.NET.PCBSLNEST.MULTICAST_GROUP_2	0x00000000020F0002	122
EH.TPCHIP.NET.PCBSLNEST.MULTICAST_GROUP_3	0x00000000020F0003	122

Mnemonic	Address	Page
EH.TPCHIP.NET.PCBSLNEST.MULTICAST_GROUP_4	0x00000000020F0004	123
EH.TPCHIP.NET.PCBSLNEST.PRE_COUNTER_REG	0x00000000020F0028	126
EH.TPCHIP.NET.PCBSLPERV.CLK_ADJ_SET	0x00000000010F0016	74
EH.TPCHIP.NET.PCBSLPERV.HANG_PULSE_0_REG	0x00000000010F0020	105
EH.TPCHIP.NET.PCBSLPERV.HANG_PULSE_1_REG	0x00000000010F0021	105
EH.TPCHIP.NET.PCBSLPERV.HANG_PULSE_2_REG	0x00000000010F0022	105
EH.TPCHIP.NET.PCBSLPERV.HANG_PULSE_3_REG	0x00000000010F0023	105
EH.TPCHIP.NET.PCBSLPERV.HANG_PULSE_4_REG	0x00000000010F0024	106
EH.TPCHIP.NET.PCBSLPERV.HANG_PULSE_5_REG	0x00000000010F0025	106
EH.TPCHIP.NET.PCBSLPERV.HANG_PULSE_6_REG	0x00000000010F0026	106
EH.TPCHIP.NET.PCBSLPERV.MULTICAST_GROUP_1	0x00000000010F0001	103
EH.TPCHIP.NET.PCBSLPERV.MULTICAST_GROUP_2	0x00000000010F0002	103
EH.TPCHIP.NET.PCBSLPERV.MULTICAST_GROUP_3	0x00000000010F0003	104
EH.TPCHIP.NET.PCBSLPERV.MULTICAST_GROUP_4	0x00000000010F0004	104
EH.TPCHIP.NET.PCBSLPERV.PLL_LOCK_REG	0x00000000010F0019	74
EH.TPCHIP.NET.PCBSLPERV.PRE_COUNTER_REG	0x00000000010F0028	106
EH.TPCHIP.PIB.ECCB.ECC_ADDRESS_REG	0x00000000000C0004	74
EH.TPCHIP.PIB.I2CM.COMMAND_REGISTER_0	0x00000000000A0005	76
EH.TPCHIP.PIB.I2CM.CONTROL_REGISTER_0	0x00000000000A0000	74
EH.TPCHIP.PIB.I2CM.DATA_REGISTER_0	0x00000000000A0003	76
EH.TPCHIP.PIB.I2CM.IMM_RESET_I2C_0	0x00000000000A000B	78
EH.TPCHIP.PIB.I2CM.MODE_REGISTER_0	0x00000000000A0006	77
EH.TPCHIP.PIB.I2CM.RESET_REGISTER_0	0x00000000000A0001	75
EH.TPCHIP.PIB.I2CM.STATUS_REGISTER_0	0x00000000000A0002	75
EH.TPCHIP.PIB.I2CM.STATUS_REGISTER_ENGINE_0	0x00000000000A000B	78
EH.TPCHIP.PIB.OTP.OTPC_M.COMMAND_REGISTER	0x0000000000010000	66
EH.TPCHIP.PIB.PCBMS.DEVICE_ID_REG	0x00000000000F000F	81
EH.TPCHIP.PIB.PCBMS.ERROR_REG	0x00000000000F001F	63
EH.TPCHIP.PIB.PCBMS.FIRST_ERR_REG	0x00000000000F001E	82
EH.TPCHIP.PIB.PCBMS.INTERRUPT_TYPE_REG	0x00000000000F001A	82
EH.TPCHIP.PIB.PCBMS.MCAST_GRP_0_SLAVES_REG	0x00000000000F0000	79
EH.TPCHIP.PIB.PCBMS.MCAST_GRP_1_SLAVES_REG	0x00000000000F0001	60
EH.TPCHIP.PIB.PCBMS.MCAST_GRP_2_SLAVES_REG	0x00000000000F0002	60
EH.TPCHIP.PIB.PCBMS.MCAST_GRP_3_SLAVES_REG	0x00000000000F0003	60
EH.TPCHIP.PIB.PCBMS.MCAST_GRP_4_SLAVES_REG	0x00000000000F0004	61
EH.TPCHIP.PIB.PCBMS.REC_ACK_REG	0x00000000000F0010	79
EH.TPCHIP.PIB.PCBMS.REC_ERR_REG0	0x00000000000F0011	79
EH.TPCHIP.PIB.PCBMS.REC_ERR_REG1	0x00000000000F0012	61
EH.TPCHIP.PIB.PCBMS.RESET_REG	0x00000000000F001D	82
EH.TPCHIP.PIB.PCBMS.TIMEOUT_REG	0x00000000000F0019	63
EH.TPCHIP.PIB.TOD.TOD_CHIP_CTRL_REG	0x0000000000040010	59
EH.TPCHIP.PIB.TOD.TOD_I_PATH_CTRL_REG	0x0000000000040006	54
EH.TPCHIP.PIB.TOD.TOD_MISC_RESET_REG	0x000000000004000B	58
EH.TPCHIP.PIB.TOD.TOD_M_PATH_CTRL_REG	0x0000000000040000	46
EH.TPCHIP.PIB.TOD.TOD_PRI_PORT_0_CTRL_REG	0x0000000000040001	47
EH.TPCHIP.PIB.TOD.TOD_PRI_PORT_1_CTRL_REG	0x0000000000040002	49

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EH.TPCHIP.PIB.TOD.TOD_PROBE_SELECT_REG	0x000000000004000C	58
EH.TPCHIP.PIB.TOD.TOD_PSS_MSS_CTRL_REG	0x0000000000040007	55
EH.TPCHIP.PIB.TOD.TOD_PSS_MSS_STATUS_REG	0x0000000000040008	56
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EH.TPCHIP.PIB.TOD.TOD_S_PATH_STATUS_REG	0x000000000004000A	57
EH.TPCHIP.PIB.TOD.TOD_TX_TTYPE_0_REG	0x0000000000040011	60
EH.TPCHIP.TPC.CC_PROTECT_MODE_REG	0x00000000010303FE	97
EH.TPCHIP.TPC.CLK_REGION	0x0000000001030006	93
EH.TPCHIP.TPC.CLOCK_STAT	0x0000000001030008	94
EH.TPCHIP.TPC.EPS.FIR.LOCAL_FIR_ACTION0	0x0000000001040010	102
EH.TPCHIP.TPC.EPS.FIR.LOCAL_FIR_ACTION1	0x0000000001040011	102
EH.TPCHIP.TPC.EPS.FIR.LOCAL_FIR_MASK	0x000000000104000D	102
EH.TPCHIP.TPC.EPS.FIR.MODE_REG	0x0000000001040008	100
EH.TPCHIP.TPC.EPS.PSC.DEBUG_STATUS_REG	0x0000000001010004	86
EH.TPCHIP.TPC.EPS.PSC.PSCOM_MODE_REG	0x0000000001010000	85
EH.TPCHIP.TPC.ERROR_STATUS	0x0000000001030009	96
EH.TPCHIP.TPC.FIR_MASK	0x0000000001040002	99
EH.TPCHIP.TPC.GP0	0x0000000001000000	26
EH.TPCHIP.TPC.GP1	0x0000000001000001	83
EH.TPCHIP.TPC.GP2	0x0000000001000002	84
EH.TPCHIP.TPC.GP4	0x0000000001000003	84
EH.TPCHIP.TPC.ITR.COMP.INTERRUPT1_REG	0x0000000001020000	87
EH.TPCHIP.TPC.ITR.COMP.INTERRUPT2_REG	0x0000000001020003	87
EH.TPCHIP.TPC.ITR.COMP.INTERRUPT3_REG	0x0000000001020006	87
EH.TPCHIP.TPC.ITR.COMP.INTERRUPT4_REG	0x0000000001020009	87
EH.TPCHIP.TPC.ITR.COMP.INTERRUPT_CONF_REG	0x000000000102000F	88
EH.TPCHIP.TPC.ITR.COMP.INTERRUPT_HOLD_REG	0x0000000001020012	89
EH.TPCHIP.TPC.ITR.COMP.INTERRUPT_TYPE_MASK_REG	0x000000000102000C	88
EH.TPCHIP.TPC.ITR.MISC.ERROR_STATUS_REG	0x0000000001020014	89
EH.TPCHIP.TPC.ITR.MISC.HOST_MASK_REG	0x0000000001020013	89
EH.TPCHIP.TPC.ITR.OSCERR.OSCERR_HOLD	0x0000000001020019	89
EH.TPCHIP.TPC.ITR.OSCERR.OSCERR_MASK	0x000000000102001A	90
EH.TPCHIP.TPC.LOCAL_FIR	0x000000000104000A	101
EH.TPCHIP.TPC.OPCG_REG0	0x0000000001030002	90
EH.TPCHIP.TPC.OPCG_REG1	0x0000000001030003	91
EH.TPCHIP.TPC.OPCG_REG2	0x0000000001030004	91
EH.TPCHIP.TPC.OPCG_REG3	0x0000000001030005	92
EH.TPCHIP.TPC.RFIR	0x0000000001040001	98
EH.TPCHIP.TPC.SCANSELQ	0x0000000001030007	94
EH.TPCHIP.TPC.SPATTN	0x0000000001040004	99
EH.TPCHIP.TPC.SPA_MASK	0x0000000001040007	100
EH.TPCHIP.TPC.TRA.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG	0x0000000001010400	86
EH.TPCHIP.TPC.TRA.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG	0x0000000001010401	86
EH.TPCHIP.TPC.XFIR	0x0000000001040000	97
EN.PB.TPC.GP0	0x0000000004000000	29

Mnemonic	Address	Page
EX03.EC.FX.T0_XER	0x0000000000010000	67
EX03.EC.IFU.I.T0_LR	0x0000000000000040	127
EX03.EC.IFU.I.T3_CTR	0x000000000000004B	128
EX03.EC.IFU.I.T3_LR	0x0000000000000043	128
EX03.EC.LS.T0_AMR	0x0000000000000068	126
EX03.EC.LS.T1_AMR	0x0000000000000069	127
EX03.EC.LS.T3_AMR	0x000000000000006B	127
EX03.EC.PC.PC_NW.CORE_INSTRUCTION_DISPATCH	0x0000000000000040	128
EX03.EC.PC.PC_NW.CORE_MEM_C_LPAR3	0x000000000000004B	129
EX03.EC.PC.PC_NW.CORE_WORKRATE_FINISH	0x0000000000000043	128
EX03.EC.PC.PC_NW.TFC.T0_TFMR	0x0000000000000000	21
EX03.EC.PC.PC_NW.TFC.T1_TFMR	0x0000000000000001	31
EX03.EC.PC.PC_NW.TFC.T2_TFMR	0x0000000000000002	34
EX03.EC.PC.PC_NW.TFC.T3_TFMR	0x0000000000000003	36
EX03.EC.PC.PC_NW.TFC.T4_TFMR	0x0000000000000004	40
EX03.EC.PC.PC_NW.TFC.T5_TFMR	0x0000000000000005	42
EX03.EC.PC.PC_NW.THREAD4_MEM_HIER_A	0x0000000000000068	126
EX03.EC.PC.PC_NW.THREAD4_MEM_HIER_B	0x0000000000000069	127
EX03.EC.PC.PC_NW.THREAD5_INSTRUCTION_COMPLETE	0x000000000000006B	127
IOMC0.TX_WRAP.PLL_MCIO.CWRAP.PLL_CNTRL0	0x0000000000000000	23
IOMC0.TX_WRAP.PLL_MCIO.CWRAP.PLL_CNTRL1	0x0000000000000001	33
IOMC0.TX_WRAP.PLL_MCIO.CWRAP.PLL_CNTRL2	0x0000000000000002	35
IOMC0.TX_WRAP.PLL_MCIO.CWRAP.PLL_CNTRL_SETUP0	0x0000000000000003	38
IOMC0.TX_WRAP.PLL_MCIO.CWRAP.PLL_CNTRL_SETUP1	0x0000000000000004	41
IOMC0.TX_WRAP.PLL_MCIO.CWRAP.PLL_CNTRL_SETUP2	0x0000000000000005	43
IOMC1.TX_WRAP.PLL_MCIO.CWRAP.PLL_CNTRL0	0x0000000000000000	24
IOMC1.TX_WRAP.PLL_MCIO.CWRAP.PLL_CNTRL1	0x0000000000000001	33
IOMC1.TX_WRAP.PLL_MCIO.CWRAP.PLL_CNTRL2	0x0000000000000002	35
IOMC1.TX_WRAP.PLL_MCIO.CWRAP.PLL_CNTRL_SETUP0	0x0000000000000003	38
IOMC1.TX_WRAP.PLL_MCIO.CWRAP.PLL_CNTRL_SETUP1	0x0000000000000004	41
IOMC1.TX_WRAP.PLL_MCIO.CWRAP.PLL_CNTRL_SETUP2	0x0000000000000005	43
TPC.FSI.FSI2PIB.COMMAND_REGISTER	0x0000000000001002	65
TPC.FSI.FSI2PIB.DATA_REGISTER_0	0x0000000000001000	64
TPC.FSI.FSI2PIB.DATA_REGISTER_1	0x0000000000001001	65
TPC.FSI.FSI2PIB.RESET	0x0000000000001006	65
TPC.FSI.FSI2PIB.SET_PIB_RESET	0x0000000000001007	65
TPC.FSI.FSI2PIB.STATUS	0x0000000000001007	65
TPC.FSI.FSI_MAILBOX.FSXCOMP.FSXLOG.FSIGP3	0x0000000000002812	67
TPC.FSI.FSI_MAILBOX.FSXCOMP.FSXLOG.FSIGP4	0x0000000000002813	68
TPC.FSI.FSI_MAILBOX.FSXCOMP.FSXLOG.FSIGP5	0x0000000000002814	69
TPC.FSI.FSI_MAILBOX.FSXCOMP.FSXLOG.FSIGP6	0x0000000000002815	70
TPC.FSI.FSI_MAILBOX.FSXCOMP.FSXLOG.FSIGP7	0x0000000000002816	70
TPC.FSI.FSI_MAILBOX.FSXCOMP.FSXLOG.FSIGProcessor	0x0000000000002817	70
TPC.FSI.FSI_MAILBOX.FSXCOMP.FSXLOG.PERV_GP3	0x000000000000281B	71
TPC.FSI.FSI_MAILBOX.FSXCOMP.FSXLOG.SBE_VITAL	0x000000000000281C	72
TPC.FSI.FSI_MAILBOX.FSXCOMP.FSXLOG.SCRATCH_REGISTER_1	0x0000000000002838	73

Mnemonic	Address	Page
TPC.FSI.FSI_MAILBOX.FSXCOMP.FSXLOG.SCRATCH_REGISTER_2	0x0000000000002839	73
TPC.FSI.FSI_MAILBOX.FSXCOMP.FSXLOG.SCRATCH_REGISTER_3	0x000000000000283A	73
TPC.FSI.FSI_MAILBOX.FSXCOMP.FSXLOG.SCRATCH_REGISTER_4	0x000000000000283B	73
TPC.FSI.FSI_MAILBOX.FSXCOMP.FSXLOG.SNS1LTH	0x0000000000002819	71
TPC.FSI.FSI_MAILBOX.FSXCOMP.FSXLOG.SNS2LTH	0x000000000000281A	71
TPC.FSI.FSI_SHIFT.SHIFT_CONTROL_REGISTER_2	0x0000000000000C10	64
TPC.FSI.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#0.P.CMD_WRDAT	0x0000000000020000	67
TPC.FSI.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.CMD_WRDAT	0x0000000000030000	44
TPC.FSI.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.CRSIC	0x0000000000030005	44
TPC.FSI.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.CRSIM	0x0000000000030006	45
TPC.FSI.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.CRSIS	0x0000000000030007	45
TPC.FSI.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.LSTAT	0x0000000000030002	44
TPC.FSI.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.RESET	0x0000000000030004	44
TPC.FSI.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.RSIC	0x0000000000030008	45
TPC.FSI.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.RSIM	0x0000000000030009	45
TPC.FSI.FSI_SLAVE.FSI_A_MST_0_MSIEP4	0x0000000000000C10	64
TPC.FSI.FSI_SLAVE.FSI_B_MST_0_MSIEP4	0x0000000000000C10	64

3. Register Tables

The POWER8 Common registers are listed in the following tables.

Register Name	*PLL Control Register*
Mnemonic	ABUS.TX_WRAP.PLL_A.CWRAP.PLL_CNTRL0
Address	0000000000000000 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0:2	RW	Reserved.
3	RW	BYPASSN: Bypass low active. When set to 0, this bit keeps PLL in bypass independent from external reset or bypass. For operation mode, set this bit to 1. 1: Off 0: On
4:8	RW	SPEDIV: PCLK divider control. Applies when PCLKSEL<2:0> = X10 or X11. <4:0> : freq divider
9:11	RW	CPISEL: Selects the current in the PLL charge pump based on application conditions. The charge pump is determined based on the baud rate and mult.factor. <2:0>= 000: 50 ua 001: 100 ua 010: 150 ua 011: 200 ua 100: 250 ua 101: 300 ua 110: 350 ua 111: 400 ua
12:20	RW	DIVSELB: Selects the feedback divider setting 2*(2-255) or 4-510.
21:22	RW	PCLKSEL: Selects the function of pclksel. <1:0>= 00: Off 01: VCO/spediv 10: ref 11: fb
23	RW	UNUSED0: Not used; keep at 0.
24:27	RO	BANDSEL: Capture the current bandsel of the PLL that is in use.
28	RW	ANALOGTUNE0: Unused. PLL input is driven by an external PIN (single-ended sel), not by the PLL control latch.
29	RW	ANALOGTUNE1: ICP tuning based on band select. 0: Enabled. 1: Disabled.
30:31	RW	ANALOGTUNE23: LPF resistor tuning. <3:2>= 00: 2061 01: 3391 10: 4721 11: 5984
32	RW	ANALOGTUNE4: BI comparator override (Vref). 0: Normal mode (bgag). 1: Override (rdiv).
33	RW	ANALOGTUNE5: Unused.
34	RW	ANALOGTUNE6: Unused. PLL input is driven by an external PIN (feedback clock), not by the PLL control latch.

Bits	PLLREG	Field Mnemonic: Description
35	RW	ANALOGTUNE7: fbclk select. 0: Internal. 1: External.
36	RW	ANALOGTUNE8: Unused. PLL input is driven by an external PIN (altref_sel), not by the PLL control latch.
37	RW	ANALOGTUNE9: Unused. PLL input is driven by an external PIN (altref_clk), not by the PLL control latch.
38	RW	ANALOGTUNE10: VCO tune. 0: 8.6 GHz maximum ring. 1: 8.8 GHz maximum ring.
39:42	RW	ATSTSEL: Selects one of 15 analog signals to be the multiplexer to the ATST output.
43	RW	VCOSEL: Selects either the slow VCO or the fast VCO. 0: lctank 1: ring
44:47	RW	BGOFFSET: Bandgap circuit adjustment setting. Bgoffset<3:0>= 0xxx: 0 mV 1000: -100 mV 1001: =-75 mV … 1111: +100 mV
48:51	RW	CCALBANDSEL: Override for VCO frequency band select when CCALLOAD is asserted.
52:54	RW	UNUSED1: Unused; keep at 0.
55	RW	CCALFMAX: Defines the fmax during calibration when in manual mode. (See CCALLOAD.)
56	RW	CCALFMIN: Defines the fmin during calibration when in manual mode. (See CCALLOAD.)
57	RW	CCALLOAD: When asserted, calibration is in manual mode. (See CCALFMAX, CCALFMIN.)
58	RW	CCALCVHOLD: Override to force differential control voltage to zero at VCO input when CCALLOAD is asserted.
59	RW	DCTEST_DC: Control signal that does not get changed in mission mode or during LBIST except for during specific tester-only periods.
60	RW	CCALMETH: Calibration method. 1: (Fmin + Fmax) / 2 0: CVHold
61	RW	UNUSED4: Controls vregbypass.
62	RW	CMLEN: Unused at LC PLL, but on filter PLL it enables the CML output PLLOUT.
63	RW	UNUSED5: Unused.

Register Name	*TFMR Time Facility Management Register*
Mnemonic	EX03.EC.PC.PC_NW.TFC.T0_TFMR
Address	0000000000000000 (SPRD) 00000000000009E8 (SPR_T0)
Attributes	
Description	

Bits	SPRD	SPR_T0	Field Mnemonic: Description
0:7	RWX	RWX	Reserved field. (Access type is max_cyc_bet_steps.)
8:9	RWX	RWX	Reserved field. (Access type is n_clks_per_step.)
10	RWX	RWX	Reserved field. (Access type is mask_hmi.)
11:13	RWX	RWX	Reserved field. (Access type is sync_bit_sel.)
14	RWX	RWX	Reserved field.

Bits	SPRD	SPR_T0	Field Mnemonic: Description
15	RWX	RWX	Reserved field. (Access type is reserved_bit15.)
16	RWX	RWX	Reserved field. (Access type is load_tod_mod.)
17	RWX	RWX	Reserved field. (Access type is reserved_bit17.)
18	RWX	RWX	Reserved field. (Access type is move_chip_tod_to_tb.)
19	RWX	RWX	Reserved field. (Access type is reserved_bit19.)
20	RWX	RWX	Reserved field. (Access type is reserved_bit20.)
21	RWX	RWX	Reserved field. (Access type is reserved_bit21.)
22	RWX	RWX	Reserved field. (Access type is reserved_bit22.)
23	RWX	RWX	Reserved field. (Access type is reserved_bit23.)
24	RWX	RWX	Reserved field. (Access type is clear_tb_errors.)
25	ROX	ROX	Reserved field. (Access type is reserved_bit25.)
26	ROX	ROX	Reserved field. (Access type is hdec_parity_error.)
27	ROX	ROX	Reserved field. (Access type is tbst_corrupt.)
28:31	ROX	ROX	Reserved field. (Access type is tbst_encoded.)
32:35	ROX	ROX	Reserved field. (Access type is tbst_last.)
36	ROX	ROX	Reserved field. (Access type is reserved_bit36.)
37	ROX	ROX	Reserved field. (Access type is reserved_bit37.)
38	ROX	ROX	Reserved field. (Access type is reserved_bit38.)
39	ROX	ROX	Reserved field. (Access type is reserved_bit39.)
40	ROX	ROX	Reserved field. (Access type is tb_enabled.)
41	ROX	ROX	Reserved field. (Access type is tb_valid.)
42	ROX	ROX	Reserved field. (Access type is tb_sync_occurred.)
43	ROX	ROX	Reserved field. (Access type is tb_missing_sync.)
44	ROX	ROX	Reserved field. (Access type is tb_missing_step.)
45	ROX	ROX	Reserved field. (Access type is tb_residue_err.)
46	ROX	ROX	Reserved field. (Access type is firmware_control_error.)
47:50	ROX	ROX	CHIP_TOD_STATUS: Chip time-of-day status.
51	ROX	ROX	Reserved field. (Access type is chip_tod_interrupt.)
52	ROX	ROX	Reserved field. (Access type is reserved_bit52.)
53	ROX	ROX	Reserved field. (Access type is reserved_bit53.)
54	ROX	ROX	Reserved field. (Access type is reserved_bit54.)
55	ROX	ROX	Reserved field. (Access type is reserved_bit55.)
56	ROX	ROX	Reserved field. (Access type is chip_tod_parity_error.)
57	ROX	ROX	Reserved field. (Access type is purr_parity_error.)
58	ROX	ROX	Reserved field. (Access type is spurr_parity_error.)
59	ROX	ROX	Reserved field. (Access type is dec_parity_error.)
60	ROX	ROX	Reserved field. (Access type is tfmr_corrupt.)
61	ROX	ROX	Reserved field. (Access type is purr_overflow_error.)
62	ROX	ROX	Reserved field. (Access type is spurr_overflow_error.)
63	ROX	ROX	Reserved field. (Access type is reserved_bit63.)

Register Name	***PLL Control Register***
Mnemonic	IOMC0.TX_WRAP.PLL_MCIO.CWRAP.PLL_CNTRL0
Address	0000000000000000 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0:2	RW	Reserved.
3	RW	BYPASSN: Bypass low active. When it is set to 0, it keeps PLL in bypass independent from ext reset or bypass. For operation mode, set this bit to 1. 1: Off 0: On
4:8	RW	SPEDIV: PCLK divider control. Applies when PCLKSEL<2:0>=X10or X11. <4:0> : freq divider
9:11	RW	CPISEL: Selects the current in the PLL charge pump based on application condition. The charge pump is determined based on the baud rate and mult.factor. <2:0>= 000: 50 ua 001: 100 ua 010: 150 ua 011: 200 ua 100: 250 ua 101: 300 ua 110: 350 ua 111: 400 ua
12:20	RW	DIVSELB: Selects the feedback divider setting 2*(2-255) or 4-510.
21:22	RW	PCLKSEL: Selects the function of pclksel. <1:0>= 00: Off 01: VCO/spediv 10: ref 11: fb
23	RW	UNUSED0: Not used; keep 0.
24:27	RO	BANDSEL: Capture the current bandsel of the PLL that is in use.
28	RW	ANALOGTUNE0: Unused. PLL input is driven by an external PIN (single-ended sel), not by the PLL control latch.
29	RW	ANALOGTUNE1: ICP tuning based on band select. 0: Enabled 1: Disabled
30:31	RW	ANALOGTUNE23: LPF resistor tuning. <3:2>= 00: 2061 01: 3391 10: 4721 11: 5984
32	RW	ANALOGTUNE4: BI comparator override (Vref). 0: Normal mode (bgag). 1: Override (rdiv).
33	RW	ANALOGTUNE5: Unused.
34	RW	ANALOGTUNE6: Unused. PLL input is driven by an external PIN (feedback clock), not by the PLL control latch.
35	RW	ANALOGTUNE7: fbclk select. 0: Internal. 1: External.
36	RW	ANALOGTUNE8: Unused. PLL input is driven by an external PIN (altref_sel), not by the PLL control latch.
37	RW	ANALOGTUNE9: Unused. PLL input is driven by an external PIN (altref_clk), not by the PLL control latch.

Bits	PLLREG	Field Mnemonic: Description
38	RW	ANALOGTUNE10: VCO tune. 0: 8.6 GHz maximum ring. 1: 8.8 GHz maximum ring.
39:42	RW	ATSTSEL: Selects one of 15 analog signals to be multiplexed to the ATST output.
43	RW	VCOSEL: Selects either the slow VCO or fast VCO. 0: lctank 1: Ring
44:47	RW	BGOFFSET: Bandgap circuit adjustment setting. Bgoffset<3:0>= 0xxx: 0 mV 1000: -100 mV 1001: =-75 mV … 1111: +100 mV
48:51	RW	CCALBANDSEL: Override for VCO frequency band select when CCALLOAD is asserted.
52:54	RW	UNUSED1: Unused; keep 0.
55	RW	CCALFMAX: Defines the fmax during calibration when in manual mode. (See CCALLOAD.)
56	RW	CCALFMIN: Defines the fmin during calibration when in manual mode. (See CCALLOAD.)
57	RW	CCALLOAD: When asserted, calibration is in manual mode. (See CCALFMAX, CCALFMIN.)
58	RW	CCALCVHOLD: Override to force differential control voltage to zero at VCO input when CCALLOAD is asserted.
59	RW	DCTEST_DC: Control signal that does not get changed in mission mode or during LBIST except for during specific tester-only periods.
60	RW	CCALMETH: Calibration method. 1: (Fmin + Fmax) / 2 0: CVHold
61	RW	UNUSED4: Controls vregbypass.
62	RW	CMLEN: Unused at LC PLL, but on filter PLL it enables the CML output PLLOUT.
63	RW	UNUSED5: Unused.

Register Name	***PLL Control Register***
Mnemonic	IOMC1.TX_WRAP.PLL_MCIO.CWRAP.PLL_CNTRL0
Address	0000000000000000 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0:2	RW	
3	RW	BYPASSN: Bypass low active. When it is set to 0, it keeps PLL in bypass independent from ext reset or bypass. For operation mode, set this bit to 1. 1: Off 0: On
4:8	RW	SPEDIV: PCLK divider control. Applies when PCLKSEL<2:0> = X10 or X11. <4:0> : freq divider

Bits	PLLREG	Field Mnemonic: Description
9:11	RW	CPISEL: Selects the current in the PLL charge pump based on application condition. The charge pump is determined based on the baud rate and mult.factor. <2:0>= 000: 50 ua 001: 100 ua 010: 150 ua 011: 200 ua 100: 250 ua 101: 300 ua 110: 350 ua 111: 400 ua
12:20	RW	DIVSELB: Selects the feedback divider setting 2*(2-255) or 4-510.
21:22	RW	PCLKSEL: Selects the function of pclksel. <1:0>= 00: Off 01: VCO/spediv 10: ref 11: fb
23	RW	UNUSED0: Not used; keep 0.
24:27	RO	BANDSEL: Capture the current bandsel of the PLL that is in use.
28	RW	ANALOGTUNE0: Unused. PLL input is driven by an external PIN (single-ended sel), not by the PLL control latch.
29	RW	ANALOGTUNE1: ICP tuning based on band select. 0: Enabled. 1: Disabled.
30:31	RW	ANALOGTUNE23: LPF resistor tuning. <3:2>= 00: 2061 01: 3391 10: 4721 11: 5984
32	RW	ANALOGTUNE4: BI comparator override (Vref). 0: Normal mode (bgag). 1: Override (rdiv).
33	RW	ANALOGTUNE5: Unused.
34	RW	ANALOGTUNE6: Unused. PLL input is driven by an external PIN (feedback clock), not by the PLL control latch.
35	RW	ANALOGTUNE7: fbclk select. 0: Internal. 1: External.
36	RW	ANALOGTUNE8: Unused. PLL input is driven by an external PIN (altref_sel), not by the PLL control latch.
37	RW	ANALOGTUNE9: Unused. PLL input is driven by an external PIN (altref_clk), not by the PLL control latch.
38	RW	ANALOGTUNE10: VCO tune. 0: 8.6 GHz maximum ring. 1: 8.8 GHz maximum ring.
39:42	RW	ATSTSEL: Selects one of 15 analog signals to be multiplexed to the ATST output.
43	RW	VCOSEL: Selects either the slow VCO or the fast VCO. 0: lctank 1: Ring
44:47	RW	BGOFFSET: Bandgap circuit adjustment setting. Bgoffset<3:0>= 0xxx: 0 mV 1000: -100 mV 1001: =-75 mV … 1111: +100 mV
48:51	RW	CCALBANDSEL: Override for VCO frequency band select when CCALLOAD is asserted.
52:54	RW	UNUSED1: Unused; keep 0.

Bits	PLLREG	Field Mnemonic: Description
55	RW	CCALFMAX: Defines the fmax during calibration when in manual mode. (See CCALLOAD.)
56	RW	CCALFMIN: Defines the fmin during calibration when in manual mode. (See CCALLOAD.)
57	RW	CCALLOAD: When asserted, calibration is in manual mode. (See CCALFMAX, CCALFMIN.)
58	RW	CCALCVHOLD: Override to force differential control voltage to zero at VCO input when CCALLOAD is asserted.
59	RW	DCTEST_DC: Control signal that does not get changed in mission mode or during LBIST except for during specific tester-only periods.
60	RW	CCALMETH: Calibration method. 1: (Fmin + Fmax) / 2 0: CVHold
61	RW	UNUSED4: Controls vregbypass.
62	RW	CMLEN: Unused at LC PLL, but on filter PLL it enables the CML output PLLOUT.
63	RW	UNUSED5: Unused.

Register Name	*GP Register 0*
Mnemonic	EH.TPCHIP.TPC.GP0
Address	0000000001000000 (PCB) 0000000001000004 (PCB1) 0000000001000005 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	NOT_USED0: Not used. Reset(0b0).
1	RWX	WOX_AND	WOX_OR	TC_SYNCCLK_MUXSEL_DC: For LPC. Reset(0b1).
2	RWX	WOX_AND	WOX_OR	TC_GPIO_FLUSHMODE_INH_DC: Prevent plats from going into flush mode (init value 1). Reset(0b1).
3	RWX	WOX_AND	WOX_OR	TC_GPIO_FORCEALIGN: Force align signal to be sent (init value 1, drop before dropping flushmode_inh). Reset(0b1).
4	RWX	WOX_AND	WOX_OR	NOT_USED1: Not used. Reset(0b0).
5	RWX	WOX_AND	WOX_OR	NOT_USED2: Not used. Reset(0b0).
6	RWX	WOX_AND	WOX_OR	TC_SCAN_DIS_DC_B: Disable scan. Set output of scan chain to zero. Reset(0b0).
7	RWX	WOX_AND	WOX_OR	NOT_USED3: Not used. Reset(0b0).
8	RWX	WOX_AND	WOX_OR	TC_LBIST_EN_DC: LBIST mode. Reset(0b0).
9	RWX	WOX_AND	WOX_OR	TC_LBIST_AC_MODE_DC: LBIST AC mode. Reset(0b0).
10	RWX	WOX_AND	WOX_OR	TC_LBIST_ARY_WRT_THRU_DC: Array write-through mode. Set array in bypass mode. Reset(0b0).
11	RWX	WOX_AND	WOX_OR	TC_ABIST_MODE_DC: Set during ABIST. Reset(0b0).
12	RWX	WOX_AND	WOX_OR	TC_ABIST_START_TEST_DC: Set to start ABIST testing. Reset(0b0).
13	RWX	WOX_AND	WOX_OR	NOT_USED4: Not used. Reset(0b0).
14	RWX	WOX_AND	WOX_OR	TC_ATPG_EN_DC: ATPG mode. Reset(0b0).
15	RWX	WOX_AND	WOX_OR	TC_SCAN_PROTECT_DC: Scan protection enable (initial value 1). Reset(0b1).
16	RWX	WOX_AND	WOX_OR	NOT_USED5: Not used. Reset(0b1).
17	RWX	WOX_AND	WOX_OR	NOT_USED6: Not used. Reset(0b0).

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
18	RWX	WOX_AND	WOX_OR	NOT_USED7: Not used. Reset(0b0).
19	RWX	WOX_AND	WOX_OR	TCPERV_OCC_PIB_FENCE_DC: OCC fence for partial good/independent scanning. Reset(0b1).
20	RWX	WOX_AND	WOX_OR	TC_DBG_TRACE_START: Start trace to debug macros. Reset(0b0).
21	RWX	WOX_AND	WOX_OR	TC_DBG_TRACE_STOP: Stop trace to debug macros. Reset(0b0).
22	RWX	WOX_AND	WOX_OR	TC_DBG_TRACE_RESET: Reset trace to debug macros. Reset(0b0).
23	RWX	WOX_AND	WOX_OR	TC_PIB_TRACE_MODE_DATA_DC: Enable data trace mode of PIB. Reset(0b0).
24:25	RWX	WOX_AND	WOX_OR	TC_GPIO_CLKDIV_SEL_DC: Select clock divider ratio for probing. Reset(0b0).
26	RWX	WOX_AND	WOX_OR	NOT_USED8: Not used. Reset(0b0).
27	RWX	WOX_AND	WOX_OR	NOT_USED9: Not used: 0b0. Reset(0b0).
28:31	RWX	WOX_AND	WOX_OR	TC_DBG_MUXSEL_DC: Nest debug bus selects(0:3). Reset(0b0).
32:39	RWX	WOX_AND	WOX_OR	TC_MHCRO_SEL_DC: PSRO selects(0:7). Reset(0b0).
40:42	RWX	WOX_AND	WOX_OR	TC_NODE_ID_DC: Node ID. Reset(0b0).
43:45	RWX	WOX_AND	WOX_OR	TC_CHIP_ID_DC: Chip ID. Reset(0b0).
46	RWX	WOX_AND	WOX_OR	NOT_USED10: Not used. Reset(0b0).
47	RWX	WOX_AND	WOX_OR	NOT_USED11: Not used. Reset(0b0).
48	RWX	WOX_AND	WOX_OR	TC_BSC_INV_DC: I/O Valid. Reset(0b0)
49	RWX	WOX_AND	WOX_OR	TC_BSC_EXTMODE_DC: I/O Valid. Reset(0b0).
50	RWX	WOX_AND	WOX_OR	NOT_USED12: Not used. Reset(0b0).
51	RWX	WOX_AND	WOX_OR	NOT_USED13: Not used. Reset(0b0).
52	RWX	WOX_AND	WOX_OR	NOT_USED14: Not used. Reset(0b0).
53	RWX	WOX_AND	WOX_OR	NOT_USED15: Not used. Reset(0b0).
54	RWX	WOX_AND	WOX_OR	NOT_USED16: Not used. Reset(0b0).
55	RWX	WOX_AND	WOX_OR	NOT_USED17: Not used. Reset(0b0).
56	RWX	WOX_AND	WOX_OR	NOT_USED18: Not used. Reset(0b0).
57	RWX	WOX_AND	WOX_OR	NOT_USED19: Not used. Reset(0b0).
58	RWX	WOX_AND	WOX_OR	NOT_USED20: Not used. Reset(0b0).
59	RWX	WOX_AND	WOX_OR	TC_EXPORT_FREEZE_DC: Workaround for DD1 only. Bypass fuse autoread (export restriction fuse). Reset(0b0).
60	RWX	WOX_AND	WOX_OR	TC_MASK_CC_PCB_ERR_DC: Mask for PCB error (access or parity) in CC. Reset(0b0).
61	RWX	WOX_AND	WOX_OR	TC_MASK_CC_SCAN_OPCG_ERR_DC: Mask for PCB write while OPCG_IP / scan collision in CC. Reset(0b0).
62	RWX	WOX_AND	WOX_OR	NOT_USED21: Not used. Reset(0b1).
63	RWX	WOX_AND	WOX_OR	TC_FENCE_PERV_DC: Fence pervasive logic during scan (initial value 1). Reset(0b1).

Register Name	*GP Register 0*
Mnemonic	EH.TPC.GP0
Address	0000000002000000 (PCB) 0000000002000004 (PCB1) 0000000002000005 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	TC_ABSTCLK_MUXSEL_DC: Select ABIST clock source for arrays on a chiplet boundary. When set to 1, clocks were used from the chiplet with ABIST. Reset(0b0).
1	RWX	WOX_AND	WOX_OR	TC_SYNCCLK_MUXSEL_DC: syncclk multiplexer for MC. Reset(0b1).
2	RWX	WOX_AND	WOX_OR	TC_GPIO_FLUSHMODE_INH_DC: Prevent plats from going into flush mode (initial value 1). Reset(0b1).
3	RWX	WOX_AND	WOX_OR	TC_GPIO_FORCEALIGN: Force align signal to be sent (initial value 1, drop before dropping flushmode_inh). Reset(0b1).
4	RWX	WOX_AND	WOX_OR	NOT_USED0: Not used. Reset(0b0).
5	RWX	WOX_AND	WOX_OR	NOT_USED1: Not used. Reset(0b0).
6	RWX	WOX_AND	WOX_OR	TC_SCAN_DIS_DC_B: Disable scan. Set output of scan chain to zero. Reset(0b0).
7	RWX	WOX_AND	WOX_OR	TC_SKIT_MODE_BIST_DC: Enable skitter measuring during BIST. Reset(0b0).
8	RWX	WOX_AND	WOX_OR	TC_LBIST_EN_DC: LBIST mode. Reset(0b0).
9	RWX	WOX_AND	WOX_OR	TC_LBIST_AC_MODE_DC: LBIST AC mode. Reset(0b0).
10	RWX	WOX_AND	WOX_OR	TC_LBIST_ARY_WRT_THRU_DC: Array write-through mode. Set array in bypass mode. Reset(0b0).
11	RWX	WOX_AND	WOX_OR	TC_ABIST_MODE_DC: Set during ABIST. Reset(0b0).
12	RWX	WOX_AND	WOX_OR	TC_ABIST_START_TEST_DC: Set to start ABIST testing. Reset(0b0).
13	RWX	WOX_AND	WOX_OR	NOT_USED2: Not used. Reset(0b0).
14	RWX	WOX_AND	WOX_OR	TC_ATPG_EN_DC: ATPG mode. Reset(0b0).
15	RWX	WOX_AND	WOX_OR	TC_SCAN_PROTECT_DC: Scan protection enable (initial value 1). Reset(0b1).
16	RWX	WOX_AND	WOX_OR	NOT_USED3: Not used. Reset(0b1).
17	RWX	WOX_AND	WOX_OR	NOT_USED4: Not used. Reset(0b0).
18	RWX	WOX_AND	WOX_OR	NOT_USED5: Not used. Reset(0b0).
19	RWX	WOX_AND	WOX_OR	NOT_USED6: Not used. Reset(0b1).
20	RWX	WOX_AND	WOX_OR	TC_DBG_TRACE_START: Start trace to debug macros. Reset(0b0).
21	RWX	WOX_AND	WOX_OR	TC_DBG_TRACE_STOP: Stop trace to debug macros. Reset(0b0).
22	RWX	WOX_AND	WOX_OR	TC_DBG_TRACE_RESET: Reset trace to debug macros. Reset(0b0).
23	RWX	WOX_AND	WOX_OR	NOT_USED7: Not used. Reset(0b0).
24:25	RWX	WOX_AND	WOX_OR	TC_GPIO_CLKDIV_SEL_DC: Select clock divider ratio for probing. Reset(0b0).
26	RWX	WOX_AND	WOX_OR	NOT_USED8: Not used. Reset(0b0).
27	RWX	WOX_AND	WOX_OR	TC_IOBIST_TX_WRAP_ENABLE_DC: 0. Reset(0b0).
28:31	RWX	WOX_AND	WOX_OR	TC_DBG_MUXSEL_DC: Nest debug bus selects(0:3). Reset(0b0).
32:39	RWX	WOX_AND	WOX_OR	TC_PSRO_SEL_DC: PSRO selects(0:7). Reset(0b0).

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
40:42	RWX	WOX_AND	WOX_OR	TC_NODE_ID_DC: Node ID. Reset(0b0).
43:45	RWX	WOX_AND	WOX_OR	TC_CHIP_ID_DC: Chip ID. Reset(0b0).
46	RWX	WOX_AND	WOX_OR	TC_BSC_WRAPSEL_DC: for MC. Reset(0b0).
47	RWX	WOX_AND	WOX_OR	TC_BSC_INTMODE_DC: for MC. Reset(0b0).
48	RWX	WOX_AND	WOX_OR	NOT_USED9: Not used. Reset(0b0).
49	RWX	WOX_AND	WOX_OR	NOT_USED10: Not used. Reset(0b0).
50	RWX	WOX_AND	WOX_OR	TC_PSI_IOVALID_DC: I/O valid for PSI. Reset(0b0).
51	RWX	WOX_AND	WOX_OR	TP_MCL_FENCE_B_DC: Partial good fence for MCL (POWER8 only). Reset(0b0).
52	RWX	WOX_AND	WOX_OR	TP_MCR_FENCE_B_DC: Partial good fence for MCR. Reset(0b0).
53	RWX	WOX_AND	WOX_OR	TP_NX_FENCE_B_DC: Partial good fence for NX. Reset(0b0).
54	RWX	WOX_AND	WOX_OR	NOT_USED11: Not used. Reset(0b0).
55	RWX	WOX_AND	WOX_OR	NOT_USED12: Not used. Reset(0b0).
56	RWX	WOX_AND	WOX_OR	NOT_USED13: Not used. Reset(0b0).
57	RWX	WOX_AND	WOX_OR	NOT_USED14: Not used. Reset(0b0).
58	RWX	WOX_AND	WOX_OR	NOT_USED15: Not used. Reset(0b0).
59	RWX	WOX_AND	WOX_OR	NOT_USED16: Not used. Reset(0b0).
60	RWX	WOX_AND	WOX_OR	TC_MASK_CC_PCB_ERR_DC: Mask for PCB error (access or parity) in CC. Reset(0b0).
61	RWX	WOX_AND	WOX_OR	TC_MASK_CC_SCAN_OPCG_ERR_DC: Mask for PCB write while OPCG_IP / scan collision in CC. Reset(0b0).
62	RWX	WOX_AND	WOX_OR	NOT_USED17: Not used. Reset(0b1).
63	RWX	WOX_AND	WOX_OR	TC_FENCE_PERV_DC: Fence pervasive logic during scan (initial value 1). Reset(0b1).

Register Name	*GP Register 0*
Mnemonic	EN.PB.TPC.GP0
Address	0000000004000000 (PCB) 0000000004000004 (PCB1) 0000000004000005 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	NOT_USED0: Not used. Reset(0b0).
1	RWX	WOX_AND	WOX_OR	TC_SYNCCLK_MUXSEL_DC: syncclk multiplexer for X+PSI. Reset(0b1).
2	RWX	WOX_AND	WOX_OR	TC_GPIO_FLUSHMODE_INH_DC: Prevent plats from going into flush mode (initial value 1). Reset(0b1).
3	RWX	WOX_AND	WOX_OR	TC_GPIO_FORCEALIGN: Force align signal to be sent (initial value 1, drop before dropping flushmode_inh). Reset(0b1).
4	RWX	WOX_AND	WOX_OR	NOT_USED1: Not used. Reset(0b0).
5	RWX	WOX_AND	WOX_OR	NOT_USED2: Not used. Reset(0b0).
6	RWX	WOX_AND	WOX_OR	TC_SCAN_DIS_DC_B: Disable scan. Set output of scan chain to zero. Reset(0b0).

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
7	RWX	WOX_AND	WOX_OR	TC_SKIT_MODE_BIST_DC: Enable skitter measuring during BIST. Reset(0b0).
8	RWX	WOX_AND	WOX_OR	TC_LBIST_EN_DC: LBIST mode. Reset(0b0).
9	RWX	WOX_AND	WOX_OR	TC_LBIST_AC_MODE_DC: LBIST AC mode. Reset(0b0).
10	RWX	WOX_AND	WOX_OR	TC_LBIST_ARY_WRT_THRU_DC: Array write-through mode. Set array in bypass mode. Reset(0b0).
11	RWX	WOX_AND	WOX_OR	TC_ABIST_MODE_DC: Set during ABIST. Reset(0b0).
12	RWX	WOX_AND	WOX_OR	TC_ABIST_START_TEST_DC: Set to start ABIST testing. Reset(0b0).
13	RWX	WOX_AND	WOX_OR	NOT_USED3: Not used. Reset(0b0).
14	RWX	WOX_AND	WOX_OR	TC_ATPG_EN_DC: ATPG mode. Reset(0b0).
15	RWX	WOX_AND	WOX_OR	TC_SCAN_PROTECT_DC: Scan protection enable (initial value 1). Reset(0b1).
16	RWX	WOX_AND	WOX_OR	NOT_USED4: Not used. Reset(0b1).
17	RWX	WOX_AND	WOX_OR	NOT_USED5: Not used. Reset(0b0).
18	RWX	WOX_AND	WOX_OR	NOT_USED6: Not used. Reset(0b0).
19	RWX	WOX_AND	WOX_OR	NOT_USED7: Not used. Reset(0b1).
20	RWX	WOX_AND	WOX_OR	TC_DBG_TRACE_START: Start trace to debug macros. Reset(0b0).
21	RWX	WOX_AND	WOX_OR	TC_DBG_TRACE_STOP: Stop trace to debug macros. Reset(0b0).
22	RWX	WOX_AND	WOX_OR	TC_DBG_TRACE_RESET: Reset trace to debug macros. Reset(0b0).
23	RWX	WOX_AND	WOX_OR	NOT_USED8: Not used. Reset(0b0).
24:25	RWX	WOX_AND	WOX_OR	TC_GPIO_CLKDIV_SEL_DC: Select clock divider ratio for probing. Reset(0b0).
26	RWX	WOX_AND	WOX_OR	NOT_USED9: Not used. Reset(0b0).
27	RWX	WOX_AND	WOX_OR	TC_IOBIST_TX_WRAP_ENABLE_DC: 0. Reset(0b0).
28:31	RWX	WOX_AND	WOX_OR	TC_DBG_MUXSEL_DC: Nest debug bus selects(0:3). Reset(0b0).
32:39	RWX	WOX_AND	WOX_OR	TC_PSRO_SEL_DC: PSRO selects(0:7). Reset(0b0).
40:42	RWX	WOX_AND	WOX_OR	TC_NODE_ID_DC: Node ID. Reset(0b0).
43:45	RWX	WOX_AND	WOX_OR	TC_CHIP_ID_DC: Chip ID. Reset(0b0).
46	RWX	WOX_AND	WOX_OR	TC_BSC_WRAPSEL_DC: For X+PSI. Reset(0b0).
47	RWX	WOX_AND	WOX_OR	TC_BSC_INTMODE_DC: For X+PSI. Reset(0b0).
48	RWX	WOX_AND	WOX_OR	TC_X0_IOVALID_DC: I/O valid for X0. Reset(0b0).
49	RWX	WOX_AND	WOX_OR	TC_X1_IOVALID_DC: I/O valid for X1. Reset(0b0).
50	RWX	WOX_AND	WOX_OR	TC_X2_IOVALID_DC: I/O valid for X2. Reset(0b0).
51	RWX	WOX_AND	WOX_OR	TC_X3_IOVALID_DC: I/O valid for X3. Reset(0b0).
52	RWX	WOX_AND	WOX_OR	NOT_USED10: Not used. Reset(0b0).
53	RWX	WOX_AND	WOX_OR	NOT_USED11: Not used. Reset(0b0).
54	RWX	WOX_AND	WOX_OR	NOT_USED12: Not used. Reset(0b0).
55	RWX	WOX_AND	WOX_OR	NOT_USED13: Not used. Reset(0b0).
56	RWX	WOX_AND	WOX_OR	NOT_USED14: Not used. Reset(0b0).
57	RWX	WOX_AND	WOX_OR	NOT_USED15: Not used. Reset(0b0).
58	RWX	WOX_AND	WOX_OR	NOT_USED16: Not used. Reset(0b0).
59	RWX	WOX_AND	WOX_OR	NOT_USED17: Not used. Reset(0b0).

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
60	RWX	WOX_AND	WOX_OR	TC_MASK_CC_PCB_ERR_DC: Mask for PCB error (access or parity) in CC. Reset(0b0).
61	RWX	WOX_AND	WOX_OR	TC_MASK_CC_SCAN_OPCG_ERR_DC: Mask for PCB write while OPCG_IP / scan collision in CC. Reset(0b0).
62	RWX	WOX_AND	WOX_OR	TC_CC_LCC_EDGE_DELAYED_DC: Offset the clocking in the f domain by one cycle. Reset(0b1).
63	RWX	WOX_AND	WOX_OR	TC_FENCE_PERV_DC: Fence pervasive logic during scan (initial value 1). Reset(0b1).

Register Name	*PLL Control Register*
Mnemonic	ABUS.TX_WRAP.PLL_A.CWRAP.PLL_CNTRL1
Address	0000000000000001 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0	RW	CALREQ: Manual start of calibration on the falling edge. Combined with the reset signal.
1	RW	CALRECAL: Start recalibration without reset.
2:5	RW	RDIV: Refclk Divider
6:7	RW	UNUSED2: Unused.
8	RO	CCALCOMP: OBSERVE: Calibration complete.
9	RO	CCALERR: OBSERVE: Calibration error.
10:11	RW	SEL: EXTERNAL: Select bits for the driver. The default setting is <00>.
12	RW	EN: EXTERNAL: Enable bit for the driver.
13:15	RW	VSEL: EXTERNAL: Select for analog-multiplexer-to-multiplexer ATST signals.
16:62	RO	Reserved field. (Access type is unused.)
63	RW	PLLOUTA_DISABLE: Disable PLL output. Keep 0 in operation mode.

Register Name	*TFMR Time Facility Management Register*
Mnemonic	EX03.EC.PC.PC_NW.TFC.T1_TFMR
Address	0000000000000001 (SPRD) 00000000000009E9 (SPR_T1)
Attributes	
Description	

Bits	SPRD	SPR_T1	Field Mnemonic: Description
0:7	RWX	RWX	Reserved field. (Access type is max_cyc_bet_steps.)
8:9	RWX	RWX	Reserved field. (Access type is n_clks_per_step.)
10	RWX	RWX	Reserved field. (Access type is mask_hmi.)
11:13	RWX	RWX	Reserved field. (Access type is sync_bit_sel.)
14	RWX	RWX	Reserved field.
15	RWX	RWX	Reserved field. (Access type is reserved_bit15.)
16	RWX	RWX	Reserved field. (Access type is load_tod_mod.)
17	RWX	RWX	Reserved field. (Access type is reserved_bit17.)

Bits	SPRD	SPR_T1	Field Mnemonic: Description
18	RWX	RWX	Reserved field. (Access type is move_chip_tod_to_tb.)
19	RWX	RWX	Reserved field. (Access type is reserved_bit19.)
20	RWX	RWX	Reserved field. (Access type is reserved_bit20.)
21	RWX	RWX	Reserved field. (Access type is reserved_bit21.)
22	RWX	RWX	Reserved field. (Access type is reserved_bit22.)
23	RWX	RWX	Reserved field. (Access type is reserved_bit23.)
24	RWX	RWX	Reserved field. (Access type is clear_tb_errors.)
25	ROX	ROX	Reserved field. (Access type is reserved_bit25.)
26	ROX	ROX	Reserved field. (Access type is hdec_parity_error.)
27	ROX	ROX	Reserved field. (Access type is tbst_corrupt.)
28:31	ROX	ROX	Reserved field. (Access type is tbst_encoded.)
32:35	ROX	ROX	Reserved field. (Access type is tod_cmd_last.)
36	ROX	ROX	Reserved field. (Access type is reserved_bit36.)
37	ROX	ROX	Reserved field. (Access type is reserved_bit37.)
38	ROX	ROX	Reserved field. (Access type is reserved_bit38.)
39	ROX	ROX	Reserved field. (Access type is reserved_bit39.)
40	ROX	ROX	Reserved field. (Access type is tb_enabled.)
41	ROX	ROX	Reserved field. (Access type is tb_valid.)
42	ROX	ROX	Reserved field. (Access type is tb_sync_occurred.)
43	ROX	ROX	Reserved field. (Access type is tb_missing_sync.)
44	ROX	ROX	Reserved field. (Access type is tb_missing_step.)
45	ROX	ROX	Reserved field. (Access type is tb_residue_err.)
46	ROX	ROX	Reserved field. (Access type is firmware_control_error.)
47:50	ROX	ROX	CHIP_TOD_STATUS: Chip time-of-day status..
51	ROX	ROX	Reserved field. (Access type is chip_tod_interrupt.)
52	ROX	ROX	Reserved field. (Access type is reserved_bit52.)
53	ROX	ROX	Reserved field. (Access type is reserved_bit53.)
54	ROX	ROX	Reserved field. (Access type is reserved_bit54.)
55	ROX	ROX	Reserved field. (Access type is reserved_bit55.)
56	ROX	ROX	Reserved field. (Access type is chip_tod_parity_error.)
57	ROX	ROX	Reserved field. (Access type is purr_parity_error.)
58	ROX	ROX	Reserved field. (Access type is spurr_parity_error.)
59	ROX	ROX	Reserved field. (Access type is dec_parity_error.)
60	ROX	ROX	Reserved field. (Access type is tfmr_corrupt.)
61	ROX	ROX	Reserved field. (Access type is purr_overflow_error.)
62	ROX	ROX	Reserved field. (Access type is spurr_overflow_error.)
63	ROX	ROX	Reserved field. (Access type is reserved_bit63.)

Register Name	*PLL Control Register*
Mnemonic	IOMC0.TX_WRAP.PLL_MCIO.CWRAP.PLL_CNTRL1
Address	0000000000000001 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0	RW	CALREQ: Manual start of calibration on the falling edge. Combined with the reset signal.
1	RW	CALRECAL: Start recalibration without reset.
2:5	RW	RDIV: Refclk Divider.
6:7	RW	UNUSED2: Unused.
8	RO	CCALCOMP: OBSERVE: Calibration complete.
9	RO	CCALERR: OBSERVE: Calibration error.
10:11	RW	SEL: EXTERNAL: Select bits for the driver. The default setting is <00>.
12	RW	EN: EXTERNAL: Enable bit for the driver.
13:15	RW	VSEL: EXTERNAL: Select for analog-multiplexer-to-multiplexer ATST signals.
16:62	RO	Reserved field. (Access type is unused.)
63	RW	PLLOUTA_DISABLE: Disable PLL output. Keep 0 in operation mode.

Register Name	*PLL Control Register*
Mnemonic	IOMC1.TX_WRAP.PLL_MCIO.CWRAP.PLL_CNTRL1
Address	0000000000000001 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0	RW	CALREQ: Manual start of calibration on the falling edge. Combined with the reset signal.
1	RW	CALRECAL: Start recalibration without reset.
2:5	RW	RDIV: Refclk Divider.
6:7	RW	UNUSED2: Unused.
8	RO	CCALCOMP: OBSERVE: Calibration complete.
9	RO	CCALERR: OBSERVE: Calibration error.
10:11	RW	SEL: EXTERNAL: Select bits for the driver. The default setting is <00>.
12	RW	EN: EXTERNAL: Enable bit for the driver.
13:15	RW	VSEL: EXTERNAL: Select for analog-multiplexer-to-multiplexer ATST signals.
16:62	RO	Reserved field. (Access type is unused.)
63	RW	PLLOUTA_DISABLE: Disable PLL output. Keep 0 in operation mode.

Register Name	*PLL Control Register*
Mnemonic	ABUS.TX_WRAP.PLL_A.CWRAP.PLL_CNTRL2
Address	0000000000000002 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0	RO	UNUSED_OUTB_DISABLE: Unused: Disable for output b.
1:3	RO	UNUSED: Unused.
4	RW	RESET: Reset for Tank and Filt PLL. Keep 0 during operation mode.
5:7	RO	SPARE: Not used. Spare.

Register Name	***TFMR Time Facility Management Register***
Mnemonic	EX03.EC.PC.PC_NW.TFC.T2_TFMR
Address	0000000000000002 (SPRD) 00000000000009EA (SPR_T2)
Attributes	
Description	

Bits	SPRD	SPR_T2	Field Mnemonic: Description
0:7	RWX	RWX	Reserved field. (Access type is max_cyc_bet_steps.)
8:9	RWX	RWX	Reserved field. (Access type is n_clks_per_step.)
10	RWX	RWX	Reserved field. (Access type is mask_hmi.)
11:13	RWX	RWX	Reserved field. (Access type is sync_bit_sel.)
14	RWX	RWX	Reserved field.
15	RWX	RWX	Reserved field. (Access type is reserved_bit15.)
16	RWX	RWX	Reserved field. (Access type is load_tod_mod.)
17	RWX	RWX	Reserved field. (Access type is reserved_bit17.)
18	RWX	RWX	Reserved field. (Access type is move_chip_tod_to_tb.)
19	RWX	RWX	Reserved field. (Access type is reserved_bit19.)
20	RWX	RWX	Reserved field. (Access type is reserved_bit20.)
21	RWX	RWX	Reserved field. (Access type is reserved_bit21.)
22	RWX	RWX	Reserved field. (Access type is reserved_bit22.)
23	RWX	RWX	Reserved field. (Access type is reserved_bit23.)
24	RWX	RWX	Reserved field. (Access type is clear_tb_errors.)
25	ROX	ROX	Reserved field. (Access type is reserved_bit25.)
26	ROX	ROX	Reserved field. (Access type is hdec_parity_error.)
27	ROX	ROX	Reserved field. (Access type is tbst_corrupt.)
28:31	ROX	ROX	Reserved field. (Access type is tbst_encoded.)
32:35	ROX	ROX	Reserved field. (Access type is tbst_last.)
36	ROX	ROX	Reserved field. (Access type is reserved_bit36.)
37	ROX	ROX	Reserved field. (Access type is reserved_bit37.)
38	ROX	ROX	Reserved field. (Access type is reserved_bit38.)
39	ROX	ROX	Reserved field. (Access type is reserved_bit39.)
40	ROX	ROX	Reserved field. (Access type is tb_enabled.)
41	ROX	ROX	Reserved field. (Access type is tb_valid.)
42	ROX	ROX	Reserved field. (Access type is tb_sync_occurred.)
43	ROX	ROX	Reserved field. (Access type is tb_missing_sync.)
44	ROX	ROX	Reserved field. (Access type is tb_missing_step.)

Bits	SPRD	SPR_T2	Field Mnemonic: Description
45	ROX	ROX	Reserved field. (Access type is tb_residue_err.)
46	ROX	ROX	Reserved field. (Access type is firmware_control_error.)
47:50	ROX	ROX	CHIP_TOD_STATUS: Chip time-of-day status..
51	ROX	ROX	Reserved field. (Access type is chip_tod_interrupt.)
52	ROX	ROX	Reserved field. (Access type is reserved_bit52.)
53	ROX	ROX	Reserved field. (Access type is reserved_bit53.)
54	ROX	ROX	Reserved field. (Access type is reserved_bit54.)
55	ROX	ROX	Reserved field. (Access type is reserved_bit55.)
56	ROX	ROX	Reserved field. (Access type is chip_tod_parity_error.)
57	ROX	ROX	Reserved field. (Access type is purr_parity_error.)
58	ROX	ROX	Reserved field. (Access type is spurr_parity_error.)
59	ROX	ROX	Reserved field. (Access type is dec_parity_error.)
60	ROX	ROX	Reserved field. (Access type is tfmr_corrupt.)
61	ROX	ROX	Reserved field. (Access type is purr_overflow_error.)
62	ROX	ROX	Reserved field. (Access type is spurr_overflow_error.)
63	ROX	ROX	Reserved field. (Access type is reserved_bit63.)

Register Name	***PLL Control Register***
Mnemonic	IOMC0.TX_WRAP.PLL_MCIO.CWRAP.PLL_CNTRL2
Address	0000000000000002 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0	RO	UNUSED_OUTB_DISABLE: Unused: Disable for output b.
1:3	RO	UNUSED: Unused.
4	RW	RESET: Reset for Tank and Filt PLL. Keep 0 during operation mode.
5:7	RO	SPARE: Not used. Spare.

Register Name	***PLL Control Register***
Mnemonic	IOMC1.TX_WRAP.PLL_MCIO.CWRAP.PLL_CNTRL2
Address	0000000000000002 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0	RO	UNUSED_OUTB_DISABLE: Unused: Disable for output b.
1:3	RO	UNUSED: Unused.
4	RW	RESET: Reset for Tank and Filt PLL. Keep 0 during operation mode.
5:7	RO	SPARE: Not used. Spare.

Register Name	*PLL Control Register NSL*
Mnemonic	ABUS.TX_WRAP.PLL_A.CWRAP.PLL_CNTRL_SETUP0
Address	0000000000000003 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0:2	RW	
3	RW	SHADOW_BYPASSN: Bypass low active. When it is set to 0, it keeps PLL in bypass independent from ext reset or bypass. For operation mode, set this bit to 1. 1: Off 0: On
4:8	RW	SHADOW_SPEDIV: Testout Divide Selector
9:11	RW	SHADOW_CPISEL:
12:20	RW	SHADOW_DIVSELB:
21:22	RW	SHADOW_PCLKSEL:
23	RW	SHADOW_UNUSED0:
24:27	RO	SHADOW_BANDSEL:
28:38	RW	SHADOW_ANALOGTUNE:
39:42	RW	SHADOW_ATSTSEL:
43	RW	SHADOW_VCOSEL:
44:47	RW	SHADOW_BGOFFSET:
48:51	RW	SHADOW_CCALBANDSEL:
52:54	RW	SHADOW_UNUSED1:
55	RW	SHADOW_CCALFMAX:
56	RW	SHADOW_CCALFMIN:
57	RW	SHADOW_CCALLOAD:
58	RW	SHADOW_CCALCVHOLD:
59	RW	Reserved field. (Access type is SHADOW_unused.)
60	RW	SHADOW_CCALMETH:
61	RW	SHADOW_UNUSED4: Controls vregbypass.
62	RW	SHADOW_CMLEN:
63	RW	SHADOW_UNUSED5:

Register Name	*TFMR Time Facility Management Register*
Mnemonic	EX03.EC.PC.PC_NW.TFC.T3_TFMR
Address	0000000000000003 (SPRD) 00000000000009EB (SPR_T3)
Attributes	
Description	

Bits	SPRD	SPR_T3	Field Mnemonic: Description
0:7	RWX	RWX	Reserved field. (Access type is max_cyc_bet_steps.)
8:9	RWX	RWX	Reserved field. (Access type is n_clks_per_step.)
10	RWX	RWX	Reserved field. (Access type is mask_hmi.)

Bits	SPRD	SPR_T3	Field Mnemonic: Description
11:13	RWX	RWX	Reserved field. (Access type is sync_bit_sel.)
14	RWX	RWX	Reserved field.
15	RWX	RWX	Reserved field. (Access type is reserved_bit15.)
16	RWX	RWX	Reserved field. (Access type is load_tod_mod.)
17	RWX	RWX	Reserved field. (Access type is reserved_bit17.)
18	RWX	RWX	Reserved field. (Access type is move_chip_tod_to_tb.)
19	RWX	RWX	Reserved field. (Access type is reserved_bit19.)
20	RWX	RWX	Reserved field. (Access type is reserved_bit20.)
21	RWX	RWX	Reserved field. (Access type is reserved_bit21.)
22	RWX	RWX	Reserved field. (Access type is reserved_bit22.)
23	RWX	RWX	Reserved field. (Access type is reserved_bit23.)
24	RWX	RWX	Reserved field. (Access type is clear_tb_errors.)
25	ROX	ROX	Reserved field. (Access type is reserved_bit25.)
26	ROX	ROX	Reserved field. (Access type is hdec_parity_error.)
27	ROX	ROX	Reserved field. (Access type is tbst_corrupt.)
28:31	ROX	ROX	Reserved field. (Access type is tbst_encoded.)
32:35	ROX	ROX	Reserved field. (Access type is tbst_last.)
36	ROX	ROX	Reserved field. (Access type is reserved_bit36.)
37	ROX	ROX	Reserved field. (Access type is reserved_bit37.)
38	ROX	ROX	Reserved field. (Access type is reserved_bit38.)
39	ROX	ROX	Reserved field. (Access type is reserved_bit39.)
40	ROX	ROX	Reserved field. (Access type is tb_enabled.)
41	ROX	ROX	Reserved field. (Access type is tb_valid.)
42	ROX	ROX	Reserved field. (Access type is tb_sync_occurred.)
43	ROX	ROX	Reserved field. (Access type is tb_missing_sync.)
44	ROX	ROX	Reserved field. (Access type is tb_missing_step.)
45	ROX	ROX	Reserved field. (Access type is tb_residue_err.)
46	ROX	ROX	Reserved field. (Access type is firmware_control_error.)
47:50	ROX	ROX	CHIP_TOD_STATUS: Chip time-of-day status.
51	ROX	ROX	Reserved field. (Access type is chip_tod_interrupt.)
52	ROX	ROX	Reserved field. (Access type is reserved_bit52.)
53	ROX	ROX	Reserved field. (Access type is reserved_bit53.)
54	ROX	ROX	Reserved field. (Access type is reserved_bit54.)
55	ROX	ROX	Reserved field. (Access type is reserved_bit55.)
56	ROX	ROX	Reserved field. (Access type is chip_tod_parity_error.)
57	ROX	ROX	Reserved field. (Access type is purr_parity_error.)
58	ROX	ROX	Reserved field. (Access type is spurr_parity_error.)
59	ROX	ROX	Reserved field. (Access type is dec_parity_error.)
60	ROX	ROX	Reserved field. (Access type is tfmr_corrupt.)
61	ROX	ROX	Reserved field. (Access type is purr_overflow_error.)
62	ROX	ROX	Reserved field. (Access type is spurr_overflow_error.)

Bits	SPRD	SPR_T3	Field Mnemonic: Description
63	ROX	ROX	Reserved field. (Access type is reserved_bit63.)

Register Name	*PLL Control Register NSL*
Mnemonic	IOMC0.TX_WRAP.PLL_MCIO.CWRAP.PLL_CNTRL_SETUP0
Address	0000000000000003 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0:2	RW	
3	RW	SHADOW_BYPASSN: Bypass low active. When it is set to 0, it keeps PLL in bypass independent from external reset or bypass. For operation mode, set this bit to 1. 1: Off 0: On
4:8	RW	SHADOW_SPEDIV: Testout Divide Selector
9:11	RW	SHADOW_CPISEL:
12:20	RW	SHADOW_DIVSELB:
21:22	RW	SHADOW_PCLKSEL:
23	RW	SHADOW_UNUSED0:
24:27	RO	SHADOW_BANDSEL:
28:38	RW	SHADOW_ANALOGTUNE:
39:42	RW	SHADOW_ATSTSEL:
43	RW	SHADOW_VCOSEL:
44:47	RW	SHADOW_BGOFFSET:
48:51	RW	SHADOW_CCALBANDSEL:
52:54	RW	SHADOW_UNUSED1:
55	RW	SHADOW_CCALFMAX:
56	RW	SHADOW_CCALFMIN:
57	RW	SHADOW_CCALLOAD:
58	RW	SHADOW_CCALCVHOLD:
59	RW	Reserved field. (Access type is SHADOW_unused.)
60	RW	SHADOW_CCALMETH:
61	RW	SHADOW_UNUSED4: Controls vregbypass.
62	RW	SHADOW_CMLEN:
63	RW	SHADOW_UNUSED5:

Register Name	*PLL Control Register NSL*
Mnemonic	IOMC1.TX_WRAP.PLL_MCIO.CWRAP.PLL_CNTRL_SETUP0
Address	0000000000000003 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0:2	RW	
3	RW	SHADOW_BYPASSN: Bypass low active. When it is set to 0, it keeps PLL in bypass independent from external reset or bypass. For operation mode, set this bit to 1. 1: Off 0: On
4:8	RW	SHADOW_SPEDIV: Testout Divide Selector
9:11	RW	SHADOW_CPISEL:
12:20	RW	SHADOW_DIVSELB:
21:22	RW	SHADOW_PCLKSEL:
23	RW	SHADOW_UNUSED0:
24:27	RO	SHADOW_BANDSEL:
28:38	RW	SHADOW_ANALOGTUNE:
39:42	RW	SHADOW_ATSTSEL:
43	RW	SHADOW_VCOSEL:
44:47	RW	SHADOW_BGOFFSET:
48:51	RW	SHADOW_CCALBANDSEL:
52:54	RW	SHADOW_UNUSED1:
55	RW	SHADOW_CCALFMAX:
56	RW	SHADOW_CCALFMIN:
57	RW	SHADOW_CCALLOAD:
58	RW	SHADOW_CCALCVHOLD:
59	RW	Reserved field. (Access type is SHADOW_unused.)
60	RW	SHADOW_CCALMETH:
61	RW	SHADOW_UNUSED4: Controls vregbypass.
62	RW	SHADOW_CMLEN:
63	RW	SHADOW_UNUSED5:

Register Name	***PLL Control Register NSL***
Mnemonic	ABUS.TX_WRAP.PLL_A.CWRAP.PLL_CNTRL_SETUP1
Address	0000000000000004 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0	RW	SHADOW_CALREQ:
1	RW	SHADOW_CALRECAL:
2:5	RW	SHADOW_RDIV:
6:7	RW	SHADOW_UNUSED2:
8	RO	SHADOW_CCALCOMP:
9	RO	SHADOW_CCALERR:
10:62	RO	Reserved field. (Access type is SHADOW_unused.)
63	RW	SHADOW_PLLOUTA_DISABLE:

Register Name	*TFMR Time Facility Management Register*
Mnemonic	EX03.EC.PC.PC_NW.TFC.T4_TFMR
Address	0000000000000004 (SPRD) 00000000000009EC (SPR_T4)
Attributes	
Description	

Bits	SPRD	SPR_T4	Field Mnemonic: Description
0:7	RWX	RWX	Reserved field. (Access type is max_cyc_bet_steps.)
8:9	RWX	RWX	Reserved field. (Access type is n_clks_per_step.)
10	RWX	RWX	Reserved field. (Access type is mask_hmi.)
11:13	RWX	RWX	Reserved field. (Access type is sync_bit_sel.)
14	RWX	RWX	Reserved field.
15	RWX	RWX	Reserved field. (Access type is reserved_bit15.)
16	RWX	RWX	Reserved field. (Access type is load_tod_mod.)
17	RWX	RWX	Reserved field. (Access type is reserved_bit17.)
18	RWX	RWX	Reserved field. (Access type is move_chip_tod_to_tb.)
19	RWX	RWX	Reserved field. (Access type is reserved_bit19.)
20	RWX	RWX	Reserved field. (Access type is reserved_bit20.)
21	RWX	RWX	Reserved field. (Access type is reserved_bit21.)
22	RWX	RWX	Reserved field. (Access type is reserved_bit22.)
23	RWX	RWX	Reserved field. (Access type is reserved_bit23.)
24	RWX	RWX	Reserved field. (Access type is clear_tb_errors.)
25	ROX	ROX	Reserved field. (Access type is reserved_bit25.)
26	ROX	ROX	Reserved field. (Access type is hdec_parity_error.)
27	ROX	ROX	Reserved field. (Access type is tbst_corrupt.)
28:31	ROX	ROX	Reserved field. (Access type is tbst_encoded.)
32:35	ROX	ROX	Reserved field. (Access type is tbst_last.)
36	ROX	ROX	Reserved field. (Access type is reserved_bit36.)
37	ROX	ROX	Reserved field. (Access type is reserved_bit37.)
38	ROX	ROX	Reserved field. (Access type is reserved_bit38.)
39	ROX	ROX	Reserved field. (Access type is reserved_bit39.)
40	ROX	ROX	Reserved field. (Access type is tb_enabled.)
41	ROX	ROX	Reserved field. (Access type is tb_valid.)
42	ROX	ROX	Reserved field. (Access type is tb_sync_occurred.)
43	ROX	ROX	Reserved field. (Access type is tb_missing_sync.)
44	ROX	ROX	Reserved field. (Access type is tb_missing_step.)
45	ROX	ROX	Reserved field. (Access type is tb_residue_err.)
46	ROX	ROX	Reserved field. (Access type is firmware_control_error.)
47:50	ROX	ROX	CHIP_TOD_STATUS: Chip time-of-day status.
51	ROX	ROX	Reserved field. (Access type is chip_tod_interrupt.)
52	ROX	ROX	Reserved field. (Access type is reserved_bit52.)
53	ROX	ROX	Reserved field. (Access type is reserved_bit53.)

Bits	SPRD	SPR_T4	Field Mnemonic: Description
54	ROX	ROX	Reserved field. (Access type is reserved_bit54.)
55	ROX	ROX	Reserved field. (Access type is reserved_bit55.)
56	ROX	ROX	Reserved field. (Access type is chip_tod_parity_error.)
57	ROX	ROX	Reserved field. (Access type is purr_parity_error.)
58	ROX	ROX	Reserved field. (Access type is spurr_parity_error.)
59	ROX	ROX	Reserved field. (Access type is dec_parity_error.)
60	ROX	ROX	Reserved field. (Access type is tfmr_corrupt.)
61	ROX	ROX	Reserved field. (Access type is purr_overflow_error.)
62	ROX	ROX	Reserved field. (Access type is spurr_overflow_error.)
63	ROX	ROX	Reserved field. (Access type is reserved_bit63.)

Register Name	***PLL Control Register NSL***
Mnemonic	IOMC0.TX_WRAP.PLL_MCIO.CWRAP.PLL_CNTRL_SETUP1
Address	0000000000000004 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0	RW	SHADOW_CALREQ:
1	RW	SHADOW_CALRECAL:
2:5	RW	SHADOW_RDIV:
6:7	RW	SHADOW_UNUSED2:
8	RO	SHADOW_CCALCOMP:
9	RO	SHADOW_CCALERR:
10:62	RO	Reserved field. (Access type is SHADOW_unused.)
63	RW	SHADOW_PLLOUTA_DISABLE:

Register Name	***PLL Control Register NSL***
Mnemonic	IOMC1.TX_WRAP.PLL_MCIO.CWRAP.PLL_CNTRL_SETUP1
Address	0000000000000004 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0	RW	SHADOW_CALREQ:
1	RW	SHADOW_CALRECAL:
2:5	RW	SHADOW_RDIV:
6:7	RW	SHADOW_UNUSED2:
8	RO	SHADOW_CCALCOMP:
9	RO	SHADOW_CCALERR:
10:62	RO	Reserved field. (Access type is SHADOW_unused.)
63	RW	SHADOW_PLLOUTA_DISABLE:

Register Name	*PLL Control Register NSL*
Mnemonic	ABUS.TX_WRAP.PLL_A.CWRAP.PLL_CNTRL_SETUP2
Address	0000000000000005 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0	RO	SHADOW_UNUSED_OUTB_DISABLE: Unused: Disable for output b.
1:3	RO	SHADOW_UNUSED: Unused.
4	RW	SHADOW_RESET: Reset for Tank and Filt PLL.
5:7	RO	SHADOW_SPARE: Not used. Spare.

Register Name	*TFMR Time Facility Management Register*
Mnemonic	EX03.EC.PC.PC_NW.TFC.T5_TFMR
Address	0000000000000005 (SPRD) 00000000000009ED (SPR_T5)
Attributes	
Description	

Bits	SPRD	SPR_T5	Field Mnemonic: Description
0:7	RWX	RWX	Reserved field. (Access type is max_cyc_bet_steps.)
8:9	RWX	RWX	Reserved field. (Access type is n_clks_per_step.)
10	RWX	RWX	Reserved field. (Access type is mask_hmi.)
11:13	RWX	RWX	Reserved field. (Access type is sync_bit_sel.)
14	RWX	RWX	Reserved field.
15	RWX	RWX	Reserved field. (Access type is reserved_bit15.)
16	RWX	RWX	Reserved field. (Access type is load_tod_mod.)
17	RWX	RWX	Reserved field. (Access type is reserved_bit17.)
18	RWX	RWX	Reserved field. (Access type is move_chip_tod_to_tb.)
19	RWX	RWX	Reserved field. (Access type is reserved_bit19.)
20	RWX	RWX	Reserved field. (Access type is reserved_bit20.)
21	RWX	RWX	Reserved field. (Access type is reserved_bit21.)
22	RWX	RWX	Reserved field. (Access type is reserved_bit22.)
23	RWX	RWX	Reserved field. (Access type is reserved_bit23.)
24	RWX	RWX	Reserved field. (Access type is clear_tb_errors.)
25	ROX	ROX	Reserved field. (Access type is reserved_bit25.)
26	ROX	ROX	Reserved field. (Access type is hdec_parity_error.)
27	ROX	ROX	Reserved field. (Access type is tbst_corrupt.)
28:31	ROX	ROX	Reserved field. (Access type is tbst_encoded.)
32:35	ROX	ROX	Reserved field. (Access type is tbst_last.)
36	ROX	ROX	Reserved field. (Access type is reserved_bit36.)
37	ROX	ROX	Reserved field. (Access type is reserved_bit37.)

Bits	SPRD	SPR_T5	Field Mnemonic: Description
38	ROX	ROX	Reserved field. (Access type is reserved_bit38.)
39	ROX	ROX	Reserved field. (Access type is reserved_bit39.)
40	ROX	ROX	Reserved field. (Access type is tb_enabled.)
41	ROX	ROX	Reserved field. (Access type is tb_valid.)
42	ROX	ROX	Reserved field. (Access type is tb_sync_occurred.)
43	ROX	ROX	Reserved field. (Access type is tb_missing_sync.)
44	ROX	ROX	Reserved field. (Access type is tb_missing_step.)
45	ROX	ROX	Reserved field. (Access type is tb_residue_err.)
46	ROX	ROX	Reserved field. (Access type is firmware_control_error.)
47:50	ROX	ROX	CHIP_TOD_STATUS: Chip time-of-day status.
51	ROX	ROX	Reserved field. (Access type is chip_tod_interrupt.)
52	ROX	ROX	Reserved field. (Access type is reserved_bit52.)
53	ROX	ROX	Reserved field. (Access type is reserved_bit53.)
54	ROX	ROX	Reserved field. (Access type is reserved_bit54.)
55	ROX	ROX	Reserved field. (Access type is reserved_bit55.)
56	ROX	ROX	Reserved field. (Access type is chip_tod_parity_error.)
57	ROX	ROX	Reserved field. (Access type is purr_parity_error.)
58	ROX	ROX	Reserved field. (Access type is spurr_parity_error.)
59	ROX	ROX	Reserved field. (Access type is dec_parity_error.)
60	ROX	ROX	Reserved field. (Access type is tfmr_corrupt.)
61	ROX	ROX	Reserved field. (Access type is purr_overflow_error.)
62	ROX	ROX	Reserved field. (Access type is spurr_overflow_error.)
63	ROX	ROX	Reserved field. (Access type is reserved_bit63.)

Register Name	***PLL Control Register NSL***
Mnemonic	IOMC0.TX_WRAP.PLL_MCIO.CWRAP.PLL_CNTRL_SETUP2
Address	0000000000000005 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0	RO	SHADOW_UNUSED_OUTB_DISABLE: Unused: Disable for output b.
1:3	RO	SHADOW_UNUSED: Unused.
4	RW	SHADOW_RESET: Reset for Tank and Filt PLL.
5:7	RO	SHADOW_SPARE: Not used. Spare.

Register Name	***PLL Control Register NSL***
Mnemonic	IOMC1.TX_WRAP.PLL_MCIO.CWRAP.PLL_CNTRL_SETUP2
Address	0000000000000005 (PLLREG)
Attributes	
Description	

Bits	PLLREG	Field Mnemonic: Description
0	RO	SHADOW_UNUSED_OUTB_DISABLE: Unused: Disable for output b.
1:3	RO	SHADOW_UNUSED: Unused.
4	RW	SHADOW_RESET: Reset for Tank and Filt PLL.
5:7	RO	SHADOW_SPARE: Not used. Spare.

Register Name	*FSI PIB2OPB Locked Status*
Mnemonic	TPC.FSI.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.LSTAT
Address	0000000000030002 (PIB)
Attributes	
Description	The PIB2OPB FSI master ports locked status via PIB FSI-0 host access via ports. The lower address is for the host only.

Bits	PIB	Field Mnemonic: Description
0:31	RO	Reserved.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	*PIB2OPB Unit Reset*
Mnemonic	TPC.FSI.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.RESET
Address	0000000000030004 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	WO_1P	Reset. Unit Reset

Register Name	*FSI PIB2OPB cMFSI Remote Slave Interrupt*
Mnemonic	TPC.FSI.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.CRSIC
Address	0000000000030005 (PIB)
Attributes	
Description	The PIB2OPB interrupts of the cMFSI port attached to FSI slaves read/clear via PIB FSI-0 host access via ports. The lower address is for the host only.

Bits	PIB	Field Mnemonic: Description
0:63	RW_WCLEAR	FSI PIB2OPB cMFSI remote slave interrupt.

Register Name	*FSI PIB2OPB Command and Write Data*
Mnemonic	TPC.FSI.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.CMD_WRDAT
Address	0000000000030000 (PIB)
Attributes	
Description	The PIB2OPB command/write-data register to access FSI master ports via PIB FSI-0 host access via ports. The lower address is for the host only.

Bits	PIB	Field Mnemonic: Description
0	RW	WRITE_NOT_READ: Write not read.

Bits	PIB	Field Mnemonic: Description
1:31	RW	Reserved field. (Access type is cmd.)
32:63	RW	Reserved field. (Access type is wdata.)

Register Name	*FSI PIB2OPB cMFSI Remote Slave Interrupt Mask*
Mnemonic	TPC.FSI.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.CRSIM
Address	0000000000030006 (PIB)
Attributes	
Description	The PIB2OPB mask for interrupts of cMFSI port attached FSI slaves read/write via PIB FSI-0 Host access via ports. The lower address is for the host only.

Bits	PIB	Field Mnemonic: Description
0:63	RW	FSI PIB2OPB cMFSI remote slave interrupt mask.

Register Name	*FSI PIB2OPB cMFSI Remote Slave Interrupt Status*
Mnemonic	TPC.FSI.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.CRSIS
Address	0000000000030007 (PIB)
Attributes	
Description	PIB2OPB status of interrupts of cMFSI port attached FSI slaves PIB read via PIB FSI-0 host access via ports. The lower address is for the host only.

Bits	PIB	Field Mnemonic: Description
0:63	RO	FSI PIB2OPB cMFSI remote slave interrupt status.

Register Name	*FSI PIB2OPB MFSI Remote Slave Interrupt*
Mnemonic	TPC.FSI.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.RSIC
Address	0000000000030008 (PIB)
Attributes	
Description	PIB2OPB interrupts of MFSI port attached FSI slaves read/clear via PIB FSI-0 host access via ports. The lower address is for the host only.

Bits	PIB	Field Mnemonic: Description
0:63	RW_WCLEAR	FSI PIB2OPB MFSI remote slave interrupt.

Register Name	*FSI PIB2OPB MFSI Remote Slave Interrupt Mask*
Mnemonic	TPC.FSI.FSI_SLAVE.CMFSI_INCLUDE.MFSI_B.PIB2OPB.COMP.P#0.P.RSIM
Address	0000000000030009 (PIB)
Attributes	
Description	PIB2OPB mask for interrupts of MFSI port attached FSI slaves read/write via PIB FSI-0 host access via ports. The lower address is for the host only.

Bits	PIB	Field Mnemonic: Description
0:63	RW	FSI PIB2OPB MFSI remote slave interrupt mask.

Register Name	*TOD: Master Paths Control Register*
Mnemonic	EH.TPCHIP.PIB.TOD.TOD_M_PATH_CTRL_REG
Address	0000000000040000 (PIB)
Attributes	
Description	Setup for oscillator validity, step alignment, sync pulse frequency, and step check.

Bits	PIB	Field Mnemonic: Description
0	RW	M_PATH_0_OSC_NOT_VALID: Master path-0: oscillator not valid. OFF: A valid oscillator is attached to master path-0. ON: No valid oscillator is attached to master path-0.
1	RW	M_PATH_1_OSC_NOT_VALID: Master path-1: oscillator not valid. OFF: A valid oscillator is attached to master path-1. ON: No valid oscillator is attached to master path-1.
2	RW	M_PATH_0_STEP_ALIGN_DISABLE: Master path-0: step alignment disable. OFF: Alignment of master path-0 step to master path-1 step is active. ON: Alignment of master path-0 step to master path-1 step is not active.
3	RW	M_PATH_1_STEP_ALIGN_DISABLE: Master path-1: step alignment disable. OFF: Alignment of master path-1 step to master path-0 step is active. ON: Alignment of master path-1 step to master path-0 step is not active.
4	RW	REG_0X00_SPARE_04: Spares.
5:7	RW	M_PATH_SYNC_CREATE_SPS_SELECT: Master path: sync create: Steps Per Sync (SPS). Select the number of step pulses per sync pulse. 000: 512_STEPS 001: 128_STEPS 010: 64_STEPS 011: 32_STEPS 100: 4096_STEPS 101: 2048_STEPS 110: 1024_STEPS 111: 256_STEPS
8:11	RW	M_PATH_0_STEP_CHECK_CPS_DEVIATION: Master path-0: step check: CPS deviation. 0000: 00_00_PCENT 0001: 06_25_PCENT 0010: 12_50_PCENT 0011: 18_75_PCENT 0100: 25_00_PCENT 0101: 31_25_PCENT 0110: 37_50_PCENT 0111: 43_75_PCENT 1000: 50_00_PCENT 1001: 56_25_PCENT 1010: 62_50_PCENT 1011: 68_75_PCENT 1100: 75_00_PCENT 1101: 81_25_PCENT 1110: 87_50_PCENT 1111: 93_75_PCENT
12	RW	REG_0X00_SPARE_12: Spares.
13:15	RW	M_PATH_0_STEP_CHECK_VALIDITY_COUNT: Master path-0: step check: validity count. Defines the required number of valid steps before step check is enabled. 000: 1_STEPS 001: 2_STEPS 010: 4_STEPS 011: 8_STEPS 100: 16_STEPS 101: 32_STEPS 110: 64_STEPS 111: 128_STEPS

Bits	PIB	Field Mnemonic: Description
16:19	RW	M_PATH_1_STEP_CHECK_CPS_DEVIATION: Master path-1: step check: CPS deviation. 0000: 00_00_PCENT 0001: 06_25_PCENT 0010: 12_50_PCENT 0011: 18_75_PCENT 0100: 25_00_PCENT 0101: 31_25_PCENT 0110: 37_50_PCENT 0111: 43_75_PCENT 1000: 50_00_PCENT 1001: 56_25_PCENT 1010: 62_50_PCENT 1011: 68_75_PCENT 1100: 75_00_PCENT 1101: 81_25_PCENT 1110: 87_50_PCENT 1111: 93_75_PCENT
20	RW	M_PATH_STEP_CREATE_DUAL_EDGE_DISABLE: Master path-01: step create: dual edge disable. OFF: Sample both edges of the oscillator. ON: Sample only the rising edge of the oscillator.
21:23	RW	M_PATH_1_STEP_CHECK_VALIDITY_COUNT: Master path-1: step check: validity count. Defines the required number of valid steps before step check is enabled. 000: 1_STEPS 001: 2_STEPS 010: 4_STEPS 011: 8_STEPS 100: 16_STEPS 101: 32_STEPS 110: 64_STEPS 111: 128_STEPS
24:25	RW	M_PATH_STEP_CHECK_CPS_DEVIATION_FACTOR: Master path-01: step check: CPS deviation factor: 00: 1 01: 2 10: 4 11: 8
26:31	RW	REG_0X00_SPARE_26_31: Spares.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	*TOD: Primary Configuration: Distribution Port-0 Control Register*
Mnemonic	EH.TPCHIP.PIB.TOD.TOD_PRI_PORT_0_CTRL_REG
Address	0000000000040001 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:2	RW	PRI_PORT_0_RX_SELECT: Distribution: primary configuration: port-0 RX select: 000: A0_PORT_0 001: A1_PORT_0 010 : A2_PORT_0 011: X0_PORT_0 100: X1_PORT_0 101 : X2_PORT_0 110: X3_PORT_0 111: X4_PORT_0
3	RW	REG_0X01_SPARE_03: Spares.

Bits	PIB	Field Mnemonic: Description
4:5	RWX	PRI_A0_PORT_0_TX_SELECT: Distribution: primary configuration: A0 port-0 TX select: 00: S_PATH_0 01: S_PATH_1 10 : M_PATH_0 11: M_PATH_1
6:7	RWX	PRI_A1_PORT_0_TX_SELECT: Distribution: primary configuration: A1 port-0 TX select: 00: S_PATH_0 01: S_PATH_1 10: M_PATH_0 11; M_PATH_1
8:9	RWX	PRI_A2_PORT_0_TX_SELECT: Distribution: primary configuration: A2 port-0 TX select: 00: S_PATH_0 01: S_PATH_1 10: M_PATH_0 11: M_PATH_1
10:11	RWX	PRI_X0_PORT_0_TX_SELECT: Distribution: primary configuration: X0 port-0 TX select: 00: S_PATH_0 01: S_PATH_1 10: M_PATH_0 11: M_PATH_1
12:13	RWX	PRI_X1_PORT_0_TX_SELECT: Distribution: primary configuration: X1 port-0 TX select: 00: S_PATH_0 01: S_PATH_1 10: M_PATH_0 11: M_PATH_1
14:15	RWX	PRI_X2_PORT_0_TX_SELECT: Distribution: primary configuration: X2 port-0 TX select: 00: S_PATH_0 01: S_PATH_1 10: M_PATH_0 11: M_PATH_1
16:17	RWX	PRI_X3_PORT_0_TX_SELECT: Distribution: primary configuration: X3 port-0 TX select: 00: S_PATH_0 01: S_PATH_1 10: M_PATH_0 11: M_PATH_1
18:19	RWX	PRI_X4_PORT_0_TX_SELECT: Distribution: primary configuration: X3 port-0 TX select: 00: S_PATH_0 01: S_PATH_1 10: M_PATH_0 11: M_PATH_1
20	RW	PRI_A0_PORT_0_TX_ENABLE: Distribution: primary configuration: A0 port-0 TX enable: OFF: Port is configured as a receiver. ON: Port is configured as a sender.
21	RW	PRI_A1_PORT_0_TX_ENABLE: Distribution: primary configuration: A1 port-0 TX enable: OFF: Port is configured as a receiver. ON: Port is configured as a sender.
22	RW	PRI_A2_PORT_0_TX_ENABLE: Distribution: primary configuration: A2 port-0 TX enable.: OFF: Port is configured as a receiver. ON: Port is configured as a sender.
23	RW	PRI_X0_PORT_0_TX_ENABLE: Distribution: primary configuration: X0 port-0 TX enable: OFF: Port is configured as a receiver. ON: Port is configured as a sender.
24	RW	PRI_X1_PORT_0_TX_ENABLE: Distribution: primary configuration: X1 port-0 TX enable: OFF: Port is configured as a receiver. ON: Port is configured as a sender.
25	RW	PRI_X2_PORT_0_TX_ENABLE: Distribution: primary configuration: X2 port-0 TX enable: OFF: Port is configured as a receiver. ON: Port is configured as a sender.

Bits	PIB	Field Mnemonic: Description
26	RW	PRI_X3_PORT_0_TX_ENABLE: Distribution: primary configuration: X3 port-0 TX enable: OFF: Port is configured as a receiver. ON: Port is configured as a sender.
27	RW	PRI_X4_PORT_0_TX_ENABLE: Distribution: primary configuration: X4 port-0 TX enable: OFF: Port is configured as a receiver. ON: Port is configured as a sender.
28:31	RW	REG_0X01_SPARE_28_31: Spares.
32:39	RW	PRI_I_PATH_DELAY_VALUE: Internal path: primary configuration: delay value.
40:63	RO	Constant = 0b000000000000000000000000

Register Name	*TOD: Primary Configuration: Distribution Port-1 Control Register*
Mnemonic	EH.TPCHIP.PIB.TOD.TOD_PRI_PORT_1_CTRL_REG
Address	0000000000040002 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:2	RW	PRI_PORT_1_RX_SELECT: Distribution: primary configuration: port-1 RX select: 000: A0_PORT_1 001: A1_PORT_1 010: A2_PORT_1 011: X0_PORT_1 100: X1_PORT_1 101: X2_PORT_1 110: X3_PORT_1 111: X4_PORT_1
3	RW	REG_0X02_SPARE_03: Spares.
4:5	RWX	PRI_A0_PORT_1_TX_SELECT: Distribution: primary configuration: A0 port-1 TX select: 00: S_PATH_0 01: S_PATH_1 10: M_PATH_0 11: M_PATH_1
6:7	RWX	PRI_A1_PORT_1_TX_SELECT: Distribution: primary configuration: A1 port-1 TX select: 00: S_PATH_0 01: S_PATH_1 10: M_PATH_0 11: M_PATH_1
8:9	RWX	PRI_A2_PORT_1_TX_SELECT: Distribution: primary configuration: A2 port-1 TX select: 00: S_PATH_0 01: S_PATH_1 10: M_PATH_0 11: M_PATH_1
10:11	RWX	PRI_X0_PORT_1_TX_SELECT: Distribution: primary configuration: X0 port-1 TX select: 00: S_PATH_0 01: S_PATH_1 10: M_PATH_0 11: M_PATH_1
12:13	RWX	PRI_X1_PORT_1_TX_SELECT: Distribution: primary configuration: X1 port-1 TX select: 00: S_PATH_0 01: S_PATH_1 10: M_PATH_0 11: M_PATH_1

Bits	PIB	Field Mnemonic: Description
14:15	RWX	PRI_X2_PORT_1_TX_SELECT: Distribution: primary configuration: X2 port-1 TX select: 00: S_PATH_0 01: S_PATH_1 10: M_PATH_0 11: M_PATH_1
16:17	RWX	PRI_X3_PORT_1_TX_SELECT: Distribution: primary configuration: X3 port-1 TX select: 00: S_PATH_0 01: S_PATH_1 10: M_PATH_0 11: M_PATH_1
18:19	RWX	PRI_X4_PORT_1_TX_SELECT: Distribution: primary configuration: X3 port-1 TX select: 00: S_PATH_0 01: S_PATH_1 10: M_PATH_0 11: M_PATH_1
20	RW	PRI_A0_PORT_1_TX_ENABLE: Distribution: primary configuration: A0 port-1 TX enable: OFF: Port is configured as a receiver. ON: Port is configured as a sender.
21	RW	PRI_A1_PORT_1_TX_ENABLE: Distribution: primary configuration: A1 port-1 TX enable: OFF: Port is configured as a receiver. ON: Port is configured as a sender.
22	RW	PRI_A2_PORT_1_TX_ENABLE: Distribution: primary configuration: A2 port-1 TX enable: OFF: Port is configured as a receiver. ON: Port is configured as a sender.
23	RW	PRI_X0_PORT_1_TX_ENABLE: Distribution: primary configuration: X0 port-1 TX enable: OFF: Port is configured as a receiver. ON: Port is configured as a sender.
24	RW	PRI_X1_PORT_1_TX_ENABLE: Distribution: primary configuration: X1 port-1 TX enable: OFF: Port is configured as a receiver. ON: Port is configured as a sender.
25	RW	PRI_X2_PORT_1_TX_ENABLE: Distribution: primary configuration: X2 port-1 TX enable: OFF: Port is configured as a receiver. ON: Port is configured as a sender.
26	RW	PRI_X3_PORT_1_TX_ENABLE: Distribution: primary configuration: X3 port-1 TX enable: OFF: Port is configured as a receiver. ON: Port is configured as a sender.
27	RW	PRI_X4_PORT_1_TX_ENABLE: Distribution: primary configuration: X4 port-1 TX enable: OFF: Port is configured as a receiver. ON: Port is configured as a sender.
28:31	RW	REG_0X02_SPARE_28_31: Spares.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	***TOD: Secondary Configuration: Distribution Port-1 Control Register***
Mnemonic	EH.TPCHIP.PIB.TOD.TOD_SEC_PORT_1_CTRL_REG
Address	0000000000040004 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:2	RW	SEC_PORT_1_RX_SELECT: Distribution: secondary configuration: port-1 RX select: 000: A0_PORT_0 001: A1_PORT_0 010: A2_PORT_0 011: X0_PORT_0 100: X1_PORT_0 101: X2_PORT_0 110: X3_PORT_0 111: X4_PORT_0
3	RW	REG_0X04_SPARE_03: Spares.
4:5	RWX	SEC_A0_PORT_1_TX_SELECT: Distribution: secondary configuration: A0 port-1 TX select: 00: S_PATH_0 01: S_PATH_1 10: M_PATH_0 11: M_PATH_1
6:7	RWX	SEC_A1_PORT_1_TX_SELECT: Distribution: secondary configuration: A1 port-1 TX select: 00: S_PATH_0 01: S_PATH_1 10: M_PATH_0 11: M_PATH_1
8:9	RWX	SEC_A2_PORT_1_TX_SELECT: Distribution: secondary configuration: A2 port-1 TX select: 00: S_PATH_0 01: S_PATH_1 10: M_PATH_0 11: M_PATH_1
10:11	RWX	SEC_X0_PORT_1_TX_SELECT: Distribution: secondary configuration: X0 port-1 TX select: 00: S_PATH_0 01: S_PATH_1 10: M_PATH_0 11: M_PATH_1
12:13	RWX	SEC_X1_PORT_1_TX_SELECT: Distribution: secondary configuration: X1 port-1 TX select: 00: S_PATH_0 01: S_PATH_1 10: M_PATH_0 11: M_PATH_1
14:15	RWX	SEC_X2_PORT_1_TX_SELECT: Distribution: secondary configuration: X2 port-1 TX select: 00: S_PATH_0 01: S_PATH_1 10: M_PATH_0 11: M_PATH_1
16:17	RWX	SEC_X3_PORT_1_TX_SELECT: Distribution: secondary configuration: X3 port-1 TX select: 00: S_PATH_0 01: S_PATH_1 10: M_PATH_0 11: M_PATH_1
18:19	RWX	SEC_X4_PORT_1_TX_SELECT: Distribution: secondary configuration: X3 port-1 TX select: 00: S_PATH_0 01: S_PATH_1 10: M_PATH_0 11: M_PATH_1
20	RW	SEC_A0_PORT_1_TX_ENABLE: Distribution: secondary configuration: A0 port-1 TX enable: OFF: Port is configured as a receiver. ON: Port is configured as a sender.
21	RW	SEC_A1_PORT_1_TX_ENABLE: Distribution: secondary configuration: A1 port-1 TX enable: OFF: Port is configured as a receiver. ON: Port is configured as a sender.

Bits	PIB	Field Mnemonic: Description
22	RW	SEC_A2_PORT_1_TX_ENABLE: Distribution: secondary configuration: A2 port-1 TX enable: OFF: Port is configured as a receiver. ON: Port is configured as a sender.
23	RW	SEC_X0_PORT_1_TX_ENABLE: Distribution: secondary configuration: X0 port-1 TX enable: OFF: Port is configured as a receiver. ON: Port is configured as a sender.
24	RW	SEC_X1_PORT_1_TX_ENABLE: Distribution: secondary configuration: X1 port-1 TX enable: OFF: Port is configured as a receiver. ON: Port is configured as a sender.
25	RW	SEC_X2_PORT_1_TX_ENABLE: Distribution: secondary configuration: X2 port-1 TX enable: OFF: Port is configured as a receiver. ON: Port is configured as a sender.
26	RW	SEC_X3_PORT_1_TX_ENABLE: Distribution: secondary configuration: X3 port-1 TX enable: OFF: Port is configured as a receiver. ON: Port is configured as a sender.
27	RW	SEC_X4_PORT_1_TX_ENABLE: Distribution: secondary configuration: X4 port-1 TX enable: OFF: Port is configured as a receiver. ON: Port is configured as a sender.
28:31	RW	REG_0X04_SPARE_28_31: Spares.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	*TOD: Slave Path Control Register*
Mnemonic	EH.TPCHIP.PIB.TOD.TOD_S_PATH_CTRL_REG
Address	0000000000040005 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	RW	PRI_S_PATH_SELECT: Primary configuration: slave path select.
1:3	RW	REG_0X05_SPARE_01_03: Spares.
4	RW	SEC_S_PATH_SELECT: Secondary configuration: slave path select.
5	RW	REG_0X05_SPARE_05: Spares.
6:7	RW	S_PATH_STEP_CHECK_CPS_DEVIATION_FACTOR: Slave path-01: step check: CPS deviation factor: 00: 1 01: 2 10: 4 11: 8

Bits	PIB	Field Mnemonic: Description
8:11	RW	S_PATH_0_STEP_CHECK_CPS_DEVIATION: Slave path-0: step check: CPS deviation: 0000: 00_00_PCENT 0001: 06_25_PCENT 0010: 12_50_PCENT 0011: 18_75_PCENT 0100: 25_00_PCENT 0101: 31_25_PCENT 0110: 37_50_PCENT 0111: 43_75_PCENT 1000: 50_00_PCENT 1001: 56_25_PCENT 1010: 62_50_PCENT 1011: 68_75_PCENT 1100: 75_00_PCENT 1101: 81_25_PCENT 1110: 87_50_PCENT 1111: 93_75_PCENT
12	RW	REG_0X05_SPARE_12: Spares.
13:15	RW	S_PATH_0_STEP_CHECK_VALIDITY_COUNT: Slave path-0: step check: validity count. Defines the required number of valid steps before a step check is enabled. 000: 1_STEPS 001: 2_STEPS 010: 4_STEPS 011: 8_STEPS 100: 16_STEPS 101: 32_STEPS 110: 64_STEPS 111: 128_STEPS
16:19	RW	S_PATH_1_STEP_CHECK_CPS_DEVIATION: Slave path-1: step check: CPS deviation: 0000: 00_00_PCENT 0001: 06_25_PCENT 0010: 12_50_PCENT 0011: 18_75_PCENT 0100: 25_00_PCENT 0101: 31_25_PCENT 0110: 37_50_PCENT 0111: 43_75_PCENT 1000: 50_00_PCENT 1001: 56_25_PCENT 1010: 62_50_PCENT 1011: 68_75_PCENT 1100: 75_00_PCENT 1101: 81_25_PCENT 1110: 87_50_PCENT 1111: 93_75_PCENT
20	RW	REG_0X05_SPARE_20: Spares.
21:23	RW	S_PATH_1_STEP_CHECK_VALIDITY_COUNT: Slave path-1: step check: validity count Defines the required number of valid steps before a step check is enabled. 000: 1_STEPS 001: 2_STEPS 010: 4_STEPS 011: 8_STEPS 100: 16_STEPS 101: 32_STEPS 110: 64_STEPS 111: 128_STEPS

Bits	PIB	Field Mnemonic: Description
24:63	RO	Constant = 0b000000000000000000000000000000000000000000000000 000: 1_STEPS 001: 2_STEPS 010: 4_STEPS 011: 8_STEPS 100: 16_STEPS 101: 32_STEPS 110: 64_STEPS 111: 128_STEPS

Register Name	*TOD: Internal Path Control Register*
Mnemonic	EH.TPCHIP.PIB.TOD.TOD_I_PATH_CTRL_REG
Address	0000000000040006 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	RW	I_PATH_DELAY_DISABLE: Internal path: delay disable.
1	RW	I_PATH_DELAY_ADJUST_DISABLE: Internal path: delay adjust disable.
2:5	RW	REG_0X06_SPARE_02_05: Spares.
6:7	RWX	I_PATH_STEP_CHECK_CPS_DEVIATION_FACTOR: Internal path: step check: CPS deviation factor. 00: 1 01: 2 10: 4 11: 8
8:11	RW	I_PATH_STEP_CHECK_CPS_DEVIATION: Internal path: step check: CPS deviation. 0000: 00_00_PCENT 0001: 06_25_PCENT 0010: 12_50_PCENT 0011: 18_75_PCENT 0100: 25_00_PCENT 0101: 31_25_PCENT 0110: 37_50_PCENT 0111: 43_75_PCENT 1000: 50_00_PCENT 1001: 56_25_PCENT 1010: 62_50_PCENT 1011: 68_75_PCENT 1100: 75_00_PCENT 1101: 81_25_PCENT 1110: 87_50_PCENT 1111: 93_75_PCENT
12	RW	REG_0X06_SPARE_12: Spares.
13:15	RW	I_PATH_STEP_CHECK_VALIDITY_COUNT: Internal path: step check: validity count. Defines the required number of valid steps before a step check is enabled. 000: 1_STEPS 001: 2_STEPS 010: 4_STEPS 011: 8_STEPS 100: 16_STEPS 101: 32_STEPS 110: 64_STEPS 111: 128_STEPS

Bits	PIB	Field Mnemonic: Description
16:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000 000: 1_STEPS 001: 2_STEPS 010: 4_STEPS 011: 8_STEPS 100: 16_STEPS 101: 32_STEPS 110: 64_STEPS 111: 128_STEPS

Register Name	*TOD: Primary/Secondary Configuration Control Register*
Mnemonic	EH.TPCHIP.PIB.TOD.TOD_PSS_MSS_CTRL_REG
Address	0000000000040007 (PIB)
Attributes	
Description	Master/slave select, master path select, slave path select, step check setup

Bits	PIB	Field Mnemonic: Description
0	RWX	PRI_M_PATH_SELECT: Primary configuration: master path select. OFF: Master path-0 is selected. ON: Master path-1 is selected.
1	RWX	PRI_M_S_TOD_SELECT: Primary configuration: master-slave TOD select. OFF: TOD is slave. ON: TOD is master.
2	RWX	PRI_M_S_DRAWER_SELECT: Primary configuration: master-slave drawer select . OFF: Drawer is slave. ON: Drawer is master. It is just used for TOD internal power gating.
3	RWX	PRI_S_PATH_1_STEP_CHECK_ENABLE: Primary configuration: slave path-1: step check enable. OFF: Step check is disabled. ON: Step check is enabled.
4	RWX	PRI_M_PATH_0_STEP_CHECK_ENABLE: Primary configuration: master path-0: step check enable. OFF: Step check is disabled. ON: Step check is enabled.
5	RWX	PRI_M_PATH_1_STEP_CHECK_ENABLE: Primary configuration: master path-1: step check enable. OFF: Step check is disabled. ON: Step check is enabled.
6	RWX	PRI_S_PATH_0_STEP_CHECK_ENABLE: Primary configuration: slave path-0: step check enable. OFF: Step check is disabled. ON: Step check is enabled.
7	RWX	PRI_I_PATH_STEP_CHECK_ENABLE: Primary configuration: internal path: step check enable. OFF: Step check is disabled. ON: Step check is enabled.
8	RWX	SEC_M_PATH_SELECT: Secondary configuration: master path select. OFF: Master path-0 is selected. ON: Master path-1 is selected.
9	RWX	SEC_M_S_TOD_SELECT: Secondary configuration: master-slave TOD select. OFF: TOD is slave. ON: TOD is master.
10	RWX	SEC_M_S_DRAWER_SELECT: Secondary configuration: master-slave drawer select. OFF: Drawer is slave. ON: Drawer is master. It is just used for TOD internal power gating.
11	RWX	SEC_S_PATH_1_STEP_CHECK_ENABLE: Secondary configuration: slave path-1: step check enable. OFF: Step check is disabled. ON: Step check is enabled.

Bits	PIB	Field Mnemonic: Description
12	RWX	SEC_M_PATH_0_STEP_CHECK_ENABLE: Secondary configuration: master path-0: step check enable OFF: Step check is disabled. ON: Step check is enabled.
13	RWX	SEC_M_PATH_1_STEP_CHECK_ENABLE: Secondary configuration: master path-1: step check enable. OFF: Step check is disabled. ON: Step check is enabled.
14	RWX	SEC_S_PATH_0_STEP_CHECK_ENABLE: Secondary configuration: slave path-0: step check enable. OFF: Step check is disabled. ON: Step check is enabled.
15	RWX	SEC_I_PATH_STEP_CHECK_ENABLE: Secondary configuration: internal path: step check enable. OFF: Step check is disabled. ON: Step check is enabled.
16	RW	PSS_SWITCH_SYNC_ERROR_DISABLE: Miscellaneous error sync hold mode. OFF: Gating of one sync on topology switch (ttype-01) to force TOD sync check error except for the backup TOD master. ON: Disable sync-gating.
17	RWX	I_PATH_STEP_CHECK_CPS_DEVIATION_X_DISABLE: Internal path: step check: enlarge CPS deviation. That is, the CPS deviation factor = 8. OFF: Enabled. ON: Disabled.
18	RW	STEP_CHECK_ENABLE_CHICKEN_SWITCH: TType-2: Step check enable: debug switch. OFF: New behavior. ON: Old behavior.
19	RW	REG_0X07_SPARE_19: Spares.
20	RW	REG_0X07_SPARE_20: Spares.
21	RW	MISC_RESYNC_OSC_FROM_TOD: miscellaneous: OFF: Disable resynchronization of master OSC sync pulse from the TOD synchronization bit. ON: Enable resynchronization of master OSC sync pulse from the TOD synchronization bit legacy.
22:31	RW	REG_0X07_SPARE_22_31: Spares.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	***TOD: Primary/Secondary Configuration Status Register***
Mnemonic	EH.TPCHIP.PIB.TOD.TOD_PSS_MSS_STATUS_REG
Address	0000000000040008 (PIB)
Attributes	
Description	Primary/secondary status, oscillator validity, master/slave status, selected master path, selected slave path, step validity.

Bits	PIB	Field Mnemonic: Description
0:2	RWX	PRI_SEC_SELECT: Primary secondary configuration select. 000: Primary 111: Secondary
3	RW	REG_0X08_SPARE_03: Spares.
4	ROX	M_PATH_0_OSC_NOT_VALID_STATUS: Master path-0: oscillator not valid.
5	ROX	M_PATH_1_OSC_NOT_VALID_STATUS: Master path-1: oscillator not valid.
6	ROX	M_PATH_0_STEP_CHECK_VALID: Master path-0: step check: step valid.
7	ROX	M_PATH_1_STEP_CHECK_VALID: Master path-1: step check: step valid.
8	ROX	S_PATH_0_STEP_CHECK_VALID: Slave path-0: step check: step valid.
9	ROX	I_PATH_STEP_CHECK_VALID: Internal path: step check: step valid.

Bits	PIB	Field Mnemonic: Description
10	ROX	S_PATH_1_STEP_CHECK_VALID: Slave path-1: step check: step valid.
11	RWX	IS_SPECIAL_STATUS: Control: backup master: status indicating takeover.
12	ROX	PRI_M_PATH_SELECT_STATUS: Primary configuration: master path select.
13	ROX	PRI_M_S_TOD_SELECT_STATUS: Primary configuration: master-slave TOD select.
14	ROX	PRI_M_S_DRAWER_SELECT_STATUS: Primary configuration: master-slave drawer select.
15	ROX	PRI_S_PATH_SELECT_STATUS: Primary configuration: slave path select.
16	ROX	SEC_M_PATH_SELECT_STATUS: Secondary configuration: master path select.
17	ROX	SEC_M_S_TOD_SELECT_STATUS: Secondary configuration: master-slave TOD select.
18	ROX	SEC_M_S_DRAWER_SELECT_STATUS: Secondary configuration: master-slave drawer select.
19	ROX	SEC_S_PATH_SELECT_STATUS: Secondary configuration: slave path select.
20	ROX	IS_RUNNING: Status: TOD is running.
21	ROX	IS_PRIMARY: Status: TOD is using primary configuration.
22	ROX	IS_SECONDARY: Status: TOD is using secondary configuration.
23	ROX	IS_ACTIVE_MASTER: Status: TOD is active master.
24	ROX	IS_BACKUP_MASTER: Status: TOD is backup master.
25	ROX	IS_SLAVE: Status: TOD is slave.
26	ROX	M_PATH_SELECT: Status: TOD is using master path 0 or 1.
27	ROX	S_PATH_SELECT: Status: TOD is using slave path 0 or 1.
28	ROX	M_PATH_0_STEP_ALIGN_VALID_SWITCH: Master path-0: step alignment: valid switch flag.
29	ROX	M_PATH_1_STEP_ALIGN_VALID_SWITCH: Master path-1: step alignment: valid switch flag.
30	RW	REG_0X08_SPARE_30: Spares.
31	RWX	M_PATH_SWITCH_TRIGGER: Master path switch trigger.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	***TOD: Slave Path Status Register***
Mnemonic	EH.TPCHIP.PIB.TOD.TOD_S_PATH_STATUS_REG
Address	000000000004000A (PIB)
Attributes	
Description	Cycle-per-step (CPS) TOD reset triggering. A write into this register triggers the following resets if the corresponding enable bits in reg_0x0B are active: • Master path-0 step alignment FSM reset • Master path-1 step alignment FSM reset • Slave path-0 step creation CPS counter reset • Slave path-1 step creation CPS counter reset

Bits	PIB	Field Mnemonic: Description
0:3	RWX	M_PATH_0_STEP_ALIGN_FSM_STATE: Master path-0: step alignment: FSM state (debug only).
4:7	RWX	M_PATH_1_STEP_ALIGN_FSM_STATE: Master path-1: step alignment: FSM state (debug only).
8:12	RWX	I_PATH_DELAY_ADJUST_RATIO: Internal path: delay: adjustment ratio (debug only).
13:15	RW	REG_0X0A_SPARE_13_15: Spares.
16:23	RWX	S_PATH_1_CPS: Slave path-1: CPS.
24:31	RWX	S_PATH_0_CPS: Slave path-0: CPS.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	*TOD: Miscellaneous, TOD Reset Triggering*
Mnemonic	EH.TPCHIP.PIB.TOD.TOD_MISC_RESET_REG
Address	000000000004000B (PIB)
Attributes	
Description	A write into this register triggers the following resets if the corresponding enable bits in reg_0x0B are active: • Master path-0 sync create counter reset • Master path-1 sync create counter reset

Bits	PIB	Field Mnemonic: Description
0	RW	M_PATH_0_STEP_CREATE_THRESHOLD_RESET_ENABLE: Master path-0: step create: threshold reset enable. Master path-0: step alignment: FSM reset enable.
1	RW	M_PATH_0_STEP_ALIGN_THRESHOLD_RESET_ENABLE: Master path-0: step alignment: threshold reset enable. Master path-1: step alignment: FSM reset enable.
2	RW	M_PATH_1_STEP_CREATE_THRESHOLD_RESET_ENABLE: Master path-1: step create: threshold reset enable. Slave path-1: step RX: threshold reset enable.
3	RW	M_PATH_1_STEP_ALIGN_THRESHOLD_RESET_ENABLE: Master path-1: step alignment: threshold reset enable .Slave path-0: step RX: threshold reset enable.
4:7	RW	REG_0X0B_SPARE_04_07: Spares.
8	RW	PROBE_0_TOGGLE_ENABLE: Probe output-0: toggle enable.
9	RW	PROBE_1_TOGGLE_ENABLE: Probe output-1: toggle enable.
10	RW	PROBE_2_TOGGLE_ENABLE: Probe output-2: toggle enable.
11	RW	PROBE_3_TOGGLE_ENABLE: Probe output-3: toggle enable.
12:15	RW	REG_0X0B_SPARE_12_15: Spares.
16	RW	TRACE_ENABLE: Trace: Tracing enable.
17	RW	REG_0X0B_SPARE_17: Spares.
18:19	RW	TRACE_DATA_SELECT: Trace: trace data select. Select one of the four blocks of 88-bit data.
20	RW	M_PATH_0_SYNC_CREATE_COUNTER_RESET_ENABLE: Master path-0: sync create: counter reset enable.
21	RW	M_PATH_1_SYNC_CREATE_COUNTER_RESET_ENABLE: Master path-1: sync create: counter reset enable.
22	RW	REG_0X0B_SPARE_22: Spares.
23	RWX	I_PATH_DELAY_ADJUST_RESET: Internal path: delay: adjust reset.
24:32	RWX	I_PATH_DELAY_TWOS_COMPL_LOAD_VALUE: Internal path: delay: twos complement load value.
33:39	RW	REG_0X0B_SPARE_33_39: Spares.
40:63	RO	Constant = 0b000000000000000000000000

Register Name	*TOD: Probe Data Select Register*
Mnemonic	EH.TPCHIP.PIB.TOD.TOD_PROBE_SELECT_REG
Address	000000000004000C (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:7	RW	PROBE_0_DATA_SELECT: Probe-0: input data select.
8:15	RW	PROBE_1_DATA_SELECT: Probe-1: input data select.

Bits	PIB	Field Mnemonic: Description
16:23	RW	PROBE_2_DATA_SELECT: Probe-2: input data select.
24:31	RW	PROBE_3_DATA_SELECT: Probe-3: input data select.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	*TOD: Chip Control Register*
Mnemonic	EH.TPCHIP.PIB.TOD.TOD_CHIP_CTRL_REG
Address	0000000000040010 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	RW	TIMEBASE_ENABLE: Timebase enable.
1:3	RW	I_PATH_CORE_SYNC_PERIOD_SELECT: Internal path: core sync period select: 000: 8_US 001: 4_US 010: 2_US 011: 1_US 100: 128_US 101: 64_US 110: 32_US 111: 16_US
4	RW	I_PATH_SYNC_CHECK_DISABLE: Internal path: sync check disable: OFF: TOD sync check enable. ON: TOD sync check disable.
5	RW	TX_TTYPE_PIB_MST_FSM_STATE_DISABLE: TX TType: PIB master FSM state: enable: OFF: Disabled. ON: Enabled.
6	RW	REG_0X10_SPARE_06: Spares.
7	RW	MOVE_TOD_TO_TB_ON_2X_SYNC_ENABLE: Move-TOD-To-Timebase on 2x sync boundary: enable: OFF: Move-TOD-To-Timebase on 1x sync boundary. ON: Move-TOD-To-Timebase on 2x sync boundary.
8	RW	USE_TB_SYNC_MECHANISM: Use Timebase sync mechanism: OFF: Reserved. ON: Use the tb_enable signal as sync event.
9	RW	USE_TB_STEP_SYNC: Use Timebase step sync: OFF: Use stepsync from the internal path. ON: Use the programmable cycle counter for the step.
10:15	RW	LOW_ORDER_STEP_VALUE: Low-order step value needed to use_tb_step_sync as the programmable cycle counter for creating a step: 000000: INVALID 000001: 1_CYCLE_STEP 000010: 2_CYCLE_STEP 000011: 3_CYCLE_STEP 000100: 4_CYCLE_STEP
16:25	RW	REG_0X10_SPARE_16_25: Spares.
26	WO	TX_TTYPE_PIB_MST_IF_RESET: TX TType: PIB master interface reset. Request a PIB master reset to the PIB arbiter. The reset request is sent to the PIB arbiter after a delay of four steps.
27:29	RW	REG_0X10_SPARE_27_29: Spares.
30	RW	XSTOP_GATE: System checkstop gate: OFF: Stop TOD when a system checkstop occurs. ON: Keep TOD running when a system checkstop occurs.

Bits	PIB	Field Mnemonic: Description
31	RW	STICKY_ERROR_INJECT_ENABLE: Sticky error inject enable.
32:63	RO	Constant = 0b00000000000000000000000000000000

Register Name	*TOD: TX TTYPE-0 Triggering Register*
Mnemonic	EH.TPCHIP.PIB.TOD.TOD_TX_TTYPE_0_REG
Address	0000000000040011 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	WO	TX_TTYPE_0_TRIGGER: TX TTYPE-0 trigger
1:63	RO	Constant = 0b00000000000000000000000000000000000000000000000000000000000000

Register Name	*Number of Slaves in Multicast Group 1*
Mnemonic	EH.TPCHIP.PIB.PCBMS.MCAST_GRP_1_SLAVES_REG
Address	00000000000F0001 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:5	RWX	SLAVES_MCAST_GROUP_1: Number of slaves in multicast group 1.

Register Name	*Number of Slaves in Multicast Group 2*
Mnemonic	EH.TPCHIP.PIB.PCBMS.MCAST_GRP_2_SLAVES_REG
Address	00000000000F0002 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:5	RWX	SLAVES_MCAST_GROUP_2: Number of slaves in multicast group 2.

Register Name	*Number of Slaves in Multicast Group 3*
Mnemonic	EH.TPCHIP.PIB.PCBMS.MCAST_GRP_3_SLAVES_REG
Address	00000000000F0003 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:5	RWX	SLAVES_MCAST_GROUP_3: Number of slaves in multicast group 3.

Register Name	*Number of Slaves in Multicast Group 4*
Mnemonic	EH.TPCHIP.PIB.PCBMS.MCAST_GRP_4_SLAVES_REG
Address	00000000000F0004 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:5	RWX	SLAVES_MCAST_GROUP_4: Number of slaves in multicast group 4.

Register Name	*Register Containing Information on what Slave Responded with an Error During a Multicast Access*
Mnemonic	EH.TPCHIP.PIB.PCBMS.REC_ERR_REG1
Address	00000000000F0012 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	ROX	SLAVE16_RESPONSE_BIT: Bit indicating that Slave16 has responded.
1:3	RWX_WAND	SLAVE16_ERROR_CODE: Slave16 error code: 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout.
4	ROX	SLAVE17_RESPONSE_BIT: Bit indicating that Slave17 has responded.
5:7	RWX_WAND	SLAVE17_ERROR_CODE: Slave17 error code: 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout.
8	ROX	SLAVE18_RESPONSE_BIT: Bit indicating that Slave18 has responded.
9:11	RWX_WAND	SLAVE18_ERROR_CODE: Slave18 error code: 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout.
12	ROX	SLAVE19_RESPONSE_BIT: Bit indicating that Slave19 has responded.
13:15	RWX_WAND	SLAVE19_ERROR_CODE: Slave19 error code: 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout.
16	ROX	SLAVE20_RESPONSE_BIT: Bit indicating that Slave20 has responded.
17:19	RWX_WAND	SLAVE20_ERROR_CODE: Slave20 error code: 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout.
20	ROX	SLAVE21_RESPONSE_BIT: Bit indicating that Slave21 has responded.

Bits	PIB	Field Mnemonic: Description
21:23	RWX_WAND	SLAVE21_ERROR_CODE: Slave21 error code: 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout.
24	ROX	SLAVE22_RESPONSE_BIT: Bit indicating that Slave22 has responded.
25:27	RWX_WAND	SLAVE22_ERROR_CODE: Slave22 error code: 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout.
28	ROX	SLAVE23_RESPONSE_BIT: Bit indicating that Slave23 has responded.
29:31	RWX_WAND	SLAVE23_ERROR_CODE: Slave23 error code: 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout.
32	ROX	SLAVE24_RESPONSE_BIT: Bit indicating that Slave24 has responded.
33:35	RWX_WAND	SLAVE24_ERROR_CODE: Slave24 error code: 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout.
36	ROX	SLAVE25_RESPONSE_BIT: Bit indicating that Slave25 has responded.
37:39	RWX_WAND	SLAVE25_ERROR_CODE: Slave25 error code: 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout.
40	ROX	SLAVE26_RESPONSE_BIT: Bit indicating that Slave26 has responded.
41:43	RWX_WAND	SLAVE26_ERROR_CODE: Slave26 error code: 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout.
44	ROX	SLAVE27_RESPONSE_BIT: Bit indicating that Slave27 has responded.
45:47	RWX_WAND	SLAVE27_ERROR_CODE: Slave27 error code: 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout.
48	ROX	SLAVE28_RESPONSE_BIT: Bit indicating that Slave28 has responded.
49:51	RWX_WAND	SLAVE28_ERROR_CODE: Slave28 error code: 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout.
52	ROX	SLAVE29_RESPONSE_BIT: Bit indicating that Slave29 has responded.

Bits	PIB	Field Mnemonic: Description
53:55	RWX_WAND	SLAVE29_ERROR_CODE: Slave29 error code: 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout.
56	ROX	SLAVE30_RESPONSE_BIT: Bit indicating that Slave30 has responded.
57:59	RWX_WAND	SLAVE30_ERROR_CODE: Slave30 error code: 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout.
60	ROX	SLAVE31_RESPONSE_BIT: Bit indicating that Slave31 has responded.
61:63	RWX_WAND	SLAVE31_ERROR_CODE: Slave31 error code:. 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout.

Register Name	***Internal PCB Master Error Register***
Mnemonic	EH.TPCHIP.PIB.PCBMS.ERROR_REG
Address	00000000000F001F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	RWX_WCLRREG	TIMEOUT_ACTIVE: Active when the master ran into timeout.
1	RWX_WCLRREG	PARITY_ERR: Parity error on internal FSMs.
2	RWX_WCLRREG	BEAT_NUM_ERR: Beat with the wrong beat number received.
3	RWX_WCLRREG	BEAT_REC_ERR: Unexpected beat received.
4	RWX_WCLRREG	RECEIVED_ERROR: Error packet received.
5	RWX_WCLRREG	RX_PCB_DATA_P_ERR: Data parity on an incoming packet.
6	RWX_WCLRREG	PIB_ADDR_P_ERR: Parity error on a PIB address.
7	RWX_WCLRREG	PIB_DATA_P_ERR: Parity error on PIB data.

Register Name	***Timeout Value for PCB Master***
Mnemonic	EH.TPCHIP.PIB.PCBMS.TIMEOUT_REG
Address	00000000000F0019 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:7	RW	TIMEOUT_REGISTER: Contains timeout value for the PCB master.

Register Name	*Shift Control Register*
Mnemonic	TPC.FSI.FSI_SHIFT.SHIFT_CONTROL_REGISTER_2
Address	0000000000000C10 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RWX	SHIFT_CONTROL_REGISTER: Controls the length of the set pulse.

Register Name	*FSI A Master 0*
Mnemonic	TPC.FSI.FSI_SLAVE.FSI_A_MST_0_MSIEP4
Address	0000000000000C10 (SCOMFSI0) 0000000000003040 (FSI0)
Attributes	
Description	

Bits	SCOMFSI0	FSI0	Field Mnemonic: Description
0:31	RO	RO	Constant = 0b00000000000000000000000000000000

Register Name	*FSI B Master 0*
Mnemonic	TPC.FSI.FSI_SLAVE.FSI_B_MST_0_MSIEP4
Address	0000000000000C10 (SCOMFSI1) 0000000000003040 (FSI1)
Attributes	
Description	

Bits	SCOMFSI1	FSI1	Field Mnemonic: Description
0:31	RO	RO	Constant = 0b00000000000000000000000000000000

Register Name	*FSI Data Register 0*
Mnemonic	TPC.FSI.FSI2PIB.DATA_REGISTER_0
Address	0000000000001000 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RWX	DATA_REG_0: First 32 bits for PIB access.

Register Name	*FSI Data Register 1*
Mnemonic	TPC.FSI.FSI2PIB.DATA_REGISTER_1
Address	0000000000001001 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RWX	DATA_REG_1: Second 32 bits for PIB access.

Register Name	*Contains Command to the FSI2PIB Engine*
Mnemonic	TPC.FSI.FSI2PIB.COMMAND_REGISTER
Address	0000000000001002 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0:31	RWX	CMD_REG: Command register.

Register Name	*Resets Data, Command, Status Registers*
Mnemonic	TPC.FSI.FSI2PIB.RESET
Address	0000000000001006 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0	WOX_1P	Reset. Resets command, mode, watermark, interrupt mask, status, complement mask, and true mask registers.

Register Name	*Reset PIB Master IF*
Mnemonic	TPC.FSI.FSI2PIB.SET_PIB_RESET
Address	0000000000001007 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0	WOX_1P	set_pib_reset Reset the PIB master interface.

Register Name	*Status Register*
Mnemonic	TPC.FSI.FSI2PIB.STATUS
Address	0000000000001007 (FSI)
Attributes	
Description	

Bits	FSI	Field Mnemonic: Description
0	ROX	ANY_ERROR: One of the following STATUS register bits is active: bit1, or bit2, or bit3, or bit5.
1	ROX	SYSTEM_CHECKSTOP: System checkstop.
2	ROX	SPECIAL_ATTENTION: Special attention.
3	ROX	RECOVERABLE_ERROR: Recoverable error.
4	ROX	CHIPLET_INTERRUPT_FROM_HOST: Chiplet interrupt from the host.
5	ROX	PARITY_CHECK: The FSI2PIB engine detected a parity error.
6	ROX	POWER_MANAGEMENT_INTERRUPT: Power management interrupt.
7	ROX	PROTECTION_CHECK: The FSI2PIB engine blocked operation due to security.
8	ROX	SELFBOOT_DONE: The pervasive clock controller has completed scan0.
9	ROX	RESERVED_9: Reserved.
10	ROX	RESERVED_10: Reserved.
11	ROX	PIB_ABORT: A PIB reset occurred during operation.
12:15	ROX	USE_OSC_OBSERVATION: Use the OSC observe bits.
16	ROX	VDD_NEST_OBSERVE: VDD is on.
17:19	ROX	PIB_ERROR_CODE: PIB response code.
20:23	ROX	OSCILLATOR_STATUS: OSC status.
24	ROX	PLLLOCK_0_FILTER_PLL_NEST: Nest filter PLL locked.
25	ROX	PLLLOCK_1_FILTER_PLL_MC: MC filter PLL locked.
26	ROX	PLLLOCK_2_XBUS: XBUS PLL locked (main nest).
27	ROX	PLLLOCK_3_NEST: Nest PLL locked (backup nest).
28	ROX	INTERRUPT_CONDITION_PENDING: Pending FSI2PIB interrupt condition.
29	ROX	INTERRUPT_ENABLED: FSI2PIB interrupt enabled.
30	ROX	SELFBOOT_ENGINE_ATTENTION: The self-boot engine requires attention.
31	ROX	RESERVED_31: Reserved.

Register Name	***Command Register Fast Mode***
Mnemonic	EH.TPCHIP.PIB.OTP.OTPC_M.COMMAND_REGISTER
Address	0000000000010000 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	RW	CMD_REG_BIT_WITHSTART: To initiate operation, don't care for OTP ROM controller.
1	RW	CMD_REG_BIT_WITHADDR: To initiate operation, don't care for OTP ROM controller.
2	RW	CMD_REG_BIT_READCONT: To initiate operation, don't care for OTP ROM controller.
3	RW	CMD_REG_BIT_WITHSTOP: To initiate operation, don't care for OTP ROM controller.
4:7	RW	CMD_REG_LENGTH: Maximum_read = 8. This is the only permitted value.
8:14	RW	UNUSED_8_14: Reserved. Not used.
15	RW	CMD_REG_BIT_RNW: Only a read is permitted (0b1).
16:22	RW	UNUSED_16_22: Reserved. Not used.

Bits	PIB	Field Mnemonic: Description
23:25	RW	REG_ADDR_LEN: 000: No register address in the FIFO. 001: 1 byte of CMD_REG_ADDR is valid. 010: 2 bytes of CMD_REG_ADDR are valid. 011: 3 bytes of CMD_REG_ADDR are valid. 111: 4 bytes of CMD_REG_ADDR are valid.
26:31	RW	UNUSED_26_31: Reserved. Not used.
32:39	RW	CMD_REG_ADDR_1: Address to read from: first byte.
40:47	RW	CMD_REG_ADDR_2: Address to read from: second byte.
48:55	RW	CMD_REG_ADDR_3: Address to read from: third byte.
56:63	RW	CMD_REG_ADDR_4: Address to read from: fourth byte.

Register Name	*T0 XER*
Mnemonic	EX03.EC.FX.T0_XER
Address	0000000000010000 (SPR_T0)
Attributes	
Description	Architected XER for Thread 00 (XER0)

Bits	SPR_T0	Field Mnemonic: Description
0:15	RO	Constant = 0b0000000000000000
16:63	RW	Architected XER for Thread 00 (XER0).

Register Name	*FSI PIB2OPB Command and Write Data*
Mnemonic	TPC.FSI.FSI_SLAVE.CMFSI_INCLUDE.MFSI_A.PIB2OPB.COMP.P#0.P.CMD_WRDAT
Address	0000000000020000 (PIB)
Attributes	
Description	PIB2OPB command/write-data register to access FSI master ports via PIB FSI-0 host access via ports. Lower address is for host only.

Bits	PIB	Field Mnemonic: Description
0	RW	WRITE_NOT_READ: write not read.
1:31	RW	Reserved field. (Access type is cmd.)
32:63	RW	Reserved field. (Access type is wdata.)

Register Name	*FSI GP3 Register*
Mnemonic	TPC.FSI.FSI_MAILBOX.FSXCOMP.FSXLOG.FSIGP3
Address	0000000000002812 (FSI) 0000000000002848 (FSI_BYTE) 0000000000050012 (PIB)
Attributes	
Description	

Bits	FSI	FSI_BYTE	PIB	Field Mnemonic: Description
0:15	RW	RW	RW	OSCSWITCH_CNTL0_DC: Oscillator switch 0 configuration.
16	RW	RW	RW	GP3_UNUSED_16: Not used.

Bits	FSI	FSI_BYTE	PIB	Field Mnemonic: Description
17:19	RW	RW	RW	GP3_UNUSED_17_19: Not used.
20	RW	RW	RW	PIB2PCB_DC: Directly connect FSI2PIB to the pervasive chiplet (bypass PIB and PCB).
21	RW	RW	RW	OOB_MUX_DC: Select OOB multiplexer.
22	RW	RW	RW	PCB_RESET_DC: Reset of pervasive chiplet.
23	RW	RW	RW	FENCE2_DC: FSI fence 2.
24	RW	RW	RW	FENCE3_DC: FSI fence 3.
25	RW	RW	RW	FENCE4_DC: FSI fence 4.
26	RW	RW	RW	FENCE5_DC: FSI fence 5.
27	RW	RW	RW	FENCE_DC: VDD/VIO fence.
28	RW	RW	RW	FILTPLL_PLL_RESET_DC: Reset of CP/MC filter PLL.
29	RW	RW	RW	FILTPLL_PLL_BYPASS_DC: Bypass of CP/MC filter PLL.
30	RW	RW	RW	OSCSW_PGOOD_DC_B: OSC switch power good indication.
31	RW	RW	RW	GLOBAL_EP_RESET_DC: Global endpoint reset to all slaves.

Register Name	*FSI GP4 Register*
Mnemonic	TPC.FSI.FSI_MAILBOX.FSXCOMP.FSXLOG.FSIGP4
Address	0000000000002813 (FSI) 000000000000284C (FSI_BYTE) 0000000000050013 (PIB)
Attributes	
Description	

Bits	FSI	FSI_BYTE	PIB	Field Mnemonic: Description
0	RW	RW	RW	TPFSI_SBE_FENCE_VTLIO_DC: Separate VTLIO fence for controlling SBE fencing.
1	RW	RW	RW	TPCFSI_OPB_SW_RESET_DC: Reset FSI OPB switch on VSB.
2	RW	RW	RW	TPFSI_TP_FENCE_VTLIO_DC: Fence vital I/Os.
3	RW	RW	RW	TPCFSI_OPB_SW0_FENCE_DC_0: Fence off FSI slave0 access to OPB.
4	RW	RW	RW	TPCFSI_OPB_SW0_FENCE_DC_1: Fence off PIB/host access to OPB.
5	RW	RW	RW	TPCFSI_OPB_SW0_FENCE_DC_2: Fence off PIB/nonhost access to OPB.
6	RW	RW	RW	TPCFSI_OPB_SW1_FENCE_DC_0: Fence off FSI slave1 access to OPB.
7	RW	RW	RW	TPCFSI_OPB_SW1_FENCE_DC_1: Fence off PIB access to OPB.
8:9	RW	RW	RW	TP_PLLREFCLK_RCVR_TERM_DC: PLL Refclk receiver termination.
10:11	RW	RW	RW	TP_PCIREFCLK_RCVR_TERM_DC: PCI Refclk receiver termination.
12:15	RW	RW	RW	TP_GLBCK_RELAY_STRENGTH_DC: Set strength of pervasive relay buffers.
16	RW	RW	RW	GP4_UNUSED_16: Not used.
17	RW	RW	RW	GP4_UNUSED_17: Not used.
18	RW	RW	RW	GCLK_NEST_MESH_SEL: Setting this bit controls the clock used for the Nest Clock Mesh. 0: SYNC_NEST_MESH 1: ASYNC_NEST_MESH

Bits	FSI	FSI_BYTE	PIB	Field Mnemonic: Description
19	RW	RW	RW	TP_GLBCK_MEM_TESTCLK_SEL_DC: Global clock memory test clock select.
20	RW	RW	RW	TPI2CM_BUS_FENCE_DC: I2C master bus fence.
21	RW	RW	RW	TPFSI_ARRAY_SET_VBL_TO_VDD_DC: Array set VBL to VDD.
22	RW	RW	RW	TP_PLL_TEST_BYPASS1_DC: PLL test bypass1.
23	RW	RW	RW	GP4_UNUSED_23: Not used.
24	RW	RW	RW	TP_GP_PLL_TEST_EN_DC: PLL test enable.
25	RW	RW	RW	GP4_UNUSED_25: Not used.
26	RW	RW	RW	GP4_UNUSED_26: Not used.
27	RW	RW	RW	GP4_UNUSED_27: Not used.
28	RW	RW	RW	TP_RI_DC_B: Receiver inhibit (ANDed to test pin ri).
29	RW	RW	RW	TP_DI1_DC_B: Driver inhibit (ANDed to test pin di1).
30	RW	RW	RW	TP_DI2_DC_B: Driver inhibit (ANDed to test pin di2).
31	RW	RW	RW	TP_IDDQ_DC: DDQ.

Register Name	*FSI GP5 Register*
Mnemonic	TPC.FSI.FSI_MAILBOX.FSXCOMP.FSXLOG.FSIGP5
Address	0000000000002814 (FSI) 0000000000002850 (FSI_BYTE) 0000000000050014 (PIB)
Attributes	
Description	

Bits	FSI	FSI_BYTE	PIB	Field Mnemonic: Description
0:3	RW	RW	RW	TP_PROBE0_SEL_DC: Probe 0 select.
4:7	RW	RW	RW	TP_PROBE1_SEL_DC: Probe 1 select.
8	RW	RW	RW	TP_PROBE_LOGIC_SEL_DC: Probe 0 and 1 select: 0: Clock probing 1: Logic probing
9	RW	RW	RW	TP_PROBE_DRV_EN_DC: Probe enable.
10	RW	RW	RW	TP_TEST_BURNIN_MODE_DC: Burn-in mode.
11	RW	RW	RW	GP5_UNUSED_11: Not used.
12:15	RW	RW	RW	GP5_UNUSED_12_15: Not used.
16	RW	RW	RW	FSI_PROBE_SEL_DC: Probe enable.
17	RW	RW	RW	Reserved field. (Access type is fsi_probe_sel_dc.)
18:22	RW	RW	RW	GP5_UNUSED_18_22: Not used.
23	RW	RW	RW	TP_PLL_DRV_EN_DC: PLL driver enable.
24	RW	RW	RW	TPFSI_TP_DBG_PCB_ASYNC_EN_DC:
25	RW	RW	RW	TPFSI_TP_DBG_PCB_DATA_PAR_DIS_DC:
26	RW	RW	RW	TPFSI_TP_DBG_PCB_TYPE_PAR_DIS_DC:
27	RW	RW	RW	TPFSI_TP_PCB_GSD_LATCHED_MODE_DC:
28	RW	RW	RW	TP_PIB_DISABLE_PARITY_DC: PIB parity check disable for PIB masters and slaves.
29:31	RW	RW	RW	TPFSI_TP_GPIO_PIB_TIMEOUT_DC: PIB timeout select.

Register Name	*FSI GP6 Register*
Mnemonic	TPC.FSI.FSI_MAILBOX.FSXCOMP.FSXLOG.FSIGP6
Address	0000000000002815 (FSI) 0000000000002854 (FSI_BYTE) 0000000000050015 (PIB)
Attributes	
Description	

Bits	FSI	FSI_BYTE	PIB	Field Mnemonic: Description
0:8	RW	RW	RW	TPFSI_GLBCK_RESCLK_VALUE_DC: Global resonant clock.
9:15	RW	RW	RW	GP6_UNUSED_9_15: Not used.
16:18	RW	RW	RW	TP_OSCSW_ERRINJ0_DC:
19:21	RW	RW	RW	GP6_UNUSED_19_21: Not used.
22:23	RW	RW	RW	TP_OSCSW_TWEAK_DC:
24:27	RW	RW	RW	TP_OSCSW_SKEW_ADJUST_DC:
28:30	RW	RW	RW	TP_OSCSW_SNS_CONTENT_SEL_DC:
31	RW	RW	RW	PCIE_OSCSW_PGOOD_DC: PCIe Osc switch power good.

Register Name	*FSI GP7 Register*
Mnemonic	TPC.FSI.FSI_MAILBOX.FSXCOMP.FSXLOG.FSIGP7
Address	0000000000002816 (FSI) 0000000000002858 (FSI_BYTE) 0000000000050016 (PIB)
Attributes	
Description	

Bits	FSI	FSI_BYTE	PIB	Field Mnemonic: Description
0:3	RW	RW	RW	TP_GLBCK_PCIESW_USEOSC_DC: PCIe use OSC switch.
4:7	RW	RW	RW	TP_GLBCK_PCIESW_TWEAK_DC: PCIe tweak.
8:31	RW	RW	RW	TP_OSCSWITCH_CNTL_DC: OSC switch control.

Register Name	*FSI GProcessor Register*
Mnemonic	TPC.FSI.FSI_MAILBOX.FSXCOMP.FSXLOG.FSIGProcessor
Address	0000000000002817 (FSI) 000000000000285C (FSI_BYTE) 0000000000050017 (PIB)
Attributes	
Description	

Bits	FSI	FSI_BYTE	PIB	Field Mnemonic: Description
0:7	RW	RW	RW	TP_GLBCK_XBUS_PROG_DELAY_DC: XBUS Global clock prog delay.
8:10	RW	RW	RW	TP_GLBCK_NEST_VREGDLY_BGOFFSET_DC: NEST VREG delay bgoffset.
11	RW	RW	RW	TP_GLBCK_NEST_VREGDLY_SHUTOFF_DC: NEST VREG delay shutoff.

Bits	FSI	FSI_BYTE	PIB	Field Mnemonic: Description
12:15	RW	RW	RW	GProcessor_UNUSED_12_15: Unused.
16:23	RW	RW	RW	TP_TPIO_CENT_REFCLK_EN_DC: POWER8 Memory Bus refclock enable.
24:25	RW	RW	RW	GProcessor_UNUSED_24_25: Unused.
26	RW	RW	RW	TP_TCXB_PLL_RESET_DC: XB PLL reset: Not XB, but backup PLL.
27	RW	RW	RW	TP_TCXB_PLL_BYPASS_EN_DC: XB PLL BYPASS: Not XB, but backup PLL.
28	RW	RW	RW	TP_LOWFREQTEST_VSB_REFCLK_DC: Low-frequency test VSB refclk.
29:31	RW	RW	RW	GProcessor_UNUSED_29_31: Unused.

Register Name	*Osc Switch Sense 1 Register*
Mnemonic	TPC.FSI.FSI_MAILBOX.FSXCOMP.FSXLOG.SNS1LTH
Address	0000000000002819 (FSI) 0000000000002864 (FSI_BYTE) 0000000000050019 (PIB)
Attributes	
Description	

Bits	FSI	FSI_BYTE	PIB	Field Mnemonic: Description
0:31	ROX	ROX	ROX	SNS1_UNUSED_0_31: Not used.

Register Name	*Osc Switch Sense 2 Register*
Mnemonic	TPC.FSI.FSI_MAILBOX.FSXCOMP.FSXLOG.SNS2LTH
Address	000000000000281A (FSI) 0000000000002868 (FSI_BYTE) 000000000005001A (PIB)
Attributes	
Description	

Bits	FSI	FSI_BYTE	PIB	Field Mnemonic: Description
0:31	ROX	ROX	ROX	SNS2_UNUSED_0_31: Not used.

Register Name	*PERV GP3 Register*
Mnemonic	TPC.FSI.FSI_MAILBOX.FSXCOMP.FSXLOG.PERV_GP3
Address	000000000000281B (FSI) 000000000000286C (FSI_BYTE) 000000000005001B (PIB)
Attributes	
Description	

Bits	FSI	FSI_BYTE	PIB	Field Mnemonic: Description
0	RW	RW	RW	TP_CHIPLET_CHIPLET_EN_DC: Set if chiplet is good (no partial good control).
1	RW	RW	RW	TP_CHIPLET_PCB_EP_RESET_DC: Global EP reset.
2:3	RW	RW	RW	PERV_GP3_UNUSED_2_3: Not used.
4	RW	RW	RW	TP_CHIPLET_PLLRST_DC: PLL reset. XB PLL = primary nest PLL.

Bits	FSI	FSI_BYTE	PIB	Field Mnemonic: Description
5	RW	RW	RW	TP_CHIPLET_PLLBYP_DC: PLL bypass. XB PLL = primary nest PLL.
6:10	RW	RW	RW	PERV_GP3_UNUSED_6_10: Not used.
11	RW	RW	RW	TP_CHIPLET_VTL_D_MODE_DC: LCB control for vital logic.
12	RW	RW	RW	TP_CHIPLET_VTL_ACT_DIS_DC: LCB control for vital logic.
13	RW	RW	RW	TP_CHIPLET_VTL_MPW2_DC_B: LCB control for vital logic.
14	RW	RW	RW	TP_CHIPLET_VTL_MPW1_DC_B: LCB control for vital logic.
15	RW	RW	RW	TP_CHIPLET_VTL_DELAY_LCLKR_DC: LCB control for vital logic.
16	RW	RW	RW	TP_CHIPLET_VTL_CLKOFF_DC: LCB control for vital logic.
17	RW	RW	RW	PERV_GP3_UNUSED_17: Not used.
18	RW	RW	RW	TP_CHIPLET_FENCE_EN_DC: Fencing for the chiplet.
19:25	RW	RW	RW	PERV_GP3_UNUSED_19_25: Not used.
26	RW	RW	RW	TP_CHIPLET_FENCE_PCB_DC: Fencing PCB.
27:31	RW	RW	RW	PERV_GP3_UNUSED_27_31: Not used.

Register Name	***SBE Vital Register***
Mnemonic	TPC.FSI.FSI_MAILBOX.FSXCOMP.FSXLOG.SBE_VITAL
Address	000000000000281C (FSI) 0000000000002870 (FSI_BYTE) 000000000005001C (PIB)
Attributes	
Description	

Bits	FSI	FSI_BYTE	PIB	Field Mnemonic: Description
0	RW	RW	RW	SBE_WARMSTART: A rising edge of this bit resets the selfBootEngine; this is a warmstart.
1	RW	RW	RW	SBE_PREVENT_AUTOSTART: Prevents autostart of selfBootEngine; FSI fences 2, 3, and 4 are controlled through the FSI GP register.
2	RW	RW	RW	SBE_HW_TRIGGER: Drives the sbe_hw_trigger.
3	WO	WO	WO	SBE_UPDATE_1ST_NIBBLE: If set, bits 0 - 2 get written.
4	RWX	RWX	RWX	SBE_DONE_FENCE_B_HOLD: Observation and control bit for SBE_DONE_FENCE_B_HOLD.
5	RW	RW	RW	SBE_UNUSED_5: Unused.
6	RW	RW	RW	SBE_UNUSED_6: Unused.
7	WO	WO	WO	SBE_UPDATE_2ND_NIBBLE: If set, bits 4 - 6 get written.
8	RW	RW	RW	SBE_IMAGE_SELECT: Select SEEPROM image. If 0, then first image; otherwise, second image.
9	RW	RW	RW	SBE_SELECT_CORE: Select core for hostBootImage. If 0, then first good core; otherwise, second good core.
10	RW	RW	RW	SBE_SELECT_MODE_MASTER: Select node master.
11	WO	WO	WO	SBE_UPDATE_3RD_NIBBLE: If set, bits 8 - 10 get written.
12:15	RW	RW	RW	SBE_HALT_CODE: Indicates the selfBootEngine halt reason. Set by the selfBootEngine procedure.
16:19	RW	RW	RW	SBE_PROC_AREA: Indicates the procedure area of the currently running or last running selfBootEngine procedure. Set by the selfBootEngine procedure.

Bits	FSI	FSI_BYTE	PIB	Field Mnemonic: Description
20:27	RW	RW	RW	SBE_PROC_ID: Indicates the procedure ID of the currently running or last running selfBootEngine procedure. Set by the selfBootEngine procedure.
28:31	RW	RW	RW	SBE_PROC_STEP: Indicates the procedure step of the currently running or last running selfBootEngine procedure. Set by the selfBootEngine procedure.

Register Name	*The First of Four Scratch Registers*
Mnemonic	TPC.FSI.FSI_MAILBOX.FSXCOMP.FSXLOG.SCRATCH_REGISTER_1
Address	0000000000002838 (FSI) 00000000000028E0 (FSI_BYTE) 0000000000050038 (PIB)
Attributes	
Description	

Bits	FSI	FSI_BYTE	PIB	Field Mnemonic: Description
0:31	RWX	RWX	RWX	SR_SCRATCH_REGISTER_1: Scratch 1 register.

Register Name	*The Second of Four Scratch Registers*
Mnemonic	TPC.FSI.FSI_MAILBOX.FSXCOMP.FSXLOG.SCRATCH_REGISTER_2
Address	0000000000002839 (FSI) 00000000000028E4 (FSI_BYTE) 0000000000050039 (PIB)
Attributes	
Description	

Bits	FSI	FSI_BYTE	PIB	Field Mnemonic: Description
0:31	RWX	RWX	RWX	SR_SCRATCH_REGISTER_2: Scratch 2 register.

Register Name	*The Third of Four Scratch Registers*
Mnemonic	TPC.FSI.FSI_MAILBOX.FSXCOMP.FSXLOG.SCRATCH_REGISTER_3
Address	000000000000283A (FSI) 00000000000028E8 (FSI_BYTE) 000000000005003A (PIB)
Attributes	
Description	

Bits	FSI	FSI_BYTE	PIB	Field Mnemonic: Description
0:31	RWX	RWX	RWX	SR_SCRATCH_REGISTER_3: Scratch 3 register.

Register Name	*The Last of Four Scratch Registers*
Mnemonic	TPC.FSI.FSI_MAILBOX.FSXCOMP.FSXLOG.SCRATCH_REGISTER_4
Address	000000000000283B (FSI) 00000000000028EC (FSI_BYTE) 000000000005003B (PIB)
Attributes	
Description	

Bits	FSI	FSI_BYTE	PIB	Field Mnemonic: Description
0:31	RWX	RWX	RWX	SR_SCRATCH_REGISTER_4: Scratch 4 register.

Register Name	*Lock Indications from PLLs*
Mnemonic	EH.TPCHIP.NET.PCBSLPERV.PLL_LOCK_REG
Address	00000000010F0019 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	ROX	Reserved field. (Access type is lock.)

Register Name	*Clk Ajust Config*
Mnemonic	EH.TPCHIP.NET.PCBSLPERV.CLK_ADJ_SET
Address	00000000010F0016 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:31	RW	CLK_ADJ_SET_REG: Clock adjust configuration.

Register Name	*ECCB : ECC Address Register*
Mnemonic	EH.TPCHIP.PIB.ECCB.ECC_ADDRESS_REG
Address	00000000000C0004 (PIB)
Attributes	Secure = true
Description	

Bits	PIB	Field Mnemonic: Description
0:31	WO	START_ADDR: Start of ECC range.
32:63	WO	STOP_ADDR: End of ECC range.

Register Name	*Control Register_PMC_Mode_0*
Mnemonic	EH.TPCHIP.PIB.I2CM.CONTROL_REGISTER_0
Address	00000000000A0000 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	WOX	PIB_CNTR_REG_BIT_WITHSTART_0: For the command register of the I2C engine.
1	WOX	PIB_CNTR_REG_BIT_WITHADDR_0: For the command register of the I2C engine.
2	WOX	PIB_CNTR_REG_BIT_READCONT_0: For the command register of the I2C engine.
3	WOX	PIB_CNTR_REG_BIT_WITHSTOP_0: For the command register of the I2C engine.
4:7	WOX	PIB_CNTR_REG_LENGTH_0: Maximum_write = 4. Maximum_read = 8.

Bits	PIB	Field Mnemonic: Description
8:14	WOX	PIB_CNTR_REG_ADDR_0: For the command register of the I2C engine.
15	WOX	PIB_CNTR_REG_BIT_RNW_0: For the command register of the I2C engine.
16:17	WOX	PIB_CNTR_REG_SPEED_0: 00 = 100K 01 = 400K 10 = 3400K 11 = 50K
18:22	WOX	PIB_CNTR_REG_PORT_NUMBER_0: For the mode register of the I2C engine.
23:25	WOX	REG_ADDR_LEN_0: 00 = No register address in the FIFO . 01 = 1 byte of FIFO data is the register address. 10 = 2 bytes of FIFO data are the register address. 11 = 3 bytes of FIFO data are the register address.
26	WOX	ENH_MODE_0: Enable enhanced mode in the mode register of the I2C engine.
27:31	WOX	UNUSED_0: Reserved. Not used.
32:39	WOX	PIB_CNTR_REG_DATA_1_0: Data for the I2C FIFO.
40:47	WOX	PIB_CNTR_REG_DATA_2_0: Data for the I2C FIFO.
48:55	WOX	PIB_CNTR_REG_DATA_3_0: Data for the I2C FIFO.
56:63	WOX	PIB_CNTR_REG_DATA_4_0: Data for the I2C FIFO.

Register Name	***Reset Register_PMC_Mode***
Mnemonic	EH.TPCHIP.PIB.I2CM.RESET_REGISTER_0
Address	00000000000A0001 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	WOX	overall_reset_0 This 1-bit register resets all the registers and the I2C engine.

Register Name	***Status Register_PMC_Mode***
Mnemonic	EH.TPCHIP.PIB.I2CM.STATUS_REGISTER_0
Address	00000000000A0002 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	ROX	BUS_STATUS_ADDR_NVLD_0: Address invalid.
1	ROX	BUS_STATUS_WRITE_NVLD_0: Write invalid.
2	ROX	BUS_STATUS_READ_NVLD_0: Read invalid.
3	ROX	BUS_STATUS_ADDR_P_ERR_0: Address parity error.
4	ROX	BUS_STATUS_PAR_ERR_0: Data parity error.
5	ROX	BUS_STATUS_LB_PARITY_ERROR_0: Local bus parity error.
6:13	ROX	PIB_REG_DATA_ACT_0_0: First byte of data.
14:21	ROX	PIB_REG_DATA_ACT_1_0: Second byte of data.

Bits	PIB	Field Mnemonic: Description
22:29	ROX	PIB_REG_DATA_ACT_2_0: Third byte of data.
30:37	ROX	PIB_REG_DATA_ACT_3_0: Fourth byte of data.
38:43	RO	Constant = 0b000000
44	ROX	BUS_STATUS_BUSY_0: Local bus busy.
45	ROX	BUS_STATUS_INVALID_COMMAND_0: Invalid command.
46	ROX	BUS_STATUS_PARITY_ERROR_0: Parity error.
47	ROX	BUS_STATUS_BACK_END_OVERRUN_ERROR_0: Back-end overrun error.
48	ROX	BUS_STATUS_BACK_END_ACCESS_ERROR_0: Back-end access error.
49	ROX	BUS_STATUS_ARBITRATION_LOST_ERROR_0: Arbitration lost error.
50	ROX	BUS_STATUS_NACK_RECEIVED_ERROR_0: NACK received error.
51	ROX	BUS_STATUS_DATA_REQUEST_0: Data request.
52	ROX	BUS_STATUS_COMMAND_COMPLETE_0: Command complete.
53	ROX	BUS_STATUS_STOP_ERROR_0: Stop error.
54	ROX	BUS_STATUS_I2C_PORT_BUSY_0: I2C port busy.
55	ROX	BUS_STATUS_I2C_INTERFACE_BUSY_0: I2C interface busy.
56:63	ROX	BUS_STATUS_FIFO_ENTRY_COUNT_0: FIFO entry count.

Register Name	***Data Register_PMC_Mode***
Mnemonic	EH.TPCHIP.PIB.I2CM.DATA_REGISTER_0
Address	00000000000A0003 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:7	RWX	PIB_REG_DATA_ACT_0_0: First byte of data.
8:15	RWX	PIB_REG_DATA_ACT_1_0: Second byte of data.
16:23	RWX	PIB_REG_DATA_ACT_2_0: Third byte of data.
24:31	RWX	PIB_REG_DATA_ACT_3_0: Fourth byte of data.
32:39	RWX	PIB_REG_DATA_ACT_4_0: Fifth byte of data.
40:47	RWX	PIB_REG_DATA_ACT_5_0: Sixth byte of data.
48:55	RWX	PIB_REG_DATA_ACT_6_0: Seventh byte of data.
56:63	RWX	PIB_REG_DATA_ACT_7_0: Eighth byte of data.

Register Name	***Command_Register_0***
Mnemonic	EH.TPCHIP.PIB.I2CM.COMMAND_REGISTER_0
Address	00000000000A0005 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	RWX	WITH_START_0: Decides if the start command is to be issued or not during the beginning of the operation.

Bits	PIB	Field Mnemonic: Description
1	RWX	WITH_ADDRESS_0: Decides if the device address is to be sent or not during the beginning of the operation.
2	RWX	READ_CONTINUE_0: Decides if the next read operation is a continuation of the present operation or not.
3	RWX	WITH_STOP_0: Decides if the stop command is to be issued or not during the end of the operation.
4:7	RWX	NOT_USED_0: Not used.
8:14	RWX	DEVICE_ADDRESS_0: Device address of the slave on the I2C bus.
15	RWX	READ_NOT_WRITE_0: I2C read or write.
16:31	RWX	LENGTH_IN_BYTES_0: Length of bytes to be accessed through the I2C bus.
32:39	ROX	PEEK_DATA1_0: 0: Invalid command. Written with a new command when the old command is still in progress. 1: Parity error. 2: Back-end overrun error: Writing or reading into a full or empty FIFO reply. 3: Back-end access error: Writing or reading more data than requested. 4: Arbitration lost error: The I2C bus is held by some other master when trying to access. 5: NACK received error: The slave is not responding back with the ACK. 6: Data request: The FIFO needs to be accessed some more times to fulfill the expectation. 7: State m/c idle: The I2C state machine is now an in idle state.
40	ROX	LBUS_PARITY_ERR1_0: Local bus parity error from the local bus to glue logic.
41:63	RO	Constant = 0b00000000000000000000000

Register Name	***Mode_Register_0***
Mnemonic	EH.TPCHIP.PIB.I2CM.MODE_REGISTER_0
Address	00000000000A0006 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:15	RWX	BIT_RATE_DIVISOR_0: Decides the speed on the I2C bus.
16:21	RWX	PORT_NUMBER_0: Port number.
22:26	RO	Constant = 0b00000
27	RWX	CHKSW_I2C_BUSY_0: Debug only. Should always be zero.
28	RWX	FGAT_MODE_0: FGAT mode.
29	RWX	DIAG_MODE_0: DIAG mode.
30	RWX	PACING_ALLOW_MODE_0: Pacing allow mode.
31	RWX	WRAP_MODE_0: Wrap mode.
32:39	ROX	PEEK_DATA1_0: 0: Invalid command. Written with a new command when the old command is still in progress. 1: Parity error. 2: Back-end overrun error: Writing or reading into a full or empty FIFO reply. 3: Back-end access error: Writing or reading more data than requested. 4: Arbitration lost error: The I2C bus is held by some other master when trying to access. 5: NACK received error: The slave is not responding back with the ACK. 6: Data request: The FIFO needs to be accessed some more times to fulfill the expectation. 7: State m/c idle: The I2C state machine is now an in idle state.
40	ROX	LBUS_PARITY_ERR1_0: Local bus parity error from the local bus to glue logic.
41:63	RO	Constant = 0b00000000000000000000000

Register Name	*IMM_Reset_I2C_0*
Mnemonic	EH.TPCHIP.PIB.I2CM.IMM_RESET_I2C_0
Address	00000000000A000B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	WOX	imm_reset_i2c_0. Resets command, mode, watermark, interrupt mask, and status registers.

Register Name	*Status_Register_Engine_0*
Mnemonic	EH.TPCHIP.PIB.I2CM.STATUS_REGISTER_ENGINE_0
Address	00000000000A000B (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	ROX	INVALID_CMD_0: Invalid command. New command given when the old command is not yet completed.
1	ROX	LBUS_PARITY_ERROR_0: Local bus parity error.
2	ROX	BE_OV_ERROR_0: Back-end overrun error. Writing or reading into a full or empty FIFO reply.
3	ROX	BE_ACC_ERROR_0: Back-end access error. Writing or reading more data than requested.
4	ROX	ARBITRATION_LOST_ERROR_0: Arbitration lost error. The I2C bus is held by some other master when trying to access.
5	ROX	NACK_RECEIVED_ERROR_0: NACK received error. The slave is not responding back with the ACK.
6	ROX	DATA_REQUEST_0: data request. The FIFO needs to be accessed some more times to fulfill the expectation data request.
7	ROX	cmd_complete_0: command complete. Indicates the completion of command.
8	ROX	STOP_ERROR_0: stop error. Was not able to send the stop condition on the bus.
9:15	ROX	max_num_of_ports_0. Maximum number of ports defined for this engine.
16	ROX	any_i2c_int_0
17:18	RO	Constant = 0b00
19	ROX	i2c_port_history_busy_0
20	ROX	scl_syn_0
21	ROX	sda_syn_0
22	ROX	i2c_busy_0: I2C busy. The I2C bus is occupied.
23	ROX	SELF_BUSY_0: self busy. The I2C bus is occupied by itself.
24:27	RO	Constant = 0b0000
28:31	ROX	FIFO_ENTRY_COUNT_0: fifo_entry count : The number of bytes present in the FIFO.
32:39	ROX	PEEK_DATA1_0: 0: Invalid command. Written with a new command when the old command is still in progress. 1: Parity error. 2: Back-end overrun error: Writing or reading into a full or empty FIFO reply. 3: Back-end access error: Writing or reading more data than requested. 4: Arbitration lost error: The I2C bus is held by some other master when trying to access. 5: NACK received error: The slave is not responding back with the ACK. 6: Data request: The FIFO needs to be accessed some more times to fulfill the expectation. 7: State m/c idle: The I2C state machine is now an in idle state.

Bits	PIB	Field Mnemonic: Description
40	ROX	LBUS_PARITY_ERR1_0: Local bus parity error from the local bus to glue logic.
41:63	RO	Constant = 0b00000000000000000000000

Register Name	*Number of Slaves in Multicast Group 0*
Mnemonic	EH.TPCHIP.PIB.PCBMS.MCAST_GRP_0_SLAVES_REG
Address	00000000000F0000 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:5	RWX	SLAVES_MCAST_GROUP_0: Number of slaves in multicast group 0.

Register Name	*Register Containing Information on What Slave Responded during a Multicast Access*
Mnemonic	EH.TPCHIP.PIB.PCBMS.REC_ACK_REG
Address	00000000000F0010 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:63	RWX_WCLRREG	RECEIVE_ACKNOWLEDGE_REGISTER: Register that contains the information about what slave responded during a multicast access.

Register Name	*Register Containing Information on What Slave Responded with an Error during a Multicast Access*
Mnemonic	EH.TPCHIP.PIB.PCBMS.REC_ERR_REG0
Address	00000000000F0011 (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	ROX	MASTER_RESPONSE_BIT: Bit indicating that PCBMS has responded.
1:3	RWX_WAND	MASTER_ERROR_CODE: Master error code.
4	ROX	SLAVE1_RESPONSE_BIT: Bit indicating that Slave1 has responded.
5:7	RWX_WAND	SLAVE1_ERROR_CODE: Slave1 error code, for example. 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout
8	ROX	SLAVE2_RESPONSE_BIT: Bit indicating that Slave2 has responded.
9:11	RWX_WAND	SLAVE2_ERROR_CODE: Slave2 error code, for example. 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout.
12	ROX	SLAVE3_RESPONSE_BIT: Bit indicating that Slave3 has responded.

Bits	PIB	Field Mnemonic: Description
13:15	RWX_WAND	SLAVE3_ERROR_CODE: Slave3 error code, for example. 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout.
16	ROX	SLAVE4_RESPONSE_BIT: Bit indicating that Slave4 has responded.
17:19	RWX_WAND	SLAVE4_ERROR_CODE: Slave4 error code, for example. 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout.
20	ROX	SLAVE5_RESPONSE_BIT: Bit indicating that Slave5 has responded.
21:23	RWX_WAND	SLAVE5_ERROR_CODE: Slave5 error code, for example. 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout.
24	ROX	SLAVE6_RESPONSE_BIT: Bit indicating that Slave6 has responded.
25:27	RWX_WAND	SLAVE6_ERROR_CODE: Slave6 error code, for example. 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout.
28	ROX	SLAVE7_RESPONSE_BIT: Bit indicating that Slave7 has responded.
29:31	RWX_WAND	SLAVE7_ERROR_CODE: Slave7 error code, for example. 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout.
32	ROX	SLAVE8_RESPONSE_BIT: Bit indicating that Slave8 has responded.
33:35	RWX_WAND	SLAVE8_ERROR_CODE: Slave8 error code, for example. 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout.
36	ROX	SLAVE9_RESPONSE_BIT: Bit indicating that Slave9 has responded.
37:39	RWX_WAND	SLAVE9_ERROR_CODE: Slave9 error code, for example. 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout.
40	ROX	SLAVE10_RESPONSE_BIT: Bit indicating that Slave10 has responded.
41:43	RWX_WAND	SLAVE10_ERROR_CODE: Slave10 error code, for example. 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout.
44	ROX	SLAVE11_RESPONSE_BIT: Bit indicating that Slave11 has responded.

Bits	PIB	Field Mnemonic: Description
45:47	RWX_WAND	SLAVE11_ERROR_CODE: Slave11 error code, for example. 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout.
48	ROX	SLAVE12_RESPONSE_BIT: Bit indicating that Slave12 has responded.
49:51	RWX_WAND	SLAVE12_ERROR_CODE: Slave12 error code, for example. 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout.
52	ROX	SLAVE13_RESPONSE_BIT: Bit indicating that Slave13 has responded.
53:55	RWX_WAND	SLAVE13_ERROR_CODE: Slave13 error code, for example. 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout.
56	ROX	SLAVE14_RESPONSE_BIT: Bit indicating that Slave14 has responded.
57:59	RWX_WAND	SLAVE14_ERROR_CODE: Slave14 error code, for example. 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout.
60	ROX	SLAVE15_RESPONSE_BIT: Bit indicating that Slave15 has responded.
61:63	RWX_WAND	SLAVE15_ERROR_CODE: Slave15 error code, for example. 000: OK. 010: Chiplet offline. 100: Invalid address. 110: Parity error or an unexpected or wrong packet. 111: Timeout.

Register Name	*Chip-ID Readout*
Mnemonic	EH.TPCHIP.PIB.PCBMS.DEVICE_ID_REG
Address	00000000000F000F (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0:19	RO	cfam_chipid: Chip ID also known as cfam_chipid. 0xEA049: POWER8 Processor SCM 0xE9049: POWER8 Memory Buffer
20:31	RO	vendor_id: Vendor ID. The IBM vendor ID is 0x49.
32	RO	device_id bit 32.
33	RO	device_id bit 33.
34	RO	device_id bit 34.
35	RO	Reserved field. (Access type is reserved.)
36:38	RO	socket_id: Socket position. Socket 0x0 is connected to the primary service element. Socket 0x1 is connected to the secondary service element (high end only).

Bits	PIB	Field Mnemonic: Description
39	RO	chippos_id: 0: SCMs or the first chip on DCMs. 1: Reserved.
40:45	RO	Constant = 0b000000

Register Name	*Interrupt Register for Special Attention, Checkstop, Recoverable Error*
Mnemonic	EH.TPCHIP.PIB.PCBMS.INTERRUPT_TYPE_REG
Address	00000000000F001A (PIB)
Attributes	
Description	

Bits	PIB	Field Mnemonic: Description
0	RWX_WAND	ATTENTION: Attention.
1	RWX_WAND	RECOVERABLE_ERROR: Recoverable error.
2	RWX_WAND	CHECKSTOP: Checkstop.

Register Name	*Reset Register*
Mnemonic	EH.TPCHIP.PIB.PCBMS.RESET_REG
Address	00000000000F001D (PIB)
Attributes	
Description	Bit 0 resets all PCB elements outside of the standby domain. Bit 1 resets all endpoints.

Bits	PIB	Field Mnemonic: Description
0	RW	RESET_PCB: Reset all PCB elements outside of the standby domain.
1	RW	RESET_ENDPOINTS: Unused: Reset all endpoints attached to the PCB. The bit is now in the FSI domain.
2	RW	TIMEOUT_RESET_EN: Enable to autoreset the PCB on PCB timeout.

Register Name	*PCB Master Error Register*
Mnemonic	EH.TPCHIP.PIB.PCBMS.FIRST_ERR_REG
Address	00000000000F001E (PIB)
Attributes	
Description	Contains the first error.

Bits	PIB	Field Mnemonic: Description
0	RWX_WCLRREG	FIRST_TIMEOUT_ACTIVE: Active when the master ran into timeout.
1	RWX_WCLRREG	FIRST_PARITY_ERR: Parity error on internal FSMs.
2	RWX_WCLRREG	FIRST_BEAT_NUM_ERR: Beat with wrong beat number received.
3	RWX_WCLRREG	FIRST_BEAT_REC_ERR: Unexpected beat received.
4	RWX_WCLRREG	FIRST_RECEIVED_ERROR: Error packet received.

Bits	PIB	Field Mnemonic: Description
5	RWX_WCLRREG	FIRST_RX_PCB_DATA_P_ERR: Data parity on an incoming packet.
6	RWX_WCLRREG	FIRST_PIB_ADDR_P_ERR: Parity error on a PIB address.
7	RWX_WCLRREG	FIRST_PIB_DATA_P_ERR: Parity error on PIB data.

Register Name	*GP Register 1*
Mnemonic	EH.TPCHIP.TPC.GP1
Address	0000000001000001 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	OCC_TC_ABIST_DONE_DC: OCC complex ABIST done. Reset(0).
1	ROX	NOT_USED22: Not used. Reset(0).
2	ROX	NOT_USED23: Not used. Reset(0).
3	ROX	NET_TC_ABIST_DONE_DC: PCBSL power management arrays. Reset(0).
4	ROX	OCC_TC_ABIST_DIAG_DC: OCC complex ABIST diag/RTF. Reset(0).
5	ROX	NOT_USED24: Not used. Reset(0).
6	ROX	NOT_USED25: Not used. Reset(0).
7	ROX	NOT_USED26: Not used. Reset(0).
8	ROX	NOT_USED27: Not used. Reset(0).
9	ROX	NOT_USED28: Not used. Reset(0).
10	ROX	NOT_USED29: Not used. Reset(0).
11	ROX	NOT_USED30: Not used. Reset(0).
12	ROX	NOT_USED31: Not used. Reset(0).
13	ROX	NOT_USED32: Not used. Reset(0).
14	ROX	NOT_USED33: Not used. Reset(0).
15	ROX	TC_OPCG_DONE_DC: OPCG done. For LBIST, ABIST, or other OPCG runs. Reset(0).
16	ROX	FREE_USAGE0: chiplet specific. Reset(0).
17	ROX	FREE_USAGE1: chiplet specific. Reset(0).
18	ROX	FREE_USAGE2: chiplet specific. Reset(0).
19	ROX	FREE_USAGE3: chiplet specific. Reset(0).
20	ROX	FREE_USAGE4: chiplet specific. Reset(0).
21	ROX	FREE_USAGE5: chiplet specific. Reset(0).
22	ROX	FREE_USAGE6: chiplet specific. Reset(0).
23	ROX	FREE_USAGE7: chiplet specific. Reset(0).

Register Name	*GP Register 2*
Mnemonic	EH.TPCHIP.TPC.GP2
Address	0000000001000002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:23	RW	GPIN_MASKING: GPIN bitwise interrupt masking.

Register Name	*GP Register 4*
Mnemonic	EH.TPCHIP.TPC.GP4
Address	0000000001000003 (PCB) 0000000001000006 (PCB1) 0000000001000007 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0:5	RWX	WOX_AND	WOX_OR	TC_PROBE0_SEL_DC: Probe 0 select.
6:7	RWX	WOX_AND	WOX_OR	NOT_USED34: Not used. 0b0. Reset(0b00)
8:13	RWX	WOX_AND	WOX_OR	TC_PROBE1_SEL_DC: Probe 1 select.
14:15	RWX	WOX_AND	WOX_OR	NOT_USED35: Not used. 0b0. Reset(0b00).
16:21	RWX	WOX_AND	WOX_OR	TC_PROBE2_SEL_DC: Probe 2 select.
22:23	RWX	WOX_AND	WOX_OR	NOT_USED36: Not used.: 0b0. Reset(0b00)
24:29	RWX	WOX_AND	WOX_OR	TC_PROBE3_SEL_DC: tc_probe3_sel_dc(0:5) / tcperv_sense_sel_dc(0:2). Reset(0b000000).
30	RWX	WOX_AND	WOX_OR	NOT_USED37: Not used. 0b0. Reset(0b0).
31	RWX	WOX_AND	WOX_OR	TC_GP4_OFLOW_FEH_SEL_DC: ABIST: When 1, the fail bit is an overflow. Otherwise, it is a fail. Reset(0b0).
32	RWX	WOX_AND	WOX_OR	NOT_USED38: Not used. Reset(0b0).
33	RWX	WOX_AND	WOX_OR	NOT_USED39: Not used. Reset(0b0).
34	RWX	WOX_AND	WOX_OR	NOT_USED40: Not used.
35	RWX	WOX_AND	WOX_OR	NOT_USED41: Not used. Reset(0b0).
36	RWX	WOX_AND	WOX_OR	NOT_USED42: Not used. Reset(0b0).
37	RWX	WOX_AND	WOX_OR	NOT_USED43: Not used. Reset(0b0).
38	RWX	WOX_AND	WOX_OR	NOT_USED44: Not used. Reset(0b0).
39	RWX	WOX_AND	WOX_OR	NOT_USED45: Not used. Reset(0b0).
40	RWX	WOX_AND	WOX_OR	NOT_USED46: Not used.
41	RWX	WOX_AND	WOX_OR	NOT_USED47: Not used. Reset(0b0).
42	RWX	WOX_AND	WOX_OR	NOT_USED48: Not used. Reset(0b0).
43	RWX	WOX_AND	WOX_OR	NOT_USED49: Not used. Reset(0b0).
44	RWX	WOX_AND	WOX_OR	NOT_USED50: Not used. Reset(0b0).
45	RWX	WOX_AND	WOX_OR	NOT_USED51: Not used. Reset(0b0).
46	RWX	WOX_AND	WOX_OR	NOT_USED52: Not used. Reset
47	RWX	WOX_AND	WOX_OR	NOT_USED53: Not used. Reset(0b0).

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
48	RWX	WOX_AND	WOX_OR	NOT_USED54: Not used. Reset(0b0).
49	RWX	WOX_AND	WOX_OR	NOT_USED55: Not used. Reset(0b0).
50	RWX	WOX_AND	WOX_OR	NOT_USED56: Not used. Reset(0b0).
51	RWX	WOX_AND	WOX_OR	NOT_USED57: Not used. Reset(0b0).
52	RWX	WOX_AND	WOX_OR	NOT_USED58: Not used.
53	RWX	WOX_AND	WOX_OR	NOT_USED59: Not used. Reset(0b0).
54	RWX	WOX_AND	WOX_OR	NOT_USED60: Not used. Reset(0b0).
55	RWX	WOX_AND	WOX_OR	NOT_USED61: Not used. Reset(0b0).
56	RWX	WOX_AND	WOX_OR	NOT_USED62: Not used. Reset(0b0).
57	RWX	WOX_AND	WOX_OR	NOT_USED63: Not used. Reset(0b0).
58	RWX	WOX_AND	WOX_OR	NOT_USED64: Not used.
59	RWX	WOX_AND	WOX_OR	NOT_USED65: Not used. Reset(0b0).
60	RWX	WOX_AND	WOX_OR	NOT_USED66: Not used. Reset(0b0).
61	RWX	WOX_AND	WOX_OR	NOT_USED67: Not used. Reset(0b0).
62	RWX	WOX_AND	WOX_OR	NOT_USED68: Not used. Reset(0b0).
63	RWX	WOX_AND	WOX_OR	NOT_USED69: Not used. Reset(0b0).

Register Name	***PSCOMLE Mode Register***
Mnemonic	EH.TPCHIP.TPC.EPS.PSC.PSCOM_MODE_REG
Address	0000000001010000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	ABORT_ON_PCB_ADDR_PARITY_ERROR: Abort on PCB address parity error.
1	RW	ABORT_ON_PCB_WDATA_PARITY_ERROR: Abort on PCB with data parity_error.
2	RW	ABORT_ON_DL_RETURN_P0_ERROR: Abort on DL return P0 error.
3	RW	ABORT_ON_DL_RETURN_WDATA_PARITY_ERROR: Abort on DL return with data parity error.
4	RW	WATCHDOG_ENABLE: watchdog_enable.
5:6	RW	SCOM_HANG_LIMIT: 11: 256 10: 512 01: 768 00: 1023
7	RW	FORCE_ALL_RINGS: Set to logic 1 if all rings should be enabled independent of the ring address.
8	RW	FSM_SELFRESET_ON_STATEVEC_PARITYERROR_ENABLE: Reset the state machine if the system is in an invalid state.
9:11	RW	RESERVED_PSCOM_MODE_LT: Reserved.

Register Name	*Debug Status Register*
Mnemonic	EH.TPCHIP.TPC.EPS.PSC.DEBUG_STATUS_REG
Address	0000000001010004 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	LOCAL_TRACE_RUN_IN: Local trace run.
1:2	RWX	TRACE_STATE_LAT: Trace state latch.
3	RWX	TRACE_FREEZE: Trace freeze.
4:5	RWX	COND3_STATE_LT: Condition 3 state latch.
6:7	RWX	COND5_STATE_LT: Condition 5 state latch.
8	RWX	HISTORY_CONDITION0_LT: Condition event history for condtition0_lt.
9	RWX	HISTORY_CONDITION1_LT: Condition event history for condtition1_lt.
10	RWX	HISTORY_COND2_3_EVENT: Condition event history for cond2_3_event.
11	RWX	HISTORY_COND2_TIMEOUT: Condition event history for cond2_timeout.
12	RWX	HISTORY_COND4_5_EVENT: Condition event history for cond4_5_event.
13	RWX	HISTORY_COND4_TIMEOUT: Condition event history for cond4_timeout.
14:15	RWX	RESERVED_TCDBG_STATUS_LT: Reserved. Set to zero.

Register Name	*Trace Array High Data Register*
Mnemonic	EH.TPCHIP.TPC.TRA.TR.SAMP.LEAF.COMP.TRACE_HI_DATA_REG
Address	0000000001010400 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:63	ROX	TRACE_HI_DATA: Trace array data 0:63.

Register Name	*Trace Array Low Data Register*
Mnemonic	EH.TPCHIP.TPC.TRA.TR.SAMP.LEAF.COMP.TRACE_LO_DATA_REG
Address	0000000001010401 (SCOM)
Attributes	
Description	

Bits	SCOM	Field Mnemonic: Description
0:31	ROX	TRACE_LO_DATA: Trace Array Data 64:95.
32:41	ROX	TRACE_ADDRESS: Trace address.
42:50	ROX	TRACE_LAST_BANK: Trace last bank.
51	ROX	TRACE_LAST_BANK_VALID: Trace last bank valid.
52	ROX	TRACE_WRITE_ON_RUN: Trace write-on-run indicator.
53	ROX	TRACE_RUNNING: Trace run indicator.
54:63	ROX	TRACE_HOLD_ADDRESS: Trace hold address (pointing to last entry).

Register Name	*Interrupt Presentation Register 1*
Mnemonic	EH.TPCHIP.TPC.ITR.COMP.INTERRUPT1_REG
Address	0000000001020000 (PCB) 0000000001020001 (PCB1) 0000000001020002 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0:31	RWX	WOX_OR	WOX_AND	INTERRUPT1: Interrupt type 1 (gp) for up to 32 chiplets.

Register Name	*Interrupt Presentation Register 2*
Mnemonic	EH.TPCHIP.TPC.ITR.COMP.INTERRUPT2_REG
Address	0000000001020003 (PCB) 0000000001020004 (PCB1) 0000000001020005 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0:31	RWX	WOX_OR	WOX_AND	INTERRUPT2: Interrupt type 2 (cc) for up to 32 chiplets

Register Name	*Interrupt Presentation Register 3*
Mnemonic	EH.TPCHIP.TPC.ITR.COMP.INTERRUPT3_REG
Address	0000000001020006 (PCB) 0000000001020007 (PCB1) 0000000001020008 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0:31	RWX	WOX_OR	WOX_AND	INTERRUPT3: Interrupt type 3 (--) for up to 32 chiplets.

Register Name	*Interrupt Presentation Register 4*
Mnemonic	EH.TPCHIP.TPC.ITR.COMP.INTERRUPT4_REG
Address	0000000001020009 (PCB) 000000000102000A (PCB1) 000000000102000B (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0:31	RWX	WOX_OR	WOX_AND	INTERRUPT4: Interrupt type 4 (--) for up to 32 chiplets.

Register Name	*Interrupt Type Mask Register*
Mnemonic	EH.TPCHIP.TPC.ITR.COMP.INTERRUPT_TYPE_MASK_REG
Address	000000000102000C (PCB) 000000000102000D (PCB1) 000000000102000E (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RW	RW_WOR	RW_WAND	INTERRUPT_TYPE_MASK_GP: Mask all BIST Done interrupts. 0: Active. 1: Masked.
1	RW	RW_WOR	RW_WAND	INTERRUPT_TYPE_MASK_CC: Mask all clock state change interrupts . 0: Active. 1: Masked.
2	RW	RW_WOR	RW_WAND	INTERRUPT_TYPE_MASK_UNUSED2: Mask all clock state change interrupts. 0: Active. 1: Masked.
3	RW	RW_WOR	RW_WAND	INTERRUPT_TYPE_MASK_UNUSED3: Mask all clock state change interrupts. 0: Active. 1: Masked.

Register Name	*Interrupt Configuration Register*
Mnemonic	EH.TPCHIP.TPC.ITR.COMP.INTERRUPT_CONF_REG
Address	000000000102000F (PCB) 0000000001020010 (PCB1) 0000000001020011 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RW	RW_WOR	RW_WAND	INTERRUPT_CONF_GP: Configuration for BIST Done interrupts. 0: Or. 1: And.
1	RW	RW_WOR	RW_WAND	INTERRUPT_CONF_CC: Configuration for clock state change interrupts . 0: Or. 1: And.
2	RW	RW_WOR	RW_WAND	INTERRUPT_CONF_UNUSED2: Configuration for clock state change interrupts . 0: Or. 1: And.
3	RW	RW_WOR	RW_WAND	INTERRUPT_CONF_UNUSED3: Configuration for clock state change interrupts. 0: Or. 1: And.

Register Name	*Last Interrupt Packet Received from PCB Master*
Mnemonic	EH.TPCHIP.TPC.ITR.COMP.INTERRUPT_HOLD_REG
Address	0000000001020012 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:25	ROX	INTERRUPT_HOLD: Last interrupt packet received from the PCB master.

Register Name	*IPOLL Mask Register*
Mnemonic	EH.TPCHIP.TPC.ITR.MISC.HOST_MASK_REG
Address	0000000001020013 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	IPOLL_MASK_X: Mask xstop for host/core/millicode.
1	RW	IPOLL_MASK_R: Mask recoverable for host/core/millicode.
2	RW	IPOLL_MASK_A: Mask special attention for host/core/millicode.
3	RW	IPOLL_MASK_H: Mask host attention for host/core/millicode.
4	RW	ERROR_MASK_X: Mask xstop from fsi_intr.
5	RW	ERROR_MASK_R: Mask recoverable from fsi_intr.
6	RW	ERROR_MASK_A: Mask attention from fsi_intr.
7	RW	ERROR_MASK_H: Mask host attention from fsi_intr.

Register Name	*Status of the Errors*
Mnemonic	EH.TPCHIP.TPC.ITR.MISC.ERROR_STATUS_REG
Address	0000000001020014 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	ROX	ipoll_err_masked. Status of ipoll errors.
4:7	ROX	fsi_err_masked. Status of FSI errors.

Register Name	*OSC Error Hold Latch*
Mnemonic	EH.TPCHIP.TPC.ITR.OSCERR.OSCERR_HOLD
Address	0000000001020019 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RWX	OSCERR_CP: OSC error hold values for cp.
4:7	RWX	OSCERR_MEM: OSC error hold values for mem.

Bits	PCB	Field Mnemonic: Description
8:11	RWX	Reserved.
12:15	RWX	OSCERR_CPLITE: OSC error hold values for cplite.

Register Name	*OSC Error Mask Latch*
Mnemonic	EH.TPCHIP.TPC.ITR.OSCERR.OSCERR_MASK
Address	000000000102001A (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	OSCERR_CP_MASK: OSC error mask values for cp.
4:7	RW	OSCERR_MEM_MASK: OSC error mask values for mem.
8:11	RW	Reserved.
12:15	RW	OSCERR_CPLITE_MASK: OSC error mask values for cplite.

Register Name	*OPCG Control Register 0*
Mnemonic	EH.TPCHIP.TPC.OPCG_REG0
Address	0000000001030002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	RUNN_MODE: 1: runn-mode. 0: BIST mode.
1	RWX	OPCG_GO: OPCG go (start sequence).
2	RWX	RUN_SCAN0: Run scan0 (overrides all BIST mode settings but the scan_ratio).
3	RW	SCAN0_MODE: Set PRPGs in scan0_mode but do not run automatic scan0 sequence.
4:8	RW	SCAN_RATIO: scan_ratio (n=0-15: (n+1):1). 16: 24:1 17: 32:1 18: 48:1 19: 64:1 20: 128:1
9	RW	INOP_FORCE_SG: Set SG high during INOP.
10:13	RW	INOP_ALIGN: INOP phase alignment: 0: none 1: 2:1 2: 3:1 3: 4:1 4: 6:1 5: 8:1 6: 12:1 7: 16:1 8: 24:1
14:20	RW	INOP_WAIT: INOP cycle delay (1 - 127).
21:24	RWX	SNOP_ALIGN: BIST mode: SNOP phase alignment (like INOP), runn-mode: loopcnt(0:3).
25:27	RWX	SNOP_WAIT: BIST mode: SNOP cycle delay (0 - 7), runn-mode: loopcnt(4:6).

Bits	PCB	Field Mnemonic: Description
28:31	RWX	ENOP_ALIGN: BIST mode: ENOP phase alignment (like INOP), runn-mode: loopcnt(7:10).
32:34	RWX	ENOP_WAIT: BIST mode: ENOP cycle delay (0 - 7), runn-mode: loopcnt(11:13).
35	RWX	ENOP_FORCE_SG: BIST mode: Set SG high during ENOP, runn-mode: loopcnt(14).
36:63	RWX	LOOP_COUNT: BIST mode: Loop count (l = 1-2^28 (about 5 minutes LBIST)), runn-mode: loopcnt(15:42).

Register Name	*OPCG Control Register 1*
Mnemonic	EH.TPCHIP.TPC.OPCG_REG1
Address	0000000001030003 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	FUNC_CAPT_COUNT: BIST mode: Capture cycles (1 - 12) encoded as capture cycle – 1.
4:8	RW	FUNC_CAPT_SEQ01_01F: BIST mode: Capture cycle 1 for fast domain or single mesh support (SL, NSL, ARY, SG, FCE).
9:13	RW	FUNC_CAPT_SEQ02_02F: BIST mode: Capture cycle 2 for fast domain or single mesh support (SL, NSL, ARY, SG, FCE).
14:18	RW	FUNC_CAPT_SEQ03_03F: BIST mode: Capture cycle 3 for fast domain or single mesh support (SL, NSL, ARY, SG, FCE).
19:23	RW	FUNC_CAPT_SEQ04_04F: BIST mode: Capture cycle 4 for fast domain or single mesh support (SL, NSL, ARY, SG, FCE).
24:28	RW	FUNC_CAPT_SEQ05_05F: BIST mode: Capture cycle 5 for fast domain or single mesh support (SL, NSL, ARY, SG, FCE).
29:33	RW	FUNC_CAPT_SEQ06_06F: BIST mode: Capture cycle 6 for fast domain or single mesh support (SL, NSL, ARY, SG, FCE).
34:38	RW	FUNC_CAPT_SEQ07_07F: BIST mode: Capture cycle 7 for fast domain or single mesh support (SL, NSL, ARY, SG, FCE).
39:43	RW	FUNC_CAPT_SEQ08_08F: BIST mode: Capture cycle 8 for fast domain or single mesh support (SL, NSL, ARY, SG, FCE).
44:48	RW	FUNC_CAPT_SEQ09_01FBY2: BIST mode: Capture cycle 1 for slow domain or cycle 9 for single mesh support (SL, NSL, ARY, SG, FCE).
49:53	RW	FUNC_CAPT_SEQ10_02FBY2: BIST mode: Capture cycle 2 for slow domain or cycle 10 for single mesh support (SL, NSL, ARY, SG, FCE).
54:58	RW	FUNC_CAPT_SEQ11_03FBY2: BIST mode: Capture cycle 3 for slow domain or cycle 11 for single mesh support (SL, NSL, ARY, SG, FCE).
59:63	RW	FUNC_CAPT_SEQ12_04FBY2: BIST mode: Capture cycle 4 for slow domain or cycle 12 for single mesh support (SL, NSL, ARY, SG, FCE).

Register Name	*OPCG Control Register 2*
Mnemonic	EH.TPCHIP.TPC.OPCG_REG2
Address	0000000001030004 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:11	RW	SCAN_COUNT: BIST mode: Channel scan count (s = 0 - 4095) runn-mode: start_abist match value (0:11).

Bits	PCB	Field Mnemonic: Description
12:23	RW	MISR_A_VAL: BIST mode: The a value for the MISR aperture, runn-mode: start_abist match value (12:23).
24:35	RW	MISR_B_VAL: BIST mode: The b value for the MISR aperture, runn-mode: start_abist match value (24:35).
36:47	RW	MISR_INIT_WAIT: BIST mode: Delay the MISR aperture. MISRs become active after this number of loops.
48	RW	OPCG_SUPPRESS_EVEN_CLK: OPCG will only create even and not odd clocks. Used for runn to create only one clock in fast domain. The default is 0.
49:51	RW	OPCG_PAD_VALUE: After setting all DC signals, wait this many number of cycle x 16 before applying tholds.
52	RW	USE_F_AND_FDIV2: BIST mode: If 1, use the 8 f and 4 f/2 patterns concurrently. Otherwise, use 1 - 12 local mesh patterns.
53	RW	USE_ARY_CLK_DURING_FILL: BIST mode: Fire nsl_ary_clock during NSL-fill runn-mode. Stop run-n on xstop.
54	RW	SG_HIGH_DURING_FILL: BIST mode: Hold SG high during NSL-fill runn-mode. The OPCG engine controls start_abist (overrides GP0 setting).
55	RW	RTIM_THOLD_FORCE: Force rtim_thold low when not in test_dc mode (must be 0 at all times).
56	RW	LBIST_SKITTER_CTL: BIST mode: 0: Enable skitter during lbist_ip. 1: Enable skitter when misr_active.
57	RW	MISR_MODE: BIST mode: MISR aperture mode: 0: a-1 to b-1. 1: Start to a and b to end.
58	RW	INFINITE_MODE: Infinite mode.
59:63	RW	NSL_FILL_COUNT: BIST mode: NSL-fill count (0 - 31).

Register Name	*OPCG Start Register*
Mnemonic	EH.TPCHIP.TPC.OPCG_REG3
Address	0000000001030005 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	OPCG_GO2: OPCG go for broadcast sequences (start sequence).
1	RW	RUN_OPCG_ON_UPDATE_DR: Start the OPCG engine when scan updated (update_dr) is received (set pulse).
2	RW	RUN_OPCG_ON_CAPTURE_DR: Start the OPCG engine when scan updated (capture_dr) is received (set pulse).
3:4	RW	ALIGN_SOURCE_SELECT: 0: Use the inopa setting from opcg_reg0. 1: Use the rising edge of the sync pulse. 2: Use input from the unit (for AVP).
5:7	RW	PRPG_WEIGHTING: prpg_activate: Steer the logic built-in self test (LBIST) pattern generation to increase test coverage. 000: 1/2 (Default). The pseudo-random generator generates 1s 50% of the time and 0s 50% of the time. 001: 1/4. The pseudo-random generator generates 1s 25% of the time and 0s 75% of the time. 010: 1/8. The pseudo-random generator generates 1s 12% of the time and 0s 88% of the time. 011: 1/16. The pseudo-random generator generates 1s 6% of the time and 0s 94% of the time. 100: 1/2. The pseudo-random generator generates 1s 50% of the time and 0s 50% of the time. 101: 3/4. The pseudo-random generator generates 1s 75% of the time and 0s 25% of the time. 110: 7/8. The pseudo-random generator generates 1s 88% of the time and 0s 12% of the time. 111: 15/16. The pseudo-random generator generates 1s 94% of the time and 0s 6% of the time.
8:19	RWX	PRPG_VALUE: Set to 0 for PRPG always on. Otherwise, set to a starting value for the PRPG.

Bits	PCB	Field Mnemonic: Description
20	RW	EXTEND_INOPW_ENOPW: Extend I/ENOPW. Add 256 cycles if INOP or ENOP is greater than 0. Otherwise, 257 + maximum INOP or ENOP.
21	RW	EXTEND_SNOPW: Add 256 cycles if SNOP is greater than 0. Otherwise, 257 + maximum SNOP.
22	RW	FORCE_SG_HIGH_DURING_SNOP: Force sg high during SNOP.
23:31	RW	CHKSW: Reserved for debug switches (keep 0 unless a debug switch is required).
32:43	RW	PRPG_A_VAL: The a value for the PRPG aperture.
44:55	RW	PRPG_B_VAL: The b value for the PRPG aperture.
56	RW	PRPG_MODE: PRPG aperture mode: 0: a-1 to b-1. 1: Start to a and b to end.
57	RW	SCAN_CLK_USE_EVEN: Generate the scan clock in an odd cycle instead of an even cycle. The default is 0.
58	RWX	AUTO_SCAN0: Will run a full scan0 on chiplet to clear all data.
59:63	RW	SPARE3: Spares.

Register Name	***Start/Stop of Clocks***
Mnemonic	EH.TPCHIP.TPC.CLK_REGION
Address	0000000001030006 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RWX	CLOCK_CMD: Command for clock control: 00: NOP. 01: START. 10: STOP. 11: PULSE (one pulse).
2:3	RO	Constant = 0b00
4	RWX	CLOCK_REGION_PERV: For clock region perv (Pervasive).
5	RWX	CLOCK_REGION_UNIT0: For clock region net.
6	RWX	CLOCK_REGION_UNIT1: For clock region PIB.
7	RWX	CLOCK_REGION_UNIT2: For clock region OCC.
8	RWX	CLOCK_REGION_UNIT3: For clock region unit3. Region is unused.
9	RWX	CLOCK_REGION_UNIT4: For clock region unit4. Region is unused.
10	RWX	CLOCK_REGION_UNIT5: For clock region unit5. Region is unused.
11	RWX	CLOCK_REGION_PLL: For clock region PLL.
12	RWX	CLOCK_REGION_OSCSW: For clock region oscsw.
13:19	RO	Constant = 0b0000000
20	RWX	SEL_THOLD_SL: Select sl tholds.
21	RWX	SEL_THOLD_NSL: Select nsl tholds.
22	RWX	SEL_THOLD_ARY: Select array thold.

Register Name	*Scan Region and Type*
Mnemonic	EH.TPCHIP.TPC.SCANSELQ
Address	0000000001030007 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	Constant = 0b000
3	RW_WCLRPART	SCANSEL_CLK_VITL: Scan clock region vitl (Vital = Clock).
4	RWX	SCANSEL_CLK_PERV: Scan clock region perv (Pervasive).
5	RWX	SCANSEL_CLK_UNIT0: Scan clock region net.
6	RWX	SCANSEL_CLK_UNIT1: Scan clock region PIB.
7	RWX	SCANSEL_CLK_UNIT2: Scan clock region OCCextra DRAM.
8	RWX	SCANSEL_CLK_UNIT3: Scan clock region unit3. Region is unused.
9	RWX	SCANSEL_CLK_UNIT4: Scan clock region unit4. Region is unused.
10	RWX	SCANSEL_CLK_UNIT5: Scan clock region unit5. Region is unused.
11	RWX	SCANSEL_CLK_PLL: Scan clock region PLL.
12	RWX	SCANSEL_CLK_OSCSW: Scan clock region oscsw.
13:19	RO	Constant = 0b0000000
20	RW	SCANSEL_FUNC: Scan chain func (functional).
21	RW	SCANSEL_CFG: Scan chain mode (boot configuration and debug configuration).
22	RW	SCANSEL_CCFG_GPTR: Scan chain ccfg / gptr (Pervasive: CC configuration, Others: GPTR).
23	RW	SCANSEL_REGF: Scan chain regf (register files).
24	RW	SCANSEL_LBIST: Scan chain lbst (LBIST).
25	RW	SCANSEL_ABIST: Scan chain abst (ABIST).
26	RW	SCANSEL_REPR: Scan chain repr (Array Repair).
27	RW	SCANSEL_TIME: Scan chain time (Array Timing).
28	RW	SCANSEL_BNDY: Scan chain bndy (Boundary I/Os).
29	RW	SCANSEL_FARR: Scan chain farr (fast array unload).
30	RW	SCANSEL_CMSK: Scan chain cmsk (lbist channel mask).

Register Name	*Clocks Running*
Mnemonic	EH.TPCHIP.TPC.CLOCK_STAT
Address	0000000001030008 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	CLOCK_STATUS_PERV_FUNC_SL: Status of perv func_sl_thold: 0 = Run. 1 = Stop.
1	ROX	CLOCK_STATUS_PERV_FUNC_NSL: Status of perv func_nsl_thold: 0 = Run. 1 = Stop.

Bits	PCB	Field Mnemonic: Description
2	ROX	CLOCK_STATUS_PERV_ARY_NSL: Status of perv ary_nsl_thold: 0 = Run. 1 = Stop.
3	ROX	CLOCK_STATUS_UNIT0_FUNC_SL: Status of net func_sl_thold: 0 = Run. 1 = Stop.
4	ROX	CLOCK_STATUS_UNIT0_FUNC_NSL: Status of net func_nsl_thold: 0 = Run. 1 = Stop.
5	ROX	CLOCK_STATUS_UNIT0_ARY_NSL: Status of net ary_nsl_thold: 0 = Run. 1 = Stop.
6	ROX	CLOCK_STATUS_UNIT1_FUNC_SL: Status of pib func_sl_thold: 0 = Run. 1 = Stop.
7	ROX	CLOCK_STATUS_UNIT1_FUNC_NSL: Status of pib func_nsl_thold: 0 = Run. 1 = Stop.
8	ROX	CLOCK_STATUS_UNIT1_ARY_NSL: Status of pib ary_nsl_thold: 0 = Run. 1 = Stop.
9	ROX	CLOCK_STATUS_UNIT2_FUNC_SL: Status of occ func_sl_thold: 0 = Run. 1 = Stop.
10	ROX	CLOCK_STATUS_UNIT2_FUNC_NSL: Status of occ func_nsl_thold: 0 = Run. 1 = Stop.
11	ROX	CLOCK_STATUS_UNIT2_ARY_NSL: Status of occ ary_nsl_thold: 0 = Run. 1 = Stop.
12	ROX	CLOCK_STATUS_UNIT3_FUNC_SL: Status of unit3 func_sl_thold: 0 = Run. 1 = Stop. Region is unused.
13	ROX	CLOCK_STATUS_UNIT3_FUNC_NSL: Status of unit3 func_nsl_thold: 0 = Run. 1 = Stop. Region is unused.
14	ROX	CLOCK_STATUS_UNIT3_ARY_NSL: Status of unit3 ary_nsl_thold: 0 = Run. 1 = Stop. Region is unused.
15	ROX	CLOCK_STATUS_UNIT4_FUNC_SL: Status of unit4 func_sl_thold: 0 = Run. 1 = Stop. Region is unused.
16	ROX	CLOCK_STATUS_UNIT4_FUNC_NSL: Status of unit4 func_nsl_thold: 0 = Run. 1 = Stop. Region is unused.
17	ROX	CLOCK_STATUS_UNIT4_ARY_NSL: Status of unit4 ary_nsl_thold: 0 = Run. 1 = Stop. Region is unused.

Bits	PCB	Field Mnemonic: Description
18	ROX	CLOCK_STATUS_UNIT5_FUNC_SL: Status of unit5 func_sl_thold: 0 = Run. 1 = Stop. Region is unused.
19	ROX	CLOCK_STATUS_UNIT5_FUNC_NSL: Status of unit5 func_nsl_thold: 0 = Run. 1 = Stop. Region is unused.
20	ROX	CLOCK_STATUS_UNIT5_ARY_NSL: Status of unit5 ary_nsl_thold: 0 = Run. 1 = Stop. Region is unused.
21	ROX	CLOCK_STATUS_PLL_FUNC_SL: Status of PLL func_sl_thold: 0 = Run. 1 = Stop.
22	ROX	CLOCK_STATUS_PLL_FUNC_NSL: Status of PLL func_nsl_thold: 0 = Run. 1 = Stop.
23	ROX	CLOCK_STATUS_PLL_ARY_NSL: Status of PLL ary_nsl_thold: 0 = Run. 1 = Stop.
24	ROX	CLOCK_STATUS_OSCSW_FUNC_SL: Status of oscsw func_sl_thold: 0 = Run. 1 = Stop.
25	ROX	CLOCK_STATUS_OSCSW_FUNC_NSL: Status of oscsw func_nsl_thold: 0 = Run. 1 = Stop.
26	ROX	CLOCK_STATUS_OSCSW_ARY_NSL: Status of oscsw ary_nsl_thold: 0 = Run. 1 = Stop.
27:63	RO	Constant = 0b11111111111111111111111111111111111111

Register Name	*Error Status of CC*
Mnemonic	EH.TPCHIP.TPC.ERROR_STATUS
Address	0000000001030009 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	PCB_WRITE_NOT_ALLOWED: PCB access error: write not allowed.
1	RWX	PCB_READ_NOT_ALLOWED: PCB access error: read not allowed.
2	RWX	PCB_PARITY_ERR_ON_CMD: PCB access error: parity error on PCB command.
3	RWX	PCB_ADDRESS_NOT_VALID: PCB access error: address not valid.
4	RWX	PCB_PARITY_ADDR_ERR: PCB access error: parity error on address.
5	RWX	PCB_PARITY_DATA_ERR: PCB access error: parity error on data.
6	RWX	PCB_PROTECTED_ACCESS_INVALID: PCB access error: protection violation.
7	RWX	PCB_PARITY_SPCIF_ERR: Parity error from special packet interface.
8	RWX	PCB_WRITE_AND_OPCG: PCB write while OPCG in progress.
9	RWX	CLOCK_CMD_CONFLICT: Clock command conflict. Previous command was not yet completed (includes those triggered by tc_sync_clk_stop).

Bits	PCB	Field Mnemonic: Description
10	RWX	SCAN_COLLISION: Scan collision.
11	RWX	OPCG_TRIGGER_ERROR: OPCG triggered while in progress.
12	RWX	OPCG_PARITY_ERROR: OPCG state machine parity error.
13	RWX	PHASE_CNT_CORRUPTED: Phase hold counter corruption detected.
14	RWX	CC_PAR_ERR0: Parity error in one of the registers within the OPCG or sync configuration component.
15	RWX	CC_PAR_ERR1: Parity error in one of the registers within the Clock Multiplexer component.
16	RWX	GPIO_PAR_ERR: Parity error in the GP0 register.
17	RWX	SECURITY_VIOLATION: Security violation when chip protection is active and you try a clock start, pulse, which is invalid at this time.

Register Name	***CC Protect Mode Register***
Mnemonic	EH.TPCHIP.TPC.CC_PROTECT_MODE_REG
Address	00000000010303FE (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	CC_READ_PROTECT_ENABLE: Enable read protection.
1	RW	CC_WRITE_PROTECT_ENABLE: Enable write protection.

Register Name	***Global Checkstop FIR***
Mnemonic	EH.TPCHIP.TPC.XFIR
Address	0000000001040000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	XFIR_IN0: Summary bit(any xstop).
1	RWX	XFIR_IN1: xstop from other chiplets.
2	RWX	XFIR_IN2: Unused.
3	RWX	XFIR_IN3: xstop from pervasive unit.
4	RWX	XFIR_IN4: xstop from occ (405 core).
5	RWX	XFIR_IN5: xstop from MCS0.0 (POWER8 only).
6	RWX	XFIR_IN6: xstop from MCS0.1 (POWER8 only).
7	RWX	XFIR_IN7: xstop from MCS1.0 (POWER8 only).
8	RWX	XFIR_IN8: xstop from MCS1.1 (POWER8 only).
9	RWX	XFIR_IN9: xstop from MCS2.0.
10	RWX	XFIR_IN10: xstop from MCS2.1.
11	RWX	XFIR_IN11: xstop from MCS3.0.
12	RWX	XFIR_IN12: xstop from MCS3.1.
13	RWX	XFIR_IN13: xstop from I/O unit MC Left (POWER8 only).
14	RWX	XFIR_IN14: xstop from I/O unit MC Right.

Bits	PCB	Field Mnemonic: Description
15	RWX	XFIR_IN15: xstop from LPC.
16	RWX	XFIR_IN16: xstop from POWER8 Memory Bus connected to MC0 (POWER8 only).
17	RWX	XFIR_IN17: xstop from POWER8 Memory Bus connected to MC1 (POWER8 only).
18	RWX	XFIR_IN18: xstop from POWER8 Memory Bus connected to MC2.
19	RWX	XFIR_IN19: xstop from POWER8 Memory Bus connected to MC3.
20	RWX	XFIR_IN20: xstop from power management (PMC).
21:25	RWX	XFIR_IN21: Unused.
26	RWX	XFIR_IN26: xstop on debug trigger and local_xstop to recoverable.

Register Name	***Global Recoverable FIR***
Mnemonic	EH.TPCHIP.TPC.RFIR
Address	0000000001040001 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	RFIR_IN0: Local checkstop from the MC units or PMC (informational).
1	ROX	LFIR_RECOV_ERR: Recoverable error from the pervasive unit.
2	ROX	RFIR_IN4: Recoverable from OCC (405 core).
3	ROX	RFIR_IN5: Recoverable from MCS0.0 (POWER8 only).
4	ROX	RFIR_IN6: Recoverable from MCS0.1(POWER8 only).
5	ROX	RFIR_IN7: Recoverable from MCS1.0(POWER8 only).
6	ROX	RFIR_IN8: Recoverable from MCS1.1(POWER8 only).
7	ROX	RFIR_IN9: Recoverable from MCS2.0.
8	ROX	RFIR_IN10: Recoverable from MCS2.1.
9	ROX	RFIR_IN11: Recoverable from MCS3.0.
10	ROX	RFIR_IN12: Recoverable from MCS3.1.
11	ROX	RFIR_IN13: Recoverable from I/O unit MC Left (POWER8 only).
12	ROX	RFIR_IN14: Recoverable from I/O unit MC Right.
13	ROX	RFIR_IN15: Recoverable from LPC.
14	ROX	RFIR_IN16: Unused.
15	ROX	RFIR_IN17: Unused.
16	ROX	RFIR_IN18: Unused.
17	ROX	RFIR_IN19: Unused.
18	ROX	RFIR_IN20: Recoverable from Power management (PMC).
19:23	ROX	RFIR_IN21: Unused.

Register Name	*FIR Mask*
Mnemonic	EH.TPCHIP.TPC.FIR_MASK
Address	0000000001040002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	FIR_MASK_IN0: Mask for XFIR summary bit (any xstop).
1	RW	FIR_MASK_IN1: Mask for XFIR from other chiplets.
2	RW	FIR_MASK_IN2: Unused.
3	RW	FIR_MASK_IN3: Mask for XFIR from pervasive unit error.
4	RW	FIR_MASK_IN4: Mask for OCC (405 core) XFIR and RFIR.
5	RW	FIR_MASK_IN5: Mask for MCS0.0 (POWER8 only) XFIR and RFIR.
6	RW	FIR_MASK_IN6: Mask for MCS0.1 (POWER8 only) XFIR and RFIR.
7	RW	FIR_MASK_IN7: Mask for MCS1.0 (POWER8 only) XFIR and RFIR.
8	RW	FIR_MASK_IN8: Mask for MCS1.1 (POWER8 only) XFIR and RFIR.
9	RW	FIR_MASK_IN9: Mask for MCS2.0 XFIR and RFIR.
10	RW	FIR_MASK_IN10: Mask for MCS2.1 XFIR and RFIR.
11	RW	FIR_MASK_IN11: Mask for MCS3.0 XFIR and RFIR.
12	RW	FIR_MASK_IN12: Mask for MCS3.1 XFIR and RFIR.
13	RW	FIR_MASK_IN13: Mask for I/O unit MC Left (POWER8 only) XFIR and RFIR.
14	RW	FIR_MASK_IN14: Mask for I/O unit MC Right XFIR and RFIR.
15	RW	FIR_MASK_IN15: Mask for LPC XFIR and RFIR.
16	RW	FIR_MASK_IN16: Mask for POWER8 Memory Bus connected to MC0 (POWER8 only) XFIR.
17	RW	FIR_MASK_IN17: Mask for POWER8 Memory Bus connected to MC1 (POWER8 only) XFIR.
18	RW	FIR_MASK_IN18: Mask for POWER8 Memory Bus connected to MC2 XFIR.
19	RW	FIR_MASK_IN19: Mask for POWER8 Memory Bus connected to MC3 XFIR.
20	RW	FIR_MASK_IN20: Mask for power management (PMC) XFIR and RFIR mask.
21:25	RW	FIR_MASK_IN21: Unused.
26	RW	FIR_MASK_IN26: Mask for debug trigger and local xstop to recoverable error.

Register Name	*Special Attention*
Mnemonic	EH.TPCHIP.TPC.SPATTN
Address	0000000001040004 (PCB) 0000000001040005 (PCB1) 0000000001040006 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	ROX	NCX	NCX	SPATTN_IN0: Special attention from OCC complex.
1	ROX	NCX	NCX	SPATTN_IN1: Special attention from memory controller (MC00).
2	ROX	NCX	NCX	SPATTN_IN2: Special attention from memory controller (MC01).
3	ROX	NCX	NCX	SPATTN_IN3: Special attention from memory controller (MC10).

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
4	ROX	NCX	NCX	SPATTN_IN4: Special attention from memory controller (MC11).
5	ROX	NCX	NCX	SPATTN_IN5: Special attention from memory controller (MC20).
6	ROX	NCX	NCX	SPATTN_IN6: Special attention from memory controller (MC21).
7	ROX	NCX	NCX	SPATTN_IN7: Special attention from memory controller (MC30).
8	ROX	NCX	NCX	SPATTN_IN8: Special attention from memory controller (MC31).
9	ROX	NCX	NCX	SPATTN_IN9: Unused special attentions.

Register Name	***Special Attention Mask***
Mnemonic	EH.TPCHIP.TPC.SPA_MASK
Address	0000000001040007 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:9	RW	SPA_MASK_IN: Special attention mask.

Register Name	***Mode Register***
Mnemonic	EH.TPCHIP.TPC.EPS.FIR.MODE_REG
Address	0000000001040008 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	MODE_IN0: Enable clockstop on checkstop.
1	RW	MODE_IN1: Enable clockstop on recoverable.
2	RW	MODE_IN2: Enable clockstop on SPATTN.
3	RW	MODE_IN3: Core-only SPATTN.
4	RW	MODE_IN4: Stop chip TOD on checkstop.
5	RW	MODE_IN5: Stop chip TOD on recoverable.
6	RW	MODE_IN6: Disable propagation of checkstop to other chips.
7	RW	MODE_IN7: Turns xstop on trigger into clkstp on trigger.
8	RW	MODE_IN8: Enable xstop on special attention.
9	RW	MODE_IN9: Mask_direct/local_error.
10	RW	MODE_IN10: Mask_xstop_to_pcb.
11	RW	MODE_IN11: Mask external xstop.
12:15	RW	MODE_IN: Unused.

Register Name	*Local FIR*
Mnemonic	EH.TPCHIP.TPC.LOCAL_FIR
Address	000000000104000A (PCB) 000000000104000B (PCB1) 000000000104000C (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_IN0: CFIR internal parity error.
1	RWX	WOX_AND	WOX_OR	FIR_IN1: Local errors from GPIO (PCB error).
2	RWX	WOX_AND	WOX_OR	FIR_IN2: Local errors from CC (PCB error).
3	RWX	WOX_AND	WOX_OR	FIR_IN3: Local errors from CC (OPCG, parity, scan collision, and so on).
4	RWX	WOX_AND	WOX_OR	FIR_IN4: Local errors from PSC (PCB error).
5	RWX	WOX_AND	WOX_OR	FIR_IN5: Local errors from PSC (parity error).
6	RWX	WOX_AND	WOX_OR	FIR_IN6: Local errors from thermal (parity error).
7	RWX	WOX_AND	WOX_OR	FIR_IN7: Local errors from thermal (PCB error).
8	RWX	WOX_AND	WOX_OR	FIR_IN8: Local errors from thermal (Trip error) critical error.
9	RWX	WOX_AND	WOX_OR	FIR_IN9: Local errors from thermal (Trip error) fatal error.
10	RWX	WOX_AND	WOX_OR	FIR_IN10: Local errors from trace array (error).
11	RWX	WOX_AND	WOX_OR	FIR_IN11: Local errors from trace array (SCOM error)
12:13	RWX	WOX_AND	WOX_OR	FIR_IN12: Local errors from ITR (PCBIF err(12), FMU err(13)).
14	RWX	WOX_AND	WOX_OR	FIR_IN14: Local errors from PCB (error).
15	RWX	WOX_AND	WOX_OR	FIR_IN15: Local errors from I2CM (error).
16:18	RWX	WOX_AND	WOX_OR	FIR_IN16: Local errors from TOD (error).
19	RWX	WOX_AND	WOX_OR	FIR_IN19: Local errors from PORT2 (error).
20	RWX	WOX_AND	WOX_OR	FIR_IN20: SBE indicated error_event0to4 enabled by SBE error mask register bits 5 - 9.
21	RWX	WOX_AND	WOX_OR	FIR_IN21: SBE indicated error_event0to4 enabled by SBE error mask register bits 10 - 14.
22:23	RWX	WOX_AND	WOX_OR	FIR_IN22: Local errors from I2CS (PCBIF err(22), internal logic error(23)).
24	RWX	WOX_AND	WOX_OR	FIR_IN24: Local error from OTP.
25	RWX	WOX_AND	WOX_OR	FIR_IN25: Local error from an Ext trigger.
26	RWX	WOX_AND	WOX_OR	FIR_IN26: Fast xstop FIR error.
27	RWX	WOX_AND	WOX_OR	FIR_IN27: PCB MCAST GRP error.
28	RWX	WOX_AND	WOX_OR	FIR_IN28: PCB parity error.
29:30	RWX	WOX_AND	WOX_OR	FIR_IN29: EECB LPC FIR error.
31:32	RWX	WOX_AND	WOX_OR	FIR_IN31: EECB I2C FIR error.
33:34	RWX	WOX_AND	WOX_OR	FIR_IN33: Local errors from PIBMEM (ECC error(33), bad array address error(34)).
35	RWX	WOX_AND	WOX_OR	FIR_IN35: OTP correctable error.
36:39	RWX	WOX_AND	WOX_OR	FIR_IN36: Unused errors.
40	RWX	WOX_AND	WOX_OR	FIR_IN40: Malfunction alert (local xstop in another chiplet).

Register Name	*Local FIR Mask*
Mnemonic	EH.TPCHIP.TPC.EPS.FIR.LOCAL_FIR_MASK
Address	000000000104000D (PCB) 000000000104000E (PCB1) 000000000104000F (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0:40	RW	WO_AND	WO_OR	LFIR_MASK_IN: Mask for LEM error collection vector.

Register Name	*Local FIR Action0*
Mnemonic	EH.TPCHIP.TPC.EPS.FIR.LOCAL_FIR_ACTION0
Address	0000000001040010 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:40	RW	FIR_ACTION0_IN: Action0 mask.

Register Name	*Local FIR Action1*
Mnemonic	EH.TPCHIP.TPC.EPS.FIR.LOCAL_FIR_ACTION1
Address	0000000001040011 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:40	RW	FIR_ACTION1_IN: Action1 mask.

Register Name	***Multicast Group 1***
Mnemonic	EH.TPCHIP.NET.PCBSLPERV.MULTICAST_GROUP_1
Address	00000000010F0001 (PCB)
Attributes	
Description	Multicast Group Registers 1 – 4 are used to are used to assign chiplets to a specific multicast group within the pervasive connect bus (PCB). Multicast groups make it possible to address more than a single chiplet at a time. They are used to read or write the same resource in multiple chiplets at the same time. **Note:** Multicast groups are initially set up at IPL, but they can be modified at any time by firmware or power management code.

Bits	PCB	Field Mnemonic: Description
0:2	RO	Constant = 0b111
3:5	RW	MULTICAST1_GROUP: Multicast group1 setting. Set this field to a multicast group that this chiplet should be a member of. The chiplet can be assigned to up to four multicast groups by setting this field in the four multicast group registers to the corresponding multicast group numbers. If the chiplet is member of less than four multicast groups, set this field to 0b111 in the multicast group register that is not required. The 0b111 setting indicates multicast group 7; all chiplets are members of multicast group 7 regardless of any multicast register being set to 0b111. 000: Multicast group 0. 001: Multicast group 1. 010: Multicast group 2. 011: Multicast group 3. 100: Multicast group 4 – unused. 101: Multicast group 5 – unused. 110: Multicast group 6 – unused. 111: Multicast group 7.

Register Name	***Multicast Group 2***
Mnemonic	EH.TPCHIP.NET.PCBSLPERV.MULTICAST_GROUP_2
Address	00000000010F0002 (PCB)
Attributes	
Description	Multicast Group Registers 1 – 4 are used to are used to assign chiplets to a specific multicast group within the pervasive connect bus (PCB). Multicast groups make it possible to address more than a single chiplet at a time. They are used to read or write the same resource in multiple chiplets at the same time. **Note:** Multicast groups are initially set up at IPL, but they can be modified at any time by firmware or power management code.

Bits	PCB	Field Mnemonic: Description
0:2	RO	Constant = 0b111
3:5	RW	MULTICAST2_GROUP: Multicast group2 setting. Set this field to a multicast group that this chiplet should be a member of. The chiplet can be assigned to up to four multicast groups by setting this field in the four multicast group registers to the corresponding multicast group numbers. If the chiplet is member of less than four multicast groups, set this field to 0b111 in the multicast group register that is not required. The 0b111 setting indicates multicast group 7; all chiplets are members of multicast group 7 regardless of any multicast register being set to 0b111. 000: Multicast group 0. 001: Multicast group 1. 010: Multicast group 2. 011: Multicast group 3. 100: Multicast group 4 – unused. 101: Multicast group 5 – unused. 110: Multicast group 6 – unused. 111: Multicast group 7.

Register Name	***Multicast Group 3***
Mnemonic	EH.TPCHIP.NET.PCBSLPERV.MULTICAST_GROUP_3
Address	00000000010F0003 (PCB)
Attributes	
Description	Multicast Group Registers 1 – 4 are used to are used to assign chiplets to a specific multicast group within the pervasive connect bus (PCB). Multicast groups make it possible to address more than a single chiplet at a time. They are used to read or write the same resource in multiple chiplets at the same time. **Note:** Multicast groups are initially set up at IPL, but they can be modified at any time by firmware or power management code.

Bits	PCB	Field Mnemonic: Description
0:2	RO	Constant = 0b111
3:5	RW	MULTICAST3_GROUP: Multicast group3 setting. Set this field to a multicast group that this chiplet should be a member of. The chiplet can be assigned to up to four multicast groups by setting this field in the four multicast group registers to the corresponding multicast group numbers. If the chiplet is member of less than four multicast groups, set this field to 0b111 in the multicast group register that is not required. The 0b111 setting indicates multicast group 7; all chiplets are members of multicast group 7 regardless of any multicast register being set to 0b111. 000: Multicast group 0. 001: Multicast group 1. 010: Multicast group 2. 011: Multicast group 3. 100: Multicast group 4 – unused. 101: Multicast group 5 – unused. 110: Multicast group 6 – unused. 111: Multicast group 7.

Register Name	***Multicast Group 4***
Mnemonic	EH.TPCHIP.NET.PCBSLPERV.MULTICAST_GROUP_4
Address	00000000010F0004 (PCB)
Attributes	
Description	Multicast Group Registers 1 – 4 are used to are used to assign chiplets to a specific multicast group within the pervasive connect bus (PCB). Multicast groups make it possible to address more than a single chiplet at a time. They are used to read or write the same resource in multiple chiplets at the same time. **Note:** Multicast groups are initially set up at IPL, but they can be modified at any time by firmware or power management code.

Bits	PCB	Field Mnemonic: Description
0:2	RO	Constant = 0b111
3:5	RW	MULTICAST4_GROUP: Multicast group4 setting. Set this field to a multicast group that this chiplet should be a member of. The chiplet can be assigned to up to four multicast groups by setting this field in the four multicast group registers to the corresponding multicast group numbers. If the chiplet is member of less than four multicast groups, set this field to 0b111 in the multicast group register that is not required. The 0b111 setting indicates multicast group 7; all chiplets are members of multicast group 7 regardless of any multicast register being set to 0b111. 000: Multicast group 0. 001: Multicast group 1. 010: Multicast group 2. 011: Multicast group 3. 100: Multicast group 4 – unused. 101: Multicast group 5 – unused. 110: Multicast group 6 – unused. 111: Multicast group 7.

Register Name	*Hang Pulse Generation Register 0*
Mnemonic	EH.TPCHIP.NET.PCBSLPERV.HANG_PULSE_0_REG
Address	00000000010F0020 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_0: Value of hang pulse 0. Time period = 2^value * (precounter_reg+1) / pcb_freq. The value must be in the range 1 – 34.
6	RW	SUPPRESS_HANG_0: If set to '1', hang pulses are suppressed in the case of an xstop.

Register Name	*Hang Pulse Generation Register 1*
Mnemonic	EH.TPCHIP.NET.PCBSLPERV.HANG_PULSE_1_REG
Address	00000000010F0021 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_1: Value of hang pulse 1. Time period = 2^value * (precounter_reg+1) / pcb_freq. The value must be in the range 1 – 34.
6	RW	SUPPRESS_HANG_1: If set to '1', hang pulses are suppressed in the case of an xstop.

Register Name	*Hang Pulse Generation Register 2*
Mnemonic	EH.TPCHIP.NET.PCBSLPERV.HANG_PULSE_2_REG
Address	00000000010F0022 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_2: Value of hang pulse 2. Time period = 2^value * (precounter_reg+1) / pcb_freq. The value must be in the range 1 – 34.
6	RW	SUPPRESS_HANG_2: If set to '1', hang pulses are suppressed in the case of an xstop.

Register Name	*Hang Pulse Generation Register 3*
Mnemonic	EH.TPCHIP.NET.PCBSLPERV.HANG_PULSE_3_REG
Address	00000000010F0023 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_3: Value of hang pulse 3. Time period = 2^value * (precounter_reg+1) / pcb_freq. The value must be in the range 1 – 34.
6	RW	SUPPRESS_HANG_3: If set to '1', hang pulses are suppressed in the case of an xstop.

Register Name	*Hang Pulse Generation Register 4*
Mnemonic	EH.TPCHIP.NET.PCBSLPERV.HANG_PULSE_4_REG
Address	00000000010F0024 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_4: Value of hang pulse 4. Time period = 2^value * (precounter_reg+1) / pcb_freq. The value must be in the range 1 – 34.
6	RW	SUPPRESS_HANG_4: If set to '1', hang pulses are suppressed in the case of an xstop.

Register Name	*Hang Pulse Generation Register 5*
Mnemonic	EH.TPCHIP.NET.PCBSLPERV.HANG_PULSE_5_REG
Address	00000000010F0025 (PCB)
Attributes	
Description	This hang counter is exclusively used to generate the malfunction alert pulse.

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_5: Value of hang pulse 5. Time period = 2^value * (precounter_reg+1) / pcb_freq. The value must be in the range 1 – 34.
6	RW	SUPPRESS_HANG_5: If set to '1', hang pulses are suppressed in the case of an xstop.

Register Name	*Hang Pulse Generation Register 6*
Mnemonic	EH.TPCHIP.NET.PCBSLPERV.HANG_PULSE_6_REG
Address	00000000010F0026 (PCB)
Attributes	
Description	This hang counter is exclusively used for the heartbeat generation.

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_6: Value of hang pulse 6. Time period = 2^value * (precounter_reg+1) / pcb_freq. The value must be in the range 1 – 34.
6	RW	SUPPRESS_HANG_6: If set to '1', hang pulses are suppressed in the case of an xstop.

Register Name	*Divider for Hang Counter Clock*
Mnemonic	EH.TPCHIP.NET.PCBSLPERV.PRE_COUNTER_REG
Address	00000000010F0028 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PRE_COUNTER: Divider for hang counter clock. Divides clock by n + 1 (default: n = 0).

Register Name	*GP Register 1*
Mnemonic	EH.TPC.GP1
Address	0000000002000001 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	PART1_TC_ABIST_DONE_DC: Nest trace arrays, Bridge units (PBA,INTP,HCABR,PSI,PSIHB,ADU,NHTM), HCAnest ABIST dones. Reset(0).
1	ROX	NX_TC_ABIST_DONE_DC: NX complex ABIST done (the unit must force this bit to 1 at fence). Reset(0).
2	ROX	NOT_USED18: Not used. Reset(0).
3	ROX	PART2_TC_ABIST_DONE_DC: PB, PCIEX*, XB sync, AB sync, MC* (partial good bypass), PCI sync ABIST dones. Reset(0).
4	ROX	NOT_USED19: Not used. Reset(0).
5	ROX	NOT_USED20: Not used. Reset(0).
6	ROX	NOT_USED21: Not used. Reset(0).
7	ROX	MC00_TC_HOST_ATTN: Host attention from MC0.0 for inbound PRD (POWER8 only). Reset(0).
8	ROX	MC01_TC_HOST_ATTN: Host attention from MC0.1 for inbound PRD (POWER8 only). Reset(0).
9	ROX	MC10_TC_HOST_ATTN: Host attention from MC1.0 for inbound PRD (POWER8 only). Reset(0).
10	ROX	MC11_TC_HOST_ATTN: Host attention from MC1.1 for inbound PRD (POWER8 only). Reset(0).
11	ROX	MC20_TC_HOST_ATTN: Host attention from MC2.0 for inbound PRD. Reset(0).
12	ROX	MC21_TC_HOST_ATTN: Host attention from MC2.1 for inbound PRD. Reset(0).
13	ROX	MC30_TC_HOST_ATTN: Host attention from MC3.0 for inbound PRD. Reset(0).
14	ROX	MC31_TC_HOST_ATTN: Host attention from MC3.1 for inbound PRD. Reset(0).
15	ROX	TC_OPCG_DONE_DC: Clock control OPCG done. Reset(0).
16	ROX	FREE_USAGE0: Chiplet specific. Reset(0).
17	ROX	FREE_USAGE1: Chiplet specific. Reset(0).
18	ROX	FREE_USAGE2: Chiplet specific. Reset(0).
19	ROX	FREE_USAGE3: Chiplet specific. Reset(0).
20	ROX	FREE_USAGE4: Chiplet specific. Reset(0).
21	ROX	FREE_USAGE5: Chiplet specific. Reset(0).
22	ROX	FREE_USAGE6: Chiplet specific. Reset(0).
23	ROX	FREE_USAGE7: Chiplet specific. Reset(0).

Register Name	*GP Register 2*
Mnemonic	EH.TPC.GP2
Address	0000000002000002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:23	RW	GPIN_MASKING: GPIN bitwise interrupt masking.

Register Name	*GP Register 4*
Mnemonic	EH.TPC.GP4
Address	0000000002000003 (PCB) 0000000002000006 (PCB1) 0000000002000007 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0:5	RWX	WOX_AND	WOX_OR	TC_PROBE0_SEL_DC: Probe 0 select.
6:7	RWX	WOX_AND	WOX_OR	NOT_USED22: Not used: 0b0. Reset(0b00).
8:13	RWX	WOX_AND	WOX_OR	TC_PROBE1_SEL_DC: Probe 1 select.
14:15	RWX	WOX_AND	WOX_OR	NOT_USED23: Not used: 0b0. Reset(0b00).
16:21	RWX	WOX_AND	WOX_OR	TC_PROBE2_SEL_DC: Probe 2 select.
22:23	RWX	WOX_AND	WOX_OR	NOT_USED24: Not used: 0b0. Reset(0b00).
24:29	RWX	WOX_AND	WOX_OR	TC_PROBE3_SEL_DC: tc_probe3_sel_dc(0:5) / tcnest_sense_sel_dc(0:2). Reset(0b000000).
30	RWX	WOX_AND	WOX_OR	NOT_USED25: Not used: 0b0. Reset(0b0).
31	RWX	WOX_AND	WOX_OR	TC_GP4_OFLOW_FEH_SEL_DC: ABIST: When 1, the fail bit is an overflow. Otherwise, it is a fail. Reset(0b0).
32	RWX	WOX_AND	WOX_OR	NOT_USED26: Not used. Reset(0b0).
33	RWX	WOX_AND	WOX_OR	NOT_USED27: Not used. Reset(0b0).
34	RWX	WOX_AND	WOX_OR	NOT_USED28: Not used.
35	RWX	WOX_AND	WOX_OR	NOT_USED29: Not used. Reset(0b0).
36	RWX	WOX_AND	WOX_OR	NOT_USED30: Not used. Reset(0b0).
37	RWX	WOX_AND	WOX_OR	NOT_USED31: Not used. Reset(0b0).
38	RWX	WOX_AND	WOX_OR	NOT_USED32: Not used. Reset(0b0).
39	RWX	WOX_AND	WOX_OR	NOT_USED33: Not used. Reset(0b0).
40	RWX	WOX_AND	WOX_OR	NOT_USED34: Not used.
41	RWX	WOX_AND	WOX_OR	NOT_USED35: Not used. Reset(0b0).
42	RWX	WOX_AND	WOX_OR	NOT_USED36: Not used. Reset(0b0).
43	RWX	WOX_AND	WOX_OR	NOT_USED37: Not used. Reset(0b0).
44	RWX	WOX_AND	WOX_OR	NOT_USED38: Not used. Reset(0b0).
45	RWX	WOX_AND	WOX_OR	NOT_USED39: Not used. Reset(0b0).
46	RWX	WOX_AND	WOX_OR	NOT_USED40: Not used.
47	RWX	WOX_AND	WOX_OR	NOT_USED41: Not used. Reset(0b0).
48	RWX	WOX_AND	WOX_OR	NOT_USED42: Not used. Reset(0b0).
49	RWX	WOX_AND	WOX_OR	NOT_USED43: Not used. Reset(0b0).
50	RWX	WOX_AND	WOX_OR	NOT_USED44: Not used. Reset(0b0).
51	RWX	WOX_AND	WOX_OR	NOT_USED45: Not used. Reset(0b0).
52	RWX	WOX_AND	WOX_OR	NOT_USED46: Not used.
53	RWX	WOX_AND	WOX_OR	NOT_USED47: Not used. Reset(0b0).
54	RWX	WOX_AND	WOX_OR	NOT_USED48: Not used. Reset(0b0).
55	RWX	WOX_AND	WOX_OR	NOT_USED49: Not used. Reset(0b0).
56	RWX	WOX_AND	WOX_OR	NOT_USED50: Not used. Reset(0b0).

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
57	RWX	WOX_AND	WOX_OR	NOT_USED51: Not used. Reset(0b0).
58	RWX	WOX_AND	WOX_OR	NOT_USED52: Not used.
59	RWX	WOX_AND	WOX_OR	NOT_USED53: Not used. Reset(0b0).
60	RWX	WOX_AND	WOX_OR	NOT_USED54: Not used. Reset(0b0).
61	RWX	WOX_AND	WOX_OR	NOT_USED55: Not used. Reset(0b0).
62	RWX	WOX_AND	WOX_OR	NOT_USED56: Not used. Reset(0b0).
63	RWX	WOX_AND	WOX_OR	NOT_USED57: Not used. Reset(0b0).

Register Name	*PSCOMLE Mode Register*
Mnemonic	EH.TPC.EPS.PSC.PSCOM_MODE_REG
Address	0000000002010000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	ABORT_ON_PCB_ADDR_PARITY_ERROR: Abort on PCB address parity error.
1	RW	ABORT_ON_PCB_WDATA_PARITY_ERROR: Abort on PCB with data parity error.
2	RW	ABORT_ON_DL_RETURN_P0_ERROR: Abort on DL return P0 error.
3	RW	ABORT_ON_DL_RETURN_WDATA_PARITY_ERROR: Abort on DL return with data parity error.
4	RW	WATCHDOG_ENABLE: Watchdog enable.
5:6	RW	SCOM_HANG_LIMIT: 11: 256 10: 512 01: 768 00: 1023.
7	RW	FORCE_ALL_RINGS: Set to logic 1 if all rings should be enabled independent of the ring address.
8	RW	FSM_SELFRESET_ON_STATEVEC_PARITYERROR_ENABLE: FSM self reset on state vector parity error enable. That is, perform an FSM self reset if in an invalid state.
9:11	RW	RESERVED_PSCOM_MODE_LT: Reserved.

Register Name	*Debug Status Register*
Mnemonic	EH.TPC.EPS.PSC.DEBUG_STATUS_REG
Address	0000000002010004 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	LOCAL_TRACE_RUN_IN: Local trace run.
1:2	RWX	TRACE_STATE_LAT: Trace state latch.
3	RWX	TRACE_FREEZE: Trace freeze.
4:5	RWX	COND3_STATE_LT: Condition 3 state latch.
6:7	RWX	COND5_STATE_LT: Condition 5 state latch.
8	RWX	HISTORY_CONDITION0_LT: Condition event history for condtition0_lt.
9	RWX	HISTORY_CONDITION1_LT: Condition event history for condtition1_lt.

Bits	PCB	Field Mnemonic: Description
10	RWX	HISTORY_COND2_3_EVENT: Condition event history for cond2_3_event.
11	RWX	HISTORY_COND2_TIMEOUT: Condition event history for cond2_timeout.
12	RWX	HISTORY_COND4_5_EVENT: Condition event history for cond4_5_event.
13	RWX	HISTORY_COND4_TIMEOUT: Condition event history for cond4_timeout.
14:15	RWX	RESERVED_TCDBG_STATUS_LT: Reserved. Set to zero.

Register Name	*OPCG Control Register 0*
Mnemonic	EH.TPC.OPCG_REG0
Address	0000000002030002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	RUNN_MODE: 1: runn-mode. 0: BIST mode.
1	RWX	OPCG_GO: OPCG go (start sequence).
2	RWX	RUN_SCAN0: Run scan0 (overrides all BIST mode settings except the scan_ratio).
3	RW	SCAN0_MODE: Set PRPGs in scan0_mode but do not run the automatic scan0 sequence.
4:8	RW	SCAN_RATIO: scan_ratio (n = 0 - 15: (n + 1): 1): 16: 24:1 17: 32:1 18: 48:1 19: 64:1 20: 128:1
9	RW	INOP_FORCE_SG: Set SG high during INOP.
10:13	RW	INOP_ALIGN: INOP phase alignment: 0: none 1: 2:1 2: 3:1 3: 4:1 4: 6:1 5: 8:1 6: 12:1 7: 16:1 8: 24:1
14:20	RW	INOP_WAIT: INOP cycle delay (1 - 127).
21:24	RWX	SNOP_ALIGN: BIST mode: SNOP phase alignment (like INOP), runn-mode: loopcnt(0:3).
25:27	RWX	SNOP_WAIT: BIST mode: SNOP cycle delay (0 - 7), runn-mode: loopcnt(4:6).
28:31	RWX	ENOP_ALIGN: BIST mode: ENOP phase alignment (like INOP), runn-mode: loopcnt(7:10).
32:34	RWX	ENOP_WAIT: BIST mode: ENOP cycle delay (0 - 7), runn-mode: loopcnt(11:13).
35	RWX	ENOP_FORCE_SG: BIST mode: Set SG high during ENOP, runn-mode: loopcnt(14).
36:63	RWX	LOOP_COUNT: BIST mode: loop count (l = 1 - 2^28 (about 5 minutes LBIST)), runn-mode: loopcnt(15:42).

Register Name	*OPCG Control Register 1*
Mnemonic	EH.TPC.OPCG_REG1
Address	0000000002030003 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:3	RW	FUNC_CAPT_COUNT: BIST mode: Capture cycles (1 -12) encoded as capture cycle – 1.
4:8	RW	FUNC_CAPT_SEQ01_01F: BIST mode: Capture cycle 1 for fast domain or single mesh support (SL, NSL, ARY, SG, FCE).
9:13	RW	FUNC_CAPT_SEQ02_02F: BIST mode: Capture cycle 2 for fast domain or single mesh support (SL, NSL, ARY, SG, FCE).
14:18	RW	FUNC_CAPT_SEQ03_03F: BIST mode: Capture cycle 3 for fast domain or single mesh support (SL, NSL, ARY, SG, FCE).
19:23	RW	FUNC_CAPT_SEQ04_04F: BIST mode: Capture cycle 4 for fast domain or single mesh support (SL, NSL, ARY, SG, FCE).
24:28	RW	FUNC_CAPT_SEQ05_05F: BIST mode: Capture cycle 5 for fast domain or single mesh support (SL, NSL, ARY, SG, FCE).
29:33	RW	FUNC_CAPT_SEQ06_06F: BIST mode: Capture cycle 6 for fast domain or single mesh support (SL, NSL, ARY, SG, FCE).
34:38	RW	FUNC_CAPT_SEQ07_07F: BIST mode: Capture cycle 7 for fast domain or single mesh support (SL, NSL, ARY, SG, FCE).
39:43	RW	FUNC_CAPT_SEQ08_08F: BIST mode: Capture cycle 8 for fast domain or single mesh support (SL, NSL, ARY, SG, FCE).
44:48	RW	FUNC_CAPT_SEQ09_01FBY2: BIST mode: Capture cycle 1 for slow domain or cycle 9 for single mesh support (SL, NSL, ARY, SG, FCE).
49:53	RW	FUNC_CAPT_SEQ10_02FBY2: BIST mode: Capture cycle 2 for slow domain or cycle 10 for single mesh support (SL, NSL, ARY, SG, FCE).
54:58	RW	FUNC_CAPT_SEQ11_03FBY2: BIST mode: Capture cycle 3 for slow domain or cycle 11 for single mesh support (SL, NSL, ARY, SG, FCE).
59:63	RW	FUNC_CAPT_SEQ12_04FBY2: BIST mode: Capture cycle 4 for slow domain or cycle 12 for single mesh support (SL, NSL, ARY, SG, FCE).

Register Name	*OPCG Control Register 2*
Mnemonic	EH.TPC.OPCG_REG2
Address	0000000002030004 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:11	RW	SCAN_COUNT: BIST mode: Channel scan count (s = 0 - 4095) runn-mode: start_abist match value (0:11).
12:23	RW	MISR_A_VAL: BIST mode: The a value for the MISR aperture, runn-mode: start_abist match value(12:23).
24:35	RW	MISR_B_VAL: BIST mode: The b value for the MISR aperture, runn-mode: start_abist match value(24:35).
36:47	RW	MISR_INIT_WAIT: BIST mode: Delay the MISR aperture. MISRs become active after this number of loops.
48	RW	OPCG_SUPPRESS_EVEN_CLK: OPCG will only create even and not odd clocks. Used for runn to create only one clock in the fast domain. The default is 0.
49:51	RW	OPCG_PAD_VALUE: After setting all DC signals, wait this number of cycle x 16 before applying tholds.
52	RW	USE_F_AND_FDIV2: BIST mode: If 1, use the 8 f and 4 f/2 patterns concurrently. Otherwise, use 1 - 12 local mesh patterns.

Bits	PCB	Field Mnemonic: Description
53	RW	USE_ARY_CLK_DURING_FILL: BIST mode: Fire the nsl_ary_clock during NSL-fill runn-mode. Stop run-n on xstop.
54	RW	SG_HIGH_DURING_FILL: BIST mode: Hold SG high during NSL-fill runn-mode. The OPCG engine controls start_abist (overrides the GP0 setting).
55	RW	RTIM_THOLD_FORCE: Force rtim_thold low when not in test_dc mode (must be 0 at all times).
56	RW	LBIST_SKITTER_CTL: BIST mode: 0: Enable skitter during lbist_ip. 1: Enable skitter when misr_active.
57	RW	MISR_MODE: BIST mode: MISR aperture mode. 0: a-1 to b-1. 1: Start to a and b to end.
58	RW	INFINITE_MODE: Infinite mode.
59:63	RW	NSL_FILL_COUNT: BIST mode: NSL fill count (0 - 31).

Register Name	*OPCG Start Register*
Mnemonic	EH.TPC.OPCG_REG3
Address	0000000002030005 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	OPCG_GO2: OPCG go for broadcast sequences (start sequence).
1	RW	RUN_OPCG_ON_UPDATE_DR: Start the OPCG engine when scan updated (update_dr) is received (set pulse).
2	RW	RUN_OPCG_ON_CAPTURE_DR: Start the OPCG engine when scan updated (capture_dr) is received (set pulse).
3:4	RW	ALIGN_SOURCE_SELECT: 0: Use INOPA setting from opcg_reg0. 1: Use the rising edge of the sync pulse. 2: Use input from the unit (for AVP).
5:7	RW	PRPG_WEIGHTING: prpg_activate: Steer the LBIST pattern generation to increase test coverage. 000: 1/2 (Default). The pseudo-random generator generates 1s 50% of the time and 0s 50% of the time. 001: 1/4. The pseudo-random generator generates 1s 25% of the time and 0s 75% of the time. 010: 1/8. The pseudo-random generator generates 1s 12% of the time and 0s 88% of the time. 011: 1/16. The pseudo-random generator generates 1s 6% of the time and 0s 94% of the time. 100: 1/2. The pseudo-random generator generates 1s 50% of the time and 0s 50% of the time. 101: 3/4. The pseudo-random generator generates 1s 75% of the time and 0s 25% of the time. 110: 7/8. The pseudo-random generator generates 1s 88% of the time and 0s 12% of the time. 111: 15/16. The pseudo-random generator generates 1s 94% of the time and 0s 6% of the time.
8:19	RWX	PRPG_VALUE: Set to 0 for PRPG always on. Otherwise, set to a starting value for the PRPG..
20	RW	EXTEND_INOPW_ENOPW: Extend I/ENOPW. Add 256 cycles if INOP or ENOP is greater than 0. Otherwise, 257 + the maximum INOP or ENOP.
21	RW	EXTEND_SNOPW: Add 256 cycles if SNOP is greater than 0. Otherwise, 257 + the maximum SNOP.
22	RW	FORCE_SG_HIGH_DURING_SNOP: Force SG high during SNOP,
23:31	RW	CHKSW: Reserved for debug switches (keep 0 unless a debug switch is required).
32:43	RW	PRPG_A_VAL: The a value for the PRPG aperture.
44:55	RW	PRPG_B_VAL: The b value for the PRPG aperture.
56	RW	PRPG_MODE: PRPG aperture mode. 0: a-1 to b-1 1: Start to a and b to end.

Bits	PCB	Field Mnemonic: Description
57	RW	SCAN_CLK_USE_EVEN: Generate the scan clock in an odd cycle instead of an even cycle. The default is 0.
58	RWX	AUTO_SCAN0: Will run a full scan0 on the chiplet to clear all data.
59:63	RW	SPARE3: Spares.

Register Name	*Start/Stop of Clocks*
Mnemonic	EH.TPC.CLK_REGION
Address	0000000002030006 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:1	RWX	CLOCK_CMD: Command for clock control: 00: NOP. 01: START. 10: STOP. 11: PULSE (one pulse).
2:3	RO	Constant = 0b00
4	RWX	CLOCK_REGION_PERV: For clock region perv (pervasive).
5	RWX	CLOCK_REGION_UNIT0: For clock region PB (pb/xbs/*br/abs).
6	RWX	CLOCK_REGION_UNIT1: For clock region NX.
7	RWX	CLOCK_REGION_UNIT2: For clock region PCIS.
8	RWX	CLOCK_REGION_UNIT3: For clock region MCL.
9	RWX	CLOCK_REGION_UNIT4: For clock region MCR.
10	RWX	CLOCK_REGION_UNIT5: For clock region unit5; the region is unused.
11	RWX	CLOCK_REGION_PLL: For clock regions PLLMCR, PLLMCL.
12	RWX	CLOCK_REGION_OSCSW: For clock region OSCSW; region is unused.
13:19	RO	Constant = 0b0000000
20	RWX	SEL_THOLD_SL: Select SL tholds.
21	RWX	SEL_THOLD_NSL: Select NSL tholds.
22	RWX	SEL_THOLD_ARY: Select array thold.

Register Name	*Scan Region and Type*
Mnemonic	EH.TPC.SCANSELQ
Address	0000000002030007 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:2	RO	Constant = 0b000
3	RW_WCLRPART	SCANSEL_CLK_VITL: Scan clock region VITL (Vital = Clock).
4	RWX	SCANSEL_CLK_PERV: Scan clock region PERV (Pervasive).
5	RWX	SCANSEL_CLK_UNIT0: Scan clock region PB (PB/XBS/*BR/ABS).

Bits	PCB	Field Mnemonic: Description
6	RWX	SCANSEL_CLK_UNIT1: Scan clock region NX.
7	RWX	SCANSEL_CLK_UNIT2: Scan clock region PCIS.
8	RWX	SCANSEL_CLK_UNIT3: Scan clock region MCL.
9	RWX	SCANSEL_CLK_UNIT4: Scan clock region MCR.
10	RWX	SCANSEL_CLK_UNIT5: Scan clock unit5; region is unused.
11	RWX	SCANSEL_CLK_PLL: Scan clock region PLLMCR, PLLMCL.
12	RWX	SCANSEL_CLK_OSCSW: Scan clock OSCSW region is unused.
13:19	RO	Constant = 0b0000000
20	RW	SCANSEL_FUNC: Scan chain func (functional).
21	RW	SCANSEL_CFG: Scan chain mode (boot configuration and debug configuration).
22	RW	SCANSEL_CCFG_GPTR: Scan chain CCFG / GPTR (Pervasive: CC config Others: GPTR).
23	RW	SCANSEL_REGF: Scan chain REGF (register files).
24	RW	SCANSEL_LBIST: Scan chain LBST (LBIST).
25	RW	SCANSEL_ABIST: Scan chain ABST (ABIST).
26	RW	SCANSEL_REPR: Scan chain REPR (Array Repair).
27	RW	SCANSEL_TIME: Scan chain time (array timing).
28	RW	SCANSEL_BNDY: Scan chain BNDY (boundary I/Os).
29	RW	SCANSEL_FARR: Scan chain FARR (fast array unload).
30	RW	SCANSEL_CMSK: Scan chain CMSK (LBIST channel mask).

Register Name	*Clocks Running*
Mnemonic	EH.TPC.CLOCK_STAT
Address	0000000002030008 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	CLOCK_STATUS_PERV_FUNC_SL: Status of perv func_sl_thold: 0: Run. 1: Stop.
1	ROX	CLOCK_STATUS_PERV_FUNC_NSL: Status of perv func_nsl_thold: 0: Run. 1: Stop.
2	ROX	CLOCK_STATUS_PERV_ARY_NSL: Status of perv ary_nsl_thold: 0: Run. 1: Stop.
3	ROX	CLOCK_STATUS_UNIT0_FUNC_SL: Status of PB (PB/XBS/*BR/ABS) func_sl_thold: 0: Run. 1: Stop.
4	ROX	CLOCK_STATUS_UNIT0_FUNC_NSL: Status of PB (PB/XBS/*BR/ABS) func_nsl_thold: 0: Run. 1: Stop.
5	ROX	CLOCK_STATUS_UNIT0_ARY_NSL: Status of PB (PB/XBS/*BR/ABS) ary_nsl_thold: 0: Run. 1: Stop.

Bits	PCB	Field Mnemonic: Description
6	ROX	CLOCK_STATUS_UNIT1_FUNC_SL: Status of NX func_sl_thold: 0: Run. 1: Stop.
7	ROX	CLOCK_STATUS_UNIT1_FUNC_NSL: Status of NX func_nsl_thold: 0: Run. 1: Stop.
8	ROX	CLOCK_STATUS_UNIT1_ARY_NSL: Status of NX ary_nsl_thold: 0: Run. 1: Stop.
9	ROX	CLOCK_STATUS_UNIT2_FUNC_SL: Status of PCIS func_sl_thold: 0: Run. 1: Stop.
10	ROX	CLOCK_STATUS_UNIT2_FUNC_NSL: Status of PCIS func_nsl_thold: 0: Run. 1: Stop.
11	ROX	CLOCK_STATUS_UNIT2_ARY_NSL: Status of PCIS ary_nsl_thold: 0: Run. 1: Stop.
12	ROX	CLOCK_STATUS_UNIT3_FUNC_SL: Status of MCL func_sl_thold: 0: Run. 1: Stop.
13	ROX	CLOCK_STATUS_UNIT3_FUNC_NSL: Status of MCL func_nsl_thold: 0: Run. 1: Stop.
14	ROX	CLOCK_STATUS_UNIT3_ARY_NSL: Status of MCL ary_nsl_thold: 0: Run. 1: Stop.
15	ROX	CLOCK_STATUS_UNIT4_FUNC_SL: Status of MCL func_sl_thold: 0: Run. 1: Stop.
16	ROX	CLOCK_STATUS_UNIT4_FUNC_NSL: Status of MCR func_nsl_thold: 0: Run. 1: Stop.
17	ROX	CLOCK_STATUS_UNIT4_ARY_NSL: Status of MCR ary_nsl_thold: 0: Run. 1: Stop.
18	ROX	CLOCK_STATUS_UNIT5_FUNC_SL: Status of unit5 func_sl_thold: 0: Run. 1: Stop. The region is unused.
19	ROX	CLOCK_STATUS_UNIT5_FUNC_NSL: Status of unit5 func_nsl_thold: 0: Run. 1: Stop. The region is unused.
20	ROX	CLOCK_STATUS_UNIT5_ARY_NSL: Status of unit5 ary_nsl_thold: 0: Run. 1: Stop. The region is unused.
21	ROX	CLOCK_STATUS_PLL_FUNC_SL: Status of PLLMCR, PLLMCL func_sl_thold: 0: Run. 1: Stop.
22	ROX	CLOCK_STATUS_PLL_FUNC_NSL: Status of PLLMCR, PLLMCL func_nsl_thold: 0: Run. 1: Stop.

Bits	PCB	Field Mnemonic: Description
23	ROX	CLOCK_STATUS_PLL_ARY_NSL: Status of PLLMCR, PLLMCL ary_nsl_thold: 0: Run. 1: Stop.
24	ROX	CLOCK_STATUS_OSCSW_FUNC_SL: Status of OSCSW func_sl_thold: 0: Run. 1: Stop. The region is unused.
25	ROX	CLOCK_STATUS_OSCSW_FUNC_NSL: Status of OSCSW func_nsl_thold: 0: Run. 1: Stop. The region is unused.
26	ROX	CLOCK_STATUS_OSCSW_ARY_NSL: Status of OSCSW ary_nsl_thold: 0: Run. 1: Stop. The region is unused.
27:63	RO	Constant = 0b11111111111111111111111111111111111111111

Register Name	*Error Status of CC*
Mnemonic	EH.TPC.ERROR_STATUS
Address	0000000002030009 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	PCB_WRITE_NOT_ALLOWED: PCB access error; write not allowed.
1	RWX	PCB_READ_NOT_ALLOWED: PCB access error; read not allowed.
2	RWX	PCB_PARITY_ERR_ON_CMD: PCB access error; parity error on PCB command.
3	RWX	PCB_ADDRESS_NOT_VALID: PCB access error; address not valid.
4	RWX	PCB_PARITY_ADDR_ERR: PCB access error; parity error on address.
5	RWX	PCB_PARITY_DATA_ERR: PCB access error; parity error on data.
6	RWX	PCB_PROTECTED_ACCESS_INVALID: PCB access error; protection violation.
7	RWX	PCB_PARITY_SPCIF_ERR: Parity error from special packet interface.
8	RWX	PCB_WRITE_AND_OPCG: PCB write while OPCG in progress.
9	RWX	CLOCK_CMD_CONFLICT: Clock command conflict; the previous command was not yet completed (includes those triggered by tc_sync_clk_stop).
10	RWX	SCAN_COLLISION: Scan collision.
11	RWX	OPCG_TRIGGER_ERROR: OPCG triggered while in progress.
12	RWX	OPCG_PARITY_ERROR: OPCG state machine parity error.
13	RWX	PHASE_CNT_CORRUPTED: Phase hold counter corruption detected.
14	RWX	CC_PAR_ERR0: Parity error in one of the registers within the OPCG or sync configuration component.
15	RWX	CC_PAR_ERR1: Parity error in one of the registers within the Clock Multiplexer component.
16	RWX	GPIO_PAR_ERR: Parity error in GP0 register.
17	RWX	SECURITY_VIOLATION: security_violation. When chip protection is active and you try a clock start, pulse, which is invalid at this time

Register Name	*CC Protect Mode Register*
Mnemonic	EH.TPC.CC_PROTECT_MODE_REG
Address	00000000020303FE (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	CC_READ_PROTECT_ENABLE: Enable read protection.
1	RW	CC_WRITE_PROTECT_ENABLE: Enable write protection.

Register Name	*Global Checkstop FIR*
Mnemonic	EH.TPC.XFIR
Address	0000000002040000 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RWX	XFIR_IN0: Summary bit (any xstop).
1	RWX	XFIR_IN1: xstop from other chiplets.
2	RWX	XFIR_IN2: xstop from the other chip.
3	RWX	XFIR_IN3: xstop from pervasive unit.
4	RWX	XFIR_IN4: xstop from NX DMA ENG FIR (nx0).
5	RWX	XFIR_IN5: xstop from NX CQ FIR (nx1).
6	RWX	XFIR_IN6: xstop from MCD FIR.
7	RWX	XFIR_IN7: xstop from PB EH WEST FIR (pb0).
8	RWX	XFIR_IN8: xstop from PB EH CENT FIR (pb1).
9	RWX	XFIR_IN9: xstop from PB EH EAST FIR (pb2).
10	RWX	XFIR_IN10: Unused.
11	RWX	XFIR_IN11: xstop from service element PSI interface.
12	RWX	XFIR_IN12: xstop from interrupt presenter (INTP).
13	RWX	XFIR_IN13: xstop from power-management processor bus interface (PBA).
14	RWX	XFIR_IN14: xstop from hot cold affinity helper (HCA).
15	RWX	XFIR_IN15: xstop from NX AS FIR (nx_2).
16	RWX	XFIR_IN16: xstop from bridge hot/cold affinity helper (hca).
17	RWX	XFIR_IN17: xstop from PCI Nest FIR (pcis0).
18	RWX	XFIR_IN18: xstop from PCI Nest FIR (pcis1).
19	RWX	XFIR_IN19: xstop from PCI Nest FIR (pcis2).
20	RWX	XFIR_IN20: xstop from NX CXA FIR (nx_3).
21:25	RWX	XFIR_IN21: Unused.
26	RWX	XFIR_IN26: xstop on debug trigger.

Register Name	*Global Recoverable FIR*
Mnemonic	EH.TPC.RFIR
Address	0000000002040001 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	ROX	RFIR_IN0: Local checkstop from NX (informational).
1	ROX	LFIR_RECOV_ERR: Recoverable error from the pervasive unit.
2	ROX	RFIR_IN4: Recoverable from NX DMA ENG FIR (nx0).
3	ROX	RFIR_IN5: Recoverable from NX CQ FIR (nx1).
4	ROX	RFIR_IN6: Recoverable from MCD FIR.
5	ROX	RFIR_IN7: Recoverable from PB EH WEST FIR (pb0).
6	ROX	RFIR_IN8: Recoverable from PB EH CENT FIR (pb1).
7	ROX	RFIR_IN9: Recoverable from PB EH EAST FIR (pb2).
8	ROX	RFIR_IN10: Recoverable from PB1 DSMP errors (foreign fabric).
9	ROX	RFIR_IN11: Recoverable from service element PSI interface.
10	ROX	RFIR_IN12: Recoverable from interrupt presenter (intp).
11	ROX	RFIR_IN13: Recoverable from power-management processor bus interface (PBA).
12	ROX	RFIR_IN14: Recoverable from Hot Cold Affinity Helper (HCA).
13	ROX	RFIR_IN15: Recoverable from NX AS FIR (nx_2).
14	ROX	RFIR_IN16: Recoverable from Bridge Hot Cold Affinity Helper (HCA).
15	ROX	RFIR_IN17: Recoverable from PCI Nest FIR (pcis0).
16	ROX	RFIR_IN18: Recoverable from PCI Nest FIR (pcis1).
17	ROX	RFIR_IN19: Recoverable from PCI Nest FIR (pcis2).
18	ROX	RFIR_IN20: Recoverable from NX CXA FIR (nx_3).
19:23	ROX	RFIR_IN21: Unused.

Register Name	*FIR Mask*
Mnemonic	EH.TPC.FIR_MASK
Address	0000000002040002 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	FIR_MASK_IN0: Mask for XFIR summary bit (any xstop).
1	RW	FIR_MASK_IN1: Mask for XFIR from other chiplets.
2	RW	FIR_MASK_IN2: Mask for XFIR from other chip.
3	RW	FIR_MASK_IN3: Mask for xfir from pervasive unit. XFIR
4	RW	FIR_MASK_IN4: Mask for NX DMA ENG FIR(nx0) XFIR and RFIR.
5	RW	FIR_MASK_IN5: Mask for NX CQ FIR(nx1) XFIR and RFIR.
6	RW	FIR_MASK_IN6: Mask for MCD FIR XFIR and RFIR.
7	RW	FIR_MASK_IN7: Mask for PB EH WEST FIR(pb0) XFIR and RFIR.

Bits	PCB	Field Mnemonic: Description
8	RW	FIR_MASK_IN8: Mask for PB EH CENT FIR(pb1) XFIR and RFIR.
9	RW	FIR_MASK_IN9: Mask for PB EH EAST FIR(pb2) XFIR and RFIR.
10	RW	FIR_MASK_IN10: Mask for PB1 DSMP errors (foreign fabric) XFIR and RFIR.
11	RW	FIR_MASK_IN11: Mask for service element PSI interface XFIR and RFIR.
12	RW	FIR_MASK_IN12: Mask for interrupt presenter (intp) XFIR and RFIR.
13	RW	FIR_MASK_IN13: Mask for power-management processor bus interface (PBA) XFIR and RFIR.
14	RW	FIR_MASK_IN14: Mask for hot cold affinity helper (hca) XFIR and RFIR.
15	RW	FIR_MASK_IN15: Mask for NX AS FIR (nx_2) XFIR and RFIR.
16	RW	FIR_MASK_IN16: Mask for bridge hot cold affinity helper (hca) XFIR and RFIR.
17	RW	FIR_MASK_IN17: Mask for PCI Nest FIR (pcis0) XFIR and RFIR.
18	RW	FIR_MASK_IN18: Mask for PCI Nest FIR (pcis1) XFIR and RFIR.
19	RW	FIR_MASK_IN19: Mask for PCI Nest FIR (pcis2) XFIR and RFIR.
20	RW	FIR_MASK_IN20: Mask for NX CXA FIR (nx_3) XFIR and RFIR.
21:25	RW	FIR_MASK_IN21: Unused.
26	RW	FIR_MASK_IN26: Mask for debug trigger and local xstop to recoverable error.

Register Name	*Special Attention*
Mnemonic	EH.TPC.SPATTN
Address	0000000002040004 (PCB) 0000000002040005 (PCB1) 0000000002040006 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	ROX	NCX	NCX	SPATTN_IN0: Special attention from PB foreign fabric synchronous (DSMP).
1:9	ROX	NCX	NCX	SPATTN_IN1: Unused special attentions.

Register Name	*Special Attention Mask*
Mnemonic	EH.TPC.SPA_MASK
Address	0000000002040007 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:9	RW	SPA_MASK_IN: Special attention mask.

Register Name	*Mode Register*
Mnemonic	EH.TPC.EPS.FIR.MODE_REG
Address	0000000002040008 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0	RW	MODE_IN0: Enable clockstop on checkstop.
1	RW	MODE_IN1: Enable clockstop on recoverable.
2	RW	MODE_IN2: Enable clockstop on SPATTN.
3	RW	MODE_IN3: Core-only SPATTN.
4	RW	MODE_IN4: Stop chip TOD on checkstop.
5	RW	MODE_IN5: Stop chip TOD on recoverable.
6	RW	MODE_IN6: Disable propagation of checkstop to other chips.
7	RW	MODE_IN7: Turns checkstop on trigger into clockstop on trigger.
8	RW	MODE_IN8: Enable checkstop on special attention.
9	RW	MODE_IN9: Mask_direct/local_error.
10	RW	MODE_IN10: Mask_xstop_to_pcb.
11	RW	MODE_IN11: Mask external checkstop.
12:15	RW	MODE_IN: Unused.

Register Name	***Local FIR***
Mnemonic	EH.TPC.LOCAL_FIR
Address	000000000204000A (PCB) 000000000204000B (PCB1) 000000000204000C (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	WOX_AND	WOX_OR	FIR_IN0: CFIR internal parity error.
1	RWX	WOX_AND	WOX_OR	FIR_IN1: Local errors from GPIO (PCB error).
2	RWX	WOX_AND	WOX_OR	FIR_IN2: Local errors from CC (PCB error).
3	RWX	WOX_AND	WOX_OR	FIR_IN3: Local errors from CC (OPCG, parity, scan collision, and so on).
4	RWX	WOX_AND	WOX_OR	FIR_IN4: Local errors from PSC (PCB error).
5	RWX	WOX_AND	WOX_OR	FIR_IN5: Local errors from PSC (parity error).
6	RWX	WOX_AND	WOX_OR	FIR_IN6: Local errors from thermal (parity error).
7	RWX	WOX_AND	WOX_OR	FIR_IN7: Local errors from thermal (PCB error).
8	RWX	WOX_AND	WOX_OR	FIR_IN8: Local errors from thermal (trip error critical).
9	RWX	WOX_AND	WOX_OR	FIR_IN9: Local errors from thermal (trip error fatal).
10	RWX	WOX_AND	WOX_OR	FIR_IN10: Local errors from trace array (error).
11	RWX	WOX_AND	WOX_OR	FIR_IN11: Local errors from trace array (scom error).
15	RWX	WOX_AND	WOX_OR	FIR_IN12: Local errors from I/O bsense (crack detection).
16	RWX	WOX_AND	WOX_OR	FIR_IN16: Fast xstop FIR error.
17:39	RWX	WOX_AND	WOX_OR	FIR_IN17: Unused local errors.
40	RWX	WOX_AND	WOX_OR	FIR_IN40: Malfunction alert (local xstop in another chiplet).

Register Name	*Local FIR Mask*
Mnemonic	EH.TPC.EPS.FIR.LOCAL_FIR_MASK
Address	000000000204000D (PCB) 000000000204000E (PCB1) 000000000204000F (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0:40	RW	WO_AND	WO_OR	LFIR_MASK_IN: Mask for LEM error collection vector.

Register Name	*Local FIR Action0*
Mnemonic	EH.TPC.EPS.FIR.LOCAL_FIR_ACTION0
Address	0000000002040010 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:40	RW	FIR_ACTION0_IN: Action0 mask.

Register Name	*Local FIR Action1*
Mnemonic	EH.TPC.EPS.FIR.LOCAL_FIR_ACTION1
Address	0000000002040011 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:40	RW	FIR_ACTION1_IN: Action1 mask.

Register Name	*Multicast Group 1*
Mnemonic	EH.TPCHIP.NET.PCBSLNEST.MULTICAST_GROUP_1
Address	00000000020F0001 (PCB)
Attributes	
Description	Multicast Group Registers 1 – 4 are used to are used to assign chiplets to a specific multicast group within the pervasive connect bus (PCB). Multicast groups make it possible to address more than a single chiplet at a time. They are used to read or write the same resource in multiple chiplets at the same time. **Note:** Multicast groups are initially set up at IPL, but they can be modified at any time by firmware or power management code.

Bits	PCB	Field Mnemonic: Description
0:2	RO	Constant = 0b111

Bits	PCB	Field Mnemonic: Description
3:5	RW	MULTICAST1_GROUP: Multicast group1 setting. Set this field to a multicast group that this chiplet should be a member of. The chiplet can be assigned to up to four multicast groups by setting this field in the four multicast group registers to the corresponding multicast group numbers. If the chiplet is member of less than four multicast groups, set this field to 0b111 in the multicast group register that is not required. The 0b111 setting indicates multicast group 7; all chiplets are members of multicast group 7 regardless of any multicast register being set to 0b111. 000: Multicast group 0. 001: Multicast group 1. 010: Multicast group 2. 011: Multicast group 3. 100: Multicast group 4 – unused. 101: Multicast group 5 – unused. 110: Multicast group 6 – unused. 111: Multicast group 7.

Register Name	***Multicast Group 2***
Mnemonic	EH.TPCHIP.NET.PCBSLNEST.MULTICAST_GROUP_2
Address	00000000020F0002 (PCB)
Attributes	
Description	Multicast Group Registers 1 – 4 are used to are used to assign chiplets to a specific multicast group within the pervasive connect bus (PCB). Multicast groups make it possible to address more than a single chiplet at a time. They are used to read or write the same resource in multiple chiplets at the same time. **Note:** Multicast groups are initially set up at IPL, but they can be modified at any time by firmware or power management code.

Bits	PCB	Field Mnemonic: Description
0:2	RO	Constant = 0b111
3:5	RW	MULTICAST2_GROUP: Multicast group2 setting. Set this field to a multicast group that this chiplet should be a member of. The chiplet can be assigned to up to four multicast groups by setting this field in the four multicast group registers to the corresponding multicast group numbers. If the chiplet is member of less than four multicast groups, set this field to 0b111 in the multicast group register that is not required. The 0b111 setting indicates multicast group 7; all chiplets are members of multicast group 7 regardless of any multicast register being set to 0b111. 000: Multicast group 0. 001: Multicast group 1. 010: Multicast group 2. 011: Multicast group 3. 100: Multicast group 4 – unused. 101: Multicast group 5 – unused. 110: Multicast group 6 – unused. 111: Multicast group 7.

Register Name	***Multicast Group 3***
Mnemonic	EH.TPCHIP.NET.PCBSLNEST.MULTICAST_GROUP_3
Address	00000000020F0003 (PCB)
Attributes	
Description	Multicast Group Registers 1 – 4 are used to are used to assign chiplets to a specific multicast group within the pervasive connect bus (PCB). Multicast groups make it possible to address more than a single chiplet at a time. They are used to read or write the same resource in multiple chiplets at the same time. **Note:** Multicast groups are initially set up at IPL, but they can be modified at any time by firmware or power management code.

Bits	PCB	Field Mnemonic: Description
0:2	RO	Constant = 0b111

Bits	PCB	Field Mnemonic: Description
3:5	RW	MULTICAST3_GROUP: Multicast group3 setting. Set this field to a multicast group that this chiplet should be a member of. The chiplet can be assigned to up to four multicast groups by setting this field in the four multicast group registers to the corresponding multicast group numbers. If the chiplet is member of less than four multicast groups, set this field to 0b111 in the multicast group register that is not required. The 0b111 setting indicates multicast group 7; all chiplets are members of multicast group 7 regardless of any multicast register being set to 0b111. 000: Multicast group 0. 001: Multicast group 1. 010: Multicast group 2. 011: Multicast group 3. 100: Multicast group 4 – unused. 101: Multicast group 5 – unused. 110: Multicast group 6 – unused. 111: Multicast group 7.

Register Name	***Multicast Group 4***
Mnemonic	EH.TPCHIP.NET.PCBSLNEST.MULTICAST_GROUP_4
Address	00000000020F0004 (PCB)
Attributes	
Description	Multicast Group Registers 1 – 4 are used to are used to assign chiplets to a specific multicast group within the pervasive connect bus (PCB). Multicast groups make it possible to address more than a single chiplet at a time. They are used to read or write the same resource in multiple chiplets at the same time. **Note:** Multicast groups are initially set up at IPL, but they can be modified at any time by firmware or power management code.

Bits	PCB	Field Mnemonic: Description
0:2	RO	Constant = 0b111
3:5	RW	MULTICAST4_GROUP: Multicast group4 setting. Set this field to a multicast group that this chiplet should be a member of. The chiplet can be assigned to up to four multicast groups by setting this field in the four multicast group registers to the corresponding multicast group numbers. If the chiplet is member of less than four multicast groups, set this field to 0b111 in the multicast group register that is not required. The 0b111 setting indicates multicast group 7; all chiplets are members of multicast group 7 regardless of any multicast register being set to 0b111. 000: Multicast group 0. 001: Multicast group 1. 010: Multicast group 2. 011: Multicast group 3. 100: Multicast group 4 – unused. 101: Multicast group 5 – unused. 110: Multicast group 6 – unused. 111: Multicast group 7.

Register Name	***GP3 Register (NA in PERV CPLT)***
Mnemonic	EH.TPCHIP.NET.PCBSLNEST.GP3_REG
Address	00000000020F0012 (PCB) 00000000020F0013 (PCB1) 00000000020F0014 (PCB2)
Attributes	
Description	

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
0	RWX	RWX_WAND	RWX_WOR	CHIPLET_ENABLE: Set if the chiplet is good.
1	RWX	RWX_WAND	RWX_WOR	PCB_EP_RESET: Output ORed to the global EP reset.

Bits	PCB	PCB1	PCB2	Field Mnemonic: Description
2	RWX	RWX_WAND	RWX_WOR	GLSMUX_RESET: Glsmux reset for test purpose and stuck active mesh protection. Note: There are no clocks in the EX if this bit is set.
3	RWX	RWX_WAND	RWX_WOR	PLL_TEST_EN: Put the DPLL in test mode.
4	RWX	RWX_WAND	RWX_WOR	PLLRST: Put the PLL in reset state.
5	RWX	RWX_WAND	RWX_WOR	PLL_BYP: Enable PLL bypass.
6	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN: Scan control for the chiplet vital domain.
7	RWX	RWX_WAND	RWX_WOR	VITAL_SCAN_IN: Scan in for the chiplet vital domain.
8:10	RWX	RWX_WAND	RWX_WOR	Reserved field. (The access type is pcb_access.)
11	RWX	RWX_WAND	RWX_WOR	D_MODE: LCB control signal for vital logic.
12	RWX	RWX_WAND	RWX_WOR	ACT_DIS: LCB control signal for vital logic.
13	RWX	RWX_WAND	RWX_WOR	MPW2: LCB control signal for vital logic.
14	RWX	RWX_WAND	RWX_WOR	MPW1: LCB control signal for vital logic.
15	RWX	RWX_WAND	RWX_WOR	DELAY_LCLKR: LCB control signal for vital logic.
16	RWX	RWX_WAND	RWX_WOR	VITAL_THOLD: Thold for the chiplet vital domain.
17	RWX	RWX_WAND	RWX_WOR	Reserved field. (The access type is pm_access.)
18	RWX	RWX_WAND	RWX_WOR	FENCE_EN: Fencing signal for chiplet.
19:21	RWX	RWX_WAND	RWX_WOR	PM_PI_DECODE: Test override for power management. EX chiplet only.
22	RWX	RWX_WAND	RWX_WOR	RESCLK_DIS: Resonant clocking disable.
23:25	RWX	RWX_WAND	RWX_WOR	Reserved field. (The access type is pm_access.)
26	RWX	RWX_WAND	RWX_WOR	TP_FENCE_PCB: Fence the chiplet from the PCB bus. If set, the PCB slave reports “Chiplet Offline”.
27	RWX	RWX_WAND	RWX_WOR	TP_LVLTRANS_FENCE: Electrical winkel fence, mainly used by power management.
28	RWX	RWX_WAND	RWX_WOR	L3_EDRAM_ENABLE: L3 eDRAM enable. Forced low during EP reset.
29:31	RWX	RWX_WAND	RWX_WOR	Reserved field. (The access type is pm_access.)

Register Name	***Hang Pulse Generation Register 0***
Mnemonic	EH.TPCHIP.NET.PCBSLNEST.HANG_PULSE_0_REG
Address	00000000020F0020 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_0: Value of hang pulse 0. Time period = 2^value * (precounter_reg+1) / pcb_freq. The value must be in the range 1 – 34.
6	RW	SUPPRESS_HANG_0: If set to '1', hang pulses are suppressed in the case of an xstop.

Register Name	***Hang Pulse Generation Register 1***
Mnemonic	EH.TPCHIP.NET.PCBSLNEST.HANG_PULSE_1_REG
Address	00000000020F0021 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_1: Value of hang pulse 1. Time period = 2^value * (precounter_reg+1) / pcb_freq. The value must be in the range 1 – 34.
6	RW	SUPPRESS_HANG_1: If set to 0b1, hang pulses are suppressed in the case of an xstop.

Register Name	*Hang Pulse Generation Register 2*
Mnemonic	EH.TPCHIP.NET.PCBSLNEST.HANG_PULSE_2_REG
Address	00000000020F0022 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_2: Value of hang pulse 2. Time period = 2^value * (precounter_reg+1) / pcb_freq. The value must be in the range 1 – 34.
6	RW	SUPPRESS_HANG_2: If set to '1', hang pulses are suppressed in the case of an xstop.

Register Name	*Hang Pulse Generation Register 3*
Mnemonic	EH.TPCHIP.NET.PCBSLNEST.HANG_PULSE_3_REG
Address	00000000020F0023 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_3: Value of hang pulse 3. Time period = 2^value * (precounter_reg+1) / pcb_freq. The value must be in the range 1 – 34.
6	RW	SUPPRESS_HANG_3: If set to '1', hang pulses are suppressed in the case of an xstop.

Register Name	*Hang Pulse Generation Register 4*
Mnemonic	EH.TPCHIP.NET.PCBSLNEST.HANG_PULSE_4_REG
Address	00000000020F0024 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_4: Value of hang pulse 4. Time period = 2^value * (precounter_reg+1) / pcb_freq. The value must be in the range 1 – 34.
6	RW	SUPPRESS_HANG_4: If set to 0b1, hang pulses are suppressed in the case of an xstop.

Register Name	*Hang Pulse Generation Register 5*
Mnemonic	EH.TPCHIP.NET.PCBSLNEST.HANG_PULSE_5_REG
Address	00000000020F0025 (PCB)
Attributes	
Description	This hang counter is exclusively used to generate the malfunction alert pulse.

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_5: Value of hang pulse 5. Time period = 2^value * (precounter_reg+1) / pcb_freq. The value must be in the range 1 – 34.
6	RW	SUPPRESS_HANG_5: If set to 0b1, hang pulses are suppressed in the case of an xstop.

Register Name	*Hang Pulse Generation Register 6*
Mnemonic	EH.TPCHIP.NET.PCBSLNEST.HANG_PULSE_6_REG
Address	00000000020F0026 (PCB)
Attributes	
Description	This hang counter is exclusively used for the heartbeat generation.

Bits	PCB	Field Mnemonic: Description
0:5	RW	HANG_PULSE_REG_6: Value of hang pulse 6. Time period = 2^value * (precounter_reg+1) / pcb_freq. The value must be in the range 1 – 34.
6	RW	SUPPRESS_HANG_6: If set to '1', hang pulses are suppressed in the case of an xstop.

Register Name	*Divider for Hang Counter Clock*
Mnemonic	EH.TPCHIP.NET.PCBSLNEST.PRE_COUNTER_REG
Address	00000000020F0028 (PCB)
Attributes	
Description	

Bits	PCB	Field Mnemonic: Description
0:7	RW	PRE_COUNTER: Divider for hang counter clock. Divides clock by n + 1 (default: n = 0).

Register Name	*AMR Thread 0*
Mnemonic	EX03.EC.LS.T0_AMR
Address	0000000000000068 (SPR_T0) 00000000000000E8 (SPR_T0_PRIV)
Attributes	
Description	

Bits	SPR_T0	SPR_T0_PRIV	Field Mnemonic: Description
0:63	RW	RW	AMR thread 0.

Register Name	*Thread 4 Memory Hierarchy A Counter*
Mnemonic	EX03.EC.PC.PC_NW.THREAD4_MEM_HIER_A
Address	0000000000000068 (SPRD)
Attributes	
Description	

Bits	SPRD	Field Mnemonic: Description
0:31	RW	Reserved field. (Access type is t4_mem_hier_a.)

Register Name	*AMR Thread 1*
Mnemonic	EX03.EC.LS.T1_AMR
Address	0000000000000069 (SPR_T1) 00000000000000E9 (SPR_T1_PRIV)
Attributes	
Description	

Bits	SPR_T1	SPR_T1_PRIV	Field Mnemonic: Description
0:63	RW	RW	AMR thread 1.

Register Name	*Thread 4 Memory Hierarchy B Counter*
Mnemonic	EX03.EC.PC.PC_NW.THREAD4_MEM_HIER_B
Address	0000000000000069 (SPRD)
Attributes	
Description	

Bits	SPRD	Field Mnemonic: Description
0:31	RW	Reserved field. (Access type is t4_mem_hier_b.)

Register Name	*AMR Thread 3*
Mnemonic	EX03.EC.LS.T3_AMR
Address	000000000000006B (SPR_T3) 00000000000000EB (SPR_T3_PRIV)
Attributes	
Description	

Bits	SPR_T3	SPR_T3_PRIV	Field Mnemonic: Description
0:63	RW	RW	AMR thread 3.

Register Name	*Thread 5 Instruction Completed Counter*
Mnemonic	EX03.EC.PC.PC_NW.THREAD5_INSTRUCTION_COMPLETE
Address	000000000000006B (SPRD)
Attributes	
Description	

Bits	SPRD	Field Mnemonic: Description
0:31	RW	Reserved field. (Access type is t5_instr_cmplt.)

Register Name	*T0 LR*
Mnemonic	EX03.EC.IFU.I.T0_LR
Address	0000000000000040 (SPR_T0)
Attributes	
Description	Link Register for Thread 0.

Bits	SPR_T0	Field Mnemonic: Description
0:63	RW	Link register for thread 0.

Register Name	*Instruction Dispatch Counter*
Mnemonic	EX03.EC.PC.PC_NW.CORE_INSTRUCTION_DISPATCH
Address	0000000000000040 (SPRD)
Attributes	
Description	

Bits	SPRD	Field Mnemonic: Description
0:31	RW	Reserved field. (Access type is core_instr_disp.)

Register Name	*T3 LR*
Mnemonic	EX03.EC.IFU.I.T3_LR
Address	0000000000000043 (SPR_T3)
Attributes	
Description	Link Register for Thread 3

Bits	SPR_T3	Field Mnemonic: Description
0:63	RW	Link register for thread 3.

Register Name	*Workrate Stall Using Busy Counter*
Mnemonic	EX03.EC.PC.PC_NW.CORE_WORKRATE_FINISH
Address	0000000000000043 (SPRD)
Attributes	
Description	

Bits	SPRD	Field Mnemonic: Description
0:31	RW	Reserved field. (Access type is core_workrate_finish.)

Register Name	*T3 CTR*
Mnemonic	EX03.EC.IFU.I.T3_CTR
Address	000000000000004B (SPR_T3)
Attributes	
Description	Count Register for Thread 3

Bits	SPR_T3	Field Mnemonic: Description
0:63	RW	Count register for thread 3.

Register Name	*Memory Hierarchy C Counter LPAR3 Counter*
Mnemonic	EX03.EC.PC.PC_NW.CORE_MEM_C_LPAR3
Address	000000000000004B (SPRD)
Attributes	
Description	

Bits	SPRD	Field Mnemonic: Description
0:31	RW	Reserved field. (Access type is lpar3_mem_hier_c.)

4. Glossary

ABIST	Array built-in self test
AC	Alternating current
ACK	Acknowledgment or acknowledge
AMux	Analog multiplexer
AND write	Current register content is ANDed with write data and the result is stored in the register (access type WO_AND / WOX_AND).
ARE	Address error
ARY	Array
ATPG	Advanced test pattern generator
AVP	Architectural verification program
BCDE	Block copy download engine
BCUE	Block copy upload engine
BI	Burn in
BNDY	Boundary I/Os
BYPASSN	Bypass low active
CC	Congruence class
cmd	Command
cMFSI	Cascade master FSI
CMSK	LBIST channel mask
CP	Chip pump
CPS	Cycle-per-step

CRC	Cyclic-redundancy check
DCM	Dual-chip module
diag	Diagnostic
DMA	Direct memory access
DPLL	Digital phase-locked loop
DRAM	Dynamic random access memory
DSMP	Distributed symmetric multiprocessing
ECC	Error correction code
eDRAM	Embedded dynamic random-access memory
EH	Exclusive access hint
FARR	Fast array unload
fb	Feedback
fbclk	Feedback clock
FIFO	First-in, first-out
FIR	Fault isolation register
fmax	Maximum frequency
fmin	Minimum frequency
FSI	Flexible service interface. FSI covers all resources except FSI slave 0 and slave 1, when addressed from an external service element via the FSI interface.
FSI_BYTE	Flexible service interface byte. FSI_BYTE describes a special byte addressing mode of the FSP.
FSI0	Flexible service interface 0. FSI0 covers resources located in FSI slave 0, when addressed from an external service element via the FSI interface.

FSI1	Flexible service interface 1. FSI0 covers resources located in FSI slave 1, when addressed from an external service element via the FSI interface.
FSM	Finite state machine
Full write	Current register content is replaced by new write data (access type RWX).
func	Functional
GB	Gigabyte
GPIO	General-purpose input/output
GPR	General-purpose register
GPTR	General-purpose test register
HCA	Hot/cold affinity
I2C	Inter-integrated circuit
I2CM	Inter-integrated circuit master
I2CS	Inter-integrated circuit slave
ICP	Interrupt control presenter
IF	Interface
INTP	Interrupt presenter
LBIST	Logical built-in self test
LCB	Log-on control block or local clock buffer
LPC	Low pin count, lowest point of coherency
MC	Memory channel, memory controller
MCD	Memory coherency directory
MFSI	Master FSI

MISR	Multiple input shift register
MSB	Most-significant byte
NACK	Negative acknowledgment
NC	Not connected; that is, the data cannot be written or read by that access.
NCX	Same as NC, but unstable (can be changed functionally)
NOP	No operation
NX	Nest accelerator
OCC	On-chip controller
OCI	On-chip-controller interface. Interface used by power management.
OPB	On-chip peripheral bus
OPCG	On-product clock generator
OR write	Current register content is ORed with write data and the result is stored in the register (access type WO_OR / WOX_OR).
OSC	Oscillator
OSCSW	Oscillator switch
OTPROM	One-time programmable read-only memory
PB	Processor bus
Pb	Lead
PBA	Power management processor bus interface
PCB	Pervasive control bus. PCB is used for read and full write access.
PCB1	Pervasive control bus 1. PCB1 is used for AND write access.
PCB2	Pervasive control bus 2. PCB2 is used for OR write access.

PCBIF	Pervasive control bus interface
PCI	Peripheral Component Interface
PCIe	Peripheral Component Interface Express
PCIEX	Peripheral Component Interface Express
PCLK	Processor clock
PERV	Pervasive
PIB	Pervasive interconnect bus. PIB is used for read and full write access.
PIB1	Pervasive interconnect bus. PIB1 is used for AND write access.
PIB2	Pervasive interconnect bus. PIB2 is used for OR write access.
PLL	Phase-locked loop
PLLREG	Phase-locked loop register
PMC	Performance monitor counter, power management control
PRPG	Pseudo-random pattern generator
PSI	Processor support interface
PSRO	Performance sort-ring oscillator
RDDACK	Read acknowledgment
RDIV	Refclk divide
Refclk	Reference clock
REGF	Register file
REPR	Array repair
RO	Read only. Only used if a bit is tied. Status bits should be ROX.

ROM	Read-only memory
ROX	Same as RO, but unstable. Can be changed functionally.
ROX_CLRPART	Same as ROX, but a read access will clear the bits after they have been accessed.
RW	Readable and writable
RW_WAND	Readable and writable. A write ANDs written data with existing data and stores the result.
RW_WCLEAR	Readable and writable. A write of a ‘1’ clears the bit. A write of a ‘0’ does nothing.
RW_WCLRPART	Readable and writable. Any write to the address clears the bits regardless of value.
RW_WOR	Readable and writable. A write ORs written data with existing data and stores the result.
RW_WSETPART	Readable and writable. Any write to the address sets the bits regardless of value.
RWX	Same as RW, but unstable. Can be changed functionally.
RWX_WAND	Same as RW_WAND, but unstable. Can be changed functionally.
RWX_WCLEAR	Same as RW_WCLEAR, but unstable. Can be changed functionally.
RWX_WCLRPART	Same as RW_WCLRPART, but unstable. Can be changed functionally.
RWX_WOR	Same as RW_WOR, but unstable. Can be changed functionally.
RWX_WSETPART	Same as RW_WSETPART, but unstable. Can be changed functionally.
RX	Receive
SBE	Self-boot engine
SCM	Single-chip module
SCOM	Serial communications. SCOM is used for read and full write access.
SCOM1	Serial communications 1. SCOM1 is used for AND write access.

SCOM2	Serial communications 2. SCOM2 is used for OR write access.
SCOMFSI0	Scan communications to flexible service interface 0. SCOMFSI0 covers resources located in FSI slave 0, when addressed from the PIB.
SCOMFSI1	Scan communications to flexible service interface 1. SCOMFSI1 covers resources located in FSI slave 1, when addressed from the PIB.
SEL	Select
Slvrst	Slave reset
SPATTN	Special attention
SPR	Special-purpose register
SPRD	Special-purpose register data
SPRD_T0	Special-purpose register thread 0
SPRD_T1	Special-purpose register thread 1
SPRD_T3	Special-purpose register thread 3
SPRD_T5	Special-purpose register thread 5
SPS	Steps per sync, sleep Pstate
TFMR	Time Facility Management Register
TOD	Time of day
TX	Transmit
UE	Uncorrectable error
VCO	Voltage controlled oscillator
VIO	Voltage I/O
Vref	Voltage reference
wdata	Write data

WO	Same as RW, but bits are write-only.
WO_AND	Same as RW_WAND, but bits are write-only.
WO_CLEAR	Same as RW_WCLEAR, but bits are write-only.
WO_CLRPART	Same as RW_WCLRPART, but bits are write-only.
WO_n_mP	Write only pulsed. A write of ‘1’ creates a pulse for a minimum of n register clocks and maximum of m register clocks. A read returns ‘0’.
WO_nP Write	Only pulsed. A write of ‘1’ creates a pulse for n register clocks. A read returns ‘0’.
WO_OR	Same as RW_WOR, but bits are write-only.
WO_SETPART	Same as RW_WSETPART, but bits are write-only.
WOF	Who's on first?
WOX	Same as WO, but unstable. Can be changed functionally.
WOX_AND	Same as WO_AND, but unstable. Can be changed functionally.
WOX_CLEAR	Same as WO_CLEAR, but unstable. Can be changed functionally.
WOX_CLRPART	Same as WO_CLRPART, but unstable. Can be changed functionally.
WOX_n_mP	Same as WO_n_mP, but unstable. Can be changed functionally.
WOX_nP	Same as WO_nP, but unstable. Can be changed functionally.
WOX_OR	Same as WO_OR, but unstable. Can be changed functionally.
WOX_SETPART	Same as WO_SETPART, but unstable. Can be changed functionally.
XER	Fixed-Point Exception Register
XFIR	X Fault Isolation Register
XOR	Exclusive OR