POWER8 Processor Datasheet for the Single-Chip Module Revision Level DD 2.X

Version 1.1

Advance

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Revision Log

Each release of this document supersedes all previously released versions. The revision log lists all significant changes made to the document since its initial release. In the rest of the document, change bars in the margin indicate that the adjacent text was modified from the previous release of this document.

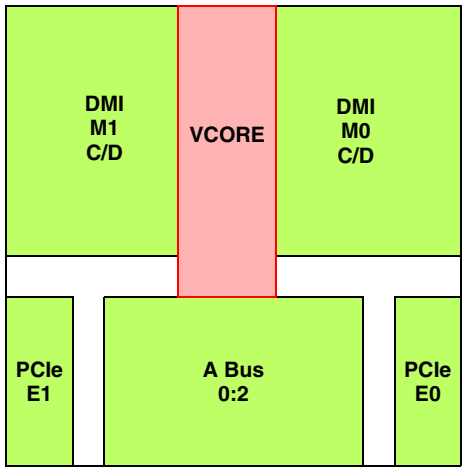
Revision Date	Description
June 17, 2014	Version 1.1. • Removed table previously known as *Table 5-4. Voltage Control Signals*. • Removed table previously known as *Table 5-6. POWER8 Memory Buffer Signals*. • Removed NC signals from the following tables: *Table 5-3 Voltage Signals* on page 29, *Table 5-5 Oscillator Switch Controls* on page 29, *Table 5-6 PLL Signals* on page 30, *Table 5-8 Test Signals* on page 30, *Table 5-12 FSI Signals* on page 32, *Table 5-13 SPI Signals* on page 32, *Table 5-15 Time of Day and Bus Synchronization Signals* on page 33, *Table 5-16 Thermal Diodes and Monitor Signals* on page 33, *Table 5-17 DMI Signals* on page 34. • Added *Section 6.3.3 FSI ac Specifications* on page 48. • Added *Section 6.3.4 SPI ac Specifications* on page 49.
April 22, 2014	Version 1.0 (initial version).

1. Introduction

This datasheet describes the IBM® POWER8™ single-chip module (SCM), which consists of a single POWER8 processor. Each processor can have up to 12 cores enabled. The 12-core POWER8 processor is designed for use in servers and large-cluster systems. It uses IBM's CMOS 22 nm SOI technology with 15 metal layers. Each core has eight threads using simultaneous multithreading (SMT8). The SMT is dynamically tunable, so that each core can have one, two, four, or eight threads.

Figure 1-1 illustrates the POWER8 pinout diagram.

Figure 1-1. POWER8 Pinout Map



1.1 Processor Feature Summary

The POWER8 processor consists of the following main components:

- Twelve POWER8 chiplets containing a POWER8 core, an L2 cache, and an L3 cache.
- One on-chip accelerator engine
  - On chip: compression, encryption, data move initiated by the hypervisor
  - In core: user invocation encryption (AES, SHA)
- Two memory controllers that support the POWER8 Memory Buffer chip
- Processor bus interconnect
- Interface controllers that support three 1-byte differential A-buses
- The interface controllers support the following interfaces:
  - Four differential memory buses (M0 - M3)
  - Three inter-node SMP buses (A0 - A2)
  - Configurable PCIe 3.0 buses (one 16× and one 8× or three 8×)
- Power management
- Pervasive functions

1.2 Supported Technologies

The POWER8 processor supports the following technologies:

- Power ISA Book I, II, and III version 2.07
- PowerPC Architecture Platform Requirements (PAPR+), Version 2.1
- IEEE P754-2008 for binary and decimal floating-point compliant
- Big-endian, little-endian, strong-ordering support extension
- 50-bit real address, 68-bit virtual address

1.3 Interfaces

The primary service interface to the POWER8 processor is the flexible service interface (FSI) that runs at 166 MHz. See *Section 3.1 Flexible Service Interface* on page 17 for more information.

1.4 Power Management Support

Key features of the POWER8 processor in the SCM are:

- Hypervisor directed power change requests using the Pstate mechanism
- Sensors
  - Digital thermal sensor (DTS2) ±5°C
  - Off-chip analog thermal diode ±1 - 2°C
  - Dedicated performance, microarchitecture, and event counters
- Accelerators
  - On-chip PowerPC 405 for real-time frequency and voltage modification
  - On-chiplet hardware assist (automated core chiplet management)
  - On-chip power management controls
    - Automated communications to the voltage regulation modules (VRMs)
    - Voltage and frequency sequencers for automated Pstate and idle state support
- Actuators
  - Per chiplet frequency control through the DPLL
  - Architected idle states: nap, sleep, and winkle; each with increasing power savings capability (and latency)
  - SPR Power Management Control Registers (PMCR, PMICR, PMSR) for hypervisor support
- Memory/DIMM throttling for memory subsystem power and thermal management

1.5 Thermal Specification

Thermal junction temperature (T_J) is measured by digital thermal sensors located on the chip. There are four sensors per core that are averaged. The specified T_J is the worst case of these averages, or the hottest core average. The maximum T_J is not allowed to exceed 85°C. The average T_J, at which the reliability is calculated, is 70°C. Margin does not need to be applied when measuring against the worst case specification because, the chip is sorted using the same thermal sensors. The digital thermal sensor has an absolute accuracy of ±5% and can be read out in Celsius (°C).

1.6 Signals

Section 5 Signals Descriptions on page 27 describes the POWER8 processor signals.

1.7 Electrical

Section 6 Electrical Characteristics on page 39 discusses the dc and ac electrical characteristics of the POWER8 processor in the SCM.

1.8 Package Support

Section 7 Mechanical Specifications on page 51 describes the POWER8 module SCM features and pin list.

1.9 Processor Version Register

The POWER8 processor has the following Processor Version Register (PVR) values for the respective design revision levels.

Table 1-1. POWER8 Processor Version Register

POWER8 Design Revision Level	POWER8 PVR
DD 2.0	x‘004D0200’

1.10 Marking Specification

The POWER8 processor SCM marking specification can be found on the OpenPOWER Connect website.

1.11 Conventions

This section explains the number, bit field, instruction, and signal conventions that are used in this document.

1.11.1 Representation of Numbers

Numbers are generally shown in decimal format, unless designated as follows:

- Hexadecimal values are preceded by an “x” and enclosed in single quotation marks.
  For example: x‘0A00’.
- Binary values in sentences are shown in single quotation marks.
  For example: ‘1010’.

Note: A bit value that is immaterial, which is called a “don't care” bit, is represented by an “x.”

1.11.2 Bit Significance

The bit on the left represents the most significant bit of a field. The bit on the right represents the least significant bit of a field. For example, in CTL[0:31], 0 is the most significant bit.

1.11.3 Other Conventions

- Instruction mnemonics are shown in lowercase, bold text. For example: **tlbivax**.
- I/O signal names are shown in uppercase.
- The notation [*] indicates all bits in a field or register.

An underscore indicates that a definition is displayed when you hoover your cursor over the underscored term.

1.12 Related Documents and Models

The following documents can be helpful when reading this specification. Contact your IBM representative to obtain any documents that are not available through IBM Customer Connect.

- *POWER8 Processor User’s Manual for the Single-Chip Module*
- *POWER8 Errata Notice*
- *POWER8 Memory Buffer Datasheet*
- *POWER8 Memory Buffer User’s Manual*
- *POWER8 Power Architecture Platform Reference (PAPR) Databook (Version 2.1)*
- *Power ISA User Instruction Set Architecture (Version 2.07)*
- *Power ISA Virtual Instruction Set Architecture (Version 2.07)*
- *Power ISA Operating Environment Architecture - Server Environment (Version 2.07)*
- *For the Development of an Electrostatic Discharge Control Program for – Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices) (ANSI/ESD S20.20-2007)*
- *For the Protection of Electrostatic Discharge Susceptible Items - Packaging Materials for ESD Sensitive Items (ANSI/ESD S541-2008)*

2. Technologies

This section provides a high-level overview of the technologies implemented in the POWER8 processor.

2.1 General Parameters

Table 2-1 lists general parameters for the POWER8 processor.

Table 2-1. POWER8 SCM Technology

Feature	Description
Technology	22 nm silicon-on-insulator (SOI), 15 metal layers
Die Size	675 mm^2
Chip Package (SCM)	See *Table 7-1 SCM Features* on page 51 for details.
Signal I/O	2296
Frequency Range (nominal)	3.425 - 3.758 GHz
Power	190 W

3. Interfaces

3.1 Flexible Service Interface

The primary service interface to the POWER8 processor is the flexible service interface (FSI), a serial interface that runs at 166 MHz. The POWER8 processor provides the following service interfaces:

- Two FSI slaves.
- Four FSI masters for communicating with the memory controller and POWER8 Memory Buffer chip.
- Four FSI masters for communicating with other POWER8 chips in the system. One POWER8 chip is defined as the master and is responsible for initializing the other POWER8 chips over these FSI interfaces.
- One serial peripheral interconnect (SPI) master for controlling the voltage regulators.
- One SPI master for on-chip controller (OCC) management.
- One LPC bus for connecting to the BMC.
- One I^2C slave that can be used in place of FSI slaves so that an industry standard BMC can be used
- Two SEEPROM interfaces to load the on-chip SEEPROMs. This path can be disabled for secure boot reasons.
- Two I^2C masters for controlling LEDs, PCIe cards, and so on. The I^2C masters can be manipulated from the OCC or hostboot code.
- Two high-speed SPI master buses for off-chip VRM control and voltage slewing.
- One time-of-day clock.

3.2 Supported Processor Interfaces

This section gives an overview of the physical layer and on-chip initialization provided by POWER8 processor.

The POWER8 processor supports the following types of driver and receivers:

- A Bus: High-speed differential at 6.4 Gb/s for memory interface
- Memory I/O: High-speed differential at 9.6 Gb/s for memory interface

Table 3-1 lists the requirements relative to the operational mode definitions.

Table 3-1. Interface Operational Mode Definitions

Mode Name	Definition
Initialization	The act of aligning and locking the data eye and bit lanes plus additional deltas relative to re-alignment and re-locking.
Functional	Passing workload data and maintaining signal integrity post-initialization.
Power Saving	All related capabilities for minimizing unused and idle lane power consumption.
Test	Capabilities related to hardware manufacturability.
Diagnostic	Bringup lab characterization of interface performance capabilities.

3.2.1 Bus Highlights

Table 3-2 highlights the differences for the A bus and memory I/O bus. See the *POWER8 Processor User's Manual for the Single-Chip Module* for additional information.

Table 3-2. A Bus and Memory Bus Highlights

Frequency	A Bus	Memory Bus
	6.4 Gb/s	9.6 Gb/s
Initialization Mode Requirement	6.4 - 4.8 Gb/s	9.6 - 8.0 Gb/s
Spare Lane Detect	Data failover One signal total per bus per port	Data failover Two signals total per bus per port
Functional Mode Specification	6.4 - 4.8 Gb/s	9.6 - 8.0 Gb/s
Power-Saving Mode Requirement	No power-saving mode support	No power-saving mode support
Test Mode Requirement	6.4 - 4.8 Gb/s[1]	9.6 - 8.0 Gb/s[1]
Driver Features	4:1 data serialization at 6.4 Gb/s Programmable drive strengths Impedance calibration Post cursor FFE levels and amplitude margining Feed forward equalization Precompensation dc test mode	4:1 data serialization at 9.6 Gb/s Programmable drive strengths Impedance calibration Post cursor FFE levels and amplitude margining Feed forward equalization Precompensation dc test mode
Receiver Features	Input descrambler 4:1 de-serializer Phase interpolator dc offset calibration	Input descrambler 4:1 de-serializer Phase interpolator dc offset calibration DFE-1 (1-tap decision feedback equalizer)

1. Subject to PLL range limitations and a test frequency of 200 MHz.

3.3 PCI Express Controller

The PCI Express controller (PEC) bridges between the internal processor bus and the high-speed serial (HSS) links that drive the PCI Express I/O. The PEC acts as a processor bus master on behalf of the PCI Express port, converting inbound memory read and write packets into processor bus DMA traffic. The PEC also acts as a processor bus slave, transferring processor load and store commands to the PCI Express devices attached to the port.

3.3.1 Specification Compliance

The PEC is compliant with the following IBM and industry standards:

- POWER Architecture Platform Requirements (PAPR+) Specification, Version 2.1
- I/O Design Architecture v2
- PCI Express Base Specification Revision 3.0, v0.71

3.3.2 PEC Feature Summary

- PCI Express Generation 3 root complex (RC)
  - Backwards compatible with generation 1 and generation 2
  - 2.5, 5.0, and 8 GT/s signalling rate
- Thirty-two PCIe I/O lanes configurable to three independent root complexes
- Each root complex has 256 partitionable endpoints (PE) for LPAR support
- TCE-based address translation for DMA requests.
  - 50-bit address support
  - Translation validation table based on PCI routing ID
- 2048 MSI interrupts per RC
- Eight LSI interrupts per RC
- IBM enhanced error handling (EEH) support
- Processor bus cache-inhibited space segmented by PEC
  - PCI 32-bit memory space segmented into 256 domains by the memory domain table
  - PCI 64-bit memory space segmented by 16 M64 BARs with 16 segments each
- Support for ECRC
- Support for lane wrapping
- Support for PCIe atomic operations and TLP hints

3.3.3 Supported Configuration

The 32 lanes of HSS I/O can be configured to support three independent PCIe buses. *Table 3-3* describes the maximum lane allocation. In addition to supporting PCI operations, the HSS I/O can be allocated for use by the processor bus SMP interface.

Table 3-3. Supported I/O Configurations

PEC0	PEC1	PEC2
16	16	Unused
16	8	8
8	16	Unused
8	8	8
Unused	16	Unused
Unused	8	8

3.3.4 PCIe Bus

The POWER8 SCM has a total of 32 PCIe Gen3 lanes. Each POWER8 die provides one ×16 and one ×8 lane. The ×16 can bifurcate into two ×8 lanes. The PCIe Gen3 bandwidth is 1 GB/s per lane. The lanes can be reversed for easier routing if required. The polarity can also be reversed on a lane-by-lane basis.

If a slot is hardcoded to be present, such as feeding a PCIe switch, tie the PRSNT signal to ground with 50 Ω. If the $\overline{\text{PRSNT}}$ signal is unused, such as PE_PIN_P_CT_E1_PRSNT0_B in ×16 mode, tie $\overline{\text{PRSNT}}$ to 1.1 V with 50 Ω..

$\overline{\text{PERST}}$ must have a 4.7 KΩ to 3.3 V. If $\overline{\text{PERST}}$ is unused, leave it floating.

Table 3-4. Chip P0

Chip	Interface	Mode	Pins	
P0	E1	×16	Data Lanes	PE_PIN_P_E1_CK0_DAT_[00:07]_[P/N] PE_PIN_P_E1_CK1_DAT_[00:07]_[P/N]
			Clocks	PE_CT_P_PIN_E1_SLOT_CLK0_[P/N] PE_CT_P_PIN_E1_SLOT_CLK1_[P/N]
			Reset	$\overline{\text{PE_CT_P_PIN_E1_PERST0_B}}$ $\overline{\text{PE_CT_P_PIN_E1_PERST1_B}}$
			Present	$\overline{\text{PE_PIN_P_CT_E1_PRSNT0_B}}$ $\overline{\text{PE_PIN_P_CT_E1_PRSNT1_B}}$
P0	E1	×8	Data Lanes	PE_PIN_P_E1_CK0_DAT_[00:07]_[P/N]
			Clocks	PE_CT_P_PIN_E1_SLOT_CLK0_[P/N] PE_CT_P_PIN_E1_SLOT_CLK1_[P/N]
			Reset	$\overline{\text{PE_CT_P_PIN_E1_PERST0_B}}$ $\overline{\text{PE_CT_P_PIN_E1_PERST1_B}}$
			Present	$\overline{\text{PE_PIN_P_CT_E1_PRSNT0_B}}$ $\overline{\text{PE_PIN_P_CT_E1_PRSNT1_B}}$
P0	E1	×8	Data Lanes	PE_PIN_P_E1_CK1_DAT_[00:07]_[P/N]
			Clocks	PE_CT_P_PIN_E1_SLOT_CLK0_[P/N] PE_CT_P_PIN_E1_SLOT_CLK1_[P/N]
			Reset	$\overline{\text{PE_CT_P_PIN_E1_PERST0_B}}$ $\overline{\text{PE_CT_P_PIN_E1_PERST1_B}}$
			Present	$\overline{\text{PE_PIN_P_CT_E1_PRSNT0_B}}$ $\overline{\text{PE_PIN_P_CT_E1_PRSNT1_B}}$
P0	E0	×16	Data Lanes	PE_PIN_P_E0_CK0_DAT_[00..07]_[P/N]
			Clocks	PE_CT_P_PIN_E0_SLOT_CLK0__[P/N]
			Reset	PE_CT_P_PIN_E0_PERST0_B PE_CT_P_PIN_E0_PERST1_B
			Present	PE_PIN_P_CT_E0_PRSNT0_B PE_PIN_P_CT_E0_PRSNT1_B

3.4 SMP Bus

The POWER8 SCM brings out a total of three 2-byte A buses (A0 - A2). The differential A bus runs at 6.4 Gb/s. For a two-socket system, it is recommended connecting the two sockets with at least two of the three A buses. An A bus port of socket 1 can go to any A bus port of socket 2 in a two-socket system.

3.5 DMI Bus

The POWER8 SCM brings out a total of four DMI interfaces at 9.6 Gb/s. The total pin bandwidth of one DMI interface is 28.8 GB/s.

See the *POWER8 Memory Buffer Datasheet* for bandwidth requirements.

4. Power Management

The POWER8 processor uses a number of the more traditional dynamic power-saving techniques, such as clock gating latches and arrays when they are not needed, in an effort to reduce peak power and therefore, thermal design point power (TDP), as well as the ability to dynamically power gate (turn the power off to) individual cores or full core chiplets when the core is not being used.

The POWER8 processor uses an adaptive power management technique to reduce average power, collectively known as EnergyScale™, proactively taking advantage of variations in workload, environmental condition, and overall system utilization. This, coupled with a policy direction from the customer and feedback from the hypervisor/operating system that is running on the machine, is used to determine modes of operation and the best power and performance trade-off to implement during runtime to meet customer goals and achieve the best possible performance.

4.1 Power Gating and On-Chip, Per-Core Voltage Regulation

Offering competitive chip and system designs requires the capability to dynamically adjust power consumption and performance levels to meet the needs of changing workloads. The POWER8 processor offers industry leading features to achieve this goal.

During idle periods, each chiplet has the ability to individually power gate or ‘turn off’ the supply to either the core or to both the core and the associated L3 cache region to reduce chiplet idle power. The gating header in the POWER8 processor is driven to an elevated voltage when OFF using an on-chip charge pump. This technique increases the leakage power reduction, bringing the total dc power reduction achieved by power gating to 50 - 100x. As a result, the power-gated power consumption should be < 1% of the chiplet idle power.

Power gating can also be used to virtually eliminate the parasitic leakage power of de-configured cores in a partial-good product offering by leaving the headers for un-configured cores in an always gated state.

The idle power saved by power gating can be used to boost the frequency of the remaining operational cores. Using this technique, the nominal frequency of operating four cores can exceed the 12-core operating frequency by almost 30%.

4.2 Efficient Power Supply Over-Subscription Capability

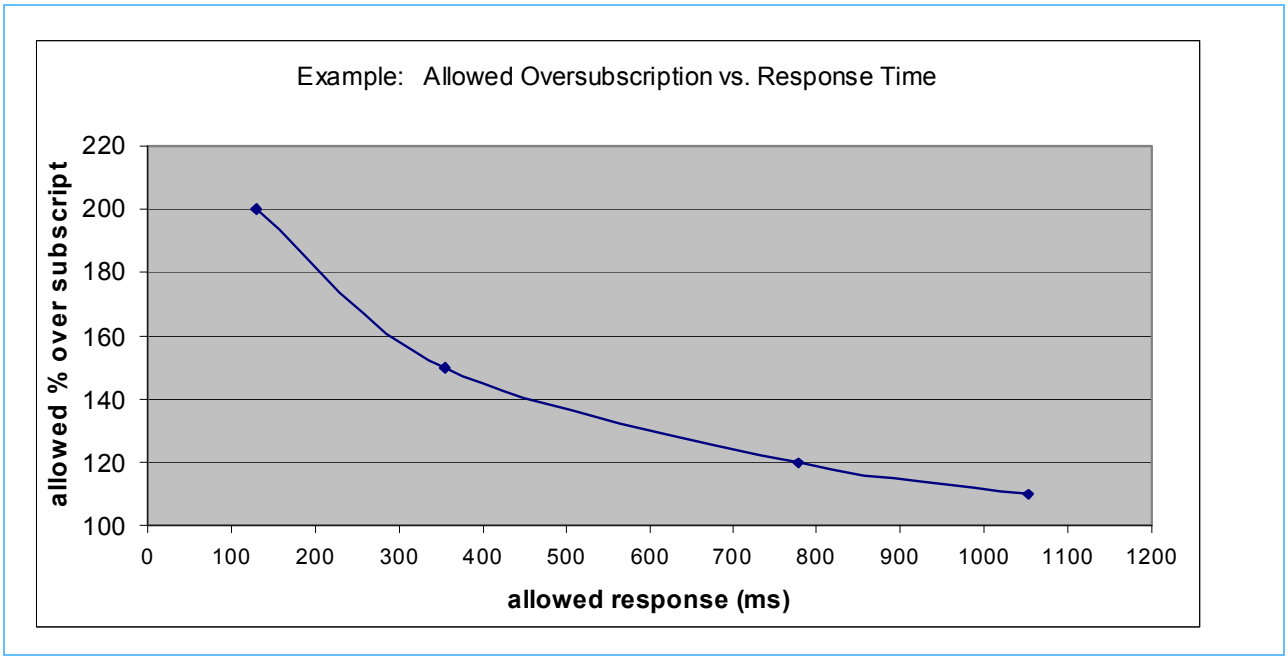
System bulk power supplies redundantly deliver worst-case power, which is significantly more power than is typically consumed. Typical workloads, parts, and environments are much less power hungry than the worst case. Also, power delivery failure is very uncommon.

This excess power capacity can be converted into performance by using over-subscription. By over-subscribing the power supply, the processor is allowed to run at voltages and frequencies that exceed the power limit of the system under a worst case workload and failure of one of the redundant supplies.

Robust system operation must be maintained in spite of over-subscription. To do this, the processor must have the capability to throttle back power quickly enough to avoid an over-current condition in the remaining bulk power supply in case of a failure in the redundant supply or a sudden power spike.

POWER8 systems increase over-subscription capabilities to 1.5x resulting in performance gains. The fundamental limit to power supply oversubscription is the circuit breakers in the utility or UPS when the redundant power fails. The system must be able to throttle back to consuming power less than the non-oversubscribed limit before the EXP(Current) × Time limit of the breaker is violated. *Figure 4-1* shows a representative curve of allowed oversubscription versus response time.

Figure 4-1. Oversubscriptions versus Response Time



To improve response time, the POWER8 processor adds a dedicated C4 pin that can directly signal a power-supply error to the on-chip controller (OCC).

The OCC engine can then use its internal power-actuation capabilities to rapidly reduce power. The POWER8 processor offers the following forms of power reduction:

- The OCC can force a halt in the fetch or issue of instructions to significantly reduce ac power within approximately 10 cycles.
- The OCC can use the DPLL to reduce frequency at a rate of approximately 25 MHz/µs. The ac power reduces linearly with the frequency reduction.

Based on these capabilities, the POWER8 processor can throttle its power to a small fraction of nominal operating power in less than 5 ms of receiving the system signal indicating a power supply failure.

The other key to enabling significant over-subscription is rapid detection of a power supply failure.

4.3 Chip Hardware Power Management Features

4.3.1 Chiplet Voltage Control

The POWER8 processor supports several voltage regulator module (VRM) control mechanisms to support multiple system configurations. The core chiplets are on a separate voltage plane than the other Nest components of the chip. The chip-level Power Management Control (PMC) macro and the OCC are, in combination, programmable to support these configurations.

Core chiplets all share the same voltage plane and must run with the “highest-common denominator” (meaning, the core demanding the highest voltage sets the value of the voltage rail). The OCC is responsible for establishing the best frequency, and therefore voltage bounds based on the workload running, the power/performance efficiency policy selected by the customer, and the system budgets established by the thermal management component.

4.3.2 Chip-Level Voltage Control Sequencing

The external VRMs (eVRMs) sourcing the logic (V_{DD}) and array (V_{CS}) rails are controlled by voltage control interfaces from the POWER8 chip. These interfaces use serial peripheral interconnect (SPI) signaling to a VRM chipset that converts the addressed VID command to industry standard Intel VRM-11 interface components or others, as implemented by the VRMs.

4.3.3 SPIVID VRM Control Sequencing

The V_{DD} target voltage and the relevant V_{CS} offset is sent in one command to the VRM set. The target might be the full voltage swing request (V_{MAX} to V_{MIN} or vice-versa) or any subset. With the V_{DD} target and associated V_{CS} offset value, the VRMs, through sampling of load lines, manage the offset of the two rails during the slew.

4.4 System Power Sequencing

The power sequencing design must check the PGOOD status before continuing to the next step. The sequencer must allow for some amount of minimum time after PGOOD issues before continuing as specified in *Table 4-1*.

Table 4-1. System Power Sequencing

Voltage Domain	Delta Time (ms)	Comments
Typically system rails associated with service processors, I/O, and storage are enabled before the processor/memory power is enabled. This guide does not cover these specifics.		
AV_{DD}	10	POWER8 Memory Buffer and POWER8 processor can be combined.
V_{IO}	10	POWER8 Memory Buffer and POWER8 processor can be combined.
POWER8 V_{DD}	10	
POWER8 V_{CS}	10	
Additional processors can be added here in the same sequence or paralleled, so that all V_{DD} come on at the same time followed by all V_{CS}.		
V_{PCI}	10	POWER8 Memory Buffer and POWER8 processor can be combined.
POWER8 Memory Buffer V_{DD}	10	
POWER8 Memory Buffer V_{CS}	10	
Additional POWER8 Memory Buffer chips can be added here in the same sequence or paralleled, so that all V_{DD} come on at the same time followed by all V_{CS}.		
Marks the beginning of the secondary sequence, memory initialization pause. (1)		
V_{PP}	10	DDR4 only. Must always be > V_{MEM}.
$V_{MEM/DDR}$	10	DDR3 or DDR4. Must be < 200 ms after V_{PP}, V_{TERM} tracks this domain/2 and comes on at the same time.
Additional V_{PP}/V_{MEM} domains can be added in the same sequence or can be paralleled, so that they all come on together.		

1. The secondary sequence pause is required for the self boot engine (SBE) to complete memory initialization tasks. The processor indicates to the service processor or power sequencer what the memory voltage must be programmed to at this step and then indicates when to turn on the memory power rails. The memory voltage calculation is performed on the processor with information from the DIMM VPD and memory configuration.

5. Signals Descriptions

This section describes the POWER8 signal groups. They are arranged in functional groups according to their interface. *Table 5-1* lists the signal type notation.

Table 5-1. Signal Type Notation

Direction	Signal Type
Rec	Receiver (input)
RecDiff	Receiver differential pair signal polarity (P or N)
Drv	Driver (output)
DrvDiff	Driver differential pair signal polarity (P or N)
AnlgIn	Analog input
AnlgOut	Analog output
BiDi	Bi-directional input/output signal

Table 5-2 lists the buffer types.

Table 5-2. Signal Description Buffer Type

Signal	Description
CMOS	CMOS buffers.
OD	Open drain.
Analog	Analog.
EI4	Elastic interface 4.
EDI	Elastic differential I/O.
PCIe	PCI Express interface signals. These signals are compatible with PCI Express 3.0.
Asynchronous	Signal has no timing relationship with any reference clock.
REF	Voltage reference signal.
PLL/CLK	PLL clock.

5.1 Pin Naming Convention

The general pin naming pattern is:

prefix_source_connectionType_sink_clockGroup_dat_bitNumber_diffBit

Prefix - the type of bus or signal type being connected. The following abbreviations are used.

DR DDR memory bus
MM Memory bus
NA For A buses
NC No connect
PE PCIe

PV	Pervasive
TS	Test

Source and Sink - the specific component and bus being connected. The following abbreviations are used.

CT	Chip test or pervasive
M0	Memory channel 0 bus
E0	PCIe 0 bus
A0	A0 bus
X0	Bus X0 of processor in SCMs (P0 is implicit)
PIN	Module Pin

Connectivity

P	Point-to-point
B	Bidirectional
M	Multipoint

Clock Group

CK0	Clock group 0
CKA	Clock group A

SigType - signal type

CLK	Clock signal
DAT	Data signal

BitNumber - bit strand number, if needed, using padding zeroes.

DiffBit - differential pair signal polarity (P or N), if needed.

5.2 Signals by Group

5.2.1 Voltage Signals

Table 5-3 lists the voltage signals.

Table 5-3. Voltage Signals

Signal Name	Description
VSB_3P30 VSB_1P20	VSB
VPCI_1P20	VPCI
VIO_1P10	VIO
VDD_0P89	VDD
VCS_0P97	VCS
DVDD_1P50	Digital VDD
AVDD_1P50	Analog VDD
GND	Ground

5.2.2 PLL/Clock Signals

Table 5-4 lists the reference clocks

Table 5-4. Reference Clocks

Signal	Description	Category	Family	Type
PV_PIN_P_CT_OSC0_C1_REFCLK_P	System Reference Clock	PLL/Clock	CMOS	RecDiff
PV_PIN_P_CT_OSC0_C1_REFCLK_N	System Reference Clock	PLL/Clock	CMOS	RecDiff
GND	System Reference Clock	PLL/Clock	CMOS	RecDiff
VIO_1P10	System Reference Clock	PLL/Clock	CMOS	RecDiff

Table 5-5 lists the oscillator switch control signals.

Table 5-5. Oscillator Switch Controls

Signal	Description	Category	Family	Type
VIO_1P10	Use Oscillator 0 from OSC0	PLL/Clock	CMOS	Rec
VIO_1P10	Use Oscillator 1 from OSC0	PLL/Clock	CMOS	Rec
GND	Use Oscillator 0 from OSC1	PLL/Clock	CMOS	Rec
GND	Use Oscillator 1 from OSC1	PLL/Clock	CMOS	Rec

Table 5-6 lists the PLL signals.

Table 5-6. PLL Signals

Signal	Description	Category	Family	Type
TS_CT_P_PIN_PXFM_PLL_ANATST	PLL analog test	PLL/Clock	Analog	AnlgOut
TS_CT_P_PIN_PXFM_PLL_HFC_P/N	PLL high-frequeny characterization	PLL/Clock	CMOS	Drv
TS_CT_P_PIN_M0_PLL_ANATST	Memory 0 PLL analog test	PLL/Clock	Analog	AnlgOut
TS_CT_P_PIN_M1_PLL_ANATST	Memory 1 PLL analog test	PLL/Clock	Analog	AnlgOut
TS_CT_P_PIN_A_PLL_ANATST	PLL analog test	PLL/Clock	Analog	AnlgOut
TS_CT_P_PIN_PE0_PLL_ANATST	PCIe PLL analog test	PLL/Clock	Analog	AnlgOut
TS_CT_P_PIN_PE1_PLL_ANATST		PLL/Clock	Analog	AnlgOut

5.2.3 Miscellaneous Signals

Table 5-7 lists the JTAG signals.

Table 5-7. JTAG Signals

Signal	Description	Category	Family	Type
TS_PIN_P_CT_CARD_TEST	Card Test	Pervasive	CMOS	Rec
TS_PIN_P_CT_JTAG_TMS	JTAG Test Mode Select	Pervasive	CMOS	Drv
TS_PIN_P_CT_JTAG_TDI	JTAG Test Data In	Pervasive	CMOS	Drv
TS_CT_P_PIN_JTAG_TDO	JTAG Test Data Out	Pervasive	CMOS	Rec
TS_PIN_P_CT_EXT_TRIGGER_TCK	External Trigger Test Clock	Pervasive	OD	BiDi

Table 5-8 lists the test signals.

Table 5-8. Test Signals

Signal	Description	Category	Family	Type
TS_PIN_P_CT_TEST_LSSD_TE	LSSD Test Mode	Pervasive	CMOS	Rec
TS_PIN_P_CT_TST_FORCE_PWR_ON	Test force power-on	Pervasive	CMOS	Rec
TS_PIN_P_CT_STBY_RESET_B	Standby Reset	Pervasive	CMOS	Rec
TS_CT_P_PIN_PROBE0_P/N	Probe Out 0 Diff hgh/Diff low	Pervasive	CMOS	DrvDiff
TS_CT_P_PIN_PROBE0_N	Probe Out 0 Diff_L	Pervasive	CMOS	DrvDiff
TS_CT_P_PIN_PROBE1_P/N	Probe Out 1 Diff_High/DIFF_Low	Pervasive	CMOS	DrvDiff
TS_CT_P_PIN_PROBE2	Probe Out 2	Pervasive	CMOS	Drv
TS_CT_P_PIN_PROBE3	Probe Out 3	Pervasive	CMOS	Drv
TS_CT_P_PIN_PROBE4	Probe Out 4	Pervasive	CMOS	Drv
TS_PIN_P_CT_EFUSE_FSOURCE	eFuse VDD	Pervasive	Analog	sPower
PV_CT_P_PIN_SPARE0	Spare 0	Pervasive	CMOS	Drv

Table 5-9 lists the pervasive signals.

Table 5-9. Pervasive Signals

Signal	Description	Category	Family	Type
TS_PIN_P_CT_STBY_RESET_B	Standby Reset	Pervasive	CMOS	Rec
TS_PIN_P_CT_EXT_TRIGGER_TCK	External Trigger TCK	Pervasive	OD	BiDi
TS_CT_P_PIN_PROBE0_P/N	Probe Out 0 Diff_H/Diff_L	Pervasive	CMOS	DrvDiff
TS_CT_P_PIN_PROBE1_P/N	Probe Out 1 Diff_H/Diff_L	Pervasive	CMOS	DrvDiff
TS_CT_P_PIN_PROBE2	Probe Out 2	Pervasive	CMOS	Drv
TS_CT_P_PIN_PROBE3	Probe Out 3	Pervasive	CMOS	Drv
TS_CT_P_PIN_PROBE4	Probe Out 4	Pervasive	CMOS	Drv
TS_PIN_P_CT_EFUSE_FSOURCE	eFuse VDD	Pervasive	Analog	sPower

Table 5-10 lists the LPC bus signals.

Table 5-10. LPC Bus Signals

Signal	Description	Category	Family	Type
PV_CT_B_PIN_LPC_DATA_[00:03]	LPC Data	Pervasive	CMOS	BiDi
PV_CT_P_PIN_LPC_FRAME_B	LPC Frame	Pervasive	CMOS	Drv
PV_PIN_P_CT_LPC_RESET_B	LPC Reset	Pervasive	CMOS	BIDI
PV_PIN_P_CT_LPC_CLK	LPC Clock	Pervasive	CMOS	Rec
PV_CT_P_PIN_ATTENTION_B	Attention	Pervasive	CMOS	Drv

Table 5-11 lists the control signals.

Table 5-11. Control Signals

Signal	Description	Category	Family	Type
GND	Chip Position	Pervasive	CMOS	Rec
PV_PIN_P_CT_CHIP_ID0	Chip Id	Pervasive	CMOS	Rec
PV_PIN_P_CT_CHIP_ID1	Chip Id	Pervasive	CMOS	Rec
PV_PIN_P_CT_FSI_IN_ENA1	Enable incoming FSI clk	Pervasive	CMOS	Rec
PV_PIN_P_CT_VIO_PGOOD	V_{IO} power good	Pervasive	CMOS	Rec
PV_CT_P_PIN_TPM_RESET	TPM reset	Pervasive	OD	BiDi
PV_PIN_P_CT_TPM_INTERRUPT	TPM interrupt	Pervasive	OD	Rec

Table 5-11 lists the FSI signals.

Table 5-12. FSI Signals

Signal	Description	Category	Family	Type
PV_PIN_P_CT_FSP0_FSI_CLK	FSI0 Clock	FSI	CMOS	Rec
PV_PIN_B_CT_FSP0_FSI_DATA	FSI0 Data	FSI	CMOS	BiDi
SH_PIN_P_CT_FSP1_FSI_CLK	FSI1 Clock	FSI	CMOS	Rec
SH_CT_P_PIN_MB_FSI0_CLK	FSI Master 0 Clock	FSI	CMOS	Drv
SH_CT_B_PIN_MB_FSI0_DATA	FSI Master 0 Data	FSI	CMOS	BiDi
SH_CT_P_PIN_MB_FSI1_CLK	FSI Master 1 Clock	FSI	CMOS	Drv
SH_CT_B_PIN_MB_FSI1_DATA	FSI Master 1 Data	FSI	CMOS	BiDi
MM_CT_P_PIN_MB_FSI2_CLK	FSI Master 2 Clock	FSI	CMOS	Drv
MM_CT_B_PIN_MB_FSI2_DATA	FSI Master 2 Data	FSI	CMOS	BiDi
MM_CT_P_PIN_MB_FSI3_CLK	FSI Master 3 Clock	FSI	CMOS	Drv
MM_CT_B_PIN_MB_FSI3_DATA	FSI Master 3 Data	FSI	CMOS	BiDi
MM_CT_P_PIN_MB_FSI6_CLK	FSI Master 6 Clock	FSI	CMOS	Drv
MM_CT_B_PIN_MB_FSI6_DATA	FSI Master 6 Data	FSI	CMOS	BiDi
MM_CT_P_PIN_MB_FSI7_CLK	FSI Master 7 Clock	FSI	CMOS	Drv
MM_CT_B_PIN_MB_FSI7_DATA	FSI Master 7 Data	FSI	CMOS	BiDi
PV_CT_P_PIN_FSI1_CLK	FSI Master CP Clock	FSI	CMOS	Drv
PV_CT_B_PIN_FSI1_DATA	FSI Master CP Data	FSI	CMOS	BiDi
PV_CT_P_PIN_FSI2_CLK	FSI Master CP Clock	FSI	CMOS	Drv
PV_CT_B_PIN_FSI2_DATA	FSI Master CP Data	FSI	CMOS	BiDi
PV_CT_P_PIN_FSI3_CLK	FSI Master CP Clock	FSI	CMOS	Drv
PV_CT_B_PIN_FSI3_DATA	FSI Master CP Data	FSI	CMOS	BiDi
PV_PIN_P_CT_FSI_SMD	FSI secure mode disable	Pervasive	CMOS	Rec

Table 5-13 lists the SPI signals.

Table 5-13. SPI Signals (Sheet 1 of 2)

Signal	Description	Category	Family	Type
PV_CT_P_PIN_SPIVID0_MOSI	SPI VIDs (To VRM0)	SPI	CMOS	Drv
PV_PIN_P_CT_SPIVID0_MISO	SPI VIDs (To VRM0)	SPI	CMOS	Rec
PV_CT_P_PIN_SPIVID0_SCLK	SPI VIDs (To VRM0)	SPI	CMOS	Drv
PV_CT_P_PIN_SPIVID0_CS	SPI VIDs (To VRM0)	SPI	CMOS	Drv
PV_CT_P_PIN_SPIADC_MOSI	SPISS MOSI	SPI	CMOS	Drv
PV_PIN_P_CT_SPIADC_MISO	SPISS MISO	SPI	CMOS	Rec

Table 5-13. SPI Signals (Sheet 2 of 2)

Signal	Description	Category	Family	Type
PV_CT_P_PIN_SPIADC_SCLK	SPISS SCLK	SPI	CMOS	Drv
PV_CT_P_PIN_SPIADC_CS0	SPISS CS0	SPI	CMOS	Drv
PV_CT_P_PIN_SPIADC_CS1	SPISS CS1	SPI	CMOS	Drv

Table 5-14 lists the I^2C signals.

Table 5-14. I^2C Signals

Signal	Description	Category	Family	Type
PV_PIN_B_CT_I2CSL_SCL	I2C Slave Clock	I2C	OD	BiDi
PV_PIN_B_CT_I2CSL_SDA	I2C Slave Data	I2C	OD	BiDi
PV_CT_M_PIN_SEEPROM0_CLK	SEEPROM Clock	I2C	OD	Drv
PV_CT_M_PIN_SEEPROM0_DATA	SEEPROM Data	I2C	OD	BiDi
PV_CT_M_PIN_SEEPROM1_CLK	SEEPROM Clock	I2C	OD	Drv
PV_CT_M_PIN_SEEPROM1_DATA	SEEPROM Data	I2C	OD	BiDi
PV_CT_B_PIN_LP_I2C_SCL_B	I2C Master Data Lightpath	I2C	OD	BiDi
PV_CT_B_PIN_LP_I2C_SDA_B	I2C Master Clock Lightpath	I2C	OD	BiDi
PV_CT_B_PIN_PCI_I2C_SCL_B	I2C Master Data PCIe E1	I2C	OD	BiDi
PV_CT_B_PIN_PCI_I2C_SDA_B	I2C Master Data PCIe E1	I2C	OD	BiDi

Table 5-15 lists the time-of-day signals.

Table 5-15. Time of Day and Bus Synchronization Signals

Signal	Description	Category	Family	Type
PV_PIN_P_CT_OSC0_TODREFCLK	TOD Refclk	CLK	CMOS	Rec

Table 5-16 lists the thermal diode and monitor signals.

Table 5-16. Thermal Diodes and Monitor Signals (Sheet 1 of 2)

Signal	Description	Category	Family	Type
TS_CT_P_PIN_TDIODE_A5	Core Thermal Diode Anode	Thermal	Analog	AnlgOut
TS_CT_P_PIN_TDIODE_C5	Core Thermal Diode Cathode	Thermal	Analog	AnlgOut
TS_CT_P_PIN_TDIODE_A13	Core Thermal Diode Anode	Thermal	Analog	AnlgOut
TS_CT_P_PIN_TDIODE_C13	Core Thermal Diode Cathode	Thermal	Analog	AnlgOut
TS_CT_P_PIN_DTS2_MONI	Digital Thermal Sensor Monitor	Thermal	Analog	AnlgOut
TS_CT_P_PIN_AMX0_VSENSE	West Analog Muxed Sense	Vsense	Analog	AnlgOut
TS_CT_P_PIN_AMX0_GSENSE	West Analog Muxed Ground Sense	Vsense	Analog	AnlgOut
TS_CT_P_PIN_AMX1_VSENSE	West Analog Muxed Sense	Vsense	Analog	AnlgOut

Table 5-16. Thermal Diodes and Monitor Signals (Sheet 2 of 2)

Signal	Description	Category	Family	Type
TS_CT_P_PIN_AMX1_GSENSE	West Analog Muxed Ground Sense	Vsense	Analog	AnlgOut
TS_CT_P_PIN_GDDCORE0_GSENSE	Chiplet Core Logic Ground Sense	Vsense	Analog	AnlgOut
TS_CT_P_PIN_VDDCORE0_VSENSE	Chiplet Core Logic Sense	Vsense	Analog	AnlgOut
TS_CT_P_PIN_GDSCORE0_GSENSE	Chiplet Core SRAM Ground Sense	Vsense	Analog	AnlgOut
TS_CT_P_PIN_VCSCORE0_VSENSE	Chiplet Core SRAM Sense	Vsense	Analog	AnlgOut
TS_CT_P_PIN_GDECO0_GSENSE	Chiplet ECO Logic Ground Sense	Vsense	Analog	AnlgOut
TS_CT_P_PIN_VDDECO0_VSENSE	Chiplet ECO Logic Sense	Vsense	Analog	AnlgOut
TS_CT_P_PIN_VCSECO0_VSENSE	Chiplet ECO SRAM Sense	Vsense	Analog	AnlgOut
TS_CT_P_PIN_VDDEX0_VSENSE	EX VDD Logic Voltage Sense	Vsense	Analog	AnlgOut
TS_CT_P_PIN_EX0_GSENSE	EX VCS Ground Sense	Vsense	Analog	AnlgOut
TS_CT_P_PIN_VCSEX0_VSENSE	EX VCS Logic Voltage Sense	Vsense	Analog	AnlgOut
TS_CT_P_PIN_VIO_VSENSE	VIO Logic Voltage Sense	Vsense	Analog	AnlgOut
TS_CT_P_PIN_VIO_VPCI_GSENSE	VIO VPCI Ground Sense	Vsense	Analog	AnlgOut
TS_CT_P_PIN_VPCI0_VSENSE	VPCI Voltage Sense	Vsense	Analog	AnlgOut
TS_CT_P_PIN_PFAMX_VSENSE	PFET Analog Muxed Sense	Vsense	Analog	AnlgOut
TS_CT_P_PIN_PFAMX_GSENSE	PFET Analog Muxed Ground Sense	Vsense	Analog	AnlgOut
GND	BEOL Sense 0	Vsense	CMOS	Rec
GND	BEOL Sense 1	Vsense	CMOS	Rec
GND	BEOL Sense 2	Vsense	CMOS	Rec
GND	BEOL Sense 3	Vsense	CMOS	Rec

Table 5-17 lists the DMI signals.

Table 5-17. DMI Signals (Sheet 1 of 2)

Signal	Description	Category	Family	Type
PV_PIN_P_CT_M0_TERMREF_P/N	Memory Termination Reference	TermRef	Analog	AnlgIn
MM_M0_P_PIN_CKC_CLK_P/N	Memory Channel Downstream Forwarded Clock	Data	EDI	DrvDiff
MM_M0_P_PIN_CKC_DAT_[00:16]_P	Memory Channel Downstream	Data	EDI	DrvDiff
MM_M0_P_PIN_CKC_DAT_[00:16]_N		Data	EDI	DrvDiff
MM_PIN_P_M0_CKC_CLK_P/N	Memory Channel Upstream Forwarded Clock	Data	EDI	RecDiff
MM_PIN_P_M0_CKC_DAT_[00:23]_P	Memory Channel Upstream	Data	EDI	RecDiff
MM_PIN_P_M0_CKC_DAT_[00:23]_N		Data	EDI	RecDiff
MM_M0_P_PIN_CKD_CLK_P/N	Memory Channel Downstream Forwarded Clock	Data	EDI	DrvDiff
MM_M0_P_PIN_CKD_DAT_[00:16]_P	Memory Channel Downstream	Data	EDI	DrvDiff
MM_M0_P_PIN_CKD_DAT_[00:16]_N		Data	EDI	DrvDiff

Table 5-17. DMI Signals (Sheet 2 of 2)

Signal	Description	Category	Family	Type
MM_PIN_P_M0_CKD_CLK_P/N	Memory Channel Upstream Forwarded Clock	Data	EDI	RecDiff
MM_PIN_P_M0_CKD_DAT_[00:23]_P	Memory Channel Upstream	Data	EDI	RecDiff
MM_PIN_P_M0_CKD_DAT_[00:23]_N		Data	EDI	RecDiff
MM_PIN_P_CT_M1_FAULT_C_N	Memory Fault Channel	Data	CMOS	Rec
MM_PIN_P_CT_M1_FAULT_D_N		Data	CMOS	Rec
PV_PIN_P_CT_M1_TERMREF_P/N	Memory Termination Reference	TermRef	Analog	AnlgIn
MM_M1_P_PIN_CKC_CLK_P/N	MC Buffered Port. Memory Channel Downstream Forwarded Clock	Data	EDI	DrvDiff
MM_M1_P_PIN_CKC_DAT_[00:16]_P	MC Buffered Port. Memory Channel Downstream	Data	EDI	DrvDiff
MM_M1_P_PIN_CKC_DAT_[00:16]_N		Data	EDI	DrvDiff
MM_PIN_P_M1_CKC_CLK_P/N	MC Buffered Port. Memory Channel Upstream Forwarded Clock	Data	EDI	RecDiff
MM_PIN_P_M1_CKC_DAT_[00:23]_P	MC Buffered Port. Memory Channel Upstream	Data	EDI	RecDiff
MM_PIN_P_M1_CKC_DAT_[00:23]_N	MC Buffered Port. Memory Channel Upstream	Data	EDI	RecDiff
MM_M1_P_PIN_CKD_CLK_P/N	Memory Channel Downstream Forwarded Clock	Data	EDI	DrvDiff
MM_M1_P_PIN_CKD_DAT_[00:16]_P	Memory Channel Downstream	Data	EDI	DrvDiff
MM_M1_P_PIN_CKD_DAT_[00:16]_N		Data	EDI	DrvDiff
MM_PIN_P_M1_CKD_CLK_P/N	Memory Channel Upstream ForwarDed Clock	Data	EDI	RecDiff
MM_PIN_P_M1_CKD_DAT_[00:23]_P	Memory Channel Upstream	Data	EDI	RecDiff
MM_PIN_P_M1_CKD_DAT_[00:23]_N		Data	EDI	RecDiff

Table 5-18 lists the A bus signals.

Table 5-18. A Bus Signals (Sheet 1 of 2)

Signal	Description	Category	Family	Type
NA_PIN_P_A0_CK0_CLK_P/N	Clock Input	Data	EDI	RecDiff
NA_PIN_P_A0_CK0_DAT_[00:22]_P	16-Bit Pack Data Input [00:22]	Data	EDI	Rec
NA_PIN_P_A0_CK0_DAT_[00:22]_N	16-Bit Pack Data Input [00:22]	Data	EDI	Rec
NA_A0_P_PIN_CK0_CLK_P/N	Clock Output	Data	EDI	DrvDiff
NA_A0_P_PIN_CK0_DAT_[00:22]_P	16-Bit Pack Data Output [00:22]	Data	EDI	Drv
NA_A0_P_PIN_CK0_DAT_[00:22]_N	16-Bit Pack Data Output [00:22]	Data	EDI	Drv
NA_PIN_P_A1_CK0_CLK_P/N	Clock Input	Data	EDI	RecDiff
NA_PIN_P_A1_CK0_DAT_[00:22]_P	16-Bit Pack Data Input [00:22]	Data	EDI	Rec

Table 5-18. A Bus Signals (Sheet 2 of 2)

Signal	Description	Category	Family	Type
NA_PIN_P_A1_CK0_DAT_[00:22]_N	16-Bit Pack Data Input [00:22]	Data	EDI	Rec
NA_A1_P_PIN_CK0_CLK_P/N	Clock Output	Data	EDI	DrvDiff
NA_A1_P_PIN_CK0_DAT_[00:22]_P	16-Bit Pack Data Output [00:22]	Data	EDI	Drv
NA_A1_P_PIN_CK0_DAT_[00:22]_N	16-Bit Pack Data Outpu t[00:22]	Data	EDI	Drv
NA_PIN_P_A2_CK0_CLK_P/N	Clock Input	Data	EDI	RecDiff
NA_PIN_P_A2_CK0_DAT_[00:22]_P	16-Bit Pack Data Input [00:22]	Data	EDI	Rec
NA_PIN_P_A2_CK0_DAT_[00:22]_N	16-Bit Pack Data Input [00:22]	Data	EDI	Rec
NA_A2_P_PIN_CK0_CLK_P/N	Clock Output	Data	EDI	DrvDiff
NA_A2_P_PIN_CK0_DAT_[00:22]_P	16-Bit Pack Data Output [00:22]	Data	EDI	Drv
NA_A2_P_PIN_CK0_DAT_[00:22]_N	16-Bit Pack Data Output [00:22]	Data	EDI	Drv
PV_PIN_P_CT_A_TERMREF_P/N	A Bus Terminal Reference (P/N)	TermRef	OD	AnlgIn

Table 5-19 lists the PCIe bus signals.

Table 5-19. PCIe Bus Signals

Signal	Description	Category	Family	Type
PV_PIN_P_CT_OSC0_E_REFCLK_P/N	PCIe Bus Input Reference Clock	PLL/CLK	PCIE	RecDiff
GND		PLL/CLK	PCIE	RecDiff
VIO_1P10		PLL/CLK	PCIE	RecDiff
PE_PIN_P_E0_CK0_DAT_[00:07]_P	Data Input (16× non-bifurcatable bus)	Data	PCIE	RecDiff
PE_PIN_P_E0_CK1_DAT_[00:07]_P	Data Input (16× non-bifurcatable bus)	Data	PCIE	RecDiff
PE_PIN_P_E0_CK0_DAT_[00:07]_N	Data Input (16× non-bifurcatable bus)	Data	PCIE	RecDiff
PE_PIN_P_E0_CK1_DAT_[00:07]_N	Data Input (16× non-bifurcatable bus)	Data	PCIE	RecDiff
PE_E0_P_PIN_CK0_DAT_[00:07]_P	Data Output (16× non-bifurcatable bus)	Data	PCIE	DrvDiff
PE_E0_P_PIN_CK1_DAT_[00:07]_P	Data Output (16× non-bifurcatable bus)	Data	PCIE	DrvDiff
PE_E0_P_PIN_CK0_DAT_[00:07]_N	Data Output (16× non-bifurcatable bus)	Data	PCIE	DrvDiff
PE_E0_P_PIN_CK1_DAT_[00:07]_N	Data Output (16× non-bifurcatable bus)	Data	PCIE	DrvDiff
$\overline{\text{PE\_CT\_P\_PIN\_E0\_PERST0\_B}}$	PCIe Reset 0	Control	OD	Drv
$\overline{\text{PE\_CT\_P\_PIN\_E0\_PERST1\_B}}$	PCIe Reset 1	Control	OD	Drv
$\overline{\text{PE\_PIN\_P\_CT\_E0\_PRSNT0\_B}}$	Present 0	Control	OD	Rec
$\overline{\text{PE\_PIN\_P\_CT\_E0\_PRSNT1\_B}}$	Present 1	Control	OD	Rec
PE_CT_P_PIN_E0_SLOT_CLK0_N	Clock 0 N/P	CLK	PCIE	DrvDiff
PV_PIN_P_CT_E0_TERMREF_P/N	PHY Support	TermRef	Analog	AnlgIn
PE_PIN_P_E1_CK0_DAT_[00:07]_P	Data Input (16×/8× bifurcatable bus)	Data	PCIE	RecDiff
PE_PIN_P_E1_CK1_DAT_[00:07]_P	Data Input (16×/8× bifurcatable bus)	Data	PCIE	RecDiff
PE_PIN_P_E1_CK0_DAT_[00:07]_N	Data Input (16×/8× bifurcatable bus)	Data	PCIE	RecDiff
PE_PIN_P_E1_CK1_DAT_[00:07]_N	Data Input (16×/8× bifurcatable bus)	Data	PCIE	RecDiff
PE_E1_P_PIN_CK0_DAT_[00:07]_P	Data Output (16×/8× bifurcatable bus)	Data	PCIE	DrvDiff
PE_E1_P_PIN_CK1_DAT_[00:07]_P	Data Output (16×/8× bifurcatable bus)	Data	PCIE	DrvDiff
PE_E1_P_PIN_CK0_DAT_[00:07]_N	Data Output (16×/8× bifurcatable bus)	Data	PCIE	DrvDiff
PE_E1_P_PIN_CK1_DAT_[00:07]_N	Data Output (16×/8× bifurcatable bus)	Data	PCIE	DrvDiff
$\overline{\text{PE\_CT\_P\_PIN\_E1\_PERST0\_B}}$	PCIe Reset 0	Control	OD	Drv
$\overline{\text{PE\_CT\_P\_PIN\_E1\_PERST1\_B}}$	PCIe Reset 1	Control	OD	Drv
$\overline{\text{PE\_PIN\_P\_CT\_E1\_PRSNT0\_B}}$	Present 0	Control	OD	Rec
$\overline{\text{PE\_PIN\_P\_CT\_E1\_PRSNT1\_B}}$	Present 1	Control	OD	Rec
PE_CT_P_PIN_E1_SLOT_CLK0_N	Clock 0	CLK	PCIE	DrvDiff
PE_CT_P_PIN_E1_SLOT_CLK1_N	Clock 1	CLK	PCIE	DrvDiff
PV_PIN_P_CT_E1_TERMREF_P/N	PHY Support	TermRef	OD	AnlgIn

6. Electrical Characteristics

This section provides ac and dc electrical specifications and thermal characteristics for the POWER8 processor.

6.1 Frequency Domains

Table 6-1 lists the POWER8 and POWER8 Memory Buffer chip frequency domains and scan frequency domains.

Table 6-1. POWER8/POWER8 Memory Buffer Frequency Domains (Sheet 1 of 2)

Region	IP	Nominal Frequency	Maximum Frequency	Minimum Frequency	Supply Type	CLY	Functional Phase	ET Cycle (ps)	Scan Phase	Scan Cycles	Macro Pin
Core	C1, L2	Varied	5.5	1.2 GHz (200 MHz)	Adaptive and Dynamic	50%	M, M×2	208	S	416	nclk
Chiplet	L3, NCU	Varied	2.75	0.6 GHz (200 MHz)	Adaptive and Dynamic	50%	M1×2	416	S1	416	cache_nclk
PB	nest	2.4 GHz	2.7 GHz	1.9 GHz	Fixed (V_{IO})	99+%	NASYNC(×2), N[0:9]ASYNC(×2)	364	SN SN[0:9]	728	nest_nclk
MCIO	DMI	4.8 GHz	5.4 GHz	3.8 GHz	Fixed (V_{IO})	99+%	MCIO (×2/×4)	182/364/728	N/A	N/A	mcio_nclk
A	A0:2	1.6 GHz	1.8 GHz	1.2 GHz	Fixed (V_{IO})	99+%	AASYNC (×2)	550/1100	SA	550	a_nclk
AIO	DiffA	3.2 GHz	3.6 GHz	2.4 GHz	Fixed (V_{IO})	99+%	AIO/AIO×2/AIO×4	275/550/1100	N/A	N/A	aio_nclk
PCIe	PCIe	1 GHz	1.1 GHz	0.9 GHz	Fixed (V_{IO})	99+%	PCIASYNC (×2/×4)	790/1580/3160	SPCI	790	pcie_nclk
PCIIO	PCI	8/5/2.5 GHz	8.8/5.5/2.5 GHz	7.2/4.5/2.25 GHz	Fixed (V_{PCI})	99+%	PCIIO(×2/×4/×8/×16/×32/×64/×128)	100	N/A	N/A	No grid clock; various tree clocks
PCIREF	PCI	0.1 GHz	0.1 GHz	0.1 GHz	Fixed (V_{PCI})	99+%	PCIREF	7900	N/A	N/A	No grid clock (trees)
PCIFB	PCI	0.1 GHz	0.1 GHz	0.1 GHz	Fixed (V_{PCI})	99+%	PCIFB	6400	N/A	N/A	No grid clock (trees)

1. Depends on PHY being at 1.2 V.

Table 6-1. POWER8/POWER8 Memory Buffer Frequency Domains (Sheet 2 of 2)

Region	IP	Nominal Frequency	Maximum Frequency	Minimum Frequency	Supply Type	CLY	Functional Phase	ET Cycle (ps)	Scan Phase	Scan Cycles	Macro Pin
FSI	FSI	166 MHz	166 MHz	1 KHz	Fixed (V_{SB})	99+%	FS0CLK, FS1CLK, FSFCLK	5200	SFS	5200	fsi_ck
DDR Memory	MBU	2.4 GHz	2.6 GHz	1.33 GHz	Fixed (V_{DD})	99+%	MEM, MEM×2, MEM×4	326	SMEM	652	mem_nclk
SDR Memory	Combo PHY	1200	1200	667	Fixed (V_{DD}, DDR)	99+%	DPHY0/1 (×2/×4), SYS, SYSC, SYSQ, SYSQC, RD, DQSMUX, WR	760[1]	SDPHY0 SDPHY1	760	dphy_nclk, sys_nclk, sysc_nclk, sysq_nclk, sysqc_nclk, rd_nclk, dqsmux_nclk, wr_nclk

1. Depends on PHY being at 1.2 V.

6.2 dc Electrical Characteristics

Table 6-2 and *Table 6-3* describes the absolute maximum ratings the POWER8 processor can withstand. The absolute maximum ratings shown are stress ratings only. Continuous operation at or beyond these maximum ratings can cause permanent damage to the device.

Table 6-2 lists the voltage specifications for the POWER8 SCM.

Table 6-2. Voltage Specifications[1]

Voltage		Number of Active Cores		
		12	10	8
V_{DD}	Turbo	1.00 ±7%	1.05 ±7%	1.12 ±7%
	Maximum	1.2 ±7%	1.2 ±7%	1.2 ±7%
	Nominal	0.913 ±7%	0.959 ±7%	1.02 ±7%
	Minimum	0.75 ±7%	0.75 ±7%	0.75 ±7%
V_{CS}	Turbo	1.10 ±7%	1.15 ±7%	1.22 ±7%
	Maximum	1.2 ±7%	1.2 ±7%	1.2 ±7%
	Nominal	1.01 ±7%	1.06 ±7%	1.12 ±7%
	Minimum	0.85 ±7%	0.85 ±7%	0.85 ±7%
V_{IO}		1.10 ±5%	1.10 ±5%	1.10 ±5%
V_{SB}		1.20 ±10%	1.20 ±10%	1.20 ±10%
AV_{DD}		1.5 ±10%	1.5 ±10%	1.5 ±10%
DV_{DD}		1.5 ±10%	1.5 ±10%	1.5 ±10%
V_{PCIe}		1.20 ±5%	1.00 ±7%	

1. Values in this table are pending hardware validation and are subject to change.

Table 6-3 list the POWER8 current specifications.

Table 6-3. Current Specifications[1]

Current	Number of Active Cores		
	12	10	8
I_{VDD} Maximum	247	235	221
I_{VCS} Maximum	30	28	27
I_{VIO} Maximum	94	94	94
I_{VPCI} Maximum	5	5	5
I_{VXDR} Maximum	TBD	TBD	TBD
I_{VSB} Maximum	0.5	0.5	0.5
I_{AVDD} Maximum	1,0	1,0	1,0
I_{DVDD} Maximum	1.0	1.0	1.0

1. Values in this table are pending hardware validation and are subject to change.

Note: *Table 6-4* lists projected frequencies and TDPs for the POWER8 processor.

Table 6-4. Frequencies and TDP[1]

Part Number	Active Cores	Nominal Frequency (GHz)	Turbo Frequency (GHz)	Nominal TDP (W)	Turbo Power (W)	T_J Maximum (°C)	ADP T_J (°C)	ADP Power (W)	P_{SAV} T_J (°C)	Maximum P_{SAV} Mode Power (W)
00NE368	12	3.425	3.891	190	247	85	70	153.9	65	128
00NE369	12	3.126	3.625	190	247	85	70	153.9	65	128
00NE370	10	3.425	3.891	190	247	85	70	153.9	65	115
00NE371	8	3.758	4.123	190	247	85	70	153.9	65	102

Note:

1. Values in this table are pending hardware validation and are subject to change.
2. TDP - thermal design point.
3. RDP - regulator design point.
4. ADP - average design point.

6.3 ac Electrical Characteristics

This section provides the preliminary ac electrical characteristics for the POWER8 processor. After fabrication, parts are sorted by maximum processor core frequency and tested for conformance to the ac specifications for that frequency.

6.3.1 Clock ac Specifications

System reference clocks are 133.33 MHz and use host clock signal level (HCSL) differential levels, which are the same as the PCIe standard levels. Termination of 50 Ω to GND on each phase is required and is built into the Silicon Labs clock generators that the POWER8 processor is using. There is also the same 50 Ω to GND termination built into the differential receivers on the processor chip, but they are not enabled when the Silicon Labs clock generators are used. It must be enabled if some other vendor clock generator was used that did not have the integrated termination.

Spread spectrum is only allowed on the system reference clocks. It is limited to a spread percentage of 0.5% in the downward direction, which is the specification allowed by the DRAMs.

PCIe reference clocks are 100.00 MHz and use HCSL differential levels, which are the same as the PCIe standard levels. Termination of 50 Ω to GND on each phase is required and is built into the Silicon Labs clock generators that the POWER8 processor uses. There is also the same 50 Ω to GND termination built into the differential receivers on the processor chip, but they are not enabled when the Silicon Labs clock generators are used. It must be enabled if some other vendor clock generator is used that does not have the integrated termination.

PCIe and system reference clocks are HCSL differential levels, which is the PCIe standard. Spread spectrum is not supported by our systems on PCIe.

The LPC clock to the processor is 33.33 MHz single-ended CMOS with an MPUL of 1.1 V. The IBM system has a resistor divider network on the board to support this. The reference clock skew specification for LPC is 2.0 ns.

The TOD reference clocks to the processor are 16.0 MHz (20 PPM frequency stability), single-ended CMOS with an MPUL of 1.1 V. There is a resistor divider network on the board to support this.

Figure 6-1 shows the differential HCSL reference clock waveforms.

Figure 6-1. Differential (HCSL) Reference Clock Waveform (System and PCIe)

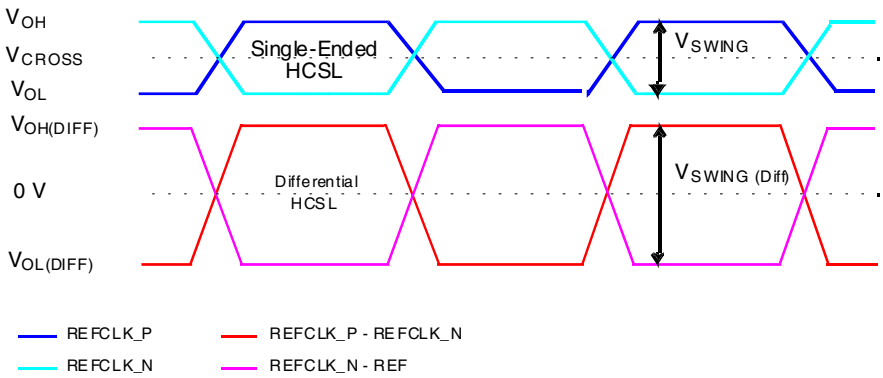


Table 6-5. Differential Reference Clock dc and ac Specification (Sheet 1 of 2)

Symbol	Parameter	Minimum	Typical	Maximum	Units	Notes
V_{OL}	Output low voltage	-0.10	0.0	0.1	V	1
V_{OH}	Output high voltage	0.50	0.70	0.90	V	1
V_{SWING}	Voltage swing	0.50	0.70	1.0	V	1
V_{CROSS}	Absolute crossing point (common mode voltage)	250	350	500	mV	1, 2, 3
V_{CROSS} Delta	Maximum variatino in common mode voltage	–	–	100	mV	1, 2, 4
V_{MAX}	Absolute maximum voltage	–	–	1.15	V	1, 5
V_{MIN}	Absolute minimum voltage	-0.20	–	–	V	1, 5
V_{OL} (Diff)	Output low voltage	-0.5	-0.7	-0.9	V	6
V_{OH} (Diff)	Output high voltage	0.50	0.70	0.90	V	6
V_{SWING} (Diff)	Voltage swing (differential)	1.0	1.4	1.8	V	6
T_R, T_F (Diff)	Rising and falling edge rates (differential)	1.0	2.0	4.0	V/ns	6, 7
V_{RB}	Ringback voltage margin	-100	–	100	mV	6, 8
T_{STABLE}	Time before VRB is allowed	500	–	–	ps	6, 8

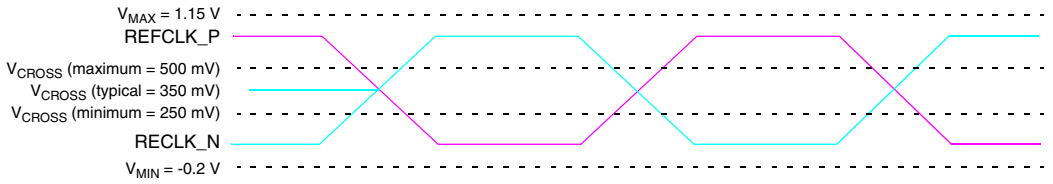
Table 6-5. Differential Reference Clock dc and ac Specification (Sheet 2 of 2)

Symbol	Parameter	Minimum	Typical	Maximum	Units	Notes
Duty Cycle	Duty cycle	45	–	55	%	6
T Period Average	Average clock period accuracy	50	–	2550	PPM	6, 9, 11, 12

1. Measurement taken from a single-ended waveform (see *Table 6-1* on page 43).
2. Measured at the crossing point where the instantaneous voltage value of the rising edge of REFCLK_P equals the falling edge of REFCLK_N (see *Figure 6-2* on page 44).
3. Refers to the total variation from the lowest crossing point to the highest crossing point, regardless of which edges are crossing. Refers to all crossing pints for this measurement (see *Figure 6-2* on page 44).
4. Defined as the total variation of all crossing voltages of rising REFCLK_P and falling REFCLK_N. This is the maximum allowed variance in V_{CROSS} for any particular system (see *Figure 6-3* on page 44).
5. Defined as the maximum instantaneous voltage including overshoot (see *Figure 6-2* on page 44).
6. Measurement taken from a differential waveform (see *Figure 6-1* on page 43).
7. Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK_P - REFCLK_N). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing (see *Figure 6-5* on page 45).
8. T_{STABLE} is the time that the differential clock must maintain a minimum ±150 mV differential voltage after the rising/falling edges before it is allowed to droop back into the VRB ±100 mV differential range (see *Figure 6-6* on page 45).
9. Defined as the average period. This includes crystal PPM and spread spectrum.
10. Defined as the minimum instantaneous voltage including overshoot (see *Figure 6-2* on page 44).
11. Defined as the frequency accuracy specification of the crystal that is used to generate the reference clock (typically less than 100 PPM).
12. PPM refers to parts per million and is a dc absolute period accuracy specification. 1 PPM is 1/1,000,000th of the clock frequency. The period is to be measured with a frequency counter with measurement window set to 100 ms or greater. For systems employing spread spectrum clocking, there is an additional 2,500 PPM average shift in the maximum period resulting from a 0.5% down spread.

Figure 6-2 shows the single-ended measurement points for absolute cross points and swing.

Figure 6-2. Single-Ended Measurement Points for Absolute Cross Points and Swing



6.3.2 Differential Reference Clock Measurements

Figure 6-3 shows the single-ended measurement points for the delta cross point.

Figure 6-3. Single-Ended Measurement Points for Delta Cross Point

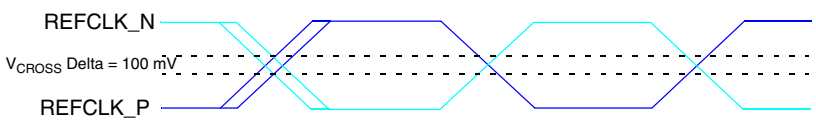


Figure 6-4 shows the differential measurement points for the duty cycle and period.

Figure 6-4. Differential Measurement Points for Duty Cycle and Period

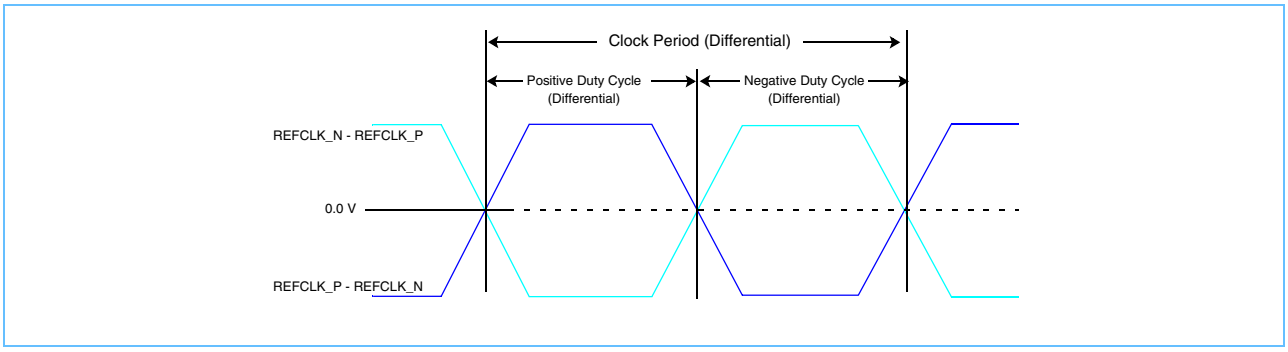


Figure 6-5 shows the differential measurement points for the rise and fall times.

Figure 6-5. Differential Measurement Points for Rise and Fall Times

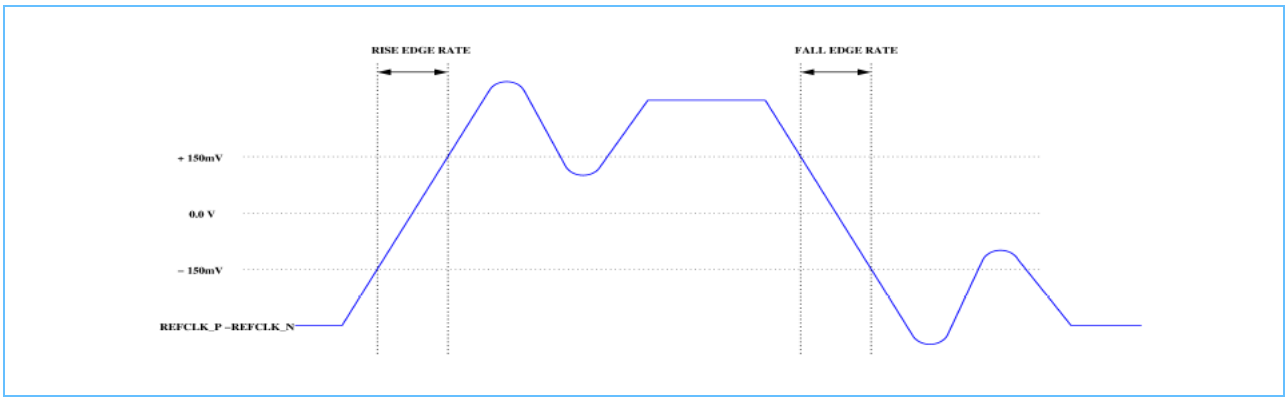


Figure 6-6 shows the differential measurement points for ringback.

Figure 6-6. Differential Measurement Points for Ringback

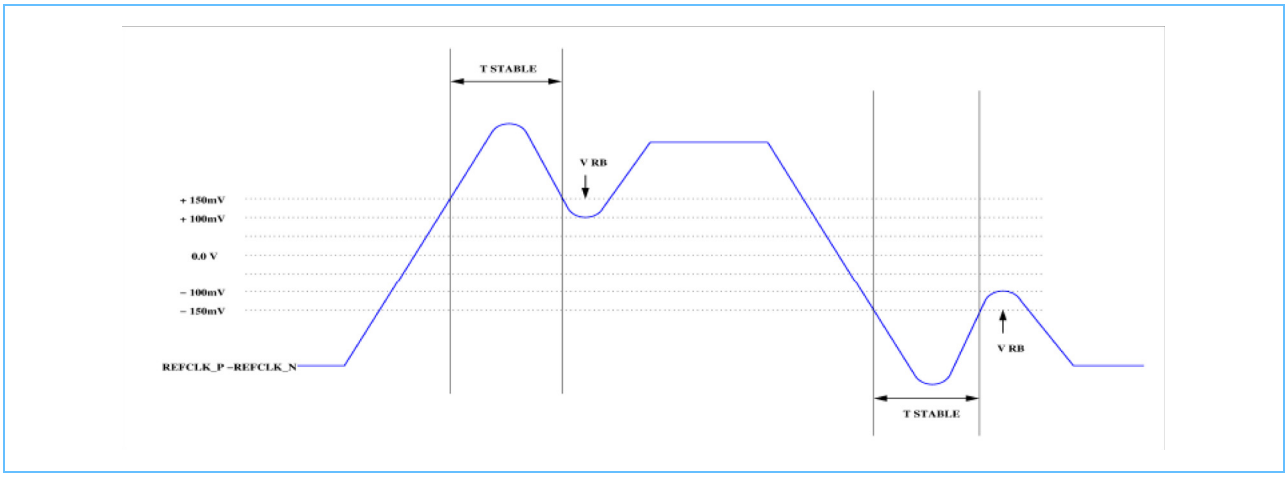


Table 6-6 lists general dc and ac specifications.

Table 6-6. dc and ac Specifications

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units	Notes
Output Voltage	V_{OL}	Output low voltage	–	0	0.2	V	1
	V_{OH}	Output high voltage	0.8	1.0	1.15	V	1
	V_{SWING}	Peak-peak, single-ended swing	0.8	1.0	1,15	V	1, 2
Rise and Fall Times	T_R, T_F	20% - 80%	–	1.5	3.0	ns	1, 3
Duty Cycle	DC	Measured at $V_{SWING}/2$	45	–	55	%	1, 2, 4
Clock Period	T_{AVG}	Clock period accuracy	-50	–	+50	PPM	1, 2, 4, 5

1. Measurements taken from a single-ended waveform (see *Figure 6-7* on page 46).
2. Voltage swing is equal to V_{OH} - V_{OL} (see *Figure 6-7* on page 46).
3. Rise and fall time measurements taken between 20% and 80% of V_{OH} and V_{OL} (see *Figure 6-7* on page 46).
4. Measurements taken at a voltage equal to $V_{SWING}/2$ (see *Figure 6-8* on page 47).
5. PPM refers to parts per million and is a dc absolute period accuracy specification. Includes only the accuracy of the crystal that is used to generate theclock because spread-spectrum is not enabled. The period is to be measured with a frequency counter with measurement window set to 100 ms or greater,

Figure 6-7 shows the single-ended processor reference clocks highlighting voltage and transition time measurement points.

Figure 6-7. Single-Ended Processor Reference Clocks (Voltage and Transition Time Measurement Points)

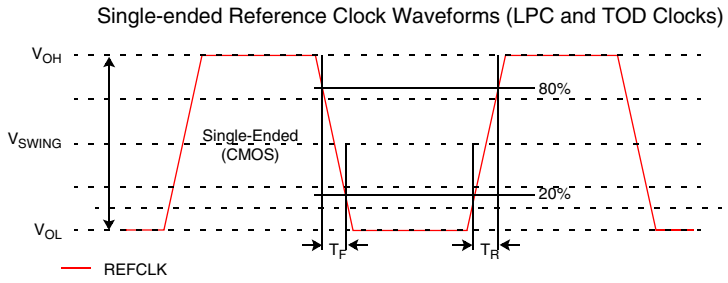
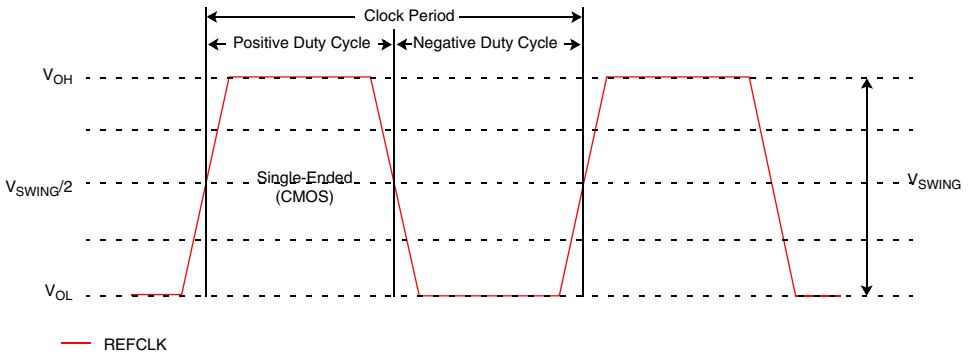


Figure 6-8 shows the single-ended processor reference clocks highlighting period and duty cycle measurement points.

Figure 6-8. Single-Ended Processor Reference Clocks (Period and Duty-Cycle Measurement Points)



6.3.3 FSI ac Specifications

Table 6-7 lists the ac specifications for the FSI bus.

Table 6-7. FSI Electrical Specification

Description	Minimum	Typical	Maximum	Units	Notes
C4 V_{MAX}			1.65	V	Maximum voltage at the chip pad.
Receiver V_{IL}			$0.3 \times 1.2\ V_{SB}$	mV	For receiver input hysteresis.
Receiver V_{IH}	$0.7 \times 1.2\ V_{SB}$			mV	For receiver input hysteresis.
1 kΩ Pull-up Resistance	1 k	1.25k	1.5 k	Ω	Pull-up resistance without leakage. If external pullups are used, they must be returned to V_{DOUT} and have a combined impedance not smaller than 1 kΩ.
1 kΩ Pull-down Resistance	1 k	1.25k	1.5 k	Ω	Pull-down resistance without leakage. If external pull downs are used, they have a combined impedance not smaller than 1 kΩ in parallel with 10 kΩ.
10 kΩ Pull-down Resistance	10 k	12.5k	15 k	Ω	Pull-up resistance without leakage.
Driver V_{OL}	$-0.1 \times 1.2\ V_{SB}$		$0.2 \times 1.2\ V_{SB}$	mV	Output pad driver levels.
Driver V_{OH}	$0.8 \times 1.2\ V_{SB}$		$1.1 \times 1.2\ V_{SB}$	mV	Output pad driver levels.
Duty Cycle distortion at 533 MHz with a 2 pF load	44.8	0	55.2	%	
Rise/Fall Time (10% - 90% of V_{DOUT} with a 2 pF load)	100	300	500	ps	

Table 6-8 lists the default settings for the internal FSI pull-up and pull-down resistors.

Table 6-8. Default FSI Settings (Sheet 1 of 2)

Function	SCM Pin	Pull-Up Internal Value	Pull-Down Internal Value
FSI0 Clock	BE29	–	10K
FSI0 Data	BE28	1K	–
FSI1 Clock	BA40	–	10K
FSI Master 0 Clock	BC42	–	–
FSI Master 0 Data	BB41	–	10K
FSI Master 1 Clock	AW38	–	–
FSI Master 1 Data	AY39	–	10K
FSI Master 2 Clock	BA25	–	–
FSI Master 2 Data	BA24	–	10K
FSI Master 3 Clock	AY23	–	–
FSI Master 3 Data	AY24	–	10K
FSI Master 6 Clock	BB22	–	–
FSI Master 6 Data	BB23	–	10K
FSI Master 7 Clock	BA22	–	–

Table 6-8. Default FSI Settings (Sheet 2 of 2)

Function	SCM Pin	Pull-Up Internal Value	Pull-Down Internal Value
FSI Master 7 Data	BA21	–	10K
FSI Master CP 1 Clock	BB25	–	–
FSI Master CP 1 Data	BB26	–	10K
FSI Master CP 2 Clock	BC24	–	–
FSI Master CP 2 Data	BC23	–	10K
FSI Master CP 3 Clock	BD24	–	–
FSI Master CP 3 Data	BD25	–	10K

6.3.4 SPI ac Specifications

Table 6-9 list the ac specifications for the SPI bus.

Table 6-9. SPI ac Specification

Description	Minimum	Typical	Maximum	Units	Notes
C4 V_{MAX}			1.65	V	Maximum voltage at the chip pad.
Receiver V_{IL}			$0.3 \times V_{I/O}$	mV	For receiver input hysteresis.
Receiver V_{IH}	$0.7 \times V_{I/O}$			mV	For receiver input hysteresis.
1 kΩ Pull-up Resistance	1 k	1.25k	1.5 k	Ω	Pull-up resistance without leakage. If external pullups are used, they must be returned to V_{DOUT} and have a combined impedance not smaller than 1 kΩ.
1 kΩ Pull-down Resistance	1 k	1.25k	1.5 k	Ω	Pull-down resistance without leakage. If external pull downs are used, they have a combined impedance not smaller than 1 kΩ in parallel with 10 kΩ.
10 kΩ Pull-down Resistance	10 k	12.5k	15 k	Ω	Pull-up resistance without leakage.
Driver V_{OL}	$-0.1 \times V_{I/O}$		$0.2 \times V_{I/O}$	mV	Output pad driver levels.
Driver V_{OH}	$0.8 \times V_{I/O}$		$1.1 \times V_{I/O}$	mV	Output pad driver levels.
Duty Cycle distortion at 533 MHz with a 2 pF load	44.8	0	55.2	%	
Rise/Fall Time (10% - 90% of V_{DOUT} with a 2 pF load)	100	300	500	ps	

Table 6-10 lists the default settings for the internal SPI pull-up and pull-down resistors.

Table 6-10. Default SPI Settings

Function	SCM Pin	Pull-Up Internal Value	Pull-Down Internal Value
SPIVID0_MOSI	H29	–	–
SPIVID0_MISO	J30	–	–
SPIVID0_SCLK	H28	–	10K
SPIVID0_CS	J28	1K	–
SPIPSS_MOSI	Y37	–	–
SPIPSS_MISO	V37	–	–
SPIPSS_SCLK	AA39	–	10K
SPIPSS_CS0	AA38	1K	–
SPIPSS_CS1	AA37	1K	–

7. Mechanical Specifications

This section describes the POWER8 module SCM features and pin list.

7.1 Single-Chip Module

Table 7-1 describes the single-chip module (SCM).

Table 7-1. SCM Features

Feature	Description
Body Size	50 x 50 mm
Interconnect Technology	22 nm SOI
	1.0 mm orthogonal pin pitch
	6-2-6 LGA
Buses	4 DMI interfaces at 9.6 Gb/s
	Three 2-byte A buses at 6.4 Gb/s
	2 x 16 PCI Express Generation 3 at 8 Gb/s
Power	190 W
Package Pin Assignments	2296 total
SEEPROM Structure	Single SEEPROM

7.2 Electrostatic Discharge Considerations

This product is electrostatic discharge (ESD) sensitive. An appropriate ESD handling procedure must be implemented and maintained by facilities handling this component. Handle according to the ANSI/ESD S20.20 or IEC 61340-5-1. Packaging of this product in an ESD safe container should be according to ANSI/ESD S541 or IEC 61340-5-3.

7.3 Mechanical Drawings

Check IBM Customer Connect for the current mechanical drawings and recommended module layout.

7.4 Pinout

Table 7-2 SCM Pin List on page 53 shows the signal pins for the POWER8 processor by position.

Table 7-2. SCM Pin List

Position	Net Name
A04	GND
A05	MM_PIN_P_M0_CKD_DAT_10_P
A06	MM_PIN_P_M0_CKD_DAT_10_N
A07	GND
A08	MM_PIN_P_M0_CKD_DAT_13_P
A09	MM_PIN_P_M0_CKD_DAT_13_N
A10	MM_PIN_P_M0_CKD_DAT_17_N
A11	MM_PIN_P_M0_CKD_DAT_17_P
A12	GND
A13	GND
A14	MM_PIN_P_M0_CKC_DAT_02_P
A15	MM_PIN_P_M0_CKC_DAT_02_N
A16	GND
A17	MM_PIN_P_M0_CKC_DAT_05_P
A18	MM_PIN_P_M0_CKC_DAT_05_N
A19	MM_PIN_P_M0_CKC_DAT_09_P
A20	MM_PIN_P_M0_CKC_DAT_09_N
A21	GND
A22	MM_PIN_P_M0_CKC_CLK_P
A23	MM_PIN_P_M0_CKC_CLK_N
A24	MM_PIN_P_M0_CKC_DAT_15_P
A25	MM_PIN_P_M0_CKC_DAT_15_N
A26	GND
A27	MM_PIN_P_M0_CKC_DAT_19_N
A28	MM_PIN_P_M0_CKC_DAT_19_P
A29	GND
A30	GND
A31	PE_E0_P_PIN_CK1_DAT_06_N
A32	PE_E0_P_PIN_CK1_DAT_06_P
A33	GND
A34	PE_E0_P_PIN_CK1_DAT_04_P
A35	PE_E0_P_PIN_CK1_DAT_04_N
A36	PE_E0_P_PIN_CK1_DAT_02_P
A37	PE_E0_P_PIN_CK1_DAT_02_N
A38	GND
A39	GND
A40	PE_PIN_P_E0_CK1_DAT_06_N
A41	PE_PIN_P_E0_CK1_DAT_06_P

Position	Net Name
A42	PE_PIN_P_E0_CK1_DAT_04_P
A43	PE_PIN_P_E0_CK1_DAT_04_N
A44	GND
A45	GND
A46	NA_A0_P_PIN_CK0_DAT_03_N
A47	NA_A0_P_PIN_CK0_DAT_03_P
A48	GND
AA01	NC_VDD
AA02	NC_VDD
AA03	NC_VDD
AA04	NC_VDD
AA05	NC_VDD
AA06	NC_VDD
AA07	NC_VDD
AA08	NC_VDD
AA09	NC_VDD
AA10	NC_VDD
AA11	NC_VDD
AA12	NC_VDD
AA13	GND
AA14	#VDD_0P89
AA15	GND
AA16	#VDD_0P89
AA17	GND
AA18	#VDD_0P89
AA19	GND
AA20	#VDD_0P89
AA21	GND
AA22	#VDD_0P89
AA23	GND
AA24	#VDD_0P89
AA25	GND
AA26	#VDD_0P89
AA27	GND
AA28	#VDD_0P89
AA29	GND
AA30	#VDD_0P89
AA31	GND

Position	Net Name
AA32	#VDD_0P89
AA33	GND
AA34	#VDD_0P89
AA35	#VIO_1P10
AA36	GND
AA37	PV_CT_P_PIN_SPIADC_CS1
AA38	PV_CT_P_PIN_SPIADC_CS0
AA39	PV_CT_P_PIN_SPIADC_SCLK
AA40	GND
AA41	NA_A2_P_PIN_CK0_DAT_22_N
AA42	NA_A1_P_PIN_CK0_DAT_21_P
AA43	GND
AA44	NA_A2_P_PIN_CK0_DAT_18_N
AA45	NA_A2_P_PIN_CK0_DAT_16_P
AA46	NA_A2_P_PIN_CK0_DAT_15_N
AA47	NA_A2_P_PIN_CK0_DAT_12_P
AA48	GND
AB01	NC_VDD
AB02	NC_VDD
AB03	NC_VDD
AB04	NC_VDD
AB05	NC_VDD
AB06	NC_VDD
AB07	NC_VDD
AB08	NC_VDD
AB09	NC_VDD
AB10	NC_VDD
AB11	GND
AB12	GND
AB13	NC_VDD
AB14	GND
AB15	#VDD_0P89
AB16	GND
AB17	#VDD_0P89
AB18	GND
AB19	#VCS_0P97
AB20	GND
AB21	#VDD_0P89

Position	Net Name
AB22	#VCS_0P97
AB23	#VDD_0P89
AB24	#VIO_1P10
AB25	TS_CT_P_PIN_PFAMX_VSENSE
AB26	GND
AB27	#VCS_0P97
AB28	GND
AB29	#VDD_0P89
AB30	#VCS_0P97
AB31	#VDD_0P89
AB32	GND
AB33	#VDD_0P89
AB34	GND
AB35	GND
AB36	#VIO_1P10
AB37	GND
AB38	GND
AB39	GND
AB40	GND
AB41	NA_A2_P_PIN_CK0_DAT_22_P
AB42	GND
AB43	NA_A2_P_PIN_CK0_DAT_20_N
AB44	NA_A2_P_PIN_CK0_DAT_18_P
AB45	NA_A2_P_PIN_CK0_DAT_17_N
AB46	NA_A2_P_PIN_CK0_DAT_15_P
AB47	GND
AB48	NA_A2_P_PIN_CK0_DAT_14_N
AC01	NC_VDD
AC02	NC_VDD
AC03	NC_VDD
AC04	NC_VDD
AC05	NC_VDD
AC06	NC_VDD
AC07	NC_VDD
AC08	PV_MSOP_M_CT_VREF_N
AC09	PV_MSOP_M_CT_VREF_P
AC10	GND
AC11	#DVDD_1P50

Position	Net Name
AC12	#DVDD_1P50
AC13	GND
AC14	#VDD_0P89
AC15	GND
AC16	#VDD_0P89
AC17	GND
AC18	#VDD_0P89
AC19	GND
AC20	#VDD_0P89
AC21	GND
AC22	#VDD_0P89
AC23	GND
AC24	TS_CT_P_PIN_VCAL
AC25	TS_CT_P_PIN_PFAMX_GSENSE
AC26	#VDD_0P89
AC27	GND
AC28	#VDD_0P89
AC29	GND
AC30	#VDD_0P89
AC31	GND
AC32	#VDD_0P89
AC33	GND
AC34	#VDD_0P89
AC35	#VIO_1P10
AC36	GND
AC37	PE_CT_P_PIN_E0_SLOT_CLK0_N
AC38	GND
AC39	GND
AC40	GND
AC41	GND
AC42	NA_A2_P_PIN_CK0_DAT_21_N
AC43	NA_A2_P_PIN_CK0_DAT_20_P
AC44	NA_A2_P_PIN_CK0_DAT_19_N
AC45	NA_A2_P_PIN_CK0_DAT_17_P
AC46	GND
AC47	GND
AC48	NA_A2_P_PIN_CK0_DAT_14_P
AD01	NC_VDD

Position	Net Name
AD02	NC_VDD
AD03	NC_VDD
AD04	NC_VDD
AD05	GND
AD06	GND
AD07	GND
AD08	GND
AD09	GND
AD10	GND
AD11	#AVDD_1P50
AD12	#AVDD_1P50
AD13	#VIO_1P10
AD14	#VIO_1P10
AD15	#VDD_0P89
AD16	GND
AD17	#VDD_0P89
AD18	#VIO_1P10
AD19	#VDD_0P89
AD20	GND
AD21	#VDD_0P89
AD22	#VIO_1P10
AD23	#VDD_0P89
AD24	GND
AD25	#VIO_1P10
AD26	GND
AD27	#VDD_0P89
AD28	GND
AD29	#VIO_1P10
AD30	GND
AD31	#VDD_0P89
AD32	GND
AD33	#VIO_1P10
AD34	GND
AD35	GND
AD36	#VIO_1P10
AD37	PE_CT_P_PIN_E0_SLOT_CLK0_P
AD38	GND

Position	Net Name
AD39	PV_PIN_P_CT_OSC0_E_REFCLK_N
AD40	PV_PIN_P_CT_OSC0_E_REFCLK_P
AD41	GND
AD42	NA_A2_P_PIN_CK0_DAT_21_P
AD43	GND
AD44	NA_A2_P_PIN_CK0_DAT_19_P
AD45	GND
AD46	GND
AD47	GND
AD48	GND
AE01	GND
AE02	GND
AE03	GND
AE04	GND
AE05	NC_VDD
AE06	NC_VDD
AE07	NC_VDD
AE08	NC_VDD
AE09	NC_VDD
AE10	GND
AE11	GND
AE12	GND
AE13	GND
AE14	#VDD_0P89
AE15	GND
AE16	#VIO_1P10
AE17	GND
AE18	#VDD_0P89
AE19	GND
AE20	#VIO_1P10
AE21	GND
AE22	#VDD_0P89
AE23	GND
AE24	#VIO_1P10
AE25	GND
AE26	#VDD_0P89
AE27	#VIO_1P10

Position	Net Name
AE28	#VDD_0P89
AE29	GND
AE30	#VDD_0P89
AE31	#VIO_1P10
AE32	#VDD_0P89
AE33	GND
AE34	#VDD_0P89
AE35	#VIO_1P10
AE36	GND
AE37	GND
AE38	GND
AE39	GND
AE40	GND
AE41	GND
AE42	GND
AE43	GND
AE44	GND
AE45	GND
AE46	GND
AE47	NA_PIN_P_A0_CK0_DAT_06_N
AE48	GND
AF01	NC_VDD
AF02	NC_VDD
AF03	NC_VDD
AF04	NC_VDD
AF05	NC_VDD
AF06	NC_VDD
AF07	NC_VDD
AF08	NC_VDD
AF09	NC_VDD
AF10	NC_VDD
AF11	NC_VDD
AF12	NC_VDD
AF13	NC_VDD
AF14	GND
AF15	#VDD_0P89
AF16	GND
AF17	#VDD_0P89

Position	Net Name
AF18	GND
AF19	#VDD_0P89
AF20	GND
AF21	#VDD_0P89
AF22	GND
AF23	#VDD_0P89
AF24	GND
AF25	#VDD_0P89
AF26	GND
AF27	#VDD_0P89
AF28	GND
AF29	#VDD_0P89
AF30	GND
AF31	#VDD_0P89
AF32	GND
AF33	#VDD_0P89
AF34	GND
AF35	GND
AF36	#VIO_1P10
AF37	GND
AF38	PE_CT_P_PIN_E1_SLOT_CLK0_N
AF39	GND
AF40	NA_PIN_P_A1_CK0_DAT_00_N
AF41	GND
AF42	GND
AF43	NA_PIN_P_A0_CK0_DAT_01_P
AF44	GND
AF45	NA_PIN_P_A0_CK0_DAT_04_N
AF46	GND
AF47	NA_PIN_P_A0_CK0_DAT_06_P
AF48	NA_PIN_P_A0_CK0_DAT_10_N
AG01	NC_VDD
AG02	NC_VDD
AG03	NC_VDD
AG04	NC_VDD
AG05	NC_VDD
AG06	NC_VDD
AG07	NC_VDD

Position	Net Name
AG08	NC_VDD
AG09	NC_VDD
AG10	NC_VDD
AG11	NC_VDD
AG12	NC_VDD
AG13	GND
AG14	#VDD_0P89
AG15	GND
AG16	#VDD_0P89
AG17	GND
AG18	#VDD_0P89
AG19	#VCS_0P97
AG20	#VDD_0P89
AG21	GND
AG22	#VCS_0P97
AG23	GND
AG24	#VDD_0P89
AG25	#VIO_1P10
AG26	#VDD_0P89
AG27	#VCS_0P97
AG28	#VDD_0P89
AG29	GND
AG30	#VCS_0P97
AG31	GND
AG32	#VDD_0P89
AG33	GND
AG34	#VDD_0P89
AG35	#VIO_1P10
AG36	GND
AG37	PE_CT_P_PIN_E1_SLOT_CLK1_N
AG38	PE_CT_P_PIN_E1_SLOT_CLK0_P
AG39	GND
AG40	NA_PIN_P_A1_CK0_DAT_00_P
AG41	NA_PIN_P_A1_CK0_DAT_01_N
AG42	GND
AG43	NA_PIN_P_A0_CK0_DAT_01_N
AG44	NA_PIN_P_A0_CK0_DAT_03_N

Position	Net Name
AG45	NA_PIN_P_A0_CK0_DAT_04_P
AG46	NA_PIN_P_A0_CK0_DAT_07_N
AG47	GND
AG48	NA_PIN_P_A0_CK0_DAT_10_P
AH01	NC_VDD
AH02	NC_VDD
AH03	NC_VDD
AH04	NC_VDD
AH05	NC_VDD
AH06	NC_VDD
AH07	NC_VDD
AH08	NC_VDD
AH09	NC_VDD
AH10	NC_VDD
AH11	NC_VDD
AH12	NC_VDD
AH13	#VIO_1P10
AH14	GND
AH15	#VDD_0P89
AH16	GND
AH17	#VDD_0P89
AH18	GND
AH19	#VDD_0P89
AH20	GND
AH21	#VDD_0P89
AH22	GND
AH23	#VDD_0P89
AH24	GND
AH25	#VDD_0P89
AH26	GND
AH27	#VDD_0P89
AH28	GND
AH29	#VDD_0P89
AH30	GND
AH31	#VDD_0P89
AH32	GND
AH33	#VDD_0P89
AH34	GND

Position	Net Name
AH35	GND
AH36	#VIO_1P10
AH37	PE_CT_P_PIN_E1_SLOT_CLK1_P
AH38	GND
AH39	GND
AH40	NA_PIN_P_A1_CK0_DAT_02_N
AH41	NA_PIN_P_A1_CK0_DAT_01_P
AH42	GND
AH43	GND
AH44	NA_PIN_P_A0_CK0_DAT_03_P
AH45	NA_PIN_P_A0_CK0_DAT_05_N
AH46	NA_PIN_P_A0_CK0_DAT_07_P
AH47	NA_PIN_P_A0_CK0_DAT_09_N
AH48	GND
AJ01	NC_VDD
AJ02	NC_VDD
AJ03	NC_VDD
AJ04	NC_VDD
AJ05	NC_VDD
AJ06	NC_VDD
AJ07	GND
AJ08	#VSB_3P30
AJ09	#VSB_3P30
AJ10	GND
AJ11	GND
AJ12	GND
AJ13	GND
AJ14	#VDD_0P89
AJ15	GND
AJ16	#VDD_0P89
AJ17	GND
AJ18	#VDD_0P89
AJ19	#VCS_0P97
AJ20	#VDD_0P89
AJ21	GND
AJ22	#VCS_0P97
AJ23	GND
AJ24	#VIO_1P10

Position	Net Name
AJ25	GND
AJ26	#VDD_0P89
AJ27	#VCS_0P97
AJ28	#VDD_0P89
AJ29	GND
AJ30	#VCS_0P97
AJ31	GND
AJ32	#VDD_0P89
AJ33	GND
AJ34	#VDD_0P89
AJ35	#VIO_1P10
AJ36	GND
AJ37	GND
AJ38	TS_CT_P_PIN_A1_MKERF_N
AJ39	GND
AJ40	NA_PIN_P_A1_CK0_DAT_02_P
AJ41	NA_PIN_P_A1_CK0_DAT_03_N
AJ42	GND
AJ43	NA_PIN_P_A0_CK0_DAT_00_P
AJ44	GND
AJ45	NA_PIN_P_A0_CK0_DAT_05_P
AJ46	NA_PIN_P_A0_CK0_CLK_N
AJ47	NA_PIN_P_A0_CK0_DAT_09_P
AJ48	NA_PIN_P_A0_CK0_DAT_11_N
AK01	GND
AK02	GND
AK03	GND
AK04	GND
AK05	GND
AK06	GND
AK07	MM_M1_P_PIN_CKD_DAT_04_P
AK08	GND
AK09	TS_CT_P_PIN_PXFM_PLL_HFC_N
AK10	TS_CT_P_PIN_PXFM_PLL_HFC_P
AK11	GND
AK12	PV_CT_P_PIN_PSI_CLK_P
AK13	#VIO_1P10

Position	Net Name
AK14	GND
AK15	#VDD_0P89
AK16	GND
AK17	#VDD_0P89
AK18	GND
AK19	#VDD_0P89
AK20	GND
AK21	#VDD_0P89
AK22	GND
AK23	#VDD_0P89
AK24	GND
AK25	#VDD_0P89
AK26	GND
AK27	#VDD_0P89
AK28	GND
AK29	#VDD_0P89
AK30	GND
AK31	#VDD_0P89
AK32	GND
AK33	#VDD_0P89
AK34	GND
AK35	GND
AK36	#VIO_1P10
AK37	GND
AK38	TS_CT_P_PIN_A1_MKERF_P
AK39	NA_PIN_P_A1_CK0_DAT_04_N
AK40	GND
AK41	NA_PIN_P_A1_CK0_DAT_03_P
AK42	GND
AK43	NA_PIN_P_A0_CK0_DAT_00_N
AK44	NA_PIN_P_A0_CK0_DAT_08_N
AK45	GND
AK46	NA_PIN_P_A0_CK0_CLK_P
AK47	NA_PIN_P_A0_CK0_DAT_12_N
AK48	NA_PIN_P_A0_CK0_DAT_11_P
AL01	MM_M1_P_PIN_CKD_DAT_07_P
AL02	GND
AL03	GND

Position	Net Name
AL04	MM_M1_P_PIN_CKD_CLK_P
AL05	GND
AL06	MM_M1_P_PIN_CKD_DAT_05_P
AL07	MM_M1_P_PIN_CKD_DAT_04_N
AL08	GND
AL09	MM_PIN_P_CT_M1_FAULT_C_N
AL10	GND
AL11	PV_CT_P_PIN_PSI_DATA
AL12	PV_CT_P_PIN_PSI_CLK_N
AL13	GND
AL14	#VDD_0P89
AL15	GND
AL16	#VDD_0P89
AL17	TS_CT_P_PIN_TDIODE_C5
AL18	TS_CT_P_PIN_TDIODE_A5
AL19	#VCS_0P97
AL20	#VDD_0P89
AL21	GND
AL22	#VCS_0P97
AL23	GND
AL24	#VDD_0P89
AL25	#VIO_1P10
AL26	#VDD_0P89
AL27	#VCS_0P97
AL28	#VDD_0P89
AL29	GND
AL30	#VCS_0P97
AL31	TS_CT_P_PIN_TDIODE_A13
AL32	TS_CT_P_PIN_TDIODE_C13
AL33	GND
AL34	#VDD_0P89
AL35	#VIO_1P10
AL36	GND
AL37	PV_CT_B_PIN_PCI_I2C_SDA_B
AL38	GND
AL39	NA_PIN_P_A1_CK0_DAT_04_P
AL40	NA_PIN_P_A1_CK0_DAT_05_N
AL41	GND

Position	Net Name
AL42	GND
AL43	NA_PIN_P_A0_CK0_DAT_02_P
AL44	NA_PIN_P_A0_CK0_DAT_08_P
AL45	NA_PIN_P_A0_CK0_DAT_13_N
AL46	GND
AL47	NA_PIN_P_A0_CK0_DAT_12_P
AL48	NA_PIN_P_A0_CK0_DAT_14_N
AM01	MM_M1_P_PIN_CKD_DAT_07_N
AM02	GND
AM03	MM_M1_P_PIN_CKD_DAT_09_N
AM04	MM_M1_P_PIN_CKD_CLK_N
AM05	MM_M1_P_PIN_CKD_DAT_08_N
AM06	MM_M1_P_PIN_CKD_DAT_05_N
AM07	GND
AM08	MM_M1_P_PIN_CKD_DAT_02_P
AM09	GND
AM10	MM_PIN_P_CT_M1_FAULT_D_N
AM11	GND
AM12	GND
AM13	#VIO_1P10
AM14	GND
AM15	#VDD_0P89
AM16	GND
AM17	#VDD_0P89
AM18	GND
AM19	#VDD_0P89
AM20	GND
AM21	#VDD_0P89
AM22	GND
AM23	#VDD_0P89
AM24	GND
AM25	TS_CT_P_PIN_AMX1_GSENSE
AM26	GND
AM27	#VDD_0P89
AM28	GND
AM29	#VDD_0P89
AM30	GND
AM31	#VDD_0P89

Position	Net Name
AM32	GND
AM33	#VDD_0P89
AM34	GND
AM35	GND
AM36	#VIO_1P10
AM37	PV_CT_B_PIN_PCI_I2C_SCL_B
AM38	GND
AM39	NA_PIN_P_A1_CK0_DAT_06_N
AM40	NA_PIN_P_A1_CK0_DAT_05_P
AM41	NA_PIN_P_A1_CK0_DAT_07_N
AM42	GND
AM43	NA_PIN_P_A0_CK0_DAT_02_N
AM44	NA_PIN_P_A0_CK0_DAT_15_N
AM45	NA_PIN_P_A0_CK0_DAT_13_P
AM46	NA_PIN_P_A0_CK0_DAT_18_N
AM47	GND
AM48	NA_PIN_P_A0_CK0_DAT_14_P
AN01	GND
AN02	MM_M1_P_PIN_CKD_DAT_12_N
AN03	MM_M1_P_PIN_CKD_DAT_09_P
AN04	MM_M1_P_PIN_CKD_DAT_11_N
AN05	MM_M1_P_PIN_CKD_DAT_08_P
AN06	GND
AN07	MM_M1_P_PIN_CKD_DAT_03_P
AN08	MM_M1_P_PIN_CKD_DAT_02_N
AN09	MM_M1_P_PIN_CKD_DAT_00_P
AN10	GND
AN11	PV_PIN_P_CT_PSI_DATA
AN12	PV_PIN_P_CT_PSI_CLK_N
AN13	GND
AN14	#VDD_0P89
AN15	GND
AN16	#VDD_0P89
AN17	GND
AN18	#VDD_0P89
AN19	GND
AN20	#VDD_0P89
AN21	GND

Position	Net Name
AN22	#VDD_0P89
AN23	GND
AN24	#VIO_1P10
AN25	TS_CT_P_PIN_AMX1_VSENSE
AN26	#VDD_0P89
AN27	GND
AN28	#VDD_0P89
AN29	GND
AN30	#VDD_0P89
AN31	GND
AN32	#VDD_0P89
AN33	GND
AN34	#VDD_0P89
AN35	#VIO_1P10
AN36	#VPCI_1P20
AN37	GND
AN38	GND
AN39	NA_PIN_P_A1_CK0_DAT_06_P
AN40	NA_PIN_P_A1_CK0_DAT_08_N
AN41	NA_PIN_P_A1_CK0_DAT_07_P
AN42	NA_PIN_P_A1_CK0_DAT_09_N
AN43	GND
AN44	NA_PIN_P_A0_CK0_DAT_15_P
AN45	NA_PIN_P_A0_CK0_DAT_22_N
AN46	NA_PIN_P_A0_CK0_DAT_18_P
AN47	NA_PIN_P_A0_CK0_DAT_16_N
AN48	GND
AP01	MM_M1_P_PIN_CKD_DAT_10_N
AP02	MM_M1_P_PIN_CKD_DAT_12_P
AP03	MM_M1_P_PIN_CKD_DAT_13_N
AP04	MM_M1_P_PIN_CKD_DAT_11_P
AP05	GND
AP06	MM_M1_P_PIN_CKD_DAT_06_P
AP07	MM_M1_P_PIN_CKD_DAT_03_N
AP08	MM_M1_P_PIN_CKD_DAT_01_P
AP09	MM_M1_P_PIN_CKD_DAT_00_N
AP10	TS_CT_P_PIN_PXFM_PLL_ANATST
AP11	GND

Position	Net Name
AP12	PV_PIN_P_CT_PSI_CLK_P
AP13	#VIO_1P10
AP14	GND
AP15	#VDD_0P89
AP16	GND
AP17	#VDD_0P89
AP18	GND
AP19	#VCS_0P97
AP20	GND
AP21	#VDD_0P89
AP22	#VCS_0P97
AP23	#VDD_0P89
AP24	GND
AP25	TS_PIN_P_CT_EFUSE_FSOURCE
AP26	GND
AP27	#VCS_0P97
AP28	GND
AP29	#VDD_0P89
AP30	#VCS_0P97
AP31	#VDD_0P89
AP32	GND
AP33	#VDD_0P89
AP34	GND
AP35	#VPCI_1P20
AP36	GND
AP37	GND
AP38	GND
AP39	GND
AP40	NA_PIN_P_A1_CK0_DAT_08_P
AP41	NA_PIN_P_A1_CK0_DAT_10_N
AP42	NA_PIN_P_A1_CK0_DAT_09_P
AP43	NA_PIN_P_A1_CK0_DAT_11_N
AP44	GND
AP45	NA_PIN_P_A0_CK0_DAT_22_P
AP46	NA_PIN_P_A0_CK0_DAT_20_N
AP47	NA_PIN_P_A0_CK0_DAT_16_P
AP48	NA_PIN_P_A0_CK0_DAT_17_N
AR01	MM_M1_P_PIN_CKD_DAT_10_P

Position	Net Name
AR02	MM_M1_P_PIN_CKD_DAT_14_N
AR03	MM_M1_P_PIN_CKD_DAT_13_P
AR04	GND
AR05	MM_M1_P_PIN_CKD_DAT_15_N
AR06	MM_M1_P_PIN_CKD_DAT_06_N
AR07	GND
AR08	MM_M1_P_PIN_CKD_DAT_01_N
AR09	GND
AR10	PV_PIN_P_CT_TPM_INTERRUPT
AR11	TS_PIN_P_CT_TST_FORCE_PWR_ON
AR12	GND
AR13	GND
AR14	#VDD_0P89
AR15	GND
AR16	#VDD_0P89
AR17	GND
AR18	#VDD_0P89
AR19	GND
AR20	#VDD_0P89
AR21	GND
AR22	#VDD_0P89
AR23	GND
AR24	#VDD_0P89
AR25	#VIO_1P10
AR26	#VDD_0P89
AR27	GND
AR28	#VDD_0P89
AR29	GND
AR30	#VDD_0P89
AR31	GND
AR32	#VDD_0P89
AR33	GND
AR34	#VDD_0P89
AR35	#VIO_1P10
AR36	#VPCI_1P20
AR37	TS_CT_P_PIN_PE1_PLL_ANATST
AR38	PV_PIN_P_CT_E1_TERMREF_N

Position	Net Name
AR39	NA_PIN_P_A2_CK0_DAT_00_N
AR40	GND
AR41	NA_PIN_P_A1_CK0_DAT_10_P
AR42	NA_PIN_P_A1_CK0_CLK_N
AR43	NA_PIN_P_A1_CK0_DAT_11_P
AR44	NA_PIN_P_A1_CK0_DAT_13_N
AR45	GND
AR46	NA_PIN_P_A0_CK0_DAT_20_P
AR47	NA_PIN_P_A0_CK0_DAT_19_N
AR48	NA_PIN_P_A0_CK0_DAT_17_P
AT01	MM_M1_P_PIN_CKD_DAT_16_N
AT02	MM_M1_P_PIN_CKD_DAT_14_P
AT03	GND
AT04	MM_M1_P_PIN_CKC_DAT_13_P
AT05	MM_M1_P_PIN_CKD_DAT_15_P
AT06	GND
AT07	MM_M1_P_PIN_CKC_DAT_00_P
AT08	GND
AT09	GND
AT10	PV_CT_P_PIN_TPM_RESET
AT11	GND
AT12	MM_CT_P_PIN_MB_MEM_REFCLK7_P
AT13	#VIO_1P10
AT14	GND
AT15	#VDD_0P89
AT16	GND
AT17	#VDD_0P89
AT18	GND
AT19	#VCS_0P97
AT20	GND
AT21	#VDD_0P89
AT22	#VCS_0P97
AT23	#VDD_0P89
AT24	GND
AT25	#VDD_0P89
AT26	GND
AT27	#VCS_0P97
AT28	GND

Position	Net Name
AT29	#VDD_0P89
AT30	#VCS_0P97
AT31	#VDD_0P89
AT32	GND
AT33	#VDD_0P89
AT34	GND
AT35	#VPCI_1P20
AT36	GND
AT37	GND
AT38	PV_PIN_P_CT_E1_TERMREF_P
AT39	NA_PIN_P_A2_CK0_DAT_00_P
AT40	NA_PIN_P_A2_CK0_DAT_02_N
AT41	GND
AT42	NA_PIN_P_A1_CK0_CLK_P
AT43	NA_PIN_P_A1_CK0_DAT_12_N
AT44	NA_PIN_P_A1_CK0_DAT_13_P
AT45	NA_PIN_P_A1_CK0_DAT_15_N
AT46	GND
AT47	NA_PIN_P_A0_CK0_DAT_19_P
AT48	NA_PIN_P_A0_CK0_DAT_21_N
AU01	MM_M1_P_PIN_CKD_DAT_16_P
AU02	GND
AU03	MM_M1_P_PIN_CKC_DAT_16_N
AU04	MM_M1_P_PIN_CKC_DAT_13_N
AU05	GND
AU06	MM_M1_P_PIN_CKC_DAT_02_P
AU07	MM_M1_P_PIN_CKC_DAT_00_N
AU08	GND
AU09	MM_CT_P_PIN_MB_NEST_REFCLK6_P
AU10	GND
AU11	MM_CT_P_PIN_MB_MEM_REFCLK6_N
AU12	MM_CT_P_PIN_MB_MEM_REFCLK7_N
AU13	GND
AU14	#VDD_0P89
AU15	GND
AU16	#VDD_0P89
AU17	GND

Position	Net Name
AU18	#VDD_0P89
AU19	GND
AU20	#VDD_0P89
AU21	GND
AU22	#VDD_0P89
AU23	GND
AU24	#VIO_1P10
AU25	GND
AU26	#VDD_0P89
AU27	GND
AU28	#VDD_0P89
AU29	GND
AU30	#VDD_0P89
AU31	GND
AU32	#VDD_0P89
AU33	GND
AU34	#VDD_0P89
AU35	#VIO_1P10
AU36	#VPCI_1P20
AU37	PE_CT_P_PIN_E1_PERST1_B
AU38	GND
AU39	NA_PIN_P_A2_CK0_DAT_01_N
AU40	NA_PIN_P_A2_CK0_DAT_02_P
AU41	NA_PIN_P_A2_CK0_DAT_04_N
AU42	GND
AU43	NA_PIN_P_A1_CK0_DAT_12_P
AU44	NA_PIN_P_A1_CK0_DAT_14_N
AU45	NA_PIN_P_A1_CK0_DAT_15_P
AU46	NA_PIN_P_A1_CK0_DAT_17_N
AU47	GND
AU48	NA_PIN_P_A0_CK0_DAT_21_P
AV01	GND
AV02	MM_M1_P_PIN_CKC_DAT_15_N
AV03	MM_M1_P_PIN_CKC_DAT_16_P
AV04	GND
AV05	MM_M1_P_PIN_CKC_DAT_04_P
AV06	MM_M1_P_PIN_CKC_DAT_02_N
AV07	MM_M1_P_PIN_CKC_DAT_01_P

Position	Net Name
AV08	GND
AV09	MM_CT_P_PIN_MB_NEST_REFCLK6_N
AV10	MM_CT_P_PIN_MB_NEST_REFCLK7_P
AV11	MM_CT_P_PIN_MB_MEM_REFCLK6_P
AV12	GND
AV13	#VIO_1P10
AV14	GND
AV15	#VIO_1P10
AV16	GND
AV17	#VIO_1P10
AV18	GND
AV19	#VIO_1P10
AV20	GND
AV21	#VIO_1P10
AV22	GND
AV23	#VIO_1P10
AV24	GND
AV25	#VIO_1P10
AV26	GND
AV27	#VIO_1P10
AV28	GND
AV29	#VIO_1P10
AV30	GND
AV31	#VSB_1P20
AV32	GND
AV33	#VSB_1P20
AV34	GND
AV35	#VPCI_1P20
AV36	GND
AV37	PE_CT_P_PIN_E1_PERST0_B
AV38	GND
AV39	NA_PIN_P_A2_CK0_DAT_01_P
AV40	NA_PIN_P_A2_CK0_DAT_03_N
AV41	NA_PIN_P_A2_CK0_DAT_04_P
AV42	NA_PIN_P_A2_CK0_DAT_06_N
AV43	GND
AV44	NA_PIN_P_A1_CK0_DAT_14_P

Position	Net Name
AV45	NA_PIN_P_A1_CK0_DAT_16_N
AV46	NA_PIN_P_A1_CK0_DAT_17_P
AV47	NA_PIN_P_A1_CK0_DAT_19_N
AV48	GND
AW01	MM_M1_P_PIN_CKC_DAT_14_N
AW02	MM_M1_P_PIN_CKC_DAT_15_P
AW03	GND
AW04	MM_M1_P_PIN_CKC_DAT_06_P
AW05	MM_M1_P_PIN_CKC_DAT_04_N
AW06	MM_M1_P_PIN_CKC_DAT_03_P
AW07	MM_M1_P_PIN_CKC_DAT_01_N
AW08	GND
AW09	GND
AW10	MM_CT_P_PIN_MB_NEST_REFCLK7_N
AW11	GND
AW12	SH_PIN_P_M1_CKB_DAT_03_P
AW13	GND
AW14	#VIO_1P10
AW15	GND
AW16	#VIO_1P10
AW17	GND
AW18	#VIO_1P10
AW19	GND
AW20	#VIO_1P10
AW21	GND
AW22	#VIO_1P10
AW23	GND
AW24	#VIO_1P10
AW25	GND
AW26	PV_PIN_P_CT_VIO_PGOOD
AW27	GND
AW28	#VIO_1P10
AW29	GND
AW30	#VIO_1P10
AW31	PV_CT_B_PIN_LPC_DATA_03
AW32	PV_CT_B_PIN_LPC_DATA_01
AW33	PV_CT_P_PIN_LPC_FRAME_B
AW34	PV_PIN_P_CT_LPC_RESET_B

Position	Net Name
AW35	#VIO_1P10
AW36	PV_PIN_P_CT_LPC_CLK
AW37	GND
AW38	SH_CT_P_PIN_MB_FSI1_CLK
AW39	GND
AW40	NA_PIN_P_A2_CK0_DAT_03_P
AW41	NA_PIN_P_A2_CK0_DAT_05_N
AW42	NA_PIN_P_A2_CK0_DAT_06_P
AW43	NA_PIN_P_A2_CK0_DAT_08_N
AW44	GND
AW45	NA_PIN_P_A1_CK0_DAT_16_P
AW46	NA_PIN_P_A1_CK0_DAT_18_N
AW47	NA_PIN_P_A1_CK0_DAT_19_P
AW48	NA_PIN_P_A1_CK0_DAT_21_N
AY01	MM_M1_P_PIN_CKC_DAT_14_P
AY02	GND
AY03	MM_M1_P_PIN_CKC_DAT_08_N
AY04	MM_M1_P_PIN_CKC_DAT_06_N
AY05	MM_M1_P_PIN_CKC_DAT_05_P
AY06	MM_M1_P_PIN_CKC_DAT_03_N
AY07	GND
AY08	PV_CT_M_PIN_SEEPROM0_CLK
AY09	SH_PIN_P_M1_CKB_DAT_12_P
AY10	GND
AY11	GND
AY12	SH_PIN_P_M1_CKB_DAT_14_P
AY13	SH_PIN_P_M1_CKB_DAT_10_P
AY14	GND
AY15	SH_PIN_P_M1_CKB_DAT_01_P
AY16	TS_CT_P_PIN_PROBE2
AY17	TS_CT_P_PIN_PROBE4
AY18	TS_CT_P_PIN_M1_PLL_ANATST
AY19	GND
AY20	TS_CT_P_PIN_PROBE3
AY21	PV_CT_P_PIN_SPARE0
AY22	GND
AY23	MM_CT_P_PIN_MB_FSI3_CLK
AY24	MM_CT_B_PIN_MB_FSI3_DATA

Position	Net Name
AY25	GND
AY26	PV_CT_B_PIN_LP_I2C_SCL_B
AY27	PV_CT_B_PIN_LP_I2C_SDA_B
AY28	GND
AY29	TS_CT_P_PIN_PROBE0_P
AY30	TS_CT_P_PIN_PROBE0_N
AY31	GND
AY32	PV_CT_B_PIN_LPC_DATA_02
AY33	PV_CT_B_PIN_LPC_DATA_00
AY34	GND
AY35	PE_PIN_P_CT_E1_PRSNT0_B
AY36	GND
AY37	GND
AY38	GND
AY39	SH_CT_B_PIN_MB_FSI1_DATA
AY40	GND
AY41	NA_PIN_P_A2_CK0_DAT_05_P
AY42	NA_PIN_P_A2_CK0_DAT_07_N
AY43	NA_PIN_P_A2_CK0_DAT_08_P
AY44	NA_PIN_P_A2_CK0_DAT_10_N
AY45	GND
AY46	NA_PIN_P_A1_CK0_DAT_18_P
AY47	NA_PIN_P_A1_CK0_DAT_20_N
AY48	NA_PIN_P_A1_CK0_DAT_21_P
B03	GND
B04	MM_PIN_P_M0_CKD_DAT_09_P
B05	MM_PIN_P_M0_CKD_DAT_09_N
B06	MM_PIN_P_M0_CKD_CLK_P
B07	MM_PIN_P_M0_CKD_CLK_N
B08	GND
B09	MM_PIN_P_M0_CKD_DAT_15_P
B10	MM_PIN_P_M0_CKD_DAT_15_N
B11	MM_PIN_P_M0_CKD_DAT_18_N
B12	MM_PIN_P_M0_CKD_DAT_18_P
B13	GND
B14	GND
B15	GND
B16	MM_PIN_P_M0_CKC_DAT_03_P

Position	Net Name
B17	MM_PIN_P_M0_CKC_DAT_03_N
B18	MM_PIN_P_M0_CKC_DAT_06_P
B19	MM_PIN_P_M0_CKC_DAT_06_N
B20	GND
B21	MM_PIN_P_M0_CKC_DAT_10_P
B22	MM_PIN_P_M0_CKC_DAT_10_N
B23	MM_PIN_P_M0_CKC_DAT_12_P
B24	MM_PIN_P_M0_CKC_DAT_12_N
B25	GND
B26	MM_PIN_P_M0_CKC_DAT_16_N
B27	MM_PIN_P_M0_CKC_DAT_16_P
B28	GND
B29	GND
B30	PE_E0_P_PIN_CK1_DAT_07_N
B31	PE_E0_P_PIN_CK1_DAT_07_P
B32	GND
B33	PE_E0_P_PIN_CK1_DAT_05_N
B34	PE_E0_P_PIN_CK1_DAT_05_P
B35	PE_E0_P_PIN_CK1_DAT_03_P
B36	PE_E0_P_PIN_CK1_DAT_03_N
B37	GND
B38	GND
B39	PE_PIN_P_E0_CK1_DAT_07_N
B40	PE_PIN_P_E0_CK1_DAT_07_P
B41	PE_PIN_P_E0_CK1_DAT_05_P
B42	PE_PIN_P_E0_CK1_DAT_05_N
B43	GND
B44	GND
B45	NA_A0_P_PIN_CK0_DAT_02_P
B46	NA_A0_P_PIN_CK0_DAT_02_N
B47	GND
B48	NA_A0_P_PIN_CK0_DAT_05_P
BA01	GND
BA02	MM_M1_P_PIN_CKC_DAT_12_N
BA03	MM_M1_P_PIN_CKC_DAT_08_P
BA04	MM_M1_P_PIN_CKC_DAT_07_P
BA05	MM_M1_P_PIN_CKC_DAT_05_N
BA06	GND

Position	Net Name
BA07	SH_PIN_P_M1_CKB_DAT_15_P
BA08	PV_CT_M_PIN_SEEPROM0_DATA
BA09	GND
BA10	MM_PIN_P_M1_CKD_DAT_00_P
BA11	MM_PIN_P_M1_CKD_DAT_00_N
BA12	GND
BA13	GND
BA14	TS_CT_P_PIN_M1_T_PLLHFC_MKERF_P
BA15	TS_CT_P_PIN_M1_T_PLLHFC_MKERF_N
BA16	GND
BA17	PV_PIN_P_CT_M1_TERMREF_P
BA18	PV_PIN_P_CT_M1_TERMREF_N
BA19	GND
BA20	GND
BA21	MM_CT_B_PIN_MB_FSI7_DATA
BA22	MM_CT_P_PIN_MB_FSI7_CLK
BA23	GND
BA24	MM_CT_B_PIN_MB_FSI2_DATA
BA25	MM_CT_P_PIN_MB_FSI2_CLK
BA26	GND
BA27	PV_PIN_B_CT_I2CSL_SCL
BA28	PV_PIN_B_CT_I2CSL_SDA
BA29	GND
BA30	GND
BA31	GND
BA32	GND
BA33	PE_PIN_P_CT_E1_PRSNT1_B
BA34	GND
BA35	PE_PIN_P_E1_CK0_DAT_00_N
BA36	PE_PIN_P_E1_CK0_DAT_00_P
BA37	PE_PIN_P_E1_CK0_DAT_02_N
BA38	PE_PIN_P_E1_CK0_DAT_02_P
BA39	GND
BA40	SH_PIN_P_CT_FSP1_FSI_CLK
BA41	GND
BA42	NA_PIN_P_A2_CK0_DAT_07_P
BA43	NA_PIN_P_A2_CK0_DAT_09_N

Position	Net Name
BA44	NA_PIN_P_A2_CK0_DAT_10_P
BA45	NA_PIN_P_A2_CK0_DAT_11_N
BA46	GND
BA47	NA_PIN_P_A1_CK0_DAT_20_P
BA48	NA_PIN_P_A1_CK0_DAT_22_N
BB01	MM_M1_P_PIN_CKC_DAT_11_N
BB02	MM_M1_P_PIN_CKC_DAT_12_P
BB03	MM_M1_P_PIN_CKC_CLK_P
BB04	MM_M1_P_PIN_CKC_DAT_07_N
BB05	GND
BB06	SH_PIN_P_M1_CKB_DAT_06_P
BB07	SH_PIN_P_M1_CKB_DAT_13_P
BB08	GND
BB09	MM_PIN_P_M1_CKD_DAT_01_N
BB10	MM_PIN_P_M1_CKD_DAT_01_P
BB11	MM_PIN_P_M1_CKD_DAT_02_P
BB12	MM_PIN_P_M1_CKD_DAT_02_N
BB13	GND
BB14	GND
BB15	GND
BB16	MM_PIN_P_M1_CKC_DAT_07_N
BB17	MM_PIN_P_M1_CKC_DAT_07_P
BB18	MM_PIN_P_M1_CKC_DAT_23_P
BB19	MM_PIN_P_M1_CKC_DAT_23_N
BB20	GND
BB21	GND
BB22	MM_CT_P_PIN_MB_FSI6_CLK
BB23	MM_CT_B_PIN_MB_FSI6_DATA
BB24	GND
BB25	PV_CT_P_PIN_FSI1_CLK
BB26	PV_CT_B_PIN_FSI1_DATA
BB27	GND
BB28	PV_CT_P_PIN_ATTENTION_B
BB29	GND
BB30	PE_E1_P_PIN_CK0_DAT_01_N
BB31	PE_E1_P_PIN_CK0_DAT_01_P
BB32	PE_E1_P_PIN_CK0_DAT_02_N
BB33	PE_E1_P_PIN_CK0_DAT_02_P

Position	Net Name
BB34	GND
BB35	GND
BB36	PE_PIN_P_E1_CK0_DAT_01_N
BB37	PE_PIN_P_E1_CK0_DAT_01_P
BB38	PE_PIN_P_E1_CK0_DAT_04_N
BB39	PE_PIN_P_E1_CK0_DAT_04_P
BB40	GND
BB41	SH_CT_B_PIN_MB_FSI0_DATA
BB42	GND
BB43	NA_PIN_P_A2_CK0_DAT_09_P
BB44	NA_PIN_P_A2_CK0_CLK_N
BB45	NA_PIN_P_A2_CK0_DAT_11_P
BB46	NA_PIN_P_A2_CK0_DAT_12_N
BB47	GND
BB48	NA_PIN_P_A1_CK0_DAT_22_P
BC01	MM_M1_P_PIN_CKC_DAT_11_P
BC02	MM_M1_P_PIN_CKC_DAT_10_N
BC03	MM_M1_P_PIN_CKC_CLK_N
BC04	GND
BC05	SH_PIN_P_M1_CKB_DAT_18_P
BC06	SH_SPARE_BG01
BC07	GND
BC08	MM_PIN_P_M1_CKD_DAT_03_P
BC09	MM_PIN_P_M1_CKD_DAT_03_N
BC10	MM_PIN_P_M1_CKD_DAT_04_P
BC11	MM_PIN_P_M1_CKD_DAT_04_N
BC12	GND
BC13	MM_PIN_P_M1_CKD_DAT_22_P
BC14	MM_PIN_P_M1_CKD_DAT_22_N
BC15	GND
BC16	GND
BC17	MM_PIN_P_M1_CKC_DAT_08_N
BC18	MM_PIN_P_M1_CKC_DAT_08_P
BC19	MM_PIN_P_M1_CKC_DAT_22_P
BC20	MM_PIN_P_M1_CKC_DAT_22_N
BC21	GND
BC22	GND
BC23	PV_CT_B_PIN_FSI2_DATA

Position	Net Name
BC24	PV_CT_P_PIN_FSI2_CLK
BC25	GND
BC26	TS_PIN_P_CT_TEST_LSSD_TE
BC27	GND
BC28	TS_PIN_P_CT_STBY_RESET_B
BC29	PV_PIN_P_CT_FSI_IN_ENA1
BC30	GND
BC31	PE_E1_P_PIN_CK0_DAT_00_P
BC32	PE_E1_P_PIN_CK0_DAT_00_N
BC33	PE_E1_P_PIN_CK0_DAT_04_N
BC34	PE_E1_P_PIN_CK0_DAT_04_P
BC35	GND
BC36	GND
BC37	PE_PIN_P_E1_CK0_DAT_03_N
BC38	PE_PIN_P_E1_CK0_DAT_03_P
BC39	PE_PIN_P_E1_CK0_DAT_06_N
BC40	PE_PIN_P_E1_CK0_DAT_06_P
BC41	GND
BC42	SH_CT_P_PIN_MB_FSI0_CLK
BC43	GND
BC44	NA_PIN_P_A2_CK0_CLK_P
BC45	NA_PIN_P_A2_CK0_DAT_13_N
BC46	NA_PIN_P_A2_CK0_DAT_12_P
BC47	NA_PIN_P_A2_CK0_DAT_14_N
BC48	GND
BD01	MM_M1_P_PIN_CKC_DAT_09_N
BD02	MM_M1_P_PIN_CKC_DAT_10_P
BD03	GND
BD04	SH_PIN_P_M1_CKB_DAT_07_P
BD05	SH_PIN_P_M1_CKB_DAT_11_P
BD06	GND
BD07	MM_PIN_P_M1_CKD_DAT_05_P
BD08	MM_PIN_P_M1_CKD_DAT_05_N
BD09	MM_PIN_P_M1_CKD_DAT_06_P
BD10	MM_PIN_P_M1_CKD_DAT_06_N
BD11	GND
BD12	MM_PIN_P_M1_CKD_DAT_20_P
BD13	MM_PIN_P_M1_CKD_DAT_20_N

Position	Net Name
BD14	MM_PIN_P_M1_CKD_DAT_23_P
BD15	MM_PIN_P_M1_CKD_DAT_23_N
BD16	GND
BD17	GND
BD18	MM_PIN_P_M1_CKC_DAT_20_N
BD19	MM_PIN_P_M1_CKC_DAT_20_P
BD20	MM_PIN_P_M1_CKC_DAT_21_N
BD21	MM_PIN_P_M1_CKC_DAT_21_P
BD22	GND
BD23	GND
BD24	PV_CT_P_PIN_FSI3_CLK
BD25	PV_CT_B_PIN_FSI3_DATA
BD26	GND
BD27	TS_PIN_P_CT_CARD_TEST
BD28	GND
BD29	GND
BD30	PV_PIN_P_CT_CHIP_ID1
BD31	GND
BD32	PE_E1_P_PIN_CK0_DAT_03_N
BD33	PE_E1_P_PIN_CK0_DAT_03_P
BD34	PE_E1_P_PIN_CK0_DAT_06_N
BD35	PE_E1_P_PIN_CK0_DAT_06_P
BD36	GND
BD37	GND
BD38	PE_PIN_P_E1_CK0_DAT_05_N
BD39	PE_PIN_P_E1_CK0_DAT_05_P
BD40	PE_PIN_P_E1_CK1_DAT_00_N
BD41	PE_PIN_P_E1_CK1_DAT_00_P
BD42	GND
BD43	GND
BD44	GND
BD45	NA_PIN_P_A2_CK0_DAT_13_P
BD46	NA_PIN_P_A2_CK0_DAT_18_N
BD47	NA_PIN_P_A2_CK0_DAT_14_P
BD48	NA_PIN_P_A2_CK0_DAT_15_N
BE01	MM_M1_P_PIN_CKC_DAT_09_P
BE02	GND
BE03	SH_PIN_P_M1_CKB_DAT_20_P

Position	Net Name
BE04	SH_PIN_P_M1_CKB_DAT_16_P
BE05	GND
BE06	MM_PIN_P_M1_CKD_DAT_07_P
BE07	MM_PIN_P_M1_CKD_DAT_07_N
BE08	MM_PIN_P_M1_CKD_DAT_12_P
BE09	MM_PIN_P_M1_CKD_DAT_12_N
BE10	GND
BE11	MM_PIN_P_M1_CKD_DAT_16_P
BE12	MM_PIN_P_M1_CKD_DAT_16_N
BE13	MM_PIN_P_M1_CKD_DAT_21_N
BE14	MM_PIN_P_M1_CKD_DAT_21_P
BE15	GND
BE16	MM_PIN_P_M1_CKC_DAT_01_P
BE17	MM_PIN_P_M1_CKC_DAT_01_N
BE18	GND
BE19	MM_PIN_P_M1_CKC_DAT_14_P
BE20	MM_PIN_P_M1_CKC_DAT_14_N
BE21	MM_PIN_P_M1_CKC_DAT_18_N
BE22	MM_PIN_P_M1_CKC_DAT_18_P
BE23	GND
BE24	GND
BE25	GND
BE26	GND
BE27	GND
BE28	PV_PIN_B_CT_FSP0_FSI_DATA
BE29	PV_PIN_P_CT_FSP0_FSI_CLK
BE30	GND
BE31	PE_E1_P_PIN_CK0_DAT_07_N
BE32	PE_E1_P_PIN_CK0_DAT_07_P
BE33	PE_E1_P_PIN_CK0_DAT_05_N
BE34	PE_E1_P_PIN_CK0_DAT_05_P
BE35	GND
BE36	GND
BE37	PE_PIN_P_E1_CK0_DAT_07_P
BE38	PE_PIN_P_E1_CK0_DAT_07_N
BE39	PE_PIN_P_E1_CK1_DAT_01_N
BE40	PE_PIN_P_E1_CK1_DAT_01_P
BE41	GND

Position	Net Name
BE42	GND
BE43	NA_PIN_P_A2_CK0_DAT_22_P
BE44	NA_PIN_P_A2_CK0_DAT_22_N
BE45	GND
BE46	NA_PIN_P_A2_CK0_DAT_18_P
BE47	NA_PIN_P_A2_CK0_DAT_16_N
BE48	NA_PIN_P_A2_CK0_DAT_15_P
BF01	GND
BF02	SH_PIN_P_M1_CKB_DAT_19_P
BF03	SH_PIN_P_M1_CKB_DAT_08_P
BF04	GND
BF05	MM_PIN_P_M1_CKD_DAT_08_N
BF06	MM_PIN_P_M1_CKD_DAT_08_P
BF07	MM_PIN_P_M1_CKD_DAT_11_P
BF08	MM_PIN_P_M1_CKD_DAT_11_N
BF09	GND
BF10	MM_PIN_P_M1_CKD_DAT_14_P
BF11	MM_PIN_P_M1_CKD_DAT_14_N
BF12	MM_PIN_P_M1_CKD_DAT_19_N
BF13	MM_PIN_P_M1_CKD_DAT_19_P
BF14	GND
BF15	MM_PIN_P_M1_CKC_DAT_00_P
BF16	MM_PIN_P_M1_CKC_DAT_00_N
BF17	MM_PIN_P_M1_CKC_DAT_04_P
BF18	MM_PIN_P_M1_CKC_DAT_04_N
BF19	GND
BF20	MM_PIN_P_M1_CKC_DAT_11_P
BF21	MM_PIN_P_M1_CKC_DAT_11_N
BF22	MM_PIN_P_M1_CKC_DAT_13_P
BF23	MM_PIN_P_M1_CKC_DAT_13_N
BF24	GND
BF25	MM_PIN_P_M1_CKC_DAT_17_N
BF26	MM_PIN_P_M1_CKC_DAT_17_P
BF27	GND
BF28	GND
BF29	PV_PIN_P_CT_FSI_SMD
BF30	PV_PIN_P_CT_CHIP_ID0
BF31	GND

Position	Net Name
BF32	PE_E1_P_PIN_CK1_DAT_01_P
BF33	PE_E1_P_PIN_CK1_DAT_01_N
BF34	PE_E1_P_PIN_CK1_DAT_00_N
BF35	PE_E1_P_PIN_CK1_DAT_00_P
BF36	GND
BF37	GND
BF38	PE_PIN_P_E1_CK1_DAT_03_P
BF39	PE_PIN_P_E1_CK1_DAT_03_N
BF40	PE_PIN_P_E1_CK1_DAT_02_N
BF41	PE_PIN_P_E1_CK1_DAT_02_P
BF42	GND
BF43	GND
BF44	NA_PIN_P_A2_CK0_DAT_21_P
BF45	NA_PIN_P_A2_CK0_DAT_21_N
BF46	GND
BF47	NA_PIN_P_A2_CK0_DAT_16_P
BF48	NA_PIN_P_A2_CK0_DAT_17_N
BG01	SH_PIN_P_M1_CKB_DAT_23_P
BG02	SH_PIN_P_M1_CKB_DAT_22_P
BG03	GND
BG04	MM_PIN_P_M1_CKD_DAT_09_P
BG05	MM_PIN_P_M1_CKD_DAT_09_N
BG06	MM_PIN_P_M1_CKD_CLK_P
BG07	MM_PIN_P_M1_CKD_CLK_N
BG08	GND
BG09	MM_PIN_P_M1_CKD_DAT_15_P
BG10	MM_PIN_P_M1_CKD_DAT_15_N
BG11	MM_PIN_P_M1_CKD_DAT_18_N
BG12	MM_PIN_P_M1_CKD_DAT_18_P
BG13	GND
BG14	SH_PIN_P_M1_CKB_DAT_17_P
BG15	GND
BG16	MM_PIN_P_M1_CKC_DAT_03_P
BG17	MM_PIN_P_M1_CKC_DAT_03_N
BG18	MM_PIN_P_M1_CKC_DAT_06_P
BG19	MM_PIN_P_M1_CKC_DAT_06_N
BG20	GND
BG21	MM_PIN_P_M1_CKC_DAT_10_P

Position	Net Name
BG22	MM_PIN_P_M1_CKC_DAT_10_N
BG23	MM_PIN_P_M1_CKC_DAT_12_P
BG24	MM_PIN_P_M1_CKC_DAT_12_N
BG25	GND
BG26	MM_PIN_P_M1_CKC_DAT_16_N
BG27	MM_PIN_P_M1_CKC_DAT_16_P
BG28	GND
BG29	GND
BG30	PE_E1_P_PIN_CK1_DAT_07_P
BG31	PE_E1_P_PIN_CK1_DAT_07_N
BG32	GND
BG33	PE_E1_P_PIN_CK1_DAT_05_P
BG34	PE_E1_P_PIN_CK1_DAT_05_N
BG35	PE_E1_P_PIN_CK1_DAT_03_N
BG36	PE_E1_P_PIN_CK1_DAT_03_P
BG37	GND
BG38	GND
BG39	PE_PIN_P_E1_CK1_DAT_07_N
BG40	PE_PIN_P_E1_CK1_DAT_07_P
BG41	PE_PIN_P_E1_CK1_DAT_05_P
BG42	PE_PIN_P_E1_CK1_DAT_05_N
BG43	GND
BG44	GND
BG45	NA_PIN_P_A2_CK0_DAT_20_P
BG46	NA_PIN_P_A2_CK0_DAT_20_N
BG47	GND
BG48	NA_PIN_P_A2_CK0_DAT_17_P
BH03	SH_PIN_P_M1_CKB_DAT_21_P
BH04	GND
BH05	MM_PIN_P_M1_CKD_DAT_10_P
BH06	MM_PIN_P_M1_CKD_DAT_10_N
BH07	GND
BH08	MM_PIN_P_M1_CKD_DAT_13_P
BH09	MM_PIN_P_M1_CKD_DAT_13_N
BH10	MM_PIN_P_M1_CKD_DAT_17_N
BH11	MM_PIN_P_M1_CKD_DAT_17_P
BH12	GND
BH13	GND

Position	Net Name
BH14	MM_PIN_P_M1_CKC_DAT_02_P
BH15	MM_PIN_P_M1_CKC_DAT_02_N
BH16	GND
BH17	MM_PIN_P_M1_CKC_DAT_05_P
BH18	MM_PIN_P_M1_CKC_DAT_05_N
BH19	MM_PIN_P_M1_CKC_DAT_09_P
BH20	MM_PIN_P_M1_CKC_DAT_09_N
BH21	GND
BH22	MM_PIN_P_M1_CKC_CLK_P
BH23	MM_PIN_P_M1_CKC_CLK_N
BH24	MM_PIN_P_M1_CKC_DAT_15_P
BH25	MM_PIN_P_M1_CKC_DAT_15_N
BH26	GND
BH27	MM_PIN_P_M1_CKC_DAT_19_N
BH28	MM_PIN_P_M1_CKC_DAT_19_P
BH29	GND
BH30	GND
BH31	PE_E1_P_PIN_CK1_DAT_06_P
BH32	PE_E1_P_PIN_CK1_DAT_06_N
BH33	GND
BH34	PE_E1_P_PIN_CK1_DAT_04_P
BH35	PE_E1_P_PIN_CK1_DAT_04_N
BH36	PE_E1_P_PIN_CK1_DAT_02_N
BH37	PE_E1_P_PIN_CK1_DAT_02_P
BH38	GND
BH39	GND
BH40	PE_PIN_P_E1_CK1_DAT_06_N
BH41	PE_PIN_P_E1_CK1_DAT_06_P
BH42	PE_PIN_P_E1_CK1_DAT_04_P
BH43	PE_PIN_P_E1_CK1_DAT_04_N
BH44	GND
BH45	GND
BH46	NA_PIN_P_A2_CK0_DAT_19_P
BH47	NA_PIN_P_A2_CK0_DAT_19_N
BH48	GND
C02	GND
C03	GND
C04	GND

Position	Net Name
C05	MM_PIN_P_M0_CKD_DAT_08_N
C06	MM_PIN_P_M0_CKD_DAT_08_P
C07	MM_PIN_P_M0_CKD_DAT_11_P
C08	MM_PIN_P_M0_CKD_DAT_11_N
C09	GND
C10	MM_PIN_P_M0_CKD_DAT_14_P
C11	MM_PIN_P_M0_CKD_DAT_14_N
C12	MM_PIN_P_M0_CKD_DAT_19_N
C13	MM_PIN_P_M0_CKD_DAT_19_P
C14	GND
C15	MM_PIN_P_M0_CKC_DAT_00_P
C16	MM_PIN_P_M0_CKC_DAT_00_N
C17	MM_PIN_P_M0_CKC_DAT_04_P
C18	MM_PIN_P_M0_CKC_DAT_04_N
C19	GND
C20	MM_PIN_P_M0_CKC_DAT_11_P
C21	MM_PIN_P_M0_CKC_DAT_11_N
C22	MM_PIN_P_M0_CKC_DAT_13_P
C23	MM_PIN_P_M0_CKC_DAT_13_N
C24	GND
C25	MM_PIN_P_M0_CKC_DAT_17_N
C26	MM_PIN_P_M0_CKC_DAT_17_P
C27	GND
C28	GND
C29	GND
C30	GND
C31	GND
C32	PE_E0_P_PIN_CK1_DAT_01_N
C33	PE_E0_P_PIN_CK1_DAT_01_P
C34	PE_E0_P_PIN_CK1_DAT_00_N
C35	PE_E0_P_PIN_CK1_DAT_00_P
C36	GND
C37	GND
C38	PE_PIN_P_E0_CK1_DAT_03_P
C39	PE_PIN_P_E0_CK1_DAT_03_N
C40	PE_PIN_P_E0_CK1_DAT_02_N
C41	PE_PIN_P_E0_CK1_DAT_02_P
C42	GND

Position	Net Name
C43	GND
C44	NA_A0_P_PIN_CK0_DAT_01_P
C45	NA_A0_P_PIN_CK0_DAT_01_N
C46	GND
C47	NA_A0_P_PIN_CK0_DAT_07_N
C48	NA_A0_P_PIN_CK0_DAT_05_N
D01	MM_M0_P_PIN_CKC_DAT_09_P
D02	GND
D03	GND
D04	GND
D05	GND
D06	MM_PIN_P_M0_CKD_DAT_07_P
D07	MM_PIN_P_M0_CKD_DAT_07_N
D08	MM_PIN_P_M0_CKD_DAT_12_P
D09	MM_PIN_P_M0_CKD_DAT_12_N
D10	GND
D11	MM_PIN_P_M0_CKD_DAT_16_P
D12	MM_PIN_P_M0_CKD_DAT_16_N
D13	MM_PIN_P_M0_CKD_DAT_21_N
D14	MM_PIN_P_M0_CKD_DAT_21_P
D15	GND
D16	MM_PIN_P_M0_CKC_DAT_01_P
D17	MM_PIN_P_M0_CKC_DAT_01_N
D18	GND
D19	MM_PIN_P_M0_CKC_DAT_14_P
D20	MM_PIN_P_M0_CKC_DAT_14_N
D21	MM_PIN_P_M0_CKC_DAT_18_N
D22	MM_PIN_P_M0_CKC_DAT_18_P
D23	GND
D24	GND
D25	GND
D26	GND
D27	GND
D28	GND
D29	GND
D30	GND
D31	PE_E0_P_PIN_CK0_DAT_07_N
D32	PE_E0_P_PIN_CK0_DAT_07_P

Position	Net Name
D33	PE_E0_P_PIN_CK0_DAT_05_N
D34	PE_E0_P_PIN_CK0_DAT_05_P
D35	GND
D36	GND
D37	PE_PIN_P_E0_CK0_DAT_07_N
D38	PE_PIN_P_E0_CK0_DAT_07_P
D39	PE_PIN_P_E0_CK1_DAT_01_N
D40	PE_PIN_P_E0_CK1_DAT_01_P
D41	GND
D42	GND
D43	NA_A0_P_PIN_CK0_DAT_00_N
D44	NA_A0_P_PIN_CK0_DAT_00_P
D45	GND
D46	NA_A0_P_PIN_CK0_DAT_08_N
D47	NA_A0_P_PIN_CK0_DAT_07_P
D48	NA_A0_P_PIN_CK0_DAT_09_N
E01	MM_M0_P_PIN_CKC_DAT_09_N
E02	MM_M0_P_PIN_CKC_DAT_10_P
E03	GND
E04	GND
E05	TS_CT_P_PIN_JTAG_TDO
E06	GND
E07	MM_PIN_P_M0_CKD_DAT_05_P
E08	MM_PIN_P_M0_CKD_DAT_05_N
E09	MM_PIN_P_M0_CKD_DAT_06_P
E10	MM_PIN_P_M0_CKD_DAT_06_N
E11	GND
E12	MM_PIN_P_M0_CKD_DAT_20_P
E13	MM_PIN_P_M0_CKD_DAT_20_N
E14	MM_PIN_P_M0_CKD_DAT_23_P
E15	MM_PIN_P_M0_CKD_DAT_23_N
E16	GND
E17	GND
E18	MM_PIN_P_M0_CKC_DAT_20_N
E19	MM_PIN_P_M0_CKC_DAT_20_P
E20	MM_PIN_P_M0_CKC_DAT_21_N
E21	MM_PIN_P_M0_CKC_DAT_21_P
E22	GND

Position	Net Name
E23	GND
E24	GND
E25	GND
E26	GND
E27	GND
E28	GND
E29	GND
E30	GND
E31	GND
E32	PE_E0_P_PIN_CK0_DAT_03_N
E33	PE_E0_P_PIN_CK0_DAT_03_P
E34	PE_E0_P_PIN_CK0_DAT_06_P
E35	PE_E0_P_PIN_CK0_DAT_06_N
E36	GND
E37	GND
E38	PE_PIN_P_E0_CK0_DAT_05_N
E39	PE_PIN_P_E0_CK0_DAT_05_P
E40	PE_PIN_P_E0_CK1_DAT_00_N
E41	PE_PIN_P_E0_CK1_DAT_00_P
E42	GND
E43	GND
E44	GND
E45	NA_A0_P_PIN_CK0_DAT_04_P
E46	NA_A0_P_PIN_CK0_DAT_08_P
E47	NA_A0_P_PIN_CK0_DAT_10_N
E48	NA_A0_P_PIN_CK0_DAT_09_P
F01	MM_M0_P_PIN_CKC_DAT_11_P
F02	MM_M0_P_PIN_CKC_DAT_10_N
F03	MM_M0_P_PIN_CKC_CLK_N
F04	GND
F05	GND
F06	TS_PIN_P_CT_JTAG_TDI
F07	GND
F08	MM_PIN_P_M0_CKD_DAT_03_P
F09	MM_PIN_P_M0_CKD_DAT_03_N
F10	MM_PIN_P_M0_CKD_DAT_04_P
F11	MM_PIN_P_M0_CKD_DAT_04_N
F12	GND

Position	Net Name
F13	MM_PIN_P_M0_CKD_DAT_22_P
F14	MM_PIN_P_M0_CKD_DAT_22_N
F15	GND
F16	GND
F17	MM_PIN_P_M0_CKC_DAT_08_N
F18	MM_PIN_P_M0_CKC_DAT_08_P
F19	MM_PIN_P_M0_CKC_DAT_22_P
F20	MM_PIN_P_M0_CKC_DAT_22_N
F21	GND
F22	GND
F23	GND
F24	GND
F25	GND
F26	GND
F27	TS_CT_P_PIN_AMX0_GSENSE
F28	GND
F29	GND
F30	GND
F31	PE_E0_P_PIN_CK0_DAT_01_N
F32	PE_E0_P_PIN_CK0_DAT_01_P
F33	PE_E0_P_PIN_CK0_DAT_04_N
F34	PE_E0_P_PIN_CK0_DAT_04_P
F35	GND
F36	GND
F37	PE_PIN_P_E0_CK0_DAT_03_N
F38	PE_PIN_P_E0_CK0_DAT_03_P
F39	PE_PIN_P_E0_CK0_DAT_06_P
F40	PE_PIN_P_E0_CK0_DAT_06_N
F41	GND
F42	GND
F43	GND
F44	NA_A0_P_PIN_CK0_DAT_06_N
F45	NA_A0_P_PIN_CK0_DAT_04_N
F46	NA_A0_P_PIN_CK0_DAT_11_N
F47	NA_A0_P_PIN_CK0_DAT_10_P
F48	GND
G01	MM_M0_P_PIN_CKC_DAT_11_N
G02	MM_M0_P_PIN_CKC_DAT_12_P

Position	Net Name
G03	MM_M0_P_PIN_CKC_CLK_P
G04	MM_M0_P_PIN_CKC_DAT_07_N
G05	GND
G06	GND
G07	TS_PIN_P_CT_JTAG_TMS
G08	GND
G09	MM_PIN_P_M0_CKD_DAT_01_N
G10	MM_PIN_P_M0_CKD_DAT_01_P
G11	MM_PIN_P_M0_CKD_DAT_02_P
G12	MM_PIN_P_M0_CKD_DAT_02_N
G13	GND
G14	GND
G15	GND
G16	MM_PIN_P_M0_CKC_DAT_07_N
G17	MM_PIN_P_M0_CKC_DAT_07_P
G18	MM_PIN_P_M0_CKC_DAT_23_P
G19	MM_PIN_P_M0_CKC_DAT_23_N
G20	GND
G21	GND
G22	GND
G23	GND
G24	GND
G25	GND
G26	GND
G27	TS_CT_P_PIN_AMX0_VSENSE
G28	GND
G29	GND
G30	PE_E0_P_PIN_CK0_DAT_00_P
G31	PE_E0_P_PIN_CK0_DAT_00_N
G32	PE_E0_P_PIN_CK0_DAT_02_P
G33	PE_E0_P_PIN_CK0_DAT_02_N
G34	GND
G35	GND
G36	PE_PIN_P_E0_CK0_DAT_01_N
G37	PE_PIN_P_E0_CK0_DAT_01_P
G38	PE_PIN_P_E0_CK0_DAT_04_N
G39	PE_PIN_P_E0_CK0_DAT_04_P
G40	GND

Position	Net Name
G41	GND
G42	GND
G43	NA_A0_P_PIN_CK0_DAT_14_N
G44	NA_A0_P_PIN_CK0_DAT_06_P
G45	NA_A0_P_PIN_CK0_DAT_12_N
G46	NA_A0_P_PIN_CK0_DAT_11_P
G47	GND
G48	NA_A0_P_PIN_CK0_CLK_N
H01	GND
H02	MM_M0_P_PIN_CKC_DAT_12_N
H03	MM_M0_P_PIN_CKC_DAT_08_P
H04	MM_M0_P_PIN_CKC_DAT_07_P
H05	MM_M0_P_PIN_CKC_DAT_05_N
H06	GND
H07	GND
H08	TS_CT_P_PIN_PROBE1_N
H09	GND
H10	MM_PIN_P_M0_CKD_DAT_00_P
H11	MM_PIN_P_M0_CKD_DAT_00_N
H12	GND
H13	GND
H14	GND
H15	GND
H16	GND
H17	GND
H18	TS_CT_P_PIN_M0_T_PLLHFC_MKERF_N
H19	GND
H20	GND
H21	GND
H22	GND
H23	GND
H24	GND
H25	TS_CT_P_PIN_M0_C_MKERF_P
H26	GND
H27	GND
H28	PV_CT_P_PIN_SPIVID0_SCLK
H29	PV_CT_P_PIN_SPIVID0_MOSI
H30	GND

Position	Net Name
H31	GND
H32	GND
H33	PE_CT_P_PIN_E0_PERST0_B
H34	GND
H35	PE_PIN_P_E0_CK0_DAT_00_N
H36	PE_PIN_P_E0_CK0_DAT_00_P
H37	PE_PIN_P_E0_CK0_DAT_02_N
H38	PE_PIN_P_E0_CK0_DAT_02_P
H39	GND
H40	GND
H41	GND
H42	NA_A1_P_PIN_CK0_DAT_01_N
H43	NA_A0_P_PIN_CK0_DAT_14_P
H44	NA_A0_P_PIN_CK0_DAT_20_N
H45	NA_A0_P_PIN_CK0_DAT_12_P
H46	GND
H47	NA_A0_P_PIN_CK0_DAT_13_N
H48	NA_A0_P_PIN_CK0_CLK_P
J01	MM_M0_P_PIN_CKC_DAT_14_P
J02	GND
J03	MM_M0_P_PIN_CKC_DAT_08_N
J04	MM_M0_P_PIN_CKC_DAT_06_N
J05	MM_M0_P_PIN_CKC_DAT_05_P
J06	MM_M0_P_PIN_CKC_DAT_03_N
J07	GND
J08	TS_CT_P_PIN_PROBE1_P
J09	GND
J10	GND
J11	GND
J12	GND
J13	GND
J14	GND
J15	GND
J16	GND
J17	TS_CT_P_PIN_M0_PLL_ANATS
J18	TS_CT_P_PIN_M0_T_PLLHFC_MKERF_P
J19	GND
J20	PV_PIN_P_CT_M0_TERMREF_P

Position	Net Name
J21	PV_PIN_P_CT_M0_TERMREF_N
J22	GND
J23	GND
J24	GND
J25	TS_CT_P_PIN_M0_C_MKERF_N
J26	GND
J27	GND
J28	PV_CT_P_PIN_SPIVID0_CS
J29	GND
J30	PV_PIN_P_CT_SPIVID0_MISO
J31	GND
J32	PE_PIN_P_CT_E0_PRSNT1_B
J33	PE_PIN_P_CT_E0_PRSNT0_B
J34	PE_CT_P_PIN_E0_PERST1_B
J35	GND
J36	GND
J37	TS_CT_P_PIN_VIO_VSENSE
J38	GND
J39	GND
J40	GND
J41	NA_A1_P_PIN_CK0_DAT_03_N
J42	NA_A1_P_PIN_CK0_DAT_01_P
J43	NA_A1_P_PIN_CK0_DAT_00_N
J44	NA_A0_P_PIN_CK0_DAT_20_P
J45	GND
J46	NA_A0_P_PIN_CK0_DAT_17_N
J47	NA_A0_P_PIN_CK0_DAT_13_P
J48	NA_A0_P_PIN_CK0_DAT_15_N
K01	MM_M0_P_PIN_CKC_DAT_14_N
K02	MM_M0_P_PIN_CKC_DAT_15_P
K03	GND
K04	MM_M0_P_PIN_CKC_DAT_06_P
K05	MM_M0_P_PIN_CKC_DAT_04_N
K06	MM_M0_P_PIN_CKC_DAT_03_P
K07	MM_M0_P_PIN_CKC_DAT_01_N
K08	GND
K09	GND
K10	MM_CT_P_PIN_MB_NEST_REFCLK3_N

Position	Net Name
K11	GND
K12	MM_CT_P_PIN_MB_MEM_REFCLK3_N
K13	#VIO_1P10
K14	GND
K15	#VIO_1P10
K16	GND
K17	#VIO_1P10
K18	GND
K19	#VIO_1P10
K20	GND
K21	#VIO_1P10
K22	GND
K23	#VIO_1P10
K24	GND
K25	#VIO_1P10
K26	GND
K27	#VIO_1P10
K28	GND
K29	#VIO_1P10
K30	GND
K31	#VIO_1P10
K32	GND
K33	#VIO_1P10
K34	GND
K35	#VIO_1P10
K36	GND
K37	TS_CT_P_PIN_VIO_VPCI_GSENSE
K38	GND
K39	GND
K40	NA_A1_P_PIN_CK0_DAT_05_N
K41	NA_A1_P_PIN_CK0_DAT_03_P
K42	NA_A1_P_PIN_CK0_DAT_02_N
K43	NA_A1_P_PIN_CK0_DAT_00_P
K44	GND
K45	NA_A0_P_PIN_CK0_DAT_22_P
K46	NA_A0_P_PIN_CK0_DAT_17_P
K47	NA_A0_P_PIN_CK0_DAT_16_N

Position	Net Name
K48	NA_A0_P_PIN_CK0_DAT_15_P
L01	GND
L02	MM_M0_P_PIN_CKC_DAT_15_N
L03	MM_M0_P_PIN_CKC_DAT_16_P
L04	GND
L05	MM_M0_P_PIN_CKC_DAT_04_P
L06	MM_M0_P_PIN_CKC_DAT_02_N
L07	MM_M0_P_PIN_CKC_DAT_01_P
L08	GND
L09	MM_CT_P_PIN_MB_NEST_REFCLK2_P
L10	MM_CT_P_PIN_MB_NEST_REFCLK3_P
L11	MM_CT_P_PIN_MB_MEM_REFCLK2_P
L12	MM_CT_P_PIN_MB_MEM_REFCLK3_P
L13	GND
L14	#VIO_1P10
L15	GND
L16	#VIO_1P10
L17	GND
L18	#VIO_1P10
L19	GND
L20	#VIO_1P10
L21	GND
L22	#VIO_1P10
L23	GND
L24	#VIO_1P10
L25	GND
L26	#VIO_1P10
L27	GND
L28	#VIO_1P10
L29	GND
L30	#VIO_1P10
L31	GND
L32	#VIO_1P10
L33	GND
L34	#VIO_1P10
L35	#VPCI_1P20

Position	Net Name
L36	#VIO_1P10
L37	TS_CT_P_PIN_VPCI0_VSENSE
L38	GND
L39	NA_A1_P_PIN_CK0_DAT_08_N
L40	NA_A1_P_PIN_CK0_DAT_05_P
L41	NA_A1_P_PIN_CK0_DAT_06_N
L42	NA_A1_P_PIN_CK0_DAT_02_P
L43	GND
L44	NA_A1_P_PIN_CK0_DAT_04_N
L45	NA_A0_P_PIN_CK0_DAT_22_N
L46	NA_A0_P_PIN_CK0_DAT_19_N
L47	NA_A0_P_PIN_CK0_DAT_16_P
L48	GND
M01	MM_M0_P_PIN_CKD_DAT_16_P
M02	GND
M03	MM_M0_P_PIN_CKC_DAT_16_N
M04	MM_M0_P_PIN_CKC_DAT_13_N
M05	GND
M06	MM_M0_P_PIN_CKC_DAT_02_P
M07	MM_M0_P_PIN_CKC_DAT_00_N
M08	GND
M09	MM_CT_P_PIN_MB_NEST_REFCLK2_N
M10	GND
M11	MM_CT_P_PIN_MB_MEM_REFCLK2_N
M12	GND
M13	#VIO_1P10
M14	GND
M15	#VDD_0P89
M16	GND
M17	#VDD_0P89
M18	GND
M19	#VDD_0P89
M20	TS_CT_P_PIN_VCSCORE0_VSENSE
M21	#VDD_0P89
M22	GND
M23	#VDD_0P89

Position	Net Name
M24	TS_CT_P_PIN_GDECO0_GSENSE
M25	#VIO_1P10
M26	GND
M27	#VDD_0P89
M28	GND
M29	#VDD_0P89
M30	GND
M31	#VDD_0P89
M32	GND
M33	#VDD_0P89
M34	GND
M35	#VIO_1P10
M36	#VPCI_1P20
M37	PV_PIN_P_CT_E0_TERMREF_P
M38	GND
M39	NA_A1_P_PIN_CK0_DAT_08_P
M40	NA_A1_P_PIN_CK0_DAT_10_N
M41	NA_A1_P_PIN_CK0_DAT_06_P
M42	GND
M43	NA_A1_P_PIN_CK0_DAT_07_N
M44	NA_A1_P_PIN_CK0_DAT_04_P
M45	NA_A0_P_PIN_CK0_DAT_21_N
M46	NA_A0_P_PIN_CK0_DAT_19_P
M47	GND
M48	NA_A0_P_PIN_CK0_DAT_18_N
N01	MM_M0_P_PIN_CKD_DAT_16_N
N02	MM_M0_P_PIN_CKD_DAT_14_P
N03	GND
N04	MM_M0_P_PIN_CKC_DAT_13_P
N05	MM_M0_P_PIN_CKD_DAT_15_P
N06	GND
N07	MM_M0_P_PIN_CKC_DAT_00_P
N08	GND
N09	GND
N10	PV_CT_M_PIN_SEEPROM1_CLK
N11	GND
N12	GND
N13	GND

Position	Net Name
N14	#VDD_0P89
N15	GND
N16	#VDD_0P89
N17	GND
N18	TS_CT_P_PIN_DTS2_MONI
N19	#VCS_0P97
N20	TS_CT_P_PIN_GDSCORE0_GSENSE
N21	GND
N22	#VCS_0P97
N23	TS_CT_P_PIN_VDDECO0_VSENSE
N24	TS_CT_P_PIN_VCSECO0_VSENSE
N25	GND
N26	#VDD_0P89
N27	#VCS_0P97
N28	#VDD_0P89
N29	GND
N30	#VCS_0P97
N31	GND
N32	#VDD_0P89
N33	GND
N34	#VDD_0P89
N35	#VPCI_1P20
N36	GND
N37	PV_PIN_P_CT_E0_TERMREF_N
N38	GND
N39	GND
N40	NA_A1_P_PIN_CK0_DAT_10_P
N41	GND
N42	NA_A1_P_PIN_CK0_DAT_09_N
N43	NA_A1_P_PIN_CK0_DAT_07_P
N44	NA_A1_P_PIN_CK0_DAT_11_N
N45	NA_A0_P_PIN_CK0_DAT_21_P
N46	GND
N47	NA_A2_P_PIN_CK0_DAT_03_N
N48	NA_A0_P_PIN_CK0_DAT_18_P
P01	MM_M0_P_PIN_CKD_DAT_10_P
P02	MM_M0_P_PIN_CKD_DAT_14_N
P03	MM_M0_P_PIN_CKD_DAT_13_P
P04	GND
P05	MM_M0_P_PIN_CKD_DAT_15_N
P06	MM_M0_P_PIN_CKD_DAT_06_N
P07	GND
P08	MM_M0_P_PIN_CKD_DAT_01_N
P09	GND
P10	PV_CT_M_PIN_SEEPROM1_DATA
P11	MM_PIN_P_CT_M0_FAULT_D_N
P12	TS_PIN_P_CT_EXT_TRIGGER_TCK
P13	#VIO_1P10
P14	GND
P15	#VDD_0P89
P16	GND
P17	#VDD_0P89
P18	GND
P19	#VDD_0P89
P20	GND
P21	#VDD_0P89
P22	GND
P23	#VDD_0P89
P24	#VIO_1P10
P25	#VDD_0P89
P26	GND
P27	#VDD_0P89
P28	GND
P29	#VDD_0P89
P30	GND
P31	#VDD_0P89
P32	GND
P33	#VDD_0P89
P34	GND
P35	#VIO_1P10
P36	#VPCI_1P20
P37	TS_CT_P_PIN_PE0_PLL_ANATST
P38	TS_CT_P_PIN_A_PLLHFC_MKERF_N
P39	GND
P40	GND
P41	NA_A1_P_PIN_CK0_DAT_12_N
P42	NA_A1_P_PIN_CK0_DAT_09_P
P43	NA_A1_P_PIN_CK0_CLK_N
P44	NA_A1_P_PIN_CK0_DAT_11_P
P45	GND
P46	NA_A2_P_PIN_CK0_DAT_02_N
P47	NA_A2_P_PIN_CK0_DAT_03_P
P48	NA_A2_P_PIN_CK0_DAT_05_N
R01	MM_M0_P_PIN_CKD_DAT_10_N
R02	MM_M0_P_PIN_CKD_DAT_12_P
R03	MM_M0_P_PIN_CKD_DAT_13_N
R04	MM_M0_P_PIN_CKD_DAT_11_P
R05	GND
R06	MM_M0_P_PIN_CKD_DAT_06_P
R07	MM_M0_P_PIN_CKD_DAT_03_N
R08	MM_M0_P_PIN_CKD_DAT_01_P
R09	MM_M0_P_PIN_CKD_DAT_00_N
R10	GND
R11	GND
R12	GND
R13	GND
R14	TS_CT_P_PIN_VDDCORE0_VSENSE
R15	GND
R16	#VDD_0P89
R17	GND
R18	#VDD_0P89
R19	#VCS_0P97
R20	#VDD_0P89
R21	GND
R22	#VCS_0P97
R23	GND
R24	#VDD_0P89
R25	GND
R26	#VDD_0P89
R27	#VCS_0P97
R28	#VDD_0P89
R29	GND

Position	Net Name
R30	#VCS_0P97
R31	GND
R32	#VDD_0P89
R33	GND
R34	#VDD_0P89
R35	#VPCI_1P20
R36	GND
R37	GND
R38	TS_CT_P_PIN_A_PLLHFC_MKERF_P
R39	GND
R40	NA_A1_P_PIN_CK0_DAT_13_N
R41	NA_A1_P_PIN_CK0_DAT_12_P
R42	NA_A1_P_PIN_CK0_DAT_15_N
R43	NA_A1_P_PIN_CK0_CLK_P
R44	GND
R45	NA_A2_P_PIN_CK0_DAT_01_N
R46	NA_A2_P_PIN_CK0_DAT_02_P
R47	NA_A2_P_PIN_CK0_DAT_06_N
R48	NA_A2_P_PIN_CK0_DAT_05_P
T01	GND
T02	MM_M0_P_PIN_CKD_DAT_12_N
T03	MM_M0_P_PIN_CKD_DAT_09_P
T04	MM_M0_P_PIN_CKD_DAT_11_N
T05	MM_M0_P_PIN_CKD_DAT_08_P
T06	GND
T07	MM_M0_P_PIN_CKD_DAT_03_P
T08	MM_M0_P_PIN_CKD_DAT_02_N
T09	MM_M0_P_PIN_CKD_DAT_00_P
T10	GND
T11	PV_PIN_P_CT_OSC0_C1_REFCLK_P
T12	PV_PIN_P_CT_OSC0_C1_REFCLK_N
T13	#VIO_1P10
T14	TS_CT_P_PIN_GDDCORE0_GSENSE
T15	#VDD_0P89
T16	GND
T17	#VDD_0P89

Position	Net Name
T18	GND
T19	#VDD_0P89
T20	GND
T21	#VDD_0P89
T22	GND
T23	#VDD_0P89
T24	TS_CT_P_PIN_EX0_GSENSE
T25	#VIO_1P10
T26	GND
T27	#VDD_0P89
T28	GND
T29	#VDD_0P89
T30	GND
T31	#VDD_0P89
T32	GND
T33	#VDD_0P89
T34	GND
T35	#VIO_1P10
T36	#VPCI_1P20
T37	TS_CT_P_PIN_A_PLL_ANATST
T38	GND
T39	NA_A1_P_PIN_CK0_DAT_14_N
T40	NA_A1_P_PIN_CK0_DAT_13_P
T41	NA_A1_P_PIN_CK0_DAT_18_N
T42	NA_A1_P_PIN_CK0_DAT_15_P
T43	GND
T44	NA_A2_P_PIN_CK0_DAT_00_N
T45	NA_A2_P_PIN_CK0_DAT_01_P
T46	NA_A2_P_PIN_CK0_DAT_04_N
T47	NA_A2_P_PIN_CK0_DAT_06_P
T48	GND
U01	MM_M0_P_PIN_CKD_DAT_07_N
U02	GND
U03	MM_M0_P_PIN_CKD_DAT_09_N
U04	MM_M0_P_PIN_CKD_CLK_N
U05	MM_M0_P_PIN_CKD_DAT_08_N
U06	MM_M0_P_PIN_CKD_DAT_05_N
U07	GND

Position	Net Name
U08	MM_M0_P_PIN_CKD_DAT_02_P
U09	GND
U10	GND
U11	GND
U12	GND
U13	GND
U14	#VDD_0P89
U15	GND
U16	#VDD_0P89
U17	GND
U18	#VDD_0P89
U19	GND
U20	#VDD_0P89
U21	GND
U22	#VDD_0P89
U23	TS_CT_P_PIN_VCSEX0_VSENSE
U24	TS_CT_P_PIN_VDDEX0_VSENSE
U25	GND
U26	#VDD_0P89
U27	GND
U28	#VDD_0P89
U29	GND
U30	#VDD_0P89
U31	GND
U32	#VDD_0P89
U33	GND
U34	#VDD_0P89
U35	GND
U36	#VIO_1P10
U37	GND
U38	PV_PIN_P_CT_A_TERMREF_P
U39	NA_A1_P_PIN_CK0_DAT_14_P
U40	NA_A1_P_PIN_CK0_DAT_17_N
U41	NA_A1_P_PIN_CK0_DAT_18_P
U42	GND
U43	NA_A1_P_PIN_CK0_DAT_20_N
U44	NA_A2_P_PIN_CK0_DAT_00_P
U45	NA_A2_P_PIN_CK0_DAT_07_N

Position	Net Name
U46	NA_A2_P_PIN_CK0_DAT_04_P
U47	GND
U48	NA_A2_P_PIN_CK0_DAT_08_N
V01	MM_M0_P_PIN_CKD_DAT_07_P
V02	GND
V03	GND
V04	MM_M0_P_PIN_CKD_CLK_P
V05	GND
V06	MM_M0_P_PIN_CKD_DAT_05_P
V07	MM_M0_P_PIN_CKD_DAT_04_N
V08	GND
V09	MM_PIN_P_CT_M0_FAULT_C_N
V10	PV_PIN_P_CT_OSC0_TODREFCLK
V11	GND
V12	NC_VDD
V13	#VIO_1P10
V14	GND
V15	#VDD_0P89
V16	GND
V17	#VDD_0P89
V18	GND
V19	#VCS_0P97
V20	GND
V21	#VDD_0P89
V22	#VCS_0P97
V23	#VDD_0P89
V24	#VIO_1P10
V25	#VDD_0P89
V26	GND
V27	#VCS_0P97
V28	GND
V29	#VDD_0P89
V30	#VCS_0P97
V31	#VDD_0P89
V32	GND
V33	#VDD_0P89
V34	GND
V35	GND

Position	Net Name
V36	#VIO_1P10
V37	PV_PIN_P_CT_SPIADC_MISO
V38	PV_PIN_P_CT_A_TERMREF_N
V39	NA_A1_P_PIN_CK0_DAT_16_N
V40	NA_A1_P_PIN_CK0_DAT_17_P
V41	GND
V42	NA_A1_P_PIN_CK0_DAT_22_N
V43	NA_A1_P_PIN_CK0_DAT_20_P
V44	NA_A2_P_PIN_CK0_DAT_09_N
V45	NA_A2_P_PIN_CK0_DAT_07_P
V46	GND
V47	NA_A2_P_PIN_CK0_DAT_10_N
V48	NA_A2_P_PIN_CK0_DAT_08_P
W01	GND
W02	GND
W03	GND
W04	GND
W05	GND
W06	GND
W07	MM_M0_P_PIN_CKD_DAT_04_P
W08	GND
W09	GND
W10	GND
W11	NC_VDD
W12	NC_VDD
W13	GND
W14	#VDD_0P89
W15	GND
W16	#VDD_0P89
W17	GND
W18	#VDD_0P89
W19	GND
W20	#VDD_0P89
W21	GND
W22	#VDD_0P89
W23	GND
W24	#VDD_0P89
W25	GND

Position	Net Name
W26	#VDD_0P89
W27	GND
W28	#VDD_0P89
W29	GND
W30	#VDD_0P89
W31	GND
W32	#VDD_0P89
W33	GND
W34	#VDD_0P89
W35	#VIO_1P10
W36	GND
W37	GND
W38	GND
W39	NA_A1_P_PIN_CK0_DAT_16_P
W40	GND
W41	NA_A1_P_PIN_CK0_DAT_19_N
W42	NA_A1_P_PIN_CK0_DAT_22_P
W43	NA_A2_P_PIN_CK0_DAT_13_N
W44	NA_A2_P_PIN_CK0_DAT_09_P
W45	GND
W46	NA_A2_P_PIN_CK0_DAT_11_N
W47	NA_A2_P_PIN_CK0_DAT_10_P
W48	NA_A2_P_PIN_CK0_CLK_N
Y01	NC_VDD
Y02	NC_VDD
Y03	NC_VDD
Y04	NC_VDD
Y05	NC_VDD
Y06	NC_VDD
Y07	GND
Y08	GND
Y09	NC_VDD
Y10	NC_VDD
Y11	NC_VDD
Y12	NC_VDD
Y13	#VIO_1P10
Y14	GND
Y15	#VDD_0P89

Position	Net Name
Y16	GND
Y17	#VDD_0P89
Y18	GND
Y19	#VCS_0P97
Y20	GND
Y21	#VDD_0P89
Y22	#VCS_0P97
Y23	#VDD_0P89
Y24	GND
Y25	#VIO_1P10
Y26	GND
Y27	#VCS_0P97
Y28	GND
Y29	#VDD_0P89
Y30	#VCS_0P97
Y31	#VDD_0P89
Y32	GND
Y33	#VDD_0P89
Y34	GND
Y35	GND
Y36	#VIO_1P10
Y37	PV_CT_P_PIN_SPIADC_MOSI
Y38	GND
Y39	GND
Y40	GND
Y41	NA_A1_P_PIN_CK0_DAT_19_P
Y42	NA_A1_P_PIN_CK0_DAT_21_N
Y43	NA_A2_P_PIN_CK0_DAT_13_P
Y44	GND
Y45	NA_A2_P_PIN_CK0_DAT_16_N
Y46	NA_A2_P_PIN_CK0_DAT_11_P
Y47	NA_A2_P_PIN_CK0_DAT_12_N
Y48	NA_A2_P_PIN_CK0_CLK_P

Glossary

AES	Advanced Encryption Standard
ASIC	Application-specific integrated circuit
BIST	Built-in self-test
BMC	Baseboard management control
BR	Branch register unit
CAI	Coherent accelerator
CMOS	Complementary metal–oxide–semiconductor
CPM	Critical path monitor
CR	Condition register unit
DDR	Double data rate
DFE	Decision feedback equalizer
DFU	Decimal floating-point unit
DIMM	Dual in-line memory module
DMA	Direct memory attach
DMI	Differential memory interface
DRAM	Dynamic random access memory
DTS	Digital thermal sensor
ECO	Extended cache option
ECID	Electronic chip identification
ECRC	End-to-end CRC
EDI	Elastic differential I/O
EEH	Enhance error handling
EEPROM	Electrically erasable programmable read-only memory
EFK	East Fishkill
EI4	Elastic interface 4
FC PLGA	Flip-chip plastic land grid array
FIFO	First-in, first-out
FSI	Flexible service interface

FXU	Fixed-point units
GFW	Global firmware
HCSL	Host clock signal level
HSS	High-speed serial
I2C	Inter-integrated circuit
IFU	Instruction fetch units
JTAG	Joint Test Action Group
LCB	Logon control block
LED	Light-emitting diode
LGA	Land grid array
LPAR	Logical partition
LPC	Low pin count bus or lowest point of coherency
LPST	Local Pstate table
LSI	Level signalled interrup
LSSD	Level-sensitive scan design
LSU	Load store units
MPG	Multi-protocol gateway
MPUL	most-positive up level
MSI	Message signalled interrup
OCC	On-chip controller
OEM	Original equipment manufacturer
PAPR	Power Architecture Platform Reference
PCIe	Peripheral Component Interconnect Express
PE	Partitionable endpoints
PEC	PCI Express controller
PLL	Phase-locked loop
PMC	Power management control
PPM	Parts per million
PVR	Processor Version Register

RC	Root complex
SBE	Self-boot engine
SCM	Single-chip module
SCOM	Scan communications
SEEPROM	Serial electrically erasable programmable read-only memory
SHA	Secure Hash Algorithm
SOI	Silicon on insulator
SPI	Serial peripheral interconnect
SRAM	Static random access memory
SVIC	Special, vertical interconnect channel
TCE	Translation control entry
TDP	Thermal design point
TLP	Transaction layer packet
TPM	Trusted platform module
UPS	Uninterrupted power system
VPD	Vital product data
VLE	Variable length encoding
VRM	Voltage regulator module